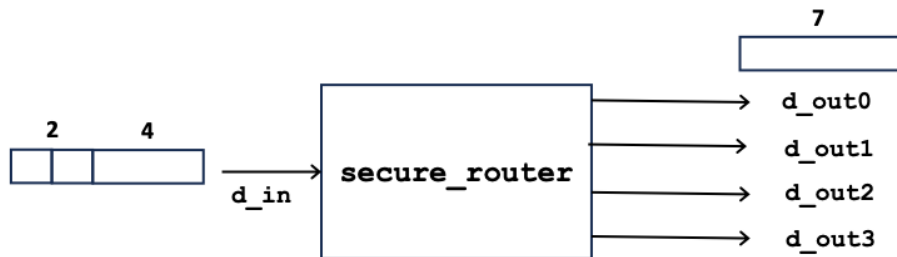


Indian Institute of Technology Kharagpur
Department of Computer Science and Engineering
Computer Organization and Architecture Laboratory

Verilog Assignment 3
27.08.2024

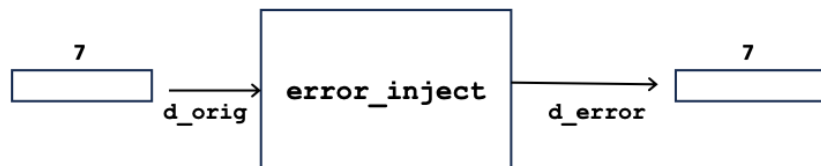
Verilog Assignment: Structural Modeling for Routing and Error Correction

- a) Write a Verilog module for single-bit error correcting router module **secure_router**, as shown in the diagram below:

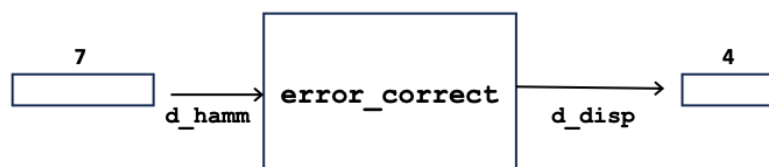


The module takes a 6-bit input **d_in**, where the first 2-bits indicate the output port number, and the last 4-bits indicate data. Using Hamming code for single-bit error correction, the 4-bit data input is converted to a 7-bit Hamming-coded data output, and is sent over one of the output ports depending on the first 2-bits of **d_in**.

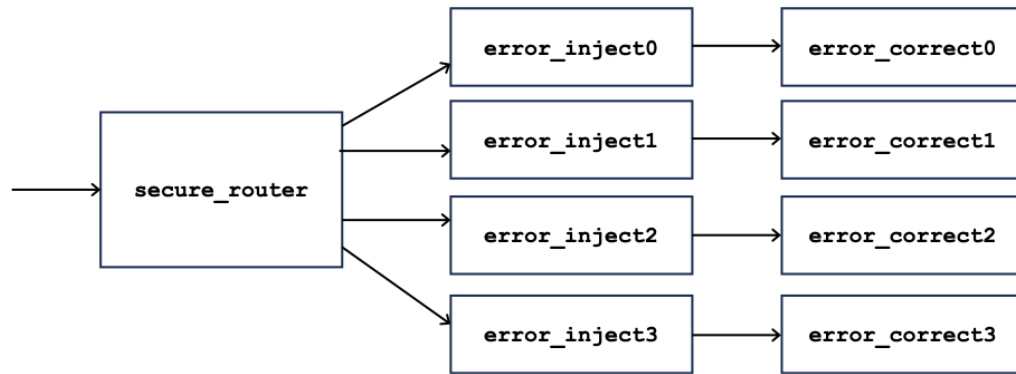
- b) Write a Verilog module **error_inject**, as shown in the diagram below, which takes a 7-bit data as input, injects a single bit error in the data, and sends it to the 7-bit output port.



- c) Write a Verilog module **error_correct**, as shown in the diagram below, which takes a 7-bit Hamming-coded data as input, corrects single-bit errors (if any), and sends the corrected 4-bit data to the output port.



- d) Write a top-level Verilog module as shown below, which instantiates the various Verilog modules as indicated.



- e) Write a test bench to simulate the operation of the design and verify its correctness. Apply various 6-bit inputs to the **secure_router** module, so that the data gets routed to various output ports.
- f) Generate the bit-map file, download it on the FPGA board, and demonstrate the working of the circuit. The outputs from the **error_correct** modules must be displayed in suitable fashion.

Assume that all circuit operations are carried out in synchronism with a clock (not shown). Make relevant assumptions where necessary.