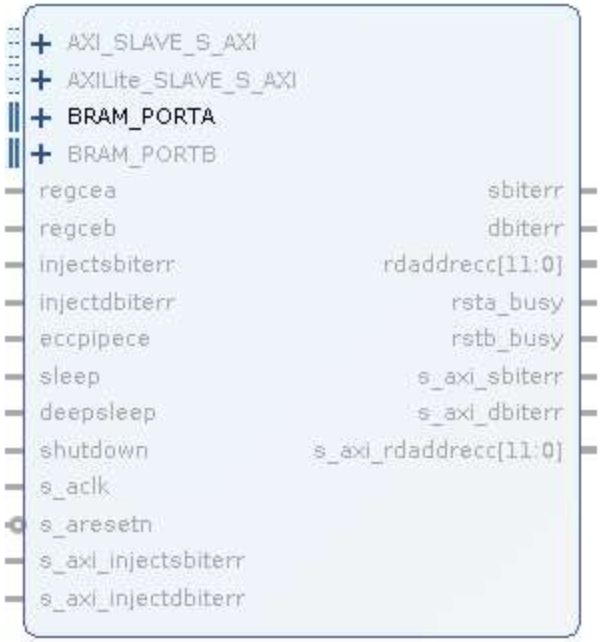
Block Memory Generator (8.4)

Documentation | IP Location | Switch to Defaults

IP Symbol | Power Estimation

Show disabled ports



Component Name: blk_mem_gen_0

Basic | Port A Options | Other Options | Summary

Interface Type: Native

Memory Type: Single Port RAM

Generate address interface with 32 bits

Common Clock

ECC Options

ECC Type: No ECC

Error Injection Pins: Single Bit Error Injection

Write Enable

Byte Write Enable

Byte Size (bits): 9

Algorithm Options

Defines the algorithm used to concatenate the block RAM primitives.
Refer datasheet for more information.

Algorithm: Minimum Area

Primitive: 8kx2

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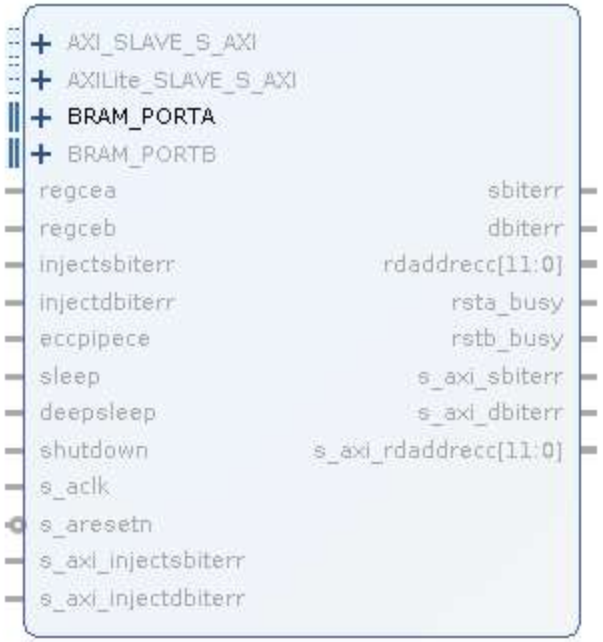

Component Name: blk_mem_gen_0

Basic | Port A Options | Other Options | Summary

Memory Size

Write Width: 32 — Range: 1 to 4608 (bits)

Read Width: 32

Write Depth: 4096 — Range: 2 to 1048576

Read Depth: 4096

Operating Mode: Write First

Enable Port Type: Use ENA Pin

Port A Optional Output Registers

- [ ] Primitives Output Register
- [ ] Core Output Register
- [ ] SoftECC Input Register
- [ ] REGCEA Pin

Port A Output Reset Options

- [ ] RSTA Pin (set/reset pin)

Output Reset Value (Hex): 0

- [ ] Reset Memory Latch

Reset Priority: CE (Latch or Register Enable)

READ Address Change A

- [ ] Read Address Change A

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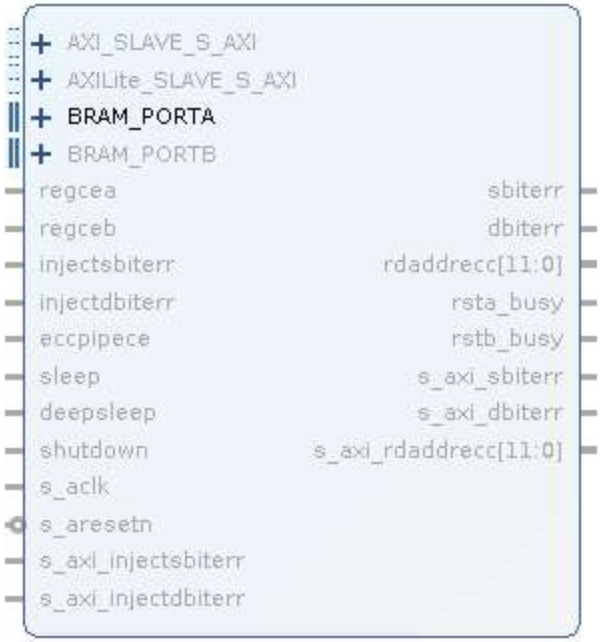

Component Name: blk_mem_gen_0

Basic | Port A Options | Other Options | Summary

Pipeline Stages within Mux: 0 — Mux Size: 1x1

Memory Initialization

- [x] Load Init File

Coe File: ../../../../Desktop/instruction_mem.coe — Browse | Edit

- [x] Fill Remaining Memory Locations

Remaining Memory Locations (Hex): 0

Structural/UniSim Simulation Model Options

Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.

Collision Warnings: All

Behavioral Simulation Model Options

- [ ] Disable Collision Warnings
- [ ] Disable Out of Range Warnings

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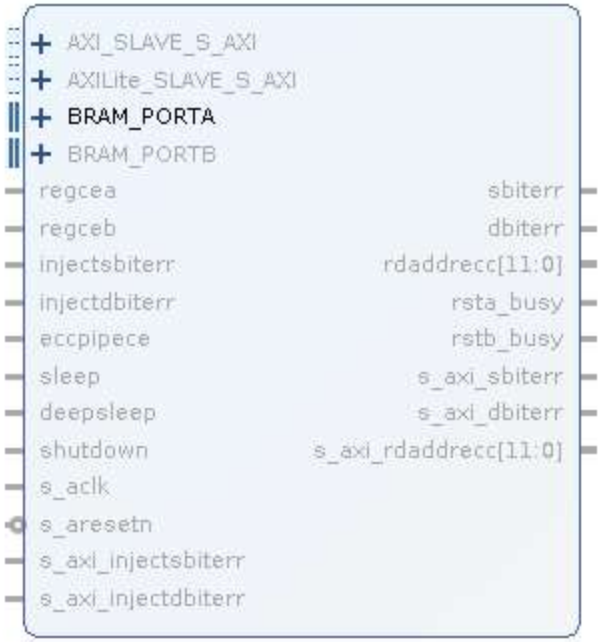

Component Name: blk_mem_gen_0

Basic | Port A Options | Other Options | Summary

Information

Memory Type: Single Port Memory

Block RAM resource(s) (18K BRAMs): 0

Block RAM resource(s) (36K BRAMs): 4

Total Port A Read Latency : 1 Clock Cycle(s)

Address Width A: 12