

IP Symbol	Power Estimation
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32
33	33
34	34
35	35
36	36
37	37
38	38
39	39
40	40
41	41
42	42
43	43
44	44
45	45
46	46
47	47
48	48
49	49
50	50
51	51
52	52
53	53
54	54
55	55
56	56
57	57
58	58
59	59
60	60
61	61
62	62
63	63
64	64
65	65
66	66
67	67
68	68
69	69
70	70
71	71
72	72
73	73
74	74
75	75
76	76
77	77
78	78
79	79
80	80
81	81
82	82
83	83
84	84
85	85
86	86
87	87
88	88
89	89
90	90
91	91
92	92
93	93
94	94
95	95
96	96
97	97
98	98
99	99
100	100

☒ Show disabled ports

```

+ AXI_SLAVE_S_AXI
+ AXILite_SLAVE_S_AXI
+ BRAM_PORTA
+ BRAM_PORTB

```

```

regcea                                sbiterr
regceb                                dbiterr
injectsbiterr                         rdaddrecc[11:0]
injectdbiterr                         rsta_busy
eccpipece                             rstb_busy
sleep                                 s_axi_sbiterr
deepsleep                             s_axi_dbiterr
shutdown                              s_axi_rdaddrecc[11:0]
s_aclk
s_aresetn
s_axi_injectsbiterr
s_axi_injectdbiterr

```

Component Name	blk mem gen 1
----------------	---------------

Basic	Port A Options	Other Options	Summary
-------	----------------	---------------	---------

Interface Type Native

☐ Generate address interface with 32 bits

Memory Type	Single Port RAM	▼
-------------	-----------------	---

☐ Common Clock

### ECC Options

ECC Type No ECC

☐ Error Injection Pins Single Bit Error Injection

### Write Enable

☐ Byte Write Enable

Byte Size (bits) 9

### Algorithm Options

Defines the algorithm used to concatenate the block RAM primitives. Refer datasheet for more information.

Algorithm Minimum Area 

Primitive 8kx2 ▼

IP Symbol	Power Estimation
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32
33	33
34	34
35	35
36	36
37	37
38	38
39	39
40	40
41	41
42	42
43	43
44	44
45	45
46	46
47	47
48	48
49	49
50	50
51	51
52	52
53	53
54	54
55	55
56	56
57	57
58	58
59	59
60	60
61	61
62	62
63	63
64	64
65	65
66	66
67	67
68	68
69	69
70	70
71	71
72	72
73	73
74	74
75	75
76	76
77	77
78	78
79	79
80	80
81	81
82	82
83	83
84	84
85	85
86	86
87	87
88	88
89	89
90	90
91	91
92	92
93	93
94	94
95	95
96	96
97	97
98	98
99	99
100	100

☒ Show disabled ports

- + AXI\_SLAVE\_S\_AXI
- + AXILite\_SLAVE\_S\_AXI

```
|| + BRAM_PORTA
```

```
|| + BRAM_PORTB
```

```
regcea                                sbiterr
```

```
regceb dbiterr
```

```
injectsbiterr      rdaddrecc[11:0]
```

```
injectdbiterr          rsta busy
```

```

- eccpipece          rstb busy

```

— sleep                      s axi sbiterr

— deepsleep s axi dbiterr

```

- shutdown                s axi rdaddrecc[11:0]

```

— *o* ack

arezetn

- s\_axi injects biterr

- s\_axi\_injectdbiterr

Component Name	blk mem gen 1
----------------	---------------

Basic	Port A Options	Other Options	Summary
-------	----------------	---------------	---------

### Memory Size

Write Width  Range: 1 to 4608 (bits)

Read Width 32 ▼

Write Depth 4096 Range: 2 to 1048576

Read Depth 4096

Operating Mode Write First ▼ Enable Port Type Use ENA Pin ▼

### Port A Optional Output Registers

☐ Primitives Output Register    ☐ Core Output Register

☐ SoftECC Input Register      ☐ REGCEA Pin

### Port A Output Reset Options

<input type="checkbox"/> RSTA Pin (set/reset pin)	Output Reset Value (Hex)	0
---	--------------------------	---

☐ Reset Memory Latch      Reset Priority      CE (Latch or Register Enable) ▾

READ Address Change A

☐ Read Address Change A

IP Symbol

### Power Estimation

☒ Show disabled ports

```

+ AXI_SLAVE_S_AXI
+ AXILite_SLAVE_S_AXI
+ BRAM_PORTA
+ BRAM_PORTB
regcea sbiterr
regceb dbiterr
injectsbiterr rdaddrecc[11:0]
injectdbiterr rsta_busy
eccpipece rstb_busy
sleep s_axi_sbiterr
deepsleep s_axi_dbiterr
shutdown s_axi_rdaddrecc[11:0]
s_ack
s_aresetn
s_axi_injectsbiterr
s_axi_injectdbiterr

```

Component Name	blk_mem_gen_1
----------------	---------------

## Basic

### Port A Options

### Other Options

## Summary

### Pipeline Stages within Mux


0

Mux Size: 1x1

## Memory Initialization

☒ Load Init File

Coe File ..../..../..../Desktop/data\_mem.coe

 Browse Edit☒ Fill Remaining Memory Locations

Remaining Memory Locations (Hex)	0
----------------------------------	---

0

### Structural/UniSim Simulation Model Options

Defines the type of warnings and outputs are generated when a read-write or write-write collision occurs.

Collision Warnings All 

AH

### Behavioral Simulation Model Options

☐ Disable Collision Warnings☐ Disable Out of Range Warnings

IP Symbol

### Power Estimation

☒

+ AXI SLAVE S AXI

+ AXILite SLAVE S AXI

|| + BRAM PORTA

```
|| + BRAM_PORTB
```

```
regcea      sbiterr
```

```
regceb      dbiterr
```

```
injectsbiterr      rdaddrecc[11:0]
```

```
injectdbiterr          rsta_busy
```

```
eccpipece          rstb busy
```

```
sleep s_axi sbiterr
```

```

- deepsleep                               s_axi_dbiterr -

```

```
shutdown      s axi rdaddrecc[11:0]
```

- s ack

• `resetn`

```

- s_axi_injectsbiterr

```

```

- s_axi_injectdbiterr

```

Component Name

blk\_mem\_gen\_1

## Basic

### Port A Options

### Other Options

## Summary

## Information

Memory Type: Single Port Memory

Block RAM resource(s) (18K BRAMs): 0

Block RAM resource(s) (36K BRAMs): 4

Total Port A Read Latency : 1 Clock Cycle(s)

Address Width A: 12