MHS
MATRA HARRIS SEMICONDUCTOR

data sheet

MB GATE ARRAY SERIES
2μ/2 METAL LAYERS
MB 850 - MB 1300 - MB 2000
MB 2700 - MB 4000 - MB 5000 -MB 7500

PRELIMINARY

MAY 1986

Features

- ADVANCED SILICON GATE CMOS PROCESS :
  - TWO LEVEL METAL
  - 2 MICRON DRAWN CHANNEL LENGTH (1.5 MICRONS EFFECTIVE)
  - 1.5 NS TYPICAL GATE DELAY
  - 3 TO 6V POWER SUPPLY RANGE
  - FULL MILITARY TEMPERATURE RANGE – 55°C TO + 125°C
- LARGE MEMORY INTEGRATION :
  - VARIABLE SIZE AND ORGANIZATION
  - UP TO 2K BIT STATIC RAM
- ON CHIP SPECIAL FUNCTIONS :
  - TEST MODE
  - LOW POWER CRYSTAL OSCILLATOR
  - OPERATIONAL AMPLIFIER
- MACRO CELL LIBRARY EXTENSION CAPABILITY :
  - COMBINATIONAL AND SEQUENTIAL SSI MACROS
  - BIT SLICE AND PROGRAMMABLE MSI/LSI MACROS : ALU, UART, COUNTERS...
- COMPLETE INPUT/OUTPUT CELL LIBRARY :
  - TTL OR CMOS COMPATIBLE I/O
  - COMPARATOR FUNCTIONS
- FULLY INTEGRATED CAD SOFTWARE (GATE AID II™) SUPPORT :
  - HIGHLY EFFICIENT AUTOMATIC PLACEMENT AND ROUTING CAPABILITY
  - ACCURATE POST LAYOUT SIMULATION WITH PARASITIC DELAYS
  - ADVANCED HIERARCHICAL SOFTWARE

Description

The MB Gate Array product family from MHS uses a silicon gate dual metal layer CMOS technology. This process, called SAJI V, features effective channel length of 1.5μ for both N and P transistors, and achieves operating speeds up to 40-45 MHz with the inherent low power consumption of CMOS technology.

These MHS gate arrays a new silicon architecture, which provides a complete, dense and flexible RAM/ROM design approach : 1 static RAM bit uses only 1 gate equivalent (2900 gates are necessary to build a 256 × 8 static RAM).

The efficient RAM/ROM integration capability, combined with an extended and open-user library of macro functions, like ALU, UART, Bit slice macro's... and a **100 % hierarchical software package,** offers an excellent solution for complete system integration.

Product Outline

PART NUMBER	GATE (1) COMPLEXITY STANDARD	GATE (1) COMPLEXITY USING RAM	NUMBER OF ROWS	MAX. I/O PADS	DEDICATED VDD/VSS PADS	TOTAL PADS (2)
MB-0850	810	1215	9	50	16	73
MB-1300	1300	1950	13	64	16	87
MB-2000	1920	2880	16	78	16	101
MB-2700	2660	3990	19	96	16	119
MB-4000	3900	5850	21	116	16	139
MB-5000	4800	7200	24	132	16	155
MB-7500 (3)	7500	11250	30	168	16	191

Note 1 : 1 gate is the equivalent of a 2 input NAND or NOR gate (2 P and 2 N channel transistors). With the MHS patented silicon architecture, MB Arrays offer the indicated gate count when no RAM/ROM are used, but offer 50 % more equivalent gates when RAM/ROM are designed.

Note 2 : The difference between the maximum number of pads and I/O's is the number of dedicated pads :
- 16 pads dedicated to VDD, VSS
- 2 pads dedicated to Test Mode
- 2 pads dedicated to low power quartz oscillator
- 3 pads dedicated to operational amplifier

Note 3 : Check with Sales Office for availability.

Architecture

The 2μ MHS gate arrays are organized as rows of uncommitted logic gates (2 N and 2 P channel transistors) separated from each other by an interconnect area reserved for metal 1 routing and RAM/ROM layout. Additional routing is provided in metal 2.

The matrix is surrounded by multi-function peripheral cells providing adequate interface with external circuitry. Floorplan example is given in fig. 5.

Basic Cell

The basic logic gate, as shown in Fig. 1, consists of 2 pairs of N and P channels MOS transistors. It is potentially equivalent to a 2 input NOR or NAND.

High internal noise immunity is provided by a gridded supply line distribution formed by horizontal metal 1 lines within each cell, and a vertical metal 2 supply line every 5 cells.

This gives a regular and low impedance power supply distribution all over the matrix.

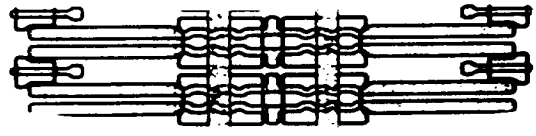


Fig. 1 Basic Cell

Peripheral Cell - I/O Buffers

The peripheral cell provides a total flexibility of input/output configurations. It is divided into 3 dedicated zones.

All these zones are independant. Then customizations relative to each of them are stackable in order to realize easily and reliably the required input/output functions thus making 40 options available.

In addition all peripheral cells have a protection network against electrostatic discharge and latch up.

Fig. 2 shows the available peripheral cell configurations for each dedicated zones.

Zone	Available Functions
INPUT	CMOS input Buffer TTL input Buffer Direct input CMOS Schmitt Trigger TTL Schmitt Trigger
OUTPUT	Output Buffer, 3 State Buffer, Open Drain } 6, 3, 1.5 or 0.75 TTL Drive Capability Options Analog Comparator (for input signals) Power Buffer (for internal use) Power supply
RESISTOR	Pull-up, Pull-down } 170 KΩ typical

Fig. 2

Bidirectional input/output is possible by placing both input and output configuration functions. In addition peripheral cell can be connected to an external RC or Crystal oscillator (see AN 1023 "A design guide for oscillators using MHS gate Arrays").

ON CHIP SPECIAL FUNCTIONS

Additional dedicated features are available on 3 corners of the chip :
- One low power Crystal oscillator.
- One operational amplifier.
- One test mode.

LOW POWER CRYSTAL OSCILLATOR

This oscillator circuitry has both input and output capacitors and feedback resistors directly integrated on the chip.

In the 1 to 10 MHz range, only an external Crystal has to be added.

To minimize static current consumption, the oscillator can be disabled.

If additional oscillators are needed, they can be designed with peripheral cells (See AN 1023).

Fig. 3 shows the schematic of this low power crystal oscillator and fig. 5 shows its location on the corner of the matrix :

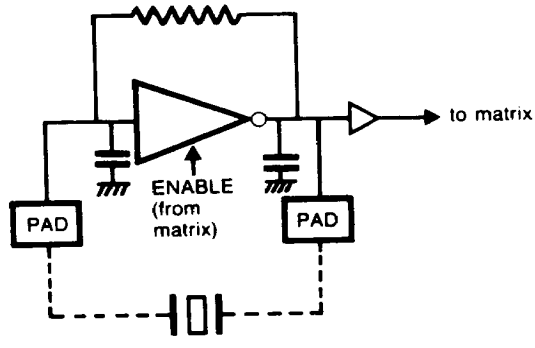


Fig. 3

Operating Consumption (Typical at V_{DD} = 5V)

@ 1 MHz	600μA.
@ 2 MHz	1mA.
@ 10 MHz	3mA.

OPERATIONAL AMPLIFIER

Designed for small analog applications, this internally compensated op amp features the following typical performance :

- Band width (Unity gain)	1 MHz
- Input offset voltage	6mV
- Open loop gain	80 dB
- Input voltage range	0 to 4V
- Output voltage swing	0 to 5V

This operational amplifier is located in a corner of of each matrix per fig. 5.

ON CHIP TEST MODE

This special test mode permits the output buffers to be directly forced to HIGH, LOW, or HIGH IMPEDANCE states allowing static parameter testing. Two pins are necessary for this function : TMODE, CKTEST and their location is shown per fig. 5.

These inputs can be rerouted to any other I/O PAD. TMODE pin at logic HIGH enables the test mode function and then CKTEST pin configures it.

CKTEST can also be used as a conventional input signal and TMODE pin as circuit master reset.

In addition 2 internal signals (CLK1 and CLK2) are given by Test Mode circuitry after static parameter test completion. These signals can be used for dynamic test.

Test Mode Timing and operating functions are shown in Fig. 4.

TIME UNIT	TMODE	CKTEST	ACTION	CLK1	CLK2
1	0	Don't care	- Test Mode inhibited	0	0
2	1	0	- Test Mode enabled - No Action on outputs	0	0
3	1	First Rising Edge	- 3 state outputs forced to high impedance - Other outputs forced to 0	0	0
4	1	2nd Rising Edge	- All outputs forced to 1	0	0
5	1	3rd Rising Edge	- All outputs forced to 0	0	0
6 ..... Until TMODE is reset	1	Following Rising Edges	- Static parameter Test Mode inhibited - No action on outputs - CLK1 is set to 1 - CKTEST is copied on CLK2	1	CKTEST

Fig. 4 : Test Mode operating functions

VDD and VSS Requirements

MHS SAJI V is a fast technology, high speed operation places stringent requirements on the ground bussing and the number of power and ground pads required to avoid current spikes when the output buffers charge and discharge their output capacitance.

To improve noise immunity, MHS MB gate-arrays are provided with two different power supplies :

- One for internal matrix : VSSA and VCCA
- One for input/output buffers : VSSB and VCCB

More than two power (VDD) and ground (VSS) pins may be required to support several high-drive outputs witching simultaneously at fast speeds.

Therefore guidelines on the number of VSS and VDD pins are given below, based on three factors :

- The driver capability of the buffer
- The number of buffers switching simultaneously
- The location of power and ground pads relative to the outputs.

Each VSS pad can support a maximum of 16 buffers (8 on each side of the VSS pad - 3 TTL drive bufout equivalent).

Each VDD pad can support up to 32 buffers (16 on each side).

The number of VDD pads required for the array depends on the array size.

Note that inputs may be ignored when calculating power pins since CMOS inputs sink and source minimal current.

Figure 5 shows the footprint for the MB series. Dedicated VSSA, VSSB, VCCA, VCCB power pads are located near corners. Additional VCCB and VSSB pads may be placed on any standard I/O buffers. Extra VCCA pads can only be placed on left and top sides, extra VSSA pads on right and bottom sides.

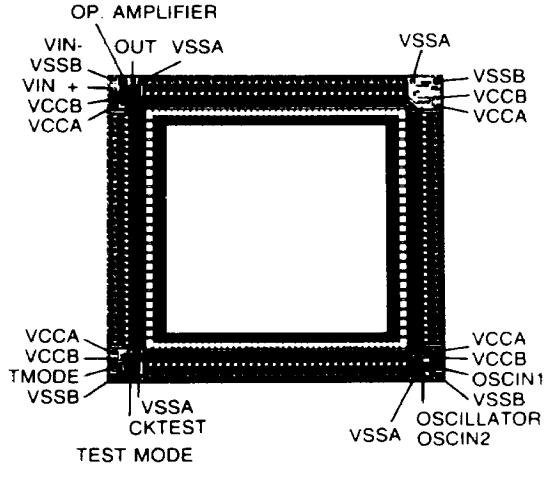


Fig. 5 : MB Gate-Array Series - Foot print example

Power Dissipation

Four basic elements are making power dissipation in a CMOS device :

1 - Leakage. It constitutes the quiescent power dissipation and is essentially negligible.

2 - DC current through on transistors.
This can be from many sources :

- Low on an input with a pull-up resistors or vice-versa
- Outputs which sink or source current
- Unconnected inputs with a pull-up or pull-down
- Floating internal gates
- Inputs at worst-case levels, particularly TTL inputs at 2V.

Care should be exercised during logic design to make sure that there is a test condition in which all this DC current may be turned off, so that DC leakage may be easily measured.

3 - Overlap currents when the P- and N-Transistors are switching from the high-to-low state or vice-versa.
This contributes less than 10 % of the power dissipated and occurs for the transition period when : VTH (N) < VIN < VDD - VTH (P).

4 - The most important factor is the charging and discharging of circuit capacitance. The charging of a capacitor C to a voltage V through a P-Channel device builds up a charge CV and stores energy CV^2. This energy is later discharged through an N-Channel transistor in the CMOS P-N pair. When such switching takes place at a frequency "f", the resulting power dissipated in the CMOS circuit is equivalent to $P = CV^2f$. This AC power dissipation usually contributes in excess of 90 % of the toal power dissipated. Thus, the power dissipation in a CMOS circuit is essentially a function of the frequency and logic configuration. Each internal gate in the MB series typically consumes 20 microwatts/gate/MHz. Each I/O buffer, with its higher output capacitance and larger capacitive loads, consumes 25 microwatts/I/O/MHz/pF.
The total power consumption is the sum of the power dissipated by all the gates and I/O buffers switching each cycle.
Table 1 illustrates typical power calculations.

Process Description

The MB arrays are fabricated using the self aligned junction isolation, SAJI V, process. The association of a 2µ lithography and a self aligned, planarized dual metal layer CMOS process allows complexities up to 5000 equivalent 2 input NAND gates with typically sub-nanosecond propagation delays.

Propagation Delays

Propagation delays of the MB series logic elements are a function of several factors :

- Fanout
- Interconnection routing
- Junction temperature
- Supply voltage
- Processing tolerance
- Input transition time and polarity.

The simultor generates the propagation delays for all networks automatically once the network has been entered. Prior to layout, these values are based on the estimated interconnection. After layout, the program is RE-RUN and final delay values based on actual interconnection are obtained.

The effect of temperature may be estimated from figure 6. The maximum junction temperature will determine a temperature multiplier (KT). In CMOS technology, the junction temperature is usually close to the ambiant temperature but for more details refer to MHS note PR/SC/2546. Similarly, figure 7 shows the effect of supply voltage (KV). MHS assumes a 33 % variability resulting from all other factors including processing thus process variation factors are :

- Kp = 0.75 in best case process
- Kp = 1 typical
- Kp = 1.33 in worst case process

The maximum propagation delay is thus :

$t_{max} = K_p \cdot K_t \cdot K_v \cdot t_{typ}$

		Example 1	Example 2
Matrix		MB 1300	MB 5000
Operating voltage	VDD =	5 V	6 V
Frequency	F =	10 MHz	20 MHz
Leakage consumption			
• ICCSB max	ICCSB =	200 µA	200 µA
• Power dissipation P1 = ICCSB . VDD	P1 =	1 mW	1.2 mW
Operate consumption			
• Available gate count		1300	4800
• Used gate count		1150	4350
• Toggle gate count (at each clock cycle)	G =	200	1000
• Elementary power dissipaton 4 µA/gate/MHz/for MB series (20 µW)	p =	4 µA	4 µA
• Power dissipation $P2 = p \cdot G \cdot VDD^2 \cdot F$	P2 =	40 mW	480 mW
Output consumption			
• Number of output buffer		30	65
• Number of output buffer toggling at each cycle	N =	8	25
• Output load capacitance	C =	50 pF	50 pF
• Power dissipation $P3 = N \cdot C \cdot VDD^2 \cdot F$	P3 =	100 mW	900 mW
Global power dissipation Pd = P1 + P2 + P3	Pd =	141 mW	1380 mW
Junction temperature			
• Package		LCC 68	PGA 144
• Thermal resistance (See section 3)	Rja =	30°C/W	15°C/W
• Operate temperature	Ta =	125°C	125°C
• Junction temperature Tj = Ta + Pd . Rja	Tj =	130°C	145°C

Table 1 : Power dissipation and junction temperature calculation example.

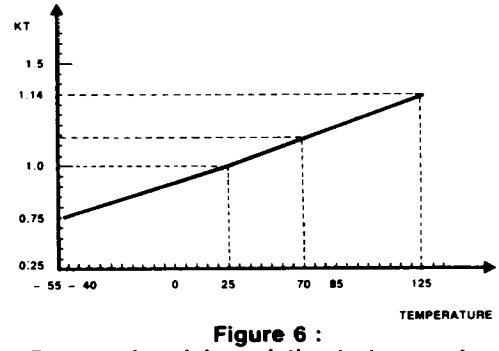


Figure 6 :
Propagation delay relative to temperature

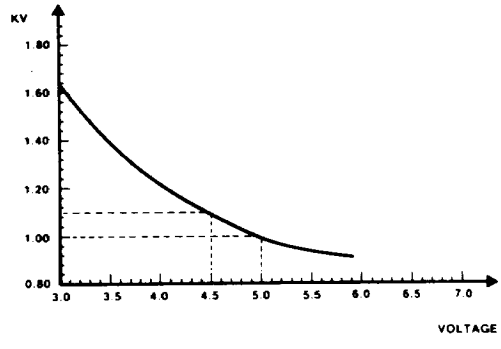


Figure 7 : CMOS propagation delays as a function of supply voltage

Factors worst case for Vcc = 5V ± 10 %

		K min	K max
Commercial – 5	0° – 70°C	0.64	1.7
Industrial – 9	– 40°C ; + 85°C	0.53	1.8
Military – 2	– 55°C ; + 125°C	0.50	2.0

Note : Factor of 1 is assumed for 5V, typical process at 25°C operating temperature range.

Table 2

MHS Macro Library

The MB arrays are supported by a complete and extensive Macrofunction Library.

Fig. 8 represents as an example the diagram of a DFFNR1, Macro cell (D Flip-Flop with Reset) as it appears to the routing software. Some signal names are available at the top and bottom of the macro : these signal names are accessible with the Metal 1 level (signals CK, R*).
Other Signal names, such as D, Q, Q, are directly accessible with the Metal 2 level.

As explained above, the Macro library can be split into :
- Basic operators
- Macrocells and I/O cells
- Macrofunctions
- User defined macros

The input/ouptut Library is not described in this section. Fig. 2, above, describes all basic input/output configurations and possible combinations.

For more drive capability, output buffers can be internally connected in parallel.

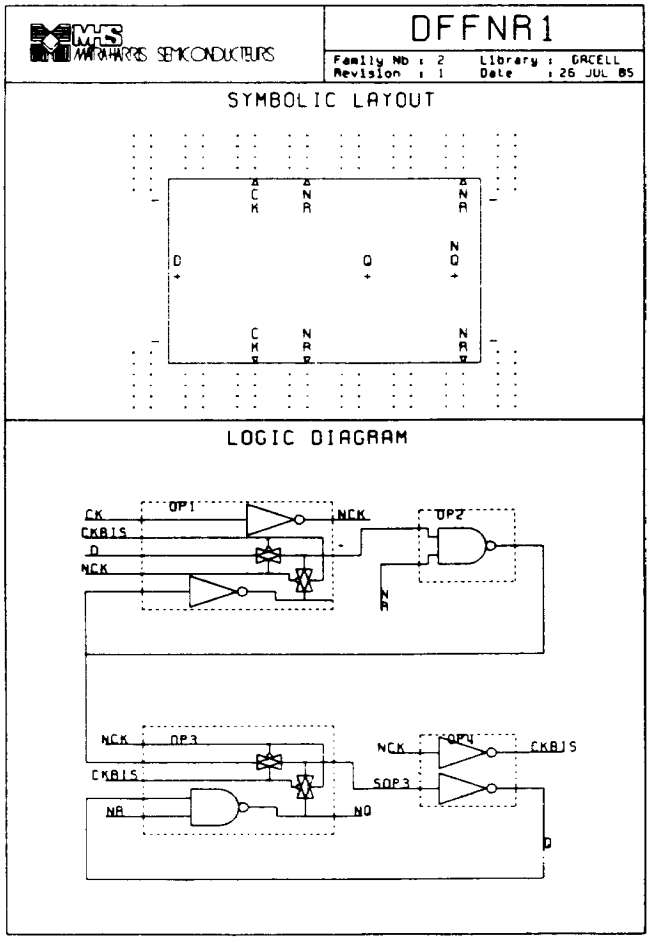


Fig. 8 : DFFNR1 Layout Diagram

Hierarchical Design Structure

The MHS design approach is supported by 5 levels of hierarchy (see Fig. 9) :
- level 1 graphical
- level 2 basic operator
- level 3 macrocells, I/O cells, user defined macro's
- level 4 blocks and macrofunctions
- level 5 final circuit

The user can only access levels 2 to 5.
Level 1 can only be accessed by MHS.

1. Graphical level

This level can only be accessed by MHS for initial library layout. Indeed, special functions, basic stackable functions for input/output, and basic operators are created using standard CAG tools. Other levels are then built with these elements.

2. Operator level

All macros (except I/O cells) are built with a few basic operators. This level eliminates all risks during macrocell generation. The list of these basic operators is given in Fig. 12.

3. Macro cell level

This is the standard level to start circuit design. Four types of macros are used :
- SSI Macros.
- User defined Macros.
- Bit slice, programmable MSI/LSI Macros.
- Input/Output cells.

4. Block and macrofunctions levels

Both top-down and bottom-up styles are supported from a logic point of view and only bottom-up from a layout point of view. Blocks are either software entities exploded during layout phases or hard blocks with a fixed lay-out. Four types of blocks can be defined :
- RAM/ROM blocks.
- MSI/LSI blocks.
- Bit slice blocks.
- User defined blocks.

5. Circuit level

A circuit is built with Macros, blocks and I/O cells.

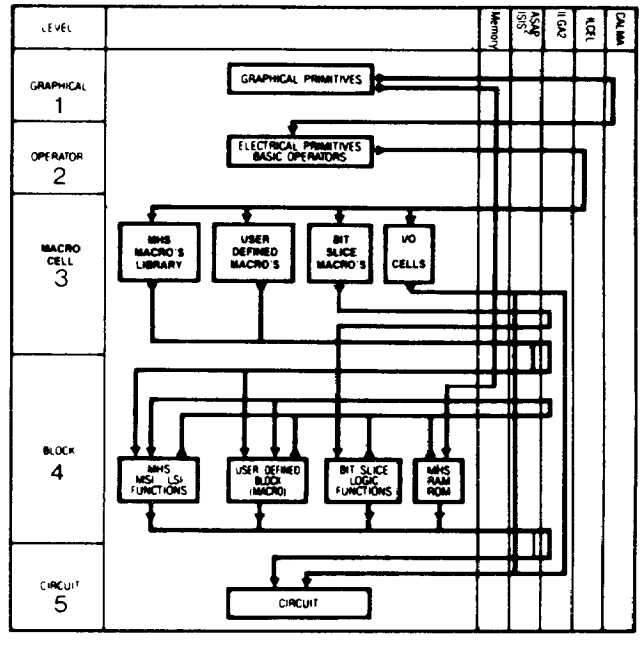


Fig. 9 : Hierarchical Level Description

Characterized basic logic operator are described below in fig. 10 :

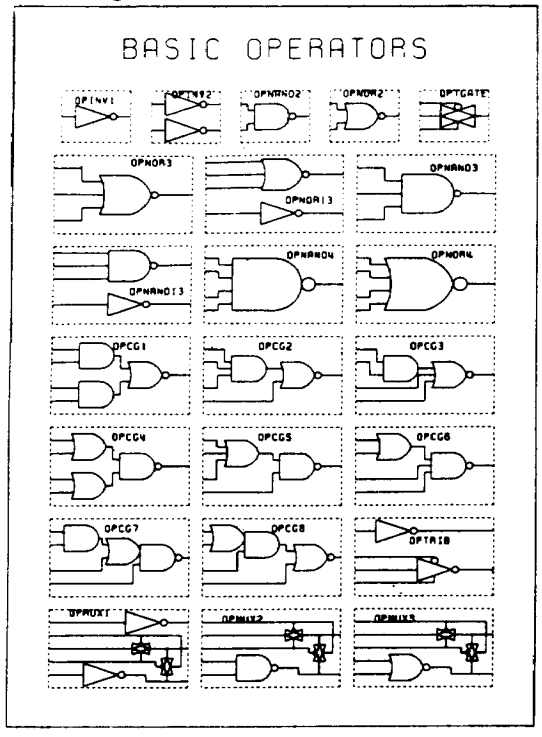


Fig. 10 : Basic Operator Library

Macrocells

These elements called Macrocells are made from level 2 basic operator listed above and are the basic building blocks available to the user. The MB series contains SSI/MSI functions such as :

- Combinatorial logic functions (AND, OR, NOR, NAND, INVERTERS)
- Sequential functions (FLIP-FLOP S, LATCHES)
- Coders, decoders, multiplexers
- Arithmetic circuits
- Comparators
- Counters
- Registers

Detailed description of available Macro Library is included in MHS booklet "Macrocell and Macrofunction Library - PR/SC/8501", and an example of this list is given below in figure 11.

MACRO NAME	COMBINATIONAL FUNCTIONS	GATE COUNT	TYPE (1)	AVAILABILITY STATUS (2)
OR5	See NOR5			
AND5	See NAND5			
INV2	Two single inverters	1	H	
NOR2	2 input NOR gate	1	H	
NOR4	4 input NOR gate	2	H	
OR2	2 input OR + NOR gate	2	H	
OR4	4 input OR + NOR gate	3	H	
AND4	4 input AND + NAND gate	3	H	
NAND4	4 input NAND gate	2	H	
AND2	2 input AND + NAND gate	2	H	
NAND2	2 input NAND gate	1	H	
EXOR	2 input EXCLUSIVE OR + NOR gate	3	H	
CG5	NOT ((A OR B OR C) AND D)	2	H	
CG7	NOT (((A AND B) AND C) OR D)	2	H	
CG3	NOT ((A AND B) OR C OR D)	2	H	
CG1	NOT ((A AND B) OR (C AND D))	2	H	
CG8	NOT (((A OR B) AND C) OR D)	2	H	
CG2	NOT ((A AND B AND C) OR D)	2	H	
CG4	NOT ((A OR B) AND (C OR D))	2	H	
INV1	One single inverter	1	H	
EXNOR	2 input EXCLUSIVE NOR + NAND gate	3	H	
NOR3	3 input NOR gate	2	H	
OR3	3 input OR + NOR gate	2	H	
NAND3	3 input NAND gate	2	H	
AND3	3 input AND + NAND gate	2	H	
INVP	Two parallel inverters	1	H	
NOR5	5 input NOR + OR gate	4	H	
NAND5	5 input NAND + AND gate	4	H	
INVP8	8 x 2 parallel inverters	8	H	
INV8	Eight single inverters	4	H	
XORF	2 input EXCLUSIVE OR gate (fast)	2	H	
XNORF	2 input EXCLUSIVE NOR gate (fast)	2	H	
INVS	Two serial inverters	1	H	
CB6	NOT ((A OR B) AND C AND D)	2	H	

	SEQUENTIAL FUNCTIONS			
RSNAND	R S NAND flip flop	2	H	
RSNOR	R S NOR flip flop	2	H	
JKFFNRNS	J K flip flop with neg Set and Reset	9	H	
JKFFNS	J K flip flop with neg Set	8	H	
DFFNR1	One clock DFF with neg Reset	6	H	
LATCH1	Latch	3	H	
DFFNRNS1	One clock DFF with neg Set and Reset	7	H	
DFF	2 phase clock D flip flop	4	H	
DFFNS1	One clock DFF with neg Set	6	H	
DFF1	One clock D flip flop	5	H	
LATCHNS1	Latch with neg Set	4	H	
LATCHNR1	Latch with neg Reset	4	H	
JKFFNR	J K flip flop with neg Reset	8	H	
LATCHNR2	Double latch with neg Reset		H	
LATCHR1	Latch with pos Reset	4	H	
JKFFRS	J K flip flop with pos Set and Reset	9	H	
DFFS1	One clock D flip flop with pos Reset	6	H	
DFFR1	One clock D flip flop with pos Reset	6	H	
JKFFS	J K flip flop with pos Set	8	H	
DFFRS1	One clock DFF with pos Set and Reset	7	H	
LATCHNS1	Latch with pos Set	4	H	
JKFFR	J K flip flop with pos Reset	8	H	
TFF	Toggle flip flop with parallel load	12	H	
	THREE STATES LOGIC FUNCTIONS			
TGATE	Transfer gate	1	H	
TRISTAN	Three states buffer inverted	2	H	
TRISTA	Three states buffer	3	H	
	CODERS/DECODERS/MULTIPLEXERS			
MUX	2 to 1 multiplexer with two enable	2	H	
MUX1	2 to 1 multiplexer with one enable	3	H	
DEC24E	2 to 4 decoder with enable	6	H	
DEC24	2 to 4 decoder	6	H	
MUX41	4 to 1 multiplexer	6	H	
H7442	BCD to decimal decoder (1 OF 10)	84	S	
H7443	Excess 3 to decimal decoder	24	S	
H7444	Excess 3 to decimal decoder	24	S	
H74137	3 to 8 decoder with address latches	32	S	
H74138	1 of 8 decoder/multiplexer	33	S	
H74148	8 to 3 line priority encoder	49	S	
H74151	8 input multiplexer with enable	50	S	
H74152	8 input multiplexer	24	S	C
H74157	Quadruple 2 to 1 multiplexer	22	S	C
H74131	3 to 8 line decoder with addr. registrs	36	S	C
H74147	10 to 4 line encoder	38	S	C
H74150	16 bit data selector with enable	79	S	C
H74154	4 to 16 decoder	69	S	C
H74157	Quad 4 to 16 decoder (non inverting)	22	S	C
H74398	Quad 2 input multiplexer with storage	40	S	C
H7447	BCD to 7 segment decoder	68	S	C
	LOGIC COMPARATORS			
H7485	4 bit magnitude comparator	58	S	

MACRO NAME	COUNTERS	GATE COUNT		
count01	4 bits synchronous counter sync reset active low	44	H	
count02	4 bits sync counter with async resl active low	44	H	
count03	4 bits sync modulo counter async reset active low	58	H	
count04	4 bits sync programmable modulo counter with async reset active low	65	H	
count5	4 bits async counter with async reset active low	24	H	
count7	4 bits async modulo counter async reset active low	38	H	
count8	4 bits async programmable modulo counter with async reset active low	46	H	
count9	4 bits sync counter with async set and reset active low	44	H	
count11	4 bits sync counter with sync set reset and load	60	H	
count13	4 bits up/down sync counter sync set reset and load	72	H	
sync01	Sync counter cell with sync reset	11	H	
sync02	Sync counter cell with async reset	11	H	
sync03	Sync modulo counter cell with async reset	13	H	
sync04	Sync programmable modulo counter cell with async reset	15	H	
sync5	Async counter cell with async reset	6	H	
sync7	Async modulo counter cell with async reset	8	H	
sync8	Async programmable modulo counter cell with async reset	10	H	
sync9	Sync counter cell with async set and reset	11	H	
sync11	Sync counter cell with sync set reset and load	15	H	
sync13	Sync up/down counter cell sync set reset and load	18	H	
ace112b	Asynchronous counter basic subcell	7	H	
aloadb	Asynchronous optional load subcell	3	H	
aprgb	Asynchronous counter optional modulo subcell	4	H	
arazb	Asynchronous counter optional reset subcell	4	H	
aupdb	Asynchronous counter optional up/down subcell	3	H	
ace113b	Asynchronous counter basic subcell	7	H	
aloada	Synchronous counter optional load subcell	3	H	
aena	Synchronous counter optional enable subcell	2	H	
asynca	Synchronous counter basic subcell	3	H	
aprga	Synchronous counter optional modulo subcell	4	H	
aupda	Synchronous counter optional up/down subcell	3	H	
acarrya	Synchronous counter basic subcell	2	H	
ace111a	Synchronous counter basic subcell	7	H	

	REGISTERS			
H74164	8 bit SIPO shift register	67	S	C
H7494	4 bit PISO shift register	42	S	C
H74179	4 bit parallel access shift register	86	S	C
H7496	5 bit shift register	47	S	C
H74165	8 bit PISO shift register	85	S	C
H74299	8 bit universal shift register	142	S	C
	ARITHMETIC FUNCTIONS			
OBFA	One bit full adder	9	H	
OBSA	One bit half adder	5	H	
CARRY	Parallel carry generator	11	H	
ADD	One bit full adder with fast carry path	9	H	
H7483	4 bit binay full adder with fast carry	56	S	
H74181	4 bit ALU	107	S	
H74182	Carry look ahead generator	31	S	
H74183	Carry save full adder	17	S	
H74283	4 bits full adder		S	
H74261	2 by 4 parallel binary multiplier	73	S	
H74381	4 bit full ALU/function generator	166	S	
H74284	4 by 4 parallel binary multiplier		S	C
H7482	2 bit binary full adder	26	S	C
H74382	4 bit ALU/function generator		S	C
H74384	8 bit multiplier		S	C
	MISCELLANEOUS			
H74180	9 bit odd/even parity generator/checker	28	S	
H74120	Pulse generator	14	S	
H7487	4 bit true/complement	19	S	
LSSD	LSSD flip flop	14		

Note 1 : C = Check with your Gate Center for availability date.

Note 2 : H = Hard macro (schematic + lay out)

S = Soft macro (schematic)

Fig. 11 : Macrocell examples (non limitative list)

MSI/LSI Macros Extension Capability

Fig. 12 gives the gate size of bit slice, programmable MSI/LSI Macros already predefined.

Other MSI/LSI Macros are in development :
- FIFO's
- Timers
- CRC Decoder/Encoder
- Bit slice microprocessor (2901 type)

With such programmable functions and with MHS RAM/ROM concept, MB Series brings circuit design to successful system integration capability.

MSI/LSI MACRO	SIZE	MSI/LSI MACRO	SIZE
- ALU of 32 functions (16 Arithmetic, 16 Logical)	(1) 21 gates/bit	- UART	(2) from 360 to 644 gates
- Static Shift Register	6 gates/stage	- Presettable Counter	14 gates/stage
- Asynchronous Counter	6 gates/stage	- Divide by N Counter	12 gates/stage
- Synchronous Counter	11 gates/stage	- Parallel Multiplier	(3) 11 gates/basic unit
- Up/Down Counter	18 gates/stage	- Dynamic PLA	1 gate/PLA output

Fig. 12

Notes : (1) ALU does not include Carry look ahead logic.
(2) UART size depends on number of bits, bit parity...
UART includes receiver and transmitter.
(3) a N by M multiplier has N x M basic units.

Memory Blocks

RAM (static RAM)

Referring to Fig. 1, the addition of 2 small N transistors within the interconnect area allows the design of a 6 transistor SRAM memory cell by using only 1 gate. Thus complete and flexible memory design is possible with very good integration and modularity, at nos cost in silicon if memory is not required.

Up to 2K bits of SRAM memory can be integrated in half a MB 5000 Array with a typical access time of 35 ns (for a 256 x 8 SRAM).

The block diagram of a 256 x 8 static RAM is described in Fig. 13. More details about memory structure and operating conditions are given in the Technical Report TR 2012 : "MB GATE ARRAY SERIES : Advanced concepts on regular silicon architecture."

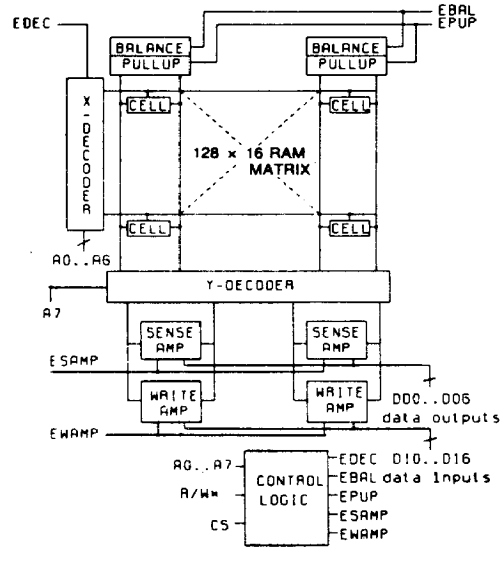
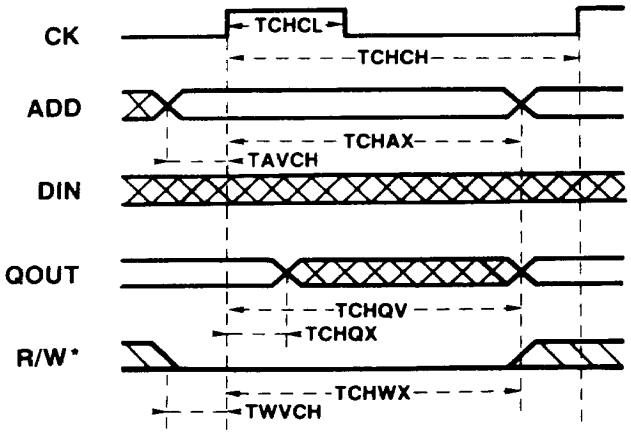
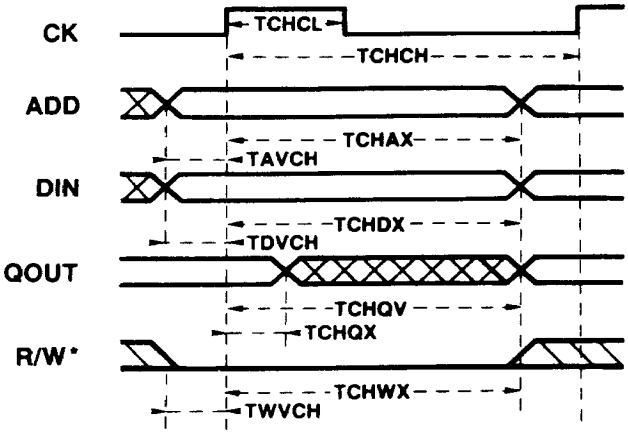


Fig. 13 A : SRAM block diagram examples (256 x 8)



RAM read cycle



RAM write cycle

		UNIT	MIN	MAX
TCHCH	Cycle time	NS	65	
TCHCL	Clock pulse width (high level)	NS	20	
TAVCH	Adress set up	NS	– 15	
TCHAX	Adress hold	NS	60	
TDVCH	Data in set up	NS	– 15	
TCHDX	Data in hold	NS	60	
TCHQX	Output hold	NS	15	
TCHQV	Access time	NS		65
TWVCH	R/W* set up	NS	– 15	
TCHVX	T/W* hold	NS	60	

Fig. 13 B : SRAM timings examples

RAM GENERATION

The generation of RAM is software assisted (MEMORY).
The user has only to specify the memory configuration : number of address bits, and word length.

Fig. 14 and 15 give some memory sizes (in number of gates).

RAM SIZE	HEIGHT (Number of rows)	WIDTH (Columns)	TOTAL GATE COUNT	WORST CASE (in ns)		TYPICAL
				Commer. temp. rang TCHQV	Military temp. range TCHQV	TCHQV
128 x 16	20	152	3040	65	76	34
32 x 16	19	56	1064	61	71	32
8 x 16	19	32	608	56	66	30
4 x 16	19	28	532	54	63	28
256 x 8	20	145	2900	65	76	34
128 x 8	20	81	1539	63	74	33
32 x 8	11	56	616	48	56	25
8 x 8	11	32	352	41	48	22
512 x 4	20	143	2860	65	76	34
128 x 4	12	81	972	50	59	26
32 x 4	7	56	392	40	47	22
8 x 4	7	32	224	38	44	20
1024 x 2	20	141	2820	65	76	34
512 x 2	20	77	1540	63	74	33
128 x 2	7	81	567	45	52	23
16 x 2	5	40	200	34	40	18
2048 x 1	20	141	2820	65	76	34
512 x 1	20	77	1540	61	71	32
128 x 1	7	47	329	42	50	22
32 x 1	5	33	165	35	38	18

Fig. 14 : SRAM size and Access Time

ROM

Two bits of ROM can be programmed by using only the 2 extra N transistors within the interconnect area (see Fig. 1).

The ROM is twice as dense as RAM. Typical access time is 75 ns.

Furthermore the standard basic gates remain free for implementing usual logic.

	Estimate number of bits N words of M bits	512 x 8	256 x 8	128 x 8
ROM	$(N1/2 + 8)(M_1 + 2)_{(1)}$	2640	1360	720

Fig. 15 : ROM size

Note : (1) N_1 and M_1 correspond to the internal memory plane format. Maximum limits of these 2 parameters are : $M_1 \leq 16$. $N_1 \leq 128$ for RAM and $M_1 \leq 256$ for ROM. In addition $N_1 \times M_1 = N \times M$.

In order to know an estimation of gates used by a memory of N words of M bits, N1 and M1 are computed in order to get the minimum memory size and by respecting their maximum respective values.

User Defined Macro's

80 % of user needs are commonly covered by previously described Macro Library. To fulfill special user requirements, MHS has introduced the concept of a user defined macro library, assisted by ILCEL CAD software (ILCEL : interactive layout of cell).

The user can generate new macro's easily and reliably in a few steps :
- Schematic capture of a Macro using GED (Graphic editor) sotfware.
- Validation of a Macro using the Logic Simulator.
- Layout of a Macro under ILCEL control.
- Automatic documentation generation and insertion into user's data base.

With ILCEL software, user is able to :
- Create a new macro (SSI or bit slice macro).
- Edit an existing macro and modify it.
- Generate documentation.

The layout of the macro is performed from a set of characterized basic logic operators which are described above in Fig. 10.

Fig. 16 shows an example of a one bit full adder macro generated using the ILCEL layout software.

Macros, generated by ILCEL, are then considered as hard macros by the CAD software package.

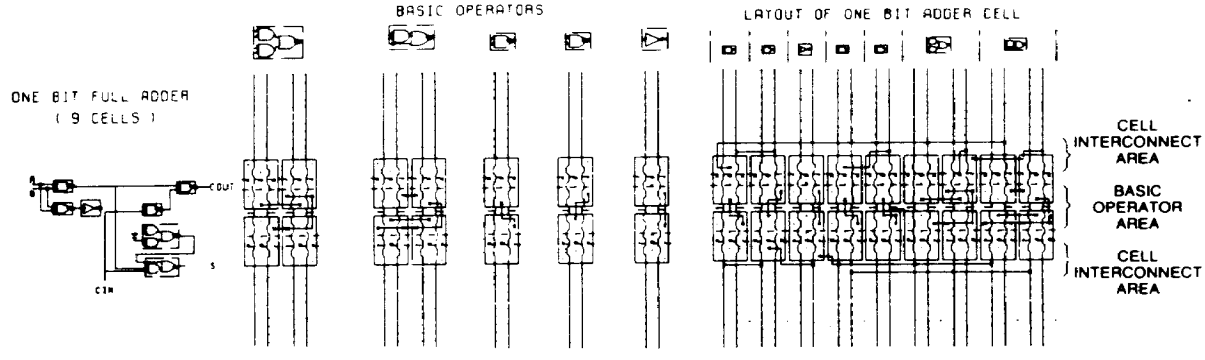


Fig. 16 : ILCEL example : one bit full adder macro generation

MHS Gateaid II Cad Software Tools

The MB family is supported by a computer aided design (CAD) system, the major of which has been developped by Matra-Harris Semiconducteurs CAD Division. The system provides CAD tools for schematic and test vector entry by graphical capture, logic simulation, accurate prediction of circuit speed performance, automated layout design, electrical and design rule checking, post-layout simulation using delays extracted from layout, and automatic conversion of simulation test patterns files into tester format.

The CAD tools are integrated under a supervisory program called « GATE AID II » that runs on Digital Equipment Corporation VAX computers (VMS operating system).

All CAD tools access a common data base which ensures information integrity and version management from schematic entry up to mask and test program generation.

Schematic Entry :

After completion of the library of macros/blocks necessary for circuit generation using ILCEL (user defined macros) and MEMORY (generation memory blocks) software, GED provides graphic capture of schematic diagram.

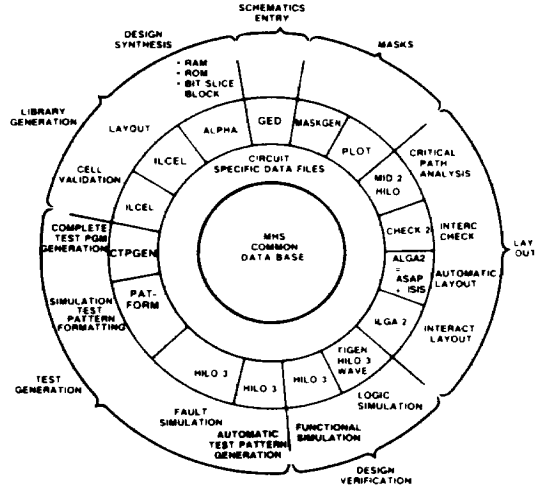


Fig. 17 : MHS Data Base Schematic.

Logic Simulation :

Users have access to the HILO 3 (1) logic simulator. For logic verification, customers may perform HILO 3 behavioral simulation. For design verification, a pre-layout timing analysis is run with calculated delays based on fanout and best, typical and worst cases libraries.

HILO 3 timing simulation is based on the input test patterns description generated with TIGEN software (graphical timing generator editor).

WAVE software provides in addition the timing simulation output in a logic analyser output format.

Placement and Routing :

2 softwares are available : ILGA 2 for interactive layout and ALGA 2 for automatic layout.

ILGA 2 is used for preplacement of I/O cells, blocks, critical path implementation or correction. In addition ILGA 2 allows generation of LSI/MSI Macros or bit slice blocks. In this case macros and blocks are seen as rigid macros or blocks.

ALGA 2 is the automatic placement and routing software. The main features of ALGA 2 sotfware are :

- Efficient automatic placement and routing performance (up to 90 % silicon use).
- Capability to force priorities for critical path routing.
- Capability to place and route blocks (hard or soft blocks).
- Possibility to take into account already preplaced macros, blocks and connections.

It consists of 2 pieces of software :

- ASAP : Automatic placement supporting hierarchical bloc placement.
- ISIS : Automatic routing handling pre-routing and critical path.

Layout checking

CHECK 2 performs electrical and design rule checking. When ILGA 2 is used, CHECK 2 performs an on-line check.

Post-layout simulation

MID 2 HILO is computing the delays of the interconnect nets from the topology of the network after performing layout. Delays are based on capacitance of the interconnection nets.

After the delay information is extracted, these delays are inserted into the network data base for post-layout HILO simulation and then critical path analysis, thus providing an excellent tool for first silicon success.

Test generation

A fault simulator is incorporated into HILO 3 and provides testability coverage ratio information according to the input test vectors generated with TIGEN.

PATFORM software automatically translates the customer's final post-layout HILO 3 simulation output file into a test vector pattern file directly compatible with the production test equipment.

CTPGEN, in conjunction with the test mode nodes, provides an easy way to add static and dynamic parameter tests to the functional test pattern file.

The complete test tape is used for probe and final test.

(1) HILO is a trademark of GENRAD

Development Flow

With MHS, the customer can determine his own level in involvement in the Gate-Array development process.

To get started on a Gate-Array design, the following sequence of preliminary steps is suggested :

- Partitionning of the complete system into building blocks. This partitionning will be made by minimizing I/O count between circuits.
- Convertion of functional block into a logic schematic : at this stage, MHS Macrocell and Macrofunction library and hierarchical features (refer above) can be used.
- Determination of critical path timing.
- Estimation of Gate-Count and I/O requirement. Do not forget test mode and power supply requirement (refer above).
- Choice of array size, package, temperature range.
- Cross-checking with MHS for feasibility.
- Agreement on a set of specifications.

Level I : Customer submit the circuit schematic and test-data to MHS and our staff will take it from here.

Level II : Customer performs design entry and simulation and generates test patterns. MHS completes layout and fabrication. This level may be done using MHS gateaid software (Level II G) or workstations (II W).

Level III : Customer completes design entry, simulation and layout. MHS makes silicon.

	LEVEL I	LEVEL II		LEVEL III	
		IIG	IIW	IIIG	IIIW
Funtional and logic design	C	C	C	C	C
Logic description	C	C	C	C	C
Test pattern	C	C	C	C	C
Schematic entry	M	C	C	C	C
Functional simulation	M	C	C	C	C
First sign-off (Intermediate design review)	C + M	C + M	C + M	—	—
Place and route	M	M	M	C	C
Re-Simulate	M	M	M	C	C
2nd Sign-Off (Design review)	C + M	C + M	C + M	C + M	C + M
Mebes tape and mask tooling	M	M	M	M	M
Wafer personalizing and testing	M	M	M	M	M
Samples delivery	M	M	M	M	M

C : Customer M : MHS or licenced gate-house

Fig. 19 :
Customer Interface Possibilities

Fig. 20 outlines the gate array development phases. This chart delineates the responsibilities of MHS and of the customer. During phase 1 (design translation), most of the responsibility lies with the customer ; during phase 3 (fabrication) with MHS. In phases 2 and 2' (design implementation and test generation) both parties, MHS and customer, are involved.

Detailed customer interface possibilities are given in fig. 19.

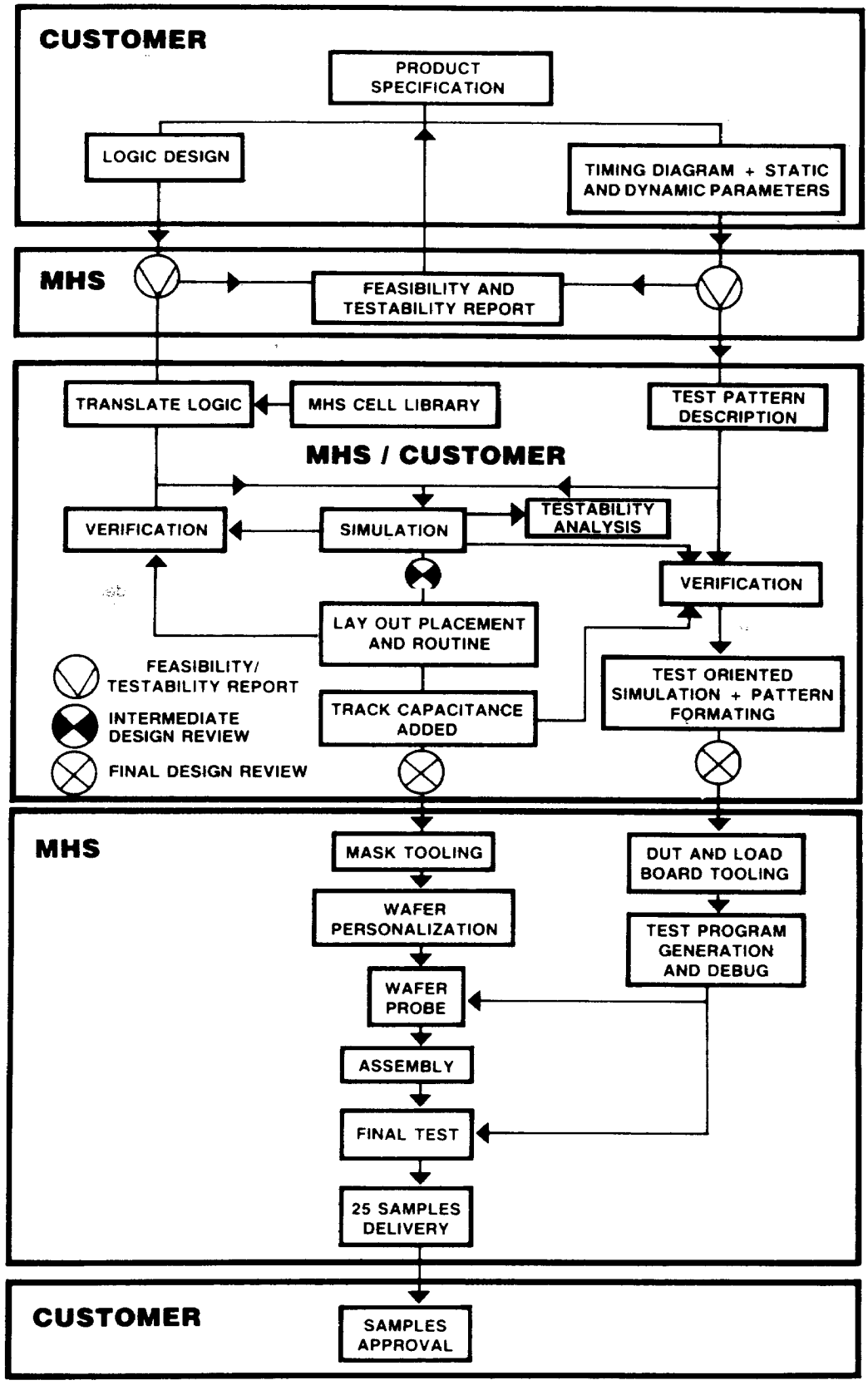


Fig. 20 : MHS Standard Gate Array Development Flow + MHS Customer Design and Test Support.

Characteristics

ABSOLUTE MAXIMUM RATINGS :

PARAMETER	SYMBOL	LIMITS	UNIT
DC Supply Voltage	VDD	- 0.5 to + 6	Volt
Input/Output Voltage	V_{IN}/V_{OUT}	- 0.5 to VDD + 0.5	Volt
Input current	I_{IN}	± 10	mA
Storage Temperature	T_{stg}	- 65 to + 150	° C

RECOMMENDED OPERATING CONDITIONS :

PARAMETER	SYMBOL	LIMITS	UNIT
DC Supply Voltage	VDD	3 to 6	Volt
Input/Output Voltage	V_{IN}/V_{OUT}	0 to VDD	Volt
Operating Temperature Range	Military (- 2) Mil 883C (- 8) Screening conditions Industrial (- 9) Commercial (- 5)	- 55 to + 125 - 55 to + 125 - 40 to + 85 0 to + 70	°C

DC ELECTRICAL CHARACTERISTICS :

(Specified at VDD = 5 V ± 10 % and all temperature ranges unless otherwise notified)

PARAMETER	MIN	TYP*	MAX	UNIT	CONDITIONS
Low Level Input Voltage VIL CMOS (BUFIN MOS) VIL TTL (BUFIN TTL)			1.5 0.8	V V	
High Level Input Voltage VIH CMOS (BUFIN MOS) VIH TTL (BUFIN TTL)	3.5 2 2.2			V V V	(0/+ 70°C) (- 40/+ 85°C) (- 55/+ 125°C)
Low Level Output Voltage VOL (BUFOUT) VOL (BUFOUT 12) VOL (BUFOUT 14) VOL (BUFOUT 2)			0.4	V	IOL = - 4.8 mA IOL = - 2.4 mA IOL = - 1.2 mA IOL = - 9.6 mA
High Level Output Voltage VOH (BUFOUT) VOH (BUFOUT 12) VOH (BUFOUT 14) VOH (BUFOUT 2)	3.9			V	IOH = - 1.0 mA IOH = - 0.5 mA IOH = - 0.25 mA IOH = - 2 mA
High Level Output Voltage VOH (BUFOUT) VOH (BUFOUT 12) VOH (BUFOUT 14) VOH (BUFOUT 2)	2.4			V	IOH = - 4.8 mA IOH = - 2.4 mA IOH = - 1.2 mA IOH = - 9.6 mA
Input Leakage Current IIL, IIH (without pull-up or pull-down)	- 1 - 3 - 5		+ 1 + 3 + 5		VIN = VDD or 0V 0°C to + 70°C - 40°C to + 85°C - 55°C to + 125°C
Input Leakage Current (with pull-up) (with pull-down)	- 100	40 + 40	+ 100	µA µA	VIN = VDD or 0 V
3 State Ouput Leakage current IOZ	- 1 - 3 - 5		+ 1 + 3 + 5	µA	VIN = VDD or 0 V 0°C to + 70°C - 40°C to + 85°C - 55°C to + 125°C
Output Short Circuit Current IOS (BUFOUT) (1)	25 - 20		80 - 75	mA	VDD = Max, VOUT = VDD VDD = Max, VOUT = 0 V
Standby Current IDDSB		5		nA/gate	VIN = VDD or VSS
Operating Current IDDOP		3		µA/gate /MHz	VIN = VDD or VSS

* *Typical values are given at VDD = 5V, TA = 25° C.*

Note (1) : No more than one output at a time may be shorted for more than a maximum duration of one second.

AC ELECTRICAL CHARACTERISTICS :

(Specified at VDD = + 5 V)

PARAMETER		Commercial – 5 0° C to + 70° C TYP *	Commercial – 5 0° C to + 70° C MAX	Industrial – 9 – 40° C to + 85° C MAX	Military – 2, – 8 – 55° C to + 125° C MAX	UNIT
Inverter Propagation Delay tp	(1)(2)	1.2	1.5	1.7	2	ns
2 input NAND Prop. Delay tp (NAND2)	(1)(2)	1.5	2	2.3	2.7	ns
2 input NOR Prop. Delay tp (NOR2)	(1)(2)	2	3.4	3.9	4.5	ns
4 input NAND Prop. Delay tp (NAND2)	(1)(2)	2.5	3.7	4.3	4.9	ns
4 input NOR Prop. Delay tp (NOR4)	(1)(2)	4.2	5.8	6.7	7.7	ns
D Flip Flop with R Prop. Delay tp (DFFR*)	(1)(2)(3)	2.5	3.9	4.5	5.2	ns
CMOS compatible input buffer Prop. Delay tp (BUFIN MOS)	(1)(2)	2.1	2.9	3.4	3.9	ns
TTL compatible input buffer Prop. Delay tp (BUFIN TTL)	(1)(2)	2.7	3.8	4.4	5.1	ns
Output Buffer Prop. Delay tp (BUFOUT)	(1)(4)	6.5	10	11.5	13	ns
Output Buffer Rise Time (10 % - 90 %) tr (BUFOUT)	(4)	5.1	7.1	8.2	9.4	ns
Output Buffer Fall Time (90 % - 10 %) tf (BUFOUT)	(4)	5.5	8.1	9.3	10.5	ns

* *Typical values are given at VDD = 5V, TA = 25° C.*

AC TEST CONDITIONS :

(1) All propagation delay times are average values between input signal and output signal.

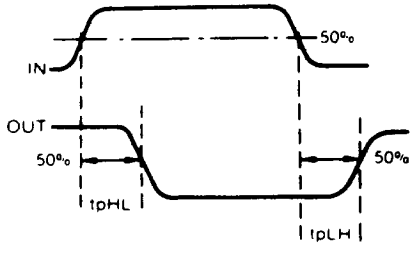
Propagation delay values given in this table are average values between tpLH and tpHL.

$$tp = \frac{tpLH + tpHL}{2}$$

Signal levels are

VIL = 0 Volt

VIH = VDD (except VIH = 3 V for TTL input buffer).



(2) Propagation delays of internal cells and input buffers are given under following conditions :
Fan out = 3 + 1000μm metal interconnect

(3) D Flip Flop (with R) propagation delay is corresponding to propagation delay between clock (CK) and output (Q)

(4) BUFOUT cell test conditions are :
Load Capacitance CL = 50 pF

Packaging

Matra-Harris semiconductor offers six types of packages for the MB gate array family :

- Dual in line packages
  - Plastic DIP
  - Ceramic (Cerdip)
  - Side Brazed DIL
- Chip Carriers
  - Plastic Leaded Chip Carriers (PLCC)
  - Ceramic Leadless Chip Carriers (LCC)
- Ceramic Pin Grid Arrays (PGA)

Fig. 21 presents all the different package suitable for MB arrays.

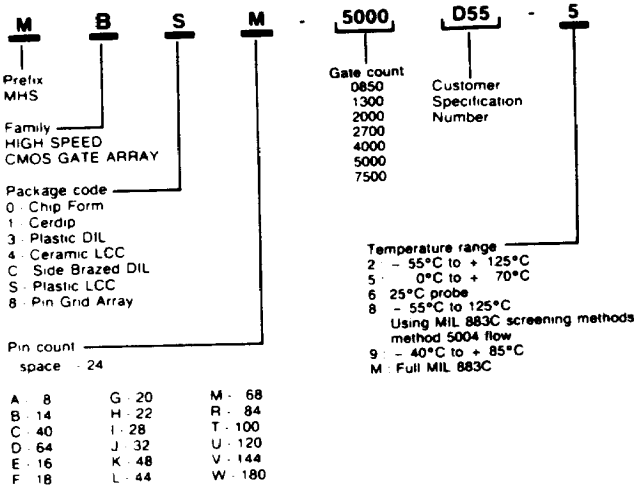
Packages types	Lead count	MATRIX MB 0850	MB 1300	MB 2000	MB 2700	MB 4000	MB 5000	MB 7500	Mark code	Lead finish	Width
Side-Braze	20	C							C	Gold plated	600
	24	A	A	A	A				CI		600
	28	A	A	A	A	A	A	C	CC		600
	40	A	A	A	A	A	A	A	CK		600
	48	A	A	A	A				CD		900
	64	A	A	A	A						
CERDIP	24	A	A	A	A				1	Tin plated	600
	28	A	A	A	C				1I		600
	40	A	A	A	A				1C		600
PDIL	20	A							3	Tin dipped	300
	24	A	A	A					3I		600
	28	A	A	A	A	A	C		3C		600
	40	A	A	A	A	C					600
PLCC	28	C	C						SI	Tin dipped SR	
	44	A	A	A	A	A	A	A	SL		
	68	A	A	A	A	A	A	A	SM		
	84		A	A	A	A	A	A			
LCC	44	A	A	A	A				4L	Gold plated	
	68	A	A	A	A	A	A	A	4M		
	84	C	A	A	A	A	A	A	4R		
P G A Cavity up	68	C	C	A	A	A	A	A	8M	Gold plated	
	84	A		A	A	A	A	A	8R		
	100			A	A	A	A	A	BT		
	120			A	A	A	A	A	BU		
	144			A	A	A	A	A	8V		
	180			C	C	C	C	C	8W		
CLCC J leaded	28	C	C						JL	Gold plated	
	44	C	C	C	C	C	C		JM		
	68	C	C	C	C	C	C	C	JR		
	84	C	C	C							

A = Available
C = Check with your Gate-Center

Fig. 21 : MB Gate-Arrays package table

MB gate arrays can also be delivered in dice form (chiptray) or wafer form.

Ordering Information



MB 5000
Test Vehicle Evaluation Chip

To evaluate the MB gate array family performance, a test vehicle has been built using an MB 5000 chip : MB 8V- 5000 DO0.

In order to verify all static, dynamic and functional aspects of MB family capabilities, this evaluation chip includes several patterns such as :

- 31 stage ring oscillator.
- Combinations of all basic operators for dynamic characterization.
- A 16 bit ALU using a bit slice approach.
- A 256 x 7 RAM and a 256 x 1 ROM.
- Combinations of input/output cells.
- Oscillators (RC oscillator, low power crystal oscillator, high frequency crystal oscillator.)
- Divider.
- Comparator.
- Operational amplifier.

This test vehicle chip is packaged into a 144 pin Pin Grid Array. It is available for customer evaluation purpose and is delivered with a complete measurement data log.

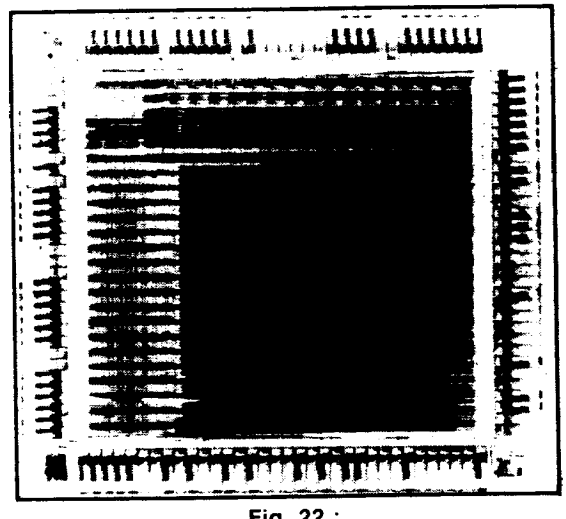


Fig. 22 :
MB8V - 5000 AAA Test Vehicle Chip Photograph