LOAD GROUP	Immediate	X Register	Y Register	A Register	8 Bit Memory	X 8 bit memory	Y 8 bit Memory	Y 8 bit Memory Y+Y+1	Y=Y-1 Y 8 bit Memory	8 bit Memory + X	8 Bit Memory + Y	16 bit Memory	16 Bit Memory XY	16 Bit Memory + X	16 Bit Memory + Y
A Register	LDAI 73	LDAX 38	LDAY 39	LDAF ca	LDA(M) 5b	LDA(X) 78	LDA(Y) 79	LDA(Y)+ e6	LDA-(Y) 7f	LDA(M+X) 7c	LDA(M+Y) 7d	LDA(MM) 8b	LDA(XY) 74	LDA(MM+X) A0	LDA(MM+Y) A4
X Register	LDXI 75		LDXY 68	LDXA f3	LDX(M) 5c		LDX(Y) 7a				LDX(M+Y) 6e	LDX(MM) 8c			LDX(MM+Y) b8
Y Register	LDYI 70	LDYX 58		LDYA 72	LDY(M) 90	LDY(X) 59				LDY(M+X) ef		LDY(MM) 8d			
X and Y Register	LDXYII 91				LDXY(M) 85	LDXY(X) 84	LDXY(Y) a3								
STORE GROUP															
A Register					STA(M) 88	STA(X) 69	STA(Y) e8	STA(Y)+ 7e	STA-(Y) e7	STA(M+X) a8	STA(M+Y) a9	STA(MM) c6	STA(XY) 95	STA(MM+X) a1	STA(MM+Y) a5
X Register					STX(M) 89		STX(Y) 8a				STX(M+Y) 6f	STX(MM) 9c			STX(MM+Y) b9
Y Register					STY(M) 6c	STY(X) 94				STY(M+X) be		STY(MM) f0			
Immediate					STI(M) 80	STI(X) e0	STI(Y) f2								
SW (Swap values)			*XY ff ad	*AY ff ec											
Clear to 0		CLX 02	CLY 01	CLA 05	CL(M) 06	CL(X) 04	CL(Y) 07				CL(M+Y) 3a				
ALU Instructions (ADC, SBC, CMP, OR, XOR, AND) Result in Except CMP														XY Register	
A Register	*AI 08-0d	*AX 20-25	*AY d0-d5		*A(M) 48-4d	*A(X) d8-dd	*A(Y) 60-65			*A(M+X) 28-2d	*A(M+Y) 30-35	*(MM) b0-b5			
X Register	*XI 10-15		*XY 40-45				*X(Y) ff 20-25								
Y Register	*YI 18-1d														
XY Register (ADC SBC CMP)	*XYII f8,f9,fa														
Y 8 Bit Memory (ADC SBC CMP)					*Y(M) 98,99,9a										
ROR / ROL		*X 8e/8f	*Y 92/93	*A a6 / a7	*(M) 82 / 83	*(X) e2/e3	*(Y) d6/d7			*(M+X) ff a6/ff a7	*(M+Y) ae/af			*XY 9e/9f	
SHR / SHL		*X 16/17	*Y 1e/1f	*A 0e/0f	*(M) 66/67	*(X) 46/47	*(Y) 4e/4f			*(M+X) ff 0e/ff 0f	*(M+Y) 36/37			*XY 27/28	
SHR4 / SHL4 (4 Shifts)	*A ff 7a / 2f														
INC		*X de	*Y ce	*A 3e	*(M) 86	*(X) 96	*(Y) b6			*(M+X) ff 3e	*(M+Y) f6	*(MM) 5e		*XY 76	
DEC		*X df	*Y cf	*A 3f	*(M) 87	*(X) 97	*(Y) b7			*(M+X) ff 3f	*(M+Y) f7	*(MM) 5f		*XY 77 (C Flag only)	
LDC (Bit 7 to Carry Flag)	*AS ab		*YS ff ab		*S(M) ff eb		*S(Y) ff 07								
TST (C Flag Reset, ZF)		*X ff 75	*Y ff 73	*A 6d	*(M) 3b	*(X) 6b	*(Y) 3d			*(M+X) 7b	*(M+Y) 9b	*(MM) ff 05		*XY 03	
BIT Immediate in * To C Flag)				*A 9d	*(M) cd	*(X) f1	*(Y) 81			*(M+X) 71	*(M+Y) e1	*(MM) c1			
BIT X in A to C Flag				*AX c5											
BIT Y in X to C Flag				*XY ff 79											
BIT Y in A to C Flag				*AY ff c5											

ADD without Carry								
X Register ADD	*XI ff fb		*XY ff 38	*XA c8				
Y Register ADD	*YI ff f5	*YX ff 39		*YA c9				
SP Stack Pointer ADD	*SPI ff ca	*SPX ff c8		*SPA ff 02				
A Register ADD	*AI ff 68							

Stack, Jump, Call	No Parameters							XY Register
PUSH / POP		*X c0 / c2	*Y c3 / c4	*AF fe/ee				*XY 80/81
JP	ac				*(M) 54		*(Y) 52	*XY ff c2
JPS (Same 256 byte page)	eb					*(X) ff f3		
CALL	2e							*XY 56
RET / RETI	57 / ff f4							

Special Register Functions	Save	Load	Sign to Carry	Load One
Stack Pointer	LDASP cc	LSPA ff 8a		
Stack Pointer		LDSPI ff ea		
Vector	LDAV ff cc	LDVA ff ed		
Y Register Memory			LDCS(Y) ff 07	
Y Register			LDCYS ff ab	
A Register			LDCAS ab	LDAONE ad

Conditional Jump / Return	Carry	No Carry	Zero	No Zero
RET	*C e4	*NC e5	*Z e9	*NZ ea
JP	*C ba	*NC bb	*Z bc	*NZ bd
JPS (Same 256 byte page)	*C f4	*NC f5	*Z ec	*NZ ed
DECYJ (Same Page)			*Z bf	*NZ c7
CPAIJ (Same Page)	*C aa	*NC a2	*Z 5a	*NZ 6a
TSTXJ (Same Page)			*Z cb	*NZ 53
JBA (Same Page)	*S 55	*C 5d		

Miscellaneous Instructions	
No Operation	NOP 00
Enable Interrupts	EIT ff fc
Disable Interrupts	DIT ff fd
Complement Carry Flag	CCF fd
Set Carry Flag	SCF fb
Clear Carry Flag	CLC fc
Jump to Vector at vv	BRK 3c vv