Computer Architecture DAT105 Exercise Session 3

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Agenda

- ▶ Problem 3.13
- ▶ Problem 3.15
- ▶ Problem 3.16

Agenda

- ▶ Problem 3.13
- ▶ Problem 3.15
- ▶ Problem 3.16

Problem 3.13

In this problem we compare the performance of three dynamically scheduled processor architectures on a simple piece of code computing $Y=Y\ast X+Z$, where X,Y and Z are (double-precision-8bytes) floating-point vectors. Using the core ISA of Table 3.3 in the notes, the loop body can be compiled as follows:.

LOOP:	L.D F0,0(R1) L.D F2,0(R2) L.D F4,0(R3)	X[i] loaded in F0 Y[i] loaded in F2 Z[i] loaded in F4
	MUL.D F6,F2,F0	Multiply X by Y
	ADD.D F8,F6,F4	Add Z
	ADDI R1,R1,#8	update address registers
	ADDI R2,R2,#8	-
	ADDI R3,R3,#8	
	S.D F8, -8(R2)	store in Y[i]
	BNE R4.R2.LOOP	(R4)-8 points to the last element of Y

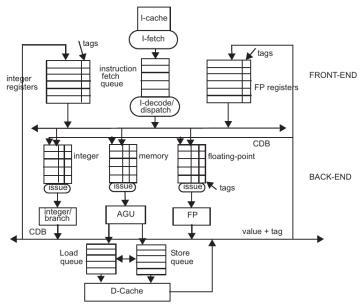


Figure 3.15. Hardware for Tomasulo algorithm

Instruction Dispatch Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
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	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	

	Instruction	Dispatch	Issue	Exec Start		Cache	CDB	COMMENTS
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	wait for F2

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	wait for F6

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	_	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	_	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	_	(9)	
17	ADDI R2,R2,#8	7	8	(9)	9	_	(10)	
					•			

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	_	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	_	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	_	(9)	
17	ADDI R2,R2,#8	7	8	(9)	9	_	(10)	
18	ADDI R3,R3,#8	8	9	(10)	10	_	(11)	
19	S.D F8, -8(R2)	9	11	(12)	12	-	-	wait for R2
								*

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	
19	S.D F8, -8(R2)	9	11	(12)	12	-	_	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	_	wait for F8

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	
19	S.D F8, -8(R2)	9	11	(12)	12	-	_	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	_	wait for F8
l11	BNE R4,R2,LOOP	11	12	(13)	13	-	(14)	

Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
			Start	End			
L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
MUL.D F6,F2,F0	4	7	(8)	12	_	(13)	wait for F2
ADD.D F8,F6,F4	5	14	(15)	19	_	(20)	wait for F6
ADDI R1,R1,#8	6	7	(8)	8	_	(9)	
ADDI R2,R2,#8	7	8	(9)	9	_	(10)	
ADDI R3,R3,#8	8	9	(10)	10	_	(11)	
S.D F8, -8(R2)	9	11	(12)	12	_	-	wait for R2
S.D F8, -8(R2)	10	21	(22)	22	(23)	-	wait for F8
BNE R4,R2,LOOP	11	12	(13)	13	_	(14)	
L.D F0,0(R1)	15	16	(17)	17	(18)	(19)	wait for I11
							in dispatch
	L.D F0,0(R1) L.D F2,0(R2) L.D F4,0(R3) MUL.D F6,F2,F0 ADD.D F8,F6,F4 ADDI R1,R1,#8 ADDI R2,R2,#8 ADDI R3,R3,#8 S.D F8, -8(R2) S.D F8, -8(R2) BNE R4,R2,LOOP	L.D F0,0(R1) 1 L.D F2,0(R2) 2 L.D F4,0(R3) 3 MUL.D F6,F2,F0 4 ADD.D F8,F6,F4 5 ADDI R1,R1,#8 6 ADDI R2,R2,#8 7 ADDI R3,R3,#8 8 S.D F8, -8(R2) 9 S.D F8, -8(R2) 10 BNE R4,R2,LOOP 11	L.D F0,0(R1) 1 2 L.D F2,0(R2) 2 3 L.D F4,0(R3) 3 4 MUL.D F6,F2,F0 4 7 ADD.D F8,F6,F4 5 14 ADDI R1,R1,#8 6 7 ADDI R2,R2,#8 7 8 ADDI R3,R3,#8 8 9 S.D F8, -8(R2) 9 11 S.D F8, -8(R2) 10 21 BNE R4,R2,LOOP 11 12	L.D F0,0(R1) 1 2 (3) L.D F2,0(R2) 2 3 (4) L.D F4,0(R3) 3 4 (5) MUL.D F6,F2,F0 4 7 (8) ADD.D F8,F6,F4 5 14 (15) ADDI R1,R1,#8 6 7 (8) ADDI R2,R2,#8 7 8 (9) ADDI R3,R3,#8 8 9 (10) S.D F8, -8(R2) 9 11 (12) S.D F8, -8(R2) 10 21 (22) BNE R4,R2,LOOP 11 12 (13)	L.D F0,0(R1) 1 2 (3) 3 L.D F2,0(R2) 2 3 (4) 4 L.D F4,0(R3) 3 4 (5) 5 MUL.D F6,F2,F0 4 7 (8) 12 ADD.D F8,F6,F4 5 14 (15) 19 ADDI R1,R1,#8 6 7 (8) 8 ADDI R2,R2,#8 7 8 (9) 9 ADDI R3,R3,#8 8 9 (10) 10 S.D F8, -8(R2) 9 11 (12) 12 S.D F8, -8(R2) 10 21 (22) 22 BNE R4,R2,LOOP 11 12 (13) 13	L.D F0,0(R1) 1 2 (3) 3 (4) L.D F2,0(R2) 2 3 (4) 4 (5) L.D F4,0(R3) 3 4 (5) 5 (6) MUL.D F6,F2,F0 4 7 (8) 12 - ADD.D F8,F6,F4 5 14 (15) 19 - ADDI R1,R1,#8 6 7 (8) 8 - ADDI R2,R2,#8 7 8 (9) 9 - ADDI R3,R3,#8 8 9 (10) 10 - S.D F8, -8(R2) 9 11 (12) 12 - S.D F8, -8(R2) 10 21 (22) 22 (23) BNE R4,R2,LOOP 11 12 (13) 13 -	L.D F0,0(R1) 1 2 (3) 3 (4) (5) L.D F2,0(R2) 2 3 (4) 4 (5) (6) L.D F4,0(R3) 3 4 (5) 5 (6) (7) MUL.D F6,F2,F0 4 7 (8) 12 — (13) ADD.D F8,F6,F4 5 14 (15) 19 — (20) ADDI R1,R1,#8 6 7 (8) 8 — (9) ADDI R2,R2,#8 7 8 (9) 9 — (10) ADDI R3,R3,#8 8 9 (10) 10 — (11) S.D F8, -8(R2) 9 11 (12) 12 — — S.D F8, -8(R2) 10 21 (22) 22 (23) — BNE R4,R2,LOOP 11 12 (13) 13 — (14)

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	COMMENTS
				Start	End			
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
14	MUL.D F6,F2,F0	4	7	(8)	12	_	(13)	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	_	(20)	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	_	(9)	
17	ADDI R2,R2,#8	7	8	(9)	9	_	(10)	
18	ADDI R3,R3,#8	8	9	(10)	10	_	(11)	
19	S.D F8, -8(R2)	9	11	(12)	12	_	-	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	-	wait for F8
l11	BNE R4,R2,LOOP	11	12	(13)	13	_	(14)	
l12	L.D F0,0(R1)	15	16	(17)	17	(18)	(19)	wait for I11
								in dispatch

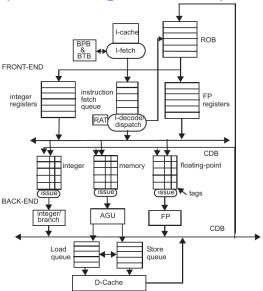


Figure 3.23. Tomasulo algorithm with support for speculative execution

Instruction Dispatch Issue Exec Ex Start Er	ec Cache CDB Retire COMMENTS
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	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
				•				•	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
	•		•	•	•	•			

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	23	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	23	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	24	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
l1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	23	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	24	
19	S.D F8, -8(R2)	9	11	(12)	12	-	-	-	wait for R2
19	S.D F8, -8(R2)	9	11	(12)	12	-	-	-	wait for R2

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	23	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	24	
19	S.D F8, -8(R2)	9	11	(12)	12	-	-	-	wait for R2
110	S.D F8, -8(R2)	10	21	(22)	22	24	_	25	wait for F8,
									then wait to reach top of ROB

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	23	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	24	
19	S.D F8, -8(R2)	9	11	(12)	12	-	-	-	wait for R2
110	S.D F8, -8(R2)	10	21	(22)	22	24	-	25	wait for F8,
									then wait to reach top of ROB
111	BNE R4,R2,LOOP	11	12	(13)	13	_	(14)	26	

	Instruction	Dispatch	Issue	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Start	End				
11	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
12	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
13	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
14	MUL.D F6,F2,F0	4	7	(8)	12	-	(13)	14	wait for F2
15	ADD.D F8,F6,F4	5	14	(15)	19	-	(20)	21	wait for F6
16	ADDI R1,R1,#8	6	7	(8)	8	-	(9)	22	
17	ADDI R2,R2,#8	7	8	(9)	9	-	(10)	23	
18	ADDI R3,R3,#8	8	9	(10)	10	-	(11)	24	
19	S.D F8, -8(R2)	9	11	(12)	12	-	-	-	wait for R2
110	S.D F8, -8(R2)	10	21	(22)	22	24	-	25	wait for F8,
									then wait to reach top of ROB
111	BNE R4,R2,LOOP	11	12	(13)	13	-	(14)	26	
112	L.D F0,0(R1)	12	13	(14)	14	(15)	(16)	27	Address of store is
									known since cycle 13

3.13(c) (Speculative scheduling)

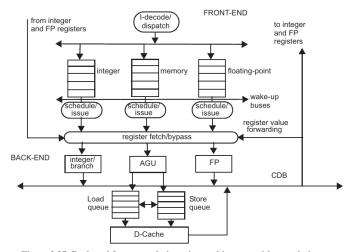


Figure 3.27. Back-end for a speculative microarchitecture with speculative scheduling

3.13(c) (Speculative scheduling)

Instruction Dispatch Issue Register E. Fetch St	ec Exec Cache art End	CDB Retire	COMMENTS
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3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
l1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
l1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	
17	ADDI R2,R2,#8	7	8	9	(10)	10	-	(11)	20	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	
17	ADDI R2,R2,#8	7	8	9	(10)	10	-	(11)	20	
18	ADDI R3,R3,#8	8	10	11	(12)	12	-	(13)	21	CDB conflict with I4

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	
17	ADDI R2,R2,#8	7	8	9	(10)	10	-	(11)	20	
18	ADDI R3,R3,#8	8	10	11	(12)	12	-	(13)	21	CDB conflict with I4
19	S.D F8, -8(R2)	9	10	11	(12)	12	-	-	-	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	
17	ADDI R2,R2,#8	7	8	9	(10)	10	-	(11)	20	
18	ADDI R3,R3,#8	8	10	11	(12)	12	-	(13)	21	CDB conflict with I4
19	S.D F8, -8(R2)	9	10	11	(12)	12	-	-	-	
I10	S.D F8, -8(R2)	10	15	16	17	17	21	-	22	wait for F8
										wait to reach top of ROB

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
l1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	
17	ADDI R2,R2,#8	7	8	9	(10)	10	-	(11)	20	
18	ADDI R3,R3,#8	8	10	11	(12)	12	-	(13)	21	CDB conflict with I4
19	S.D F8, -8(R2)	9	10	11	(12)	12	-	-	-	
110	S.D F8, -8(R2)	10	15	16	17	17	21	-	22	wait for F8
										wait to reach top of ROB
l11	BNE R4,R2,LOOP	11	12	13	(14)	14	-	(15)	23	

	Instruction	Dispatch	Issue	Register	Exec	Exec	Cache	CDB	Retire	COMMENTS
				Fetch	Start	End				
11	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
12	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
13	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
14	MUL.D F6,F2,F0	4	5	6	(7)	11	-	(12)	13	
15	ADD.D F8,F6,F4	5	10	11	(12)	16	-	(17)	18	wait for F6
16	ADDI R1,R1,#8	6	7	8	(9)	9	-	(10)	19	
17	ADDI R2,R2,#8	7	8	9	(10)	10	-	(11)	20	
18	ADDI R3,R3,#8	8	10	11	(12)	12	-	(13)	21	CDB conflict with I4
19	S.D F8, -8(R2)	9	10	11	(12)	12	-	-	-	
110	S.D F8, -8(R2)	10	15	16	17	17	21	-	22	wait for F8
										wait to reach top of ROB
111	BNE R4,R2,LOOP	11	12	13	(14)	14	-	(15)	23	
l12	L.D F0,0(R1)	12	14	15	(16)	16	(17)	(18)	24	CDB conflict with
										I5

3.13(d) (Data-flow graph)

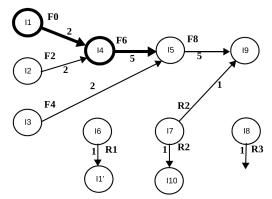
LOOP: L.D F0,0(R1) L.D F2,0(R2) L.D F4,0(R3) MUL.D F6,F2,F0 ADD.D F8,F6,F4 ADDI R1,R1,#8

X[i] loaded in F0 Y[i] loaded in F2 Z[i] loaded in F4 Multiply X by Y Add Z update address registers

ADDI R2,R2,#8 ADDI R3,R3,#8

store in Y[i]

S.D F8, -8(R2) BNE R4,R2,LOOP (R4)-8 points to the last element of Y



3.13(d) (Execution time comparisons)

Execution Time metric	Tomasulo w/o spec	Tomasulo with spec	Spec scheduling	Data-flow
Issue-to-issue	16 - 2 = 14	13 - 2 = 11	14 - 2 = 12	7
Execution-to-execution	17 - 3 = 14	14 - 3 = 11	16 - 4 = 12	7
Retirement	_	27 - 6 = 21	24 - 7 = 17	7

Agenda

- ▶ Problem 3.13
- ▶ Problem 3.15
- ▶ Problem 3.16

Problem 3.15

In this problem we explore the effect of memory disambiguation using a very simple move in memory

$$for(i = 0; i < 100; i + +)$$

 $A[i] = B[i];$

In this code vector A and B are in different areas of memory so that they don't have common elements. The assembly code is LOOP:

L.D F2,0(R1) ADDI R1,R1,#8 ADDI R2,R2,#8 S.D F2,-8(R2) BNEQ R1,R3,LOOP

Problem 3.15

The architecture is the architecture of Problem 3.14 (Tomasulo with speculation and two-way dispatch). Fill Table 3.28. Fill the table for two cases:

- ▶ 1) Conservative (a Load is not issued to cache until the addresses of all previous Stores are know
- 2) Speculative (a Load is issued to cache optimistically when addresses of prior Stores are unknown).

Remember that Stores can only issue to cache once they are at the top of the ${\sf ROB}$

Also assume that the number of ROB entries is limited to 7

3.15 (Tomasulo algorithm with speculation)

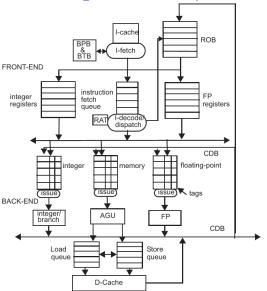


Figure 3.23. Tomasulo algorithm with support for speculative execution

Problem 3.15 - a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8								
14	S.D-A F2,-8(R2)								
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
l12	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 - a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	3	4	4	-	5		CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (4)							
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 - a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (4)							
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 - a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (4)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 - a. Conservative Disambiguation

		a:					400		
		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5		6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7 6	8	8	- 4	8	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)							
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 - a. Conservative Disambiguation

									ı
		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8		-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6 /	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	9	10	12	Wait for previous store address, Cache Conflict
18	ADDI R1,R1,#8	4 (1)							
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 – a. Conservative Disambiguation

114

ADDI R1,R1,#8

I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and 13 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address, Cache Conflict
18	ADDI R1,R1,#8	4 (1)							
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Dispatch Issue Ex_Start Ex_End Cache CDB Retire

Comments

Problem 3.15 – a. Conservative Disambiguation

114

ADDI R1,R1,#8

I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	5	6	6				FU conflict with I6
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
l12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								

Dispatch Issue Ex_Start Ex_End Cache CDB Retire

Comments

Problem 3.15 – a. Conservative Disambiguation

Dispatch

Issue

I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Ex_Start Ex_End

Cache

CDB

Retire

Comments

Problem 3.15 – a. Conservative Disambiguation

114

ADDI R1,R1,#8

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and 13 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Problem 3.15 - a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-/	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	/-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	/	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7		8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11 12	- 14		-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	12	13	13	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)							
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 – a. Conservative Disambiguation

ADDI R1,R1,#8

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	(8)	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	- /	-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	9 🖊	10	10	-	11	16	Wait for R1, CDB conflict
113	L.D F2,0(R1)								

Problem 3.15 - a. Conservative Disambiguation

114

ADDI R1,R1,#8

Dispatch

10 (0)

Issue

11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8 /	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11		-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	L.D F2,0(R1)	10 (1)	11	12	12				Wait for 2 ROB entries, FL conflict

Ex_Start Ex_End

Cache

CDB

Retire

Comments

Problem 3.15 - a. Conservative Disambiguation Dispatch L.D F2,0(R1)

ADDI R1,R1,#8

ADDI R2.R2.#8

S.D-A F2.-8(R2)

S.D-D F2,-8(R2)

ADDI R1,R1,#8

11

12

19

110

111

114

13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6

8

(11)

12

In Parenthesis: Remaining ROB entries

Ex_End

3

3

Cache

4

14

CDB

5

4

9

12

Retire

6

7

14

15

16

Comments

Wait for R2

Wait for R2 Wait for 2 ROB entries,

F2, I9 retire

Wait for R1, CDB conflict Wait for 2 ROB entries, FU

conflict, Cache conflict

Ex_Start

3

3

Issue

2

2

1 (7)

1 (6)

5 (0)

5 (0)

7(1)

10 (0)

8

11

112 BNEQ R1.R3.LOOP 113

L.D F2,0(R1) 10(1) 12 13 13 14

7

10

Problem 3.15 - a. Conservative Disambiguation Dispatch L.D F2,0(R1)

ADDI R1,R1,#8

ADDI R2,R2,#8

ADDI R2.R2.#8

S.D-A F2.-8(R2)

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

ADDI R1,R1,#8

11

12

13

19

110

111

112

113

114

14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6

8

11

12

11

13

In Parenthesis: Remaining ROB entries

Ex_End

3

3

Cache

4

CDB

5

4

9

12

16

Retire

6

7

8

14

15

16

17

Comments

CDB conflict with I1

Wait for R2

Wait for R2 Wait for 2 ROB entries,

F2, I9 retire

Wait for R1, CDB conflict Wait for 2 ROB entries, FU

conflict, Cache conflict

Ex_Start

3

3

8

11

12

11

13

Issue

2

2

7

10

11

10

12

1 (7)

1 (6)

2 (5)

5 (0)

5 (0)

7(1)

7(0)

10(1)

10 (0)

Problem 3.15 - a. Conservative Disambiguation Dispatch

L.D F2,0(R1)

ADDI R1,R1,#8

ADDI R2.R2.#8

S.D-A F2.-8(R2)

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

ADDI R1,R1,#8

11

12

19

110

111

112

113

114

13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1.R1.#8	4 (1)	6	7	7	-	8	13	FU conflict with I6

Ex_End

3

3

8

11

13

12

In Parenthesis: Remaining ROB entries

Cache

4

CDB

5

4

9

12

16

13

Retire

6

7

14

15

16

17

18

Comments

Wait for R2

Wait for R2 Wait for 2 ROB entries,

F2, I9 retire

Wait for R1, CDB conflict Wait for 2 ROB entries, FU

conflict, Cache conflict

10 11 11 13

12

8

11

Ex_Start

3

3

Issue

2

2

7

10

12

11

1 (7)

1 (6)

5 (0)

5 (0)

10(1)

10 (0)

Problem 3.15 – a. Conservative Disambiguation

Dispatch Issue Ex Start Ex End Cache CD8 Retire

119

L.D F2,0(R1)

		Dispatcii	issue	LX_Start	EX_EIIU	Cacile	CDD	Neure	Comments
11	LD F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	(11)	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	,	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11		-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	27	11	-	12	16	Wait for R1, CDB conflict
113	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
117	S.D-D F2,-8(R2)								
118	BNEQ R1,R3,LOOP								

Problem 3.15 – a. Conservative Disambiguation

119

L.D F2,0(R1)

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	LD F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	- /	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	/-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	/	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12		13	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	(19)	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	J7 - 12		<i>-</i> -	Wait for R2
117	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
118	BNEQ R1,R3,LOOP	13 (0)							

Problem 3.15 – a. Conservative Disambiguation

Dispatch

118

119

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

13 (1)

13 (0)

17

14

11	LD F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-		Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6		7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7		8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8		9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13		14	19	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16		-	-	Wait for R2

18

15

18

15

19

Ex_Start

Issue

Ex_End

Cache

CDB

Retire

20

16

Comments

Wait for ROB and F2

CDB Conflict

Problem 3.15 – a. Conservative Disambiguation

Dispatch

LD F2,0(R1)

ADDI R1.R1.#8

ADDI R1.R1.#8

ADDI R2,R2,#8

S.D-A F2,-8(R2)

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

11

12

114

115

116

117

118

119

13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-		-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	-		-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict

12

13

16

18

16

19

Ex_End

3

Cache

4

CDB

5

4

13

14

17

Retire

6

7

18

19

20

21

Comments

No ROB required for I15

Wait for R2

Wait for ROB and F2

CDB Conflict

Ex_Start

12

13

16

18

16

Issue

2

2

11

12

15

17

15

1 (7)

1 (6)

10 (0)

11 (0)

11 (0)

13 (1)

13 (0)

Problem 3.15 – a. Conservative Disambiguation

L.D F2,0(R1)

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	LD F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-		Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	· ·	(13)	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
117	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
118	BNEQ R1,R3,LOOP	13 (0)	15	16	16 -	V -	17	21	CDB Conflict

17

18

19

22

Wait for ROB

16

15 (1)

Problem 3.15 - a. Conservative Disambiguation Dispatch

LD F2,0(R1)

ADDI R2,R2,#8

S.D-A F2,-8(R2)

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

11

115

116

117

118

119

12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-			Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9		10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	10	11	11	-			Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	11	12	12	14		15	Wait for 2 ROB entries, F2, IS retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	

13

16

18

16

17

19

18

Ex_End

3

Cache

CDB

5

14

17

19

Retire

6

19

20

21

22

Comments

No ROB required for I15

Wait for R2

Wait for ROB and F2

CDB Conflict

Wait for ROB

Ex_Start

13

16

18

16

17

Issue

2

12

15

17

15

16

1 (7)

11 (0)

11 (0)

13 (1)

13 (0)

15 (1)

Problem 3.15 - b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8								
14	S.D-A F2,-8(R2)								
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	3	4	4	-	5		CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (4)							
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 - b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (4)							
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 - b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (4)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)								
16	BNEQ R1,R3,LOOP								
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 - b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5		6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7 6	8	8	- 4	8 -	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)							
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 - b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8		-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)								
18	ADDI R1,R1,#8								
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6 /	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)							
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	5	6	6				FU conflict with I6
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
111	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	6	7	7	-	8		FU conflict, CDB conflict
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	issue	Ex_Start	EX_End	Cacne	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8								
110	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8	5 (0)	6	7	7	-	8		CDB conflict
I10	S.D-A F2,-8(R2)	5 (0)							
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
110	S.D-A F2,-8(R2)	5 (0)							
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
110	S.D-A F2,-8(R2)	5 (0)	11 🙋	12	12	-).	-	Wait for R2
111	S.D-D F2,-8(R2)								
112	BNEQ R1,R3,LOOP								
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 - b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7)	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-/	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	/-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	/	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8		9	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	(14)	CDB conflict, FU conflict
110	S.D-A F2,-8(R2)	5 (0)	11	12	(12)	3 - 14	·/	<u> </u>	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)							
113	L.D F2,0(R1)								
114	ADDI R1,R1,#8								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	- /	-	-	Wait for R2
l11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10 🕢	11	11	-	12	16	Wait for R1
113	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

ADDI R1,R1,#8

114

10 (0)

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9 /	13	FU conflict, CDB conflict
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	1.0	14	CDB conflict, FU conflict
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-/-		-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1
113	L.D F2,0(R1)	10 (1)	11	12	12				Wait for 2 ROB entries, FU conflict

Problem 3.15 - b. Speculative Disambiguation Dispatch

L.D F2,0(R1)

ADDI R1,R1,#8

ADDI R2,R2,#8

S.D-A F2,-8(R2)

S.D-D F2.-8(R2)

BNEQ R1,R3,LOOP

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

ADDI R1.R1.#8

11

12

13

14

15

16

111

112

113

114

17	L.D F2,0(R1)	4 (2)	5	6	6	7	8
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-

9

10

12

Issue

2

2

4

7

6

5

1 (7)

1 (6)

2 (5)

2 (5)

3 (4)

3 (3)

7 (1)

7 (0)

10(1)

10 (0)

12

13 13 14

Ex_Start

3

3

5

8

7

6

10

11

Ex_End

3

3

5

8

7

6

10

11

Cache

4

9

14

CDB

5

4

6

7

Retire

6

7

8

10

11

12 13

14

15

16

Comments

CDB conflict with I1

Wait for R2 Wait for F2. Address and

13 retire (for cache)

Wait for R1

FU conflict, CDB conflict

CDB conflict, FU conflict Wait for R2 Wait for 2 ROB entries.

F2, I9 retire

Wait for R1

Wait for 2 ROB entries, FU

conflict, Cache Conflict

In Parenthesis: Remainina ROB entries

Problem 3.15 - b. Speculative Disambiguation Dispatch

L.D F2,0(R1)

ADDI R1,R1,#8

ADDI R2,R2,#8

S.D-A F2,-8(R2)

S.D-D F2.-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

11

12

13

14

15

16

17

112

113

18	ADDI K1,K1,#8	4 (1)	/	8	8	-
19	ADDI R2,R2,#8	5 (0)	8	9	9	-
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14

1 (7)

1 (6)

2 (5)

2 (5)

3 (4)

3 (3)

4(2)

7 (0)

10(1)

14	15

	4001040404	10 (0)		
114	ADDI R1.R1.#8	10 (0)		

Ex_Start

3

3

5

8

7

6

6

11

14

Issue

2

2

4

7

6

5

5

10

13

Ex_End

3

3

5

8

7

6

6

11

Cache

4

9

7

CDB

5

4

6

7

8

9

10

12

16

Retire

6

7

8

10

11

12 13

14

15

16

17

Comments

CDB conflict with I1

Wait for R2 Wait for F2. Address and

13 retire (for cache)

Wait for R1

FU conflict, CDB conflict

CDB conflict, FU conflict Wait for R2 Wait for 2 ROB entries,

F2, I9 retire

Wait for R1 Wait for 2 ROB entries, FU

conflict, Cache Conflict

Dispatch Issue

11 L.D F2,0(R1) 1 (7) 2

1 (6)

2 (5)

2 (5)

7 (1)

7 (0)

10(1)

10 (0)

ADDI R1,R1,#8

ADDI R2,R2,#8

S.D-A F2,-8(R2)

C D D E2 0/02\

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

ADDI R1.R1.#8

Problem 3.15 - b. Speculative Disambiguation

12

13

14

111

112

113

114

15	S.D-D F2,-8(R2)	3 (4)	ь	/	/	9	-	10
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-

9

10

13

11

2

4

7

Ex_Start

3

3

5

8

10

11

14

12

Ex_End

3

3

5

8

10

11

14

12

In Parenthesis: Remainina ROB entries

Cache

4

CDB

5

4

6

12

16

13

Retire

6

7

8

15

16

17

18

Comments

CDB conflict with I1

Wait for R2
Wait for F2. Address and

I3 retire (for cache)
Wait for R1

FU conflict, CDB conflict
CDB conflict, FU conflict
Wait for R2
Wait for 2 ROB entries

F2, I9 retire

Wait for R1

Wait for 2 ROB entries, FU

conflict, Cache Conflict

14

Problem 3.15 – b. Speculative Disambiguation

L.D F2,0(R1)

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-		Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	,11	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	8	9	9	. ,	10	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	11	12	12		-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	21	11	-	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	-		-	Wait for R2
117	S.D-D F2,-8(R2)								
118	BNEQ R1,R3,LOOP								

Problem 3.15 – b. Speculative Disambiguation

119

BNEQ R1,R3,LOOP

L.D F2,0(R1)

13 (0)

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	- /	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	/-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	/	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12		13	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13		14	(19)	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	JF - 12		<i>-</i> .	Wait for R2
117	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2

Problem 3.15 - b. Speculative Disambiguation Dispatch

118

119

BNEQ R1,R3,LOOP

L.D F2,0(R1)

13 (0)

14

11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9		10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14		15	Wait for 2 ROB entries, F2, Is retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13		14	19	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
117	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2

15

15

Ex_Start

Issue

Ex_End

Cache

CDB

Retire

16

Comments

CDB Conflict

Problem 3.15 – b. Speculative Disambiguation

Dispatch

116

117

118

119

LD F2,0(R1)

ADDI R2,R2,#8

S.D-A F2,-8(R2)

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

L.D F2,0(R1)

12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	

13

16

18

16

19

13

16

18

16

Ex_End

Cache

4

CDB

5

14

17

19

20

21

Retire

Comments

No ROB required for I15

Wait for R2

Wait for ROB and F2

CDB Conflict

Ex_Start

Issue

2

12

15

17

15

1 (7)

11 (0)

11 (0)

13 (1)

13 (0)

Problem 3.15 – b. Speculative Disambiguation

L.D F2,0(R1)

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
11	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-		Wait for R2
15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
17	LD F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	- \	Wait for R2
111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
113	LD F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
114	ADDI R1,R1,#8	10 (0)	11	12	12	· ·	(13)	18	
115	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
116	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
117	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
118	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict

17

18

19

22

Wait for ROB

16

15 (1)

Problem 3.15 – b. Speculative Disambiguation

Dispatch

L.D F2,0(R1)

ADDI R2,R2,#8

S.D-A F2,-8(R2)

S.D-D F2,-8(R2)

BNEQ R1,R3,LOOP

LD F2,0(R1)

11

115

116

117

118

119

12 ADDI R1,R1,R8 1 (6) 2 3 3 - 4 7 13 ADDI R2,R2,R8 2 (5) 4 5 5 - 6 8 CDB conflict with 11 14 S.D-A F2,8(R2) 2 (5) 7 8 8 - - - Wait for R2 15 S.D-D F2,8(R2) 3 (4) 6 7 7 9 - 10 Wait for F2, Address and 13 retire (for cache) are retire (for cache) 16 BNEQ R1,R3,LOOP 3 (3) 5 6 6 - 7 11 Wait for R1 17 LD F2,O(R1) 4 (2) 5 6 6 7 8 12 Wait for R1 18 ADDI R1,R1,R8 4 (1) 7 8 8 - 9 13 FU conflict with 16 19 ADDI R2,R2,R8 5 (0) 8 9 9 - 10 14 Wait for R2 110 S.D.A F2,8(R2) 5 (0) 11 <th></th>										
I4 S.D.A.FZ8(R2) 2 (5) 7 8 8 - - Wait for R2 I5 S.D.D.FZ8(R2) 3 (4) 6 7 7 9 - 10 Wait for R2. Address and I3 retire (for cache) I6 BNEQ.R1,R3,LOOP 3 (3) 5 6 6 - 7 11 Wait for R1 I7 L.D.FZ,O(R1) 4 (2) 5 6 6 7 8 12 Wait for R1 I8 A.D.DI R1,R1,HB 4 (1) 7 8 8 - 9 13 FU conflict with I6 I9 A.D.DI R2,R2,HB 5 (0) 8 9 9 - 10 14 Wait for R2 I10 S.D.A.F2,-8(R2) 5 (0) 11 12 12 - - Wait for 2 ROB entries, F2, 19 return I11 S.D.D.F2,-8(R2) 7 (1) 9 10 10 14 - 15 Wait for 2 ROB entries, F2, 19 return I12 BNEQ.R1,R3,LOOP	12	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
IS S.D-D FZ8(R2) 3 (4) 6 7 7 9 - 10 Walt for F2_Address and I3 retrie (for cache) I6 BNEQ R1,R3,L(ODP) 3 (3) 5 6 6 - 7 11 Walt for P1 I7 LD F2,Q(R1) 4 (2) 5 6 6 7 8 12 Walt for P2 ADD R2_R2_R2_R2 I8 ADDI R1,R1,R8 4 (1) 7 8 8 - 9 13 FU conflict with I6 I9 ADDI R2,R2,R8 5 (0) 8 9 9 - 10 14 Walt for R2 110 5.D-AF2_R8(R2) 5 (0) 11 12 12 - - Wait for R2 RD8 entries, F2_R8 111 5.D-DF2_R8(R2) 7 (1) 9 10 10 14 - 15 Wait for R2 RD8 entries, F2_R8 112 BNEQ R1,R3,LODP 7 (0) 10 11 11 - 12 16 Wait for R1,CD8 conflict 113	13	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
S.U.D.F.Z8R.Z.] 3 (4) 6	14	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
17	15	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	
18 ADDI RI,RI,H8 4(1) 7 8 8 - 9 13 FU conflict with I6 19 ADDI RI,RI,H8 5(0) 8 9 9 - 10 14 Wait for R2 10 S.DA.FZ,-8(R2) 5(0) 11 12 12 Wait for R2 11 S.DD.FZ,-8(R2) 7(1) 9 10 10 14 - 15 Wait for R2 12 BNEQ RI,RI,J.ODP 7(0) 10 11 11 - 12 16 Wait for R1,CDB conflict 13 L.D.FZ,O(R1) 10(1) 13 14 14 15 16 17 Wait for 2 ROB entries, F2, I9 14 Conflict Cache conflict Cache conflict 15 Conflict Cache conflict Cache conflict 16 Conflict Cache conflict Cache conflict 17 Conflict Cache conflict Cache conflict 18 Cache Cac	16	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
19 ADDI R2,R2,M8 5 (0) 8 9 9 - 10 14 Wait for R2	17	LD F2,0(R1)	4 (2)	5	6	6	7	8	12	
110 S.D-A.FZ,8(R2) 5 (0) 11 12 12 - - Wait for R2 111 S.D-D.FZ,8(R2) 7 (1) 9 10 10 14 - 15 Wait for 2 ROB entries, FZ, IS 112 BNEQ.R1,R3,LOOP 7 (0) 10 11 11 - 12 16 Wait for RX, COB conflict 113 LD FZ,O(R1) 10 (1) 13 14 14 15 16 17 Wait for ZROB entries, FZ, IS	18	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
III S.D-D FZ,8(R2) 7 (1) 9 10 10 14 - 15 Wait for 2 ROB entries, F2, IE retire III2 BNEQ R1,R3,LOOP 7 (0) 10 11 11 - 12 16 Wait for R1, CDB conflict II3 LD FZ,Q(R1) 10 (1) 13 14 14 15 16 17 Wait for Z ROB entries, F2, IE retire	19	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
111 SLD-PZ-(RRZ) 7(1) 9 10 10 14 - 15 rettre 112 BNEQ R1,R3,LOOP 7(0) 10 11 11 - 12 16 Wait for IX, OB conflict 113 LD FZ,Q(R1) 10 (1) 13 14 14 15 16 17 Wait for Z ROB entires, FU conflict, Cache conflict	110	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
113 LD F2,0(R1) 10 (1) 13 14 14 15 16 17 Walt for 2 ROB entries, FU conflict, Cache conflict	111	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	
113 LDF2,0(R1) 10 (1) 13 14 14 15 16 17 conflict, Cache conflict	112	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
114 ADDI R1,R1,#8 10 (0) 11 12 12 - 13 18	113	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	
	114	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	

13

16

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16

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18

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16

18

16

17

Ex_End

3

Cache

4

CDB

5

14

17

19

Retire

6

19

20

21

22

Comments

No ROB required for I15

Wait for R2

Wait for ROB and F2

CDB Conflict

Wait for ROB

Ex_Start

Issue

2

12

15

17

15

16

1 (7)

11 (0)

11 (0)

13 (1)

13 (0)

15 (1)

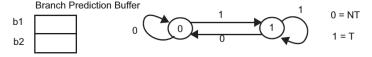
Agenda

- ▶ Problem 3.13
- ▶ Problem 3.15
- Problem 3.16

Problem 3.16

```
Consider the following code segment for a loop:
      if (x is odd) then < -(branch b1)
        increment a < -(b1 untaken)
 if (x is a multiple of 5) then < -(branch b2)
        increment b < -(b2 untaken)
Assume that the following list of 9 values of x is processed by 9
iterations of this loop: 8
9
10
11
20
29
30
31
```

3.16(a) (one-bit state machine)



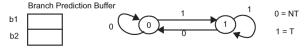
(a) BPB with 1-bit predictor

Assume that a one-bit state machine (see Figure 3.46(a)) is used as the prediction algorithm for predicting the execution of the two branches in this loop.

Show the predicted and actual branch directions of both b1 and b2 branch instructions for each iteration of this loop. Assume the initial state is 0, i.e. NT (not taken), for the predictor.

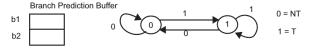
What are the prediction accuracies for b1 and for b2?

What is the overall prediction accuracy for both branches?



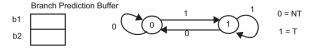
(a) BPB with 1-bit predictor

Value	Branch	b1	Branch	b2
of x	Predicticed	Actual	Predicticed	Actual
8	0	1		



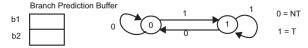
(a) BPB with 1-bit predictor

Value	Branch	b1	Branch b2		
of x	Predicticed	Actual	Predicticed	Actual	
8	0	1	0	1	



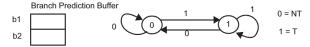
(a) BPB with 1-bit predictor

Value	Branch	b1	Branch b2		
of x	Predicticed	Actual	Predicticed	Actual	
8	0	1	0	1	
9	1	0			



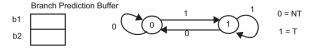
(a) BPB with 1-bit predictor

Value	Branch	b1	Branch b2		
of x	Predicticed	Actual	Predicticed	Actual	
8	0	1	0	1	
9	1	0	1	1	



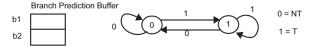
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1		



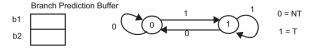
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0



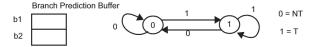
(a) BPB with 1-bit predictor

Value	Branch b1		Branch	b2
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0		



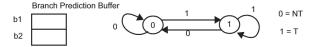
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1



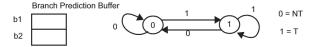
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0		



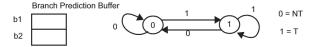
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1



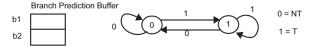
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1		



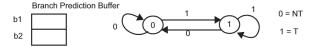
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0



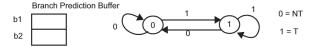
(a) BPB with 1-bit predictor

Value	Branch b1		Branch	b2
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0		



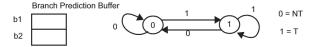
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1



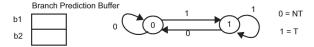
(a) BPB with 1-bit predictor

Value	Branch b1		Branch	b2
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1		



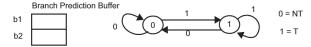
(a) BPB with 1-bit predictor

Value	Branch b1		Branch b2	
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1	1	0



(a) BPB with 1-bit predictor

Value	Branch	b1	Branch	b2
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1	1	0
31	1	0		



(a) BPB with 1-bit predictor

Value	Branch	b1	Branch	b2
of x	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1	1	0
31	1	0	0	1

3.16(a) (Prediction accuracy)

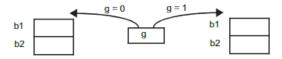
Value	Br	anch b1		Branch b2				
of x	Predicticed	Actual	Actual Success Predicticed		Actual	Success		
8	0	1	0	0	1	0		
9	1	0	0	1	1	1		
10	0	1	0	1	0	0		
11	1	0	0	0	1	0		
7	0	0	1	1	1	1		
20	0	1	0	1	0	0		
29	1	0	0	0	1	0		
30	0	1	0	1	0	0		
31	1	0	0	0	1	0		

Prediction Accuracy b1 = 1/9 = 11%

Prediction Accuracy b2 = 2/9 = 22%

Overall Prediction Accuracy = 3/18 = 16.6%

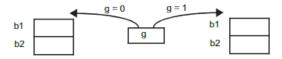
(a) BPB with 1-bit predictor



(b) BPB with 1-bit predictors and 1-bit global history

In addition to the one-bit predictor, a one-bit global history register (g) is used. g stores the direction of the last executed branch (which may or may not be the same branch as the branch currently being predicted) and is used to indexinto two separate one-bit predictor tables as shown Figure 3.46(b).

(a) BPB with 1-bit predictor



(b) BPB with 1-bit predictors and 1-bit global history

Depending on the value of g, one of the two predictor table is selected and used for the normal one-bit prediction. Again, fill in the predicted and actual branch directions of b1 and b2 for nine itera-tions of the loop. The initial state of the predictor tables is all 0's.What are the prediction accuracies for b1 and b2?What is the overall prediction accuracy?

. , .										
			g = 0					g =	= 1	
Value	Branch	g		b1		b2		b1	b2	
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-

			g = 0				g = 1				
Value	Branch	g		b1		b2		b1		b2	
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	

			g = 0				g = 1				
Value	Branch	g	b1 b2			b1	b2				
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
0	b2	1	1	-	0	1	0	-	0	1	

			g = 0				g = 1				
Value	Branch	g		b1		b2		b1	b2		
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	

			g = 0				g = 1				
Value	Branch	g		b1		b2		b1	b2		
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
9	b2	0	1	-	0	1	0	-	1	1	

				g = 0				g = 1			
Value	Branch	g		b1		b2		b1	b2		
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
9	b2	0	1	-	0	1	0	-	1	1	
10	b1	1	1	1	1	-	0	1	1	-	

				g =	= 0		g = 1				
Value	Branch	g		b1 b2		b2		b1	b2		
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
0	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
9	b2	0	1	-	0	1	0	-	1	1	
10	b1	1	1	1	1	-	0	1	1	-	
10	b2	1	1	-	1	0	1	-	1	0	

				g =	= 0			g =	= 1	
Value	Branch	g		b1		b2		b1		b2
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
9	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
10	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-

				g =	= 0			g =	= 1	
Value	Branch	g		b1		b2		b1		b2
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
9	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
10	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
11	b2	0	0	-	1	1	1	-	0	1

				g =	= 0		g = 1			
Value	Branch	g		b1		b2		b1		b2
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
9	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
10	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-

				g =	= 0			g =	= 1			
Value	Branch	g		b1		b2		b1	b2			
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual		
Initial State		0	0	-	0	-	0	-	0	-		
8	b1	0	0	1	0	-	0	1	0	-		
	b2	1	1	-	0	1	0	-	0	1		
9	b1	1	1	0	0	-	0	0	1	-		
9	b2	0	1	-	0	1	0	-	1	1		
10	b1	1	1	1	1	-	0	1	1	-		
10	b2	1	1	-	1	0	1	-	1	0		
11	b1	0	1	0	1	-	1	0	0	-		
"	b2	0	0	-	1	1	1	-	0	1		
7	b1	1	0	0	1	-	1	0	0	-		
'	b2	0	0	-	1	1	0	-	0	1		

				g =	= 0			g = 1			
Value	Branch	g		b1		b2		b1	b2		
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
9	b2	0	1	-	0	1	0	-	1	1	
10	b1	1	1	1	1	-	0	1	1	-	
10	b2	1	1	-	1	0	1	-	1	0	
11	b1	0	1	0	1	-	1	0	0	-	
11	b2	0	0	-	1	1	1	-	0	1	
7	b1	1	0	0	1	-	1	0	0	-	
'	b2	0	0	-	1	1	0	-	0	1	
20	b1	1	0	1	1	-	0	1	0	-	

				g =	= 0			g =	= 1	
Value	Branch	g		b1 b2		b2		b1	b2	
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
9	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
10	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
11	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
'	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
20	b2	1	0	-	1	0	1	-	0	0

			g = 0					g =	= 1		
Value	Branch	g		b1		b2		b1		b2	
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
0	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
9	b2	0	1	-	0	1	0	-	1	1	
10	b1	1	1	1	1	-	0	1	1	-	
10	b2	1	1	-	1	0	1	-	1	0	
11	b1	0	1	0	1	-	1	0	0	-	
11	b2	0	0	-	1	1	1	-	0	1	
7	b1	1	0	0	1	-	1	0	0	-	
'	b2	0	0	-	1	1	0	-	0	1	
20	b1	1	0	1	1	-	0	1	0	-	
20	b2	1	0	-	1	0	1	-	0	0	
29	b1	0	0	0	1	-	1	0	0	-	

				g =	= 0			g =	= 1	b2	
Value	Branch	g		b1		b2		b1		b2	
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
9	b2	0	1	-	0	1	0	-	1	1	
10	b1	1	1	1	1	-	0	1	1	-	
10	b2	1	1	-	1	0	1	-	1	0	
11	b1	0	1	0	1	-	1	0	0	-	
11	b2	0	0	-	1	1	1	-	0	1	
7	b1	1	0	0	1	-	1	0	0	-	
'	b2	0	0	-	1	1	0	-	0	1	
20	b1	1	0	1	1	-	0	1	0	-	
20	b2	1	0	-	1	0	1	-	0	0	
29	b1	0	0	0	1	-	1	0	0	-	
29	b2	0	0	-	1	1	1	-	0	1	

				g =	= 0			g =	= 1	0 - 0 - 0 1 1 - 1 1			
Value	Branch	g		b1		b2		b1		b2			
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual			
Initial State		0	0	-	0	-	0	-	0	-			
8	b1	0	0	1	0	-	0	1	0	-			
0	b2	1	1	-	0	1	0	-	0	1			
9	b1	1	1	0	0	-	0	0	1	-			
9	b2	0	1	-	0	1	0	-	1	1			
10	b1	1	1	1	1	-	0	1	1	-			
10	b2	1	1	-	1	0	1	-	1	0			
11	b1	0	1	0	1	-	1	0	0	-			
11	b2	0	0	-	1	1	1	-	0	1			
7	b1	1	0	0	1	-	1	0	0	-			
,	b2	0	0	-	1	1	0	-	0	1			
20	b1	1	0	1	1	-	0	1	0	-			
20	b2	1	0	-	1	0	1	-	0	0			
29	b1	0	0	0	1	-	1	0	0	-			
29	b2	0	0	-	1	1	1	-	0	1			
30	b1	1	0	1	1	-	1	1	0	-			

			g = 0				g=1			
Value	Branch	g		b1		b2		b1		b2
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
9	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
10	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
11	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
20	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
29	b2	0	0	-	1	1	1	-	0	1
30	b1	1	0	1	1	-	1	1	0	-
30	b2	1	0	-	1	0		-	0	0

				g = 0				g = 1			
Value	Branch	g		b1		b2		b1		b2	
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual	
Initial State		0	0	-	0	-	0	-	0	-	
8	b1	0	0	1	0	-	0	1	0	-	
	b2	1	1	-	0	1	0	-	0	1	
9	b1	1	1	0	0	-	0	0	1	-	
	b2	0	1	-	0	1	0	-	1	1	
10	b1	1	1	1	1	-	0	1	1	-	
10	b2	1	1	-	1	0	1	-	1	0	
11	b1	0	1	0	1	-	1	0	0	-	
""	b2	0	0	-	1	1	1	-	0	1	
7	b1	1	0	0	1	-	1	0	0	-	
,	b2	0	0	-	1	1	0	-	0	1	
20	b1	1	0	1	1	-	0	1	0	-	
20	b2	1	0	-	1	0	1	-	0	0	
29	b1	0	0	0	1	-	1	0	0	-	
29	b2	0	0	-	1	1	1	-	0	1	
30	b1	1	0	1	1	-	1	1	0	-	
30	b2	1	0	-	1	0		-	0	0	
31	b1	0	0	0	1	-		0	0	-	

			g = 0					g =	= 1	
Value	Branch	g		b1		b2		b1		b2
of x			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
9	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
10	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
11	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
'	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
20	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
29	b2	0	0	-	1	1	1	-	0	1
30	b1	1	0	1	1	-	1	1	0	-
30	b2	1	0	-	1	0		-	0	0
31	b1	0	0	0	1	-		0	0	-
	b2	0	0	-	1	1		-	0	1

```
Prediction Accuracy b1 = 4/9 = 44.4\%
Prediction Accuracy b2 = 6/9 = 66.7\%
Overall Prediction Accuracy = 10/18 = 55.5\%
```

What is the prediction success rate for branch b2 when g=0? Explain why this is.

Prediction Accuracy b2 = 4/5 = 80%

Among the numbers 8,9,10,11,7,20,29,30,31 There is no odd number which is also a multiple of 5.

Once predictor is warmed-up, b2 branch with g=0 is highly predictable. g=0 means the previous branch was not taken (odd) then since there are no odd numbers which is a multiple of 5 in the list, second branch will always be taken