Computer Architecture
DAT105
Exercise Session 3

Piyumal Ranawaka (piyumal@chalmers.se)

Chalmers University of Technology, Sweden

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Agenda

- Problem 3.13
- Problem 3.15
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- Problem 3.13
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Problem 3.13

In this problem we compare the performance of three dynamically scheduled processor architectures on a simple piece of code computing $Y = Y * X + Z$, where X,Y and Z are (double-precision-8bytes) floating-point vectors. Using the core ISA of Table 3.3 in the notes, the loop body can be compiled as follows:.

```
LOOP:  L.D F0,0(R1)       X[i] loaded in F0
       L.D F2,0(R2)       Y[i] loaded in F2
       L.D F4,0(R3)       Z[i] loaded in F4
       MUL.D F6,F2,F0     Multiply X by Y
       ADD.D F8,F6,F4     Add Z
       ADDI R1,R1,#8      update address registers
       ADDI R2,R2,#8
       ADDI R3,R3,#8
       S.D F8, -8(R2)     store in Y[i]
       BNE R4,R2,LOOP     (R4)-8 points to the last element of Y
```

3.13(a) (Tomasulo algorithm–no speculation)

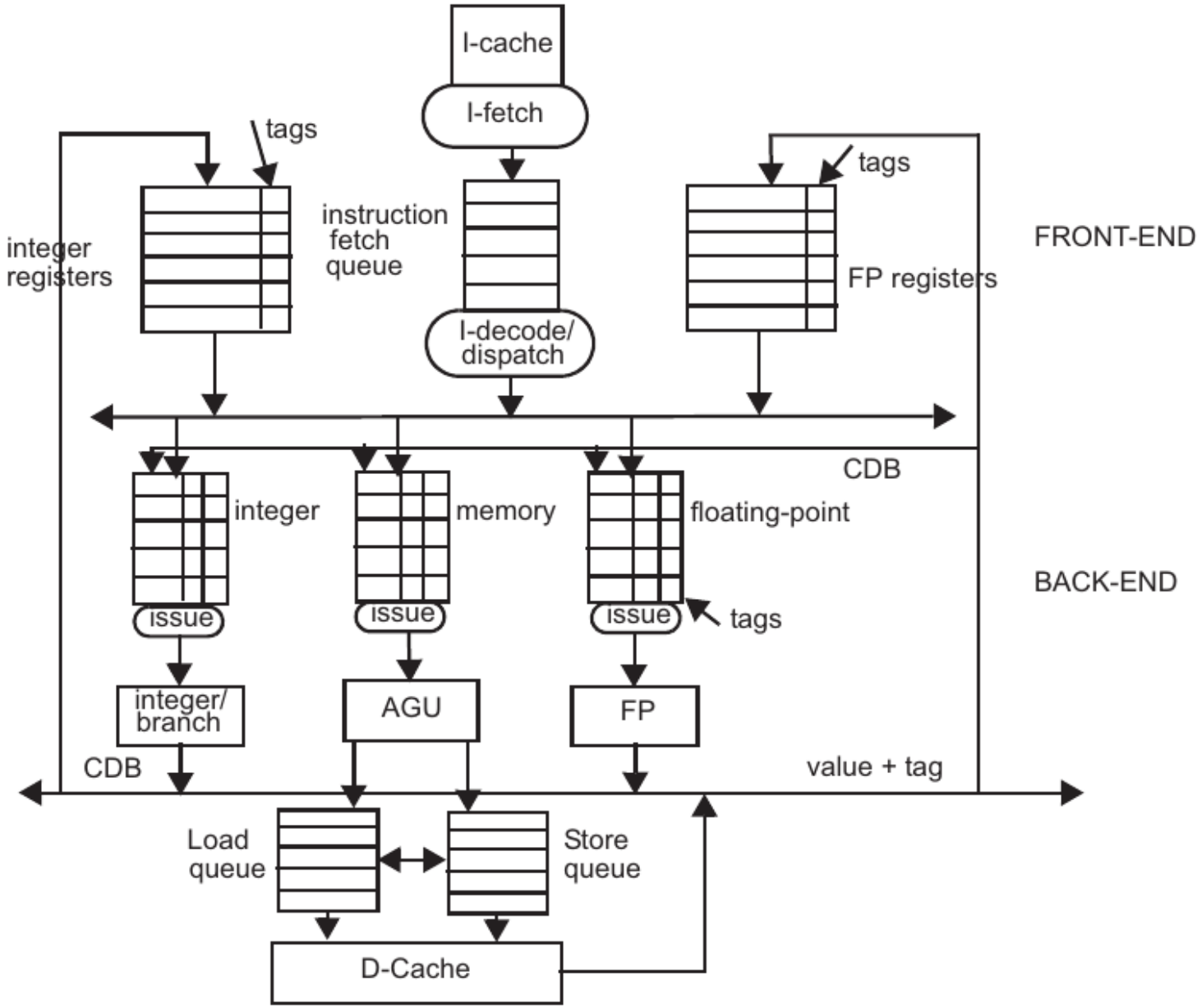


Figure 3.15. Hardware for Tomasulo algorithm

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	wait for R2

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	–	wait for F8

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	–	wait for F8
I11	BNE R4,R2,LOOP	11	12	(13)	13	–	(14)	

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	–	wait for F8
I11	BNE R4,R2,LOOP	11	12	(13)	13	–	(14)	
I12	L.D F0,0(R1)	15	16	(17)	17	(18)	(19)	wait for I11 in dispatch

3.13(a) (Tomasulo algorithm–no speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	(23)	–	wait for F8
I11	BNE R4,R2,LOOP	11	12	(13)	13	–	(14)	
I12	L.D F0,0(R1)	15	16	(17)	17	(18)	(19)	wait for I11 in dispatch

3.13(b) (Tomasulo algorithm with speculation)

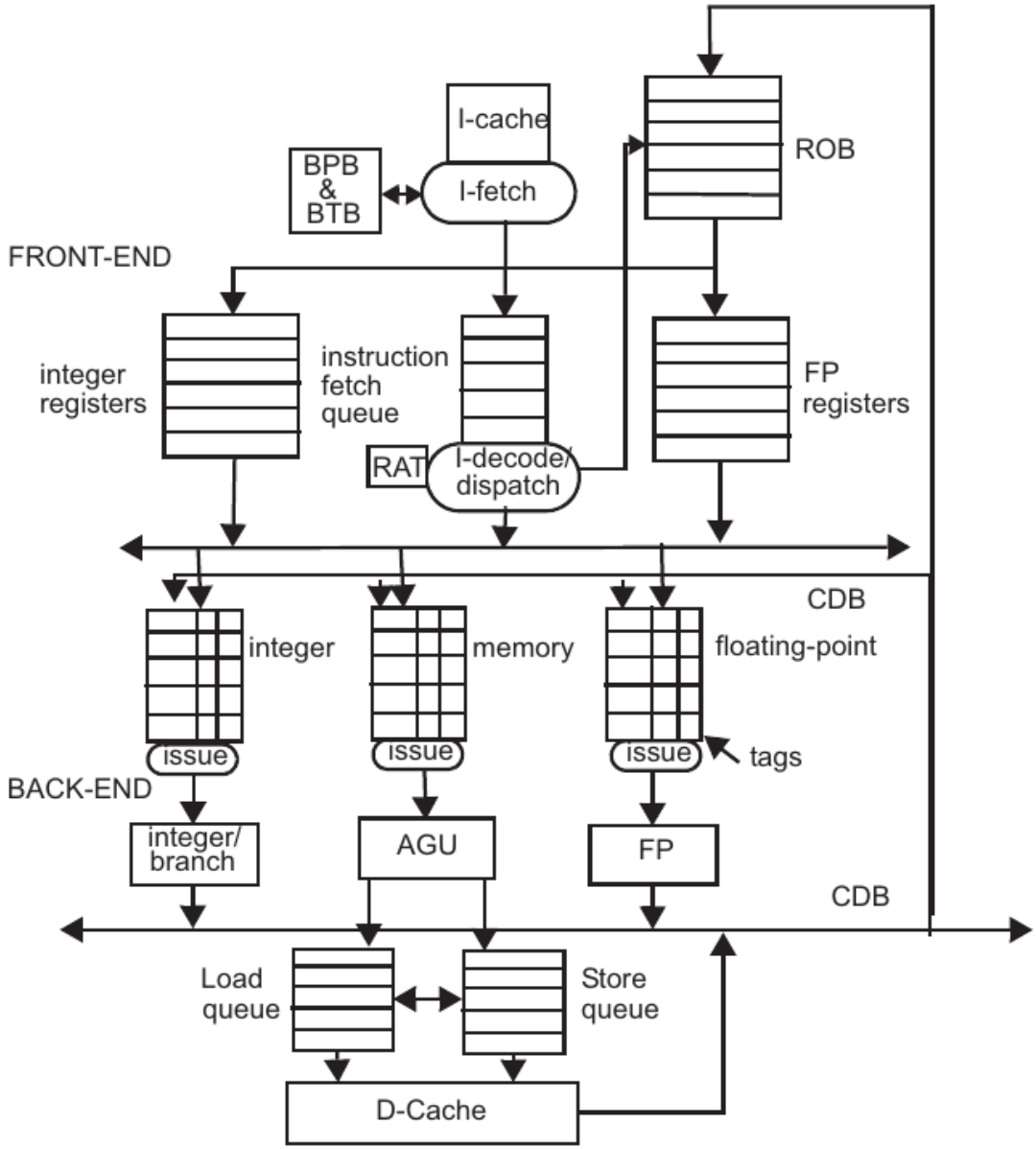


Figure 3.23. Tomasulo algorithm with support for speculative execution

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	23	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	23	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	24	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	23	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	24	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	–	wait for R2

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	23	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	24	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	24	–	25	wait for F8, then wait to reach top of ROB

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	23	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	24	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	24	–	25	wait for F8, then wait to reach top of ROB
I11	BNE R4,R2,LOOP	11	12	(13)	13	–	(14)	26	

3.13(b) (Tomasulo algorithm with speculation)

	Instruction	Dispatch	Issue	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	(3)	3	(4)	(5)	6	
I2	L.D F2,0(R2)	2	3	(4)	4	(5)	(6)	7	
I3	L.D F4,0(R3)	3	4	(5)	5	(6)	(7)	8	
I4	MUL.D F6,F2,F0	4	7	(8)	12	–	(13)	14	wait for F2
I5	ADD.D F8,F6,F4	5	14	(15)	19	–	(20)	21	wait for F6
I6	ADDI R1,R1,#8	6	7	(8)	8	–	(9)	22	
I7	ADDI R2,R2,#8	7	8	(9)	9	–	(10)	23	
I8	ADDI R3,R3,#8	8	9	(10)	10	–	(11)	24	
I9	S.D F8, -8(R2)	9	11	(12)	12	–	–	–	wait for R2
I10	S.D F8, -8(R2)	10	21	(22)	22	24	–	25	wait for F8, then wait to reach top of ROB
I11	BNE R4,R2,LOOP	11	12	(13)	13	–	(14)	26	
I12	L.D F0,0(R1)	12	13	(14)	14	(15)	(16)	27	Address of store is known since cycle 13

3.13(c) (Speculative scheduling)

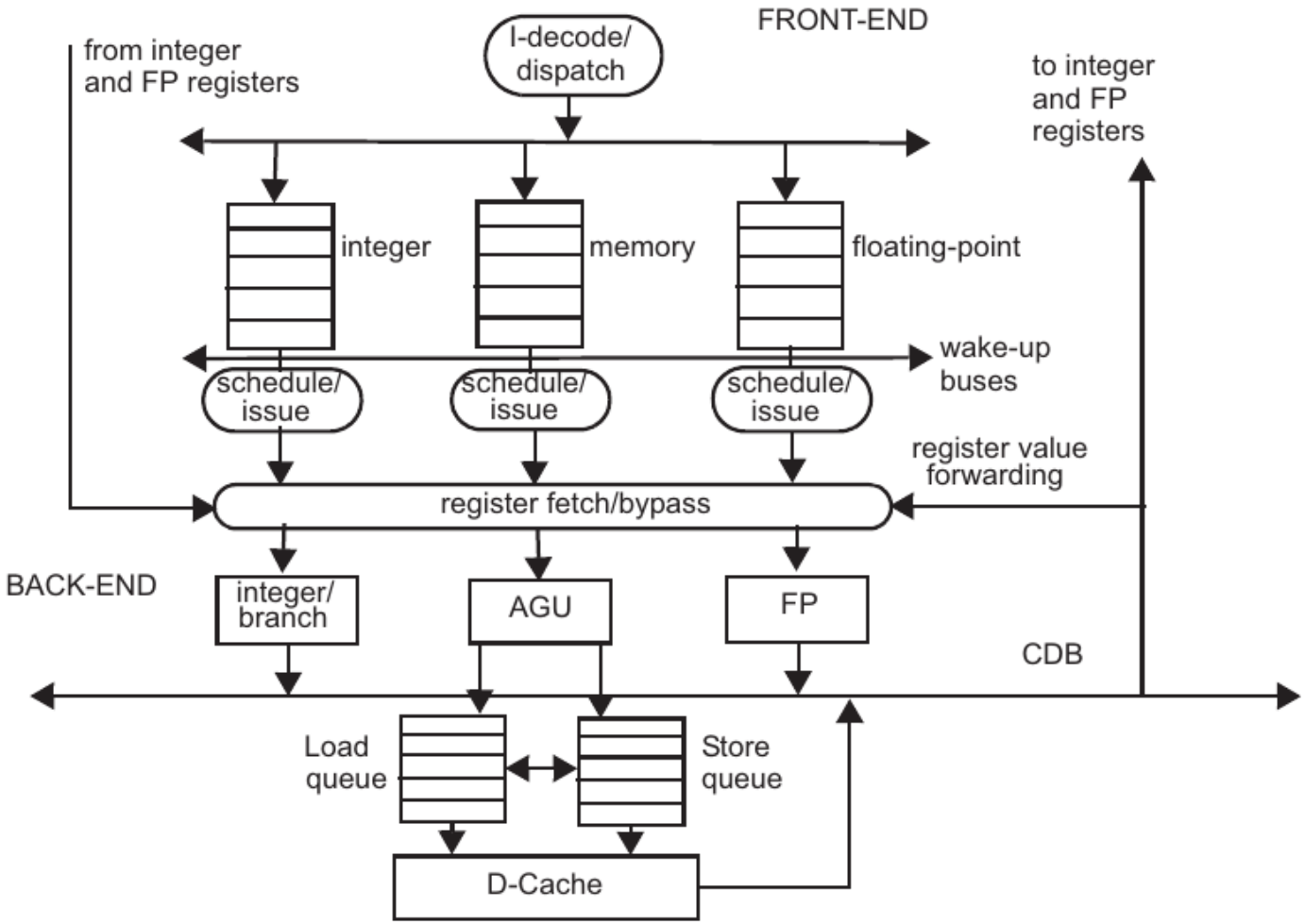


Figure 3.27. Back-end for a speculative microarchitecture with speculative scheduling

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	
I7	ADDI R2,R2,#8	7	8	9	(10)	10	–	(11)	20	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	
I7	ADDI R2,R2,#8	7	8	9	(10)	10	–	(11)	20	
I8	ADDI R3,R3,#8	8	10	11	(12)	12	–	(13)	21	CDB conflict with I4

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	
I7	ADDI R2,R2,#8	7	8	9	(10)	10	–	(11)	20	
I8	ADDI R3,R3,#8	8	10	11	(12)	12	–	(13)	21	CDB conflict with I4
I9	S.D F8, -8(R2)	9	10	11	(12)	12	–	–	–	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	
I7	ADDI R2,R2,#8	7	8	9	(10)	10	–	(11)	20	
I8	ADDI R3,R3,#8	8	10	11	(12)	12	–	(13)	21	CDB conflict with I4
I9	S.D F8, -8(R2)	9	10	11	(12)	12	–	–	–	
I10	S.D F8, -8(R2)	10	15	16	17	17	21	–	22	wait for F8 wait to reach top of ROB

3.13(c) (Speculative scheduling)

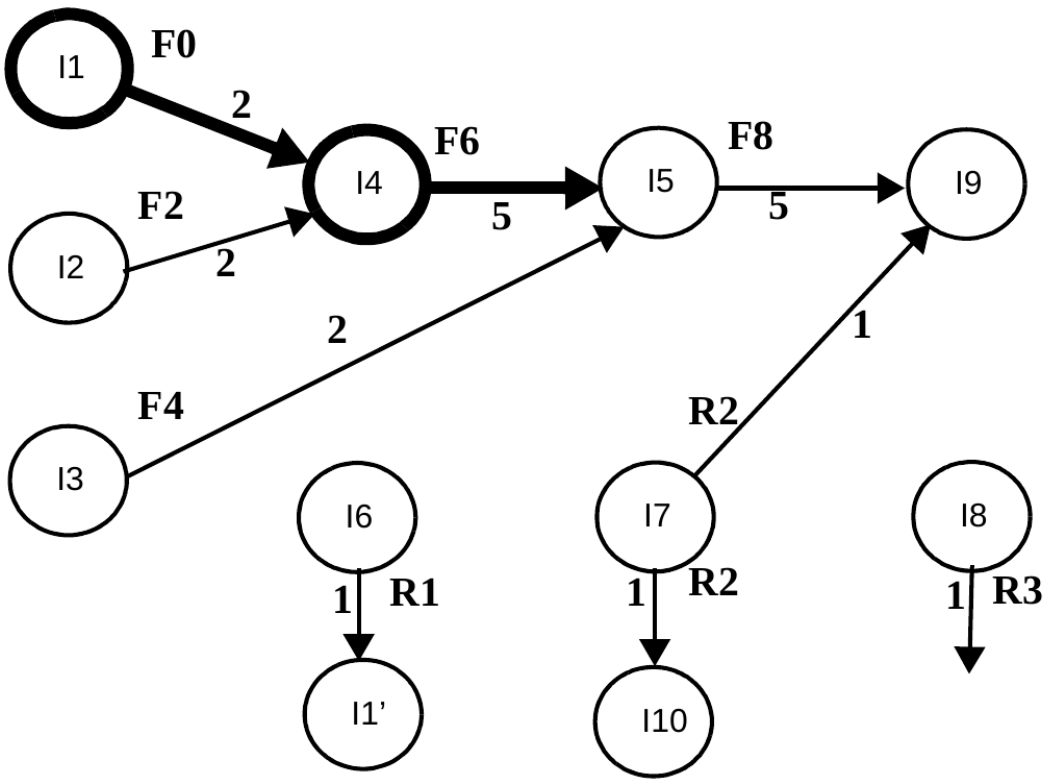
	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	
I7	ADDI R2,R2,#8	7	8	9	(10)	10	–	(11)	20	
I8	ADDI R3,R3,#8	8	10	11	(12)	12	–	(13)	21	CDB conflict with I4
I9	S.D F8, -8(R2)	9	10	11	(12)	12	–	–	–	
I10	S.D F8, -8(R2)	10	15	16	17	17	21	–	22	wait for F8 wait to reach top of ROB
I11	BNE R4,R2,LOOP	11	12	13	(14)	14	–	(15)	23	

3.13(c) (Speculative scheduling)

	Instruction	Dispatch	Issue	Register Fetch	Exec Start	Exec End	Cache	CDB	Retire	COMMENTS
I1	L.D F0,0(R1)	1	2	3	(4)	4	(5)	(6)	7	
I2	L.D F2,0(R2)	2	3	4	(5)	5	(6)	(7)	8	
I3	L.D F4,0(R3)	3	4	5	(6)	6	(7)	(8)	9	
I4	MUL.D F6,F2,F0	4	5	6	(7)	11	–	(12)	13	
I5	ADD.D F8,F6,F4	5	10	11	(12)	16	–	(17)	18	wait for F6
I6	ADDI R1,R1,#8	6	7	8	(9)	9	–	(10)	19	
I7	ADDI R2,R2,#8	7	8	9	(10)	10	–	(11)	20	
I8	ADDI R3,R3,#8	8	10	11	(12)	12	–	(13)	21	CDB conflict with I4
I9	S.D F8, -8(R2)	9	10	11	(12)	12	–	–	–	
I10	S.D F8, -8(R2)	10	15	16	17	17	21	–	22	wait for F8 wait to reach top of ROB
I11	BNE R4,R2,LOOP	11	12	13	(14)	14	–	(15)	23	
I12	L.D F0,0(R1)	12	14	15	(16)	16	(17)	(18)	24	CDB conflict with I5

3.13(d) (Data-flow graph)

LOOP:	L.D F0,0(R1)	X[i] loaded in F0
	L.D F2,0(R2)	Y[i] loaded in F2
	L.D F4,0(R3)	Z[i] loaded in F4
	MUL.D F6,F2,F0	Multiply X by Y
	ADD.D F8,F6,F4	Add Z
	ADDI R1,R1,#8	update address registers
	ADDI R2,R2,#8	
	ADDI R3,R3,#8	
	S.D F8, -8(R2)	store in Y[i]
	BNE R4,R2,LOOP	(R4)-8 points to the last element of Y



3.13(d) (Execution time comparisons)

Execution Time metric	Tomasulo w/o spec	Tomasulo with spec	Spec scheduling	Data-flow
Issue-to-issue	$16 - 2 = 14$	$13 - 2 = 11$	$14 - 2 = 12$	7
Execution-to-execution	$17 - 3 = 14$	$14 - 3 = 11$	$16 - 4 = 12$	7
Retirement	—	$27 - 6 = 21$	$24 - 7 = 17$	7

Agenda

- Problem 3.13
- Problem 3.15
- Problem 3.16

Problem 3.15

In this problem we explore the effect of memory disambiguation using a very simple move in memory

$$for(i = 0; i < 100; i++)$$

$$A[i] = B[i];$$

In this code vector A and B are in different areas of memory so that they don't have common elements. The assembly code is
LOOP:
L.D F2,0(R1)
ADDI R1,R1,#8
ADDI R2,R2,#8
S.D F2,-8(R2)
BNEQ R1,R3,LOOP

Problem 3.15

The architecture is the architecture of Problem 3.14 (Tomasulo with speculation and two-way dispatch). Fill Table 3.28. Fill the table for two cases:

- 1) Conservative (a Load is not issued to cache until the addresses of all previous Stores are know
- 2) Speculative (a Load is issued to cache optimistically when addresses of prior Stores are unknown).

Remember that Stores can only issue to cache once they are at the top of the ROB
Also assume that the number of ROB entries is limited to 7

3.15 (Tomasulo algorithm with speculation)

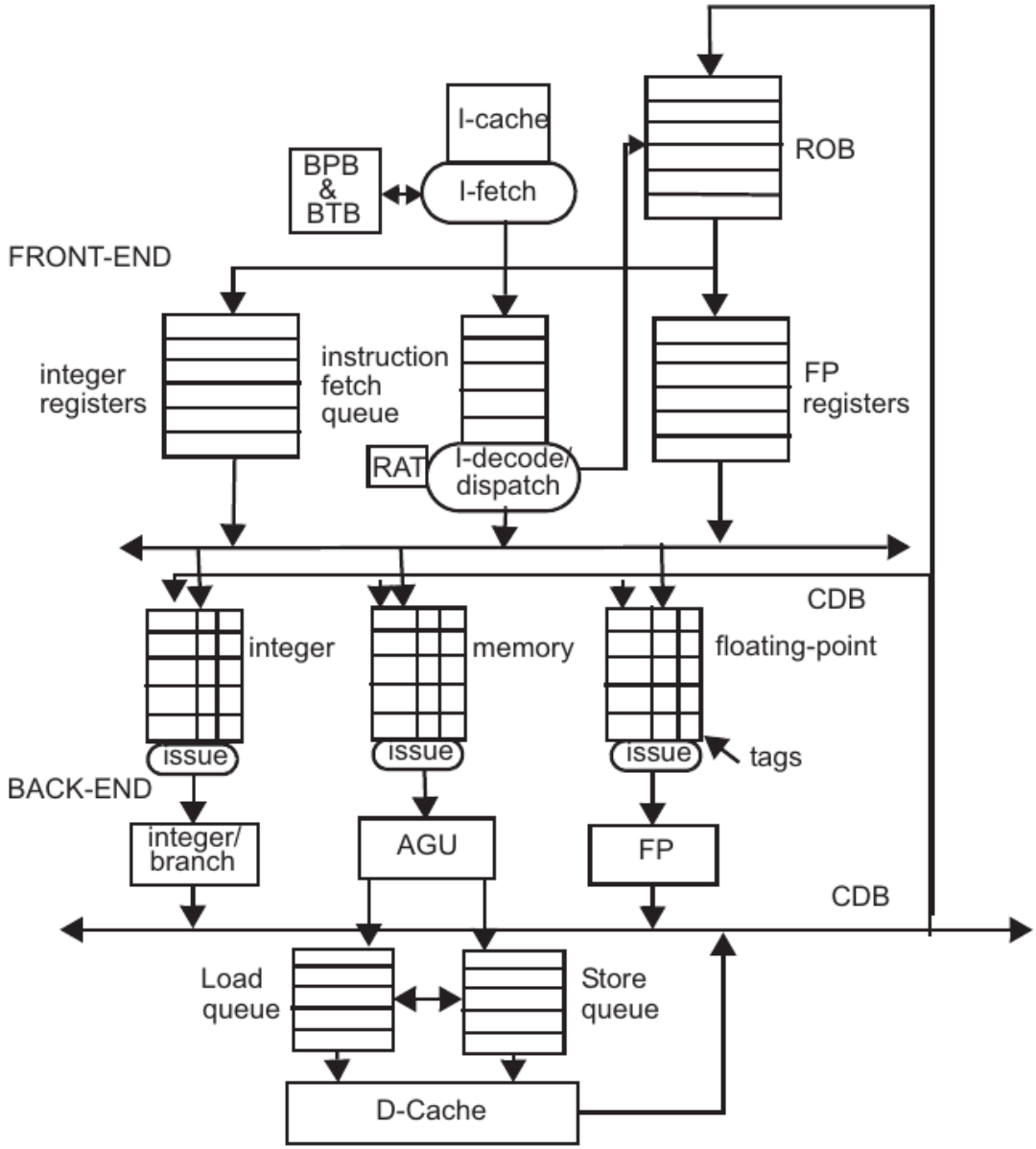


Figure 3.23. Tomasulo algorithm with support for speculative execution

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8								
I4	S.D-A F2,-8(R2)								
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	3	4	4	-	5		CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (4)							
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (4)							
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (4)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)							
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	9	10	12	Wait for previous store address, Cache Conflict
I8	ADDI R1,R1,#8	4 (1)							
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address, Cache Conflict
I8	ADDI R1,R1,#8	4 (1)							
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	5	6	6				FU conflict with I6
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	12	13	13	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)							
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	9	10	10	-	11	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	11	12	12				Wait for 2 ROB entries, FU conflict
I14	ADDI R1,R1,#8	10 (0)							

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	14			Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)							

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)							

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	

In Parenthesis: Remaining ROB entries

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)								
I18	BNEQ R1,R3,LOOP								
I19	L.D F2,0(R1)								

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)							
I19	L.D F2,0(R1)								

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	14	15	15	-	16		CDB Conflict
I19	L.D F2,0(R1)								

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict
I19	L.D F2,0(R1)								

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict
I19	L.D F2,0(R1)	15 (1)	16	17	17	18	19	22	Wait for ROB

Problem 3.15 – a. Conservative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	10	11	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	7	8	8	-	9	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	10	11	11	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	11	12	12	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	12	13	13	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict
I19	L.D F2,0(R1)	15 (1)	16	17	17	18	19	22	Wait for ROB

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8								
I4	S.D-A F2,-8(R2)								
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	3	4	4	-	5		CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (4)							
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (4)							
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (4)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)								
I6	BNEQ R1,R3,LOOP								
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)							
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)								
I8	ADDI R1,R1,#8								
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)							
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	5	6	6				FU conflict with I6
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	6	7	7	-	8		FU conflict, CDB conflict
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8								
I10	S.D-A F2,-8(R2)								
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	6	7	7	-	8		CDB conflict
I10	S.D-A F2,-8(R2)	5 (0)							
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)							
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)								
I12	BNEQ R1,R3,LOOP								
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)							
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1
I13	L.D F2,0(R1)								
I14	ADDI R1,R1,#8								

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1
I13	L.D F2,0(R1)	10 (1)	11	12	12				Wait for 2 ROB entries, FU conflict
I14	ADDI R1,R1,#8	10 (0)							

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1
I13	L.D F2,0(R1)	10 (1)	12	13	13	14			Wait for 2 ROB entries, FU conflict, Cache Conflict
I14	ADDI R1,R1,#8	10 (0)							

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache Conflict
I14	ADDI R1,R1,#8	10 (0)							

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict, CDB conflict
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	CDB conflict, FU conflict
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache Conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	

In Parenthesis: Remaining ROB entries

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)								
I18	BNEQ R1,R3,LOOP								
I19	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)							
I19	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	14	15	15	-	16		CDB Conflict
I19	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict
I19	L.D F2,0(R1)								

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict
I19	L.D F2,0(R1)	15 (1)	16	17	17	18	19	22	Wait for ROB

Problem 3.15 – b. Speculative Disambiguation

		Dispatch	Issue	Ex_Start	Ex_End	Cache	CDB	Retire	Comments
I1	L.D F2,0(R1)	1 (7)	2	3	3	4	5	6	
I2	ADDI R1,R1,#8	1 (6)	2	3	3	-	4	7	
I3	ADDI R2,R2,#8	2 (5)	4	5	5	-	6	8	CDB conflict with I1
I4	S.D-A F2,-8(R2)	2 (5)	7	8	8	-	-	-	Wait for R2
I5	S.D-D F2,-8(R2)	3 (4)	6	7	7	9	-	10	Wait for F2, Address and I3 retire (for cache)
I6	BNEQ R1,R3,LOOP	3 (3)	5	6	6	-	7	11	Wait for R1
I7	L.D F2,0(R1)	4 (2)	5	6	6	7	8	12	Wait for previous store address
I8	ADDI R1,R1,#8	4 (1)	7	8	8	-	9	13	FU conflict with I6
I9	ADDI R2,R2,#8	5 (0)	8	9	9	-	10	14	Wait for R2
I10	S.D-A F2,-8(R2)	5 (0)	11	12	12	-	-	-	Wait for R2
I11	S.D-D F2,-8(R2)	7 (1)	9	10	10	14	-	15	Wait for 2 ROB entries, F2, I9 retire
I12	BNEQ R1,R3,LOOP	7 (0)	10	11	11	-	12	16	Wait for R1, CDB conflict
I13	L.D F2,0(R1)	10 (1)	13	14	14	15	16	17	Wait for 2 ROB entries, FU conflict, Cache conflict
I14	ADDI R1,R1,#8	10 (0)	11	12	12	-	13	18	
I15	ADDI R2,R2,#8	11 (0)	12	13	13	-	14	19	No ROB required for I15
I16	S.D-A F2,-8(R2)	11 (0)	15	16	16	-	-	-	Wait for R2
I17	S.D-D F2,-8(R2)	13 (1)	17	18	18	19	-	20	Wait for ROB and F2
I18	BNEQ R1,R3,LOOP	13 (0)	15	16	16	-	17	21	CDB Conflict
I19	L.D F2,0(R1)	15 (1)	16	17	17	18	19	22	Wait for ROB

Agenda

- Problem 3.13
- Problem 3.15
- Problem 3.16

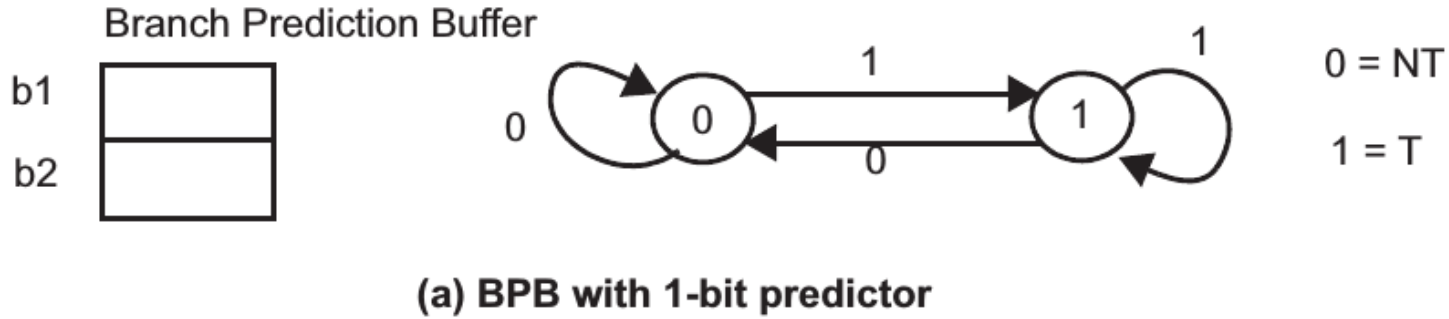
Problem 3.16

Consider the following code segment for a loop:

```
        if (x is odd) then          < −(branch b1)
          increment a               < −(b1 untaken)
  if (x is a multiple of 5) then    < −(branch b2)
          increment b               < −(b2 untaken)
```

Assume that the following list of 9 values of x is processed by 9 iterations of this loop: 8
9
10
11
7
20
29
30
31

3.16(a) (one-bit state machine)



(a) BPB with 1-bit predictor

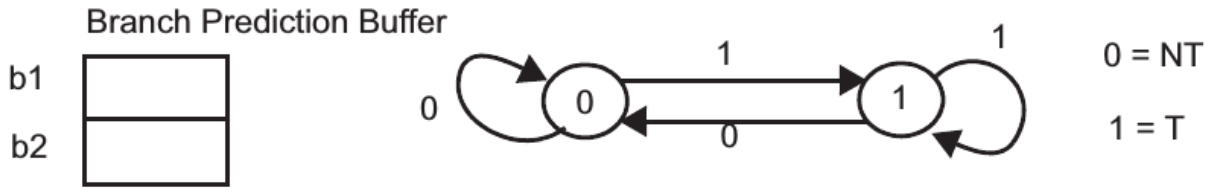
Assume that a one-bit state machine (see Figure 3.46(a)) is used as the prediction algorithm for predicting the execution of the two branches in this loop.

Show the predicted and actual branch directions of both b1 and b2 branch instructions for each iteration of this loop. Assume the initial state is 0, i.e. NT (not taken), for the predictor.

What are the prediction accuracies for b1 and for b2 ?

What is the overall prediction accuracy for both branches ?

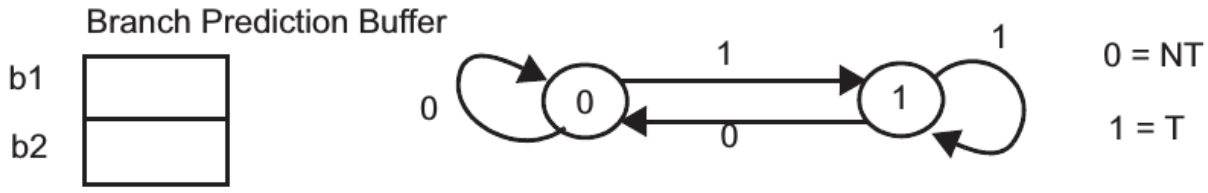
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1		

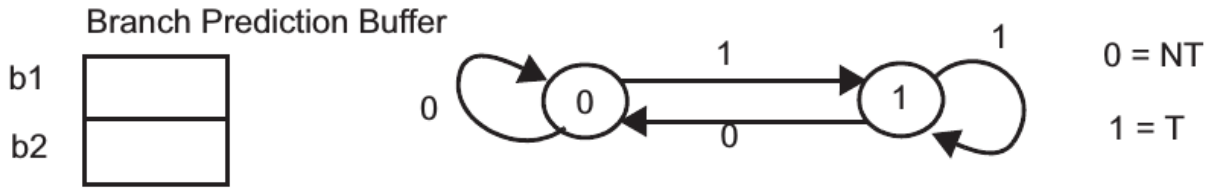
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1

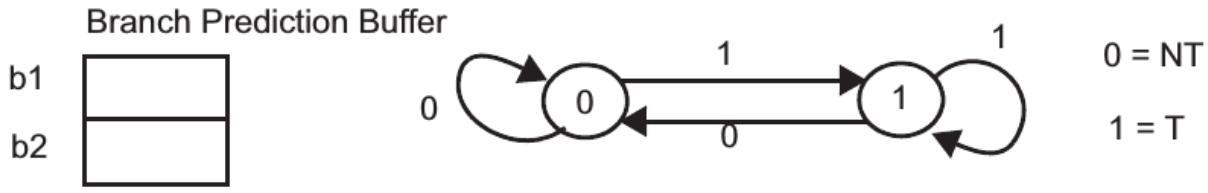
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0		

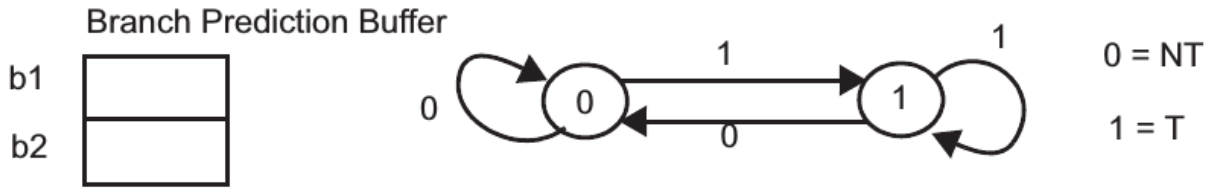
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1

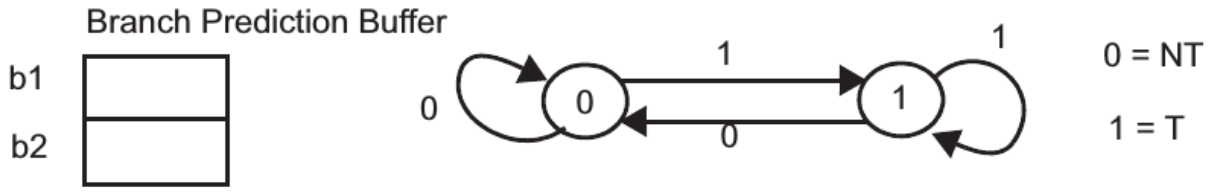
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1		

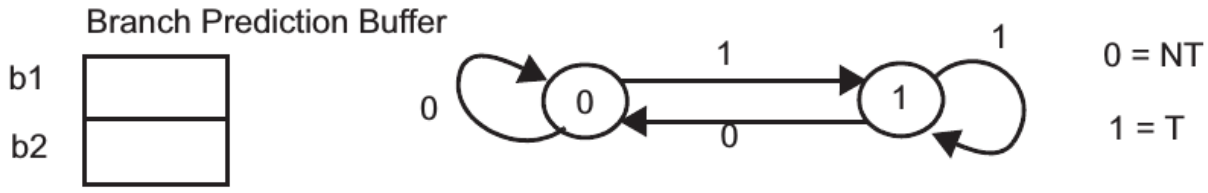
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0

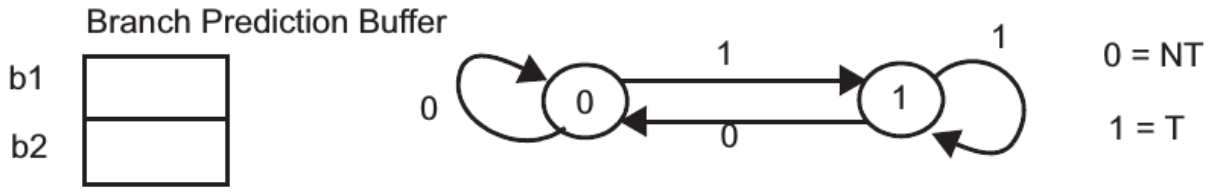
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0		

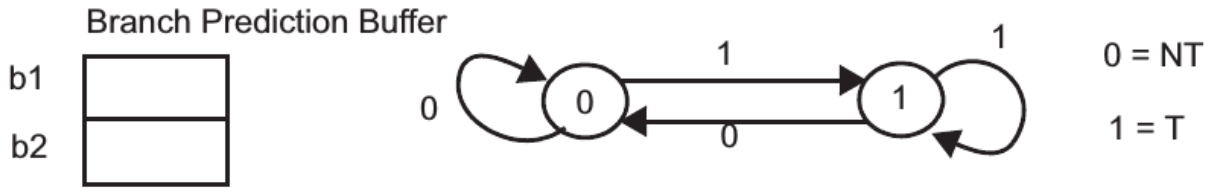
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1

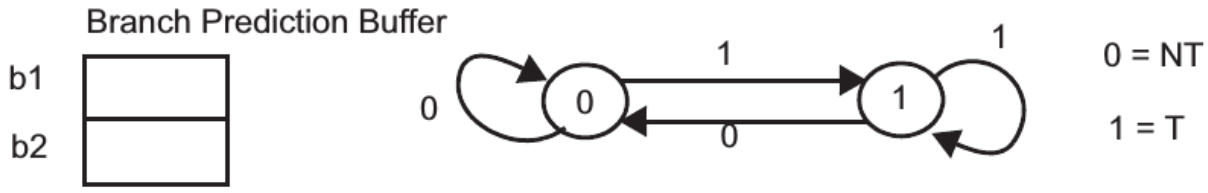
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0		

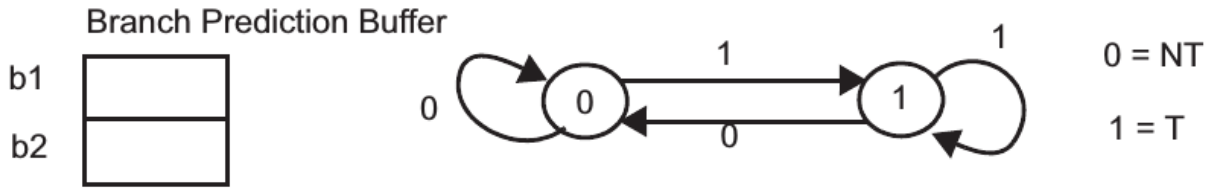
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1

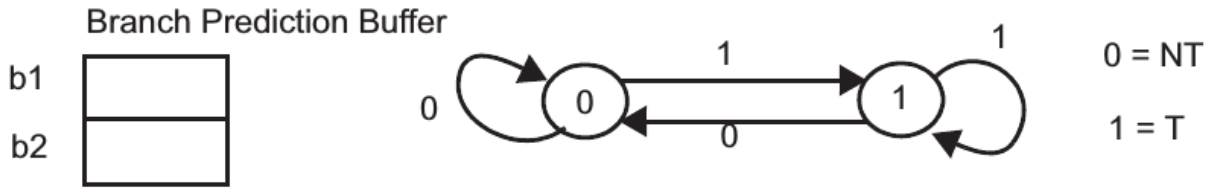
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1		

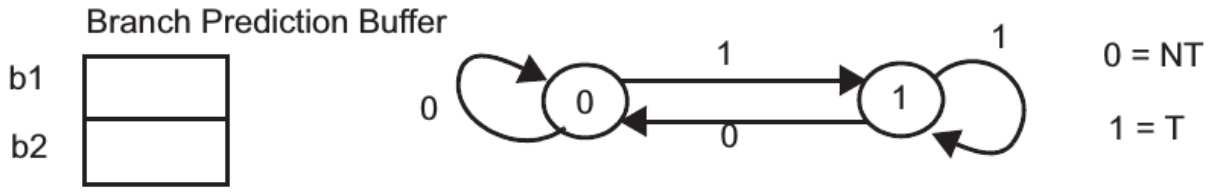
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0

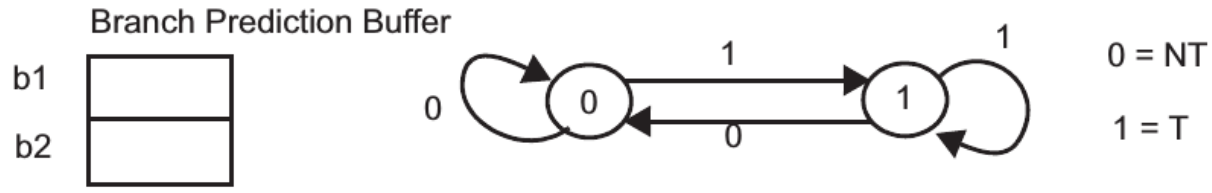
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0		

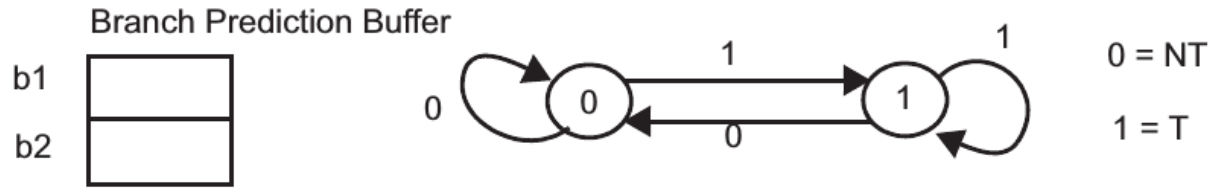
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1

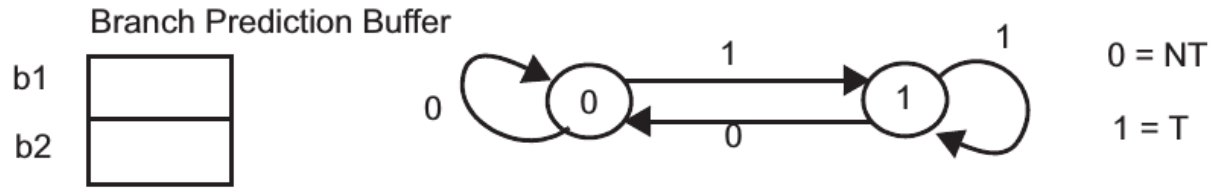
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1		

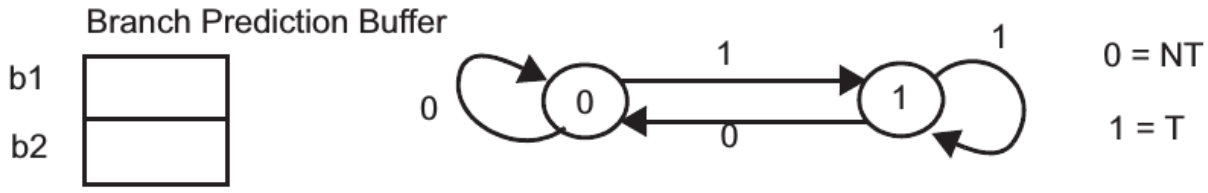
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1	1	0

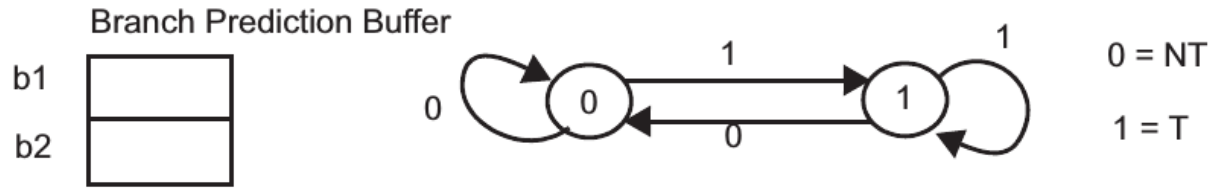
3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1	1	0
31	1	0		

3.16(a) (Predicted and Actual branch directions)



(a) BPB with 1-bit predictor

Value of x	Branch b1		Branch b2	
	Predicticed	Actual	Predicticed	Actual
8	0	1	0	1
9	1	0	1	1
10	0	1	1	0
11	1	0	0	1
7	0	0	1	1
20	0	1	1	0
29	1	0	0	1
30	0	1	1	0
31	1	0	0	1

3.16(a) (Prediction accuracy)

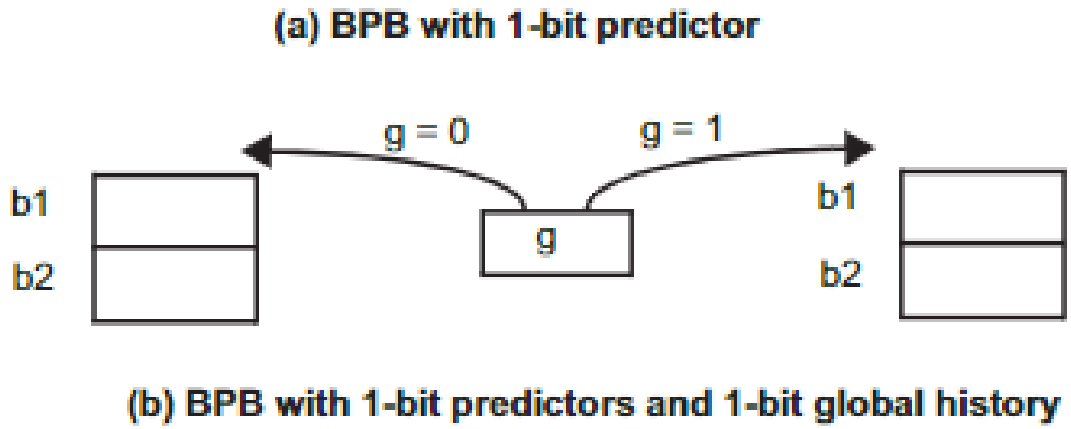
Value of x	Branch b1			Branch b2		
	Predicticed	Actual	Success	Predicticed	Actual	Success
8	0	1	0	0	1	0
9	1	0	0	1	1	1
10	0	1	0	1	0	0
11	1	0	0	0	1	0
7	0	0	1	1	1	1
20	0	1	0	1	0	0
29	1	0	0	0	1	0
30	0	1	0	1	0	0
31	1	0	0	0	1	0

Prediction Accuracy b1 $= 1/9 = 11\%$

Prediction Accuracy b2 $= 2/9 = 22\%$

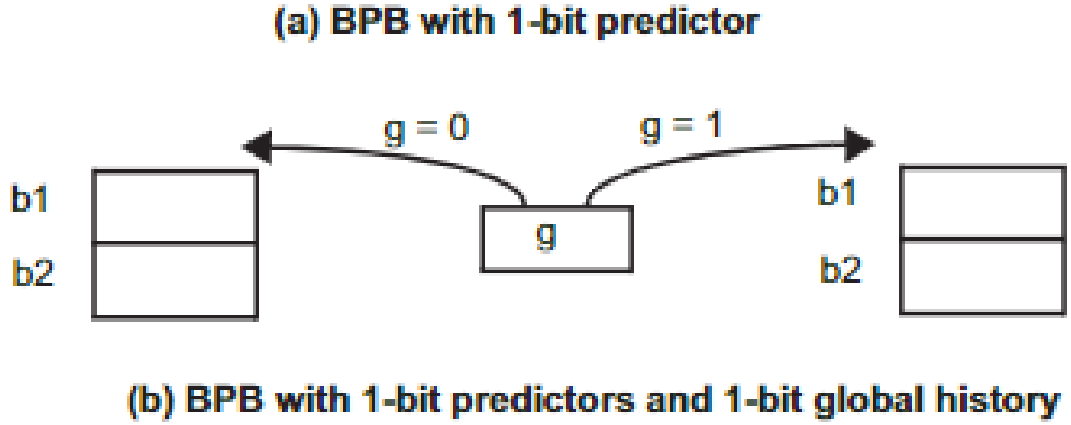
Overall Prediction Accuracy $= 3/18 = 16.6\%$

3.16(b) (Two Level Predictor)



In addition to the one-bit predictor, a one-bit global history register (g) is used. g stores the direction of the last executed branch (which may or may not be the same branch as the branch currently being predicted) and is used to indexinto two separate one-bit predictor tables as shown Figure 3.46(b).

3.16(b) (Two Level Predictor)



Depending on the value of g, one of the two predictor table is selected and used for the normal one-bit prediction. Again, fill in the predicted and actual branch directions of b1 and b2 for nine itera-tions of the loop. The initial state of the predictor tables is all 0's.What are the prediction accuracies for b1 and b2?What is the overall prediction accuracy?

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
30	b1	1	0	1	1	-	1	1	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
30	b1	1	0	1	1	-	1	1	0	-
	b2	1	0	-	1	0		-	0	0

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
30	b1	1	0	1	1	-	1	1	0	-
	b2	1	0	-	1	0		-	0	0
31	b1	0	0	0	1	-		0	0	-

3.16(b) (Two Level Predictor)

			$g = 0$				$g = 1$			
Value of x	Branch	g	b1		b2		b1		b2	
			Pred	Actual	Pred	Actual	Pred	Actual	Pred	Actual
Initial State		0	0	-	0	-	0	-	0	-
8	b1	0	0	1	0	-	0	1	0	-
	b2	1	1	-	0	1	0	-	0	1
9	b1	1	1	0	0	-	0	0	1	-
	b2	0	1	-	0	1	0	-	1	1
10	b1	1	1	1	1	-	0	1	1	-
	b2	1	1	-	1	0	1	-	1	0
11	b1	0	1	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
7	b1	1	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	0	-	0	1
20	b1	1	0	1	1	-	0	1	0	-
	b2	1	0	-	1	0	1	-	0	0
29	b1	0	0	0	1	-	1	0	0	-
	b2	0	0	-	1	1	1	-	0	1
30	b1	1	0	1	1	-	1	1	0	-
	b2	1	0	-	1	0		-	0	0
31	b1	0	0	0	1	-		0	0	-
	b2	0	0	-	1	1		-	0	1

3.16(b) (Two Level Predictor)

Prediction Accuracy b1 $= 4/9 = 44.4\%$

Prediction Accuracy b2 $= 6/9 = 66.7\%$

Overall Prediction Accuracy $= 10/18 = 55.5\%$

3.16(c) (Two Level Predictor)

What is the prediction success rate for branch b2 when g=0? Explain why this is.
Prediction Accuracy b2 = 4/5 = 80%

Among the numbers 8,9,10,11,7,20,29,30,31 There is no odd number which is also a multiple of 5.

Once predictor is warmed-up, b2 branch with g=0 is highly predictable. g=0 means the previous branch was not taken (odd) then since there are no odd numbers which is a multiple of 5 in the list, second branch will always be taken