

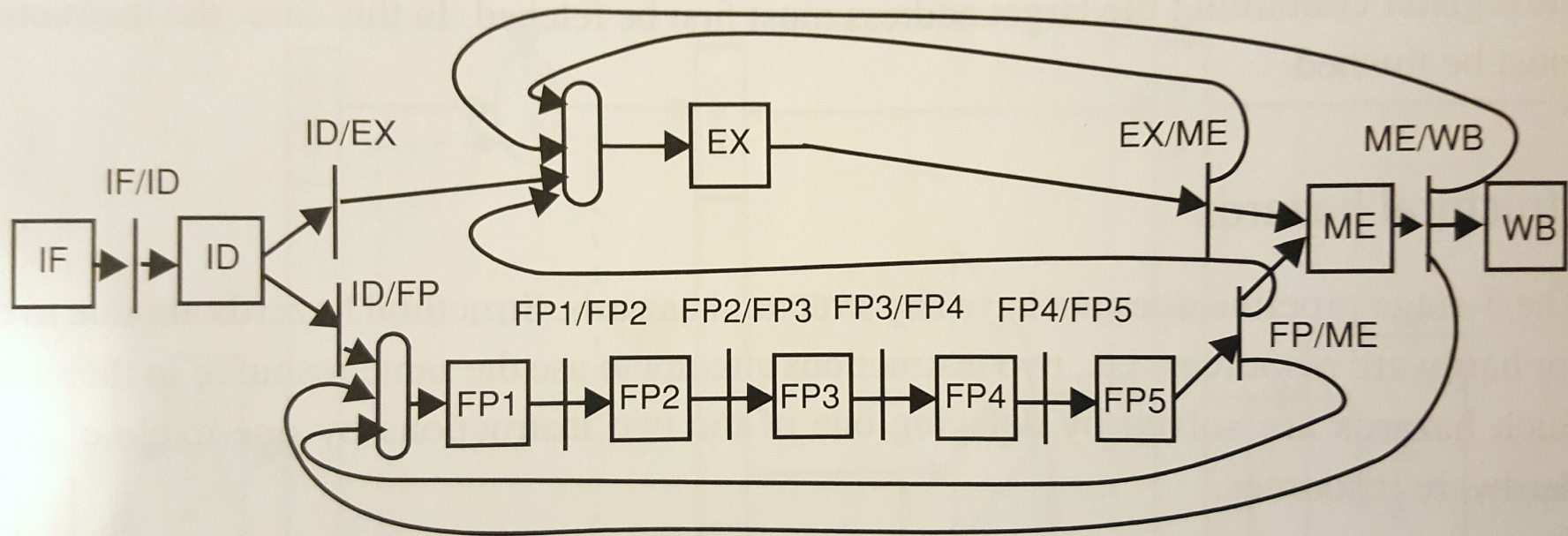
**Processor architecture**

Figure 3.8. Pipeline with out-of-order execution completion.