Design Report Form

<table>
<tr><td colspan="4">Group number:8</td></tr>
<tr><td colspan="4">RTL category</td></tr>
<tr><td>Design Stage</td><td colspan="2">Description</td><td>File Name</td></tr>
<tr><td>RTL Simulation</td><td colspan="2">RTL Netlist file name</td><td>triangle.v</td></tr>
<tr><td colspan="4">Gate-Level category</td></tr>
<tr><td>Design Stage</td><td colspan="2">Description</td><td>File Name</td></tr>
<tr><td rowspan="3">Pre-layout Gate-level Simulation</td><td colspan="2">Gate-Level Netlist file name</td><td>triangle_syn.v</td></tr>
<tr><td colspan="2">Pre-layout sdf file name</td><td>triangle_syn.sdf</td></tr>
<tr><td colspan="2">The clock period of Gate-Level simulation</td><td>(4) ns</td></tr>
<tr><td colspan="4">Physical category</td></tr>
<tr><td>Design Stage</td><td colspan="2">Description</td><td>File Name or Value</td></tr>
<tr><td rowspan="2">P&R</td><td colspan="2">GDSII file name</td><td>triangle.gds</td></tr>
<tr><td>Layout area</td><td colspan="2">(198.390) um X (184.560) um</td></tr>
<tr><td rowspan="4">Post-layout Gate-level Simulation</td><td colspan="2">Post-layout Gate-Level file name</td><td>triangle_pr.v</td></tr>
<tr><td colspan="2">Post-layout sdf file name</td><td>triangle_pr</td></tr>
<tr><td colspan="2">The clock period of Gate Level simulation</td><td>(1) ns</td></tr>
<tr><td colspan="2">Finishing time of Gate Level simulation</td><td>(780) ns</td></tr>
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