SYMPL

IEEE754-2008-Compliant RISC CPU with Quad-Shader GP-GPU-Compute Engine

Featuring: FloPoCo -Generated Floating-Point Operators

- **Performance:**
  5 FLOPS per clock or 600 FLOPS in Kintex* 7 @ 125MHz
- For Xilinx Kintex 7, Kintex UltraScale, Kintex UltraScale+, Altera Stratix V and Arria 10 -sized FPGAs.
- **Processors:**
  (1) 32-bit RISC CPU, (1) 32-bit Coarse-Grainded Schedulers, (4) interleaving, multi-threading, GP-GPU shaders (4 threads each), for a total of 16 interleaving threads.
- **Dual-Operand, Pure "Mover" Architecture**
  Not based on antiquated "load-store". Gets 4 times more work done than "load-store" operating at the same clock frequency.
- **CPU, CGS and GP-GPUs execute the same SYMPL ISA instruction set.**
- CPU and GP-GPUs have identical IEEE754-2008-compliant, memory-mapped, single-precision floating-point operators, including: FADD, FSUB, FMUL, FDIV, FMA, DOT, SQRT, LOG, EXP, FTOI, ITOF.

For more information, contact:
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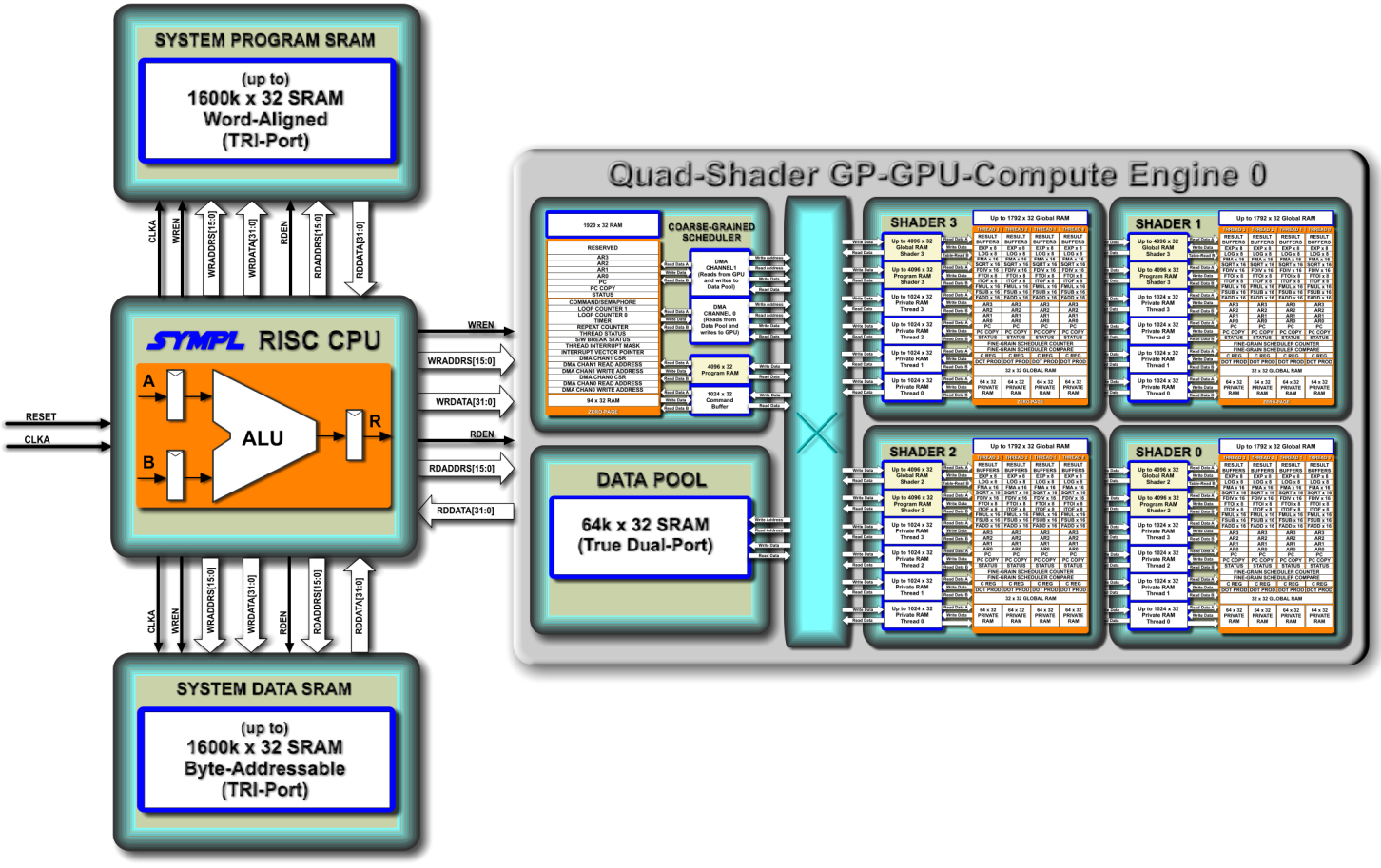
- Multi-threaded
- Multi-processor
- Dual quad-shader
- Four threads per shader
- Threads interleaved
- SYMPL Intermediate Level Language now included in the download package at GitHub
- Fully programmable CPU, GP-GPU and Coarse-Grained Scheduler execute the same instruction set
- Dual DMA channels for simultaneous R/W transfers
- 1k-word granularity for data-pool permits simultaneous accesses by CPU, CGS, and DMA controllers
- Easy to learn instruction set
- Programmer's Reference available on request

- **Operators:**
  FADD
  FSUB
  FMUL
  FMA
  DOT
  FDIV
  SQRT
  LOG
  EXP
  ITOF
  FTOI
  SIN
  COS
  TAN
  COT
  RCP

Download open-source synthesizable RTL now at:
https://www.github.com/jerry-D/SYMPL-GP-GPU-Compute-Engines



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Preliminary Information