SYMPL

IEEE754-2008-Compliant RISC CPU with Sixteen-Shader GP-GPU-Compute Engine

Featuring: FloPoCo -Generated Floating-Point Operators

- **Performance:**
  17 FLOPS per clock or 2.1 Billion FLOPS in Kintex* 7 @ 125MHz
- For Xilinx Kintex 7, Kintex UltraScale, Kintex UltraScale+, Altera Stratix V and Arria 10 -sized FPGAs.
- **Processors:**
  (1) 32-bit RISC CPU, (4) 32-bit Coarse-Grained Schedulers, (16) interleaving, multi-threading, GP-GPU shaders (4 threads each), for a total of 64 interleaving threads.
- **Dual-Operand, Pure "Mover" Architecture**
  Not based on antiquated "load-store". Gets 4 times more work done than "load-store" operating at the same clock frequency.
- **CPU, CGS and GP-GPUs execute the same SYMPL ISA instruction set.**
- CPU and GP-GPUs have identical IEEE754-2008-compliant, memory-mapped, single-precision floating-point operators, including: FADD, FSUB, FMUL, FDIV, FMA, DOT, SQRT, LOG, EXP, FTOI, ITOF.

For more information, contact:
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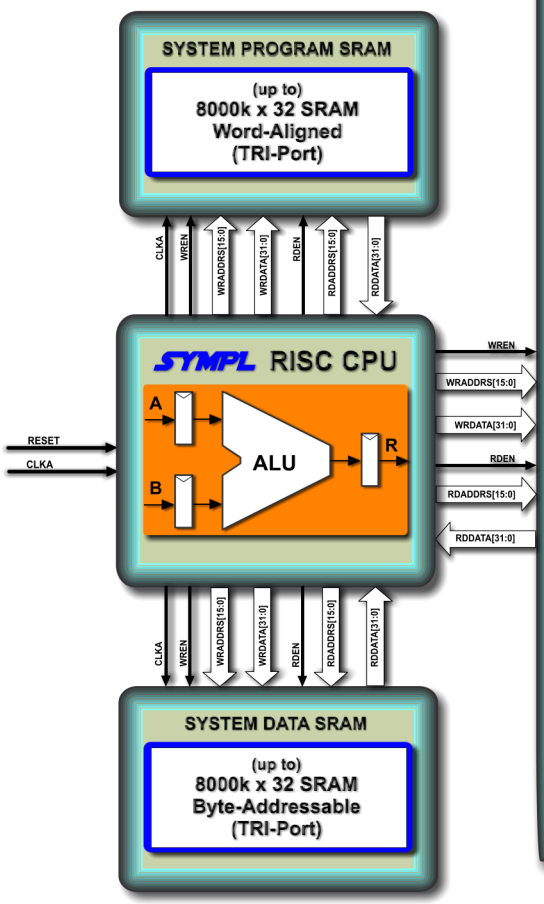

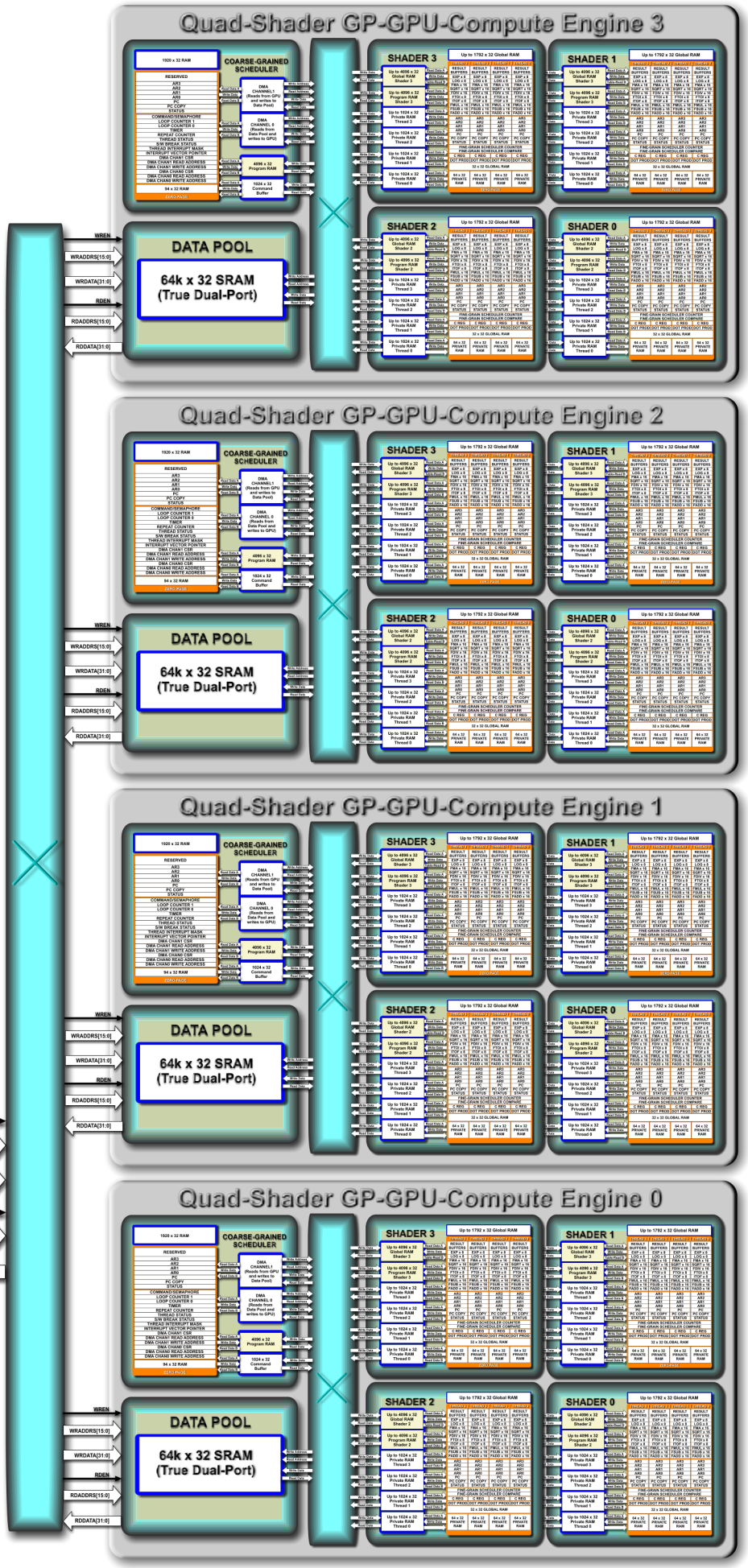

Preliminary Information

*Xilinx, Kintex 7, UltraScale, Kintex UltraScale+ are trademarks of Xilinx. Altera, Stratix V and Arria 10 are trademarks of Altera.