

1. Description

1.1. Project

Project Name	Reveil_STM32-Matrice
Board Name	custom
Generated with:	STM32CubeMX 6.8.1
Date	11/16/2023

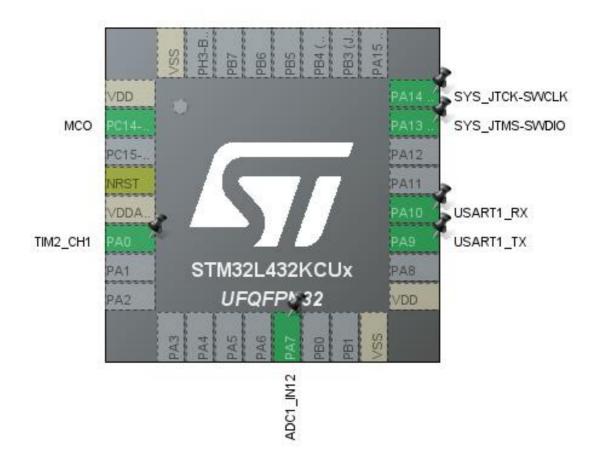
1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x2
MCU name	STM32L432KCUx
MCU Package	UFQFPN32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M4

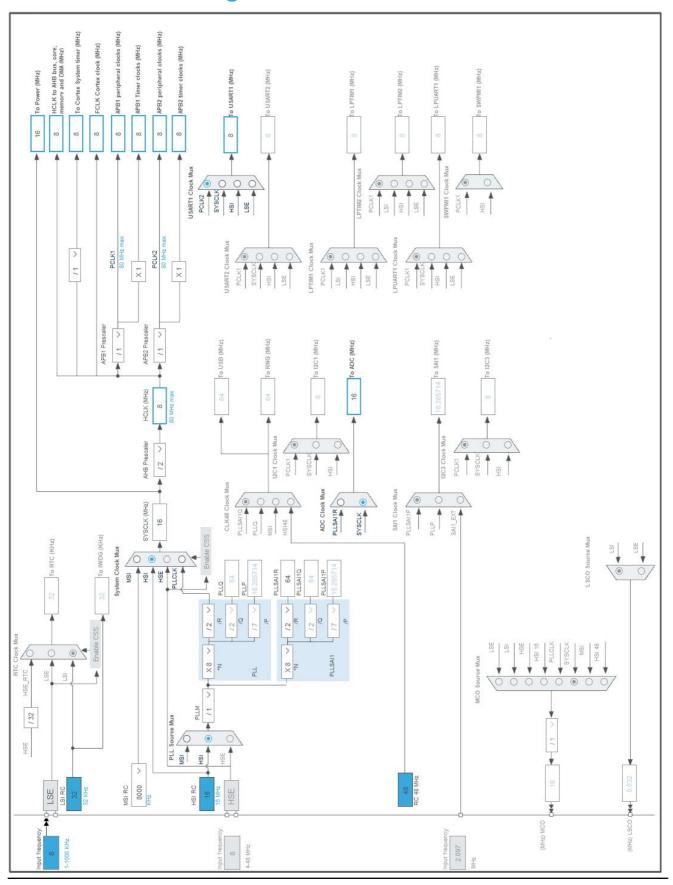
2. Pinout Configuration



3. Pins Configuration

Pin Number UFQFPN32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	MCO
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	TIM2_CH1	
13	PA7	I/O	ADC1_IN12	
16	VSS	Power		
17	VDD	Power		
19	PA9	I/O	USART1_TX	
20	PA10	I/O	USART1_RX	
23	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	
24	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	
32	VSS	Power		

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	Reveil_STM32-Matrice
Project Folder	C:\ST\Reveil_STM32-Matrice
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_TIM2_Init	TIM2
6	MX_USART1_UART_Init	USART1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x2
мси	STM32L432KCUx
Datasheet	DS11451_Rev2

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

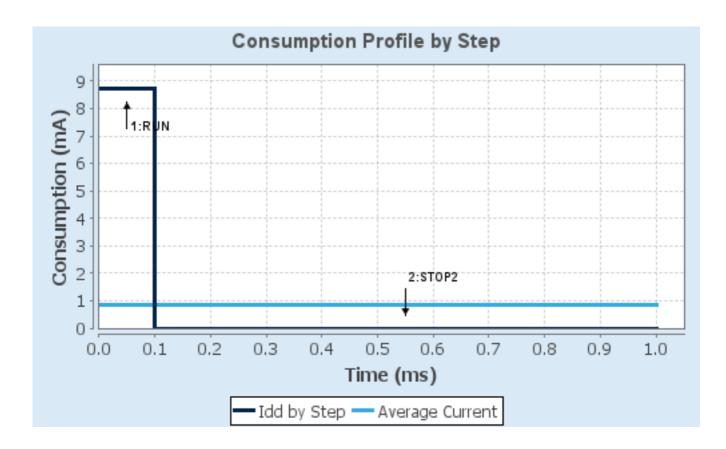
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	8.71 mA	1.06 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.98	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	871.95 μA
Battery Life	5 months, 9 days,	Average DMIPS	100.0 DMIPS
	16 hours		

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN12

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler Asynchronous clock mode divided by 1

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled
DMA Continuous Requests Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None
Rank 1

Channel Channel 12
Sampling Time 2.5 Cycles
Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

7.2. RCC

Low Speed Clock (LSE): BYPASS Clock Source

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3 Instruction Cache Enabled Prefetch Buffer Disabled Data Cache Enabled

0 WS (1 CPU cycle) Flash Latency(WS)

RCC Parameters:

HSI Calibration Value 16 MSI Calibration Value MSI Auto Calibration Disabled 100 HSE Startup Timout Value (ms) 5000 LSE Startup Timout Value (ms)

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.3. SYS

Debug: Serial Wire

7.4. TIM2

Clock Source: Internal Clock **Channel1: PWM Generation CH1**

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) Counter Mode Up Counter Period (AutoReload Register - 32 bits value) 10-1 * No Division Internal Clock Division (CKD) Disable auto-reload preload

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

0

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source Disable

PWM Generation Channel 1:

Mode PWM mode 1 Pulse (32 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate 250000 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable Disable TX Pin Active Level Inversion RX Pin Active Level Inversion Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun DMA on RX Error Enable MSB First Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA7	ADC1_IN12	Analog mode for ADC conversion	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	MCO
SYS	PA13 (JTMS- SWDIO)	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14 (JTCK- SWCLK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM2_CH1	DMA1_Channel5	Memory To Peripheral	High *
ADC1	DMA1_Channel1	Peripheral To Memory	High *
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low
USART1_RX	DMA2_Channel7	Peripheral To Memory	Medium *

TIM2_CH1: DMA1_Channel5 DMA request Settings:

Mode: Circular *
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Word
Memory Data Width: Byte *

ADC1: DMA1_Channel1 DMA request Settings:

Mode: Circular *
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte
Memory Data Width: Byte

USART1_RX: DMA2_Channel7 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Byte

Memory Data Width:	Byte

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
DMA1 channel1 global interrupt	true	0	0	
DMA1 channel4 global interrupt	true	0	0	
DMA1 channel5 global interrupt	true	0	0	
USART1 global interrupt	true	0	0	
DMA2 channel7 global interrupt	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1 global interrupt	unused			
TIM2 global interrupt	unused			
FPU global interrupt	unused			

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 channel1 global interrupt	false	true	true
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
USART1 global interrupt	false	true	true
DMA2 channel7 global interrupt	false	true	true

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32l4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32l4_ibis.zip

System View https://www.st.com/resource/en/svd/stm32l4_svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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