Texas A&M University

Sequential Logic

*Author:*

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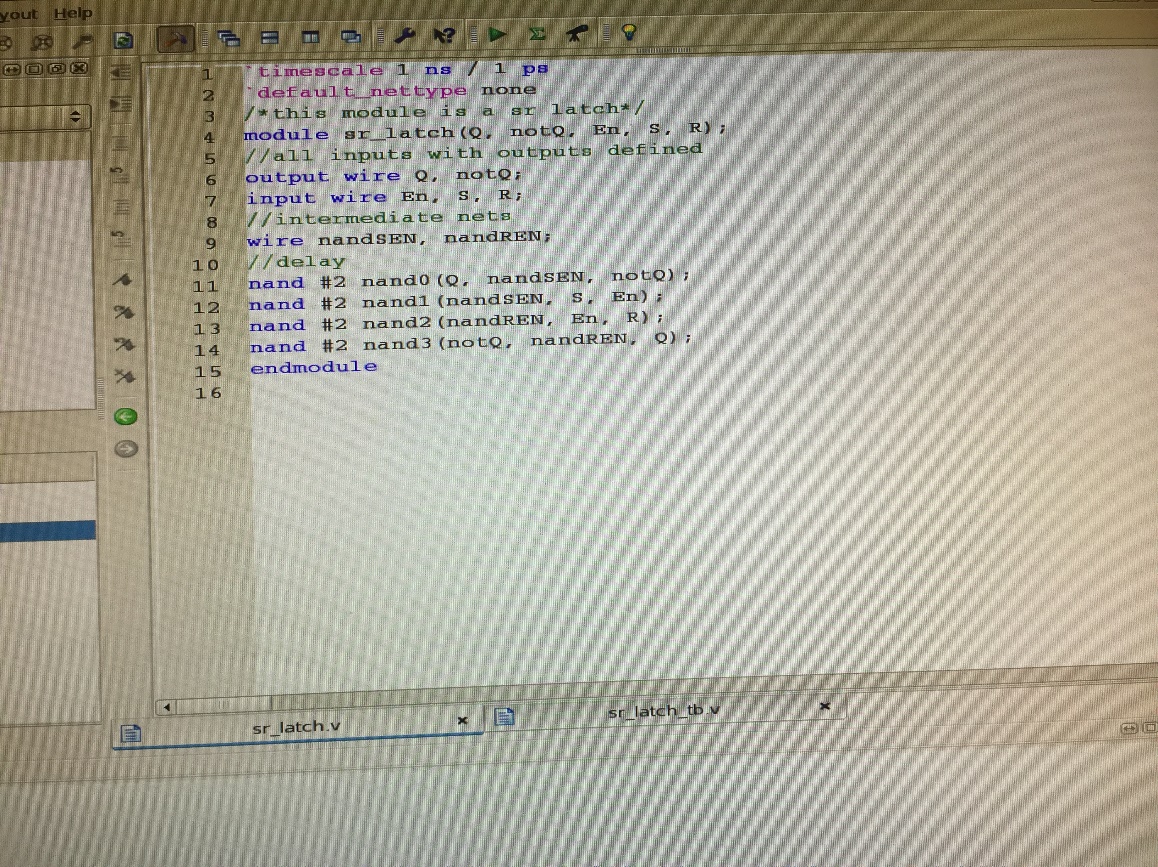
**Objective**

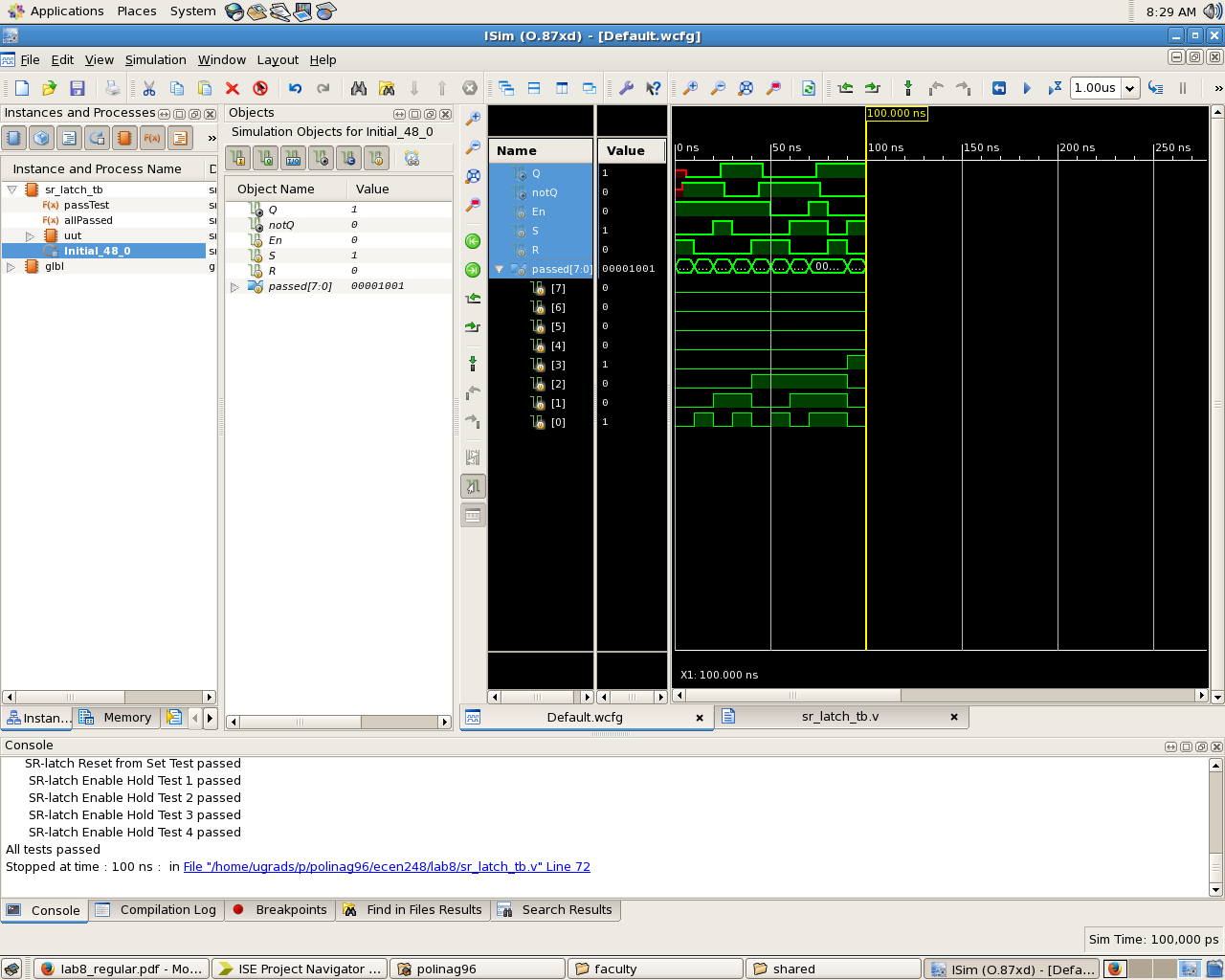
This introduces the concept of sequential logic circuits. We were able to see how elements such as a latches and flip-flops come into play. We combined flip-flops with combinational logic as discussed in previous labs to simulate the operation of synchronous logic. Furthermore we observed what timing difference delays make when they are added to combinational logic.

**Design**

In this lab we incorporated the design for a D-Latch, SR Latch, D Flip-Flop, D-Latch Behavioral, D Flip-Flop and a 2-bit Adder. We implemented these circuits into Verilog.

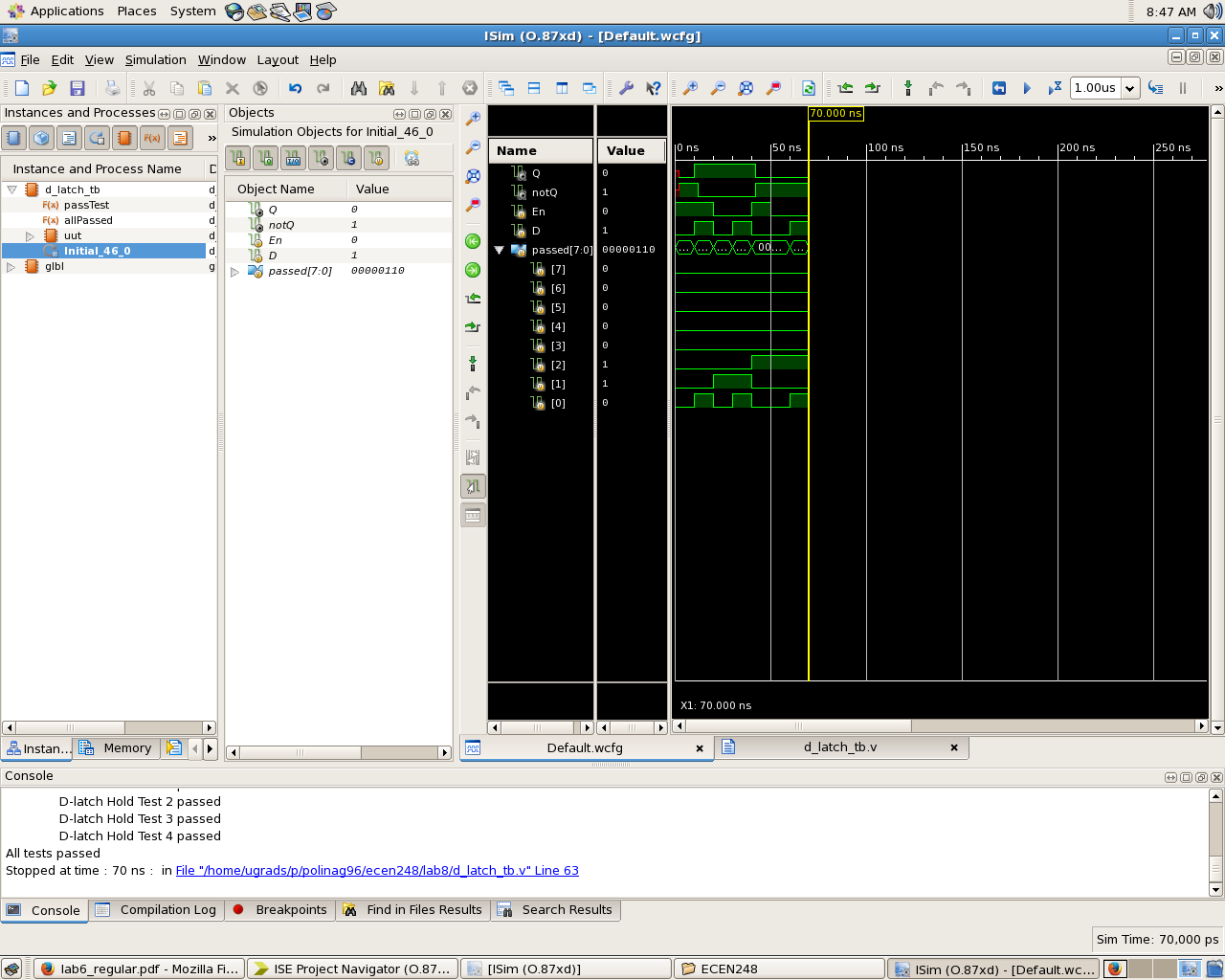
**Experiment 1**

*SR-Latch*

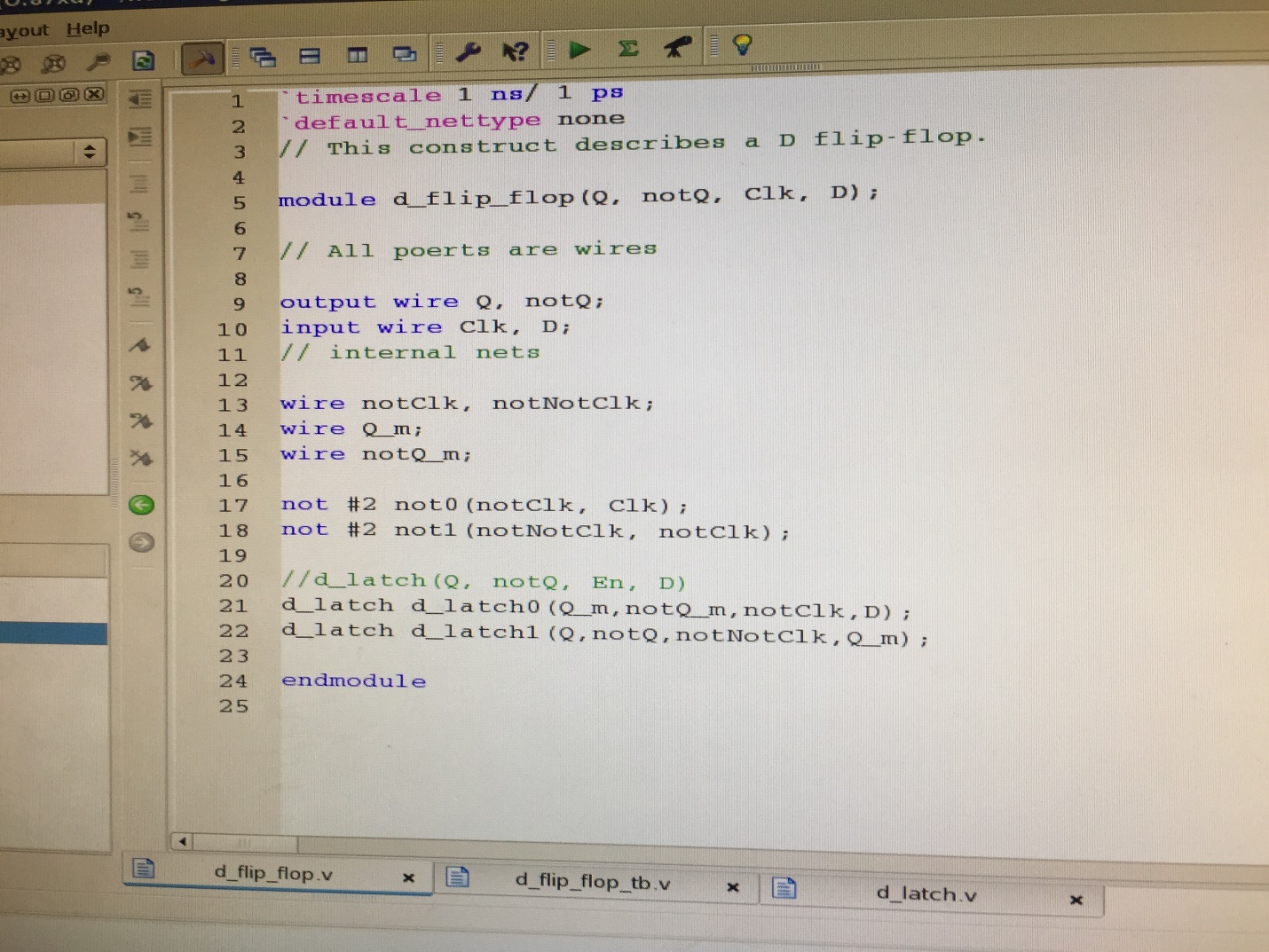


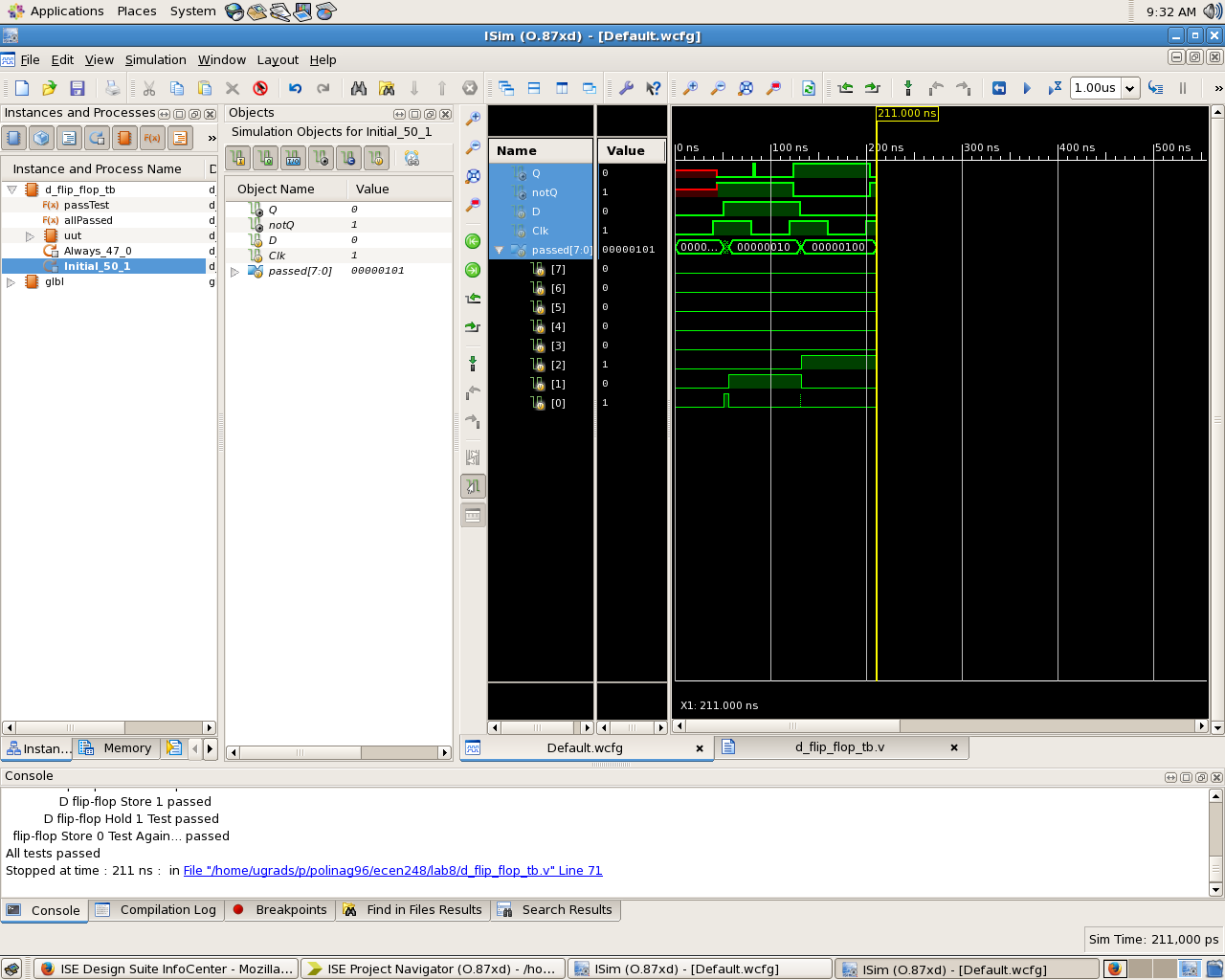
*D-Latch*

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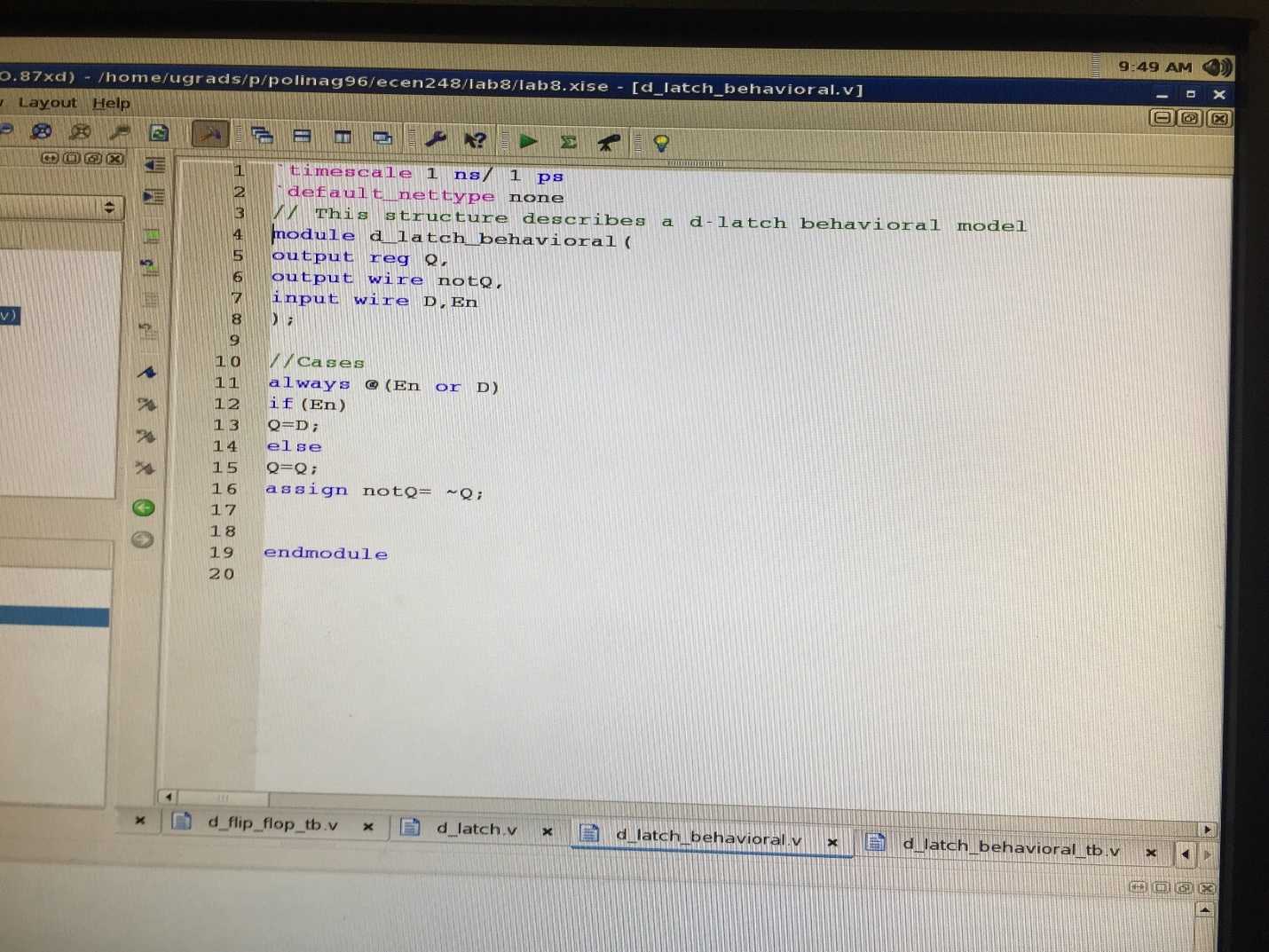
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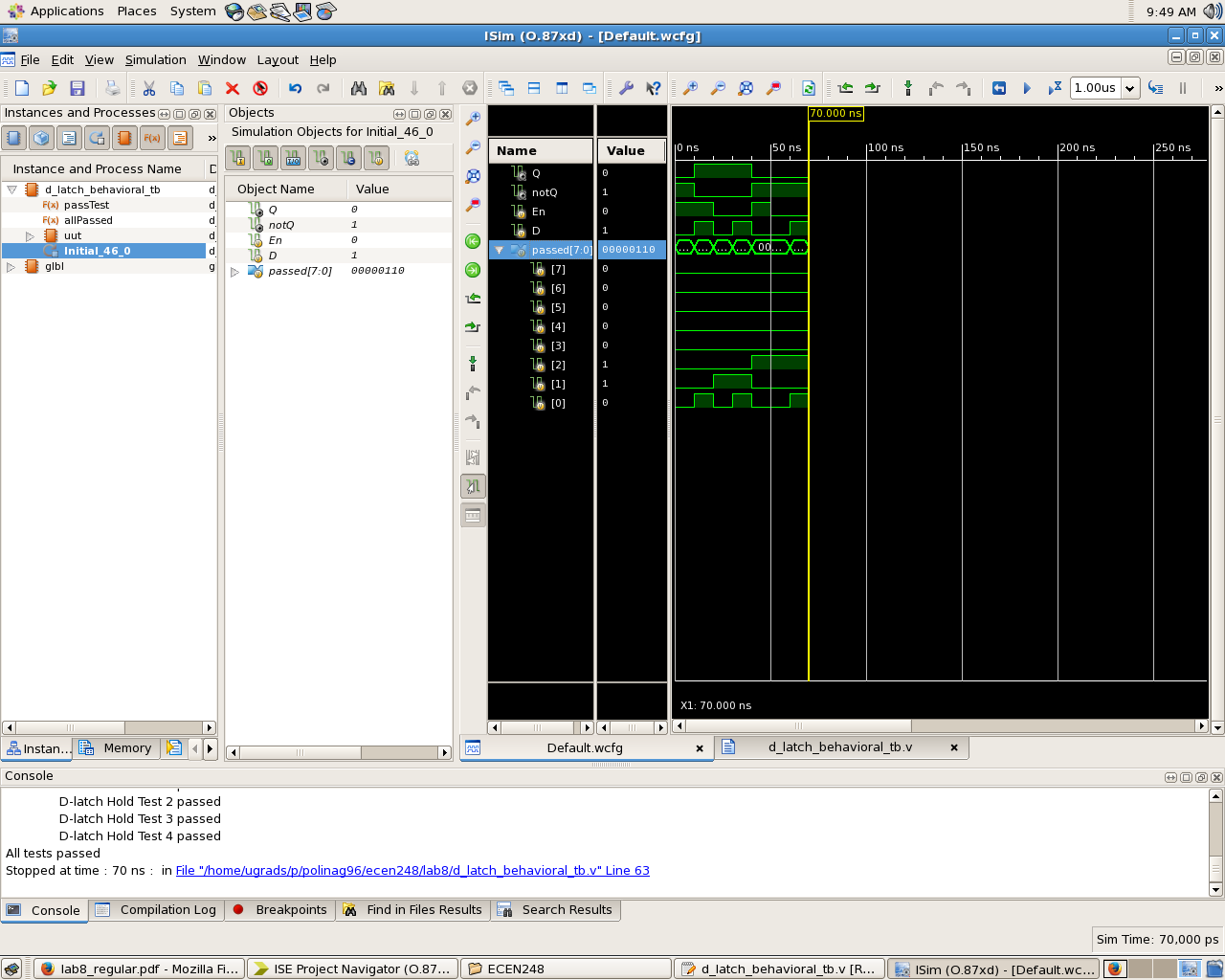
*D Flip-Flop*

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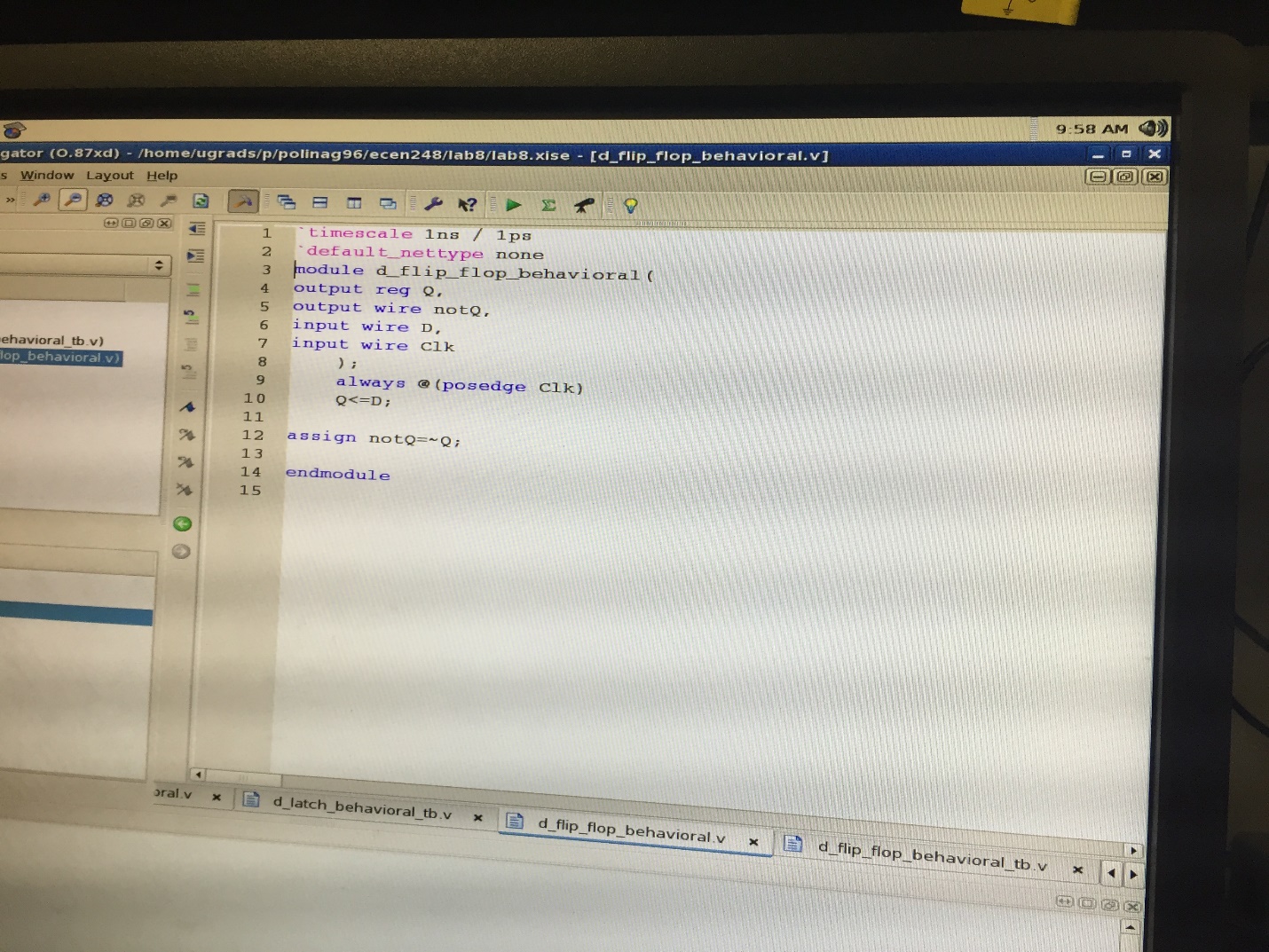
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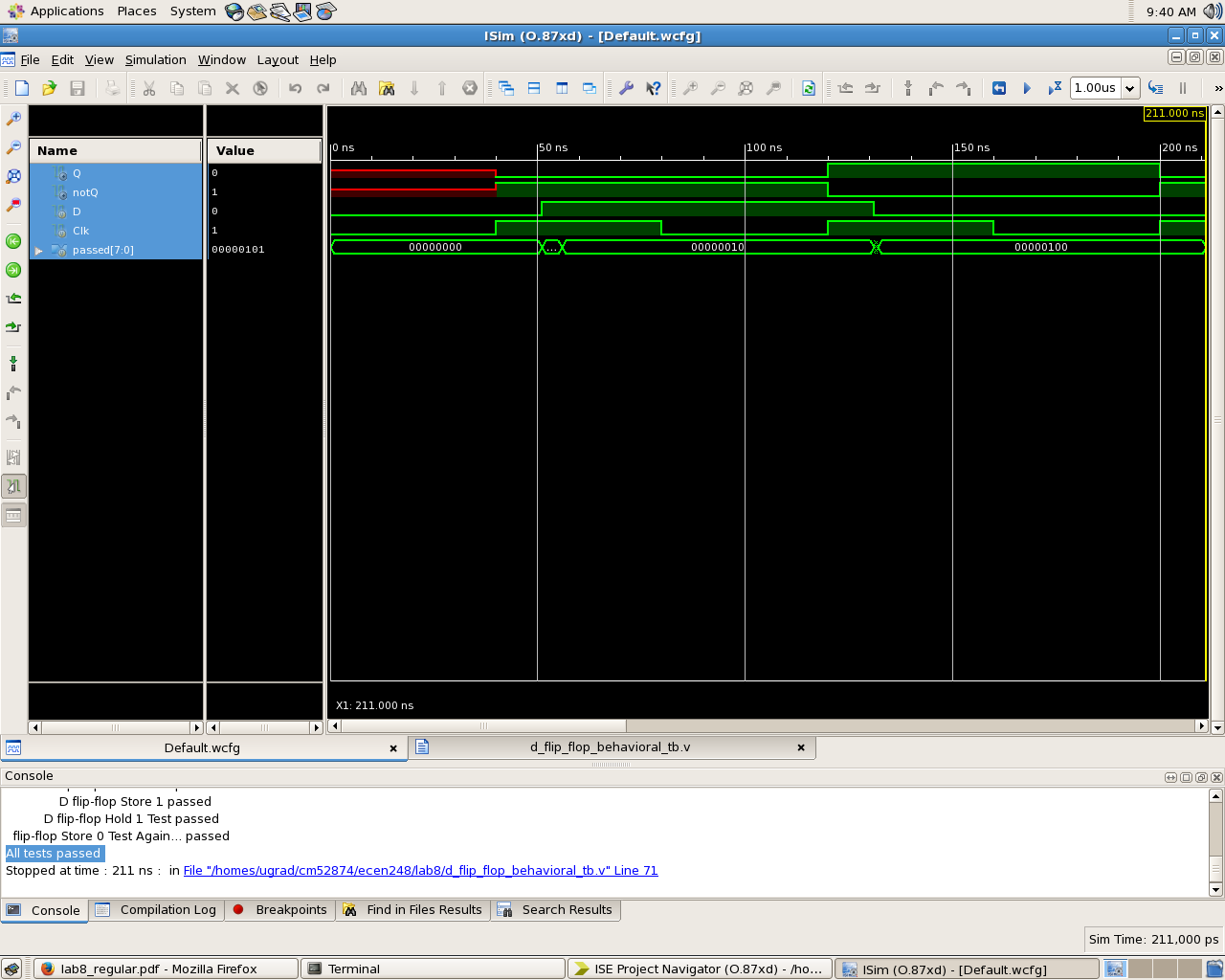
*D-Latch Behavioral*

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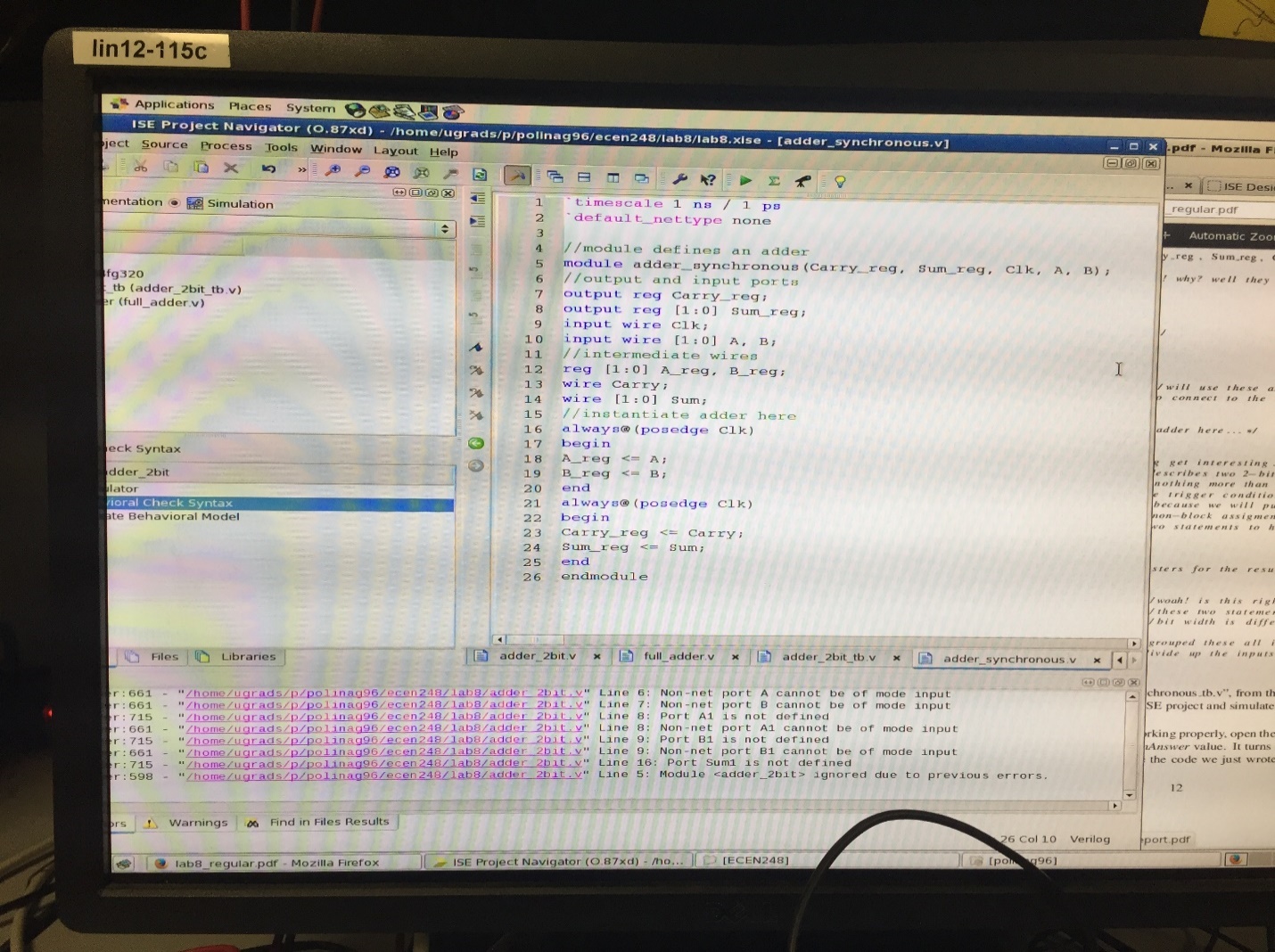
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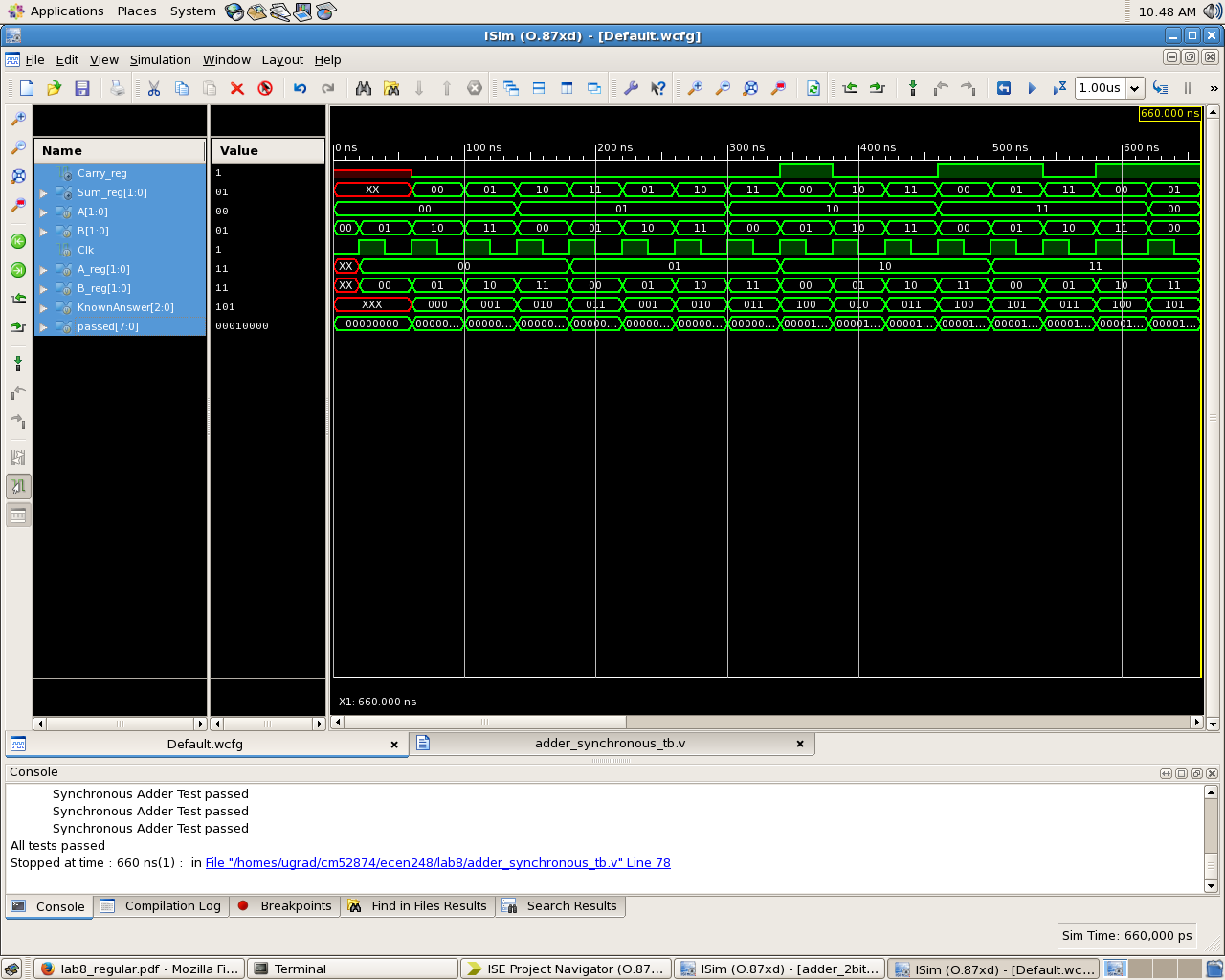
*D Flip-Flop Behavioral*

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*Adder- synchronous*

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