《硬件内存模型和 C/C++内存模型》课程参考资料

前言：为避免引起版权问题，本文只给出资料名称及其链接，请会员们自行下载/阅读。

资料 1：A Tutorial Introduction to the ARM and POWER Relaxed Memory Models
原始链接：https://www.cl.cam.ac.uk/~pes20/ppc-supplemental/test7.pdf

资料 2：An Operational Semantics for C/C++11 Concurrency:
原始链接：https://www.cl.cam.ac.uk/~pes20/cerberus/c11op.pdf

资料 3：A Tutorial Introduction to the ARM and POWER Relaxed Memory Models
原始链接：https://www.cl.cam.ac.uk/~pes20/ppc-supplemental/test7.pdf

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资料 4：Simplifying ARM Concurrency: Multicopy-Atomic Axiomatic and Operational Models for ARMv8
原始链接：https://dl.acm.org/doi/pdf/10.1145/3158107

资料 5：Common Compiler Optimisations are Invalid in the C11 Memory Model and what we can do about it
原始链接：https://plv.mpi-sws.org/c11comp/popl15.pdf

资料 6：x86-TSO: A Rigorous and Usable Programmer’s Model for x86 Multiprocessors
原始链接：https://www.cl.cam.ac.uk/~pes20/weakmemory/cacm.pdf

资料 7：Foundations of the C++ Concurrency Memory Model
原始链接：https://rsim.cs.illinois.edu/Pubs/08PLDI.pdf

资料 8：Hardware Memory Models
原始链接：https://research.swtch.com/hwmm.pdf

资料 9：How to Make a Multiprocessor Computer That Correctly Executes Multiprocess Programs
原始链接：
https://www.microsoft.com/en-us/research/uploads/prod/2016/12/How-to-Make-a-Multiprocessor-Computer-That-Correctly-Executes-Multiprocess-Programs.pdf

资料 10：Intel® 64 Architecture Memory Ordering White Paper
原始链接：https://www.cs.cmu.edu/~410-f10/doc/Intel_Reordering_318147.pdf

资料 11：Memory Barriers a Hardware View for Software Hackers
原始链接：
http://www.rdrop.com/users/paulmck/scalability/paper/whymb.2010.06.07c.pdf

资料 12：Outlawing Ghosts-Avoiding Out-of-Thin-Air Results
原始链接：http://plrg.eecs.uci.edu/publications/mspc14.pdf

资料 13：P2055R0- A Relaxed Guide to memory_order_relaxed
原始链接：
https://www.open-std.org/jtc1/sc22/wg21/docs/papers/2020/p2055r0.pdf

资料 14：Partial and Total Orders - Eli Bendersky's website
原始链接：https://eli.thegreenplace.net/2018/partial-and-total-orders/

资料 15：The Semantics of x86-CC Multiprocessor Machine Code
原始链接：https://www.cl.cam.ac.uk/~pes20/weakmemory/popl09.pdf

资料 16：Common Compiler Optimisations are Invalid in the C11 Memory Model and what we can do about it
原始链接：https://plv.mpi-sws.org/c11comp/popl15.pdf

资料 17：Programming Language Memory Models
原始链接：https://research.swtch.com/plmm

资料 18：Relaxed Separation Logic：A Program Logic for C11 Concurrency
原始链接：https://people.mpi-sws.org/~viktor/papers/oopsla2013-rsl.pdf

资料 19：On the Definition of Sequential Consistency
原始链接：https://users.cs.utah.edu/~ganesh/unpublished/sc_definition.pdf

资料 20：SNOOPING PROTOCOLS
原始链接：
https://users.cs.utah.edu/~bojnordi/classes/7810/s20/slides/07-snooping.pdf

资料 21：The C11 and C++11 Concurrency Model
原始链接：https://sigplan.org/Awards/Dissertation/2015_batty.pdf

资料 22：Updating the Go Memory Model
原始链接：https://research.swtch.com/gomm.pdf

资料 23：Weak Ordering - A New Definition
原始链接：https://rsim.cs.uiuc.edu/Pubs/ps2pdf/isca90.pdf

资料 24：A Better x86 Memory Model: x86-TSO
原始链接：
https://www.cl.cam.ac.uk/~pes20/weakmemory/x86tso-paper.tphols.pdf

资料 25：Atomic Read-Modify-Write Primitives for I/O Devices
原始链接：
https://www.intel.com/content/dam/doc/white-paper/atomic-read-modify-write-primitives-i-o-devices-paper.pdf

资料 26：Intel® 64 Architecture Memory Ordering White Paper
原始链接：https://www.cs.cmu.edu/~410-f10/doc/Intel_Reordering_318147.pdf

资料 27：Memory barriers in C
原始链接：
https://mariadb.org/wp-content/uploads/2017/11/2017-11-Memory-barriers.pdf

资料 28：N3934: Towards Implementation and Use of memory order consume
原始链接：
http://www.rdrop.com/users/paulmck/scalability/paper/consume.2014.02.16c.pdf

资料 29：N2389-Clean up atomics, non-normative changes proposal for integration to C2x
原始链接：https://www.open-std.org/jtc1/sc22/wg14/www/docs/n2389.pdf