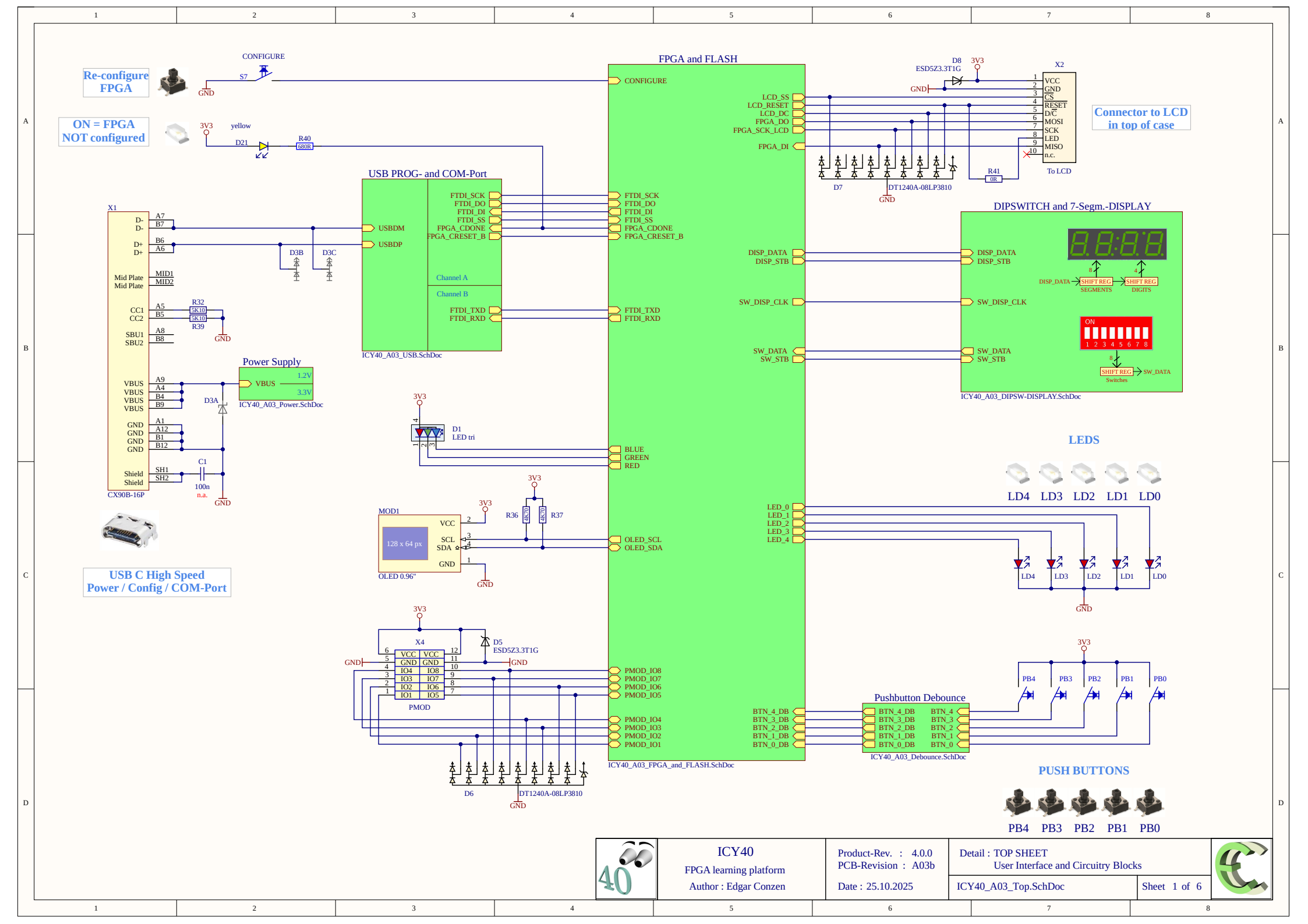
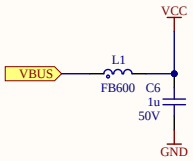
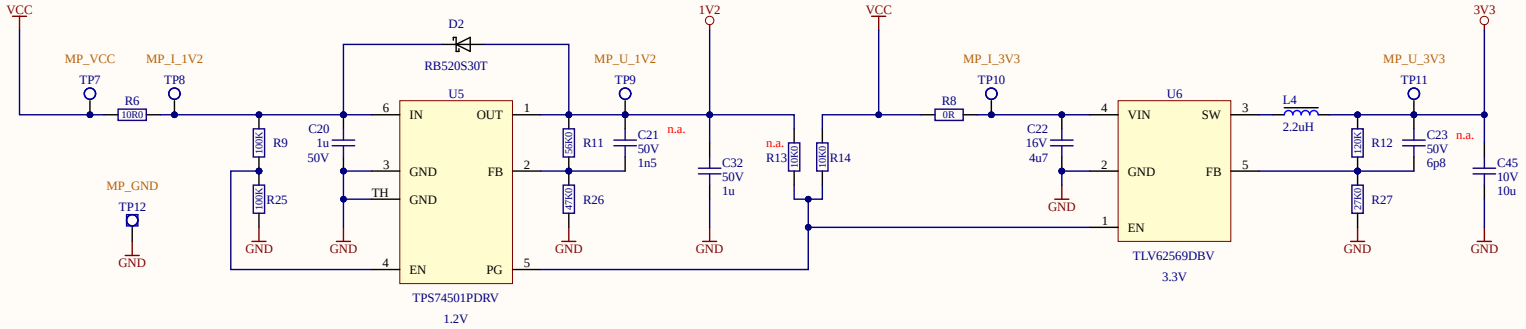

Re-configure FPGA
CONFIGURE
S7
GND
ON = FPGA NOT configured
3V3
yellow
D21
R40
680R
FPGA and FLASH
CONFIGURE
LCD_SS
LCD_RESET
LCD_DC
FPGA_DO
FPGA_SCK_LCD
FPGA_DI
D8
ESD5Z3.3T1G
3V3
GND
X2
VCC
GND
CS
RESET
D/C
MOSI
SCK
LED
MISO
n.c.
To LCD
Connector to LCD in top of case
D7
DT1240A-08LP3810
R41
0R
USB PROG- and COM-Port
FTDI_SCK
FTDI_DO
FTDI_DI
FTDI_SS
FPGA_CDONE
FPGA_CRESET_B
USBDM
USBDP
Channel A
Channel B
FTDI_TXD
FTDI_RXD
ICY40_A03_USB.SchDoc
X1
D-
D+
Mid Plate
CC1
CC2
SBU1
SBU2
VBUS
GND
Shield
CX90B-16P
D3B
D3C
R32
5K10
R39
C1
100n
n.a.
D3A
Power Supply
VBUS
1.2V
3.3V
ICY40_A03_Power.SchDoc
DISPSWITCH and 7-Segm.-DISPLAY
DISP_DATA
DISP_STB
SW_DISP_CLK
SW_DATA
SW_STB
SHIFT REG
SEGMENTS
DIGITS
Switches
ON
ICY40_A03_DIPSW-DISPLAY.SchDoc
D1
LED tri
BLUE
GREEN
RED
LEDS
LD4
LD3
LD2
LD1
LD0
LED_0
LED_1
LED_2
LED_3
LED_4
MOD1
128 x 64 px
VCC
SCL
SDA
GND
OLED 0.96"
R36
R37
4K70
OLED_SCL
OLED_SDA
X4
PMOD
PMOD_IO8
PMOD_IO7
PMOD_IO6
PMOD_IO5
PMOD_IO4
PMOD_IO3
PMOD_IO2
PMOD_IO1
D5
ESD5Z3.3T1G
D6
DT1240A-08LP3810
BTN_4_DB
BTN_3_DB
BTN_2_DB
BTN_1_DB
BTN_0_DB
Pushbutton Debounce
BTN_4
BTN_3
BTN_2
BTN_1
BTN_0
ICY40_A03_Debounce.SchDoc
ICY40_A03_FPGA_and_FLASH.SchDoc
PUSH BUTTONS
PB4
PB3
PB2
PB1
PB0
USB C High Speed
Power / Config / COM-Port
ICY40
FPGA learning platform
Author : Edgar Conzen
Product-Rev. : 4.0.0
PCB-Revision : A03b
Date : 25.10.2025
Detail : TOP SHEET
User Interface and Circuitry Blocks
ICY40_A03_Top.SchDoc
Sheet 1 of 6



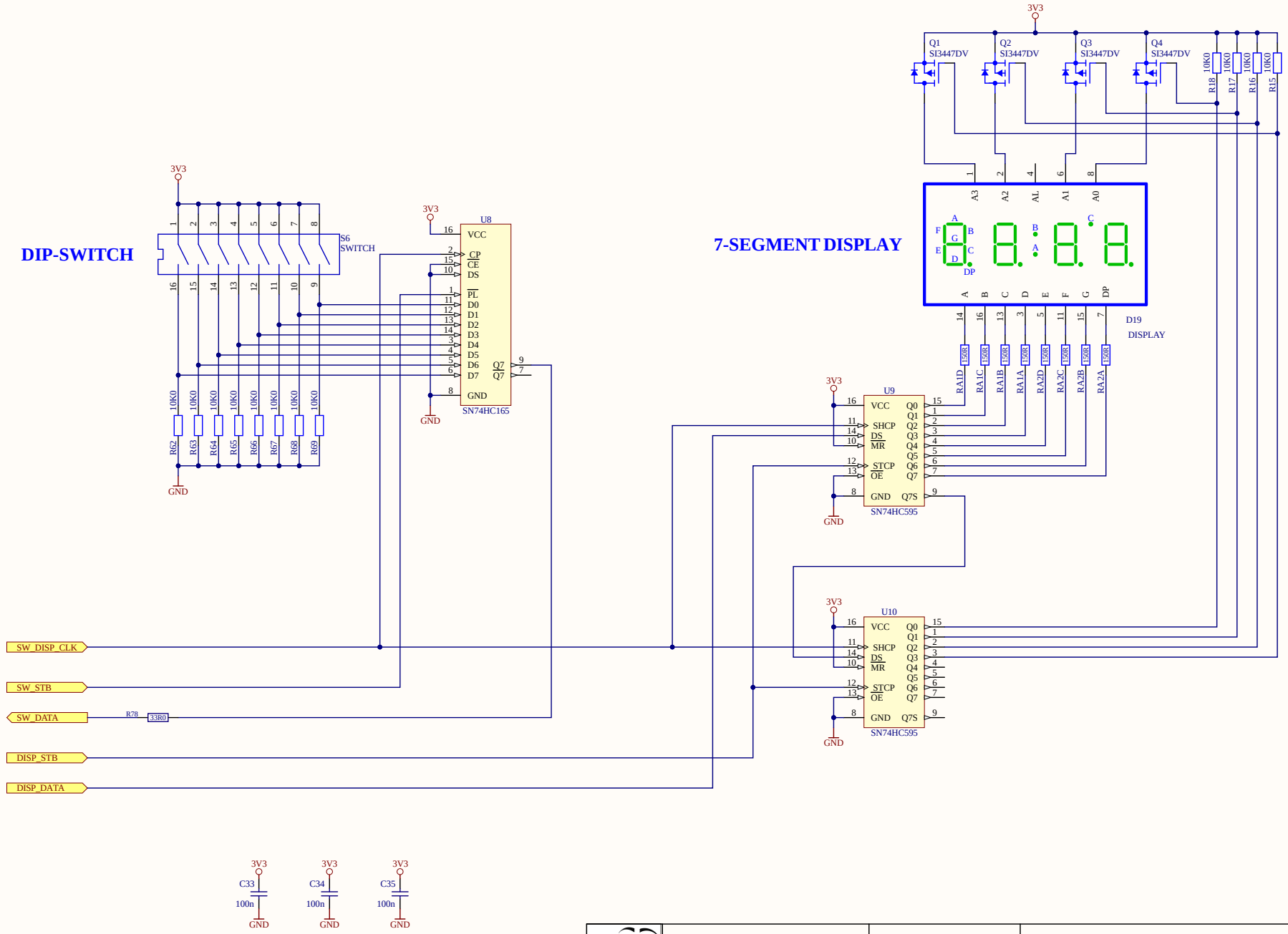
POWER SUPPLY, 1.2V & 3.3V

Power up sequence : 1.2V -> 3.3V

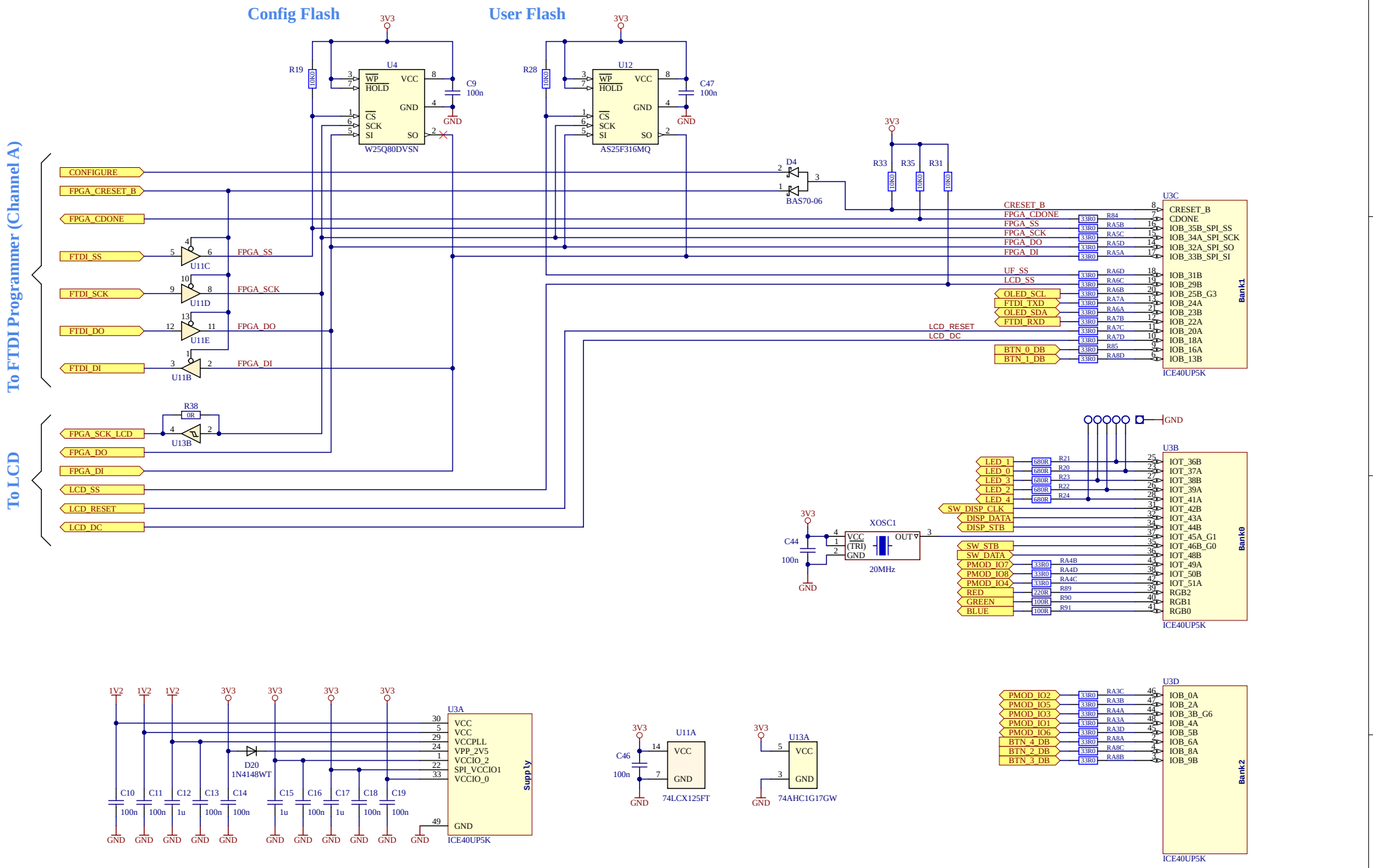
Slew rate : 0.6 .. 10 V/ms
Rise Time 1.2V : min 120us, max 2000us (1800us)
Rise Time 3.3V : min 330us, max 5500us (3800us)



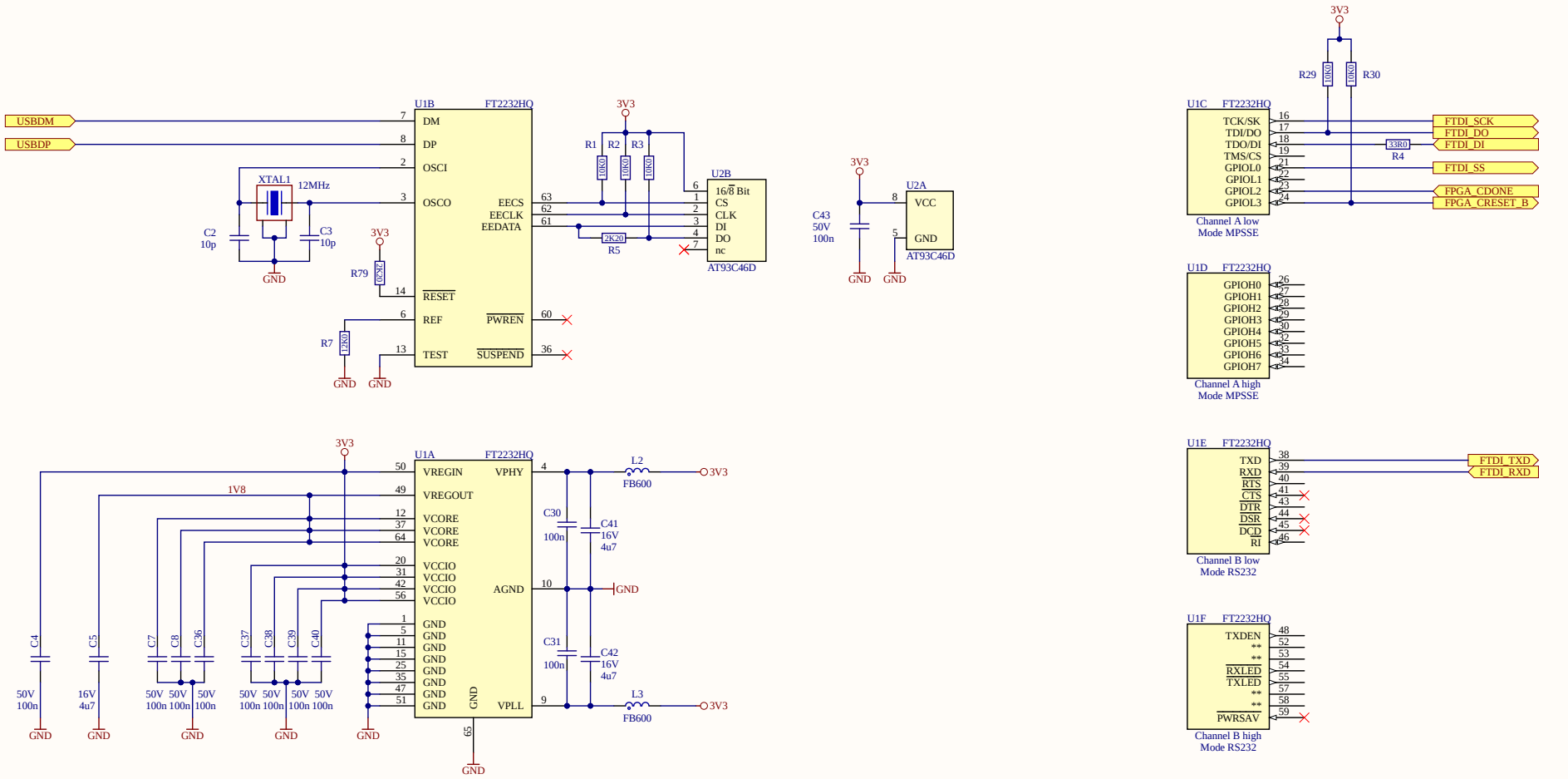
ICY40	Product-Rev. : 4.0.0	Detail : Subsheet Power Supply		
FPGA learning platform	PCB-Revision : A03b			
Author : Edgar Conzen	Date : 25.10.2025	ICY40_A03_Power.SchDoc	Sheet 2 of 6	



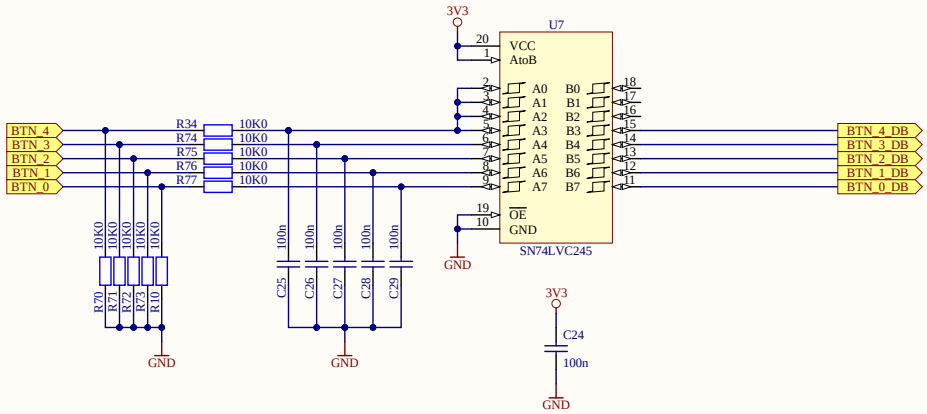
ICY40 FPGA learning platform Author : Edgar Conzen	Product-Rev. : 4.0.0 PCB-Revision : A03b Date : 25.10.2025	Detail : SWITCH & DISPLAY Dip-Switch and 7-Segment Display ICY40_A03_DIPSW-DISPLAY.SchDoc	Sheet 3 of 6



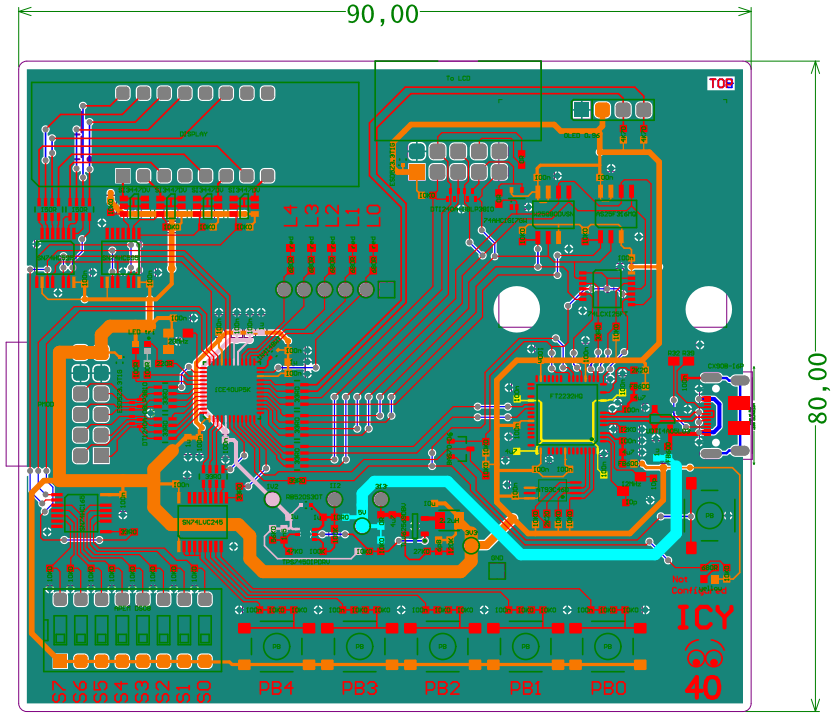
ICY40 FPGA learning platform Author : Edgar Conzen	Product-Rev. : 4.0.0 PCB-Revision : A03b Date : 25.10.2025	Detail : Subsheet FPGA and Configuration Flash	
		ICY40_A03_FPGA_and_FLASH.SchDoc	Sheet 4 of 6



ICY40 FPGA learning platform Author : Edgar Conzen	Product-Rev. : 4.0.0 PCB-Revision : A03b Date : 25.10.2025	Detail : Subsheet USB Interface Converter and Power Supply Block ICY40_A03_USB.SchDoc	Sheet 5 of 6



40	ICY40 FPGA learning platform Author : Edgar Conzen	Product-Rev. : 4.0.0 PCB-Revision : A03b Date : 25.10.2025	Detail : ICY40_A03_Debounce.SchDoc	Sheet 6 of 6



ICY40 FPGA learning platform Author : Edgar Conzen	Product-Rev. : 4.0.0 PCB-Revision : A03b Date : 25.10.2025