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Dynamic modeling, stability analysis, and controller design for DC distribution systems

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DYNAMIC MODELING, STABILITY ANALYSIS, AND CONTROLLER DESIGN

FOR DC DISTRIBUTION SYSTEMS

by

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Paper II,   Pages 49-93, "Dynamic Modeling and Stability Analysis of Converter-Dominated Dc Microgrids with Instantaneous Constant-Power Loads," submitted to *IEEE Transactions on Power Electronics*.

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ABSTRACT

The dc distribution systems or dc microgrids are known to be best suited for integration of renewable energy sources into the current power grid and are considered to be the key enabling technology for the development of future smart grid. Dc microgrids also benefit from better current capabilities of dc power lines, better short circuit protection, and transformer-less conversion of voltage levels, which result in higher efficiency, flexibility, and lower cost. While the idea of using a dc microgrid to interface distributed energy sources and modern loads to the power grid seems appealing at first, several issues must be addressed before this idea can be implemented fully. The configuration, stability, protection, economic operation, active management, and control of future dc microgrids are among the topics of interest for many researchers.

The purpose of this dissertation is to investigate the dynamic behavior and stability of a future dc microgrid and to introduce new controller design techniques for the Line Regulating Converters (LRC) in a dc distribution system. Paper I is devoted to dynamic modeling of power converters in a dc distribution system. The terminal characteristics of tightly regulated power converters which are an important factor for stability analysis and controller design are modeled in this paper. Paper II derives the simplified model of a dc distribution system and employs the model for analyzing stability of the system. Paper III introduces two controller design methods for stabilizing the operation of the LRC in presence of downstream constant power loads in a dc distribution system. Paper IV builds upon paper III and introduces another controller design method which uses an external feedback loop between converters to improve performance and stability of the dc grid.

ACKNOWLEDGMENTS

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1. INTRODUCTION

1.1. OVERVIEW OF DC DISTRIBUTION SYSTEMS

Diminishing fossil energy supplies and environmental obstacles pose increasing challenges to the traditional model of electricity generation and distribution. Harnessing renewable energy sources, such as solar and wind power, is considered one of the ideal means by which to tackle the energy crisis currently looming over the world. However, the spatially distributed and fluctuating nature of renewable energy sources challenges opportunities to integrate these sources into the current ac power grid. The dc distribution systems or dc microgrids on the other hand are known to be better suited for integration of renewable energy sources into the power grid and are considered to be the key enabling technology for the development of future smart grid.

The main advantage of employing dc distribution systems or dc microgrids is that they are better suited to integrate distributed and renewable energy sources into the power grid because the majority of these new alternative power sources are either inherently dc, such as solar and fuel cells, or, similar to wind power, can be interfaced to a dc system much more easily than an ac system using simple power electronic converter topologies. The other equally important advantage of employing dc microgrids is that most modern electronic loads, such as computers, data centers, and LED lights, as well as adjustable speed drives, require dc voltage.

Furthermore, most common energy storage devices, such as batteries in hybrid electric vehicles, are inherently dc devices. Dc microgrids also benefit from better current capabilities of dc power lines, better short circuit protection, and transformer-less

conversion of voltage levels, which result in higher efficiency and flexibility, and lower cost of the distribution network.

Dc distribution was one of the main rivals of the current ac distribution in the early years of the growth of electricity distribution systems in the late 1880s. The rivalry instigated the "war of currents" era, with George Westinghouse and Thomas Edison in opposing battle fronts, and eventually led to the adoption of ac distribution systems because of some fundamental demerits of the dc systems at the time, such as inefficient voltage conversion techniques and incompatibility with induction motors, which were the workhorse of the Industrial Revolution.

However, nowadays, new highly efficient power electronic technologies have overcome the deficiencies of dc distribution systems and even have added several advantages to employing dc systems over traditional ac distribution systems in the development of the future smart grid.

While the idea of using a dc microgrid to interface distributed energy sources and modern loads to the power grid seems appealing at first, several issues must be addressed before this idea can be implemented fully [1-4]. The configuration, stability, protection, economic operation, active management, and control of future dc microgrids are among the topics of interest for many researchers; most of these topics are still considered open problems and require further study.

In [5-12] authors provide several configurations for a future dc distribution system and analyze operational merits of a dc microgrid for integration of distributed generation into the grid. Additionally, possibility of integration of storage devices into the grid for more flexibility is discussed in [4] as well. In [13-15] application of dc

microgrids for residential houses and urban settings is explored. Specifically, in [15] characteristics of a dc microgrid for residential houses with cogeneration system in each house is inspected. In [16-28] several analysis methods, including hardware-in-the-loop simulation, reduced order modeling, and large scale modeling are introduced for dc microgrids. Moreover [29-36] address the issue of higher level control and power management of a dc microgrid. Furthermore, in [37] authors propose a solid-state transformer for voltage conversion in zonal dc microgrids and in [38] possibility of integration of dc microgrids into the smart grid is discussed.

1.2. DYNAMIC MODELING OF POWER CONVERTERS IN A DC DISTRIBUTION SYSTEM

Middlebrook's impedance criteria is the long-established approach for analyzing the stability in a dc distribution system [39-41]. In this method, the ratio of the output impedance of the source subsystem to the input impedance of the load subsystem in the frequency domain, known as the minor loop gain, is analyzed using any of the classical stability evaluation methods, such as the Nyquist diagram or the Bode plot. Numerous publications have described this method and defined explicit stability and design criteria for specific applications based on this method.

Although knowledge of the input and output impedances of the converters integrated into the dc distribution systems is a prerequisite for utilizing Middlebrook's theorem, this information has always been treated as a known assumption in the literature concerned with the stability of dc distribution networks. This has resulted in the literature containing little to no accurate information about modeling the input and output impedances of the power converters integrated in dc distribution networks.

The few papers that investigate deriving these impedances for a specific converter usually overlook two major factors [41, 42]. The first factor is that in converters operating with a voltage or current regulation loop, the closed-loop input and output impedances, rather than the open-loop impedances, should be calculated and used for the stability analysis. The control loop affects the dynamic properties and thus the input and output impedances of the converter, so it should be considered in modeling these impedances. The second overlooked factor is that the loading effect of the load subsystem alters the dynamic behavior of the source converter. Therefore, the input and output impedances of a converter should be derived while it is integrated inside the network rather than when operating singly.

The purpose of the first paper is to set forth a straightforward method for developing a precise model of a power converter and for deriving the closed-loop input and output impedances of the converter, as well as other important transfer functions required for stability analysis and controller design. The closed-loop transfer functions are formulated for both the case in which the converter operates with only a voltage regulation loop (voltage mode control) and the case in which it operates with a voltage regulation loop integrating an internal current control modulator (current mode control).

The modeling process is described considering the converter in a dc distribution network rather than in isolation. The entire procedure for modeling the converter and deriving the closed-loop impedances is performed on a buck-boost converter for better clarification of all steps. Additionally, the resulting transfer functions for several power converters are listed in the appendix; these can be used directly by design engineers without the need to go through the modeling process.

1.3. STABILITY ANALYSIS OF DC DISTRIBUTION SYSTEMS WITH CONSTANT POWER LOADS

The second paper investigates the dynamic behavior and stability of a future dc microgrid. Most distributed energy sources and modern loads are connected to the dc microgrid by means of power electronic converters, so future microgrids are expected to be mostly converter-dominated grids.

In the majority of applications, the back-end or point-of-load converters require strict output voltage regulation to satisfy the voltage requirement of the loads. Furthermore, because of their high efficiency, they draw constant power and thus exhibit negative incremental impedance. This causes stability problems for the entire system and is considered a major issue of dc distributed power systems that requires further investigation.

1.4. CONTROLLER DESIGN METHODS FOR PERFORMANCE IMPROVEMENT OF THE LINE REGULATING CONVERTER IN A CONVERTER-DOMINATED DC MICROGRID SYSTEM

The methods for addressing the problem with constant power loads (CPLs) in a dc distribution system can be classified into passive damping methods and active stabilization methods. The passive damping methods suggest using passive elements to damp the oscillations on the dc bus to improve the stability of the system. Some of the passive damping methods proposed in the literature are, use of damping resistances, passive filters, storage units, and Ultra-capacitors [43, 44]. Most of the passive damping solutions increase losses, complexity, and the overall cost of the system.

The active damping methods on the other hand, usually use more advanced control methods to improve the overall stability of the system. There are a few active damping methods proposed in the literature recently [45-47]. A nonlinear line-regulating compensator, for instance, is proposed in [45] which works locally to compensate for the CPL effect. However, the complexity of this nonlinear controller makes it less practical.

The purpose of the third paper is to propose methods to design superior linear controllers which perform better in a dc distributed network with presence of CPLs and improve the performance and stability of the system.

1.5. THE EXTRA FEEDBACK METHOD FOR IMPROVING THE PERFORMANCE AND STABILITY OF THE DC DISTRIBUTION SYSTEM

The aim of the fourth paper is to introduce a new stabilizing method for dc distribution systems. In this method the converters in a dc grid communicate with the LRC through external feedback loops when there is a disturbance in their operation. The information being communicated to the LRC eliminates the normal time delay until the LRC actually sees the disturbance on the bus and allows it to act faster to eliminate the voltage oscillations resulting from the disturbance.

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PAPER

I. Modeling Closed-Loop Terminal Characteristics Of Dc/Dc Power Converters With Voltage Mode Or Current Mode Controllers For Stability Analysis In Dc Distribution Networks

Reza Ahmadi, and Mehdi Ferdowsi

ABSTRACT -- This paper sets forth a straightforward procedure for developing a detailed model of a power converter for the purpose of formulating the closed-loop terminal characteristics of a converter when operating within a dc distribution network. First, the procedures for modeling the converter and deriving the open-loop transfer functions are discussed. A general dynamic model for a typical power converter is introduced in this stage. Next, the introduced model is expanded to the closed-loop model of the power converter operating with voltage or current mode controllers. Then, the closed-loop input and output impedances of the converter are formulated based on the closed-loop model. These impedances can be used for stability analysis and controller design in dc distribution networks. Finally, the theoretical outcomes are verified using experimental results from a built prototype system.

I. INTRODUCTION

The traditional hierarchical, unidirectional, and centrally controlled model of electricity generation and distribution recently has been challenged by reliability issues and diminishing fossil energy supplies. Exploiting renewable energy sources, such as solar and wind power, is proving to be one of the noblest means by which to address

these issues and to overcome the worldwide energy crisis [1, 2]. However, the distributed and fluctuating nature of renewable energy sources poses serious challenges to integrating these sources into the current power grid [3, 4]. Therefore, the dc distribution systems, which are far superior for integrating renewable energy sources into the current grid, recently have been the focus of power engineers.

Despite the advantages of dc distribution systems, many obstacles plague the safe, efficient, and reliable operation of these systems. Investigating the dynamic behavior and stability of a future dc distribution system is amongst the most intriguing topics of interest for engineers and is still considered an open problem in academia and industry [5-13]. The stability problem arises because future dc distribution systems are anticipated to be mostly converter-dominated grids. With their tight voltage regulation requirements and high efficiency, converters draw constant power and exhibit negative incremental impedance, which causes stability problems for the entire system.

Middlebrook's impedance criterion is the long-established approach for analyzing the stability in a dc distribution system [14]. In this method, the ratio of the output impedance of the source subsystem to the input impedance of the load subsystem in the frequency domain, known as the minor loop gain, is analyzed using any of the classical stability evaluation methods, such as the Nyquist diagram or the Bode plot. Numerous publications have described this method and defined explicit stability and design criteria for specific applications based on this method [15-20].

Although knowledge of the input and output impedances of the converters integrated into the dc distribution systems is a prerequisite for utilizing Middlebrook's theorem, this information has always been treated as a known assumption in the literature

concerned with the stability of dc distribution networks. This has resulted in the literature containing little to no accurate information about modeling the input and output impedances of the power converters integrated in dc distribution networks. The few papers that investigate deriving these impedances for a specific converter usually overlook two major factors. The first factor is that in converters operating with a voltage or current regulation loop, the closed-loop input and output impedances, rather than the open-loop impedances, should be calculated and used for the stability analysis. The control loop affects the dynamic properties and thus the input and output impedances of the converter, so it should be considered in modeling these impedances. The second overlooked factor is that the loading effect of the load subsystem alters the dynamic behavior of the source converter. Therefore, the input and output impedances of a converter should be derived while it is integrated inside the network rather than when operating singly.

The purpose of this work is to set forth a straightforward method for developing a precise model of a power converter and for deriving the closed-loop input and output impedances of the converter, as well as other important transfer functions required for stability analysis and controller design. The closed-loop transfer functions are formulated for both the case in which the converter operates with only a voltage regulation loop (voltage mode control) and the case in which it operates with a voltage regulation loop integrating an internal current control modulator (current mode control). The modeling process is described considering the converter in a dc distribution network rather than in isolation. The entire procedure for modeling the converter and deriving the closed-loop impedances is performed on a buck-boost converter for better clarification of all steps.

Additionally, the resulting transfer functions for several power converters are listed in the appendix; these can be used directly by design engineers without the need to go through the modeling process.

The remainder of the paper is organized as follows. Section II details the state-space averaging method for deriving the open-loop transfer functions of the converter required for calculating the closed-loop impedances. Additionally, a general dynamic model of a power converter based on the derived open-loop transfer functions is introduced in this section. Section III derives the closed-loop input and output impedances of the power converter in voltage mode and current mode by building upon the model introduced in Section II. Section IV verifies the theoretical outcomes by analyzing the stability of a built prototype cascaded converter system and comparing the results predicted from the theory with the results yielded from the experimental system. Section V concludes this paper.

II. OPEN-LOOP CONVERTER TRANSFER FUNCTIONS

Fig. 1 shows the buck-boost converter being modeled. As pictured, a current source (i_{load}) is connected to the output terminals of the converter. This current source models the loading effect of the load subsystem (besides the resistive load) being fed from this converter. The converter consists of only one active switch (S_1) that can be ON or OFF and thus has two modes of operation.
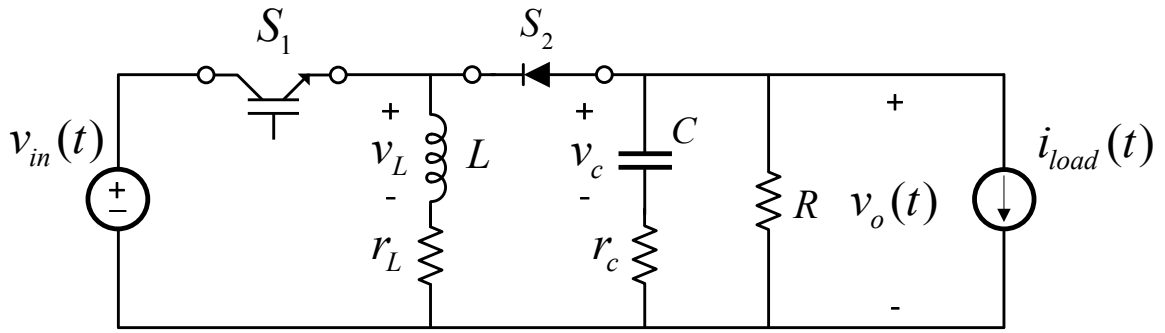
Fig. 1. Buck-boost converter modeled in this paper

Fig. 2 shows the first mode of operation, in which S_1 is ON and S_2 is OFF. The duration of this mode equals DT seconds, where D is the duty cycle of switch S_1, and T is the switching period.
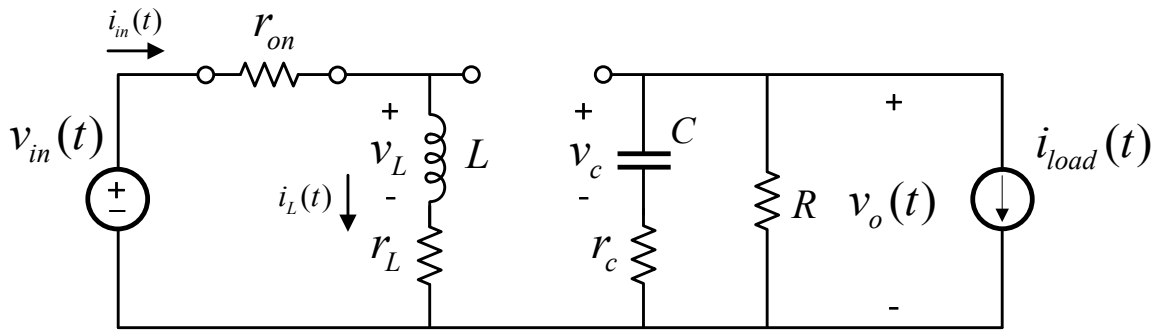
Fig. 2. First mode of operation of the buck-boost converter, in which S_1 is in the ON state and D_1 is in the OFF state.

The state equations for mode 1 can be obtained by writing KVL and KCL equations for the circuit shown in Fig. 2,

$$\begin{cases} L\dfrac{di_L(t)}{dt} = -\left(r_{on} + r_L\right)i_L(t) + v_{in}(t) \\[2mm] C\dfrac{dv_c(t)}{dt} = \dfrac{-1}{R+r_c}v_c(t) - \dfrac{R}{R+r_c}i_{load}(t) \end{cases} \tag{1}$$

Additionally, based on the circuit topology, the input current and output voltage are,

$$i_{in}(t) = i_L(t) \tag{2}$$

$$v_o(t) = r_c C\dfrac{dv_c(t)}{dt} + v_c(t) = \dfrac{-Rr_c}{R+r_c}i_L(t) + \dfrac{R}{R+r_c}v_c(t) - \dfrac{Rr_c}{R+r_c}i_{load}(t) \tag{3}$$

These equations can be merged into a descriptor state-space model as follows,

$$\begin{cases} K\dot{x}(t) = A_1 x(t) + B_1 u(t) \\ y(t) = C_1 x(t) + D_1 u(t) \end{cases} \tag{4}$$

Where the state, input, and output vectors are defined as,

$$x(t) = \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix}$$

$$u(t) = \begin{bmatrix} v_{in}(t) \\ v_d(t) \\ i_{load}(t) \end{bmatrix} \tag{5}$$

$$y(t) = \begin{bmatrix} i_{in}(t) \\ v_o(t) \\ i_L(t) \end{bmatrix}$$

Based on the definition of these vectors, the K, A_1, B_1, C_1, and D_1 matrices can be found from (1)-(4),

$$A_1 = \begin{bmatrix} -(r_{on} + r_L) & 0 \\ 0 & \dfrac{-1}{R + r_c} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & \dfrac{-R}{R + r_c} \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 1 & 0 \\ 0 & \dfrac{R}{R + r_c} \\ 1 & 0 \end{bmatrix} \tag{6}$$

$$D_1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \dfrac{-R r_c}{R + r_c} \\ 0 & 0 & 0 \end{bmatrix}$$

$$K = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}$$

Fig. 3 shows the second mode of operation, in which S_1 is OFF and S_2 is ON. The duration of this mode equals *(1-D)T* seconds.
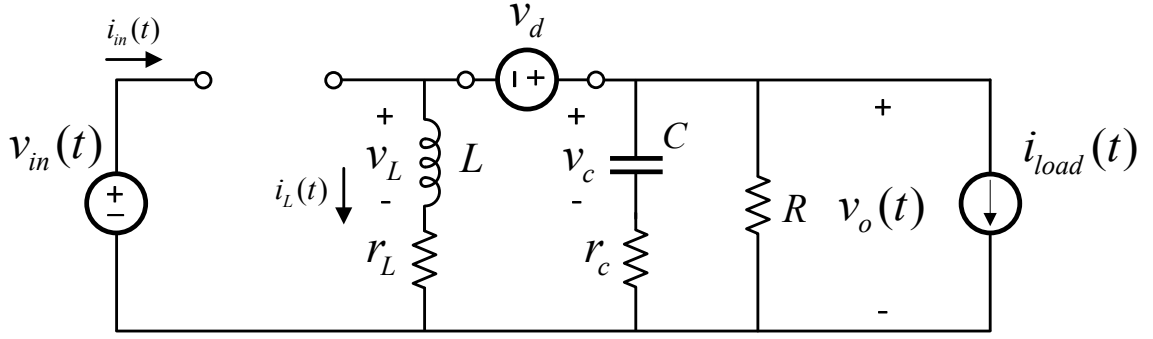
Fig. 3. Second mode of operation of the buck-boost converter, in which S_1 is in the OFF state and D_1 is in the ON state.

Similar to the previous case, the state, input current, and output voltage equations can be found from the circuit topology,

$$\begin{cases} L\dfrac{di_L(t)}{dt} = \left(\dfrac{-Rr_c}{R+r_c} - r_L\right)i_L(t) + \dfrac{R}{R+r_c}v_c(t) - v_d(t) - \dfrac{Rr_c}{R+r_c}i_{load}(t) \\[3mm] C\dfrac{dv_c(t)}{dt} = \dfrac{-R}{R+r_c}i_L(t) - \dfrac{1}{R+r_c}v_c(t) - \dfrac{R}{R+r_c}i_{load}(t) \end{cases} \tag{7}$$

$$i_{in}(t) = 0 \tag{8}$$

$$v_o(t) = r_c C\dfrac{dv_c(t)}{dt} + v_c(t) = \dfrac{R}{R+r_c}v_c(t) - \dfrac{Rr_c}{R+r_c}i_{load}(t) \tag{9}$$

These equations are merged into a second state space model as follows,

$$\begin{cases} K\dot{x}(t) = A_2 x(t) + B_2 u(t) \\ y(t) = C_2 x(t) + D_2 u(t) \end{cases} \tag{10}$$

Where the state, input, and output vectors are defined similar to (5). As a result, matrices A_2, B_2, C_2, and D_2 can be found from (7)-(10),

$$A_2 = \begin{bmatrix} \dfrac{-Rr_c}{R+r_c} - r_L & \dfrac{R}{R+r_c} \\ \dfrac{-R}{R+r_c} & \dfrac{-1}{R+r_c} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 0 & -1 & \dfrac{-Rr_c}{R+r_c} \\ 0 & 0 & \dfrac{-R}{R+r_c} \end{bmatrix}$$

$$C_2 = \begin{bmatrix} 1 & 0 \\ \dfrac{-Rr_c}{R+r_c} & \dfrac{R}{R+r_c} \\ 1 & 0 \end{bmatrix} \qquad (11)$$

$$D_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \dfrac{-Rr_c}{R+r_c} \\ 0 & 0 & 0 \end{bmatrix}$$

Knowing the state-space equations for each mode of operation ((4) and (10)) the small-signal state-space model of the converter can be found by averaging the two sets of stat-space equations over a switching period and perturbing and linearizing the resulting state-space model around a certain operating point [21]. The resulting small-signal state-space model is found in [21],

$$\begin{cases} K\dot{\bar{x}}(t) = A_{avg}\bar{x}(t) + B_{avg}\bar{u}(t) + E\bar{d}(t) \\ \bar{y}(t) = C_{avg}\bar{x}(t) + D_{avg}\bar{u}(t) + F\bar{d}(t) \end{cases} \qquad (12)$$

In (12) the vectors with bar sign ($\bar{x}(t), \bar{u}(t)$, and $\bar{y}(t)$) represent the small-signal values of the states, inputs, and outputs, respectively, and $\bar{d}(t)$ represents the small-signal value of the duty cycle. The A_{avg}, B_{avg}, C_{avg}, D_{avg}, E, and F matrices are found in [21],

$$\bar{y}(t)\ A_{avg} = DA_1 + (1-D)A_2$$
$$B_{avg} = DB_1 + (1-D)B_2$$
$$C_{avg} = DC_1 + (1-D)C_2$$
$$D_{avg} = DD_1 + (1-D)D_2 \qquad (13)$$
$$E = (A_1 - A_2)X_{eq} + (B_1 - B_2)U_{eq}$$
$$F = (C_1 - C_2)X_{eq} + (D_1 - D_2)U_{eq}$$

Where X_{eq} is the vector of the equilibrium point or the dc values of states for a specific

input vector U_{eq}, and D is the value of the duty cycle for an operating point. X_{eq} can be

found from,

$$X_{eq} = -A_{avg}^{-1}B_{avg}U_{eq} \qquad (14)$$

The small-signal state-space model of typical converters (12) can be found by calculating

the matrices in (13) and (14) given that the state-space model of the converter in each

mode of operation and thus $A_1,\ B_1,\ C_1,\ D_1,\ A_2,\ B_2,\ C_2,$ and D_2 matrices are known.

Because the parasitic resistances ($r_c,\ r_L,\ r_{on}$) and diode forward bias voltage (v_d) are

considered in the circuit topology of the buck-boost converter from the beginning, the

matrices in (13) and (14) exhibit rather complicated elements. Therefore, at this stage,

the parasitic resistance values and v_d are set to zero to simplify the results. The appendix

reports the results with parasitic resistances $r_L,\ r_c$. With this assumption, the matrices in

(13) and (14) for the buck-boost converter are found as,

$$A_{avg} = \begin{bmatrix} 0 & 1-D \\ -(1-D) & \dfrac{-1}{R} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} D & -(1-D) & 0 \\ 0 & 0 & -1 \end{bmatrix}$$

$$C_2 = \begin{bmatrix} D & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}$$

$$D_{avg} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$U_{eq} = \begin{bmatrix} V_{in} \\ 0 \\ I_{Load} \end{bmatrix}$$

$$X_{eq} = \begin{bmatrix} I_L \\ V_c \end{bmatrix} = \begin{bmatrix} \dfrac{D V_{in}}{(1-D)^2 R} - \dfrac{I_{Load}}{1-D} \\ \dfrac{-D}{1-D} V_{in} \end{bmatrix}$$

$$E = \begin{bmatrix} \dfrac{V_{in}}{1-D} \\ \dfrac{D V_{in}}{(1-D)^2 R} - \dfrac{I_{Load}}{1-D} \end{bmatrix}$$

$$F = \begin{bmatrix} \dfrac{D V_{in}}{(1-D)^2 R} - \dfrac{I_{Load}}{1-D} \\ 0 \\ 0 \end{bmatrix}$$

(15)

Where I_{Load} is the dc value of the current (no small-signal content) being drawn from the converter by the downstream network, and V_{in} is the dc value of the input voltage (no small-signal content) to the converter. The state-space equations in (12) with the matrices in (15) completely model the small-signal behavior of the buck-boost converter being studied. However, in this analysis, it is more useful to describe the small-signal model in terms of transfer functions rather than state-space representation. The transfer function $\bar{d}(s) = 0$ s describing the small-signal behavior of this converter can be found by taking the Laplace transform of the equations in (12) and calculating the output vector based on the inputs and duty cycle. Following this procedure yields the following result,

$$\bar{y}(s) = H(s)\bar{u}(s) + G(s)\bar{d}(s) \tag{16}$$

Where,

$$H(s) = C_{avg}\left(sI - K^{-1}A_{avg}\right)^{-1}K^{-1}B_{avg} + D_{avg}$$

$$G(s) = C_{avg}\left(sI - K^{-1}A_{avg}\right)^{-1}K^{-1}E + F \tag{17}$$

Based on (16) and (17), when $\bar{d}(s) = 0$ and $\bar{i}_{load}(s) = 0$, the following transfer functions are found,

$$Z_{in}^{-1}(s) = \frac{\bar{i}_{in}(s)}{\bar{v}_{in}(s)} = H_{11}(s)$$

$$G_{vg}(s) = \frac{\bar{v}_{o}(s)}{\bar{v}_{in}(s)} = H_{21}(s) \tag{18}$$

$$G_{ig}(s) = \frac{\bar{i}_{L}(s)}{\bar{v}_{in}(s)} = H_{31}(s)$$

Where $Z_{in}(s)$ is the open-loop input impedance of the converter. Similarly, when $\bar{u}(s) = 0$, the following transfer functions are found,

$$G_{ind}(s) = \frac{\overline{i}_{in}(s)}{\overline{d}(s)} = G_{11}(s)$$

$$G_{vd}(s) = \frac{\overline{v}_{o}(s)}{\overline{d}(s)} = G_{21}(s) \tag{19}$$

$$G_{id}(s) = \frac{\overline{i}_{L}(s)}{\overline{d}(s)} = G_{31}(s)$$

Finally, when $\overline{v}_{in}(s) = 0$ and $\overline{d}(s) = 0$, the following transfer functions are found,

$$G_{inL}(s) = \frac{\overline{i}_{in}(s)}{\overline{i}_{load}(s)} = H_{13}(s)$$

$$-Z_{out}(s) = \frac{\overline{v}_{o}(s)}{\overline{i}_{load}(s)} = H_{23}(s) \tag{20}$$

$$G_{iL}(s) = \frac{\overline{i}_{L}(s)}{\overline{i}_{load}(s)} = H_{33}(s)$$

Where $Z_{out}(s)$ is the open-loop output impedance of the converter.

These transfer functions can be derived for typical power converters from (17)-(20) given that the small-signal state-space model of the converter in (12) is known. For the buck-boost converter, the $H(s)$ and $G(s)$ matrices in (17) can be calculated by substituting the results of (15) into (17). The transfer functions in (18)-(19) are the elements of $H(s)$ and $G(s)$,

$$Z_{in}^{-1}(s) = H_{11}(s) = \frac{D^2}{(1-D)^2} \frac{Cs + \dfrac{1}{R}}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$G_{vg}(s) = H_{21}(s) = \frac{-D}{1-D} \frac{1}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$G_{ig}(s) = H_{31}(s) = \frac{D}{(1-D)^2} \frac{Cs + \dfrac{1}{R}}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$G_{ind}(s) = G_{11}(s) = I_L \frac{CL_e\left(1 + R\dfrac{I_{Load}}{V_o}\right)s^2 + \dfrac{L_e}{R}\left(1 + R\dfrac{I_{Load}}{V_o}\right)s + \dfrac{CRs + 2 + R\dfrac{I_{Load}}{V_o}}{(1-d)}}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$G_{vd}(s) = G_{21}(s) = \frac{V_o}{D(1-D)} \frac{\left(1 - \dfrac{DL_e}{R}s\right) - \dfrac{I_{Load}}{V_o}DL_es}{CL_es^2 + \dfrac{L_e}{R}s + 1} \tag{21}$$

$$G_{id}(s) = G_{31}(s) = -\frac{V_o(1+D)}{D(1-D)^2} \frac{\left(\dfrac{Cs}{D+1} + \dfrac{1}{R}\right) + \dfrac{I_{Load}}{V_o}\dfrac{D}{1+D}}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$G_{inL}(s) = H_{13}(s) = \frac{-D}{1-D} \frac{1}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$-Z_{out}(s) = H_{23}(s) = -\frac{L_es}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

$$G_{iL}(s) = H_{33}(s) = \frac{-1}{1-D} \frac{1}{CL_es^2 + \dfrac{L_e}{R}s + 1}$$

Where L_e is the effective inductance of the converter and equals,

$$L_e = \frac{L}{(1-D)^2} \tag{22}$$

As noted, a comprehensive list of all of the transfer functions for buck, boost, and buck-boost converters with parasitic resistances r_L, r_c appears in the appendix. Deriving all of these transfer functions, especially with parasitic values, is a tedious task to be performed by hand. Therefore, the authors have used MATLAB Symbolic to calculate these transfer functions. The MATLAB code is available at [22] so that the readers can download and use the code. This code calculates all the transfer functions for the buck, boost, and buck-boost converters, with the option to include any of the parasitic values in the calculations. Additionally, the readers can enter the A_1, B_1, C_1, D_1, A_2, B_2, C_2, and D_2 matrices for any desired converter into the code and run the code to find all the transfer functions for that converter. Also, using this code, the readers can substitute the values of the converter parameters into the symbolic transfer functions in order to find the actual transfer functions in the ZPK domain, which can be used directly in MATLAB for stability analysis, controller design, etc.

Based on (18)-(20), the three values defined as the outputs of the system (i_{in}, v_o, i_L) can be described in terms of the sum of the multiplication of inputs by the derived transfer functions,

$$\bar{v}_o(s) = G_{vg}(s)\bar{v}_{in}(s) + G_{vd}(s)\bar{d}(s) + (-Z_{out}(s))\bar{i}_{load}(s)$$

$$\bar{i}_L(s) = G_{ig}(s)\bar{v}_{in}(s) + G_{id}(s)\bar{d}(s) + G_{iL}\bar{i}_{load}(s) \tag{23}$$

$$\bar{i}_{in}(s) = Z_{in}^{-1}(s)\bar{v}_{in}(s) + G_{ind}(s)\bar{d}(s) + G_{inL}\bar{i}_{load}(s)$$

The block diagram model of a converter, as shown in Fig. 4, can be realized using (23).
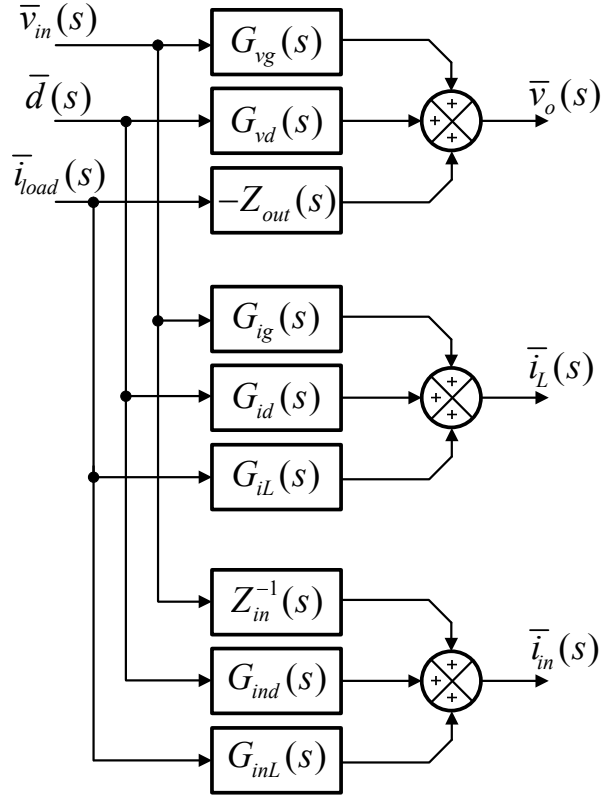
Fig. 4. General model of a power converter derived from (23) based on the open-loop transfer functions of the converter.

This model describes the small-signal dynamic behavior of the output voltage, inductor current, and input current based on the converter transfer functions and the small-signal values of the inputs, i.e., the input voltage, duty cycle, and load current. This general model works for different types of converters. To convert the model to the model of a specific type of converter, the required transfer functions listed in (18)-(20) should be calculated and used in place of the transfer functions inside the blocks shown in Fig. 4.

In the next section, this model is used as a universal model to calculate the parametric closed-loop input and output transfer functions of any type of converter that can be modeled similar to Fig. 4.

III. CLOSED-LOOP INPUT AND OUTPUT IMPEDANCES

A. Converter with Voltage Mode Control (VMC)

Fig. 5 shows a general power converter with a typical output voltage controller loop. The voltage controller loop shown in Fig. 5 can be modeled by adding a few extra blocks to the model in Fig. 4 [23].
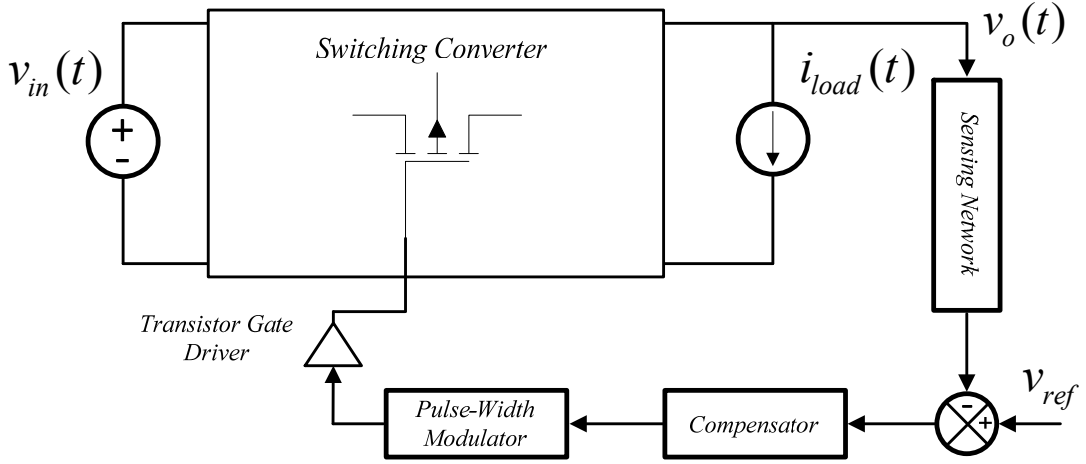
Fig. 5. General power converter with a typical output voltage controller loop.

The resulting closed-loop model is illustrated in Fig. 6. As pictured, the sensing network used for measuring the output voltage is modeled with a transfer function *S(s)*, the compensator (controller) transfer function is shown as $G_c(s)$, and the gain of the Pulse-Width Modulator (PWM) unit is modeled with a pure gain, G_M [21].
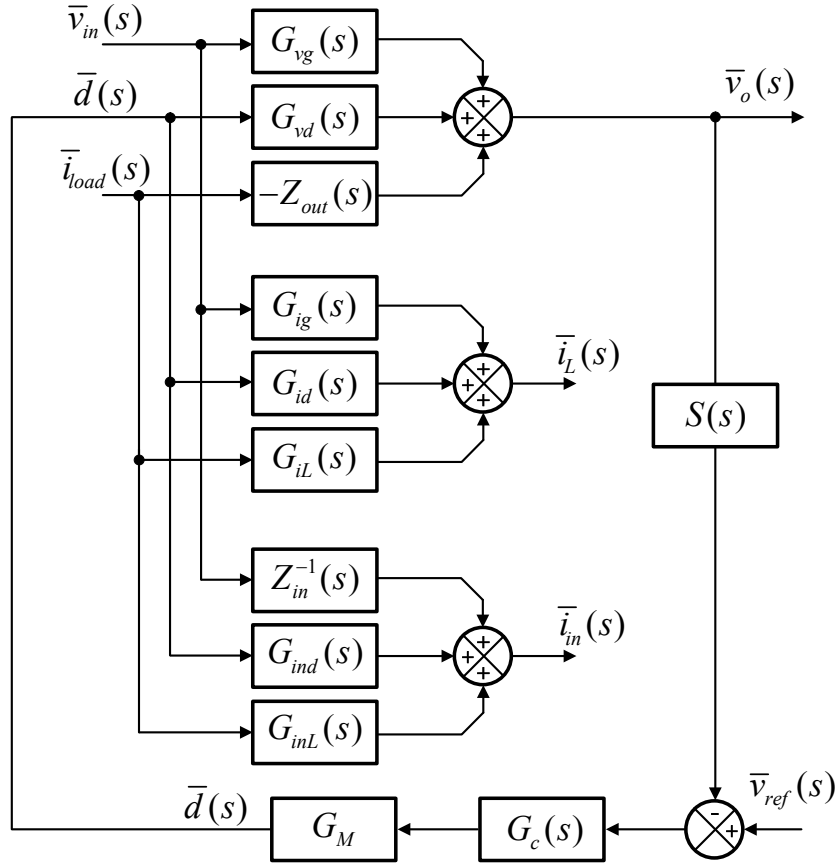
Fig. 6. Closed-loop model of a general power converter operating with a voltage control loop.

The closed-loop output impedance of a converter is defined as the negative of the ratio of the small-signal value of the output voltage to the small-signal value of the load current when the small-signal value of the input voltage equals zero[21],

$$Z_{outCL}(s) = -\frac{\overline{v}_o(s)}{\overline{i}_{load}(s)}\bigg|_{\overline{v}_i(s)=0} \tag{24}$$

This transfer function can be calculated by solving the following system of equations derived from Fig. 6 for $\overline{v}_o(s)$ and then dividing the result by $\overline{i}_{load}(s)$,

$$\begin{cases} \overline{d}(s) = -\overline{v}_o(s)S(s)G_c(s)G_M \\ \overline{v}_o(s) = G_{vd}(s)\overline{d}(s) + (-Z_{out}(s))\overline{i}_{load}(s) \end{cases} \tag{25}$$

The result equals,

$$Z_{outCL}(s) = -\left.\frac{\overline{v}_o(s)}{\overline{i}_{load}(s)}\right|_{\overline{v}_i(s)=0} = \frac{Z_{out}(s)}{1+T_v(s)} \tag{26}$$

Where $T_v(s)$ is the loop gain,

$$T_v(s) = G_c(s)S(s)G_{vd}(s)G_M \tag{27}$$

Therefore, to find the closed-loop impedance of a certain converter, the required open-loop transfer functions among those listed in (18)-(20) first are derived using the method discussed in the previous section; then, these transfer functions are substituted in (26). The open-loop transfer functions for buck, boost, and buck-boost converters appear in the appendix.

The closed-loop input impedance of a converter is defined as the ratio of the small-signal value of the input voltage to the small-signal value of the input current when the small-signal value of the load current equals zero [21],

$$Z_{inCL}(s) = \left.\frac{\overline{v}_i(s)}{\overline{i}_{in}(s)}\right|_{\overline{i}_{load}(s)=0} \tag{28}$$

Similar to the previous case, the closed-loop input impedance can be found by solving the following system of equations (derived from Fig. 6) for $\overline{v}_i(s)$ and then dividing the result by $\overline{i}_{in}(s)$,

$$\begin{cases} \overline{d}(s) = -\overline{v}_o(s)S(s)G_c(s)G_M \\ \overline{i}_{in}(s) = Z_{in}^{-1}\overline{v}_{in}(s) + G_{ind}\overline{d}(s) \\ \overline{v}_o(s) = G_{vd}(s)\overline{d}(s) + G_{vg}(s)\overline{v}_i(s) \end{cases} \tag{29}$$

The result equals,

$$Z_{inCL}(s) = \left.\frac{\overline{v}_i(s)}{\overline{i}_{in}(s)}\right|_{\overline{i}_{load}(s)=0} = \frac{Z_{in}(s)(1+T_v(s))}{1+T_v(s) - Z_{in}(s)G_{ind}(s)\left(T_{vg}(s)\right)} \tag{30}$$

Where $T_v(s)$ is identical to (27), and $T_{vg}(s)$ equals,

$$T_{vg}(s) = G_c(s)S(s)G_{vg}(s)G_M \tag{31}$$

Similar to the output impedance case, calculating the input impedance requires some of the open-loop transfer functions listed in (18)-(20).

B. Converter with Current Mode Control (CMC)

A general converter with a voltage control loop integrating a peak-current mode modulator is shown in Fig. 7. The operation and schematic of the current modulator shown in Fig. 7 is discussed in detail in [21].
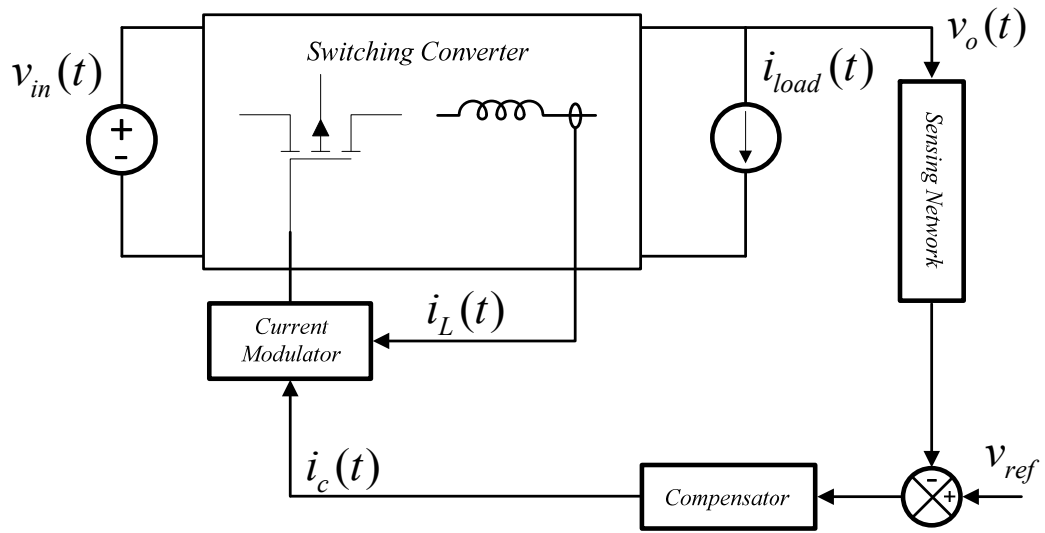
Fig. 7. General converter with a voltage control loop integrating a peak-current mode modulator.

Similar to the previous case, the external voltage loop and the internal current modulator can be modeled by adding a few elements to the model shown in Fig. 4. The resulting model appears in Fig. 8.
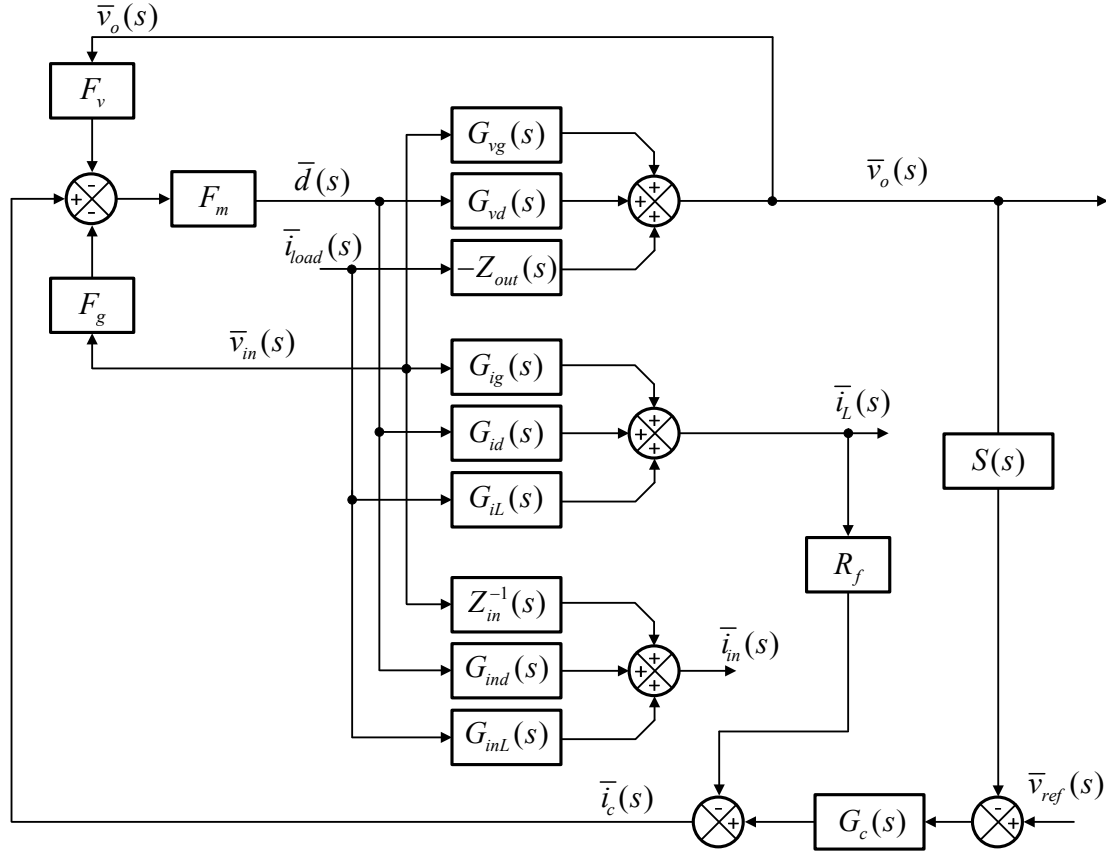
Fig. 8. Closed-loop model of a general power converter operating with an external voltage control loop and an internal current controller.

Similar to Fig. 6, in this figure, $S(s)$ and $G_c(s)$ are the sensing network and external controller transfer functions, respectively. The R_f block represents the current sensing resistor used to transform the inductor current value to a voltage value. The terms F_m, F_v, and F_g are gain values used to model the current modulator. F_m is related to the artificial ramp added to the sensed switch current waveform, which stabilizes the current modulator. This value is independent of the converter topology being controlled and equals [21],

$$F_m = \frac{f_{sw}}{m_a}$$

(32)

Where f_{sw} is the switching frequency, and m_a is the slope of the artificial ramp. The values of F_v and F_g, however, depend on the topology of the converter being controlled by the current modulator. These values for certain types of power converters are listed in TABLE I. For any converters not listed in this table, the values should be calculated following the procedure presented in [21].

TABLE I. GAINS OF CURRENT MODULATOR (f_{sw} IS THE SWITCHING FREQUENCY)

Converter	F_g	F_v
Buck	$\dfrac{d^2}{2f_{sw}L}$	$\dfrac{(1-2d)}{2f_{sw}L}$
Boost	$\dfrac{(2d-1)}{2f_{sw}L}$	$\dfrac{(1-d)^2}{2f_{sw}L}$
Buck-Boost	$\dfrac{d^2}{2f_{sw}L}$	$\dfrac{-(1-d)^2}{2f_{sw}L}$

The closed-loop output impedance of a converter was previously defined in (24). For current mode controlled converters, $Z_{outCL}(s)$ can be calculated by solving the following system of equations derived from Fig. 8 for $\bar{v}_o(s)$ and then dividing the result by $\bar{i}_{load}(s)$,

$$\begin{cases} \overline{d}(s) = F_m\left(-\overline{v}_o(s)S(s)G_c(s) - R_f\overline{i}_L(s) - F_v\overline{v}_o(s)\right) \\ \overline{v}_o(s) = G_{vd}(s)\overline{d}(s) + \left(-Z_{out}(s)\right)\overline{i}_{load}(s) \\ \overline{i}_L(s) = G_{id}(s)\overline{d}(s) + G_{iL}(s)\overline{i}_{load}(s) \end{cases} \tag{33}$$

The result equals,

$$Z_{outCL}(s) = -\frac{\overline{v}_o(s)}{\overline{i}_{load}(s)}\bigg|_{\overline{v}_i(s)=0} = \frac{Z_{out}(s)\left(F_m R_f G_{id}(s) + 1\right) + F_m R_f G_{iL}(s)G_{vd}(s)}{1 + T_i(s)} \tag{34}$$

Where,

$$T_i(s) = F_m F_v G_{vd}(s) + F_m R_f G_{id}(s) + F_m G_c(s)G_{vd}(s)S(s) \tag{35}$$

As noted, calculating the closed-loop output impedance from (34) requires some of the open-loop transfer functions listed in (18)-(20).

The closed-loop input impedance of a converter was previously defined in (28). Again, $Z_{inCL}(s)$ can be calculated by solving a system of equations derived from Fig. 8 for $\overline{v}_i(s)$ and then dividing the result by $\overline{i}_{in}(s)$,

$$\begin{cases} \overline{d}(s) = F_m\left(-\overline{v}_o(s)S(s)G_c(s) - R_f\overline{i}_L(s) - F_v\overline{v}_o(s) - F_g\overline{v}_i(s)\right) \\ \overline{v}_o(s) = G_{vd}(s)\overline{d}(s) + G_{vg}(s)\overline{v}_i(s) \\ \overline{i}_L(s) = G_{id}(s)\overline{d}(s) + G_{ig}(s)\overline{v}_i(s) \\ \overline{i}_{in}(s) = Z_{in}^{-1}(s)\overline{v}_i(s) + G_{ind}(s)\overline{d}(s) \end{cases} \tag{36}$$

The result equals,

$$Z_{inCL}(s) = \frac{\overline{v}_i(s)}{\overline{i}_{in}(s)}\bigg|_{\overline{i}_{load}(s)=0} = \frac{Z_{in}(s)(1 + T_i(s))}{1 + T_i(s) - Z_{in}(s)G_{ind}\left(F_m F_g + T_{ig}(s)\right)} \tag{37}$$

Where $T_i(s)$ is identical to (35), and $T_{ig}(s)$ equals,

$$T_{ig}(s) = F_m F_v G_{vg}(s) + F_m R_f G_{ig}(s) + F_m G_c(s) G_{vg}(s) S(s) \qquad (38)$$

Similar to the previous cases, the open-loop transfer functions in (18)-(20) should be used to calculate the closed-loop input impedance from (37).

IV. EXPERIMENTAL VERIFICATION

To validate the theoretical outcomes, the results of this paper are used to analyze the stability of a prototype cascaded converter system. Based on the Middlebrook theorem, the stability of a cascaded converter system depends on the ratio of the closed-loop output impedance of the upstream converter to the closed-loop input impedance of the downstream converter. Therefore, by investigating the stability of a cascaded converter system and comparing the outcomes with the results predicted from the impedance formulations presented in this paper, the theoretical findings can be confirmed. The schematic of the cascaded converter system is presented in Fig. 9.
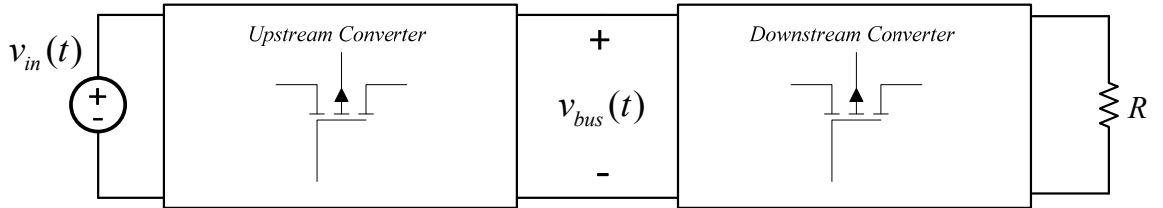
Fig. 9. Schematic of the built prototype cascaded converter system.

In this system, the upstream converter (converter 1) is a buck converter that regulates the dc bus voltage to 400 V. The downstream converter (converter 2) is another buck converter that feeds from the dc bus and regulates its output voltage to 120 V. Both converters are controlled with voltage regulation loops (VMC). A 10 kW prototype system based on the described converter system is built for experimental analysis. Fig. 10 illustrates the built converters.

Fig. 10. The built prototype cascaded converter system.

Additionally, TABLE II lists details of the converter parameters.

TABLE II. PARAMETERS OF THE HARDWARE PROTOTYPE

Converter	Input Voltage [V]	Output Voltage [V]	Processed Power [kW]	Output Capacitance [μF]	Inductance [μH]
Upstream Converter	600	400	10	5.85	18.2
Downstream Converter	400	120	10	65	336

In the first scenario, the controller transfer functions for the two converters are designed independently based solely on their loop gains. In this condition, the closed-loop output impedance of the upstream converter can be found using (26) by substituting the values from Table II,

$$Z_{outCL1}(s) = \frac{1.706 \times 10^5 s^2}{s^3 + 1.067 \times 10^4 s^2 + 1.012 \times 10^{11} s + 7.067 \times 10^{15}} \tag{39}$$

Similarly, the closed-loop input impedance of the downstream converter can be found using (30),

$$Z_{inCL2}(s) = \frac{2.1 \times 10^{-9} s^3 + 2.244 \times 10^{-5} s^2 + 0.1477 s + 440.7}{s^2 + 4955 s - 4.896 \times 10^7} \tag{40}$$

As discussed in [11], the stability of the cascaded converter system can be evaluated using the Nyquist diagram of the minor loop gain,

$$T_m(s) = \frac{Z_{outCL1}(s)}{Z_{inCL2}(s)} \tag{41}$$

The Nyquist diagram of the minor loop gain ($T_m(s)$) is shown in Fig. 11, as are the stability margins.
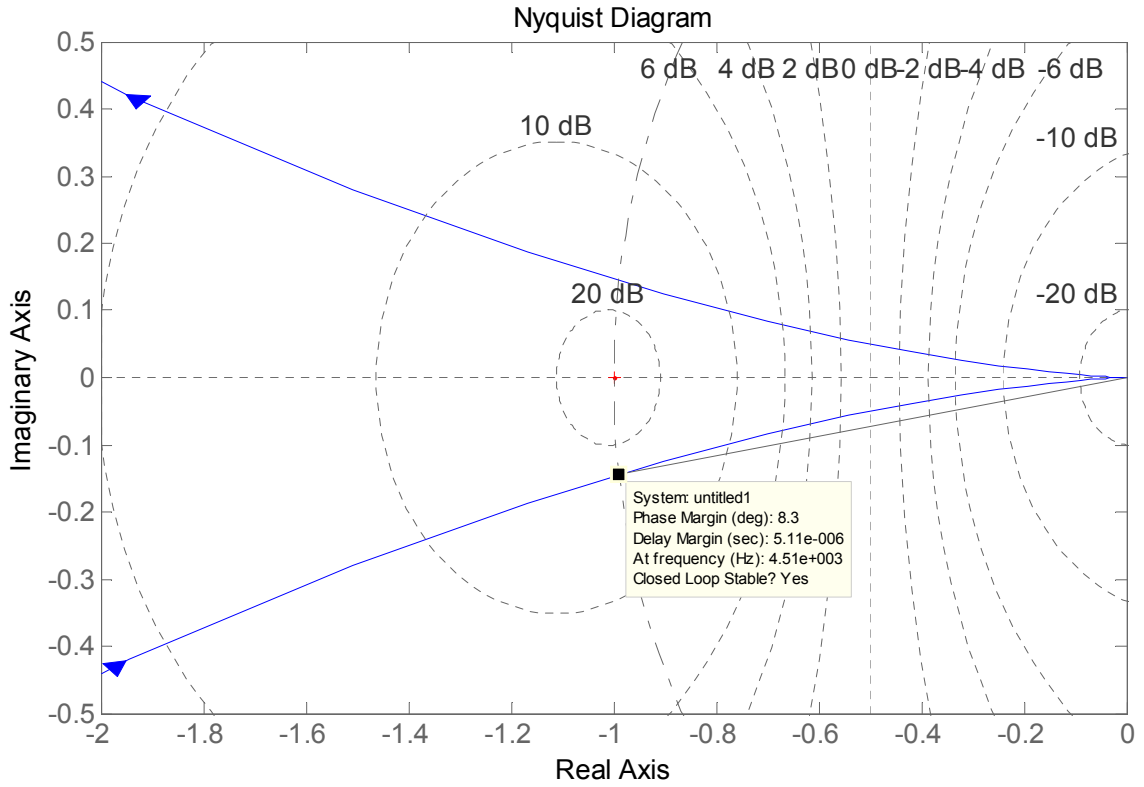
Fig. 11. Nyquist diagram of the minor loop gain of the system for the first test scenario.

Based on Fig. 11, the converter system has only $8.43°$ phase margin under the current operating condition. In order to verify this result using the designed experimental setup, the load of the downstream converter is stepped up by roughly 20% to observe the

response of the dc bus voltage. Fig. 12 shows the resulting waveforms. To visualize the waveforms in more detail, they were transferred from the oscilloscope to MATLAB and plotted using the MATLAB plot function. Fig. 12 confirms that the phase margin of the system is very low, and the dc bus voltage shows a great deal of under-damped oscillations.
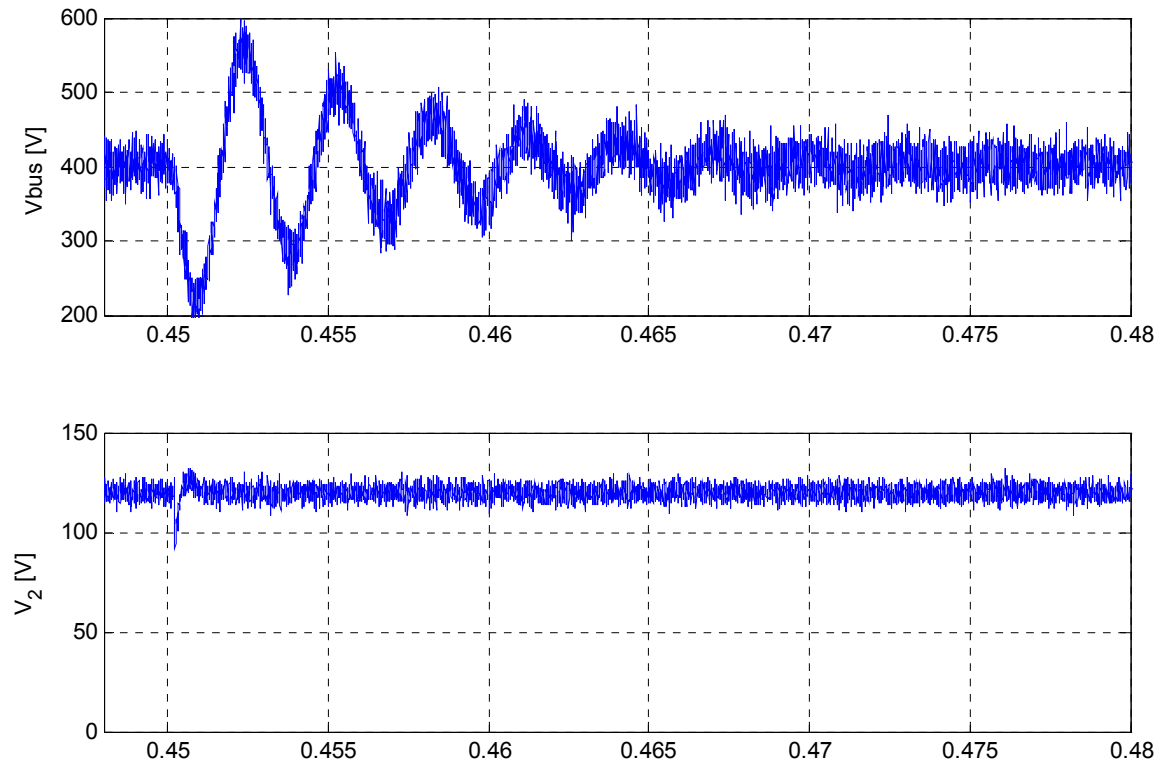
Fig. 12. Response of the dc bus voltage and the downstream converter voltage for a 20% step change in load. System exhibits high oscillations, which indicate a low stability margin.

In the next scenario, the controller transfer functions on the two converters are designed based on the method discussed in [24] to make the system more stable. The Nyquist diagram of the minor loop gain in this condition is shown in Fig. 13. Based on Fig. 13, the phase margin of the system is approximately 55°. To verify this result, an experiment similar to the one previously conducted is performed by stepping up the load of the downstream converter by 20%.
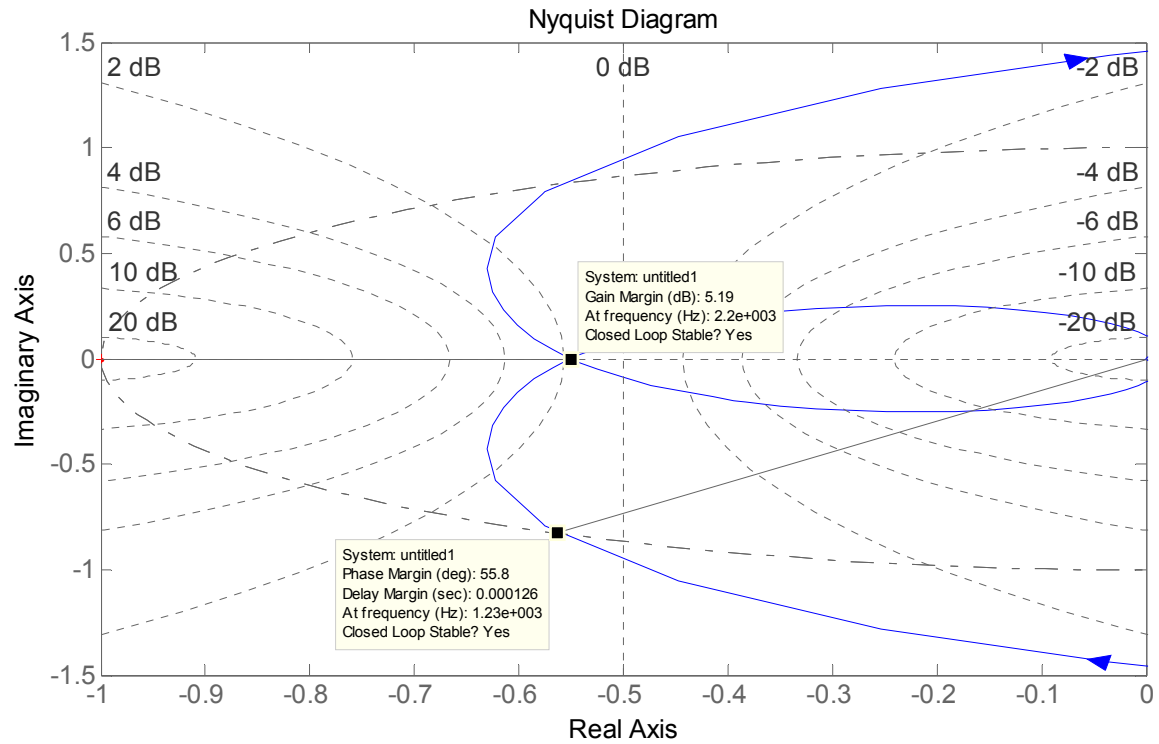
Fig. 13. Nyquist diagram of the minor loop gain of the system for the second test scenario.

Fig. 14 shows the resulting waveforms for this experiment. This figure confirms that the system has sufficient stability margins with the new controllers.
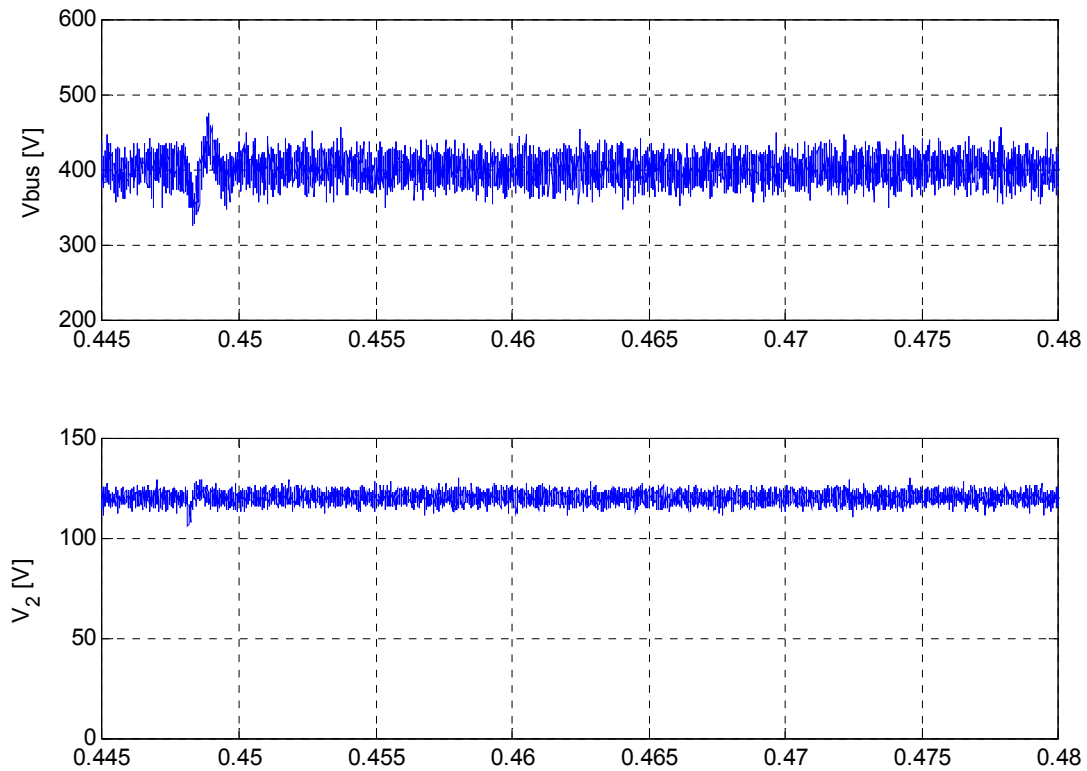
Fig. 14. Response of the dc bus voltage and downstream converter voltage for a 20% step change in load. System exhibits low oscillations, which indicate a high stability margin.

V.   CONCLUSION

This paper presented a simple procedure for modeling a power converter using its open-loop transfer functions. The resulting model was used to derive the closed-loop input and output impedances of the converters operating in voltage mode or current mode. Knowledge of the closed-loop impedances is necessary for stability analysis and controller design in a dc distribution system. The modeling process was described for a converter operating in a dc distribution network rather than in isolation; therefore, the

derived impedances can be used to precisely evaluate Middlebrook's impedance criteria. The theoretical results were verified experimentally.

VI.   APPENDIX

Open-loop transfer functions of the buck, boost, and buck-boost converters considering the parasitic resistances of the inductor and capacitor (r_L, r_c).

TABLE III. TRANSFER FUNCTIONS

OPEN-LOOP TRANSFER FUNCTIONS OF THE BUCK CONVERTER	

$$G_{vg} = RD\frac{(Cr_cs+1)}{Den_1(s)} \qquad G_{vd} = \frac{RV_o}{D}\frac{(Cr_cs+1)Num_1}{Den_1(s)}$$

$$Z_{out} = R\frac{\left(Ls+r_L+\dfrac{2RDr_c}{R+r_c}\right)(Cr_cs+1)}{Den_1(s)} \qquad G_{ig} = D\frac{C(R+r_c)s+1}{Den_1(s)}$$

$$G_{id} = \frac{V_o}{D}\frac{(C(R+r_c)s+1)Num_1}{Den_1(s)} \qquad G_{iL} = R\frac{r_c(1-2D)(C(R+r_c)s+1)+R}{(R+r_c)Den_1(s)}$$

$$Z_{in} = \frac{1}{D^2}\frac{Den_1(s)}{(C(R+r_c)s+1)} \qquad G_{inL} = RD\frac{r_c(1-2D)(C(R+r_c)s+1)+R}{(R+r_c)Den_1(s)}$$

$$G_{ind} = V_o\frac{\left((C(R+r_c)s+1)+\dfrac{Den_1(s)}{R+r_L}\right)Num_1 + Den_1(s)\dfrac{RI_{Load}}{V_o}}{Den_1(s)}$$

$$Den_1(s) = CL(R+r_c)s^2 + \left(L + Cr_L(R+r_c)+CRr_c\right)s + (R+r_L)$$

$$Num_1 = 1 - \frac{2I_{Load}Rr_cD}{V_o(R+r_c)}$$

OPEN-LOOP TRANSFER FUNCTIONS OF THE BOOST CONVERTER

$$G_{vg} = R\frac{(1-D)(Cr_cs+1)}{Den_2(s)}$$

$$Z_{out} = R\frac{(Cr_cs+1)\left(Ls+r_L+\dfrac{RDr_c(1-D)}{R+r_c}\right)}{Den_2(s)}$$

$$G_{ig} = \frac{C(R+r_c)s+1}{Den_2(s)}$$

$$G_{iL} = -R\frac{(1-D)(Cr_cs+1)}{Den_2(s)}$$

$$Z_{in} = \frac{Den_2(s)}{C(R+r_c)s+1}$$

$$G_{inL} = -R\frac{(1-D)(Cr_cs+1)}{Den_2(s)}$$

$$G_{vd} = -RV_o\frac{(1-D)^2(Cr_cs+1)\left(\dfrac{r_L}{R(1-D)^2}-\dfrac{R}{R+r_c}+\dfrac{Ls}{R(1-D)^2}+\dfrac{I_{Load}}{V_o}Num_2(s)\right)}{Den_2(s)\left(1+\dfrac{r_L}{R(1-D)}-\dfrac{Rd}{R+r_c}\right)}$$

$$G_{id} = V_o\frac{(1-D)\left(RCs+\dfrac{Cr_cs+1}{1-D}+\dfrac{R(1-2D)}{(R+r_c)(1-D)}-\dfrac{I_{load}}{V_o(1-D)^2}Num_3(s)\right)}{Den_2(s)\left(1+\dfrac{r_L}{R(1-D)}-\dfrac{RD}{R+r_c}\right)}$$

$$G_{ind} = G_{id}$$

$$Den_2(s) = Den_1(s) - RD(Cr_cs+1) - R^2D\left(\frac{1-D}{R+r_c}\right)$$

$$Num_2(s) = \frac{Ls}{(1-D)^2} + \frac{2r_L}{(1-D)^2} + \frac{Rr_c}{(R+r_c)(1-D)}$$

$$Num_3(s) = r_L\left(C(R+r_c)s+1\right) - \frac{R^2(1-D)^2}{R+r_c}$$

OPEN-LOOP TRANSFER FUNCTIONS OF THE BUCK-BOOST CONVERTER

$$G_{vg} = -RD\frac{(1-D)(Cr_c s+1)}{Den_2(s)}$$

$$Z_{out} = R\frac{\left(Ls+r_L+\dfrac{Rdr_c(1-D)}{R+r_c}\right)(Cr_c s+1)}{Den_2(s)}$$

$$G_{ig} = D\frac{C(R+r_c)s+1}{Den_2(s)}$$

$$G_{iL} = -R\frac{(1-D)(Cr_c s+1)}{Den_2(s)}$$

$$Z_{in} = \frac{1}{D^2}\frac{Den_2(s)}{C(R+r_c)s+1}$$

$$G_{inL} = -RD\frac{(1-D)(Cr_c s+1)}{Den_2(s)}$$

$$G_{vd} = \frac{V_o R(1-D)^2}{D}\frac{(Cr_c s+1)\left(1-\dfrac{LDs}{R(1-D)^2}+r_L\dfrac{1-2D}{(1-D)^2}-\dfrac{I_{load}D}{V_o}Num_2(2)\right)}{Den_2(s)\left(1+\dfrac{r_L}{R(1-D)}-\dfrac{RD}{R+r_c}\right)}$$

$$G_{id} = -\frac{V_o}{DR}\frac{(R+r_L)\left(C(R+r_c)s+1\right)-R^2D\left(Cs+\dfrac{D}{R+r_c}\right)-R\dfrac{I_{load}D}{V_o}Num_3(s)}{Den_2(s)\left(1+\dfrac{r_L}{R(1-D)}-\dfrac{RD}{R+r_c}\right)}$$

$$G_{ind} = -\frac{V_o}{R} \frac{Den_1(s) + \left(C(R+r_c)s+1\right)\left((R+r_L) - RD - \frac{R^2 D}{R+r_c}\right) - R\frac{I_{Load}D}{V_o}Num_4(s)}{Den_2(s)\left(1 + \frac{r_L}{R(1-D)} - \frac{RD}{R+r_c}\right)}$$

$$Num_4(s) = \frac{Den_1(s)}{D} + \frac{r_L}{1-D}\left(C(R+r_c)s+1\right) + R(Cr_c s+1)$$

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II. Dynamic Modeling And Stability Analysis Of Converter-Dominated Dc Microgrids With Instantaneous Constant-Power Loads

Reza Ahmadi, and Mehdi Ferdowsi

ABSTRACT − This paper describes the dynamic modeling and stability analysis procedure for a converter-dominated dc microgrid system. First, the structure of the dc microgrid under analysis is introduced and its various components are studied in detail. Next, the simplified model of the dc microgrid is developed by integrating the dynamic model of all the components. Then, the resulting model is simplified, and the required transfer functions for stability analysis are extracted from it. Afterwards, the stability analysis method using the extracted transfer functions is discussed and the utilization of the method in practice is explored by analyzing the stability of an imaginary dc microgrid system. Finally, stability of a hardware prototype dc microgrid system is analyzed using the provided method and experimental results are reported to confirm the theoretical outcomes.

I. INTRODUCTION

Diminishing fossil energy supplies and environmental obstacles pose increasing challenges to the traditional model of electricity generation and distribution. Harnessing renewable energy sources, such as solar and wind power, is considered one of the ideal means by which to tackle the energy crisis currently looming over the world. However, the spatially distributed and fluctuating nature of renewable energy sources challenges opportunities to integrate these sources into the current ac power grid. The dc

distribution systems or dc microgrids on the other hand are known to be better suited for integration of renewable energy sources into the power grid and are considered to be the key enabling technology for the development of future smart grid.

The main advantage of employing dc distribution systems or dc microgrids is that they are better suited to integrate distributed and renewable energy sources into the power grid because the majority of these new alternative power sources are either inherently dc, such as solar and fuel cells, or, similar to wind power, can be interfaced to a dc system much more easily than an ac system using simple power electronic converter topologies. The other equally important advantage of employing dc microgrids is that most modern electronic loads, such as computers, data centers, and LED lights, as well as adjustable speed drives, require dc voltage. Furthermore, most common energy storage devices, such as batteries in hybrid electric vehicles, are inherently dc devices. Dc microgrids also benefit from better current capabilities of dc power lines, better short circuit protection, and transformer-less conversion of voltage levels, which result in higher efficiency and flexibility, and lower cost of the distribution network.

Dc distribution was one of the main rivals of the current ac distribution in the early years of the growth of electricity distribution systems in the late 1880s. The rivalry instigated the "war of currents" era, with George Westinghouse and Thomas Edison in opposing battle fronts, and eventually led to the adoption of ac distribution systems because of some fundamental demerits of the dc systems at the time, such as inefficient voltage conversion techniques and incompatibility with induction motors, which were the workhorse of the Industrial Revolution. However, nowadays, new highly efficient power electronic technologies have overcome the deficiencies of dc distribution systems and

even have added several advantages to employing dc systems over traditional ac distribution systems in the development of the future smart grid.

While the idea of using a dc microgrid to interface distributed energy sources and modern loads to the power grid seems appealing at first, several issues must be addressed before this idea can be implemented fully. The configuration, stability, protection, economic operation, active management, and control of future dc microgrids are among the topics of interest for many researchers; most of these topics are still considered open problems and require further study.   In [1-12] authors provide several configurations for a future dc distribution system and analyze operational merits of a dc microgrid for integration of distributed generation into the grid. Additionally, possibility of integration of storage devices into the grid for more flexibility is discussed in [4] as well. In [13-15] application of dc microgrids for residential houses and urban settings is explored. Specifically, in [15] characteristics of a dc microgrid for residential houses with cogeneration system in each house is inspected. In [16-28] several analysis methods, including hardware-in-the-loop simulation, reduced order modeling, and large scale modeling are introduced for dc microgrids. Moreover [29-36] address the issue of higher level control and power management of a dc microgrid. Furthermore, in [37] authors propose a solid-state transformer for voltage conversion in zonal dc microgrids and in [38] possibility of integration of dc microgrids into the smart grid is discussed.

The purpose of this work is to investigate the dynamic behavior and stability of a future dc microgrid. Most distributed energy sources and modern loads are connected to the dc microgrid by means of power electronic converters, so future microgrids are expected to be mostly converter-dominated grids. In the majority of applications, the

back-end or point-of-load converters require strict output voltage regulation to satisfy the voltage requirement of the loads. Furthermore, because of their high efficiency, they draw constant power and thus exhibit negative incremental impedance. This causes stability problems for the entire system and is considered a major issue of dc distributed power systems that requires further investigation.

The building blocks, operation, and specifications of the dc microgrid being studied in this paper are introduced in Section II. Section III is devoted to developing a simplified model of the dc microgrid, which is essential to the stability analysis. Section IV explains the procedure for extracting the necessary transfer functions essential to the stability analysis and demonstrates the stability analysis method discussed in this paper by analyzing the stability of an imaginary dc microgrid. Section V introduces a built prototype dc microgrid system used for verification of theoretical outcomes and reports preliminary experimental results featuring usage of the discussed stability analysis method on an actual dc microgrid system. Section VI offers conclusions drawn from this work.

II.   Dc Microgrid

The general configuration of the future dc microgrid is shown in Fig. 1. As pictured, a bidirectional rectifier is used to interface the dc microgrid to the three-phase ac utility grid. The bidirectional rectifier is usually a power factor correction (PFC) device responsible for achieving near-unity power factor with low total harmonic distortion (THD). The line-regulating converter (LRC) shown in Fig. 1 is a bidirectional dc-dc converter that regulates the main dc bus voltage to 400 V. Many researchers believe that a 400 V distribution system will be the future standard for dc distribution

because this voltage level optimizes the tradeoff between adaptability, efficiency, and insulation [39, 40]. This converter is responsible for controlling the dc voltage level on the dc bus and for maintaining the stability of the dc microgrid. This paper focuses primarily on evaluating the stability of the dc microgrid by analyzing the dynamic behavior of the LRC.
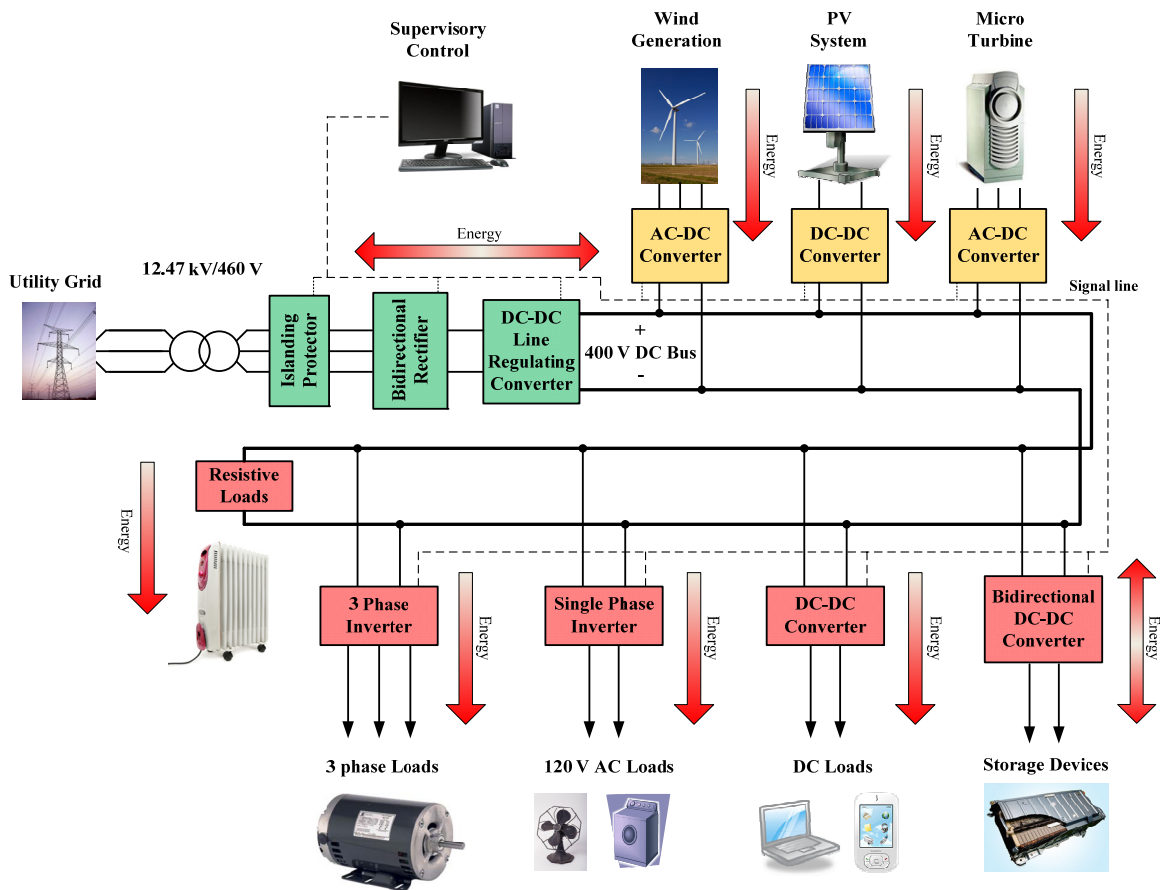
Fig. 1. The general configuration of the future dc microgrid.

Many types of low-power distributed generation units can be integrated into the dc microgrid system to energize the main dc bus. Fig. 1 illustrates the integration of three of the most anticipated future distributed generation systems, wind power generation, solar power generation, and micro turbines, into the dc microgrid. Photovoltaic (PV) systems are almost always dc; as a result, typically a dc-dc converter with maximum power point tracking (MPPT) capabilities is used to connect the PV generation system to the dc microgrid. The wind power generation system and micro turbines usually employ single-phase or three-phase generators to convert mechanical energy to electrical energy; thus, these sources should be connected to the dc bus through ac-dc converters, as shown in Fig. 1.

Modern residences contain a diversity of load types, the most common of which are: 1) Conventional ac loads, including incandescent and florescent lighting, appliances that use motors (refrigerators, washing machines, etc.), and other high-power loads. 2) Modern electronic and dc lighting devices, including cell phone chargers, LED lighting, and computers. 3) High-power motor drive applications that require dc voltage, such as HVAC systems. 4) Resistive loads (most common in electric heating systems). Various kinds of electric loads can be fed from the dc microgrid by introducing point-of-load interfacing converters.

Single-phase inverters can be used to convert the dc bus voltage to ac voltage for grid intertie (e.g., 240 V, 60 Hz, single-phase). Ac motor drives, or more generally, any kind of three-phase load driven by an inverter-based drive system, require dc voltage to operate; as a result, in a dc microgrid system, they can be fed directly from the main 400 V dc bus. Dc-dc converters can be used to achieve dc voltages with different voltage

levels suitable for a range of modern electronic and lighting loads. A low-voltage dc (e.g., 120 V dc) anticipated for use in most future dc devices is an example of a voltage level that can be generated from the main dc bus by employing one or two levels of dc-dc converters [41, 42]. These converters feature high efficiency and strict output voltage regulation; they therefore act as constant power loads (CPL) to the dc microgrid and degrade the stability margins of the overall system. Modeling the effects of CPLs on the LRC is a major part of the dynamic analysis of the dc microgrid in this paper.

Resistive loads, which are anticipated to account for 15-20% of load share in future dc microgrids [43], can be connected to the main dc bus either directly or through a dc-dc converter based on their voltage level requirements. Employing storage devices such as batteries, capacitors, or ultra-capacitors in a dc microgrid system to compensate for the intermittent nature of renewable energy sources and to stabilize the main dc bus voltage is currently an interesting research area in academia. Such storage devices are anticipated to be connected to the main dc bus by means of a bidirectional dc-dc converter, as shown in Fig. 1. An electric or plug-in hybrid electric vehicle charge station is an example of an interface that connects numerous vehicle batteries to the main dc bus.

The dc microgrid shown in Fig. 1 can operate while either connected to the utility power grid or isolated from it. If the amount of power generated by the local power generation units exceeds the power required by the loads, or if there is a power outage in the main utility grid, the dc microgrid can operate in island mode. When isolated, the microgrid can supply electric power to the loads continuously. If the isolation is caused by a power outage in the utility grid and the power consumption exceeds the local power generation, the microgrid can stop supplying power to less critical loads, such as

residential houses, by disabling their interfacing converters in order to supply power to highly critical loads, such as hospitals or data centers. The supervisory controller shown in Fig. 1 is responsible for switching between the isolated and non-isolated modes and for prioritizing the loads to be powered in island mode.

III.   DYNAMIC MODELING OF DC MICROGRID

PFC rectifiers require a large amount of capacitance in their output and are typically designed with a very low bandwidth so that they can filter out the 120 Hz voltage ripple resulting from the rectification of the 60 Hz sinusoidal input voltage. As a result, the bidirectional rectifier illustrated in Fig. 1 exhibits much slower dynamics than those in the rest of the dc microgrid system. Therefore, for the sake of simplicity, the bidirectional rectifier can be modeled with an ideal voltage source with a constant output voltage of 600 V (the 600 VDC level is easily achievable from a 3-phase 480 VAC power system using a rectifier). This voltage source (V_{rec}) is the input voltage of the LRC.

Each energy source shown in Fig. 1 is connected to the dc bus through an interfacing converter. The main objective of these converters is to deliver the maximum possible power to the dc bus regardless of any transients on the dc bus voltage or any fluctuations in the energy provided by each source. For example, typically an MPPT converter interfaces between the PV panel and the dc bus. Ordinarily, a dc-dc converter would be controlled to maintain a fixed output voltage under varying voltage and load conditions; however, in the case of the MPPT converter, the output voltage is dictated by the dc bus voltage, and thus, this converter is controlled to regulate its input voltage in such a way that the maximum possible power always is delivered to the bus. As a result,

the PV system with its interfacing converter acts as a current source that injects instantaneously constant current to the dc bus regardless of the bus voltage.

The same argument holds true for all of the other energy sources shown in Fig. 1, making it possible to model all of them with constant current sources, as shown in Fig. 2. The amount of current being injected to the bus by each source is not constant, but because the rate of change of the current is much slower than the dynamics of the dc bus voltage, these current sources are considered instantaneous constant sources. A similar argument is true for the converters that interface the energy sources, such as batteries to the dc bus. The output voltage of these converters is dictated by the battery voltage itself, and the converter regulates the flow of power to and from the bus using current control. Therefore, these converters can be modeled as constant current sinks as well.
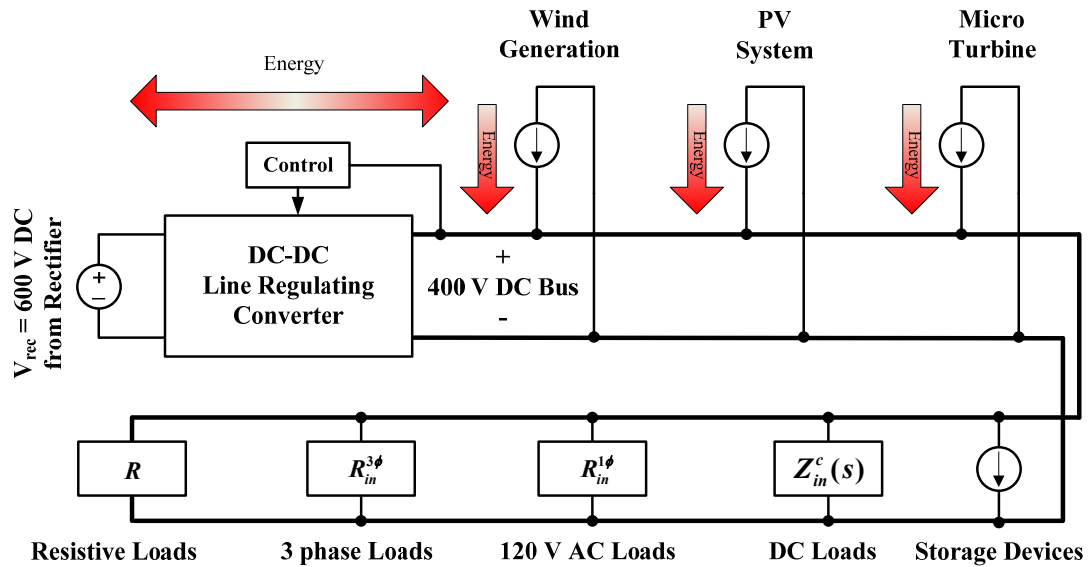
Fig. 2. The dynamic model of the dc microgrid system.

As noted previously, various types of loads can be fed from the main dc bus by employing different converters that generate the suitable type of electric power for each type of load. These tightly regulated, closed-loop converters typically are called CPLs in the literature. In [44], it is shown that the effect of the CPLs on the dynamic behavior of the LRC, and thus the stability of the dc bus voltage, can be evaluated by approximating the CPLs by their closed-loop input impedance. This impedance includes the effect of their tightly regulated control-loop and models the effect of the negative incremental impedance of CPLs on the dc bus. The closed-loop input impedance of several dc-dc converters operating in different modes (voltage mode, current mode, etc.) are derived in [45]. Most dc-ac inverter topologies do not employ energy storage elements (i.e., capacitors, inductors) and thus do not exhibit different dynamic behavior in a range of frequencies; therefore, their closed-loop input impedance usually is considered to be equal to their equivalent input resistance, which in this case is a negative number found from,

$$R_{in} = -\frac{V_b^2}{P_{in}},$$
(1)

where P_{in} is the instantaneous constant input power to the inverter, and V_b is the dc bus voltage. In Fig. 2, the input impedance of the dc-dc converters feeding the dc loads are labeled as $Z_{in}^c(s)$, the equivalent resistance of the single-phase inverters is shown as $R_{in}^{1\phi}$, and the equivalent resistance of the three-phase inverters is shown as $R_{in}^{3\phi}$. Each impedance (or resistance) is the total impedance of all of the similar converters (or inverters) feeding from the bus and is found by calculating the total impedance of all of the parallel input impedances of similar converters.

The LRC is the main component of the dc microgrid to be modeled in detail because the stability of the microgrid depends on the ability of this converter to stabilize the dc bus voltage effectively. The power stage topology to be used for the LRC depends on many factors, such as the power rating, the nominal voltage conversion ratio, the isolation requirement, etc. The topology being studied in this paper is similar to the bidirectional buck (buck in one direction, boost in the opposite direction) converter, as shown in Fig. 3. This converter uses two active switches, S_1, S_2, and two diodes, D_1, D_2, and can transfer power in both directions. In this study, the output voltage of the converter, which is the same as the bus voltage (V_b), is less than the input voltage (equal to the rectifier's output voltage V_{rec}); thus, when this converter transfers power from the grid to the dc bus, it works as the buck converter, and when it transfers power from the dc bus to the grid, it works as the boost converter in the opposite direction.

Fig. 3. The line regulating converter (LRC).

The control circuitry is responsible for regulating the bus voltage and choosing the direction of power flow. The signal "*dir*," which decides the direction of power flow in the converter, is generated based on the ratio of the amount of power being produced by the sources connected to the dc bus, to the amount of power being consumed by the loads. If "*dir*" equals 1, S_2 is always OFF, and the converter works as a buck converter, transferring power from the grid to the dc bus to compensate for the power shortage on the dc bus. If "*dir*" equals 0, S_1 is always OFF, and the converter works as a boost converter, transferring the excess power from the dc bus to the grid. In Fig. 3, resistance *R* depicts all of the resistive loads connected to the bus, and current source i_{load} represents the current being drawn from the converter by all of the non-resistive loads (i.e., converters, inverters).

The differential equations describing the dynamic behavior of this converter and the average input current being drawn from the rectifier can be found using state space averaging methods. A detailed example of applying a state space averaging method to find the average value equations of power converters is given in [46, 47]. In the case of the power converter shown in Fig. 3, the average value equations are

$$\begin{cases} L\dfrac{di_L(t)}{dt} = (-v_b)\big(d_1 + d_{D_2} + d_2 + d_{D_1}\big) + V_{rec}(d_1 + d_{D_1}) \\ C\dfrac{dv_b(t)}{dt} = \Big(i_L - \dfrac{1}{R}v_b - i_{load}\Big)\big(d_1 + d_{D_2} + d_2 + d_{D_1}\big) \\ \qquad\qquad i_{in} = i_L(d_1 + d_{D_1}) \end{cases} \tag{2}$$

where d_1 is the duty cycle of switch S_1, d_2 is the duty cycle of switch S_2, d_{D1} is the duty cycle of diode D_1, and d_{D2} is the duty cycle of diode D_2. The duty cycles of switches and

diodes can be found in terms of the main converter duty cycle (*d*) and the "*dir*" signal using Fig. 3,

$$d_1 = dir \times d$$
$$d_{D_1} = (1 - d_2) \times (1 - dir)$$
$$d_2 = (1 - d) \times (1 - dir) \tag{3}$$
$$d_{D_2} = (1 - d_1) \times dir$$

When the power flows from the grid to the dc bus, "dir" is equal to 1, and (3) becomes

$$d_1 = d$$
$$d_{D_1} = 0$$
$$d_2 = 0 \tag{4}$$
$$d_{D_2} = 1 - d$$

Substituting (4) in (2) yields equations that describe the dynamic behavior of the converter when the power flows from the grid to the dc bus,

$$\begin{cases} L \dfrac{di_L(t)}{dt} = (-v_b) + V_{rec} \times d \\ C \dfrac{dv_b(t)}{dt} = i_L - \dfrac{1}{R} v_b - i_{load} \\ i_{in} = i_L \times d \end{cases} \tag{5}$$

On the other hand, when the power flows from the dc bus to the grid, "dir" is equal to 0, and (3) becomes,

$$d_1 = 0$$
$$d_{D_1} = d$$
$$d_2 = 1 - d$$
$$d_{D_2} = 0$$

(6)

Substituting (6) in (2) yields equations that describe the dynamic behavior of the converter when the power flows from the dc bus to the grid,

$$
\begin{cases}
L\dfrac{di_L(t)}{dt} = (-v_b) + V_{rec} \times d \\
C\dfrac{dv_b(t)}{dt} = i_L - \dfrac{1}{R}v_b - i_{load} \\
\end{cases}
$$
$$i_{in} = i_L \times d$$

(7)

Comparing (5) and (7) demonstrates that the dynamic behavior of the LRC in both power flow directions is the same. The linearized small-signal model of the converter can be found by linearizing the equations in (7) about the nominal operating point using any of the linearization methods, such as the Jacobian matrix or perturbation-linearization methods. A detailed example of linearizing the average value equations of a power converter is given in [44, 48]. The linearized equations describing the dynamic small-signal behavior of the converter around the nominal operating point are found to be

$$
\begin{cases}
L\dfrac{d\hat{i}_L(t)}{dt} = (-\hat{v}_b) + V_{rec} \times \hat{d} \\
C\dfrac{d\hat{v}_b(t)}{dt} = \hat{i}_L - \dfrac{1}{R}\hat{v}_b - \hat{i}_{load} \\
\end{cases},
$$
$$\hat{i}_{in} = D \times \hat{i}_L + I_L \times \hat{d}$$

(8)

where D and I_L are the duty cycle and inductor current values in the nominal operating

point, and $\hat{d}, \hat{v}_b, \hat{i}_L,$ and $\hat{i}_{load}$ are the small-signal values of the duty cycle, bus voltage,

inductor current, and output current, respectively, drawn by the non-resistive loads.
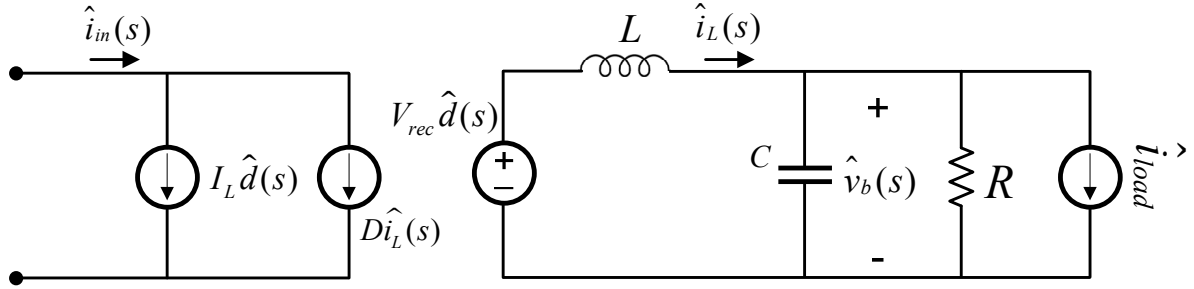
Fig. 4. Small-signal model of the LRC.

The block diagram representation of the circuit appearing in Fig. 4, which is

shown in Fig. 5, can be assembled using the small-signal transfer functions derived from

the circuit in Fig. 4. The circuit in Fig. 4 includes two types of independent sources

$\left(V_{rec}\hat{d}(s), \hat{i}_{load}(s)\right)$ that are responsible for generating the small-signal bus voltage $(\hat{v}_b)$ and

inductor current $(\hat{i}_L)$.
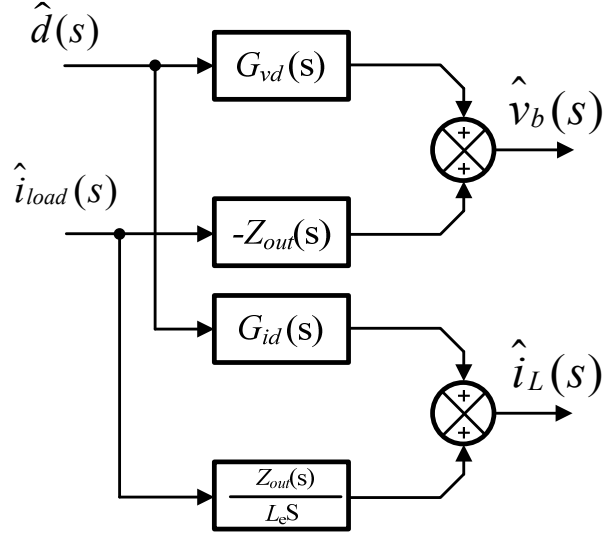
Fig. 5. Block diagram representation of circuit in Fig. 4.

The small-signal transfer functions shown in Fig. 5 relate the independent sources to the bus voltage and inductor current. The small-signal transfer functions for a circuit similar to the one in Fig. 4 are derived in [45] and are listed here,

$$G_{vd}(s) = \frac{\hat{v}_b(s)}{\hat{d}(s)}\bigg|_{\hat{i}_{load}=0} = \frac{V_{rec}}{CLs^2 + \frac{L}{R}s + 1}$$

$$Z_{out}(s) = \frac{\hat{v}_b(s)}{-\hat{i}_{load}(s)}\bigg|_{\hat{d}(s)=0} = \frac{Ls}{CLs^2 + \frac{L}{R}s + 1} \tag{9}$$

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}(s)}\bigg|_{\hat{i}_{load}=0} = \frac{V_{rec}\left(Cs + \frac{1}{R}\right)}{CLs^2 + \frac{L}{R}s + 1}$$

The converter in Fig. 3 uses a voltage regulation loop to control the bus voltage; however, up to this point, the small-signal model of this converter without the voltage

regulation loop was derived. The block diagram representation of the closed-loop converter can be obtained by adding some extra elements to Fig. 5 to model the voltage regulation loop. Details about the voltage regulation loop and the block diagrams used to model it are given in [44]. The block diagram representation of the converter with a voltage mode controller is shown in Fig. 6. In Fig. 6, the blocks that were used to model the small-signal inductor current are eliminated because no information about the small-signal value of the inductor current is needed for the remainder of the analysis.
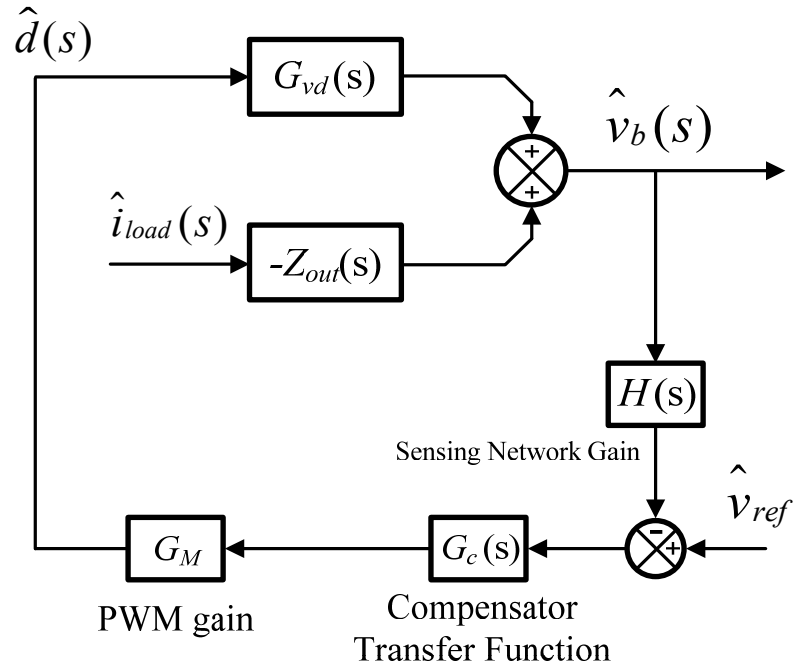
Fig. 6. The block diagram representation of the small-signal model of the LRC with voltage mode controller.

The next step in the dynamic modeling of the microgrid is to combine the LRC, energy source, and converter load models to obtain the complete dynamic model of the

system. Energy sources and their interfacing converters were modeled as constant current sources, so the small-signal value of the current injected by these sources to the bus equals zero; thus, these sources do not need to be incorporated into the small-signal dynamic model of the system. The converter loads, or CPLs, were previously modeled with their input impedance (or equivalent input resistance). The CPLs can be incorporated into the dynamic model of the LRC by considering that the total small-signal current drawn from the dc bus by all loads on the bus can be found from

$$\hat{i}_{load}(s) = \frac{\hat{v}_b(s)}{Z_{iN}(s)}, \tag{10}$$

where $Z_{iN}(s)$ is the total input impedance (or equivalent resistance) of all of the CPLs connected to the bus. Because all of the impedances are connected to the dc bus in parallel, $Z_{iN}(s)$ for the dc microgrid in Fig. 2 can be found from

$$Z_{iN}(s) = \left(\frac{1}{Z_{in}^c(s)} + \frac{1}{R_{in}^{1\phi}(s)} + \frac{1}{R_{in}^{3\phi}(s)} + \frac{1}{R} \right)^{-1} \tag{11}$$

The total input impedance of the loads, $Z_{iN}(s)$, can be incorporated into the block diagram shown in Fig. 6 using (10). Based on (10), the small-signal current drawn by the loads can be found by multiplying the bus voltage into the inverse of the total input impedance of the loads. This can be incorporated into the model in Fig. 6 by connecting the bus voltage to the load current through an inverse $Z_{iN}(s)$ block. The complete dynamic model of the LRC that incorporates the effect of CPLs is shown in Fig. 7. The model in Fig. 7 can be used to evaluate the stability of the dc microgrid under different operating conditions.
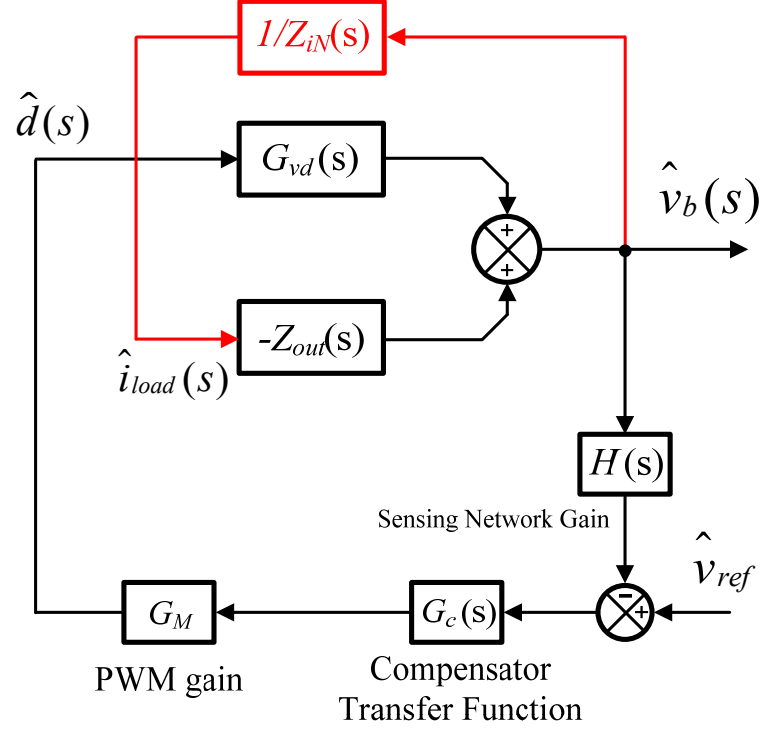
Fig. 7. Complete dynamic model of the LRC incorporating the effect of CPLs.

IV. STABILITY ANALYSIS

The stability analysis can be performed by simplifying the model in Fig. 7 and finding the loop gain of the LRC while it is driving the CPLs. Fig. 7 can be simplified to show the effect of CPLs more clearly. The simplified version of Fig. 7 is shown in Fig. 8, which clearly shows that the CPLs form an internal minor loop in the dynamic model of the system with a gain equal to the ratio of the output impedance of the LRC to the total input impedance of the CPLs.
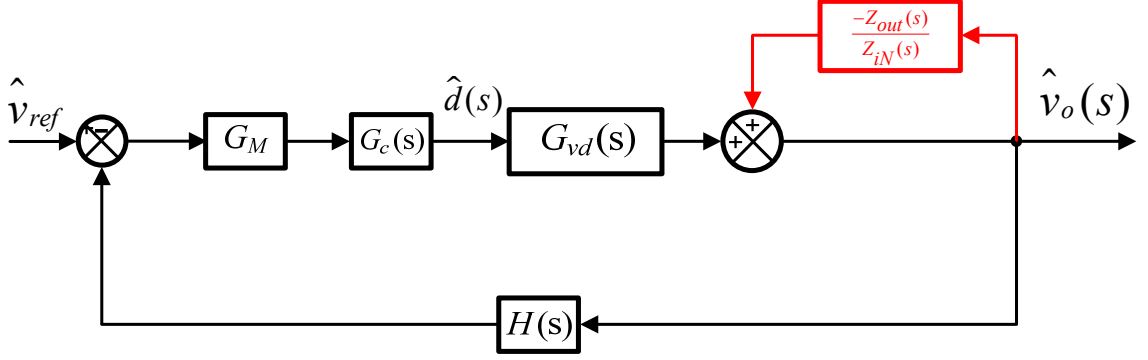
Fig. 8. Simplified version of Fig. 7, which shows the effects of CPLs more clearly.

The model in Fig. 8 can be simplified further using block diagram reduction techniques on the internal minor loop. Fig. 9 shows the dynamic model of the system when the minor loop is reduced to one block. The loop gain of the LRC can be found easily from Fig. 9,

$$T = G_M G_c(s) G_{vd}(s) \left(\frac{1}{1 + \dfrac{Z_{out}(s)}{Z_{iN}(s)}} \right) H(s) \tag{12}$$

This loop gain can be used to evaluate the stability of the LRC in the dc microgrid system. The stability analysis can be performed by employing any classical methods, such as the root locus method, Nyquist diagram, or bode diagram.
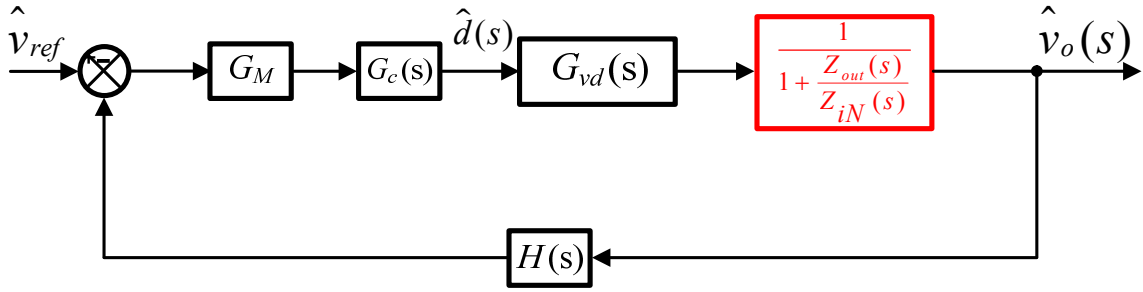
Fig. 9. Simplified version of Fig. 8 using block diagram reduction techniques.

To illustrate the use of (12) to evaluate the stability of a dc microgrid system, a virtual 100 kW dc microgrid similar to the one shown in Fig. 1 is studied. In this system, the LRC regulates the main dc bus voltage to 400 V and balances the power between the utility grid and the dc microgrid. Three types of distributed power sources contribute to the total power available on the dc bus. It is assumed that these sources generate 40 kW power when the stability of the system is being studied. The LRC provides the remaining 60 kW power needed on the bus. Furthermore, it is assumed that the dc-dc converter interfacing the dc loads to the bus, as well as the one-phase inverter, are drawing 20 kW power each, while the three-phase inverter is drawing 30 kW power from the bus. It also is assumed that under these conditions, the storage device is being charged from the bus and consuming 10 kW power, and the resistive loads are consuming 20 kW power.

The LRC being used is similar to the one shown in Fig. 3, and the dc-dc converter interfacing the dc loads is a simple buck converter. Based on the parameters of these converters listed in TABLE I, the input impedance of the dc-dc converter interfacing the dc loads to the bus can be found by using the results obtain in [45].

TABLE I. Parameters of the System

Converter	Input Voltage [V]	Output Voltage [V]	Processed Power [kW]	Output Capacitance [mF]	Inductance [μH]
Line Regulating Converter	600	400	100	0.235	711.1
Dc Load Interfacing Converter	400	120	20	0.130	168.0

Similarly, the equivalent resistance of the inverters can be found using (1) and the power rating of each inverter. The equivalent resistance of all the resistive loads connected to the bus can be found easily with the total power consumed by these loads and the dc bus voltage. After finding the input impedances and equivalent resistances of all the converters and resistive loads, the input impedance of the network can be calculated from (11). The input impedance of the dc microgrid system being studied is found to be,

$$Z_{iN}(s) = \frac{-0.4(s + 714)(s^2 + 9953\,s + 4.227 \times 10^7)}{(s + 4430)(s^2 + 4049\,s + 1.022 \times 10^7)} \tag{13}$$

To evaluate the loop gain of the LRC, it is assumed that G_m and H equal 1, and the plant transfer function $G_{vd}(s)$ is found based on the results of [44],

$$G_{vd}(s) = \frac{600}{1.667 \times 10^{-7}\, s^2 + 8.9 \times 10^{-5}s + 1} \tag{14}$$

The only remaining transfer function needed to find the loop gain of the LRC is the controller (compensator) transfer function $G_c(s)$. In this study, two controller transfer functions are used to calculate the loop gain and evaluate the stability of the dc microgrid system. Then, the results are verified in each case by simulating the system using MATLAB Simulink and comparing the results with the results predicted by analyzing the loop gains. In the first case, the controller transfer function is a simple PI controller,

$$G_c(s) = 12.562 \times 10^{-4} + \frac{2.357}{s} \tag{15}$$

Substituting (13), (14), (15), and the open loop impedance found from [45] into (12) yields the loop gain,

$$T(s)$$
$$= \frac{4.52 \times 10^6(s + 1877)(s + 714)(s^2 + 2667s + 6 \times 10^6)(s^2 + 9953s + 4.22 \times 10^7)}{s(s + 875.5)(s^2 + 2363s + 5.45 \times 10^6)(s^2 + 533.3s + 6 \times 10^6)(s^2 + 9028s + 3.8 \times 10^7)} \tag{16}$$

As noted previously, (16) can be used to evaluate the stability of the LRC. One method of evaluating the stability is to find the closed-loop poles of the system using (16). These poles can be found by solving

$$1 + T(s) = 0 \tag{17}$$

In this case, a pair of complex conjugate poles is found to be in the right half of the plane,

$$S_{1,2} = 225.1 \pm 3383\,i \tag{18}$$

This indicates that the system is unstable. More information can be obtained from the Bode diagram of the loop gain shown in Fig. 10.
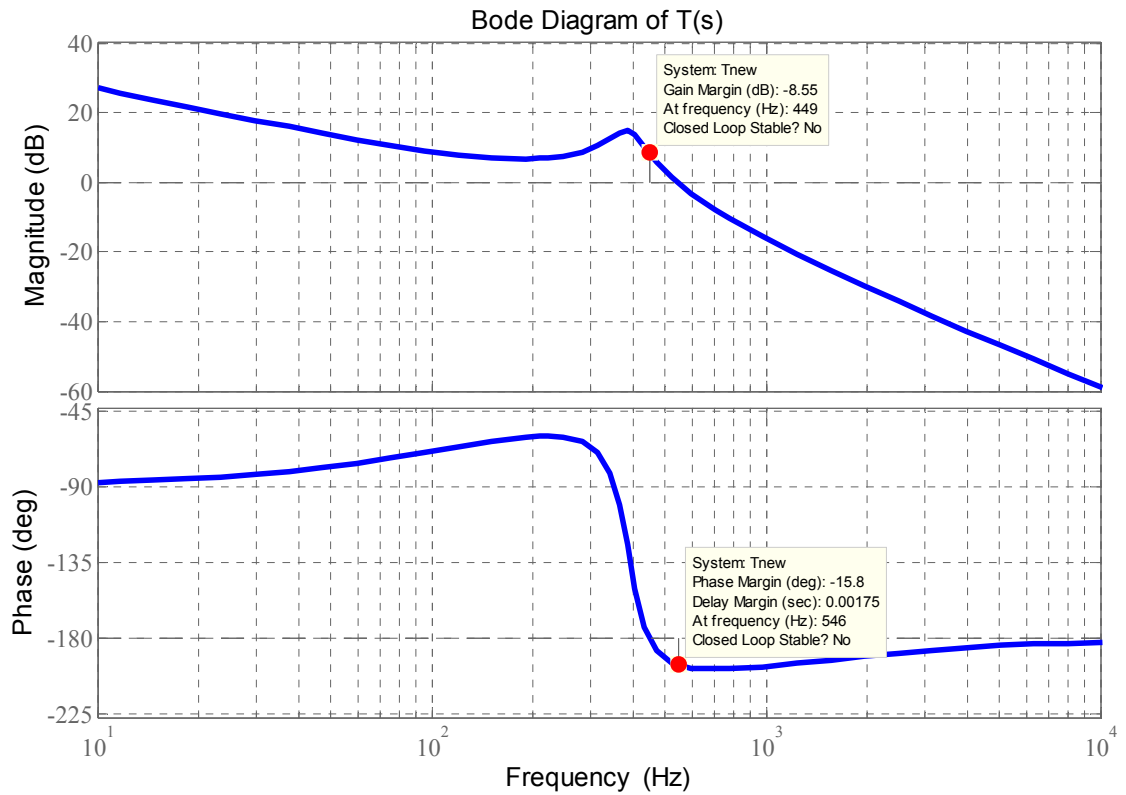
Fig. 10. Bode diagram of the loop gain when (15) is used as the controller transfer for the LRC.

Fig. 10 shows that the phase margin of the system equals $-15.8°$ and the gain margin equals -8.55 dB, which means that the system is unstable. A similar result can be

obtained by analyzing the Nyquist diagram of the loop gain, which appears in Fig. 11.
This figure shows that the Nyquist diagram is encircling the point −1; thus, the system is
unstable.
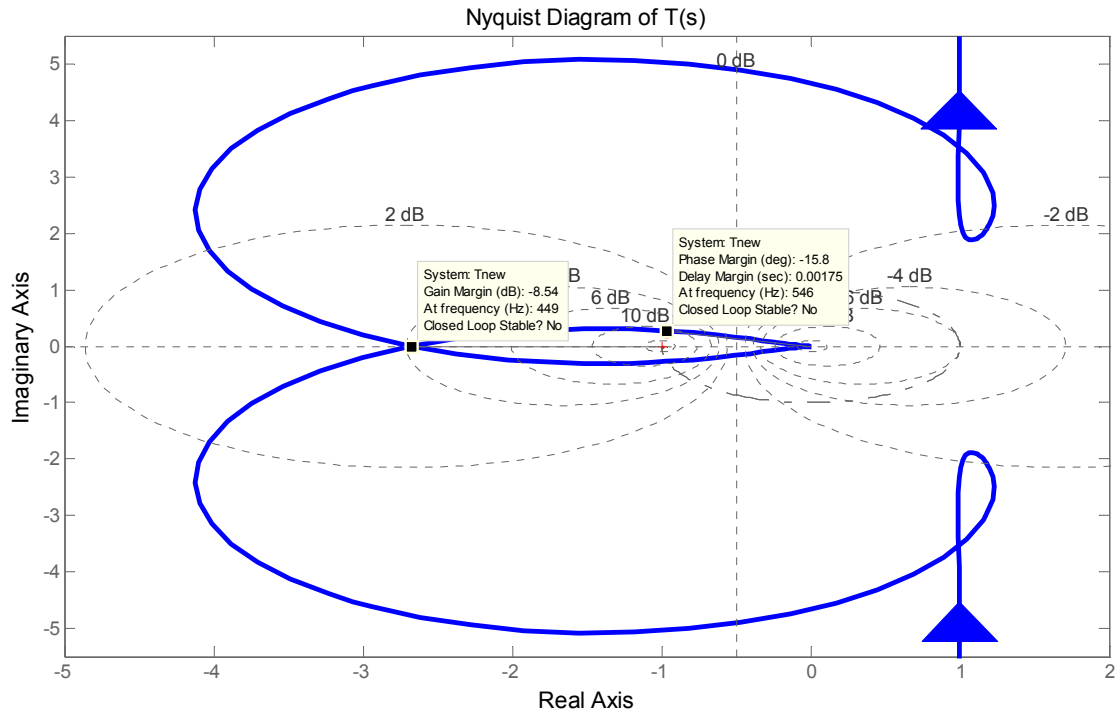
Fig. 11. Nyquist diagram of the loop gain when (15) is used as the controller transfer for the LRC.

The theoretical result of the system's stability obtained by analyzing the loop gain
can be verified by simulating the system using (15) as the controller of the LRC. Fig. 12
shows the dc bus voltage (equivalent to the output voltage of the LRC) and the inductor
current of the LRC. Fig. 12 reveals undamped oscillations of the bus voltage under this
condition and confirms that the system will be unstable.
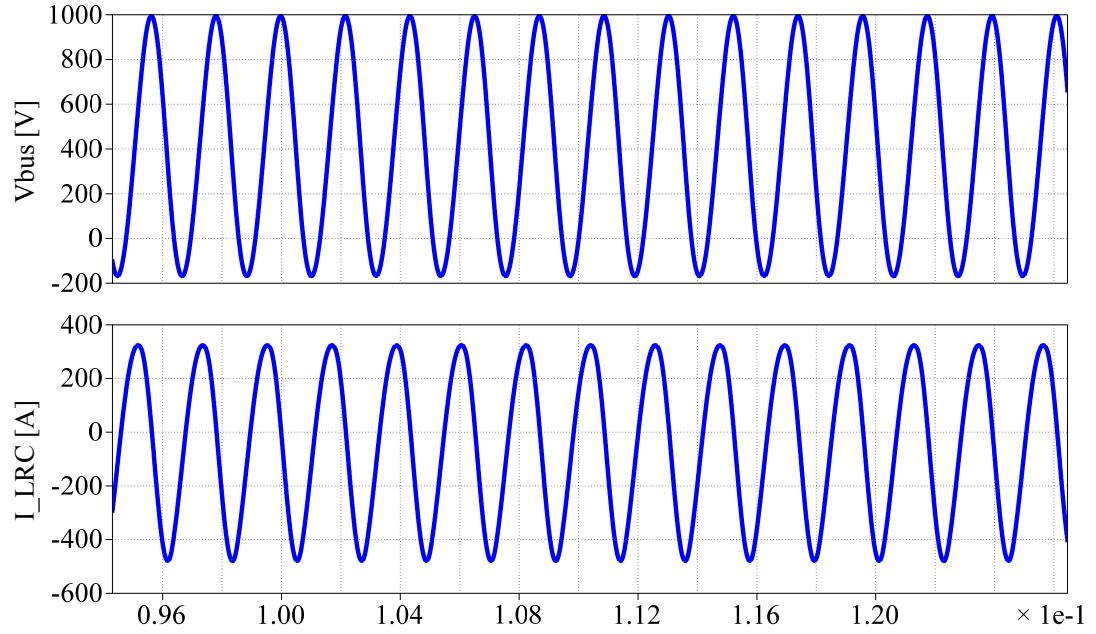
Fig. 12. Bus voltage (output voltage of the LRC) and inductor current of the LRC when (15) is used as the controller transfer function for this converter. The system is unstable in this case.

In the next case, instead of the PI controller in (15), a more complex controller transfer function is used for the LRC,

$$G_c(s) = \frac{7.253 \times 10^{-3}(s + 2456)(s + 1717)}{s(s + 9959)} \tag{19}$$

The loop gain in this case is

$$T(s)$$
$$= \frac{2.61 \times 10^7(s + 2456)(s + 1717)(s + 714)(s^2 + 2667s + 6 \times 10^6)(s^2 + 9953s + 4.22 \times 10^7)}{s(s + 9959)(s + 875.5)(s^2 + 2363s + 5.45 \times 10^6)(s^2 + 533.3s + 6 \times 10^6)(s^2 + 9028s + 3.8 \times 10^7)} \tag{20}$$

Looking at the closed-loop poles of the system by solving (17) for $T(s)$ equal to (20) shows that there are no poles in the right half-plane in the closed-loop system, which

indicates that the LRC is stable in this case. Similar to the previous case, the same result

can be obtained from the Bode diagram of the loop gain shown in Fig. 13.
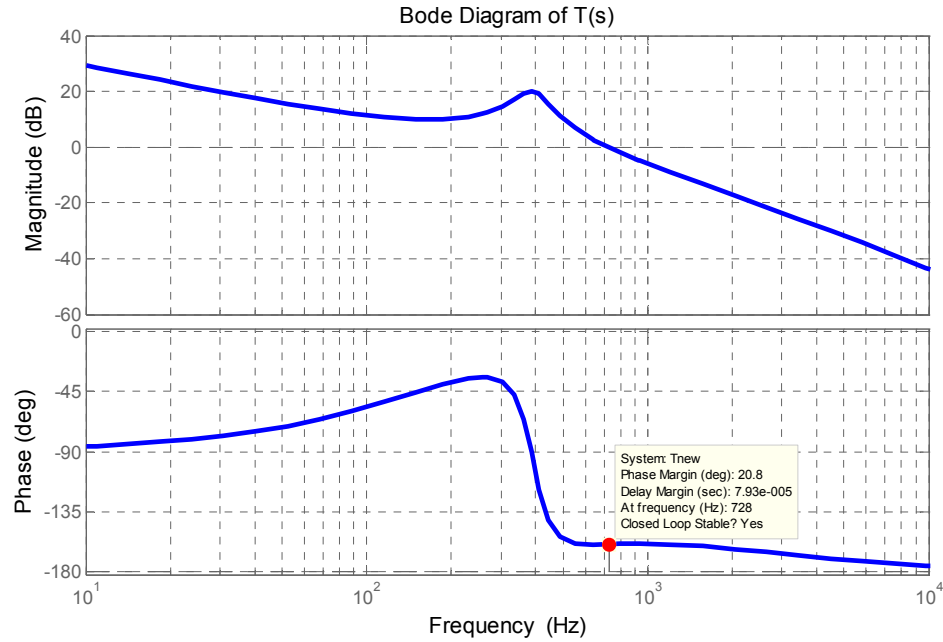
Fig. 13. Bode diagram of the loop gain when (19) is used as the controller transfer for the LRC.

Fig. 13 shows that the system is stable with a phase margin of 20°. Again, the

theoretical result can be verified by simulation, using (19) as the controller of the LRC.

Fig. 14 shows the dc bus voltage, the inductor current of LRC, and the current drawn by

each downstream converter when the load of the converter interfacing the electronic

loads to the dc bus is doubled. Fig. 14 shows that the transition occurs smoothly, and the

system is stable.
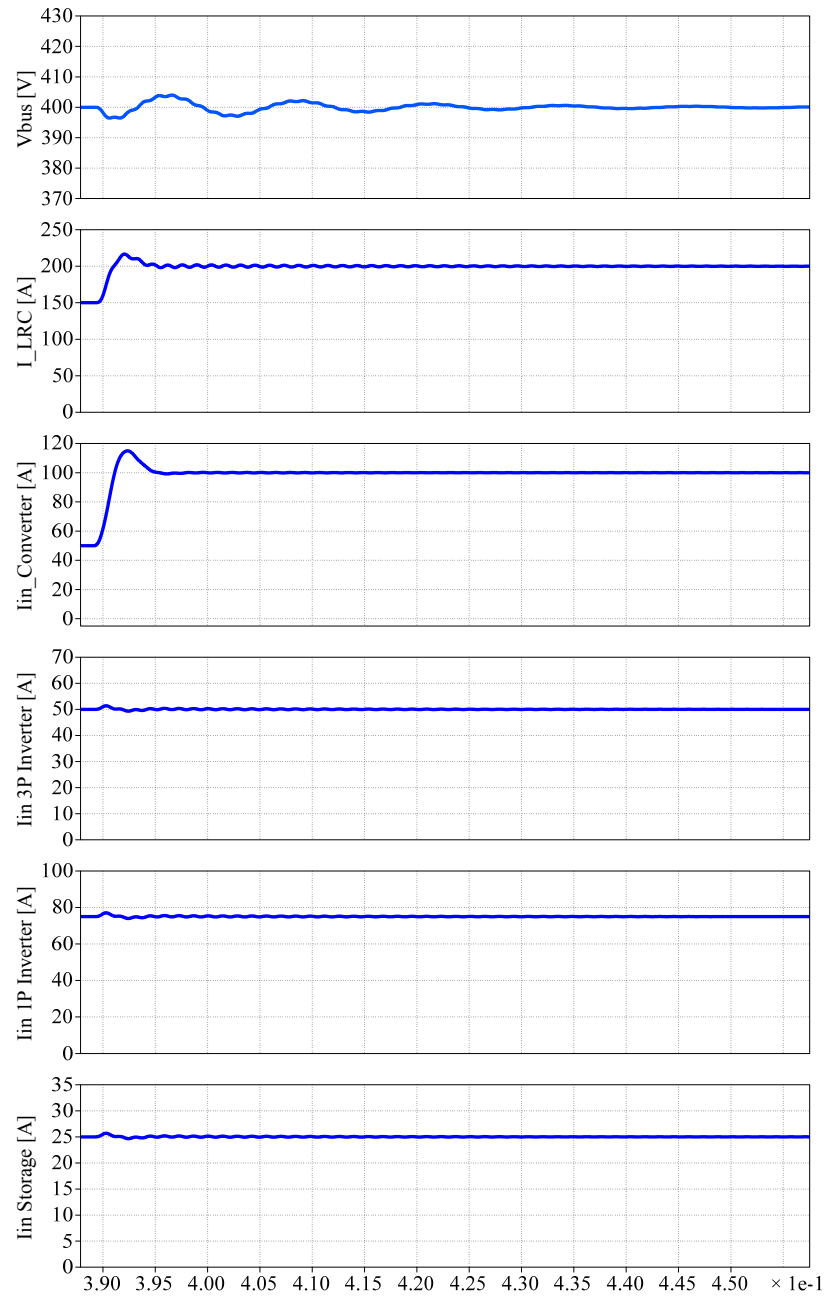
Fig. 14. Bus voltage (output voltage of the LRC), inductor current of the LRC, and current drawn by each downstream converter when (19) is used as the controller transfer function for the LRC and the load of the dc interfacing converter is doubled. The system is stable in this case.

V.   EXPERIMENTAL RESULTS

To verify the theoretical results, a scaled down version of the simulated dc microgrid system presented previously was built and studied in the lab. This prototype dc microgrid system is similar to the dc microgrid shown in Fig. 1 in terms of overall topology, with the exception that it uses only one type of distributed generation unit to energize the main dc bus. The voltage levels of the built system are similar to those in the simulated system; however, the power rating for each component of the system is scaled down to around one-tenth of that of the simulated system because of the power limitations in the lab. As a result, the overall power rating of the built system is approximately 10 kW. The designed LRC uses the same topology as shown in Fig. 3 and the dc-dc converter interfacing the dc loads to the bus is a buck converter. Fig. 15 shows the built LRC and the dc load interfacing converter.

Fig. 15. The built prototype LRC and the dc load interfacing converter.

TABLE II provides the parameters of the two converters.

TABLE II. PARAMETERS OF THE HARDWARE PROTOTYPE

Converter	Input Voltage [V]	Output Voltage [V]	Processed Power [kW]	Output Capacitance [μF]	Inductance [mH]
Line Regulating Converter	600	400	10	585	1.8
Dc Load Interfacing Converter	400	120	1.6	976	2.2

The two converters are controlled via a central digital signal processor (DSP), a Texas Instruments TMS320F28335. The "28335" incorporates a 150 MIPS floating-point DSP core with extensive microcontroller-like peripherals and offers extensive PWM capabilities and a 16-channel analog-to-digital converter (ADC).

The three phase inverter is connected to the main dc bus and drives a Permananet Magnet Synchronous Motor (PMSM). The PMSM is coupled mechanically to a dc motor which generates negative torque and emulates presence of a mechanical load on the shaft. The dc motor is driven by a DCS800 ABB drive while the PMSM drive is a custom made drive designed using a TMS320F28335 DSP and a Semikron SKS 83F B6CI 44 V 12 inverter. The coupled dc motor and PMSM are shown in Fig. 16. The single phase inverter is a conventional H-bridge based inverter which is connected to the dc bus from the input side and feeds a number of 120V, 60 Hz loads connected to its output side.

Fig. 16. The Permanent Magnet Synchronous Machine and the dc machine coupled mechanically on one shaft.

The three-phase inverter is connected to the main dc bus and drives a Permananet Magnet Synchronous Motor (PMSM). The PMSM is coupled mechanically to a dc motor, which generates negative torque and emulates the presence of a mechanical load on the shaft. The dc motor is driven by a DCS800 ABB drive, while the PMSM drive is a custom-made drive designed using a TMS320F28335 DSP and a Semikron SKS 83F B6CI 44 V 12 inverter. Fig. 22 depicts the coupled dc motor and PMSM. The single-phase inverter is a conventional H-bridge-based inverter that is connected to the dc bus from its input side and feeds a number of 120V, 60 Hz loads connected to its output side.

The operation of the distributed generation unit is emulated using another set of coupled electric machines similar to the one shown in Fig. 16. In this set, the dc drive runs the dc motor based on the torque/speed profile of an actual wind turbine; therefore, in practice, the dc motor performs similarly to a real wind turbine from the point of view

of an external observer, such as the Permanent Magnet Synchronous Generator (PMSG), coupled to it. The PMSG is interfaced to the dc bus using an active rectifier system, and transfers the power from the shaft to the bus. Therefore, the coupled dc motor and PMSG with their drive systems successfully emulate operation of an actual wind generation unit.

The stability of the system was studied when the wind generation emulator unit and the LRC were delivering roughly 4 kW and 6 kW of power to the bus, respectively. At this operating point, the dc-dc converter interfacing the dc loads to the bus, single-phase inverter, three-phase inverter, and storage device converter drew roughly 1.5 kW, 3 kW, 4 kW, and 1.5 kW of power from the bus, respectively. The scope shot shown in Fig. 17 shows the main 400 V dc bus voltage, the inductor current of the LRC, the 120 V output voltage of the dc-dc interfacing converter, and the inductor current of this converter at the equilibrium point.
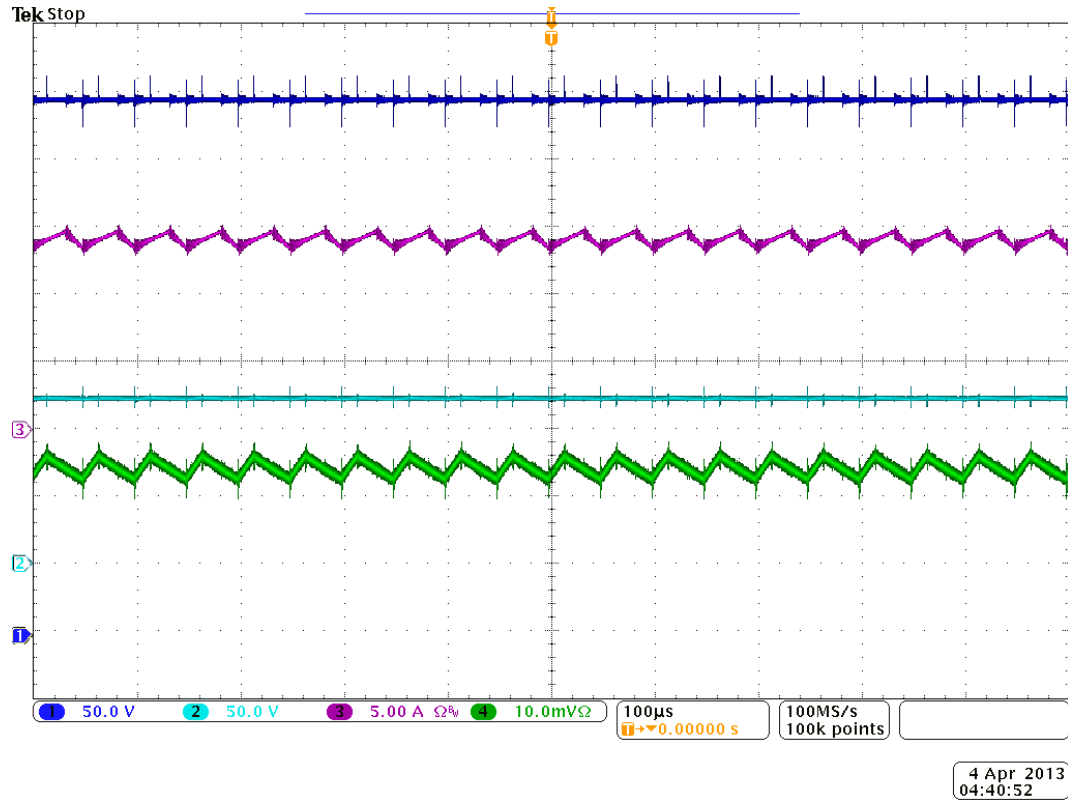
Fig. 17.   Operation of the LRC and the dc load interfacing converter in the equilibrium point. The waveforms from top to bottom are the main 400 V dc bus voltage, the inductor current of the LRC, the 120 V output voltage of the dc-dc interfacing converter, and the inductor current of this converter.

Similar to the simulated system, the stability of the dc microgrid was investigated in two cases by altering the controller transfer function of the LRC. However, to generate the experimental results, the system was not pushed completely to the unstable region because of the safety issues surrounding high-power converters and motor drives. Rather, the stability of the system was compared between the case in which the system had high stability margins and the case in which the system had very low stability margins.

In the case of the first controller, calculating and investigating the loop gain of the system using (12) revealed that the phase margin of the LRC was approximately 7°, which predicted that the LRC should exhibit oscillations in its output voltage in the case of a load or line step change. To verify this result using the experimental system, the load of the dc-dc interfacing converter was stepped up from 1.5 kW to 3 kW to observe the response of the main dc bus voltage. Fig. 18 shows the resulting waveforms. To visualize the waveforms in more detail, they were transferred from the oscilloscope to MATLAB and plotted using the MATLAB plot function. Fig. 18 shows that the waveforms, from top to bottom, are the dc bus voltage, LRC inductor current, output voltage of the dc load interfacing converter, and inductor current of this converter.

Similar results were observed by stepping down the input voltage of the LRC from 600 V to 550 V and recording the transients of the dc bus voltage. The resulting waveforms in this case are shown in Fig. 19. Both Figs. 18 and 19 confirm that when using (21) as the controller transfer function for the LRC, the phase margin of the system was very low, and the dc bus voltage showed oscillations.

In the case of the second controller the phase margin of the LRC was calculated to be approximately55°. Similar to the previous case, in order to verify this result, the response of the dc bus voltage to a step change of the load of the dc-dc interfacing converter and the input voltage of the LRC was observed. Figs. 20 and 21 show the resulting waveforms, respectively. According to these figures, the dc bus voltage in this case showed damped oscillations with low overshoot and undershoot amplitudes, which confirms the theoretical results pertaining to the high phase margin of the LRC.
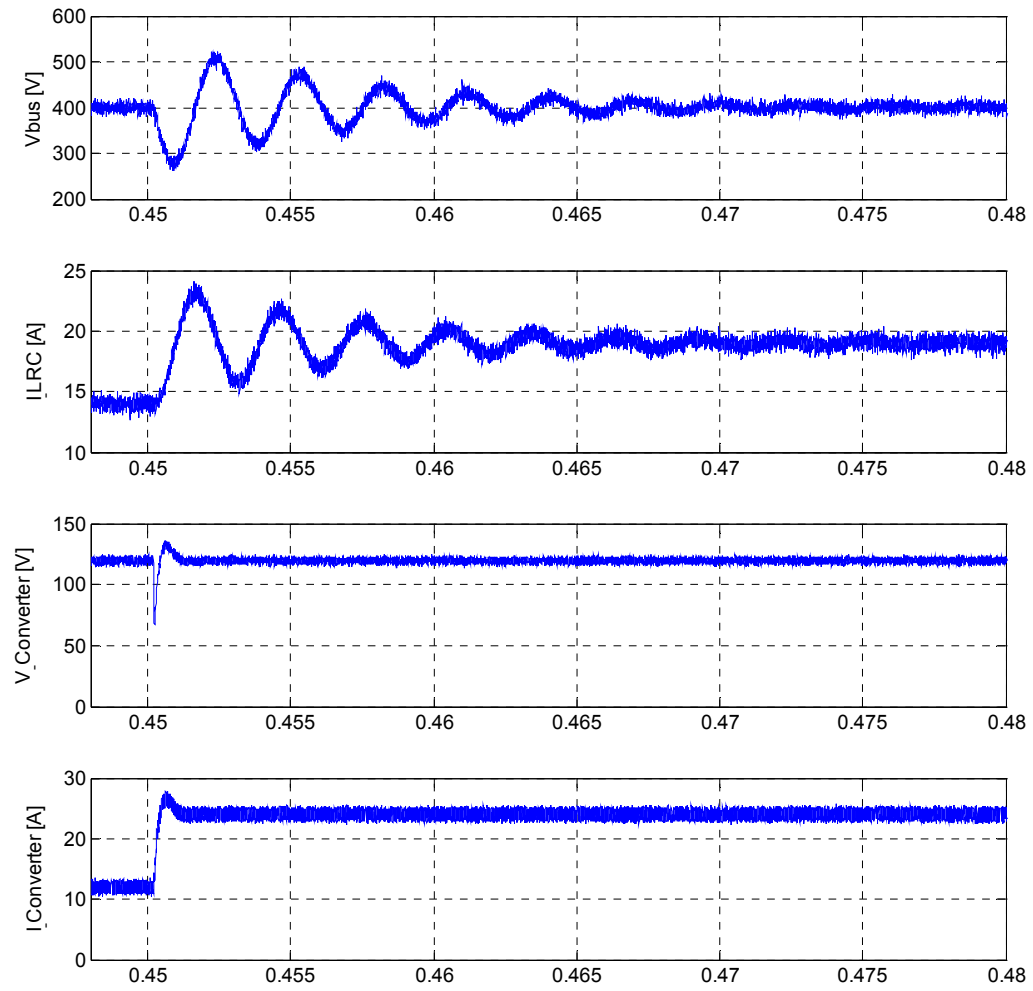
Fig. 18. Response of the dc bus voltage to a step change in the load of the dc-dc interfacing converter when the phase margin of the LRC equals to $7°$.
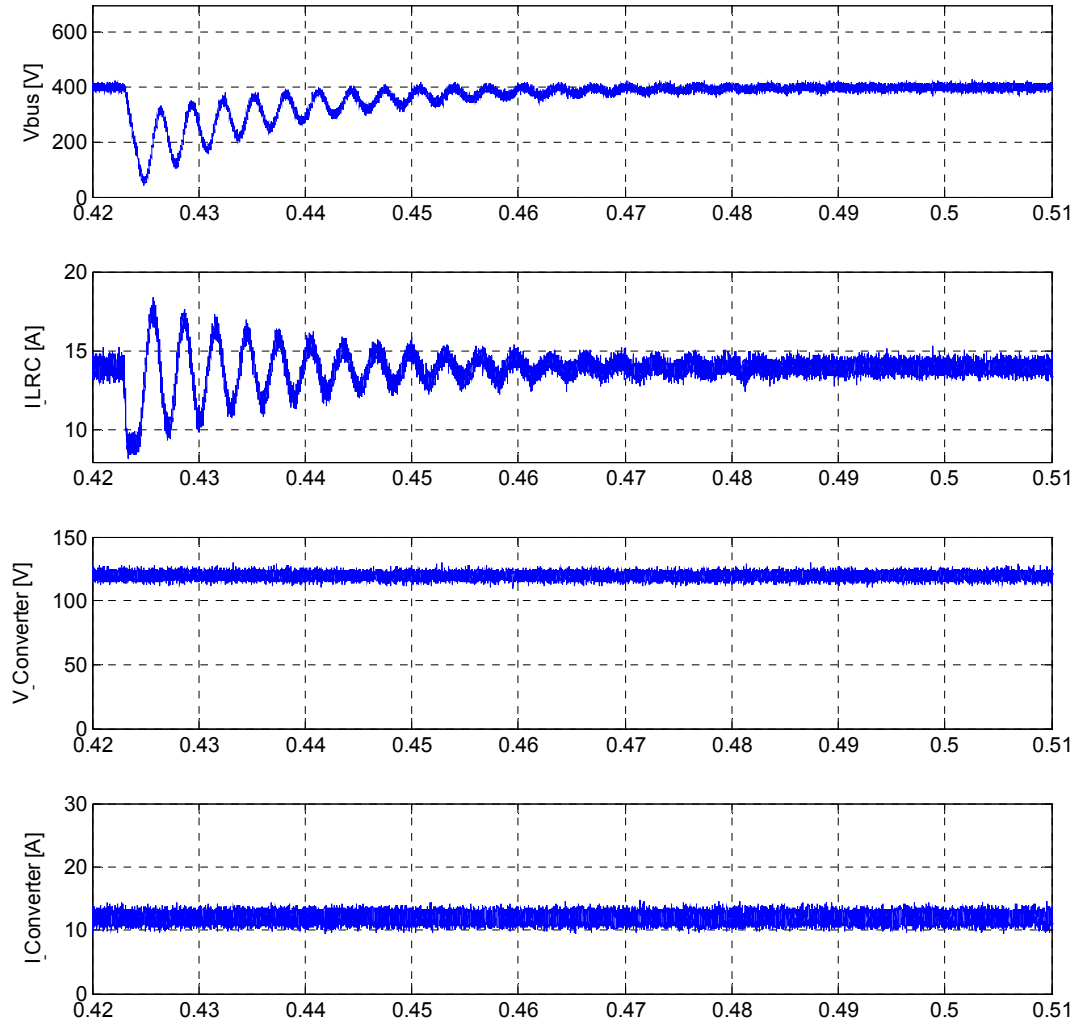
Fig. 19. Response of the dc bus voltage to a step change in the input voltage of the LRC when the phase margin of the LRC equals to 7°.
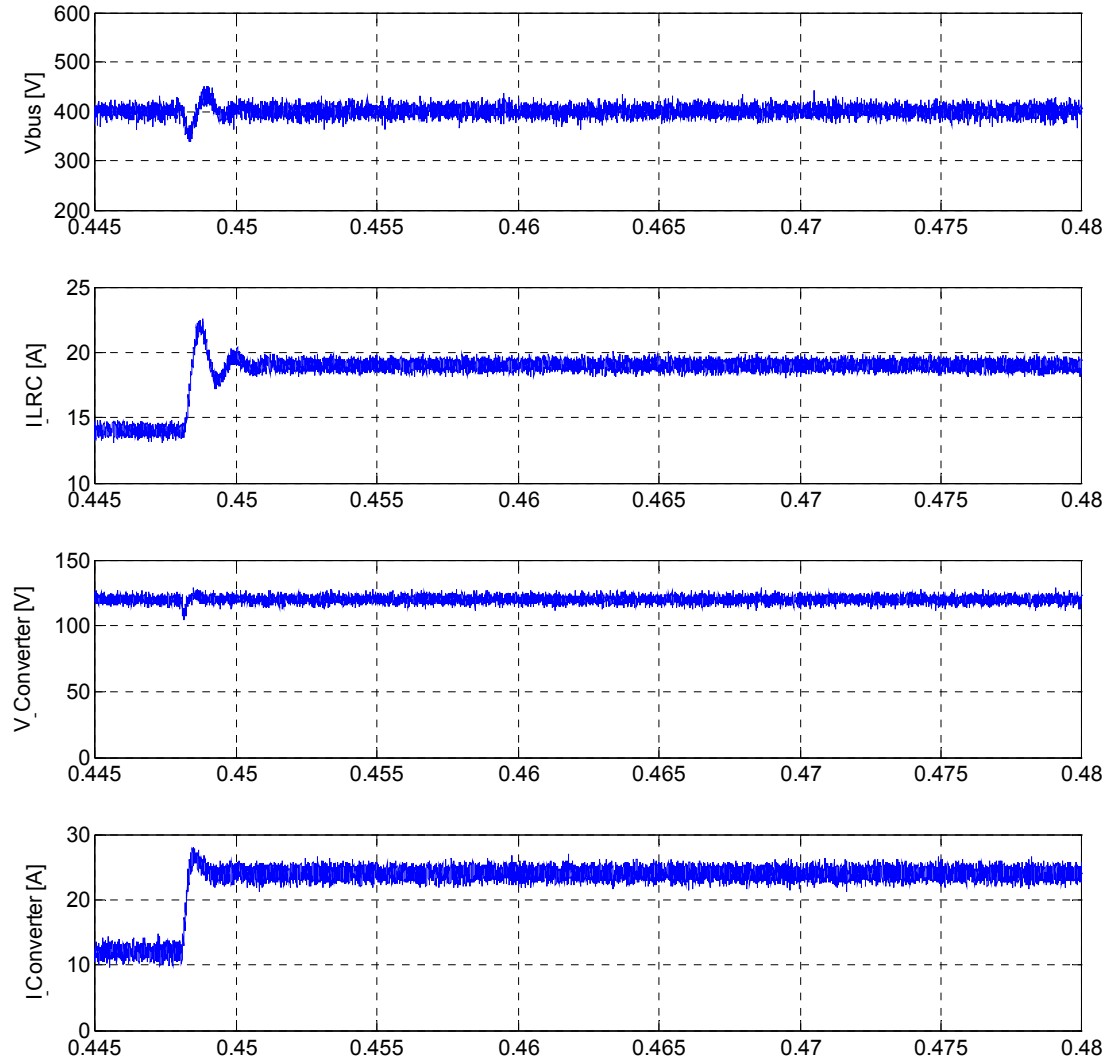
Fig. 20. Response of the dc bus voltage to a step change in the load of the dc-dc interfacing converter when the phase margin of the LRC equals to 55°.
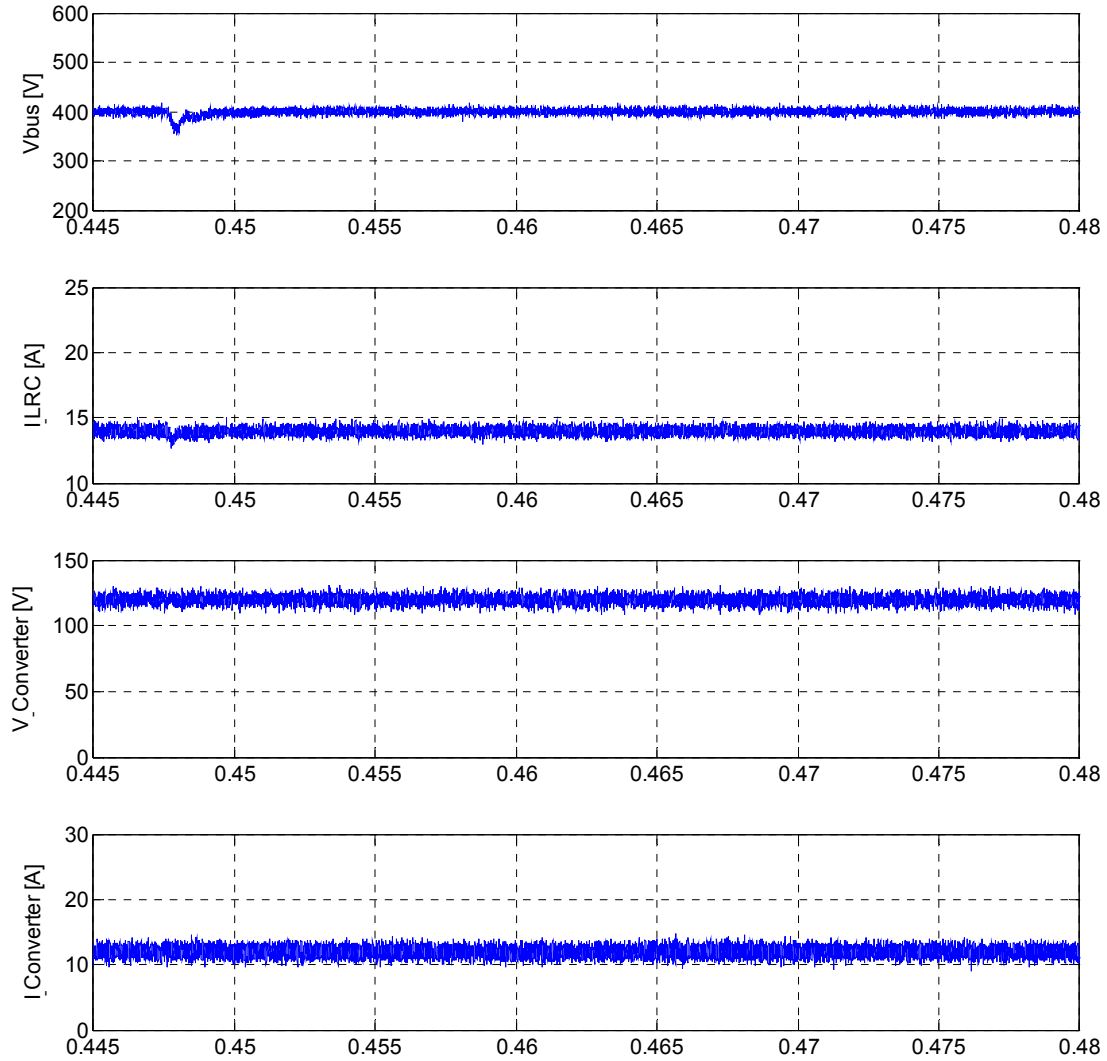
Fig. 21. Response of the dc bus voltage to a step change in the input voltage of the LRC when the phase margin of the LRC equals to 55°.

VI. CONCLUSIONS

The dynamic modeling and stability analysis of a converter-dominated dc microgrid system was explored in this work. First, the structure of one type of dc microgrid was introduced. Next, the dynamic model of all of the components of the microgrid was developed, and the complete dynamic model of the dc microgrid system

was found by combining the models of the components and simplifying the results. Then, the transfer functions used for stability analysis were extracted from the simplifed microgrid model. Afterwards, the model and the transfer functions were used to analyize the stability of a 100 kW dc microgrid system. Finally, usage of the discussed stability analysis method is investigated on a built prototype dc microgrid system.

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III. Performance Improvement Of The Line Regulating Converter In A Converter-Dominated Dc Microgrid System

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ABSTRACT – This paper describes the controller design procedure for a line regulating converter in a converter-dominated dc microgrid system. The purpose of the controller is to mitigate the effects of the constant power loads on the stability and performance of the dc microgrid system. In this work, first, the overall structure, operation and building blocks of the dc microgrid under analysis are introduced. Next, the dynamic model of the dc microgrid and the required transfer functions for the controller design are derived. Then, the two proposed controller design methods are introduced and implemented on an imaginary line regulating converter in a 1 MW dc microgrid system. Finally, the controller design methods are verified experimentally by reporting results from a built prototype dc microgrid system.

I. INTRODUCTION

Today, the resource depletion and environmental issues such as pollution and climate change are amongst the most important obstacles the humankind is facing. Burning the fossil fuels as the main source of energy is considered to contribute both to the resource depletion and the environmental hurdles. Therefore, harnessing the renewable energy sources such as solar and wind energy as a replacement for fossil energy, is in the center of attention of many governments and scholars. However, integration of these sources into the current ac power grid has proven to be a challenging task because of the spatially distributed and fluctuating nature of them. A promising

solution for this issue is the use of dc distribution systems or dc microgrids to integrate the renewable energy sources into the power grid.

The majority of the renewable energy sources are either dc or can be interfaced to dc systems easier than ac systems using simple power electronics. Therefore, the dc microgrids are in advantage over conventional ac systems for utilization of renewable energy sources. On the other hand, most modern residential and commercial loads require dc voltage for operation. The electronic loads such as computers, data centers, LED lights as well as high power applications such as adjustable speed motor drives are examples of the modern loads that require dc voltage. Even the hybrid electric vehicles which are known to be the future means of transportation require dc power because they use batteries for energy storage. The dc microgrids have other advantages over conventional ac systems such as better current capability of dc power lines, better short circuit protection, and transformer-less conversion of voltage levels.

Despite the advantages of using dc microgrids, several issues must be addressed before they can be fully utilized. The stability, protection, active management, economic operation, and control of future dc microgrids are among the topics of interest for many scholars. In [1-11] several dc microgrid configurations are explored and the functional value of employing dc microgrids for harnessing renewable energy sources are discussed. The possibility of enhancing the performance and flexibility of a future dc microgrid by integration of energy storage devices into the grid are studied in [4]. Application of dc microgrids for residential houses and urban environments are deliberated in [12-14]. Several analysis methods suitable for study and design of dc micro grids such as hardware-in-the-loop simulation techniques, reduced order modeling, and large scale

modeling are introduced in [15-27]. Furthermore, the issue of higher level control and power management in a dc microgrid is studied in [28-34]. In [35] a solid-state transformer for the purpose of dc voltage conversion in dc distribution systems is introduced. In [36] authors discuss the integration of the dc microgrids into the future smart grid.

The majority of renewable energy sources and modern loads are interfaced to the dc microgrid by power electronic converters. This makes the future microgrids a mostly converter-dominated grid. In many applications, the point-of-load converters require strict output voltage regulation to satisfy the voltage requirement of the loads, which together with the high efficiency of these converters; makes them draw constant power and hence show negative incremental impedance. The effect of negative impedance causes stability problems for the entire grid and is a major issue for stability of dc microgrid systems.

The methods for addressing the problem with constant power loads (CPLs) in a dc distribution system can be classified into passive damping methods and active stabilization methods. The passive damping methods suggest using passive elements to damp the oscillations on the dc bus to improve the stability of the system. Some of the passive damping methods proposed in the literature are, use of damping resistances, passive filters, storage units, and Ultra-capacitors [37, 38]. Most of the passive damping solutions increase losses, complexity, and the overall cost of the system. The active damping methods on the other hand, usually use more advanced control methods to improve the overall stability of the system. There are a few active damping methods proposed in the literature recently [25, 39-41]. A nonlinear line-regulating compensator,

for instance, is proposed in [39] which works locally to compensate for the CPL effect. However, the complexity of this nonlinear controller makes it less practical. The purpose of this work is to propose methods to design superior linear controllers which perform better in a dc distributed network with presence of CPLs and improve the performance and stability of the system.

The rest of this paper is organized as follows. The overall architecture, specifications, and operation of the dc microgrid studied in this paper are provided in Section II. The dynamic model of the introduced dc microgrid is derived in Section III. Furthermore, the necessary transfer functions for controller design are derived from the dynamic model in this section as well. Section IV explains the two proposed controller design methods by implementing them on an imaginary 1MW dc microgrid system and reporting some simulation results. Section V reports experimental results from a built prototype system for the purpose of verification of theoretical outcomes. Section VI concludes the paper.

II.   OVERALL STRUCTURE OF DC MICROGRID SYSTEM

Fig. 1 illustrates the overall structure of a future dc microgrid system. As visualized, a bidirectional PFC rectifier interfaces the dc microgrid to the ac utility grid. The main dc bus voltage is regulated to 400 V by the line regulating converter (LRC) shown in Fig. 1. This converter controls the dc voltage level on the dc bus and maintains the stability of the dc microgrid. This paper focuses primarily on proposing control design methods for designing the controller transfer function of the LRC in order to improve the stability of the dc microgrid system.
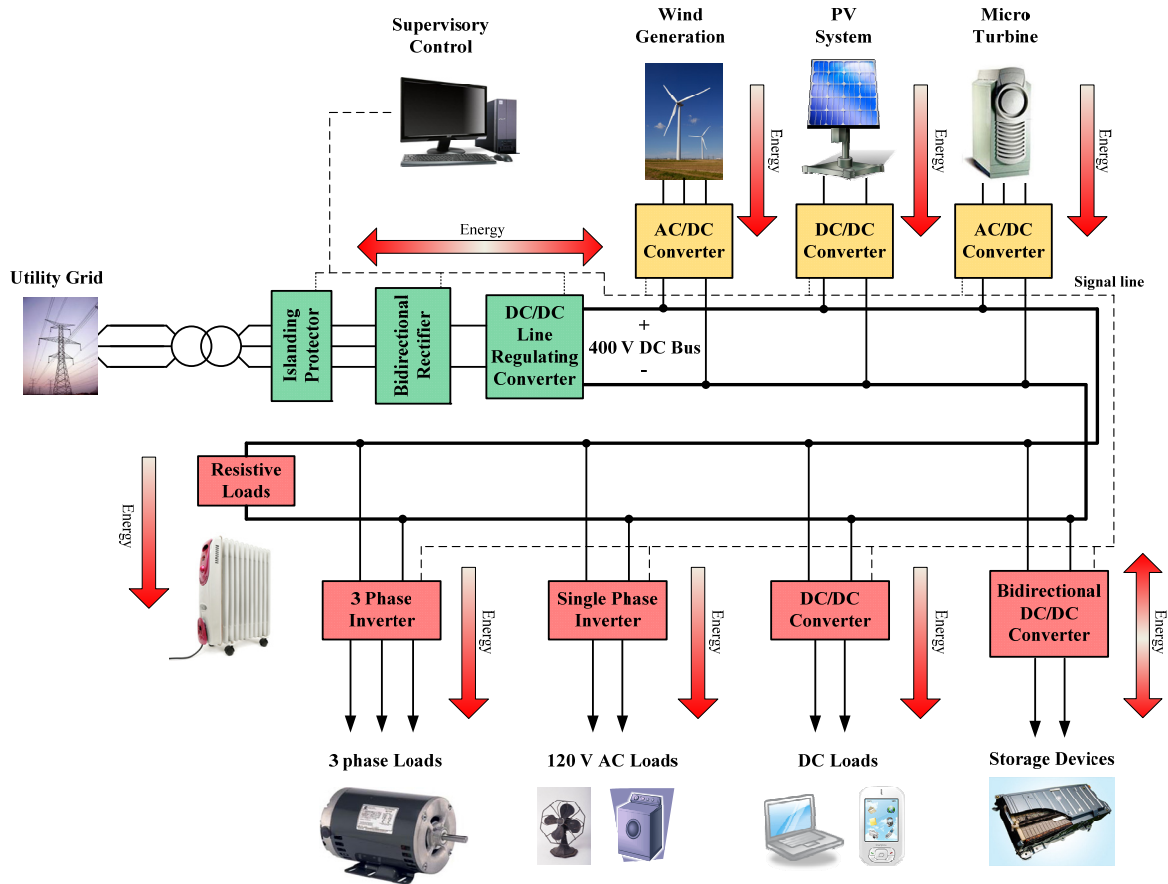
Fig. 1. The overall structure of the future dc microgrid.

Fig. 1 illustrates the integration of wind power, solar power, and micro turbines into the dc microgrid. Photovoltaic (PV) systems are almost always dc and as a result, typically a dc/dc converter is used to connect the PV generation system to the dc microgrid. The wind power generation system and micro turbines usually employ three-phase generators to convert mechanical energy to electrical energy; thus, these sources should be connected to the dc bus through ac/dc converters, as shown in Fig. 1.

Modern residences take advantage of a variety of load types, the most common of which are, conventional ac loads, modern electronic dc loads, adjustable speed drive applications that require dc voltage, and resistive loads (most common in electric heating systems). Various kinds of electric loads can be fed from the dc microgrid by introducing point-of-load interfacing converters. Single-phase inverters can be used to convert the dc bus voltage to ac voltage for grid intertie (e.g., 240 V, 60 Hz, single-phase). Ac motor drives, or more generally, any kind of three-phase load driven by an inverter-based drive system, require dc voltage to operate; as a result, in a dc microgrid system, they can be fed directly from the main 400 V dc bus. Dc/dc converters can be used to achieve dc voltages with different voltage levels suitable for a range of modern electronic and lighting loads. These converters feature high efficiency and strict output voltage regulation; they therefore act as CPLs in the dc microgrid system and degrade the stability margins of the overall system. Resistive loads, which are anticipated to account for 15-20% of load share in future dc microgrids [42], can be connected to the main dc bus either directly or through a dc/dc converter based on their voltage level requirements. Storage devices are anticipated to be connected to the main dc bus by means of a bidirectional dc/dc converter, as shown in Fig. 1. An electric or plug-in hybrid electric vehicle charge station is an example of an interface that connects numerous vehicle batteries to the main dc bus.

III.   DYNAMIC MODEL OF THE DC MICROGRID SYSTEM

The PFC rectifiers normally exhibit much slower dynamics than other converters in the rest of the dc microgrid system. Therefore, to make the modeling process simpler,

the bidirectional rectifier can be modeled with an ideal voltage source of 600 volts (V_{rec}). This voltage source is the input voltage to the LRC.

The energy sources shown in Fig.1 are linked to the dc bus using interfacing converters. These converters deliver the maximum possible power to the dc bus regardless of any bus voltage transients or fluctuations in the energy provided by each source. As a result, it is possible to model all these energy sources along with their interfacing converters with constant current sources, as shown in Fig. 2. The power being injected to the dc bus by each source is not constant in general, but because the rate of change of the amount of power being delivered is a lot slower than the dynamics of the dc bus voltage, these sources are considered instantaneous constant sources. The same idea is true for converters that interface the energy storages such as batteries to the bus. The output voltage of these converters equals the battery voltage and the converter regulates the power flow to and from the bus using current control. Therefore, these converters can be modeled as constant current sinks as well.
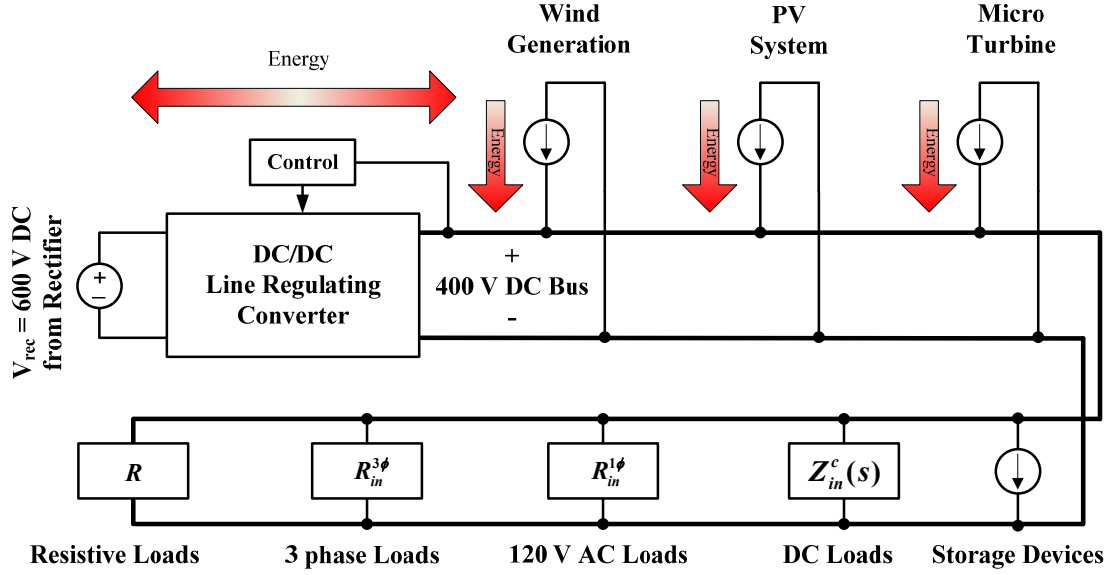
Fig. 2. The dynamic model of the dc microgrid system.

Various types of loads can be energized from the dc bus by the help of different converters that generate the appropriate type of electric power for each kind of load. These closed-loop converters which are normally tightly regulated are called constant-power loads or CPLs in the literature. The effect of the CPLs on the dynamic behavior and thus the stability of the dc bus can be evaluated by approximating the CPLs by their closed-loop input impedance [43]. The closed-loop input impedance of many dc/dc converters are derived in [44]. In case of most dc/ac inverter topologies their closed-loop input impedance usually is considered to be equal to their equivalent input resistance, which in this case is a negative number found from,

$$R_{in} = -\frac{V_b^2}{P_{in}},$$

(1)

In (1) P_{in} is the instantaneous constant input power to the inverter, and V_b is the dc bus voltage. In Fig. 2, the input impedance of the dc load interfacing converters are labeled as $Z_{in}^c(s)$, the equivalent resistance of the single-phase inverters is labeled as $R_{in}^{1\phi}$, and the equivalent resistance of the three-phase inverters is labeled as $R_{in}^{3\phi}$.

The main component of the dc microgrid modeled in detail in this paper is the LRC. The topology used for the LRC depends on many factors, such as the power rating, the voltage conversion ratio, the isolation requirement, etc. The topology studied in this paper is similar to a bidirectional buck-boost (buck in one direction, boost in the opposite direction) converter, as displayed in Fig. 3. This converter uses two active switches and two diodes and can transfer power in both directions. In this study, the output voltage of the converter, which is the same as the bus voltage (V_b), is less than the input voltage, thus, when this converter transfers power from the grid to the dc bus, it works as a buck converter, and when it transfers power from the dc bus to the grid, it works as a boost converter in the opposite direction.

Fig. 3. The line regulating converter (LRC).

The control circuitry is responsible for regulating the bus voltage and choosing the direction of power flow. The signal "*dir*," which decides the direction of power flow in the converter, is generated based on the ratio of the amount of power being produced by the sources connected to the dc bus, to the amount of power being consumed by the loads. If "*dir*" equals 1, S_2 is always OFF, and the converter works as a buck converter, transferring power from the grid to the dc bus to compensate for the power shortage on the dc bus. If "*dir*" equals 0, S_1 is always OFF, and the converter works as a boost converter, transferring the excess power from the dc bus to the grid. In Fig. 3, the resistance R depicts all of the resistive loads connected to the bus, and the current source i_{load} depicts the current being drawn from the converter by all of the non-resistive loads (i.e., converters, inverters).

The linearized equations describing the dynamic small-signal behavior of the converter around the nominal operating point are found to be

$$
\begin{cases}
L\dfrac{d\hat{i}_L(t)}{dt} = (-\hat{v}_b) + V_{rec} \times \hat{d} \\[2mm]
C\dfrac{d\hat{v}_b(t)}{dt} = \hat{i}_L - \dfrac{1}{R}\hat{v}_b - \hat{i}_{load} \\[2mm]
\hat{i}_{in} = D \times \hat{i}_L + I_L \times \hat{d}
\end{cases}
\tag{2}
$$

where D and I_L are the duty cycle and inductor current values in the nominal operating point, and $\hat{d}, \hat{v}_b, \hat{i}_L,$ and $\hat{i}_{load}$ are the small-signal values of the duty cycle, bus voltage, inductor current, and output current drawn by the non-resistive loads, respectively.

The small-signal model of the converter, which is constructed based on (2), is shown in Fig. 4. The block diagram representation of the circuit appearing in Fig. 4, which is shown in Fig. 5, can be assembled using the small-signal transfer functions derived from the circuit in Fig. 4. The circuit in Fig. 4 includes two types of independent sources $\left(V_{rec}\hat{d}(s), \hat{i}_{load}(s)\right)$ that are responsible for generating the small-signal bus voltage $(\hat{v}_b)$ and inductor current $(\hat{i}_L)$.
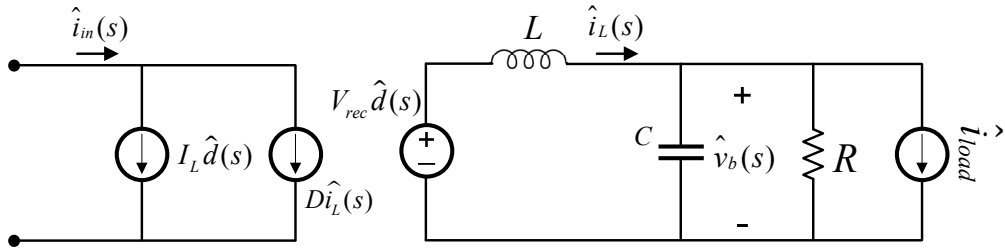
Fig. 4. Small-signal model of the LRC.

The small-signal transfer functions shown in Fig. 5 relate the independent sources to the bus voltage and inductor current. The small-signal transfer functions for a circuit similar to the one in Fig. 4 are derived in [44] and are listed here,

$$G_{vd}(s) = \left.\frac{\hat{v}_b(s)}{\hat{d}(s)}\right|_{\hat{i}_{load}=0} = \frac{V_{rec}}{CLs^2 + \frac{L}{R}s + 1}$$

$$Z_{out}(s) = \left.\frac{\hat{v}_b(s)}{-\hat{i}_{load}(s)}\right|_{\hat{d}(s)=0} = \frac{Ls}{CLs^2 + \frac{L}{R}s + 1} \tag{3}$$

$$G_{id}(s) = \left.\frac{\hat{i}_L}{\hat{d}(s)}\right|_{\hat{i}_{load}=0} = \frac{V_{rec}\left(Cs + \frac{1}{R}\right)}{CLs^2 + \frac{L}{R}s + 1}$$
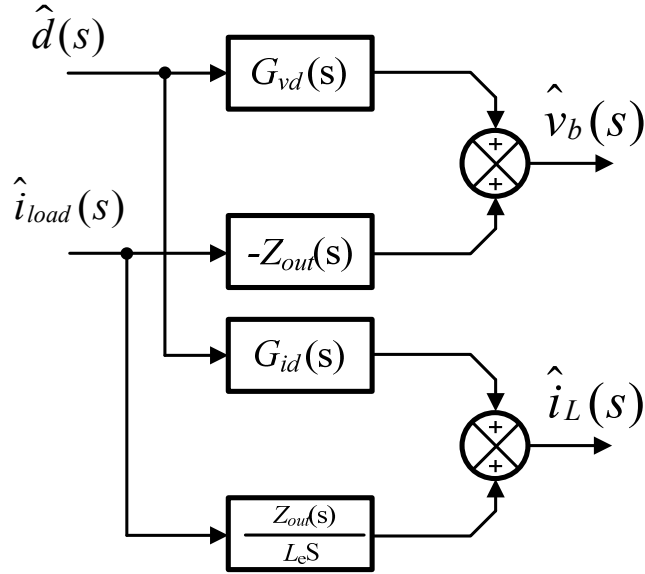
Fig. 5. Block diagram representation of circuit in Fig. 4.

The converter in Fig. 3 uses a voltage regulation loop to control the bus voltage; however, Fig. 5 only shows the block diagram representation of the open-loop converter. The block diagram representation of the closed-loop converter can be obtained by adding some extra elements to Fig. 5 to model the voltage regulation loop. Details about the voltage regulation loop and the block diagrams used to model it are given in [45]. The block diagram representation of the converter with a voltage mode controller is shown in Fig. 6. In Fig. 6, the blocks that were used to model the small-signal inductor current are eliminated because no information about the small-signal value of the inductor current is needed for the remainder of the analysis.
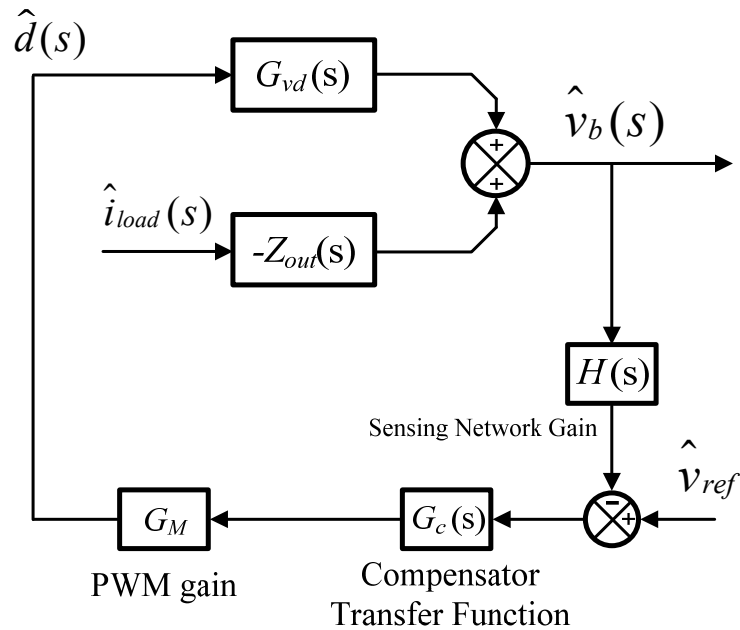
Fig. 6. The block diagram representation of the small-signal model of the LRC with voltage mode controller.

The next step in the dynamic modeling of the microgrid is to combine the models of the LRC, energy sources, and CPLs to obtain the complete dynamic model of the system. Energy sources and their interfacing converters were modeled as constant current sources, thus, these sources do not need to be incorporated into the small-signal dynamic model of the system. The CPLs were previously modeled with their input impedance (or equivalent input resistance). The CPLs can be incorporated into the dynamic model of the LRC by considering that the total small-signal current drawn from the dc bus by all CPLs on the bus can be found from,

$$\hat{i}_{load}(s) = \frac{\hat{v}_b(s)}{Z_{iN}(s)},$$

(4)

where $Z_{iN}(s)$ is the total input impedance (or equivalent resistance) of all of the CPLs connected to the bus. Because all of the impedances are connected to the dc bus in parallel, $Z_{iN}(s)$ for the dc microgrid in Fig. 2 can be found from

$$Z_{iN}(s) = \left(\frac{1}{Z_{in}^c(s)} + \frac{1}{R_{in}^{1\phi}(s)} + \frac{1}{R_{in}^{3\phi}(s)} \right)^{-1}$$

(5)

The total input impedance of the loads, $Z_{iN}(s)$, can be incorporated into the block diagram shown in Fig. 6 using (4). Based on (4), the small-signal current drawn by the loads can be found by multiplying the bus voltage into the inverse of the total input impedance of the loads. This can be incorporated into the model in Fig. 6 by connecting the bus voltage to the load current through an inverse $Z_{iN}(s)$ block. The complete dynamic model of the LRC that incorporates the effect of CPLs is shown in Fig. 7. The model in Fig. 7 can be used for controller design for the LRC.
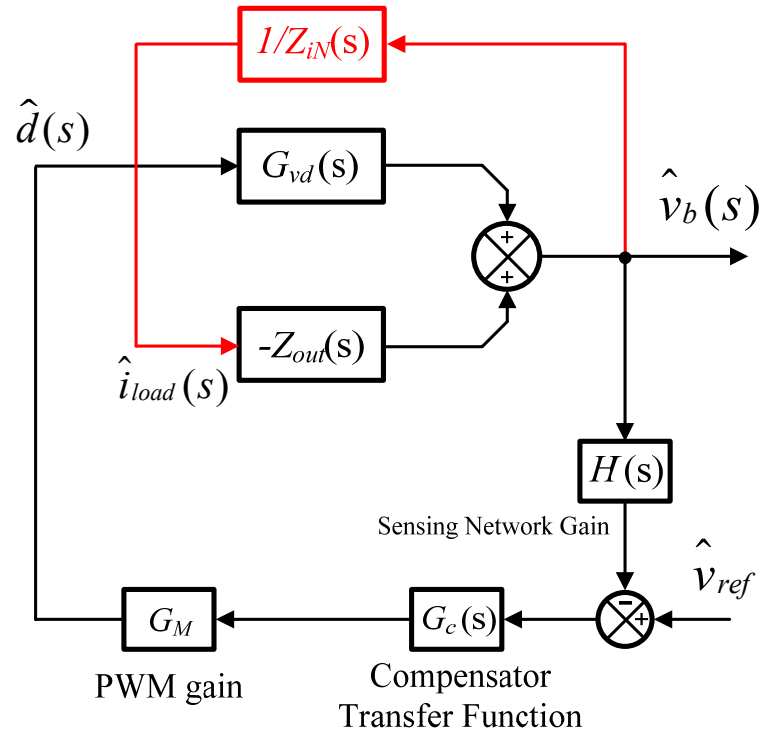
Fig. 7. Complete dynamic model of the LRC incorporating the effect of CPLs.

The controller design methods require the loop gain of the LRC, thus, the model in Fig. 7 is simplified to find the loop gain while LRC is driving the CPLs. The simplified version of Fig. 7 is shown in Fig. 8, which clearly shows that the CPLs form an internal minor loop in the dynamic model of the system with a gain equal to the ratio of the output impedance of the LRC to the total input impedance of the CPLs. The model in Fig. 8 can be simplified further using block diagram reduction techniques on the internal minor loop.
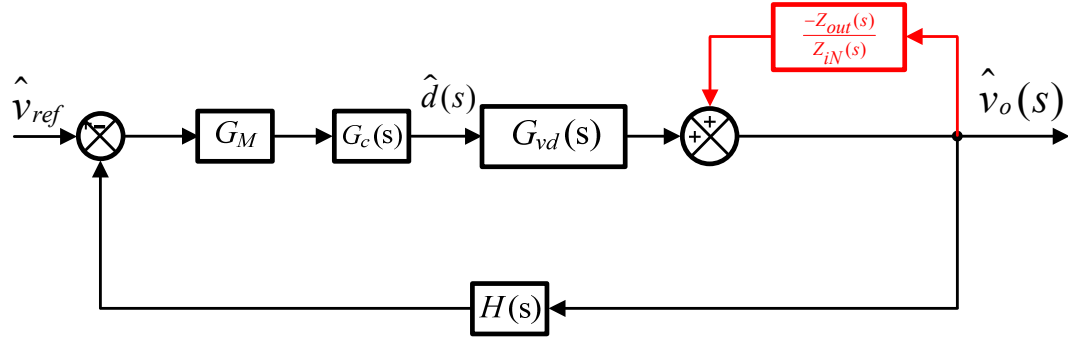
Fig. 8. Simplified version of Fig. 7, which shows the effects of CPLs more clearly.

Fig. 9 shows the dynamic model of the system when the minor loop is reduced to one block. The loop gain of the LRC can be found easily from Fig. 9,

$$T = G_M G_c(s) G_{vd}(s) \left(\frac{1}{1 + \frac{Z_{out}(s)}{Z_{iN}(s)}} \right) H(s) \tag{6}$$
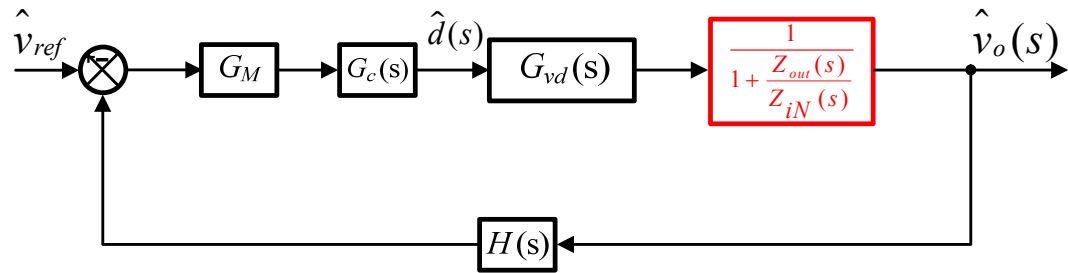
Fig. 9. Simplified version of Fig. 8 using block diagram reduction techniques.

IV.   CONTROLLER DESIGN METHODS

A. The Compensation Transfer Function Method

As previously noted the effect of CPLs reduces the stability margins of the LRC and makes the overall system unstable. The idea of the first control design method is to include some additional terms in the controller transfer function of the LRC $(G_c(s))$ to eliminate the destructive effect of the CPLs completely. In order to find these additional terms, the loop gain of the LRC when it is delivering power to the dc microgrid should be compared with the loop gain when the LRC is delivering the same amount of power to a pure resistive load. In the latter case the loop gain of the LRC can be found from Fig. 4 by eliminating $\hat{i}_{load}(s)$ which is related to the dc microgrid and changing the load resistance from R to R_t. The R_t is the resistance value which draws the same amount of power from LRC that the whole dc microgrid draws from the LRC. The new loop gain in this condition equals to,

$$T_{new} = G_M G_c(s) G_{vd_{new}}(s) H(s) \tag{7}$$

In this case the $G_{vd_{new}}$ can be found from (3) by replacing R with, R_t. Also, the new value of the output impedance $(Z_{out_{new}})$ of the LRC which is required in the rest of analysis can be found similarly in this condition,

$$G_{vd_{new}}(s) = \frac{V_{rec}}{CLs^2 + \dfrac{L}{R_t}s + 1}$$

$$Z_{out_{new}}(s) = \frac{Ls}{CLs^2 + \dfrac{L}{R_t}s + 1}$$

(8)

Comparing (8) and (3) the following relationship can be found between G_{vd} and $G_{vd_{new}}$,

$$G_{vd_{new}}(s) = \frac{R_d}{R_d + Z_{out}}G_{vd}$$

(9)

Where,

$$R_d = \frac{RR_t}{R - R_t}$$

(10)

Substituting G_{vd} from (9) into (6) yields,

$$T = G_M G_c(s) G_{vd_{new}}(s) \frac{R_d + Z_{out}}{R_d}\left(\frac{1}{1 + \dfrac{Z_{out}(s)}{Z_{iN}(s)}}\right)H(s)$$

(11)

This loop gain can be written in terms of T_{new} using (7),

$$T = T_{new}\frac{R_d + Z_{out}}{R_d}\left(\frac{1}{1 + \dfrac{Z_{out}(s)}{Z_{iN}(s)}}\right)$$

(12)

Based on (12) in order to make T the same as T_{new} the effect of the extra element multiplied in T_{new} should be canceled out. This can be done by incorporating a new element into the controller transfer function,

$$G_{c_{new}}(s) = \frac{1 + \dfrac{Z_{out}(s)}{Z_{iN}(s)}}{1 + \dfrac{Z_{out}}{R_d}} G_c(s) \tag{13}$$

As a result the compensation transfer function can be defined as,

$$G_{comp}(s) = \frac{1 + \dfrac{Z_{out}(s)}{Z_{iN}(s)}}{1 + \dfrac{Z_{out}}{R_d}} \tag{14}$$

Therefore, in order to compensate for the effect of the CPLs and improving the stability margins of the LRC, the compensation term in (14) should be multiplied into the controller transfer function of the LRC,

$$G_{c_{new}} = G_{comp}(s) \times G_c(s) \tag{15}$$

To find the compensation term, the R_d can be found from (10) and $Z_{out}(s)$ can be found from (3). To find R_d the R_t should be found from the amount of power the LRC delivers to the dc microgrid in the nominal operating condition,

$$R_t = \frac{V_b^2}{P_{LRC}} \tag{16}$$

B. The Codesign Method

Although the aim of the previous method is to eliminate the effect of the CPLs completely but it comes with a few limiting factors. The major limitation of this method is related to the case where the input impedance of the network $Z_{iN}(s)$ features non-minimum phase behavior. In this case, the $Z_{in}(s)$ has right half plane zeros which will

appear as right half plane poles in the $G_{comp}(s)$ and make it impossible to use (15) to find the controller transfer function. The codesign method discussed in this section however, can be used to improve the performance of the LRC even if the $Z_{in}(s)$ is a non-minimum phase transfer function.

Typically when a dc/dc converter such as the LRC is manufactured the controller transfer function is designed based on the nominal operating point of the converter assuming it is only feeding a pure resistive load. In this case the $G_{vd_{new}}(s)$ in (8) is used as the plant transfer function for the controller design procedure because $G_{vd_{new}}(s)$ includes R_t which indicates the whole power is delivered to a pure resistive load equal to R_t. In practice however, when this converter is used in a dc distribution network such as a dc microgrid similar to Fig. 1, the majority of the output power is delivered to CPLs and only a small percentage of the total power is consumed by pure resistive loads. In this case the controller design procedure followed initially is not valid anymore because the plant that the controller was designed for is altered for the most part. This makes the designed controller transfer function unsuitable for the application and thus reduces the stability margins of the converter and makes the whole system unstable.

The idea of the codesign method is to design the controller transfer function of the LRC based on the specific properties of the dc microgrid instead of only considering the nominal output power. When the LRC is feeding a dc microgrid instead of a pure resistive load, the plant transfer function is no longer the $G_{vd_{new}}(s)$ from (8). In this case the modified plant transfer function can be found from Fig. 9,

$$G_{vd_m} = G_{vd}(s) \times \left(\frac{1}{1 + \dfrac{Z_{out}(s)}{Z_{iN}(s)}} \right) \tag{17}$$

Where $G_{vd}(s)$ and $Z_{out}(s)$ are found from (3). These transfer functions are different from the $G_{vd_{new}}(s)$ and $Z_{out_{new}}(s)$ in (8) because they include R not R_t. As it was noted previously, R shows the resistance of the resistive loads in a dc microgrid that normally consume 15-20% of the total power on the grid, while R_t is the amount of resistance that would consume the nominal output power of the LRC. Knowing the modified plant transfer function $G_{vd_m}(s)$ the controller can be designed for this transfer function using any classical controller design methods.

To illustrate use of the codesign method for improving performance of the LRC in a dc microgrid system, a 1 MW dc microgrid similar to the one shown in Fig. 1 is studied. In this system, the LRC which is similar to the converter shown in Fig. 3 regulates the main dc bus voltage to 400 V and balances the power between the utility grid and the dc microgrid. Three types of distributed power sources contribute to the total power available on the dc bus. It is assumed that these sources generate 400 KW power when performance of the system is being studied. The LRC provides the remaining 600 KW power needed on the bus. Furthermore, it is assumed that the dc/dc converter interfacing the dc loads to the bus (which is a simple buck converter), as well as the one-phase inverter, are drawing 200 KW power each, while the three-phase inverter is drawing 300 KW power from the bus. It also is assumed that under these conditions, the storage device is being charged from the bus consuming 100 KW power while the resistive loads are consuming 200 KW power.

In the first case, the controller transfer function of the LRC is designed assuming it is delivering the nominal 600 KW power to a pure resistive load. In this case, theoretically, a simple PI controller with the following transfer function should be able to stabilize the LRC and yield the desired performance criteria,

$$G_c(s) = 12.562 \times 10^{-4} + \frac{2.357}{s} \qquad (18)$$

However, when the LRC is utilized in the dc microgrid system the performance of the system will be different than what is expected. To evaluate the performance of the LRC when feeding the dc microgrid system, the loop gain of the LRC should be found using (6). Based on the parameters of the converters listed in TABLE I, the input impedance of the dc/dc converter interfacing the dc loads to the bus can be found by using the results obtained in [44].

TABLE I. PARAMETERS OF THE SYSTEM

Converter	Input Voltage [V]	Output Voltage [V]	Processed Power [KW]	Output Capacitance [mF]	Inductance [μH]
Line Regulating Converter	600	400	600	2.35	71.11
Dc Load Interfacing Converter	400	120	200	1.30	16.80

Similarly, the equivalent resistance of the inverters can be found using (1) and the power rating of each inverter. The equivalent resistance of all the resistive loads

connected to the bus can be found easily using the total power consumed by these loads and the dc bus voltage. After finding the input impedances and equivalent resistances of all the converters and resistive loads, the input impedance of the network can be calculated from (5). The input impedance of the dc microgrid system being studied is found to be,

$$Z_{iN}(s) = \frac{-0.4(s + 714)(s^2 + 9953\ s +\ 4.227 \times 10^7)}{(s + 4430)(s^2 + 4049\ s + 1.022 \times 10^7)} \tag{19}$$

To evaluate the loop gain of the LRC, it is assumed that G_m and H equal 1, and the plant transfer function $G_{vd}(s)$ is found from (3),

$$G_{vd}(s) = \frac{600}{1.667 \times 10^{-7}\ s^2 + 8.9 \times 10^{-5}s + 1} \tag{20}$$

Substituting (18), (19), (20), and the open loop output impedance found from (3) into (6) yields the loop gain,

$$
\begin{aligned}
&T(s) \\
&= \frac{4.52 \times 10^6(s + 1877)(s + 714)(s^2 + 2667s + 6 \times 10^6)(s^2 + 9953s + 4.22 \times 10^7)}{s(s + 875.5)(s^2 + 2363s + 5.45 \times 10^6)(s^2 + 533.3s + 6 \times 10^6)(s^2 + 9028s + 3.8 \times 10^7)}
\end{aligned} \tag{21}
$$

The closed loop poles of the system can be found by solving,

$$1 + T(s) = 0 \tag{22}$$

In this case, a pair of complex conjugate poles is found to be in the right half of the S plane,

$$S_{1,2} = 225.1 \pm 3383\, i \tag{23}$$

which indicates that the LRC controlled with (18) will be unstable if used to feed the dc microgrid. The same result can be obtained from the Bode diagram of the loop gain shown in Fig. 10.
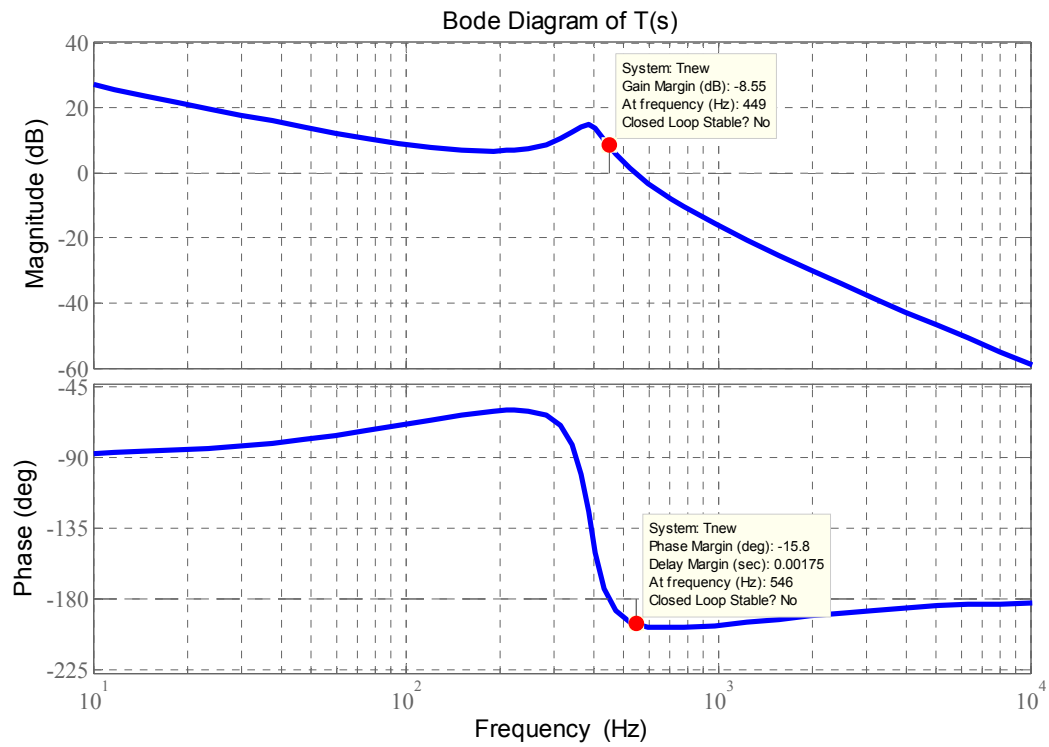
Fig. 10. Bode diagram of the loop gain when (18) is used as the controller transfer for the LRC.

In the next case instead of assuming pure resistive load for the LRC, the controller is designed for the modified plant transfer function in (17). The following controller

transfer function designed using the root locus method proves to stabilize the LRC and yield the target performance criteria,

$$G_c(s) = \frac{7.253 \times 10^{-3}(s + 2456)(s + 1717)}{s(s + 9959)} \tag{24}$$

In this case, the loop gain is found to be,

$$
\begin{aligned}
&T(s) \\
&= \frac{2.61 \times 10^7(s + 2456)(s + 1717)(s + 714)(s^2 + 2667s + 6 \times 10^6)(s^2 + 9953s + 4.22 \times 10^7)}{s(s + 9959)(s + 875.5)(s^2 + 2363s + 5.45 \times 10^6)(s^2 + 533.3s + 6 \times 10^6)(s^2 + 9028s + 3.8 \times 10^7)}
\end{aligned} \tag{25}
$$

Looking at the closed-loop poles of the system by solving (22) for $T(s)$ equal to (25) shows that there are no poles in the right half plane in the closed-loop system, which indicates that the LRC is stable in this case. Similar to the previous case, the same result can be obtained from the Bode diagram of the loop gain shown in Fig. 11. As a result, by designing the controller for the modified plant transfer function the performance of the LRC and thus the dc microgrid system could be enhanced greatly.
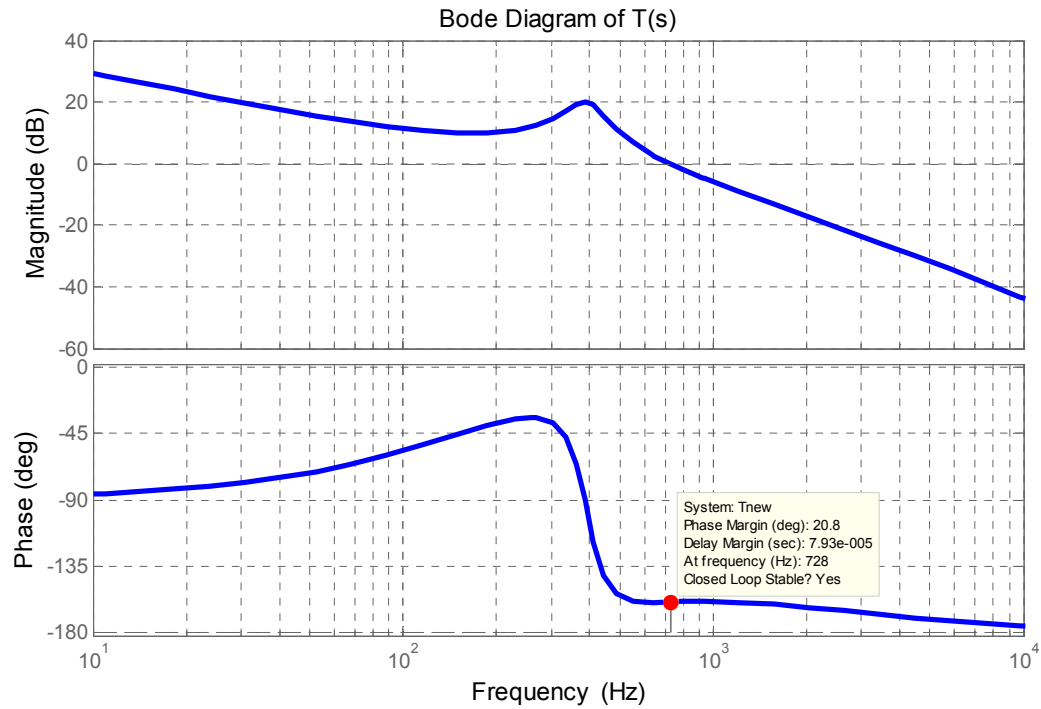
Fig. 11. Bode diagram of the loop gain when (25) is used as the controller transfer for the LRC.

V. EXPERIMENTAL RESULTS

A prototype experimental system is used to verify the theoretical results from the previous section. The overall structure of this system is similar to Fig. 1 except that it has only one type of generation unit. The power rating of this system is one-tenth of the simulation system. The topology of the LRC is similar to what is shown in Fig. 3 and the dc load interfacing converter is a buck converter. These converters are shown in Fig. 12.

Fig. 12. The built prototype LRC and the dc load interfacing converter.

Also, the parameters of these converters are listed in TABLE II. A Texas Instruments TMS320F28335 DSP is used to control these two converters. The "28335" features a 150 MIPS floating-point DSP core with microcontroller-like peripherals, extensive PWM capabilities and a 16-channel analog-to-digital converter (ADC).

TABLE II. PARAMETERS OF THE HARDWARE PROTOTYPE

Converter	Input Voltage [V]	Output Voltage [V]	Processed Power [kW]	Output Capacitance [μF]	Inductance [mH]
Line Regulating Converter	600	400	10	585	1.8
Dc Load Interfacing Converter	400	120	1.6	976	2.2

The three phase inverter connected to the bus drives a Permananet Magnet Synchronous Motor (PMSM). A dc motor is copuled mechanically to the PMSM and genartes negative torque and emulates a mechanical load on the shaft. The coupled PMSM and dc motor are shown in Fig. 13. A signle phase inverter is connected to the bus as well which feeds conventional 120V, 60 Hz ac loads.
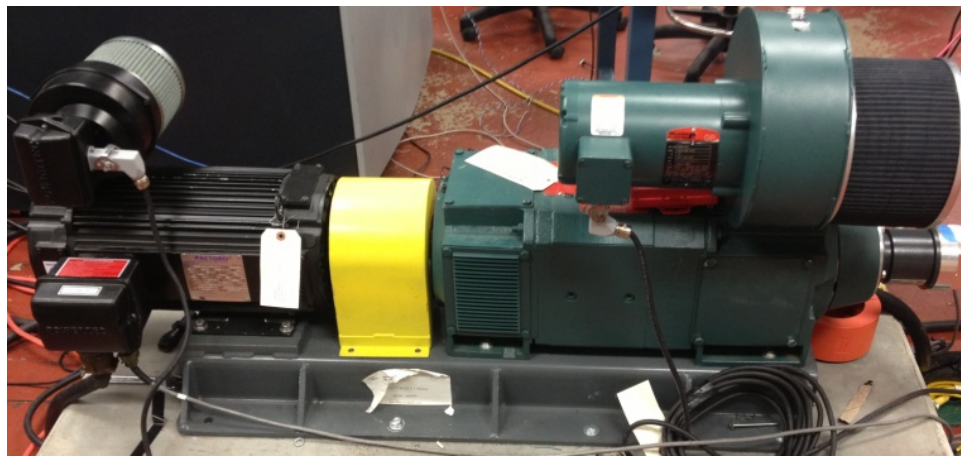
Fig. 13. The Permanent Magnet Synchronous Machine and the dc machine coupled mechanically on one shaft.

Another set of coupled dc motor-Permanent Magnet Synchronous Generator (PMSG) emulates operation of an actual wind generation unit. In this setup, the dc motor runs based on the torque/speed characteristic of a wind turbine and injects mechanical power to the bus. The PMSG draws power from the shaft and transfers it to the bus through an active rectifier system.

For experimental verification the operating point of the system was selected such that the wind generation emulator and LRC transfer roughly 4 kW and 6 kW power to the

bus. At this operating point, storage device converter, single-phase inverter, the dc-dc converter interfacing the dc loads to the bus, and three-phase inverter draw roughly 1.5 kW, 3 kW, 1.5 kW, and 4 kW of power from the bus, respectively.

In the first scenario the controller transfer function for the LRC is a simple PI controller which is designed considering the LRC is operating individually and not connected to a downstream network. The controller transfer function is,

$$G_c = \frac{9.52 \times 10^{-4}(s + 1.4 \times 10^4)}{s} \tag{26}$$

If the converter were to be used to feed a simple resistive load this controller would sufficiently stabilize the converter operation with approximately 60° of phase margin. However, when the LRC is used in its place in dc microgrid system, the phase margin of the system is decreased significantly because of the effect of downstream constant power loads. To see this effect the load of the dc load interfacing converter is stepped down from 3 kW to 1.5 kW and the response of the main dc bus voltage is observed. Fig. 14 shows the resulting waveforms. The waveforms in this figure from top to bottom, are the dc bus voltage, LRC inductor current, output voltage of the dc load interfacing converter, and inductor current of this converter. According to Fig. 14 there are underdamped oscillations in the waveforms and the stability margin of the system is very low.
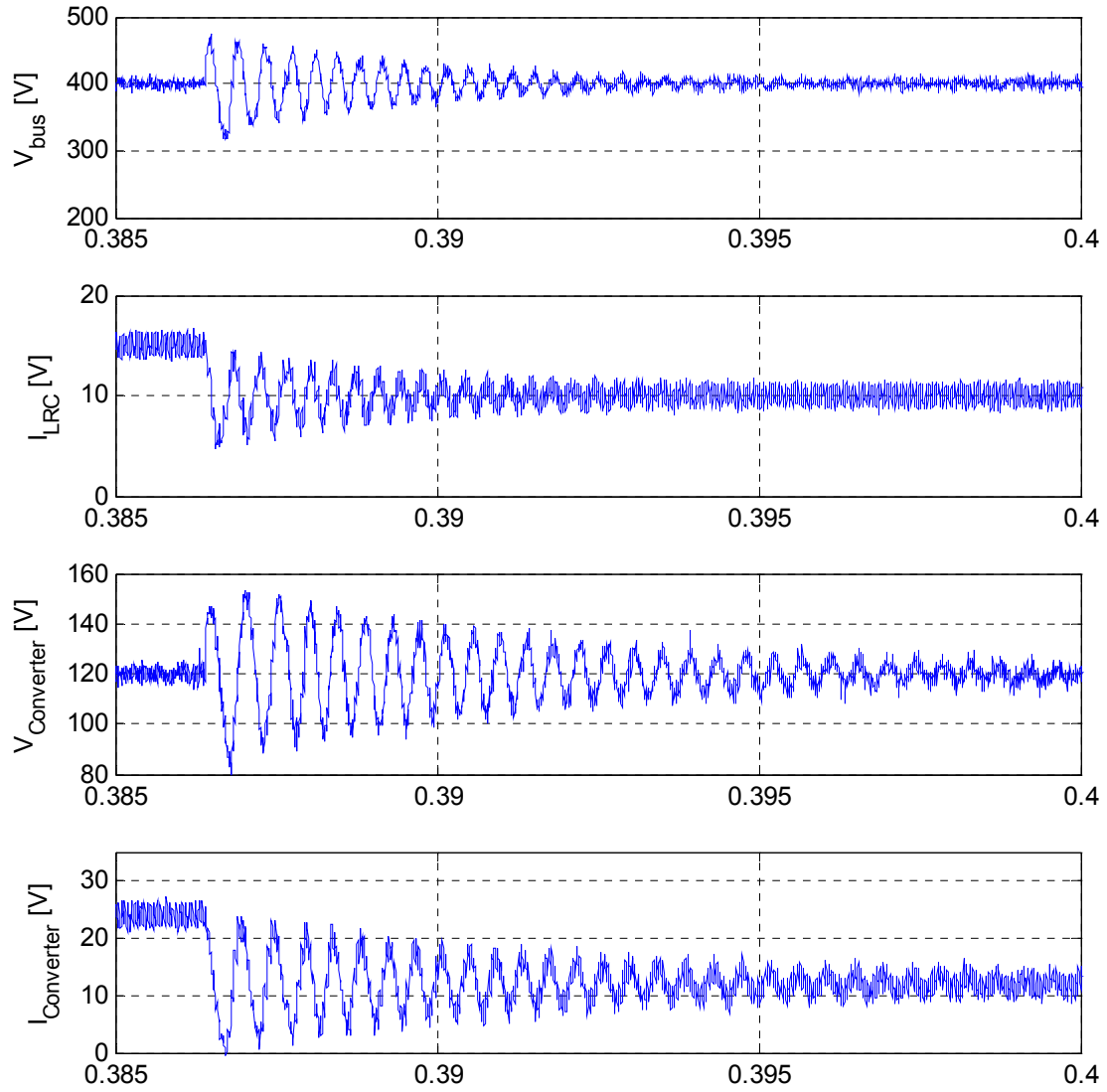
Fig. 14. Response of the dc bus voltage to a step change in the load of the dc-dc interfacing converter when the stability margins of the LRC are very low.

In the second scenario, the controller transfer function of the LRC is modified based on the compensation transfer function method. The compensation transfer function introduced in (14) for this system equals to,

$$G_{comp} = \frac{(s^2 + 3882s + 4.98 \times 10^7)(s^2 + 1.91 \times 10^4 s + 7.46 \times 10^8)}{(s + 2.23 \times 10^4)(s + 7746)(s^2 + 1.286 \times 10^4 s + 3.74 \times 10^8)} \qquad (27)$$

Therefore, a transfer function equal to the compensation transfer function in (27) multiplied by G_c in (26) is used as the main controller transfer function for the LRC. The same experiment as before is performed on the system and the results are shown in Fig. 15. Using the new controller transfer function the system shows highly damped oscillations with low overshoot and undershoot which indicates that the stability margins of the system are larger than the first scenario.

In the third scenario, the controller transfer function of the LRC is designed based on the codesign method. The controller transfer function in this case is,

$$G_c = \frac{1.35 \times 10^{-3}(s + 1.26 \times 10^4)(s + 1.1 \times 10^4)}{s\,(s + 1.57 \times 10^4)} \qquad (28)$$

In this scenario again the load of the dc interfacing converter is stepped down and the resulting waveforms are shown in Fig. 16. Similar to second scenario, the system shows highly damped oscillations with low overshoot and undershoot which indicates that the stability margins of the system are sufficiently larger than the first scenario.
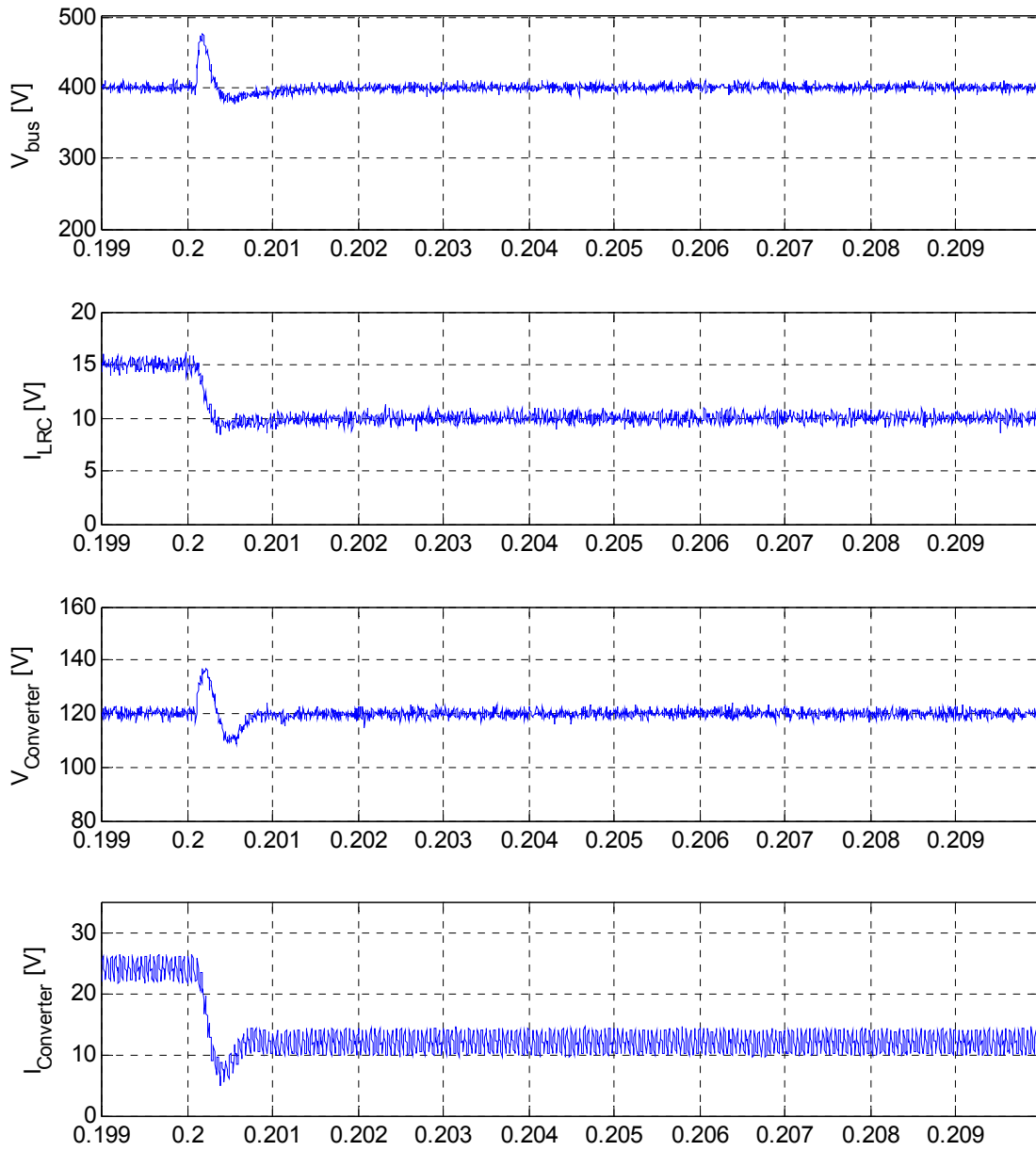
Fig. 15. Response of the dc bus voltage to a step change in the load of the dc-dc interfacing converter when the compensation transfer function method is used to stabilize operation of the LRC.
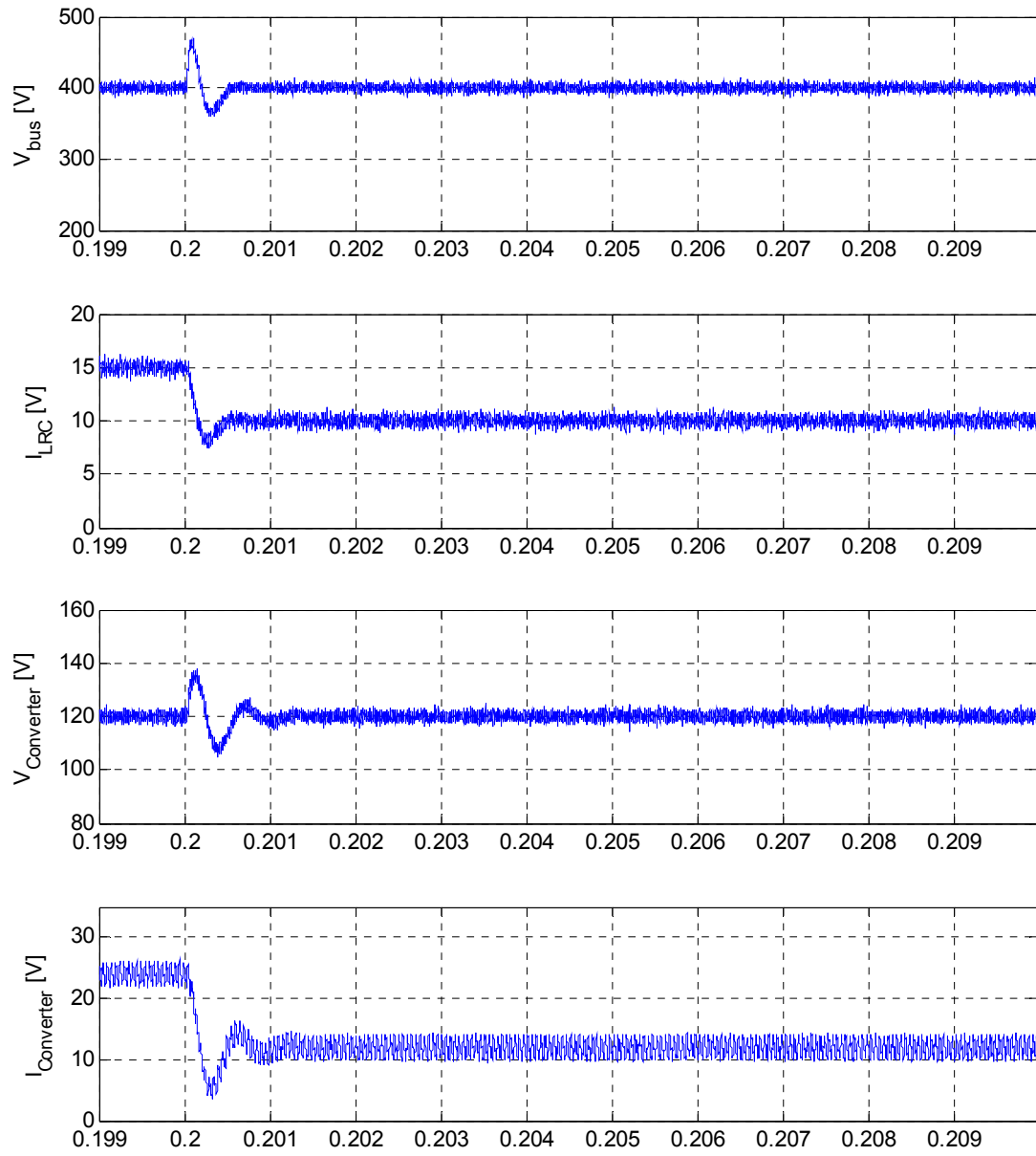
Fig. 16. Response of the dc bus voltage to a step change in the load of the dc-dc interfacing converter when the codesign method is used to stabilize operation of the LRC.

VI. CONCLUSIONS

Two active compensation methods for addressing the issues realted to the effect of the constant power loads on a dc microgrid system were proposed in this work. First, the structure of one type of dc microgrid was introduced. Next, the dynamic model of all of the components of the microgrid were developed, and the complete dynamic model of the dc microgrid system was found by combining the models of the components and simplifying the results. The transfer functions used for stability analysis were extracted from the simplifed microgrid model in this stage. Then, the two proposed controller design methods were explained using the transfer functions derived for a 1 MW microgrid system. Finally, experimntal results from a scaled-down prototype dc microgrid were reported to verify the theoritical outcomes.

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IV.   Improving Performance Of A Dc-Dc Cascaded Converter System Using An Extra Feedback Loop

Reza Ahmadi, and Mehdi Ferdowsi

ABSTRACT -- This paper introduces the extra feedback method as a technique to improve the performance of a cascaded converter system and stabilize its operation. In this paper, first, the block diagram representation of the small-signal model of a single converter is presented. The open-loop and closed-loop transfer functions of this converter are provided in this stage as well. Next, the presented model is expanded to the block diagram model of a cascaded converter system comprised of two dc-dc converters. Then, the extra feedback method which is the main contribution of the paper is introduced. Some design guidelines for applying this method to an experimental cascaded converter system are provided in this part as well. Finally, some experimental results are provided to verify the theoretical outcomes.

I.   INTRODUCTION

The traditional model of the generation and distribution of the electrical energy and the reliability of the current power grid has been recently challenged by the rapid growth of power demand in industrial and residential applications as a result of extensive advancements in the area of power electronics. On the other hand, the energy crisis all over the world has motivated the researchers to find ways to harness the renewable energy sources such as solar and wind power and integrate them into the current power grid [1-4]. Currently, integrating these sources into the power grid is not very easy

because of the distributed and fluctuating nature of renewable energy sources. Because of the two mentioned reasons, the dc distribution systems which have proven to be far more superior for the integration of renewable energy sources into the grid and solving the reliability issues related to excessive power demand have recently been in the center of attention of researchers and engineers in academia and industry.

Although dc distribution systems have many advantages over ac systems such as better compatibility with modern energy sources and electronic loads, better current capabilities of dc power lines, better short circuit protection, transformer-less conversion of voltage levels, higher efficiency, flexibility, and lower cost of implementation, but there are many issues related to safe, efficient, and stable operation of these systems that have to be addressed before they can be fully integrated with the current grid. The stability problem is one of the intriguing areas for researchers in academia and industry because of its high importance for the reliability of a dc network [5-8].

The future dc distribution systems are anticipated to be a mostly converter-dominated grid [9, 10]. This contributes adversely to the stability of the grid. The converters integrated into the dc grid normally have very tight voltage regulation requirements and high efficiency [11, 12]. Therefore, they draw constant power from the grid and exhibit negative incremental impedance property which causes stability issues for the entire system. This has resulted to the formation of a new research area in academia concerning the stability analysis and controller design methods for dc distribution power systems [13-17]. In contrary to conventional control design methods that only consider the stability of individual converters in the dc power system, the new

research efforts are focused on the analysis of the converters in the system considering the interactions between them and the network.

The purpose of this work is to analyze the stability of a simple cascaded converter system commonly found as part of a dc distribution network and introduce a new stabilizing method for the cascaded converter system by adding an extra feedback path between the two converters. The reminder of the paper is organized as follows.

Section II reviews the small-signal modeling of a typical power converter and presents a block diagram model of a power converter used for stability analysis and design. The open-loop and closed-loop transfer functions for buck, boost, and buck-boost converters are provided in this section as well. Section III integrates the models of two power converters and develops the block diagram model of the cascaded converter system. Section IV introduces the extra feedback method and sets forth some design guidelines for implementing this method on an experimental converter system. Section V provides some experimental results to verify the theoretical results. Section VI concludes this paper.

II. SMALL-SIGNAL MODEL OF A DC/DC CONVERTER

A. Open-Loop Transfer Functions

A block diagram small-signal model of a typical dc-dc power converter is shown in Fig. 1 [18]. This model can describe the dynamic behavior of different converters such as buck, boost, and buck-boost by replacing the transfer functions inside the blocks with the transfer functions of the desired converter.
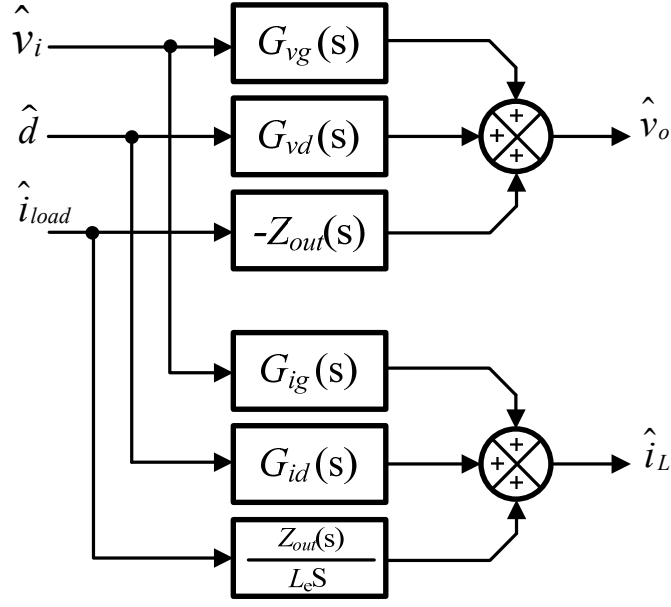
Fig. 1. Block diagram small-signal model of a dc/dc converter without feedback loop.

In this figure $\hat{v}_i(s)$, $\hat{d}(s)$, $\hat{v}_o(s)$, $\hat{i}_L(s)$, and $\hat{i}_{load}(s)$ are representing small-signal value of the input voltage, duty cycle, output voltage, inductor current, and output current respectively. The voltage and current transfer functions shown in Fig. 1 for buck, boost, and buck-boost are found in [19] and listed here,

$$G_{vg}(s) = \frac{M(D)}{L_e C s^2 + \frac{L_e}{R}s + 1}$$

$$G_{vd}(s) = \frac{M(D)e(s)}{L_e C s^2 + \frac{L_e}{R}s + 1} \qquad (1)$$

$$Z_{out}(s) = \frac{L_e s}{L_e C s^2 + \frac{L_e}{R}s + 1}$$

$$G_{ig}(s) = \frac{M(D)}{R} \frac{1+sCR}{L_eCs^2 + \frac{L_e}{R}s+1}$$

$$G_{id}(s) = \frac{M(D)}{R} \frac{(1+sCR)e(s)}{L_eCs^2 + \frac{L_e}{R}s+1}$$

Table I lists the values of $e(s), j(s), M(D)$ and L_e for the mentioned converters.

TABLE I. MODEL PARAMETERS

Converter	$M(D)$	L_e	$e(s)$	$j(s)$
Buck	D	L	$\frac{V_{out}}{D^2}$	$\frac{V_{out}}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V_{out}\left(1 - \frac{sL}{D'^2R}\right)$	$\frac{V_{out}}{D'^2R}$
Buck-Boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$\frac{V_{out}}{D^2}\left(\frac{sDL}{D'^2R}-1\right)$	$-\frac{V_{out}}{D'^2R}$

B. Closed-Loop Transfer Functions

Effect of the control circuit can be described using the above transfer functions and some extra elements related to the voltage feedback loop. The converter model shown in Fig. 1 can be expanded to the closed-loop converter model shown in Fig. 2 by adding those elements related to the feedback loop. The new blocks added to Fig. 1 are, $H(s)$ the sensing network transfer function, $G_c(s)$ the compensator or controller transfer function, and G_M which is a pure gain related to the pulse-width modulator [18]. Model of Fig. 2 permits derivation of the closed-loop transfer functions.
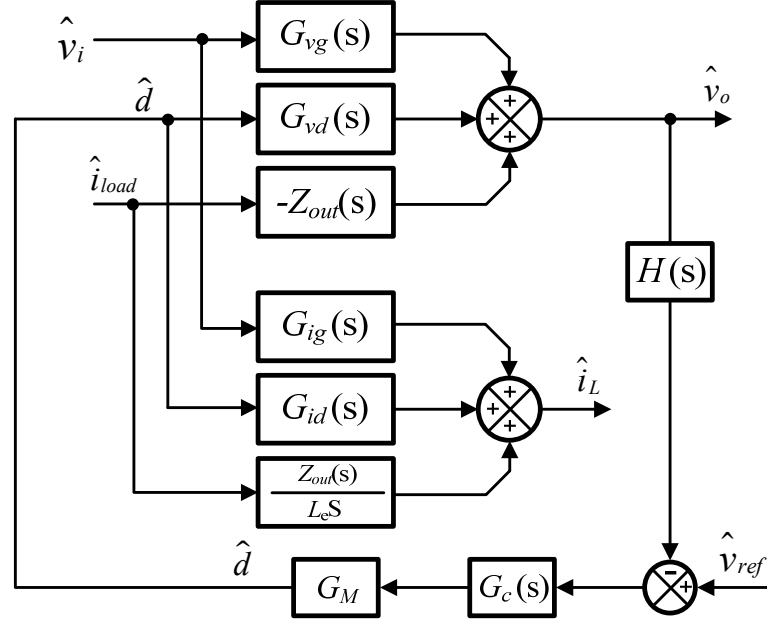
Fig 2. Block diagram small-signal model of a dc/dc converter with voltage mode controlled feedback loop.

The required closed-loop transfer functions for stability analysis are the closed-loop voltage transfer function $\left(G_{vg,CL}\right)$, the closed-loop output impedance $\left(Z_{out,CL}\right)$, and the closed-loop input impedance of the converter $\left(Z_{in,CL}\right)$. These transfer functions are derived assuming the two cascaded converters operate under an output voltage controller (voltage mode control). The closed-loop transfer functions are derived and studied in detail in [19] and are listed here,

$$G_{vg,CL} = \frac{G_{vg}(s)}{1+T(s)}$$

$$Z_{out,CL}(s) = \frac{Z_{out}(s)}{1+T(s)}$$

(2)

$$Z_{in,CL} = \left(\frac{1 + T(s)}{M(D)G_{ig}(s) - T(s)\dfrac{j(s)}{e(s)}} \right)$$

$$T(s) = H(s)G_c(s)G_M G_{vd}(s)$$

III. SMALL-SIGNAL MODEL OF CASCADED CONVERTER SYSTEM

Cascading two dc-dc converters means that the downstream converter (converter 2) acts as the load of the upstream converter (converter 1), thus, the small-signal current drawn from the first converter $\left(\hat{i}_{load1} \right)$ depends on the dynamics of the second converter and equals to the small-signal input current of the second converter. To generate the cascaded converter model from the closed-loop converter model shown in Fig. 2, it should be noted that the small-signal output current of converter 1 can be found by dividing the output voltage of the upstream converter $\left(\hat{v}_{o1} \right)$ by the closed-loop input impedance of the downstream converter $\left(Z_{in,CL2} \right)$ indicating that the effect of the downstream converter on the small-signal current drawn from the upstream converter can be approximated by considering the downstream converter as a single impedance element equal to its closed-loop input impedance. Based on this concept, the block diagram model of the cascaded converter system is shown in Fig. 3. The red branch in this figure illustrates division of the small-signal output voltage of the upstream converter by the closed-loop input impedance of the downstream converter to generate the small-signal output current of the upstream converter.
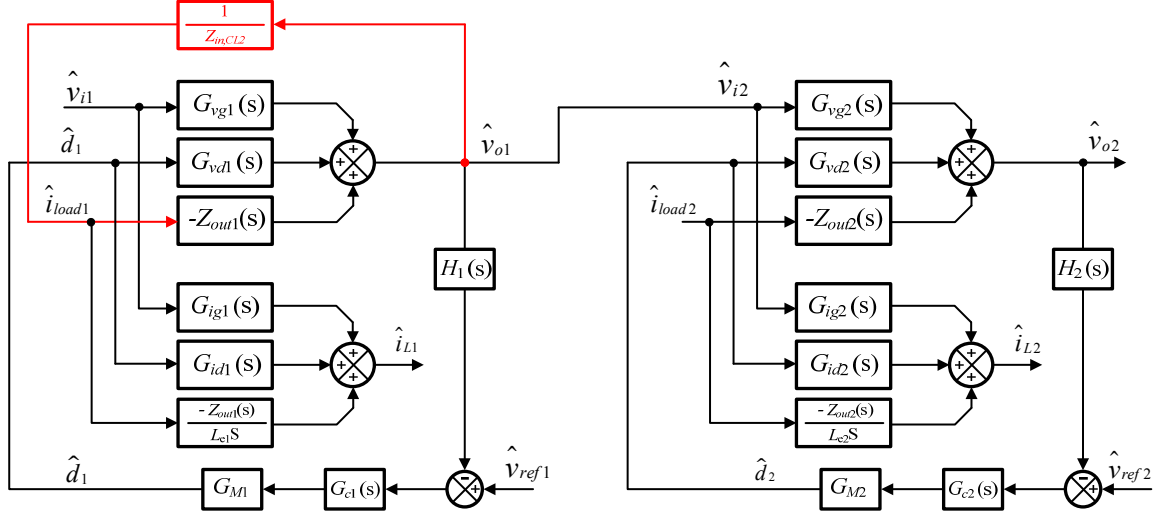
Fig. 3. Block diagram model of the cascaded converter system.

IV. EXTRA FEEDBACK METHOD

Assuming the small-signal value of the input voltage and load are equal to zero $\left(\hat{v}_{i1} = \hat{i}_{load2} = 0\right)$ and omitting the blocks related to the small-signal inductor current in Fig. 3, this block diagram can be reduced to the simplified block diagram of Fig. 4. In the cascaded converter system shown in Fig. 4, when a change in one of the parameters of the downstream converter occurs, the upstream converter's feedback loop cannot sense the resulting effects immediately. This is similar to the effect of a time delay in a control loop and degrades the performance of the system significantly.
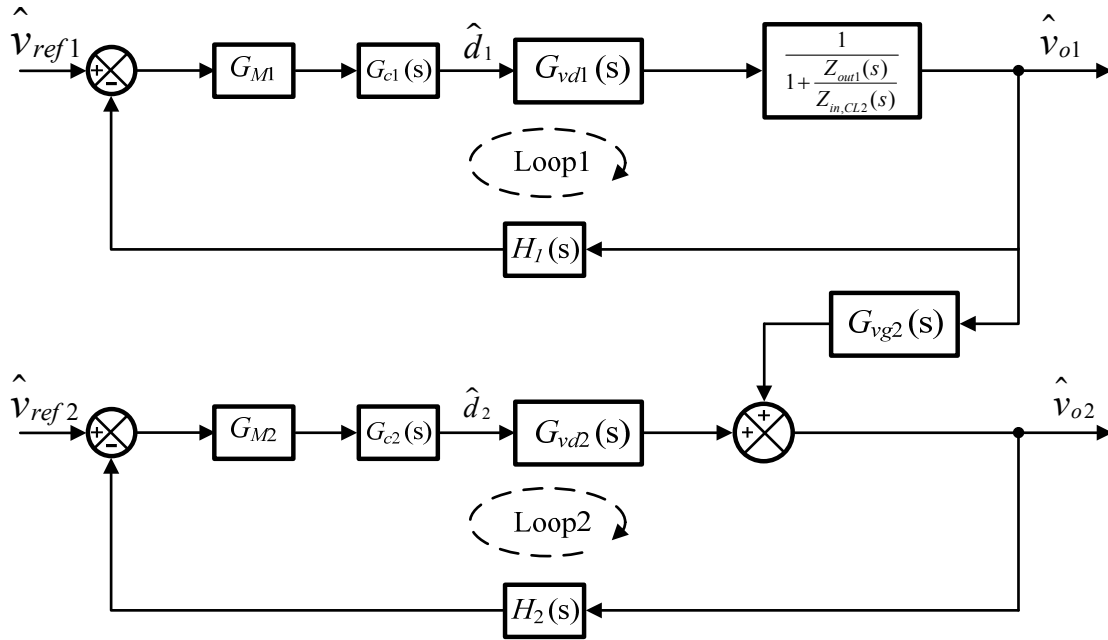
Fig. 4. The simplified block diagram of cascaded converter system.

The idea of this paper is to feed certain information about the changes in the downstream converter directly to the upstream converter's feedback loop in order to eliminate this time delay. Therefore, an extra feedback loop sensing the output voltage of the downstream converter and feeding it to the control loop of the upstream converter through a new compensator block is added to the system. The extra feedback loop is shown in Fig. 5 in red.
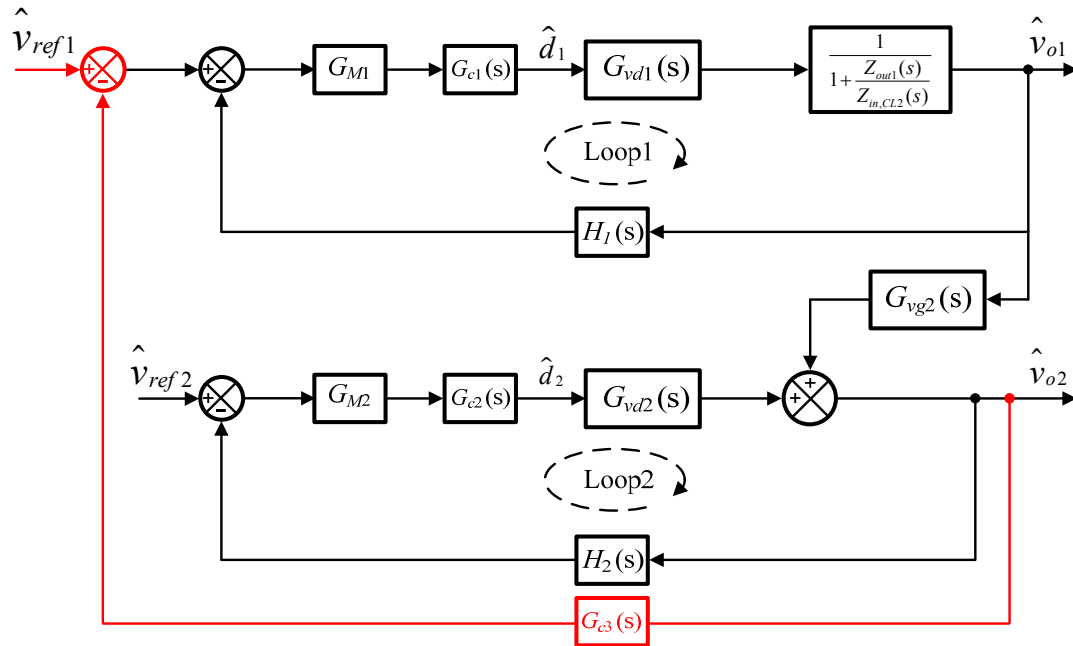
Fig. 5. Simplified block diagram of cascaded converter system with extra feedback loop.

This idea seems logical in theory, but in practice, implementing this extra feedback loop in a way that is shown in Fig. 5 is rather difficult because the dc content of $\hat{v}_{ref1}$ and $\hat{v}_{o2}$ are not generally the same and it is not easy to extract the small-signal content of $\hat{v}_{o2}$ and compare it only with the small-signal part of $\hat{v}_{ref1}$. To overcome this problem, the position of the extra feedback loop is altered by block diagram manipulation so that its operation does not interfere with the regulation of the dc levels by the two feedback loops. Fig. 6 shows the repositioned extra feedback loop in red. The repositioned extra feedback loop has the exact same effect on the system dynamics as the extra feedback loop in its original position with the advantage of not disturbing the dc value of the output voltages.
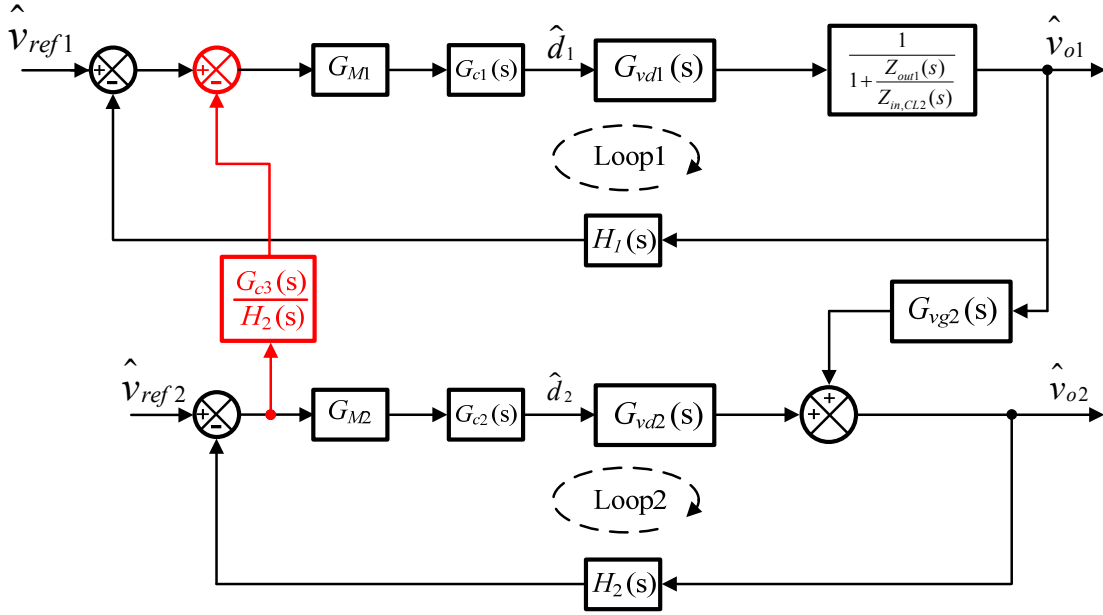
Fig. 6. Simplified block diagram of cascaded converter system with repositioned extra feedback loop.

In order to find a method to design the new compensator in the extra feedback loop $\left(G_{c3}(s)\right)$ the block diagram model shown in Fig. 4 should be simplified. In Fig. 4, it is possible to find the small-signal output voltages ($\hat{v}_{o1}$ and $\hat{v}_{o2}$) in terms of the reference voltages ($\hat{v}_{ref1}$ and $\hat{v}_{ref2}$) with block diagram reduction techniques,

$$\begin{cases} \hat{v}_{o1} = G_1(s)\hat{v}_{ref1} \\ \hat{v}_{o2} = G_2(s)\hat{v}_{ref2} + G_{vg2,CL}(s)G_1(s)\hat{v}_{ref1} \end{cases} \tag{3}$$

where,

$$G_1(s) = \frac{G_{c1}(s)G_{M1}G_{vd1}(s)G_z(s)}{1 + H_1(s)G_{c1}(s)G_{M1}G_{vd1}(s)G_z(s)}$$

$$G_2(s) = \frac{G_{c2}(s)G_{M2}G_{vd2}(s)}{1 + H_2(s)G_{c2}(s)G_{M2}G_{vd2}(s)}$$

(4)

$$G_z(s) = \frac{1}{1 + \dfrac{Z_{out1}(s)}{Z_{in,CL2}(s)}}$$

and $G_{vg2,CL}(s)$ is given in (2). Fig. 7 shows the simplified block diagram found by realizing (3) and integrating the extra feedback loop into the system. As it is obvious from Fig. 7, $G_{c3}(s)$ acts as the controller for an imaginary plant with the transfer function equal to $G_1(s)G_{vg2,CL}(s)$. Therefore $G_{c3}(s)$ can be designed using the conventional frequency response methods for the imaginary plant transfer function of $G_1(s)G_{vg2,CL}(s)$ in order to reach the required dynamic response criteria.
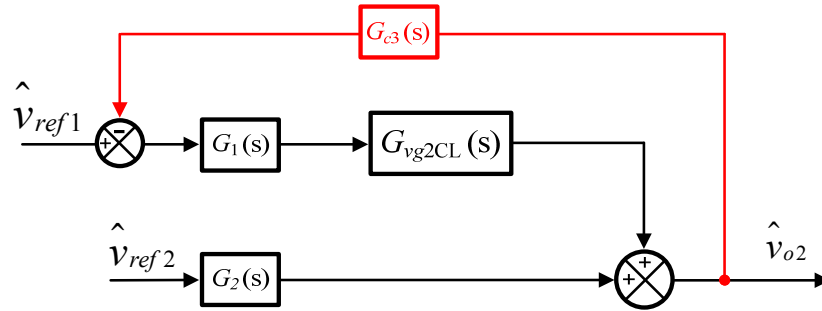

Fig. 7. Simplified block diagram of cascaded converter system found by realizing (3) and integrating the extra feedback loop into the system.

V. EXPERIMENTAL RESULTS

The extra feedback loop is implemented in a prototype cascaded converter system to conduct some experiments. The operation of the cascaded converter system is compared experimentally, when there is no extra feedback loop and when the extra feedback loop is placed in the system. The specifications of the two converters are as follows:

Converter 1) buck converter, $V_{in1} = 48\ V$, $V_{out1} = 12\ V$, $L_1 = 293\ \mu H$, $C_1 = 47\ \mu F$, $H_1 = 1$, $G_{M1} = 1$.

Converter 2) buck converter, $V_{in2} = 12\ V$, $V_{out2} = 5\ V$, $L_2 = 184\ \mu H$, $C_2 = 15\ \mu F$, $R_2 = 3\ \Omega$, $H_2 = 1$, $G_{M2} = 1$.

First, the two converters are cascaded without adding the extra feedback loop. Fig. 8 shows the operation of the two converters in this case. In this figure (and Figs 9-11) the blue trace is the output voltage of converter 1 and the red trace is the output voltage of converter 2.   Fig. 8 clearly depicts that the cascaded converter system is not stable (although each converter is stable separately).
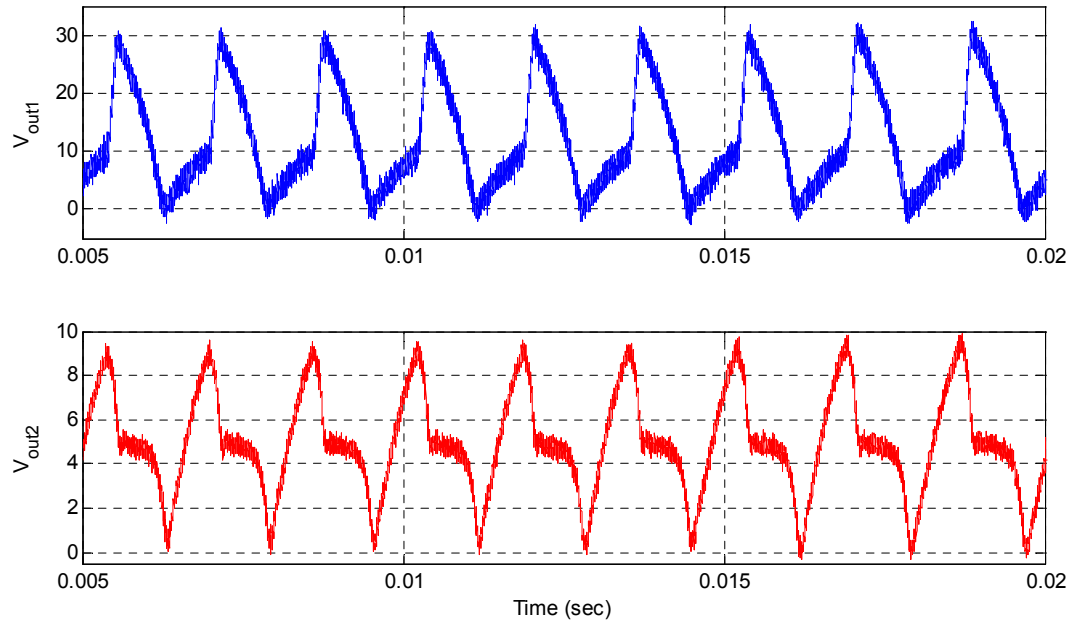
Fig. 8. Operation of the two converters when the extra feedback loop is not added to the system.

Next, the extra feedback loop is added to the system. To design $G_{c3}(s)$ for the mentioned imaginary plant, $G_1(s)$ and $G_{vg2,CL}(s)$ are found from (4) and (1) in order to find the imaginary plant transfer function $\left(G_1(s)G_{vg2,CL}(s)\right)$. $G_{c3}(s)$ is designed for this transfer function based on the required dynamic response specifications. In this case a simple controller with the following transfer function can stabilize the system with a gain margin of $52°$ and bandwidth of 1.6 kHz,

$$G_{c3}(s) = 36\frac{S+1.06\times10^4}{S+4.656\times10^4} \tag{5}$$

The extra feedback loop is integrated into the system in the position shown in Fig. 6 using a digital signal processor (DSP) with $G_{c3}(s)$ equal to the transfer function in (5).

Figures 9, 10, and 11 show the set point tracking, load regulation, and line regulation of the cascaded converter system respectively when the extra feedback loop is added to the system. Obviously, adding the extra feedback loop makes the system stable with a settling time of approximately $600 \, \mu S$.
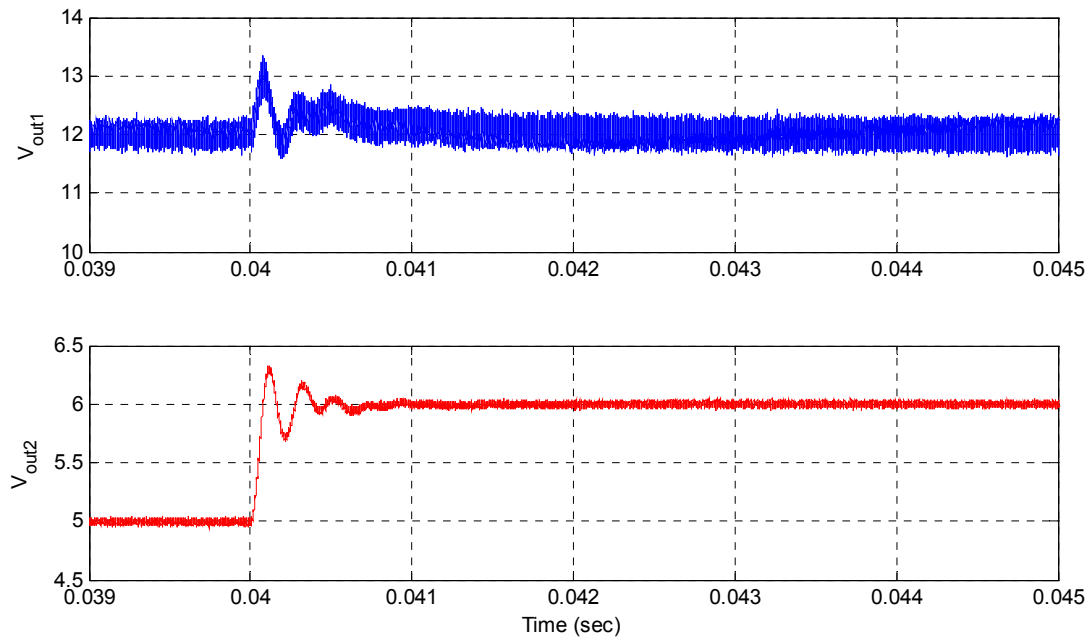

Fig. 9. Set point tracking of the converter system when the extra feedback loop is added to the system. The set point of converter 2 is stepped up from 5V to 6V.
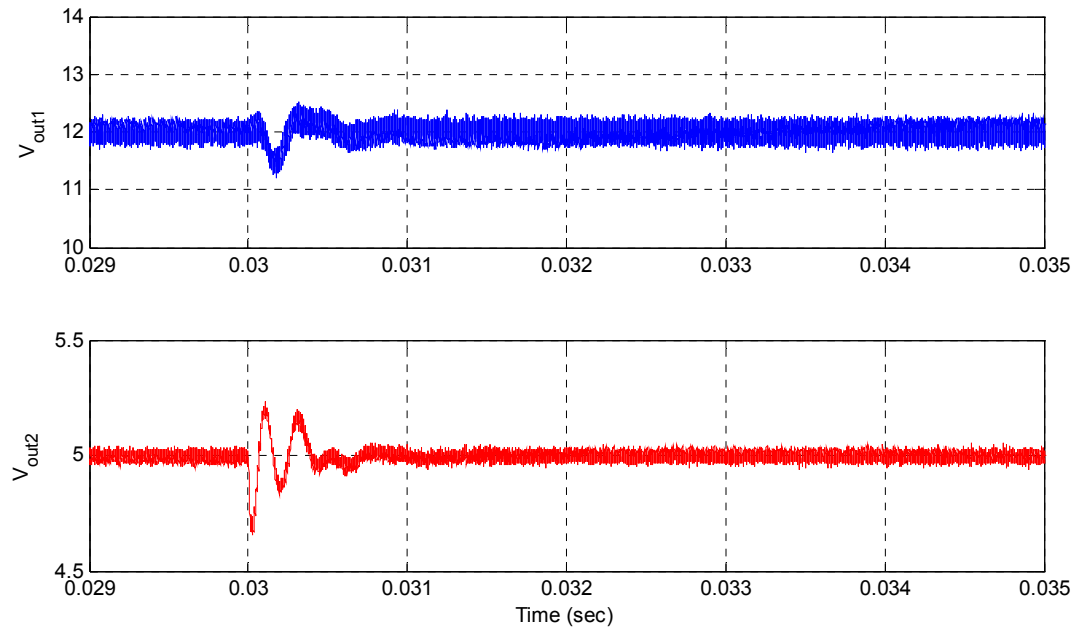
Fig. 10. Load regulation of the converter system when the extra feedback loop is added to the system. The load is stepped down from 0.5Ω to 0.45Ω.
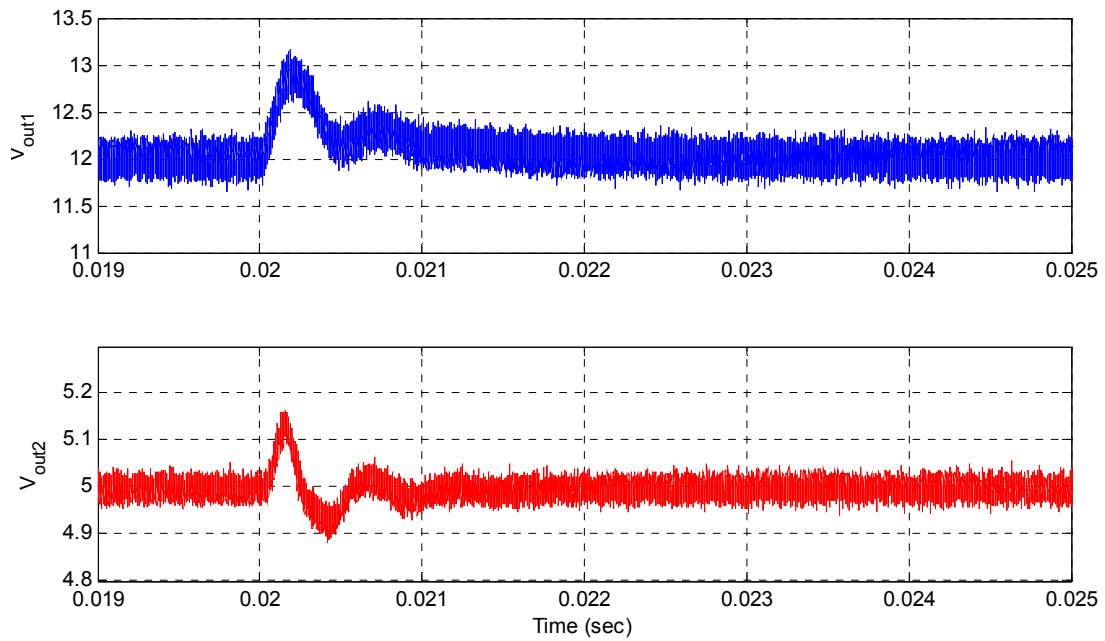

Fig. 11. Line regulation of the converter system when the extra feedback loop is added to the system. The input voltage is stepped up from 24V to 29V.

VI.   Conclusion

The extra feedback method for stabilizing a cascaded converter system was introduced in this paper. In the paper, first the small-signal block diagram model of a single dc-dc converter was introduced. The closed-loop model of the converter was built upon this model and the closed-loop transfer functions of the converter were derived from the closed-loop model. Next, single converter model was expanded to the cascaded converter system model. Then, the extra feedback method was introduced based on the cascaded model. Finally, some experimental results were provided to verify the theoretical outcomes.

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SECTION

2. CONCLUSION

The dc distribution systems are the suitable mean for integrating the renewable energy sources into the current power grid. The dc distribution systems or dc microgrids are known to be the key enabling technology to develop the future smart grid. Dc microgrids come with several advantages over the ac grids such as better current capabilities of power lines, better short circuit protection, and transformer-less conversion of voltage levels, which in turn result in higher efficiency, flexibility, and lower cost of power generation and distribution. There are many issues related to implementation and operation of the dc microgrids that have to be addressed before they can be employed widely.

In this dissertation the problem of dynamic modeling, stability analysis and controller design for a dc microgrid was studied. In Paper I the dynamic modeling of a dc distribution system was investigated. In this paper the small-signal dynamic model, transfer functions, and terminal characteristic of certain types of power electronic converters operating inside a dc grid was presented. Such comprehensive model cannot be found currently in the literature. The results of this paper are necessary for analyzing stability of dc microgrids.

In Paper II stability of a dc microgrid in presence of the constant power loads was studied. In this paper the results from the modeling process were used to assemble complete model of a certain type of dc microgrid. This model was later used to analyze stability of the microgrid using conventional stability analysis methods. The comparison

of the results from the experimental system with the results found theoretically using the methods discussed in this paper confirms the accuracy of the study.

In Paper III and IV the problem of controller transfer function design for the LRC in a dc microgrid system was addressed. In these papers three new controller design methods were introduced. Employing these methods results in finding a controller transfer function that overcomes the destructive effect of the constant power loads on the stability of the dc microgrid and enhances the overall performance and reliability of the system. These methods are found to be easily implementable by engineers in real power electronic systems.

VITA

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