

Designing Ultrafast Loop Response With Type-III Compensation for Current Mode Step-Down Converters

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ABSTRACT

One of the well-known benefits of current-mode control is that the system stability can be easily achieved by Type-II compensation design. It is possible to improve the transient response of a current mode DC/DC converter by adopting Type-III compensation to boost the crossover frequency and phase margin. Type-III compensation is simple to design and needs only one extra component.

This application report shows a general, step-by-step, Type-III compensation design procedure for current-mode, step-down DC/DC converters as well as a design example using the TPS54620 from the SWIFT™ converter product portfolio.

To simplify design efforts, a complementary design calculator ([SLVC219](#)) is available.

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1 Introduction

The latest generation of SWIFT™ DC/DC converters such as the TPS54418 and TPS54620 families have implemented current-mode control to simplify the external compensation design. [Figure 1](#) from *TPS54620EVM-374 6-A, SWIFT™ Regulator Evaluation Module user's guide (SLVU281)* shows a typical current-mode design schematic. [Figure 2](#) shows the measured loop-response characteristics at $V_{in} = 12\text{ V}$ and $V_{out} = 3.3\text{ V}/6\text{ A}$.

The resistor R4 and capacitor C4 in [Figure 1](#) determine a typical Type-II compensation network. The overall system is stable with 45-kHz crossover frequency and 46° phase margin. For a general-purpose DC/DC converter, 45-kHz crossover frequency is adequate. In some applications, ultrafast transient response may be required and 100-kHz crossover frequency or higher may be desired. Because the power-stage phase response can drop fast at high frequencies, it is usually difficult to maintain adequate phase margin using Type-II compensation. A Type-III compensation network can be selected as an alternative.

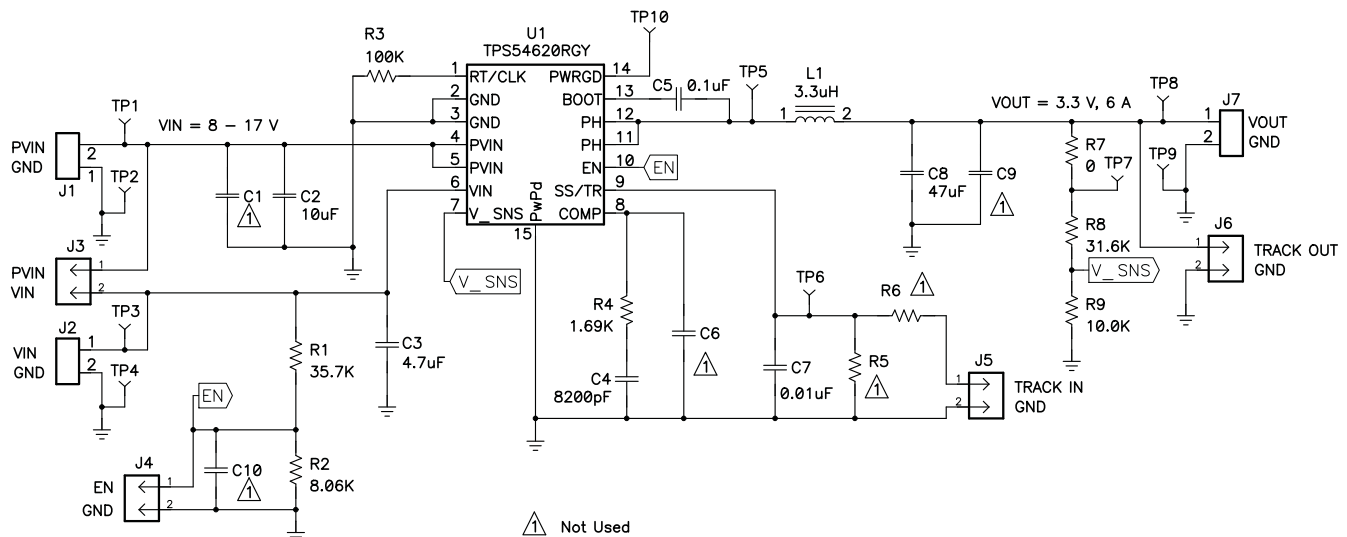


Figure 1. TPS54620EVM-374 Schematic (Fsw = 480 kHz)

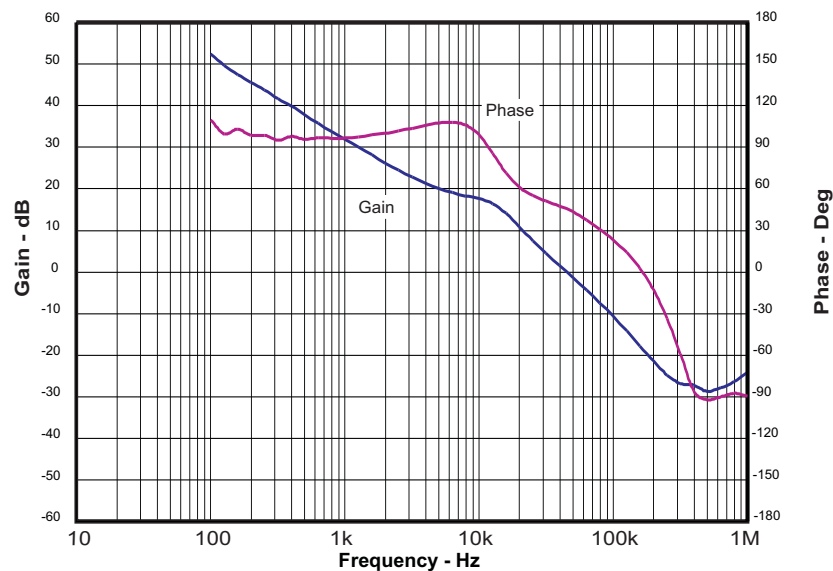


Figure 2. Measured Loop Response for TPS54620EVM-374

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2 Basic of Compensation Networks

Figure 3 and Figure 4 show commonly used Type-II and Type-III compensation networks. The difference between the Type-2A/2B and the Type-3A/3B circuits is that the Type-2A/3A circuits include an additional high-frequency pole which has been added to attenuate high-frequency noise, when necessary.

The only difference between the Type-2A/2B and Type-3A/3B circuits is the capacitor C_c . This capacitor generates one more zero around the desired crossover frequency, and forms one very-high-frequency pole in the system which is normally ignorable.

R_{oea} and C_{oea} are the equivalent output resistance and output capacitance respectively for the g_m error amplifier. The equation for R_{oea} calculation is shown in Table 1. C_{oea} is usually small and can be neglected.

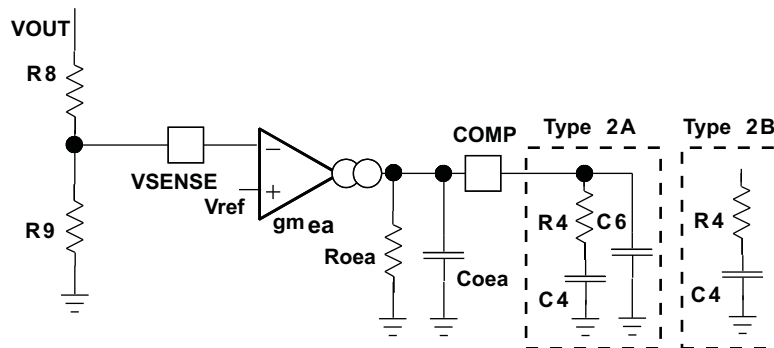


Figure 3. Type-II Compensation Networks

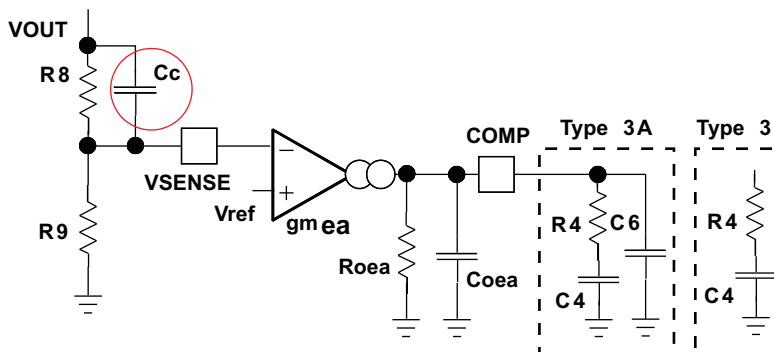
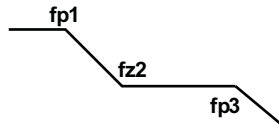
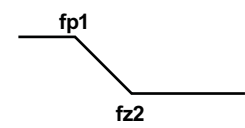
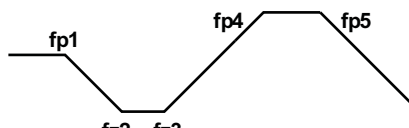
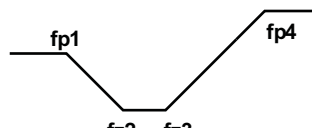


Figure 4. Type-III Compensation Networks

Table 1 provides the frequency responses and simplified pole/zero locations for the compensation networks shown in Figure 3 and Figure 4.

Table 1. Frequency Responses and Simplified Pole/Zero Locations

Compensation	Frequency Responses	Pole/Zero Locations
Type 2A		$f_{p1} = \frac{1}{2\pi \times R_{oea} \times C4}$ $f_{z2} = \frac{1}{2\pi \times R4 \times C4}$ $f_{p3} = \frac{1}{2\pi \times R4 \times C6}$
Type 2B		$f_{p1} = \frac{1}{2\pi \times R_{oea} \times C4}$ $f_{z2} = \frac{1}{2\pi \times R4 \times C4}$
Type 3A		$f_{p1} = \frac{1}{2\pi \times R_{oea} \times C4}$ $f_{z2} = \frac{1}{2\pi \times R4 \times C4}$ $f_{z3} = \frac{1}{2\pi \times R8 \times Cc}$ $f_{p4} = \frac{1}{2\pi \times (R8//R9) \times Cc}$ $f_{p5} = \frac{1}{2\pi \times R4 \times C6}$
Type 3B		$f_{p1} = \frac{1}{2\pi \times R_{oea} \times C4}$ $f_{z2} = \frac{1}{2\pi \times R4 \times C4}$ $f_{p3} = \frac{1}{2\pi \times R8 \times Cc}$ $f_{p4} = \frac{1}{2\pi \times (R8//R9) \times Cc}$
Where $R_{oea} = \frac{DCgain_{ea}}{gm_{ea}}$, $R8 // R9 = \frac{R8 \times R9}{R8 + R9}$		

3 Design Procedure for Current-Mode Type-III Compensation Networks

Using the same design parameters for [Figure 1](#), this section presents the general design procedure for Type-III compensation networks.

1. Design the power stage of the switching regulator. In this example, a 3.3-μH inductor and two 100-μF, 6.3-V ceramic capacitors are selected as the output inductor and output capacitors, respectively. See the corresponding data sheet ([SLVS949](#)) and design calculator ([SLVC219](#)) for the details.

Table 2. TPS54620EVM-374 Design Parameters

Parameter	Value
Output voltage (VOUT)	3.3 V
Output current (IOUT)	6 A
Input voltage (VIN)	12 V nominal, 8 V to 17 V
Switching frequency (Fsw)	480 kHz

2. Determine the crossover frequency f_c . It is suggested to choose f_c between 70kHz and 130kHz. Generally speaking, the desired f_c should be lower for lower output voltage applications because the limited phase boost available from the Type-III compensation network. For details, see [Section 5](#). In this case, f_c is selected to be 120 kHz.

3. R4 can be determined by

$$R4 = \frac{2\pi \times f_c \times V_{OUT} \times C_o}{g_{m_{ea}} \times V_{ref} \times g_{m_{ps}}} = \frac{2\pi \times 120\text{kHz} \times 3.3\text{V} \times (47.6\mu\text{F} \times 2)}{1300\mu\text{A/V} \times 0.8\text{V} \times 16\text{A/V}} = 14.2\text{k}\Omega \approx 14.3\text{k}\Omega \quad (1)$$

Where:

$g_{m_{ea}}$ – the GM amplifier gain (1300 $\mu\text{A/V}$)

$g_{m_{ps}}$ – the power stage gain (16 A/V).

V_{ref} – the reference voltage (0.8 V)

In [Equation 1](#), the actual output equivalent capacitance must be used. For ceramic output capacitors, the actual capacitance has to be properly derated according to the applied DC voltage. A simplified derating equation for standard ceramic output capacitor is shown in [Equation 2](#). For more accurate derating models, refer to the manufacturer data sheets for the output capacitors being used.

$$C_{o,actual} = C_{o,nominal} \times \frac{V_{rating} - V_{dc}}{V_{rating}} = 100\mu\text{F} \times \frac{6.3\text{V} - 3.3\text{V}}{6.3\text{V}} = 47.6\mu\text{F} \quad (2)$$

Where:

V_{rating} – the voltage rating of the ceramic capacitor

V_{dc} – the applied DC voltage of the ceramic capacitor

4. Place a compensation zero at the dominant pole f_p . $\left(f_p = \frac{1}{C_o \times R_L \times 2\pi} \right)$
C4 can be determined by:

$$C4 = \frac{R_L \times C_o}{R4} = \frac{V_{OUT} \times C_o}{I_{OUT} \times R4} = \frac{3.3\text{V} \times (47.6\mu\text{F} \times 2)}{6\text{A} \times 14.3\text{k}\Omega} = 3.67\text{nF} \approx 3.9\text{nF} \quad (3)$$

5. C6 is optional. It can be used to cancel the zero from the ESR (Equivalent Series Resistance) of the output capacitor C_o .

$$C6 = \frac{R_{ESR} \times C_o}{R4} \quad (4)$$

C6 is usually only needed when the ESR zero is less than half of the switching frequency.

$$f_{esr} = \frac{1}{2\pi \times R_{ESR} \times C_o} = \frac{1}{2\pi \times 2\text{m}\Omega \times (47.6\mu\text{F} \times 2)} = 836.3\text{kHz} \quad (5)$$

In this case, the ESR zero is located at 836.3 kHz, which is greater than $f_{sw}/2 = 240\text{ kHz}$. So, C6 is not used. C6 is usually not needed for ceramic output capacitors.

6. Cc is selected to provide a zero around the desired crossover frequency (f_c) with R8. When using Type-III compensation design, it is convenient to fix R8 value at 10 k Ω and vary R9 to set the output voltage V_{OUT} .

$$C_c = \frac{1}{2\pi \times R8 \times f_c} = \frac{1}{2\pi \times 10\text{k}\Omega \times 120\text{kHz}} = 132.7\text{pF} \approx 150\text{pF} \quad (6)$$

The complete example design with Type-III compensation is shown in [Figure 5](#).

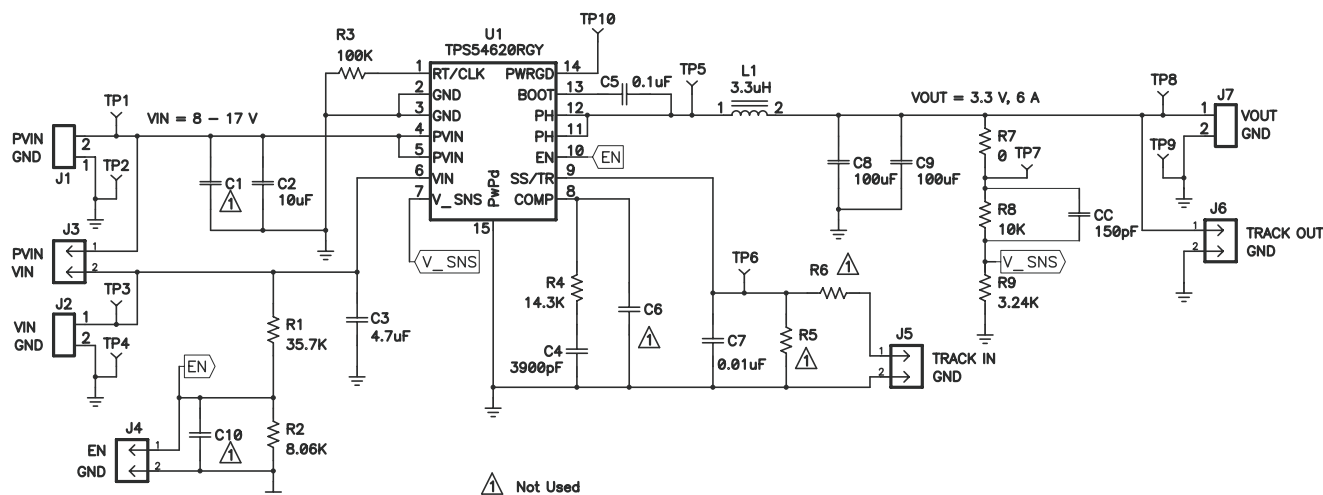


Figure 5. Example Design With Type-III Compensation ($F_{sw} = 480$ kHz)

4 System Performances for Example Design

Figure 6 shows the loop-response characteristics. Gain and phase plots are shown for $V_{in} = 12$ V and $V_{out} = 3.3$ V/6 A. The crossover frequency and phase margin are measured at 112 kHz and 60° , respectively.

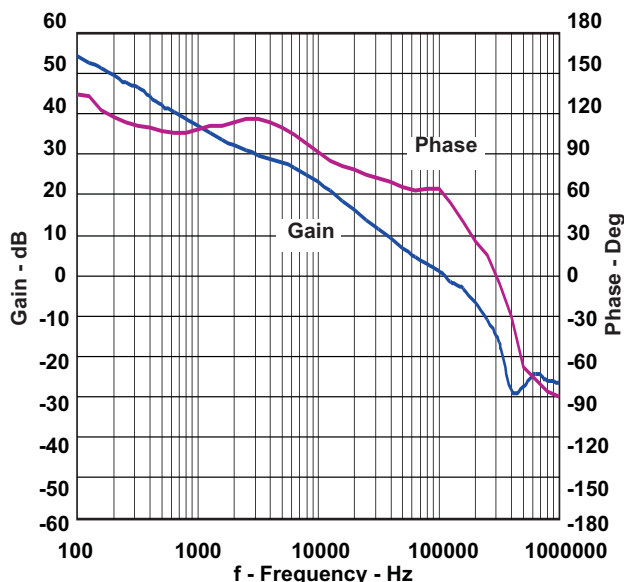


Figure 6. Measured Loop Response for Example Design

Figure 7 shows the response to load transients. The current step is from 25% to 75% of maximum-rated load at $V_{in} = 12$ V. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output. Figure 8 shows the transient response for the TPS54620EVM-374 under the same condition. Comparing Figure 7 and Figure 8, the total peak-to-peak voltage variation has been dropped from 50 mV to 25 mV.

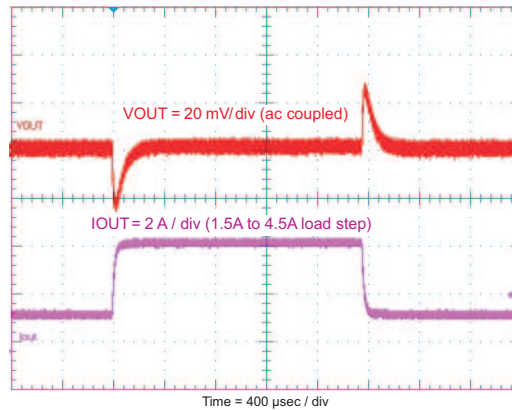


Figure 7. Example Design Transient Response

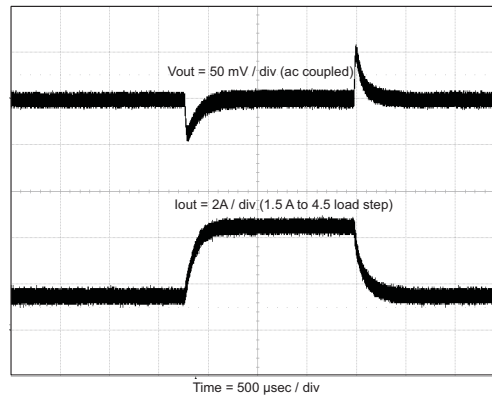


Figure 8. TPS54620EVM-374 Transient Response

5 Limitations for Current-Mode Type-III Compensation Design Procedure

The design procedure described uses simplified equations. It provides starting parameter values for a design. Sometimes, these values may have to be modified to yield the best results.

The Type-III compensation is usually able to boost the system bandwidth above 100 kHz with good phase margin. As the output voltage decreases, the phase boost from Type-III compensation is also reduced. Depending on the application requirements, the improvements on the crossover frequency and phase margin by the Type-III compensation may be limited at low output voltages. [Figure 9](#) provides guidelines on the maximum phase boost that can be obtained from Type-III compensation for popular output voltage range.

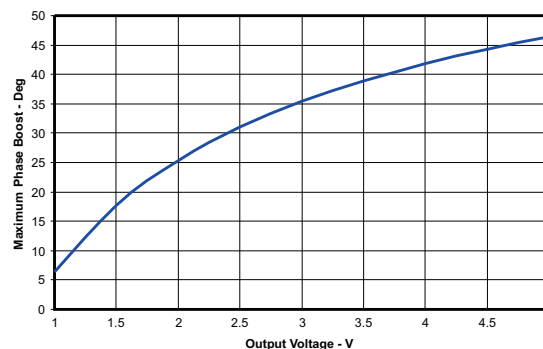


Figure 9. Maximum Phase Boost From Type-III Compensation

6 Conclusion

This application report shows an easy way to do Type-III compensation designs for current-mode, step-down DC/DC converters. The experimental measurements also illustrate the improvements of system bandwidth and transient responses by Type-III compensation design.

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