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Stabilize the Buck Converter with Transconductance Amplifier

By Michael (Chongming) Qiao, Parviz Parto and Reza Amirani

Synchronous DC-DC buck converters have high efficiency, and International Rectifier has developed a series of PWM voltage mode controllers for synch buck converters, including single and multi-phase controllers such as IRU3037, IRU3038, IRU3046 and IRU3055. One feature of these controllers is that transconductance amplifiers are employed as voltage feedback error amplifiers.

Stabilize the Buck Converter with Transconductance Amplifier

Michael (Chongming) Qiao, Parviz Parto and Reza Amirani, International Rectifier

Synchronous buck converters have received great attention in low power, low voltage DC-DC converter applications in recent years due to their high efficiency. International Rectifier Inc. has developed a series of PWM voltage mode controllers for synchronous buck converters, including single phase and multi-phase controllers such as IRU3037, IRU3038, IRU3046, IRU3055, etc. One feature of these controllers is that transconductance amplifiers are employed as voltage feedback Error Amplifiers. Theoretically, a transconductance amplifier is an equivalent voltage controlled current source. It multiplies the difference of input voltage with a certain gain and generates a current into the output node. It features high output impedance and it is stable by most of the output compensation components. The output short circuit protection and internal compensation is not required. This results in a smaller die size and simple design. In this application note, how to stabilize the buck converter with transconductance Error amplifier is discussed. The goal of the design is to provide a loop gain function with a high bandwidth (high zero-crossover frequency) and adequate phase margin. As a result, fast load response and good steady state output can be achieved.

1. Introduction to Synchronous Buck Converter with Transconductance Amplifier

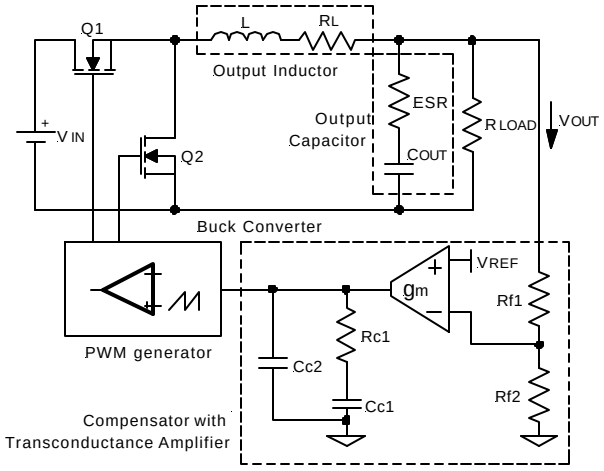

Figure 1 - Simplified diagram for synchronous buck converter with transconductance amplifier.

The simplified diagram for synchronous buck converter with transconductance amplifier is shown in Figure 1, where R_L is the inherent resistance of output inductor and ESR is the Equivalent Series Resistance of output capacitor. There are three sections. One is synchronous buck converter including output inductor and capacitor. The controller such as IRU3037 provides the basic function block such as PWM generator and transconductance amplifier. The resistor and capacitor with the transconductance amplifier, function as a compensator to stabilize the system. From control system point of view, the three blocks are shown in Figure 2.

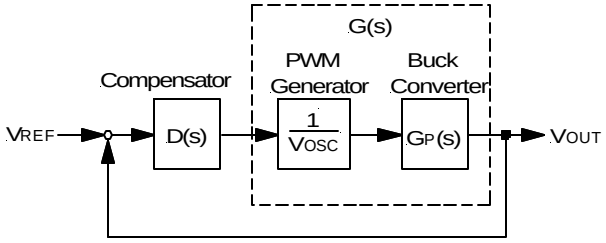

Figure 2 - The control diagram for the synchronous buck converter with transconductance amplifier.

The transfer function of the PWM generator is basically $1/V_{OSC}$, where V_{OSC} is the peak to peak voltage of oscillator listed in the datasheet. The transfer function of the buck converter can be simplified as follows:

$$G_P(s)=\frac{1+ESR\times C_{OUT}\times s}{1+s\times\left(\frac{L}{R_{LOAD}}+ESR\times C_{OUT}\right)+s^2\times L\times C_{OUT}}\times V_{IN} \quad ---(1)$$

The (s) indicates that the transfer function varies as a function of frequency.

For simplification, we can combine the transfer function of PWM generator and buck converter. This results in power stage of buck converter and is expressed as:

$$G(s) = G_P(s)\times\frac{1}{V_{OSC}} \quad ---(2)$$

Basically, the transfer function of the power stage is a second order system and the Bode plot is shown in Figure 3. The resonance of the output LC filter introduces a double pole and -40dB Gain Slope (see Figure 3). The resonance frequency of the LC filter is expressed as follows:

$$F_{PO} = \frac{1}{2\times\pi\times\sqrt{L\times C_{OUT}}} \quad ---(3)$$

The ESR of the output capacitor and capacitance introduces one zero for the system. The zero is given as:

$$F_{ZO} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad ---(4)$$

Where F_{ZO} is a character parameter and dependent on the characteristic of what capacitor is chosen. Typically, for an electrolytic capacitor, the F_{ZO} is in a few KHz range.

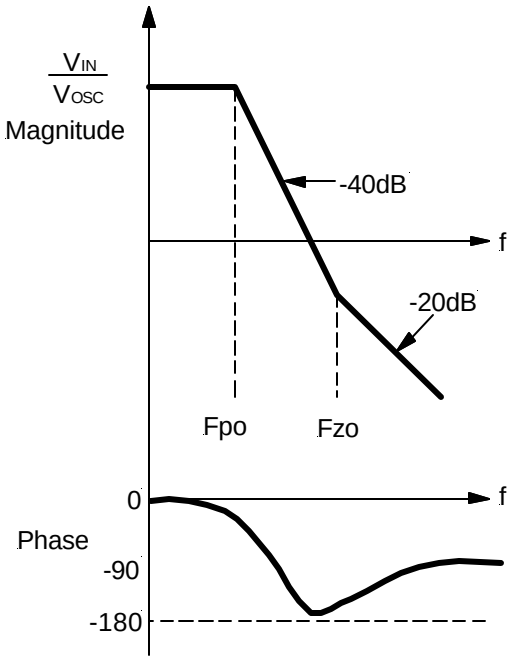

Figure 3 - The Bode plot of buck converter power stage.

2. Loop Gain of System

The loop gain of system is defined as the product of transfer function along the closed control loop. From Figure 2, the loop gain is defined as:

$$H(s) = D(s) \times \frac{1}{V_{OSC}} \times G_P(s) = D(s) \times G(s) \quad ---(5)$$

The Bode plots of desired loop gain and power stage is shown in Figure 4, where F_O is the zero crossover frequency defined as the frequency when loop gain equals unity. Typically, F_O can be chosen to be 1/10~1/5 of the switching frequency. F_O determines how fast the dynamic load response is. The higher F_O is, the faster dynamic response will be. The slope rate of loop gain around F_O should be –20dB in order to get a stable system. The phase margin is shown in Figure 4. Typically, 45° or more phase margin is desired for a stable system.

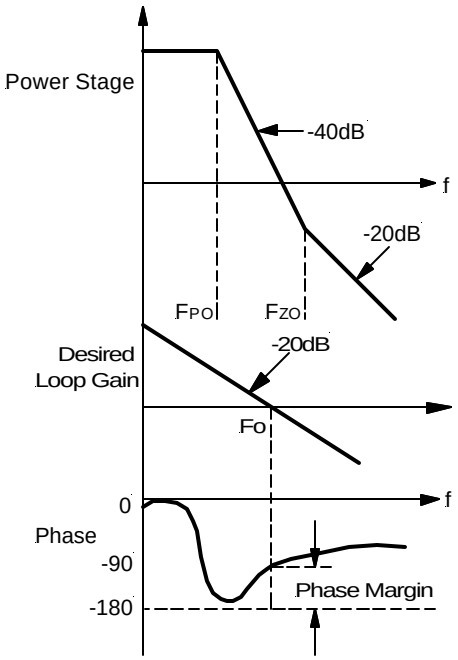

Figure 4 - Bode plot of desired loop gain function.

3. Typical Procedure of Compensator Design

In order to realize the desired loop gain with high enough zero-cross over frequency and proper phase margin, a compensator has to be designed. A typical procedure is as follows:

Step 1 - Collect system parameters such as input voltage, output voltage, etc. and determine switching frequency.
Step 2 - Determine the power stage poles and zeros.
Step 3 - Determine the zero crossover frequency and compensation type. The compensation type is determined by the location of zero crossover frequency and characteristics of output capacitor as shown in Table 1.

Compensator Type	Location of Zero Crossover Frequency (F_O)	Typical Output Capacitor
Type II (PI)	$F_{PO} < F_{ZO} < F_O < f_S/2$	Electrolytic, Tantalum
Type III (PID) Method A	$F_{PO} < F_O < F_{ZO} < f_S/2$	Tantalum, Ceramic
Type III (PID) Method B	$F_{PO} < F_O < f_S/2 < F_{ZO}$	Ceramic

Table 1 - The compensation type and location of zero crossover frequency.

Step 4 - Determine the desired location of zeros and poles for the selected compensator.
Step 5 - Calculate the real parameters-resistor and capacitors for the selected compensator. Choose the resistors and capacitors from standard catalog such that they are as close to the calculated value as possible.

4. Type II (PI) Compensator Design

4.1) Introduction to PI Compensator

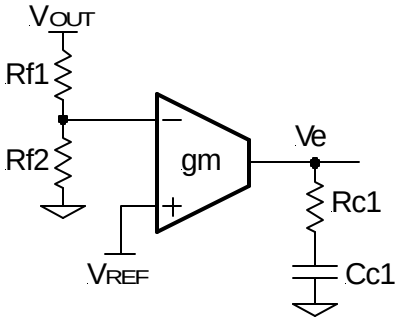

Figure 5 - PI Compensator configuration.

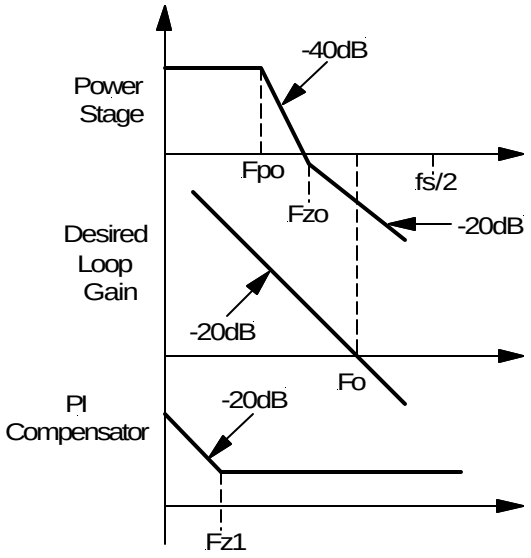

Figure 6 - Bode plot of the buck converter power stage, desired loop gain and PI compensator.

In many applications, an electrolytic capacitor is chosen as the output capacitor due to its low cost. For electrolytic capacitor, the zero caused by ESR (F_{ZO}) is a few KHz. If the switching frequency is a few hundred KHz, the zero crossover frequency F_O is chosen to be 1/10 of switching frequency and F_O is located at:

$$F_{PO} < F_{ZO} < F_O < f_S/2$$

A PI compensator can be used as shown in Figure 5. Overall, the Bode plots of power stage, desired loop gain and PI compensator are displayed in Figure 6.

A PI compensator has one zero at:

$$F_{Z1} = \frac{1}{2\pi \times R_{C1} \times C_{C1}} \qquad ---(6)$$

Resistors R_{f1} and R_{f2} are used to determine the output voltage. The output voltage is determined as:

$$\frac{V_{REF}}{V_{OUT}} = \frac{R_{f2}}{R_{f1} + R_{f2}} \qquad ---(7)$$

The output voltage can be directly connected to the feedback pin of the Error amplifier. This is shown as:

$$V_{OUT} = V_{REF}$$

The resistor R_{C1} determines the zero crossover frequency. It can be calculated as:

$$R_{C1} = \frac{2\pi \times F_O \times L \times V_{OSC}}{ESR \times V_{IN} \times gm} \times \frac{R_{f1} + R_{f2}}{R_{f2}}$$

When the above equation is combined with equation (7), it results to:

$$R_{C1} = \frac{2\pi \times F_O \times L \times V_{OSC}}{ESR \times V_{IN} \times gm} \times \frac{V_{OUT}}{V_{REF}} \qquad ---(8)$$

Set the zero of PI compensator to 75% of F_{PO}:

$$F_{Z1} = \frac{1}{2\pi \times R_{C1} \times C_{C1}} = 0.75 \times F_{PO} \qquad ---(9)$$

The compensator capacitor Cc1 can be calculated as:

$$C_{C1} = \frac{1}{0.75 \times 2\pi \times F_{PO} \times R_{C1}} = \frac{\sqrt{L \times C_{OUT}}}{0.75 \times R_{C1}} \qquad ---(10)$$

In practice, one more capacitor is sometimes added in parallel with the RC network as shown in Figure 7.

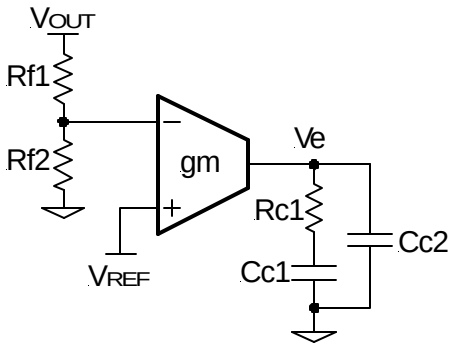

Figure 7 - PI compensator with one additional pole.

This additional capacitor gives a second pole as:

$$F_{P2} = \frac{1}{2\pi \times R_{C1} \times \frac{C_{C1} \times C_{C2}}{C_{C1} + C_{C2}}} \qquad ---(11)$$

Set this pole to one half of switching frequency, which results in the capacitor Cc2.

$$F_{P2} = \frac{f_S}{2}$$

$$C_{C2} = \frac{1}{\pi \times R_{C1} \times f_S - \frac{1}{C_{C1}}} \cong \frac{1}{\pi \times R_{C1} \times f_S} \qquad ---(12)$$

4.2) Design Example of PI Compensator

Take IRU3037 controlled buck converter as an example. The schematic is shown in Figure 8.

Step 1 - Collect system parameters such as input voltage, output voltage, etc. and determine switching frequency.

Input Voltage	5V
Output Voltage	3.3V
Output Current	10A
Switching Frequency	200KHz
Output Inductor	3.3μH
Output Capacitor	2200μF with 18mΩ ESR
Peak to Peak Oscillator Ramp Voltage	V_{OSC} = 1.25V
Reference Voltage	V_{REF} = 1.25V
Transconductance Gain	g_m=0.6mA/V or 600μmho

Table 2 - The parameters of IRU3037 controlled buck converter in Figure 8.

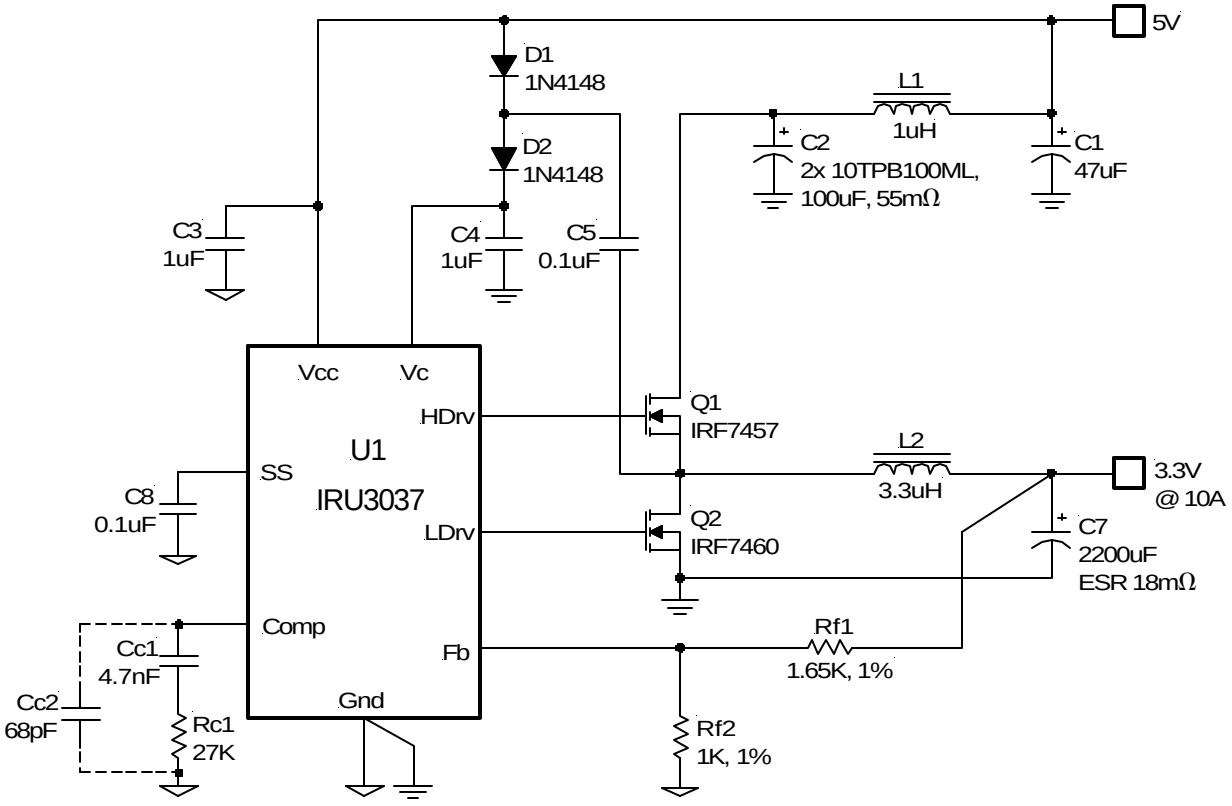

Figure 8 - Application of IRU3037 with PI compensator.

Step 2 - Determine the power stage poles and zeros. The pole caused by the output inductor and output capacitor is calculated as:

$$F_{PO} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{PO} = \frac{1}{2\pi \times \sqrt{3.3\mu H \times 2200\mu F}} \cong 1.87KHz$$

The zero caused by ESR of the output capacitor is calculated as:

$$F_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$F_{ZO} = \frac{1}{2\pi \times 18m\Omega \times 2200\mu F} \cong 4KHz$$

Step 3 - Determine the zero crossover frequency and compensation type. Select desired zero-crossover frequency:

$$F_O \le \frac{f_S}{5} \sim \frac{f_S}{10}$$

Select F_O=20KHz

Because we have $F_{PO} < F_{ZO} < F_O < \frac{f_S}{2}$, a PI Compensator is chosen.

Step 4 - Determine the desired location of zeros and poles for the selected compensator. Select:

$$F_{Z1} = 0.75 \times F_{PO} = 0.75 \times 1.87KHz \cong 1.4KHz$$

If additional capacitor is chosen:

$$F_{P2} = \frac{f_S}{2} = 100KHz$$

Step 5 - Calculate the real parameters-resistor and capacitors for the selected compensator.
Calculate R_{C1} from equation (8):

$$R_{C1} = \frac{2\pi \times F_O \times L \times V_{OSC}}{ESR \times V_{IN} \times g_m} \times \frac{V_O}{V_{REF}}$$

$$R_{C1} = \frac{2\pi \times 20KHz \times 3.3\mu H \times 1.25}{18m\Omega \times 5V \times 0.6 \times 10^{-3}} \times \frac{3.3}{1.25}$$

$R_{C1} \cong 25.3K$
Select R_{C1} = 27K

Calculate C_{C1} By:

$$C_{C1} = \frac{1}{0.75 \times 2\pi \times F_{PO} \times R_{C1}} = \frac{\sqrt{L \times C_{OUT}}}{0.75 \times R_{C1}}$$

$$C_{C1} = \frac{\sqrt{3.3\mu H \times 2200\mu F}}{0.75 \times 27K} \cong 4.2nF$$

Select C_{C1} = 4.7nF

(Optional) Second capacitor C_{C2} can be calculated using equation (12):

$$C_{C2} = \frac{1}{\pi \times R_{C1} \times f_S} = \frac{1}{\pi \times 27K \times 200K} \cong 59pF$$

Select C_{C2} = 68pF

Calculate resistors R_{f1} and R_{f2}. Select resistor R_{f2} to be a reasonable value. For example, from low noise point of view, select R_{f2}=1K, 1%.

$$R_{f1} = \frac{V_O - V_{REF}}{V_{REF}} \times R_{f2} = \frac{3.3 - 1.25}{1.25} \times 1K = 1.64K$$

Select R_{f1} = 1.64K, 1%

5. Type III (PID) Compensator

5.1) Introduction

The PI compensation is based on the output capacitor having enough ESR to ensure stability. If the output capacitor is a ceramic capacitor, the zero caused by ESR will be much larger than the desired zero cross over frequency, the type III (PID) compensation is considered as shown in Figure 9. The Bode plot of the PID compensation network is shown in Figure 10.

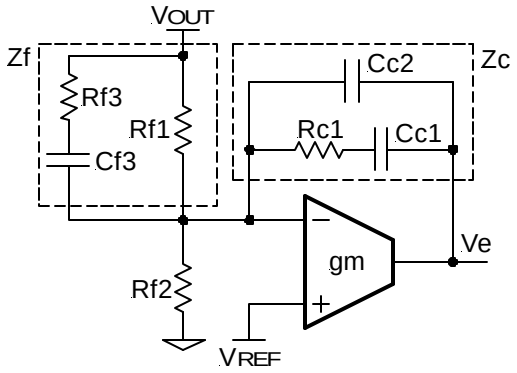

Figure 9 - PID compensation network.

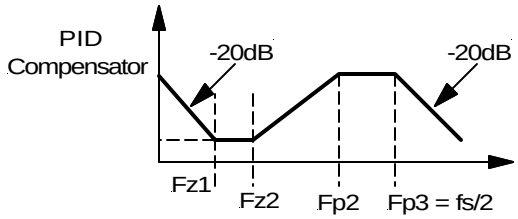

Figure 10 - Bode plot of PID compensator.

The transfer function of the PID compensator is given as:

$$\frac{V_e}{V_{OUT}} = \frac{1-g_m \times Z_C}{1+g_m \times Z_f+Z_f/R_{f2}} \quad \text{---(13)}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m \times Z_f >> 1+ \frac{Z_f}{R_{f2}} \quad \text{and} \quad g_m \times Z_C >> 1$$

So we have:

$$\frac{V_e}{V_{OUT}} \cong -\frac{Z_C}{Z_f}$$

By replacing the Z_C and Z_f according to Figure 9, the transfer function can be expressed as:

$$D(s)= \frac{1}{s \times R_{f1} \times (C_{C1}+C_{C2})} \times \frac{\left(1+ \frac{s}{2\pi \times F_{Z1}}\right)\left(1+ \frac{s}{2\pi \times F_{Z2}}\right)}{\left(1+ \frac{s}{2\pi \times F_{P2}}\right)\left(1+ \frac{s}{2\pi \times F_{P3}}\right)} \quad \text{---(14)}$$

The compensator has two zeros and three poles.

$$F_{Z1} = \frac{1}{2\pi \times R_{C1} \times C_{C1}} \quad \text{---(15)}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{f3} \times (R_{f1}+R_{f3})} \quad \text{---(16)}$$

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_{f3} \times C_{f3}} \quad \text{---(17)}$$

$$F_{P3} = \frac{1}{2\pi \times R_{C1} \times \frac{C_{C1} \times C_{C2}}{C_{C1}+C_{C2}}} \quad \text{---(18)}$$

The type III compensator is usually designed by selection of location of F_{Z1}, F_{Z2}, F_{P2} and F_{P3} in order to get the desired zero crossover frequency and enough phase margin. If $g_m \times Z_C > 1$, equation (13) will change its polarity and a 180 degree phase shift will be introduced. The system will become unstable. Therefore, a careful selection of Z_C has to be made. It is verified that the following restriction has to be followed:

$$R_{C1} >> \frac{2}{g_m} \text{ (mandatory);}$$

$$R_{f1} \,||\, R_{f2} \,||\, R_{f3} > \frac{1}{g_m} \text{ (desirable)} \quad \text{---(19)}$$

Where $R_{f1} \,||\, R_{f2} \,||\, R_{f3}$ are the parallel resistance of R_{f1}, R_{f2} and R_{f3}.

5.2) Type III (PID) Compensator Design Method A

If the zero caused by ESR is less than half of the switching frequency, that is $F_{PO}<F_O<F_{ZO}<f_S/2$, then the following design method can be used.

Set first zero of PID at 75% of the resonant pole caused by output inductor and capacitor:

$$F_{Z1} = 75\% \times F_{PO} \quad \text{---(20)}$$

Set second zero of PID at exact resonant pole caused by output inductor and capacitor:

$$F_{Z2} = F_{PO} \quad \text{---(21)}$$

Set second pole of PID at the zero caused by output capacitor ESR:

$$F_{P2} = F_{ZO} \quad \text{---(22)}$$

Set the third pole of PID at one half of switching frequency:

$$F_{P3} = f_S/2 \quad \text{---(23)}$$

The Bode plot of power stage and proposed PID compensator is shown in Figure 11.

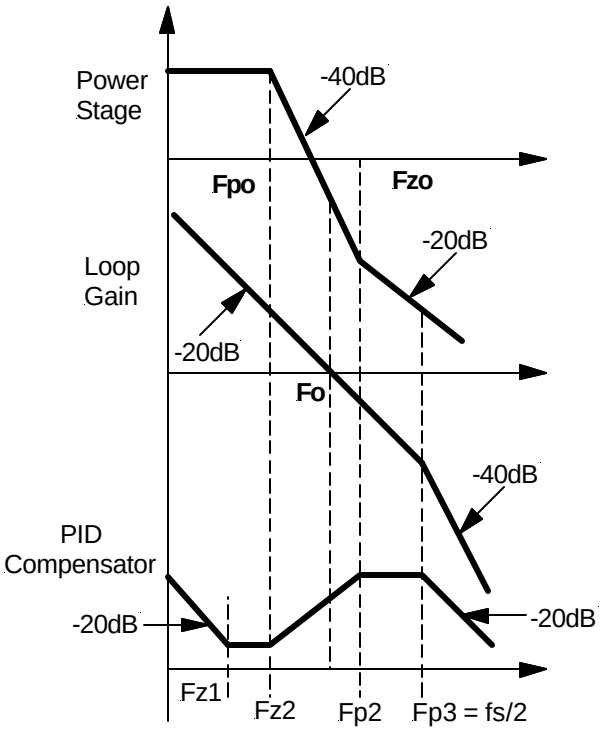

Figure 11 - The Bode plot of the buck converter power stage, the desired loop gain and PID compensator (method A).

The zero crossover frequency F_O is determined by the following equation:

$$C_{f3} = \frac{V_{OSC} \times 2\pi \times F_O \times L \times C_{OUT}}{V_{IN} \times R_{C1}} \quad \text{---(24)}$$

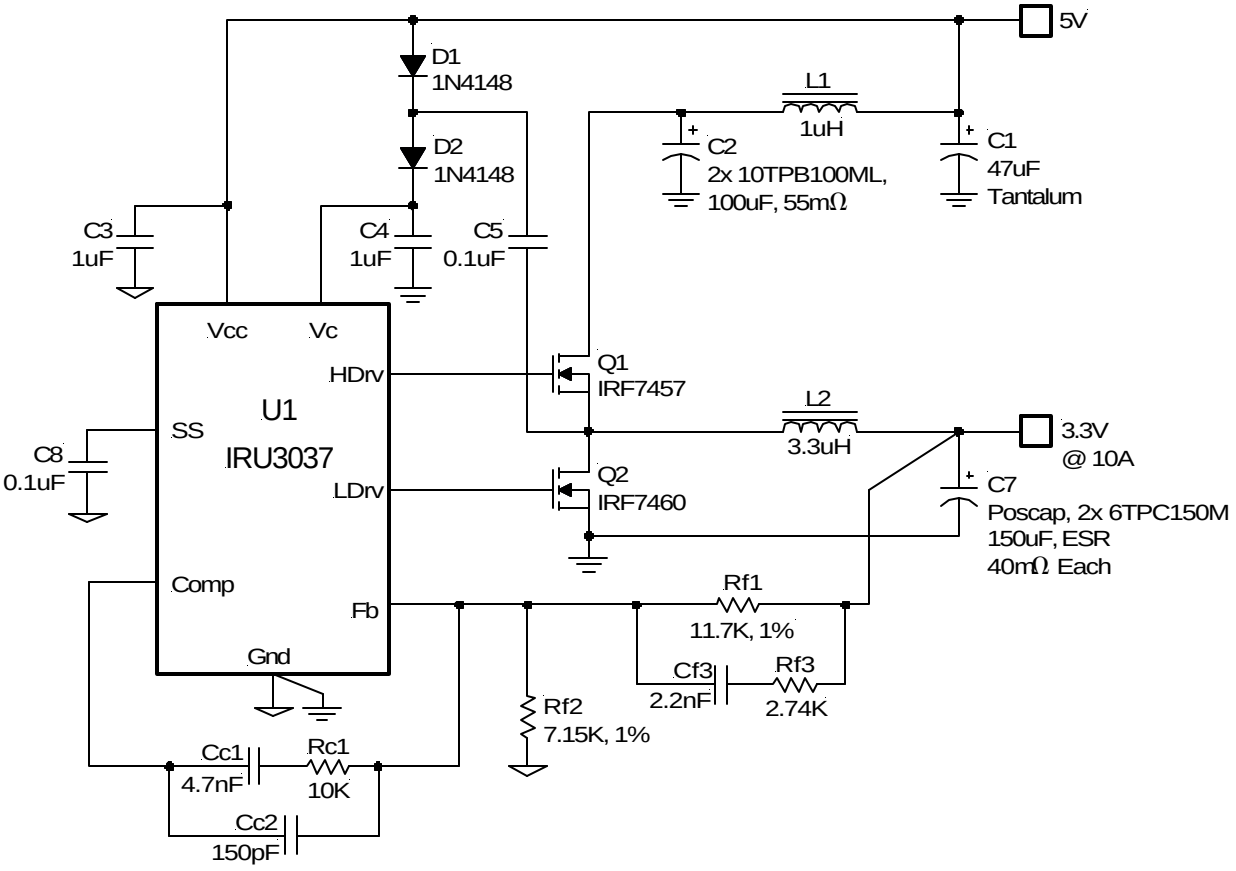

Figure 12 - An example of IRU3037 controlled buck converter with PID compensation method A.

5.3) Design Example of PID Compensator Method A

Step 1 - Collect system parameters in Figure 12 such as input voltage, output voltage, etc. and determine the switching frequency. Comparing with section 4.2, only the output capacitor is changed. The output capacitor is $2\times150\mu F$ with $40m\Omega$ each. The total ESR is:

$$ESR = 40m\Omega/2 = 20m\Omega$$

Total capacitor is:

$$C_{OUT} = 2\times150\mu F = 300\mu F$$

Step 2 - Determine the power stage poles and zeros.

$$F_{PO} = \frac{1}{2\pi\times\sqrt{L\times C_{OUT}}}$$

$$F_{PO} = \frac{1}{2\pi\times\sqrt{3.3\mu H\times300\mu F}} \cong 5KHz$$

Zero caused by ESR:

$$F_{ZO} = \frac{1}{2\pi\times ESR\times C_{OUT}} = \frac{1}{2\pi\times20m\Omega\times2\times150\mu F}$$

$$F_{ZO} \cong 26.5KHz$$

Step 3 - Determine the zero crossover frequency and compensation type. Select desired zero-crossover frequency.

$$F_O \le \frac{f_S}{5} \sim \frac{f_S}{10}$$

If we select F_O=30KHz and we have $F_{PO}<F_{ZO}<F_O<f_S/2$, the PI compensator in section 4.2 can be chosen.

Suppose F_O=15KHz and $F_{PO}<F_O<F_{ZO}<f_S/2$, then a PID compensator with method A is chosen.

Step 4 - Determine the desired location of zeros and poles for the selected compensator. Select:

$$F_{Z1} = 0.75\times F_{PO} = 3.75KHz$$

$$F_{Z2} = F_{PO} = 5KHz$$

$$F_{P2} = F_{ZO} = 26.5KHz$$

$$F_{P3} = \frac{f_S}{2} = \frac{200KHz}{2} = 100KHz$$

Step 5 - Calculate the real parameters-resistor and capacitors for the selected compensator.

Select R_{C1} so that $R_{C1} >> \frac{2}{g_m}$

$$\frac{2}{g_m} = \frac{2}{0.6mA / V} \cong 3.3K$$

Select $R_{C1} = 10K$

Calculate C_{C1} and C_{C2} by setting $F_{Z1}=0.75 \times F_{PO}$ and $F_{P3}=f_S/2$:

$$C_{C1} = \frac{1}{2\pi \times F_{Z1} \times R_{C1}} = \frac{1}{2\pi \times 3.75KHz \times 10K} = 4.2nF$$

Select $C_{C1} = 4.7nF$

$$C_{C2} \cong \frac{1}{2\pi \times F_{P3} \times R_{C1}} = \frac{1}{2\pi \times 100KHz \times 10K} = 159pF$$

Select $C_{C2} = 150pF > 30pF$(reasonable capacitor)

Calculate capacitor C_{f3} by using equation (24):

$$C_{f3} = \frac{V_{OSC} \times 2\pi \times F_O \times L \times C_{OUT}}{V_{IN} \times R_{C1}}$$

$$C_{f3} = \frac{1.25 \times 2\pi \times 15KHz \times 3.3\mu H \times 300\mu F}{5V \times 10K} \cong 2.3nF$$

Select $C_{f3}=2.2nF$

Calculate R_{f3} and R_{f1} by setting $F_{P2}=F_{ZO}$ and $F_{Z2}=F_{PO}$:

$$R_{f3} = \frac{1}{2\pi \times C_{f3} \times F_{P2}} = \frac{1}{2\pi \times 2.2nF \times 26.5KHz} = 2.73K$$

Select $R_{f3} = 2.74K$

$$R_{f1} = \frac{1}{2\pi \times C_{f3} \times F_{Z2}} - R_{f3}$$

$$R_{f1} = \frac{1}{2\pi \times 2.2nF \times 5KHz} - 2.74K = 11.7K$$

Select $R_{f1} = 11.7K$

Calculate R_{f2}:

$$R_{f2} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{f1}$$

$$R_{f2} = \frac{1.25}{3.3 - 1.25} \times 11.7K = 7.13K$$

Select $R_{f2} = 7.15K$, 1%

Check:

$R_{f1} \| R_{f2} \| R_{f3} = 11.7K \| 7.15K \| 2.74K$
$R_{f1} \| R_{f2} \| R_{f3} \cong 1.7K > 1/g_m = 1.6K$

If $R_{f1} \| R_{f2} \| R_{f3} < 1/g_m$, then iteration may be required by going back and selecting a larger R_{C1}.

5.4) Type III (PID) Compensation Design Method B

If a ceramic capacitor is chosen, the zero caused by ESR of capacitor is in the order of the switching frequency such as $F_{ZO} > f_S/2$. The compensator method A will not be very suitable. The compensation calculation can be based on the lead lag compensation (method B). The Bode plot of power stage, loop gain, PID compensator method B and phase are shown in Figure 13.

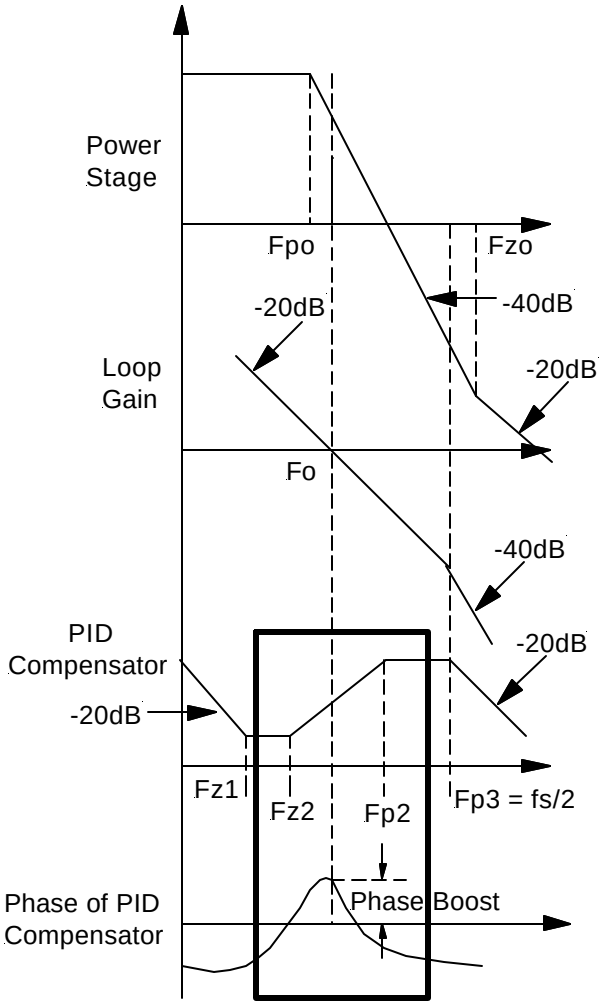

Figure 13 - Bode plot of buck converter with PID compensator method B.

In the bold outline area of Figure 13, the PID compensator can be seen as lead-lag compensation. It is known that the lead-lag compensation can give a maximum phase boost at frequency.

$$F = \sqrt{F_{P2} \times F_{Z2}} \qquad \text{---(25)}$$

The maximum phase gain will be generated, that is:

$$\theta_{MAX} = \text{Sin}^{-1}\left(\frac{F_{P2} - F_{Z2}}{F_{P2} + F_{Z2}}\right) \quad \text{---(26)}$$

One of the design strategies is that we can set the maximum phase boost occurring at zero-cross over frequency, that is:

$$F_O = \sqrt{F_{P2} \times F_{Z2}} \quad \text{---(27)}$$

Suppose θ_{MARGIN} is the desired phase margin and 60° is typical value. Parameter ϕ is the phase of power stage at zero crossover frequency. The required phase boost from PID compensator is set by:

$$\theta_{MAX} = \theta_{MARGIN} - \phi \quad \text{---(28)}$$

Because $\phi \cong 0$ and $\theta_{MAX} \cong \theta_{MARGIN}$.

The second zero of PID compensator can be calculated by:

$$F_{Z2} = F_O \times \sqrt{\frac{1 - \text{Sin}\theta_{MAX}}{1 + \text{Sin}\theta_{MAX}}} \quad \text{---(29)}$$

The second pole of compensator is given by:

$$F_{P2} = F_O \times \sqrt{\frac{1 + \text{Sin}\theta_{MAX}}{1 - \text{Sin}\theta_{MAX}}} \quad \text{---(30)}$$

The other zeroes and poles of compensator can be set by:

Select F_{Z1} by $F_{Z1}<F_{Z2}$ and $F_{Z1}<F_{PO}$ ---(31)

$$F_{P3} = F_S/2 \quad \text{---(32)}$$

The zero crossover frequency is determined by the following:

$$C_{f3} = \frac{2\pi \times F_O \times L \times C_{OUT}}{R_{C1}} \times \frac{V_{OSC}}{V_{IN}} \quad \text{---(33)}$$

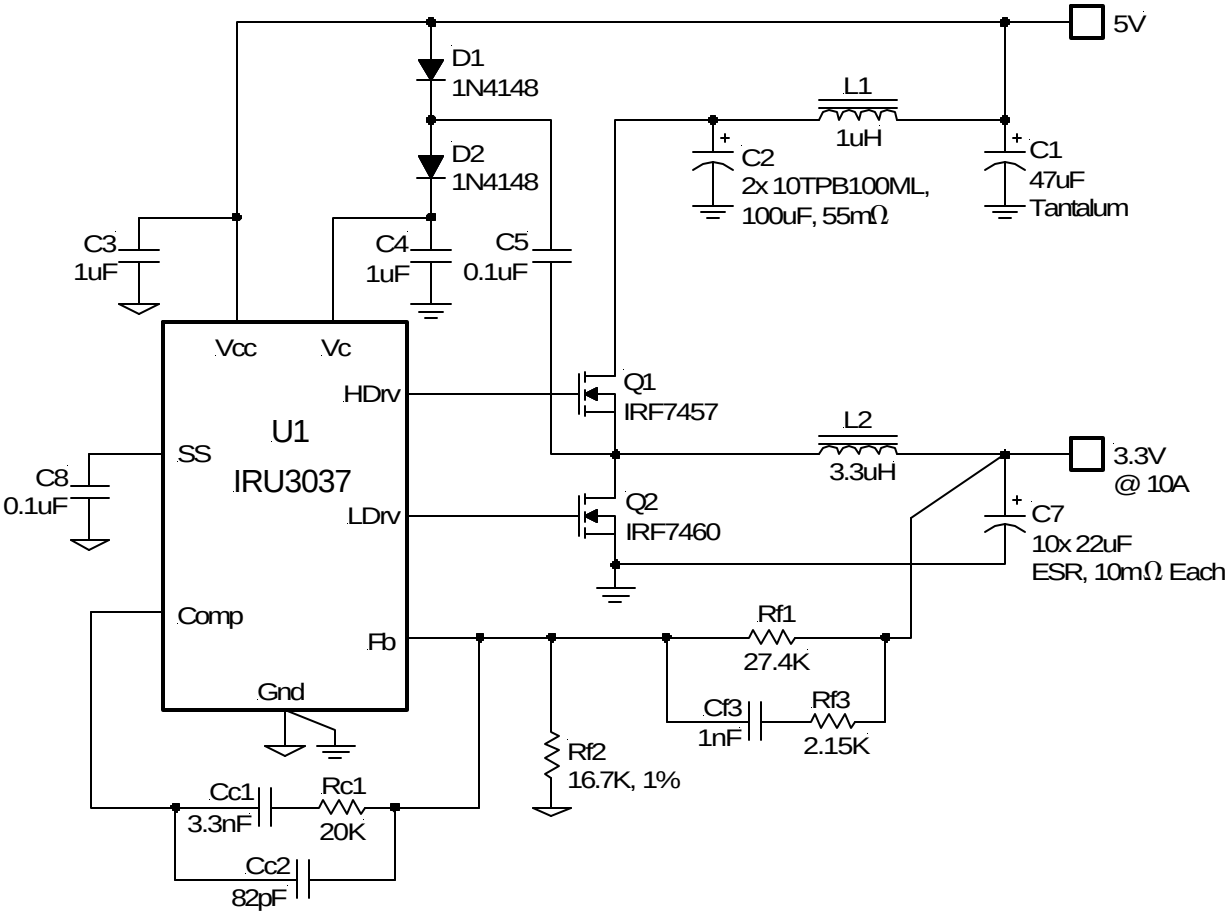

Figure 14 - Example of IRU3037 controlled buck converter with ceramic capacitors and PID compensator method B.

5.5) Design Example of IRU3037 with Ceramic Capacitor and PID Compensator Method B

Step 1 - Collect system parameters in Figure 14 and determine switching frequency. Comparing with section 4.2 output capacitor is 10 ceramic cap with 22μF, 10mΩ ESR. Total capacitance is:

$C_{OUT} = 10 \times 22\mu F = 220\mu F$

$ESR = 10m\Omega/10 = 1m\Omega$

Step 2 - Determine the power stage poles and zeros.

$$F_{PO} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{PO} = \frac{1}{2\pi \times \sqrt{3.3\mu H \times 220\mu F}} \cong 5.9Hz$$

$$F_{ZO} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

$$F_{ZO} = \frac{1}{2\pi \times 1m\Omega \times 220\mu F} \cong 723KHz$$

Step 3 - Determine the zero crossover frequency and compensation type. Select zero crossover frequency as:

$$F_O = \frac{f_S}{10} = \frac{200KHz}{10} = 20KHz$$

Because $F_{PO} < F_O < f_S/2 << F_{ZO}$, we select the PID compensation based on lead lag (method B).

Step 4 - Determine the desired location of zeros and poles for PID compensator. The desired phase margin is:

$\theta_{MAX} \cong \theta_{MARGIN} = 60°$

Then:

$$F_{Z2} = F_O \times \sqrt{\frac{1 - Sin\theta_{MAX}}{1 + Sin\theta_{MAX}}} \cong 5.36KHz$$

$$F_{P2} = F_O \times \sqrt{\frac{1 + Sin\theta_{MAX}}{1 - Sin\theta_{MAX}}} \cong 74KHz$$

Select $F_{Z1} < F_{Z2}$ and $F_{Z1} < F_{PO}$

Select $F_{Z1} = 0.5 \times F_{Z2} = 0.5 \times 5.36KHz \cong 2.68KHz$

Select $F_{P3} = f_S/2 = 100KHz$

Step 5 - Calculate the real parameters-resistor and capacitors of compensator. Select R_{C1}:

$R_{C1} >> 2/g_m = 2/0.6\mu mho \cong 3.3K$

Select $R_{C1} = 20K$

Calculate:

$$C_{C1} = \frac{1}{2\pi \times F_{Z1} \times R_{C1}} = \frac{1}{2\pi \times 2.68KHz \times 20K} \cong 3nF$$

Select $C_{C1} = 3.3nF$

Calculate:

$$C_{C2} = \frac{1}{2\pi \times F_{P3} \times R_{C1}} = \frac{1}{2\pi \times 100KHz \times 20K} \cong 80pF$$

Select $C_{C2} = 82pF$

Calculate C_{f3} based on location of zero crossover frequency:

$$C_{f3} = \frac{2\pi \times F_O \times L \times C_{OUT}}{R_{C1}} \times \frac{V_{OSC}}{V_{IN}}$$

$$C_{f3} = \frac{2\pi \times 20K \times 3.3\mu H \times 220\mu F}{20K} \times \frac{1.25V}{5V} \cong 1.14nF$$

Select $C_{f3} = 1nF$

Calculate:

$$R_{f3} = \frac{1}{2\pi \times C_{f3} \times F_{P2}} = \frac{1}{2\pi \times 1nF \times 74KHz} \cong 2.15K$$

Select $R_{f3} = 2.15K$

Calculate:

$$R_{f1} = \frac{1}{2\pi \times C_{f3} \times F_{Z2}} - R_{f3}$$

$$R_{f1} = \frac{1}{2\pi \times 1nF \times 5.36KHz} - 2.15K \cong 27.5K$$

Select $R_{f1} = 27.4K$, 1%

For DC regulation, calculate:

$$R_{f2} = \frac{V_{REF}}{V_O - V_{REF}} \times R_{f1} = \frac{1.25}{3.3 - 1.25} \times 27.4K \cong 16.7K$$

Select $R_{f2} = 16.7K$, 1%

Check:

$R_{f1} \| R_{f2} \| R_{f3} = 27.5K \| 16.7 \| 2.15K \cong 1.8K$

$R_{f1} \| R_{f2} \| R_{f3} > 1/g_m = 1.6K$

Conclusion

The control loop design based on transconductance amplifier is proposed for buck converter. For most of buck converter with electrolytic capacitor and low performance tantalum capacitors, a simple type II (PI) compensator can be employed. For ceramic output capacitors, a type III or PID compensator is usually required. Although IRU3037 controlled circuits are taken as an example in this application note, the proposed design method also applies to other IC applications such as IRU3046 or IRU3055 controlled multi-phase buck converters.

References

[1] D. Maksimovic, R. Erickson, “Advances in Averaged Switch Modeling and Simulation” 2.4MB slides from 3 hour tutorial seminar presented at the IEEE Power Electronics Specialists Conference, June 1999, Charleston, South Carolina.

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