Power Integrity

February 14, 2017

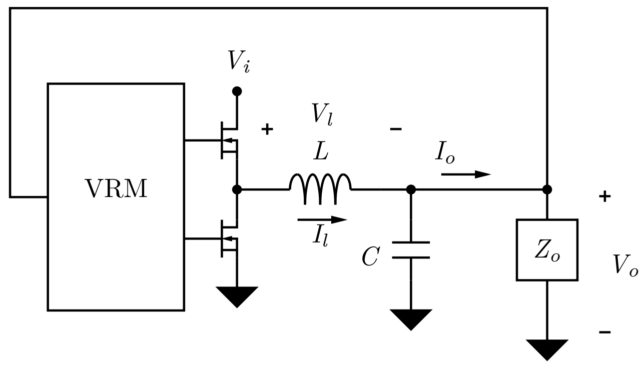

Figure 0.1: System Block Diagram

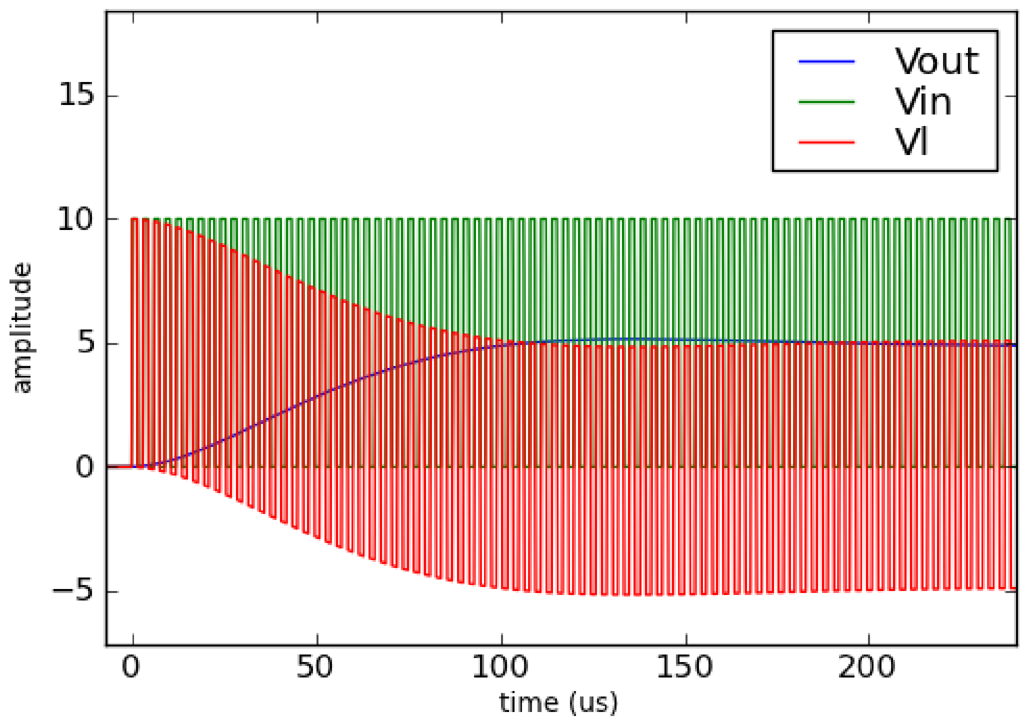

Figure 0.2: Startup Voltages

0.1 Introduction

A simplified block diagram of a switched-mode power supply is shown in Figure 0.1 on page 1. This block diagram is of a "buck" converter configuration, so called because the system produces a regulated voltage V_o which is lower than the input voltage V_i. Other configurations are possible including "boost" configurations where the output voltage is higher than the input voltage, along with combinations ("buck-boost") and flyback configurations that provide isolated outputs. The

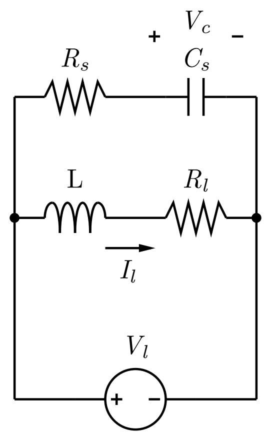

Figure 0.3: Inductor Current Sense Circuit

analysis of all configurations is similar as they are rearrangements of the inductor location and sometimes include a transformer.

In this simplified configuration, the input voltage is switched on and off with a given duty cycle. When the top FET switches on, the input voltage is connected directly to the inductor. Since the inductance is very large, current increases nearly linearly, building up a magnetic field in the inductor. When the top FET switches off, current wants to continue flowing and the bottom FET switches on allowing the current to continue through the inductor. At this point, the current decreases nearly linearly discharging into the bulk capacitance and the load. At startup, the voltage across the inductor during the top FET on time is approximately V_i, and the output voltage V_o is nearly zero, but as the system reaches steady state, V_o approaches a voltage that is proportional to V_i based on the switching duty cycle. In steady state, the voltage across the inductor alternates between the positive and negative difference between the steady state output voltage and the input voltage and the inductor current is nearly steady and is nearly equal to the load current.

Typically, the output voltage is fed back to the voltage regulation module (VRM) and the duty cycle is regulated based on observations of the output voltage. Thus, under dynamic conditions, the VRM modulates the duty cycle in order to supply more or less current to the load and to keep V_o as constant as possible.

In the analysis of switched-mode supplies, it is interesting to measure the input voltage, output voltage, inductor current, and load current in order to understand the dynamics of the supply.

0.2 Measurement of Inductor Current

A standard way of measuring the inductor current is shown in 0.3. Analyzing this circuit, we have:

$$I_l = \frac{V_l}{s \cdot L + R_l} = \frac{\frac{V_l}{L}}{s + \frac{R_l}{L}}$$

$$V_{cs} = \frac{V_l}{R_s + \frac{1}{C_s \cdot s}} \cdot \frac{1}{C_s \cdot s} = \frac{\frac{V_l}{R_s \cdot C_s}}{s + \frac{1}{R_s \cdot C_s}}$$

Therefore, the inductor current relative to the voltage across C_{cs} is:

$$\frac{I_l}{V_{cs}} = \frac{s + \frac{1}{R_s \cdot C_s}}{s + \frac{R_l}{L}} \cdot \frac{R_s \cdot C_s}{L}$$

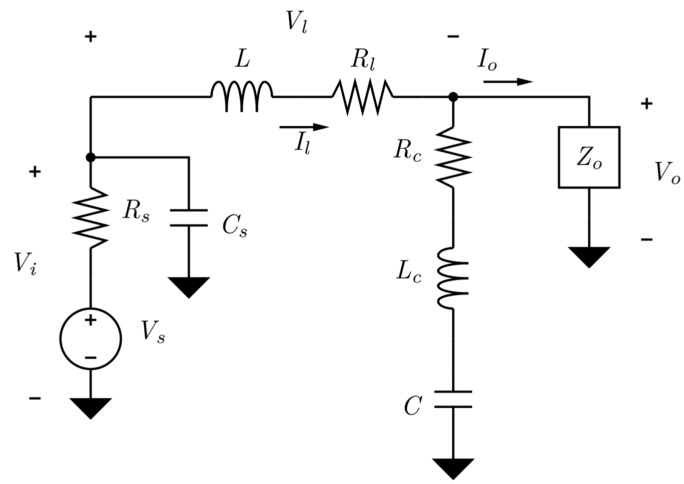

Figure 0.4: System Equivalent Circuit

Ideally, we have:

$$\frac{R_l}{L} = \frac{1}{R_s \cdot C_s}$$

or:

$$C_s = \frac{L}{R_l \cdot R_s}$$

The DC gain is:

$$G = \frac{R_s \cdot C_s}{L} = \frac{1}{R_l}$$

A reasonable set of values would be an inductance of $220\,\mu H$ and the series inductor resistance of $R_l = 1\,m\Omega$. The product of the sense resistor R_s and the sense capacitor C_s is therefore:

$$R_s \cdot C_s = \frac{L}{R_l} = 0.22$$

Thus, for a sense resistance of $R_s = 1\,M\Omega$, we have a sense capacitor of $220\,nF$. Unfortunately, the DC gain is:

$$G = \frac{1}{R_l} = 1000$$

Ideally, we can find another way of making this measurement.

0.3 Processing

In this section, we endeavor to try to calculate the important measurements V_l, I_l, and I_o from two single-ended measurements V_i and V_o. In order to do this, we consider the equivalent circuit in Figure 0.4 on page 3. Here we have included numerous parasitics including the on-resistance and capacitance of the drive circuit R_s and C_s[1], the series resistance in the inductor R_l and the series

[1]Note that these are not the same R_s and C_s from last section

resistance and inductance of the capacitor R_c and L_c. For now, we consider the load as an unknown quantity Z_o.

Computation of I_l

Considering the current across the inductor, we solve:

$$I_l(s) = \frac{V_i(s) - V_o(s)}{s \cdot L + R_l} = \frac{V_l(s)}{s \cdot L + R_l}$$

We note that V_l is simply the difference between V_i and V_s. In sampled systems, we use the approximation of the derivative that lets us convert from the Laplace transform to the z transform:

$$s \approx \frac{1}{T} \cdot \left(1 - z^{-1}\right)$$

Making the substitution, we have:

$$I_l(z) = \frac{V_l(z)}{\frac{L}{T} \cdot (1 - z^{-1}) + R_l} = \frac{V_l(z)}{\left(\frac{L}{T} + R_l\right) - \frac{L}{T} \cdot z^{-1}} = \frac{V_l(z)}{\left(\frac{L + R_l \cdot T}{T}\right) - \frac{L}{T} \cdot z^{-1}}$$

$$I_l(z) = \frac{T}{L + R_l \cdot T} \left(V_l(z) + \frac{L}{T} \cdot z^{-1} \cdot I_l(z)\right) = \frac{T}{L + R_l \cdot T} \cdot V_l(z) + \frac{L}{L + R_l \cdot T} \cdot z^{-1} \cdot I_l(z)$$

Taking the inverse z transform, we obtain the difference equation of the inductor current with respect to the voltage across the inductor.

$$I_l[k] = \frac{T}{L + R_l \cdot T} \cdot V_l[k] + \frac{L}{L + R_l \cdot T} \cdot I_l[k-1]$$

The transfer function that produces the inductor current from the inductor voltage is:

$$H_l(z) = \frac{I_l(z)}{V_l(z)} = \frac{\frac{T}{L + R_l \cdot T}}{1 - \frac{L}{L + R_l \cdot T} \cdot z^{-1}} = \frac{T}{L + R_l \cdot T} \cdot \frac{1}{1 - \frac{L}{L + R_l \cdot T} \cdot z^{-1}} = \frac{T}{L + R_l \cdot T} \cdot \frac{z}{z - \frac{L}{L + R_l \cdot T}} \quad (1)$$

When $L \gg R_l \cdot T$:

$$H_l(z) \approx \frac{T}{L} \cdot \frac{1}{1 - z^{-1}}$$

which means that:

$$I_l(t) \approx \frac{1}{L} \int V_L(t) \cdot dt$$

Returning to the transfer function for $H_l(z)$ in (1), we have the DC gain of the function as:

$$G = \left. \frac{T}{L + R_l \cdot T} \cdot \frac{z}{z - \frac{L}{L + R_l \cdot T}} \right|_{z=1} = \frac{T}{L + R_l \cdot T} \cdot \frac{1}{1 - \frac{L}{L + R \cdot T}} = \frac{1}{R_l}$$

It turns out that the series R_l is very important, because without it, the computation will diverge.

For nonzero R_l, we prefer to take the gain outside of the filter computation, making the new transfer function:

$$H_l(z) = \frac{1}{R_l} \cdot \frac{R_l \cdot T}{L + R_l \cdot T} \cdot \frac{1}{1 - \frac{L}{L + R_l \cdot T} \cdot z^{-1}} \quad (2)$$

and the new difference equation:

$$R_l \cdot I_l[k] = \frac{R_l \cdot T}{L + R_l \cdot T} \cdot V_l[k] + \frac{L}{L + R_l \cdot T} \cdot I_l[k-1] \tag{3}$$

In practical applications, R_l is very small (on the order of $1\, m\Omega$. With an inductance of $L = 220\, \mu H$, and a sample rate of $10\, MS/s$, $(T = 100\, ns)$, we would have a pole location at:

$$\frac{L}{L + R_l \cdot T} = \frac{220\, \mu}{220\, \mu + .001\, \mu \cdot .1\, \mu} = \frac{220}{220 + .0001} = 0.9999995455$$

This pole so close to unity can be very problematic in filtering and will require very long filter startup times and will require processing techniques to guess the starting point of I_l similar to what we need to do in clock recovery in serial data processing.

Computation of I_o:

Given the inductor current I_l, we solve for the current away from the voltage node V_o

$$-I_l(s) + \frac{V_o(s)}{\frac{1}{C \cdot s}} + I_o(s) = 0$$

$$I_o(s) = I_l(s) - C \cdot s \cdot V_o(s)$$

Again, we use the approximation of the derivative that lets us convert from the Laplace transform to the z transform:

$$s \approx \frac{1}{T} \cdot \left(1 - z^{-1}\right)$$

$$I_o(z) = I_l(z) - \frac{C}{T} \cdot \left(1 - z^{-1}\right) \cdot V_o(z)$$

$$I_o[k] = I_l[k] - \frac{C}{T} \cdot (V_o[k] - V_o[k-1])$$

Alternate computation with more parasitics

With the full set of parasitics inserted, we have:

$$-I_l(s) + \frac{V_o(s)}{\frac{1}{C \cdot s} + s \cdot L_c + R_c} + I_o(s) = 0$$

We define:

$$A = \frac{T^2}{T^2 + L_c \cdot C + R_c \cdot C \cdot T}$$

and have the difference equation:

$$\begin{aligned} I_o[k] = I_l[k] + -C \cdot A \cdot \frac{2 \cdot L_c + R_c \cdot T}{T^2} \cdot I_l[k-1] + \frac{L_c \cdot C}{T^2} \cdot A \cdot I_l[k-2] + \ldots \\ \ldots + C \cdot A \cdot \frac{2 \cdot L_c + R_c \cdot T}{T^2} \cdot I_o[k-1] + -\frac{L_c \cdot C}{T^2} \cdot A \cdot I_o[k-2] + \ldots \\ \ldots + -\frac{C}{T} \cdot A \cdot V_o[k] + \frac{C}{T} \cdot A \cdot V_o[k-1] \end{aligned} \tag{4}$$

$$A = \frac{T^2}{T^2 + L_c \cdot C + R_c \cdot C \cdot T}$$

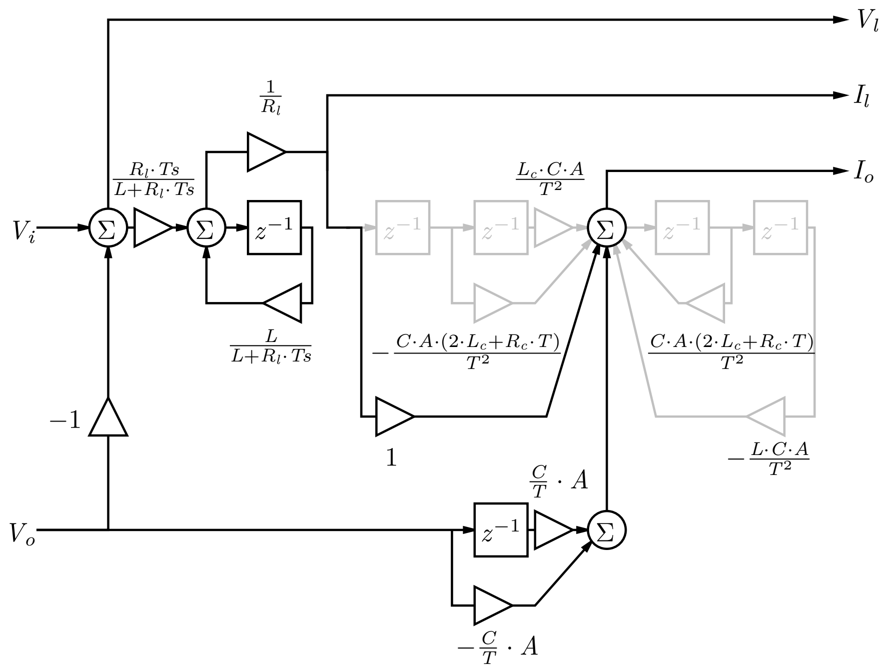

Figure 0.5: Processing Block Diagram

It is comforting to find that if $L_c = R_c = 0$, then $A = 1$, and we have:

$$I_o[k] = I_l[k] + -\frac{C}{T} \cdot V_o[k] + \frac{C}{T} \cdot V_o[k-1]$$

In any case, the full processing system that produces all of the desired output waveforms is provided in Figure 0.5 on page 6. Here we have grayed out the processing that is a function of the nonzero parasitics for the capacitor R_c and L_c to simplify the understanding.

0.4 Power Integrity Solutions

Given the processor in Figure 0.5 on page 6, one could imagine a simple signal integrity solution for the scope centered around this kind of processing:

- Given V_i and V_o, it should be possible to determine the closed loop transfer function and the transfer function of the control loop.
  - And if the control loop can be broken (i.e. connecting the voltage sense circuit to a constant voltage so the converter runs open loop), we can separate the slower control loop portion from the dynamic response of the regulation circuit alone.
- Given V_o and I_o we can find Z_o, or the ac impedance of the load.
- Given V_l and I_l we can find the ac source impedance.

- Given V_i and V_o, it is my hope to be able to perform some sort of system identification that can allow us to characterize the parasitic portion of the inductor portion of the circuit - in any case, we will probably need some form of calibration of the system to avoid divergence of the measurement waveforms.

Some things that I'm suspicious of is whether slight DC offsets and DC inaccuracies will cause measurement problems. I don't think noise and such will be such an issues. Also, the very long time-constants will be some sort of issue for sure and I'm wondering how mis-estimates or measurements of the parasitics will cause problems.

Many of the dynamic measurements would benefit from some sort of stimulus to the load to induce variations (ideally in load current). If the processing can be performed satisfactorily, we would not need to precisely control the stimulus as we would be measuring the effects, but might need some method of controlling the magnitude of the stimulus and certainly in attaching it to the circuit.

0.5 Errors in Measurements of I_l

This section calculates how noise in measurements of V_l translate into noise in the calculation of I_l as put forth in 0.3.

Given $N+1$ discrete frequency bins in a frequency response, the noise in each bin is calculated as, for $n \in 0 \ldots N$:

$$\mathcal{N}[n] = \frac{VDIV \cdot 2 \cdot 10^{-\frac{SNR}{20}}}{L \cdot \sqrt{N} \cdot \pi \cdot f[n]}$$

where $VDIV$ is the volt/division setting of the oscilloscope at which the voltages V_i and V_o are measured, SNR is the signal-to-noise ratio of the oscilloscope at that volt/division setting, L is the inductance, and $f[n]$ is the frequency of the bin according to:

$$f[n] = \frac{n}{N} \cdot \frac{Fs}{2}$$

where Fs is the sample rate.

Thus, to make a $K = 2 \cdot N$ element time-domain signal with these noise characteristics :

$$A[n] = \mathcal{N}[n] \cdot \begin{cases} \sqrt{2} & n > 0 \\ 1 & otherwise \end{cases}$$

$$X[n] = A[n] \cdot \begin{cases} \frac{1}{2} \cdot e^{j \cdot \mathrm{rnd}(2 \cdot \pi)} & 0 < n < N \\ 1 & otherwise \end{cases}$$

for $n' \in 1 \ldots N-1$:

$$X[N+n'] = X[N-n']^*$$

for $k \in 0 \ldots K-1$:

$$x[k] = \frac{1}{K} \sum_{n=0}^{K-1} X[n] \cdot e^{j \cdot \frac{n \cdot k}{K}}$$

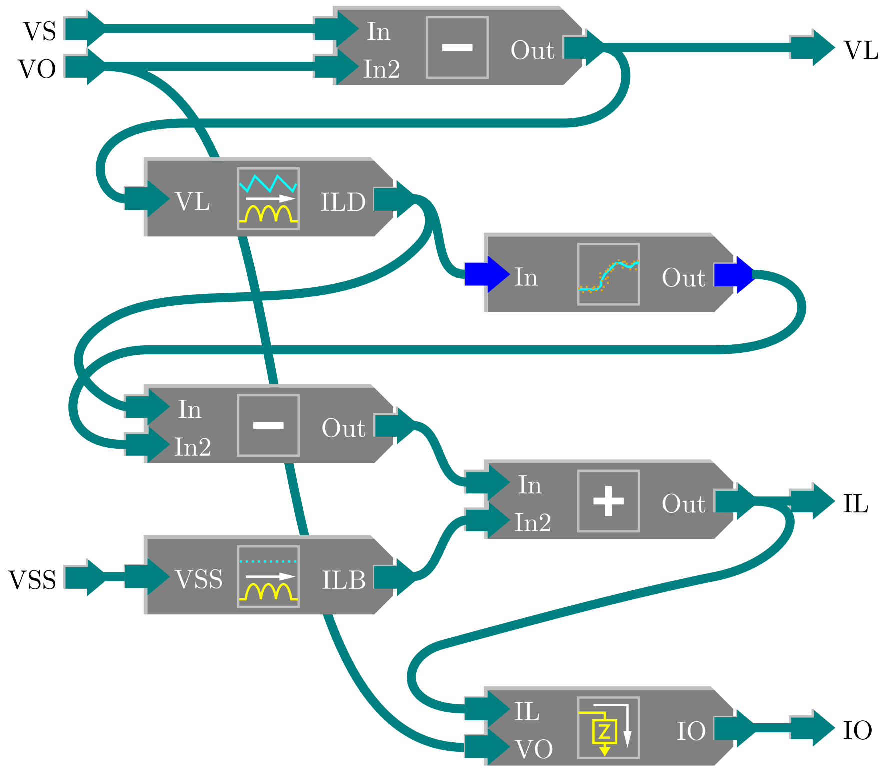

Figure 0.6: Power Integrity Scope Processing

0.6 Processing

In Figure 0.6 on page 8 we see a processing web setup to perform the desired power integrity measurements. Specifically, the processing takes in three voltage waveforms:

- VS - the voltage at the switch (the voltage at the input to the inductor). This voltage waveform should be arranged such that it maximizes the vertical scale of the scope, but does not go offscreen.
- VO - the voltage at the output (the voltage at the output side of the inductor). This voltage waveform should be arranged such that under all conditions (including transient conditions, the waveform does not go offscreen. It should include zero volts.
- VSS - the voltage at the switch overdriven into the scope such that bottom portion of the switch voltage is onscreen where it settles after the overdrive recovery. The top portion of this waveform will be far offscreen above.

The output of this processing is three waveforms:

- VL - the voltage across the inductor, formed as a simple subtraction: $VL = VS - VO$.
- IL - the current through the inductor.
- IO - the current into the load.

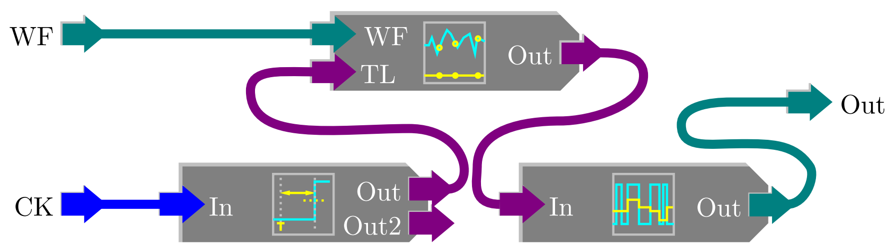

Figure 0.7: *WaveformSampler* Composite Processor Internals

Optionally, we might want to provide power waveforms formed by taking the product of VO and IO and VS and IL, but that is simple processing.

The key complexity here is the computation of IL. The first part of the processing forms the *dynamic* inductor current ILD. This is performed by applying the difference equation in (3). Typically, because of small R_l, this will perform much like an integrator on V_l. The output will tend to look like a sawtooth current waveform. Because of integration, it will highly amplify very low frequency noise and the waveform will have a low frequency wander in it. This amplification can be seen by the DC gain $1/R_l$, where R_l tends to be very small. Therefore, the wander is removed by subtracting a smoothed waveform from the ILD waveform output. The result is the sawtooth current waveform with the wander removed.

To restore the baseline inductor current, the overdriven waveform VSS is supplied to a processor that produces the per-cycle baseline current ILB. This production of the baseline inductor current is provided in 0.6. The baseline inductor current is added to the sawtooth dynamic current and output as IL.

Using the waveforms VO (supplied) and the computed IL, the output current IO is produced by a processor that implements the difference equation in (4).

WaveformSampler

The *WaveformSampler* processor is a composite processor. It has two inputs:

- WF - the waveform to sample
- CK - the clock waveform

It has a single output - the sampled waveform.

It consists internally of three processors:

- A *Time@Level* processor
- A *WaveformSamplerInternal* processor
- A *TrackOfParameter* processor

The internals of the *WaveformSampler* processor are shown in Figure 0.7 on page 9. The *Time@Level* processor determines the locations of clock edges on the clock waveform based on specified polarity, threshold, and hysteresis values programmed and passes these values to the TL input of the *WaveformSamplerInternal* processor. The *WaveformSamplerInternal* processor then interpolates values on the waveform supplied at the clock edge times supplied and outputs parameter values that are the coordinates of the sampled waveform where the x ordinate is the clock edge time and the y ordinate is the value of the waveform at that time. The *TrackOfParameter* processor is utilized to turn the parameter values back into a waveform representing the sampled waveform. The track produces a waveform with the same sample locations as the supplied waveform to the *WaveformSampler*.

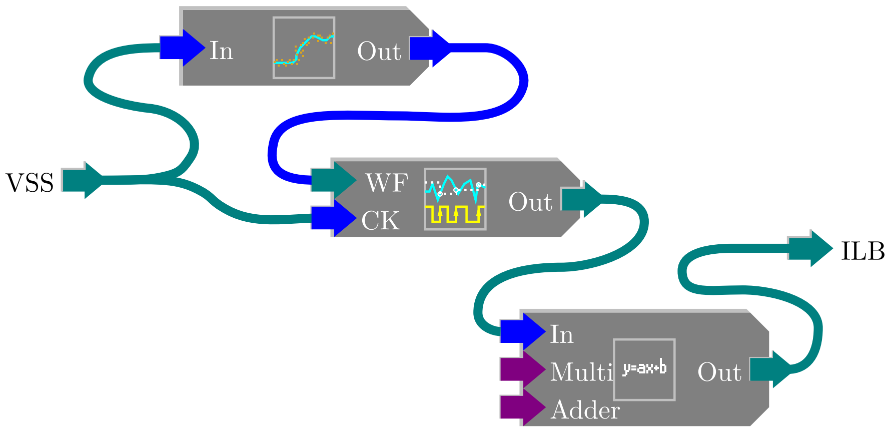

Figure 0.8: *InductorBaselineCurrent* Composite Processor Internals

InductorBaselineCurrent

The *InductorBaselineCurrent* processor is a composite processor. It has one input: VSS - The voltage at the switch (saturated). This is the switch voltage severely overdriven but showing the switch on voltage on the screen. It has one output: ILB - The inductor baseline current.

The processor consists internally of three processors:

- An *Eres* processor
- A *WaveformSampler* processor
- A *Rescaler* processor

The internals of the *InductorBaselineCurrent* processor are shown in Figure 0.8 on page 10.

The baseline current is defined as the average inductor current over one cycle of the switched voltage waveform. It is used to augment the inductor dynamic current defined by dynamic voltage across the inductor. The inductor baseline current is calculated by sampling a smoothed version of the over-driven switch voltage somewhere around the middle to the end of the switch voltage cycle. Since this essentially a per-cycle measurement of the voltage drop across the FET switch when the switch is connected to ground, the inductor current is proportional to this voltage. Therefore, the *Rescaler* processor is utilized to provide the gain and offset for such a conversion, and to supply the new units of Amps. The gain and offset in the rescaler will need to be determined through some sort of calibration step.

Outline of PowerIntegrity Offering

In Figure 0.9 on page 11, we have a block diagram showing the location of various power integrity measurements. In this diagram, there are several voltages that will be probed by the oscilloscope and transient current generation circuitry delivered with an AWG.

The voltages being measured are:

- V_{in} the input voltage to the system - in a buck converter typically a large voltage like 10-20 V.
- V_{out} the output voltage - this is the voltage that the VRM module is regulating to. Usually this is small, like 1-3 V. Knowing the static resistance R_{static} along with V_{out} allows us to know the static DC load current I_{static}.
- V_{sw} the switch-node voltage. This voltage swings nominally between ground and V_{in}.
- V_t the transient resistor voltage. Knowing the transient resistor value R_t allows this to be a proxy for the transient current I_t.
- V_{cs} this shunt capacitance voltage. This voltage across an RC network (R_s and C_s) added to the system allows measurement of the inductor current I_L.

Transient Current

The transient current (which might be a DC current added to the static DC load current) is calculated based on voltage measurement V_t and knowledge of R_t as:

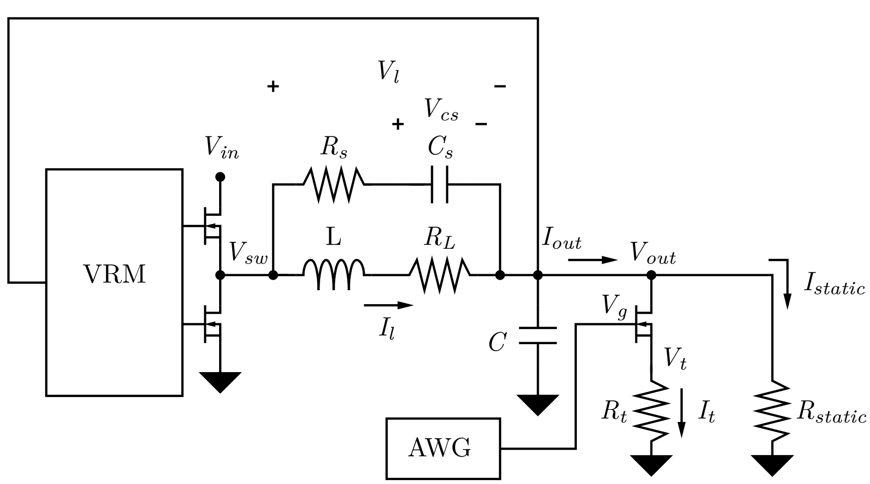

Figure 0.9: Power Integrity Measurements Circuit

$$I_t = \frac{V_t}{R_t}$$

Static Load Current

The static load current is defined as the output current when the transient current is zero and is based on the voltage measurement V_{out} and knowledge of R_{static} as:

$$I_{static} = \frac{V_{out}}{R_{static}}$$

Output Current

The output current is calculated based on voltage measurements V_t and V_{out} and specification or calibration of R_{static} and R_t as:

$$I_{out} = I_{static} + I_t = \frac{V_t}{R_t} + \frac{V_{out}}{R_{dc}}$$

Transient Current Generation

Transient current is generated by applying voltage to the gate of the transient FET V_g. This must be calibrated in some manner, preferably by sweeping the gate voltage between a minimum and maximum gate voltage value by a specified step size. Ideally, the data is fit somehow to something like splines that allow the determination of V_g as a function of desired I_t or I_{out} (with nominal V_{out}) and vice versa.

Inductor Current Measurement Probe

After all the work done here, I believe that the best and easiest way to measure the inductor current is with the RC measurement method. This is a series RC in parallel with the inductor. In theory, the RC time constant is matched to the L/R time constant of the inductor and its parasitic resistance. There are several problems with this that need to be addressed:

1. We will need some configurability of either or both the R and the C (need to work out details).
2. We will need to deal with lead inductance of the wires connecting the two sides of the inductor. (I believe that this is theoretically done by picking large C values along with the R that matches the RC time constant).
3. There is significant pickup from the inductor. I have an idea for dealing with this.
4. In the end, the gain that needs to be supplied is $1/R_L$ where R_L is the parasitic series resistance. This can be very small leading to large gain required in the probe. I think we want some active gain here.
5. Despite all this, the probe will need to be calibrated with each inductor, because it is not the absolute RC that must be known, but also the L and R of the inductor.
6. Istvan thinks inductor linearity can be an issue.

It turns out that this probe must touch down on two important locations in the circuit:

- The switch node voltage.

- The output node.

So, although the measurement is taken differentially across the capacitor, the two connection points are important locations to monitor. I could imagine the circuit board that goes between the differential probe and the two sides of the inductor also contain probing locations for attachment of passive probes.

To figure out the R and C configuration, we need to know the ranges of L and R_L that need to be supported (with ideally, one a function of the other to minimize possibilities).

$$\min\left(L\right)/\max\left(R_L\right) = \min\left(R \cdot C\right)$$

$$\max\left(L\right)/\min\left(R_L\right) = \max\left(R \cdot C\right)$$

$$R \in 1 \ldots 2\,k\Omega$$

$$C \in .01, .1, 1, 10\,\mu F$$

Inductor Current Swing

Actuall, using KVL around the loop, considering the initial conditions of the current through the inductor, we have:

$$-\frac{V_L}{s} + I_L \cdot R_L + I_L \cdot s \cdot L - L \cdot I_{L0} = 0$$

or:

$$I_L\left(s\right) = \frac{\frac{V_L}{s} + L \cdot I_{L0}}{s \cdot L + R_L}$$

$$I_L\left(t\right) = \mathscr{L}^{-1}\left(\frac{\frac{V_L}{s} + L \cdot I_{L0}}{s \cdot L + R_L}\right) = \frac{V_L}{R_L} \cdot \left(1 - e^{-\frac{R_L}{L} \cdot t}\right) + I_{L0} \cdot e^{-\frac{R_L}{L} \cdot t}$$

$$\lim_{R_L \to 0}\left[I_L\left(t\right)\right] = \frac{V_L}{L} \cdot t + I_{L0}$$

for $\frac{R_L}{L} \cdot t$ small, we use $e^{-x} \approx 1 - x$ for small x:

$$I_L\left(t\right) \approx I_{L0} + \frac{1}{L} \cdot \left(V_L - R_L \cdot I_{L0}\right) \cdot t$$

These equations basically say that we start a portion of the cycle with an inductor current I_{L0} and the inductor current changes mostly linearly with a slope V_L/L until the voltage across the inductor V_L is switched. In steady state, the duty cycle D (in fraction of switching period T_{sw}) is the ratio of the output voltage V_{out} to the input voltage V_{in}. During the time in the cycle where $t \leq D \cdot T_{sw}$, the voltage across the inductor is $V_L = V_{in} - V_{out}$. During the time in the cycle where $t > D \cdot T_{sw}$, the voltage across the inductor is $V_L = -V_{out}$. Therefore, the amount that the inductor current swings during the on time is:

$$I_{Lswing} = \dots$$

$$\dots = [I_L(t) - I_{L0}] = \dots$$

$$\dots = \frac{V_L}{R_L} \cdot \left(1 - e^{-\frac{R_L}{L} \cdot t}\right) - I_{L0} \cdot \left(1 - e^{-\frac{R_L}{L} \cdot t}\right) \approx \dots$$

$$\dots \approx \frac{V_L}{L} \cdot t$$

During the on-time, we have:

$$I_{Lswing-on} \approx \frac{V_{in} - V_{out}}{L} \cdot \frac{V_{out}}{V_{in}} \cdot T_{sw}$$

During the off-time, we have:

$$I_{Lswing-off} \approx -\frac{V_{out}}{L} \cdot \left(1 - \frac{V_{out}}{V_{in}}\right) \cdot T_{sw}$$

And we find, as expected, that:

$$I_{Lswing-on} + I_{Lswing-off} = 0$$

Thus, we find that the inductor current consists of a DC component I_{LDC} which essentially equals the DC load current and a sawtooth waveform with duty cycle $D = V_{out}/V_{in}$, a period T_{sw} and a peak-peak swing of $I_{Lswing-on}$ centered about I_{LDC}.

Voltage Across Shunt Capacitor

Why the RC

We have the switch node switching between V_{in} and ground, and the output voltage wherever it is. Therefore, the voltage across the inductor, V_L is switching between $V_{in} - V_{out}$ and $-V_{out}$. When the switch is on, The voltage across the inductor $V_L = V_{in} - V_{out}$ and the current through the inductor builds by:

$$I_{LON} = V_{Linitial} + \frac{V_L}{}$$

Duty Cycle

The fractional duty cycle D must obey the following equation for a static DC current I_L:

$$\frac{1}{T_{sw}} \cdot \left[\int_0^{D \cdot T_{sw}} \frac{V_{in} - V_{out}}{L} \cdot dt - \int_0^{(1-D) \cdot T_{sw}} \frac{V_{out}}{L} \cdot dt\right] = I_L$$

This means:

$$D = \frac{V_{out} + I_L \cdot L}{V_{in}} \approx \frac{V_{out}}{V_{in}}$$

Inductor Current Swing

The inductor current swings up and down like a saw-tooth waveform. The peak-peak swing can be calculated as:

$$I_{Lpp} = \int_0^{D\cdot T_{sw}} \frac{V_{in} - V_{out}}{L} \cdot dt = \frac{D \cdot T_{sw}}{L} \cdot (V_{in} - V_{out})$$

Actually, the exact inductor current during the on time is:

$$\begin{aligned} I_{Lpp} = \mathscr{L}^{-1}\left((V_{in} - V_{out}) \cdot \frac{1}{s \cdot L + R_L} \cdot \frac{1}{s}\right)\Bigg|_{t=D\cdot T_{sw}} &= \ldots \\ \ldots = (V_{in} - V_{out}) \cdot \frac{1}{R_L} \cdot \left[1 - e^{-\frac{R_L}{L}\cdot D \cdot T_{sw}}\right] &\approx \ldots \\ \ldots \approx (V_{in} - V_{out}) \cdot \frac{1}{R_L} \cdot \left[\frac{R_L}{L} \cdot D \cdot T_{sw}\right] &= \ldots \\ \ldots = \frac{D \cdot T_{sw}}{L} \cdot (V_{in} - V_{out}) \end{aligned}$$

but, for small x:

$$1 - e^{-x} \approx x$$

Actuall, using KVL around the loop, considering the initial conditions of the current through the inductor, we have:

$$-\frac{V_L}{s} + I_L \cdot R_L + I_L \cdot s \cdot L - L \cdot I_{L0} = 0$$

or:

$$I_L(s) = \frac{\frac{V_L}{s} + L \cdot I_{L0}}{s \cdot L + R_L}$$

$$I_L(t) = \mathscr{L}^{-1}\left(\frac{\frac{V_L}{s} + L \cdot I_{L0}}{s \cdot L + R_L}\right) = \frac{V_L}{R_L} \cdot \left(1 - e^{-\frac{R_L}{L}\cdot t}\right) + I_{L0} \cdot e^{-\frac{R_L}{L}\cdot t}$$

$$\lim_{R_L \to 0} [I_L(t)] = \frac{V_L}{L} \cdot t + I_{L0}$$

for $\frac{R_L}{L} \cdot t$ small, we use $e^{-x} \approx 1 - x$ for small x:

$$I_L(t) \approx I_{L0} + \frac{1}{L} \cdot (V_L - R_L \cdot I_{L0}) \cdot t$$

Voltage Across Shunt Capacitor

The voltage across the shunt capactor swings up and down like a saw-tooth waveform. The peak-peak swing can be calculated as:

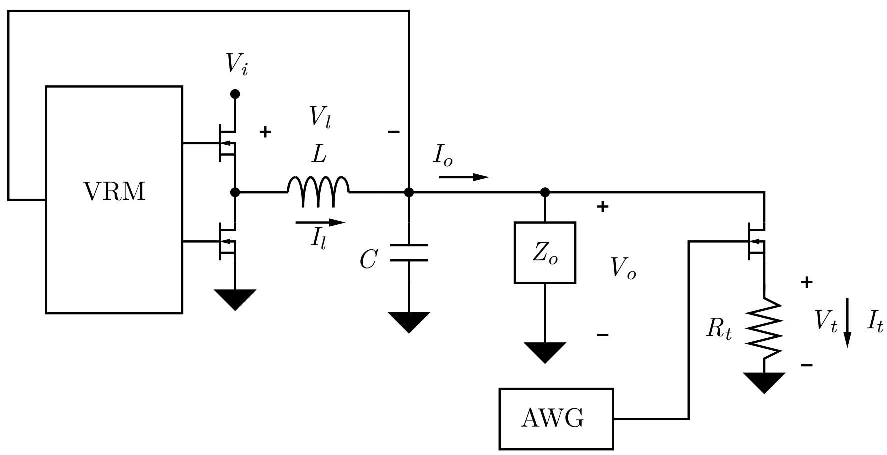

Figure 0.10: Output Impedance Measurement Setup

$$V_{cspp} = \mathscr{L}^{-1}\left[\left(V_{in} - V_{out}\right) \cdot \frac{1}{R_s + \frac{1}{C_s \cdot s}} \cdot \frac{1}{C_s \cdot s} \cdot \frac{1}{s}\right]\Bigg|_{t=D\cdot T_{sw}} = \dots$$

$$\left(V_{in} - V_{out}\right) \cdot \left[1 - e^{-\frac{1}{R_s \cdot C_s} \cdot t}\right] \approx \dots$$

$$\dots \approx \frac{D \cdot T_{sw}}{R_s \cdot C_s} \cdot \left(V_{in} - V_{out}\right)$$

Output Impedance Measurement

To measure the output impedance, we need:

1. A way to stimulate transient output current.
2. A way to measure the transient output current.
3. A way to measure the output voltage.

The block diagram showing how to perform this measurement is shown in Figure 0.10 on page 16 where we see a FET connected to the output in parallel with a static load Z_o. The FET is connected with the drain connected to the output node and the source connected to ground through a known resistance R_t. By driving the gate of the FET with an AWG, we are able to vary the drain-source resistance of the FET, thus allowing extra current draw. Because the resistance R_t is known, we can compute the transient current $I_t = V_t/R_t$. In order to calibrate the transient current source, we sweep DC levels at the gate of the FET and measure the transient current I_t, thus obtaining a transfer characteristic.

Many evaluation boards are instrumented with a transient generator. And even when they're not, one can be added to the board as shown in Figure 0.12 on page 17.

It's important to distinguish two types of transient generators typically on the boards that are used for different purposes. One type stimulates the feedback loop by either perturbing the measured, fed back output voltage or output current. This perturbation causes the servo system to react and in this way, it's possible to measure the loop transfer characteristics. This type of transient will not

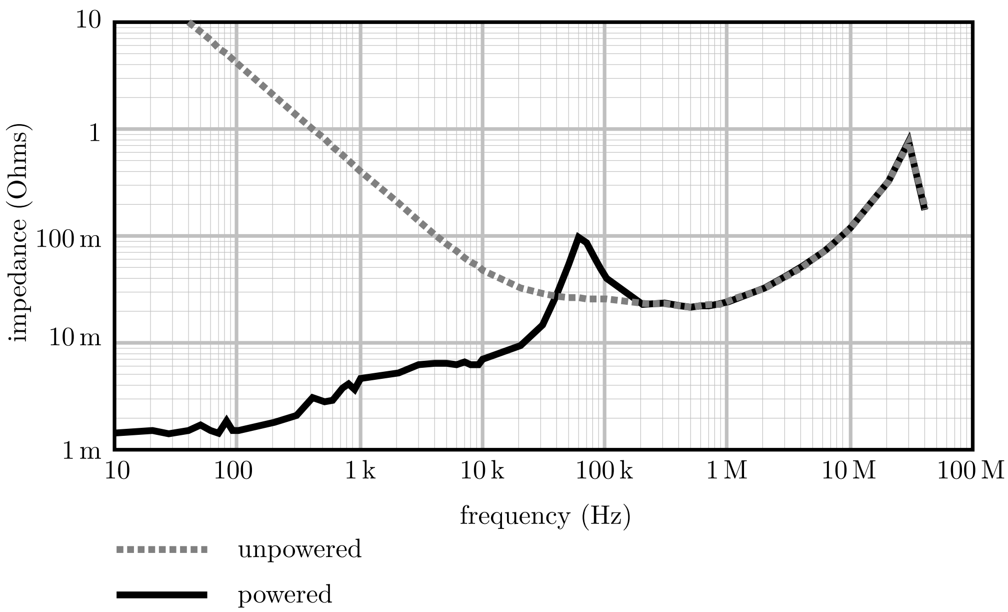

Figure 0.11: Output Impedance Measurement

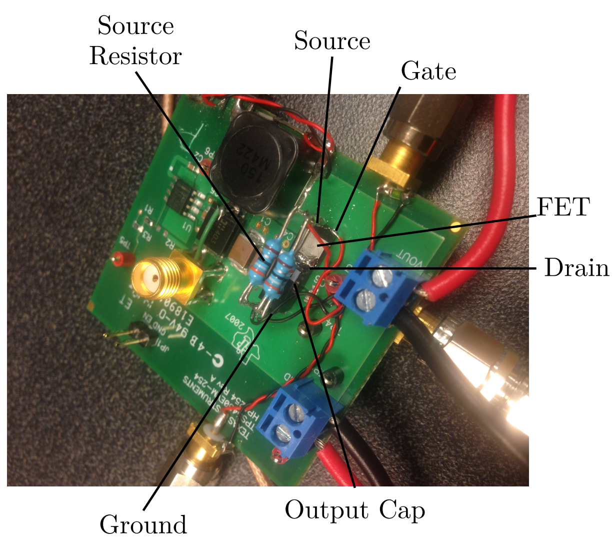

Figure 0.12: Transient FET Circuitry

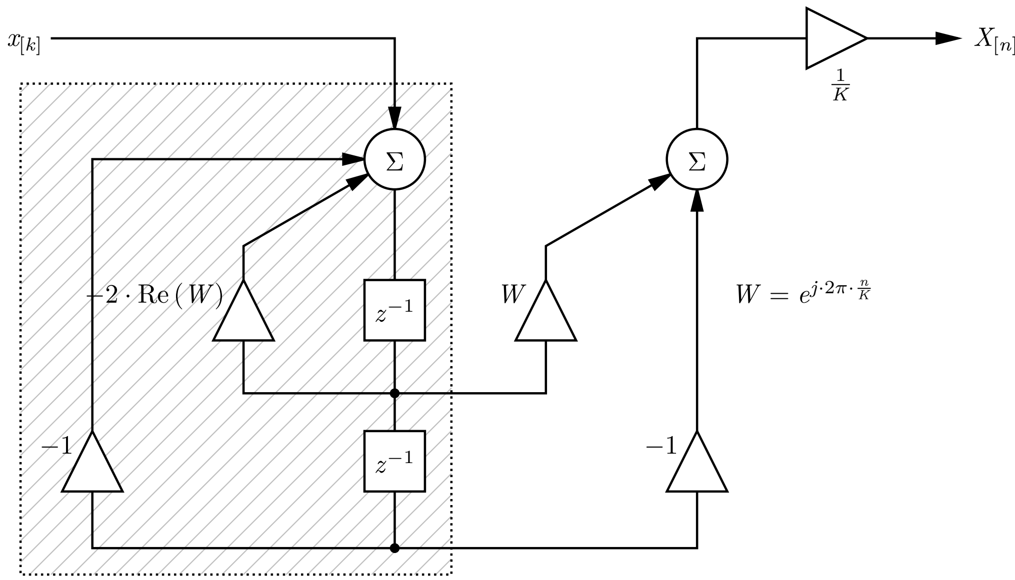

Figure 0.13: Goertzel Algorithm Implementation

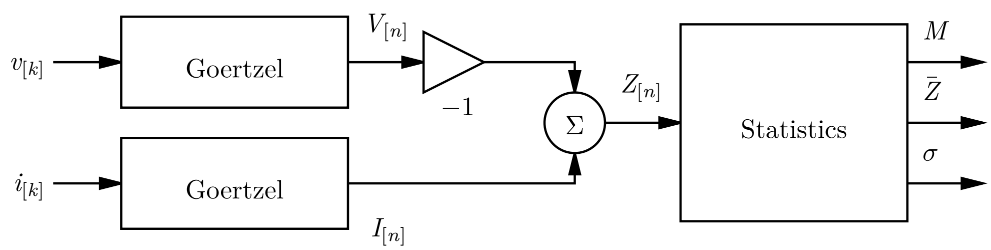

Figure 0.14: Output Impedance Processor Internals

be high frequency and will only be capable of stimulating the system within the bandwidth of the feedback system. The type of transient generator we are interested in is the kind that directly draws current from the output.

Our solution needs to provide programming of location and characteristics of output transient current generators. . Aspects of programming include:

- acceptable range of the gate voltage.
- value of the load resistance.
- pk-pk current desired for AC transient analysis.
- nominal load current desired (determines offset to gate voltage to set DC load current in conjunction with load resistance).
- (or even range of nominal load currents desired and step interval to generate shmoo plot).
- ability to calibrate current vs. gate voltage (or load the already calibrated transfer curve).

To sweep the

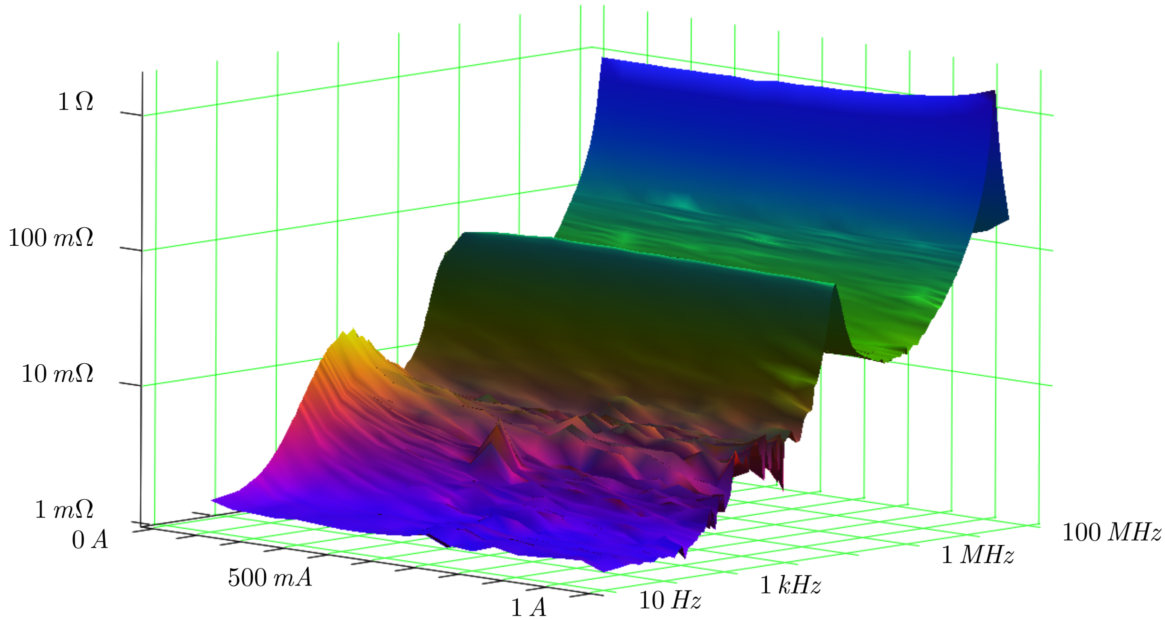

Figure 0.15: Output Impedance vs. Load Current

Statistics

Estimate of the standard deviation

For a population of n samples *taken from a normally distributed set* and a standard deviation of the samples calculated as s, the bounds on the standard deviation within a confidence interval of $P/100$ percent is given as, for $\alpha = 1 - P$:

$$\sqrt{\frac{(n-1)\cdot s^2}{\chi^2_{\frac{\alpha}{2}}}} \leq \sigma \leq \sqrt{\frac{(n-1)\cdot s^2}{\chi^2_{1-\frac{\alpha}{2}}}}$$

where χ^2_x is calculated for a number of degrees of freedom, $df = (n-1)^2$.[2]
Thus, the maximum standard deviation is given as:

$$\sigma_{max} = \sqrt{\frac{(n-1)\cdot s^2}{\chi^2_{1-\frac{\alpha}{2}}}}$$

Estimate of the mean

For a population of n samples and a known standard deviation of the samples σ, the bounds on the mean μ within a confidence interval of $P/100$ percent is given as, for $\alpha = 1 - P$:[3]

$$Z_{\frac{\alpha}{2}} \cdot \frac{\sigma}{\sqrt{n}} \leq \mu \leq Z_{1-\frac{\alpha}{2}} \cdot \frac{\sigma}{\sqrt{n}}$$

[2] note that in MathCad, χ^2_x for a given df is calculated as $\text{qchisq}(1-x, df)$

[3] note that in MathCad, Z_x is calculated as $\text{qnorm}(x, 0, 1)$

Worst case estimate of the mean

For a population of n samples *taken from a normally distributed set* and a standard deviation of the samples calculated as s, with a mean calculated as μ, the worst case bounds on the mean within a confidence interval of $P/100$ percent is given as, for $\alpha = 1 - P$:

$$\Delta\mu \le Z_{1-\frac{\alpha}{2}} \cdot \frac{\sigma_{max}}{\sqrt{n}} = Z_{1-\frac{\alpha}{2}} \cdot \sqrt{\frac{(n-1)}{n} \cdot \frac{s^2}{\chi^2_{1-\frac{\alpha}{2}}}}$$

Noise Estimates for Impedance Measurements

Reduction of Noise in the DFT

We start with a given measurement of noise in a voltage measurement σ. For a K point waveform, we have $N = K/2$ bins in the DFT. We are sampling at a given sample rate Fs, and we assume the noise bandwidth is the entire Nyquist band $Fs/2$. Furthermore, the width of a single bin in frequency is $Fs/(2 \cdot N)$. Therefore, the amount of noise in a single bin is given by:

$$\sigma_{bin} = \frac{\sigma}{\sqrt{\frac{Fs}{2}}} \cdot \sqrt{\frac{Fs}{2 \cdot N}} = \frac{\sigma}{\sqrt{N}}$$

independent of sample rate.

Noise at a given VDIV setting on a scope channel

Given a volt/division setting of the scope $VDIV$ and a given SNR in dB, we can calculate the amount of noise σ. The full-scale signal effective voltage is:

$$V_{fs} = \frac{4 \cdot VDIV}{\sqrt{2}}$$

assuming eight divisions vertically across the screen.
In dBm, this is:

$$V_{dBm} = 20 \cdot \log\left(V_{fs}\right) + 13.010$$

The noise, in dBm is $\sigma_{dBm} = V_{dBm} - SNR$. Converting this back to volts, we have:

$$\sigma = 10^{-\frac{13.010}{20}} \cdot 10^{\frac{V_{dBm}-SNR}{20}} = 10^{\frac{20 \cdot \log\left(V_{fs}\right) - SNR}{20}} = V_{fs} \cdot 10^{-\frac{SNR}{20}} = \frac{4 \cdot VDIV}{\sqrt{2}} \cdot 10^{-\frac{SNR}{20}}$$

Noise in the ratio of two normally distributed values

The statistics of the ratio x/y where x and y have mean values μ_X and μ_Y and each are normally distributed with standard deviations σ_X and σ_Y and two variables are completely independent of one another is:

$$\sigma_R^2 = \frac{1}{\mu_Y^2} \cdot \sigma_X^2 + \frac{\mu_X^2}{\mu_Y^4} \cdot \sigma_Y^2$$

Noise in Impedance Measurements

We are taking an impedance measurement $Z = V/I$, we have $\sigma_Z = \sigma_R$, $I = \mu_Y$, $V = \mu_X = Z \cdot I$, $\sigma'_I = \sigma_Y$, $\sigma_V = \sigma_X$. So, we have:

$$\sigma_Z^2 = \frac{1}{I^2} \cdot \sigma_V^2 + \frac{V^2}{I^4} \cdot {\sigma'_I}^2 = \frac{1}{I^2} \cdot \sigma_V^2 + \frac{V^2}{I^4} \cdot {\sigma'_I}^2 = \frac{1}{I^2} \cdot \left(\sigma_V^2 + Z^2 \cdot {\sigma'_I}^2\right)$$

We use σ'_I because in our case, the current is inferred from a voltage across a resistor R_t so we have $\sigma'_I = \sigma_I / R_t$ where σ_I is the statistics of the voltage measurement used to infer the current. This leads to:

$$\sigma_Z = \frac{1}{I} \cdot \sqrt{\sigma_V^2 + \left(\frac{Z}{R_t}\right)^2 \cdot \sigma_I^2}$$

If the noise in the voltage measurements are such that $\sigma_I = \sigma_V = \sigma$, then we have:

$$\sigma_Z|_{\sigma=\sigma_I=\sigma_V} = \frac{\sigma}{I} \cdot \sqrt{1 + \left(\frac{Z}{R_t}\right)^2}$$

When the impedance being measured approaches zero, we have:

$$\lim \left(\sigma_Z\right)_{Z \to 0} = \frac{\sigma_V}{I}$$