Universal Power Distribution Test Tool and Methodology

April 8, 2016

Istvan Novak
T-Series Hardware Engineering

General note

the disclosures are made pursuant to Section 16, Confidentiality, of the Master Purchase and Services Agreement between Oracle and Teledyne-LeCroy Corporation (LFI # 165044 , effective 23 JUNE 2011).

Confidential- Oracle Restricted

Summary Description

A methodology and tool to test the electrical performance of power distribution networks based on the evaluation and post processing of time-domain measured data of device under test collected at one or more accessible test points, as a result of intentional external excitation and/or internal stimulus.

ORACLE
Confidential- Oracle Restricted

Problem Statement, Overall Solution

In power distribution network testing there are multiple tasks to be performed, including but not limited to transient noise and/or impedance testing, filter and/or power block transfer function testing, small and large signal stability testing of power source control loops and time and/or frequency-domain current sharing of multi-phase power sources. Test methodologies and processes do currently exist for all of the above, but for each kind of test they require different instrumentation, test setup, connections/probing and test methodology. For instance, impedance measurements of power distribution networks are typically done either with a dedicated impedance analyzer or a vector network analyzer in the frequency domain. However, many power engineers are unfamiliar with vector network analyzers; they are familiar with oscilloscopes. Also as an example, current sharing of multi-phase power sources is typically tested with an oscilloscope, but it requires extra custom hardware. The downsides of the existing solutions include, but not limited to: necessity to use unfamiliar instruments, need to change connections and test methodologies when switching between tasks, the need of extra hardware for some of the tasks (transient current sharing).

The proposed solution is based on time-domain measurements with an oscilloscope, and the various tasks can be performed just by changing the post-processing routine that can run real time on the oscilloscope. The stimulus can be the DUT's own functional operation or an optional external source. The universal solution can be achieved by the proper post-processing of the measured time-domain data.

Confidential- Oracle Restricted

Benefits Summary

Overall simpler and cheaper test setup and potentially new test functions not available with current solutions. The main advantages are ease of testing, increased efficiency and throughput of testing. In cases where custom hardware would be required to perform the test with the current methodology, the new solution could be also an enabler.

The methodology and solutions can be used for any power distribution tests; the method and implementation is not Oracle specific. The solutions and methodology can be used by the general HW electronic industry.

Confidential- Oracle Restricted

Detailed Problem Statement

Power distribution network testing, debug and validation is becoming a more and more time consuming task because of the increasing complexity of power solutions and tighter requirements.

Optimization of performance, size and cost has resulted in a sharp increase of the number of power converter circuits. At present time and for the foreseeable future, a large portion of power distribution validation and testing involves DC-DC converters.

The most advanced designs require –among others- several or all of the following test and validation tasks on the power conversion and distribution circuits [1]:

1. Transient response to step-current load
2. Current sharing and tracking (in multi-phase converters) to load current transients
3. Output response to input voltage transients
4. Output impedance
5. Input-to-output transfer function (power supply rejection ratio and filter transfer function)
6. Output-to-input transfer function, supply rail crosstalk and interactions
7. Input impedance of filters and power conversion circuits

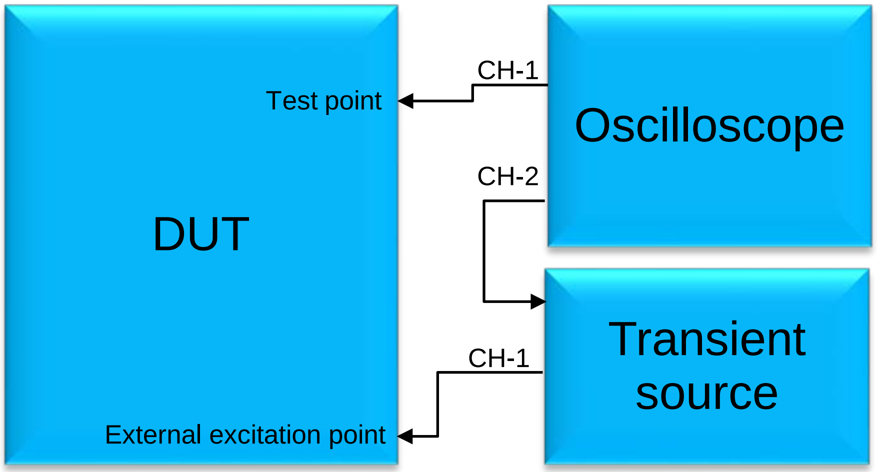
Detailed Problem Statement

- 1 through 3 are done in the time domain with transient sources and oscilloscopes [2]
- In addition, 2) typically requires extra signal conditioning hardware
- 4 through 7 are done in the frequency domain with Frequency Response Analyzers or Vector Network Analyzers [3]
- Time domain test procedures are valid for linear and nonlinear circuits alike.
- Frequency domain test procedures are limited to linear circuits or linearized testing of nonlinear circuits.
- Traditional oscilloscopes do not require (sophisticated) calibration, but their accuracy and dynamic range is limited
- Frequency Response Analyzers and especially Vector Network Analyzers require detailed calibration and skilled operators, but offer higher accuracy and better dynamic range.
- Performing all of the test and validation tasks require very different instrumentations and operator skill sets.

Confidential- Oracle Restricted

Task 1: Transient Response to Step-Current Load Setup

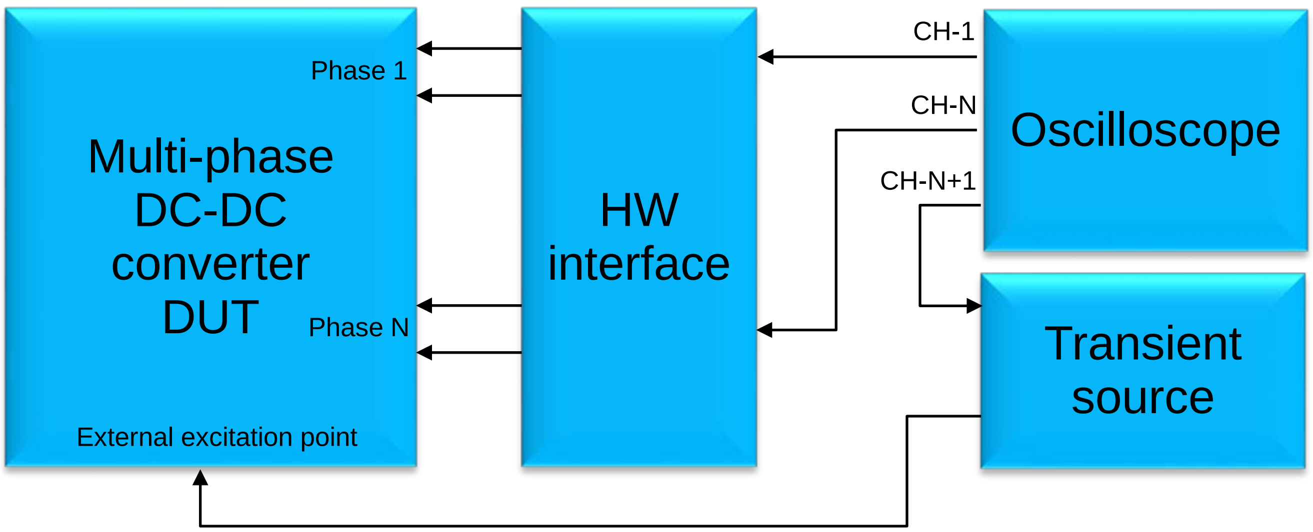
Typical block schematics of the test setup:



Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

Task 2: Multi-Phase Converter Current Sharing Test Setup

Typical block schematics of the test setup:



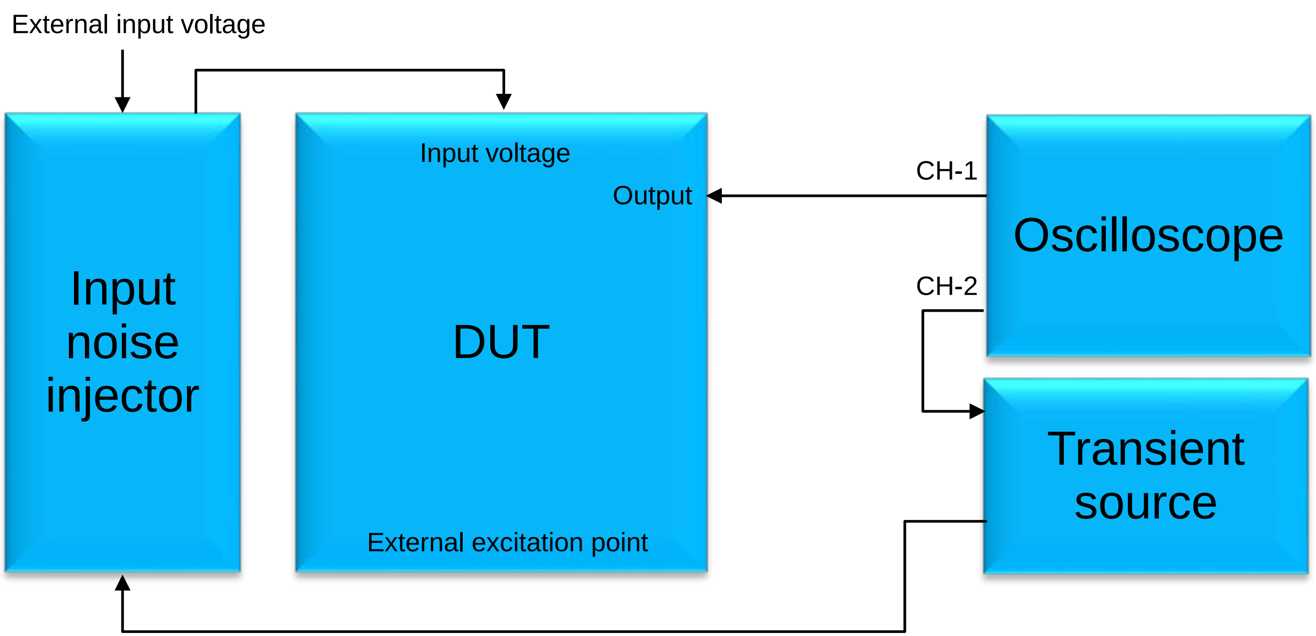
Note: the typical HW interface could be a set of RC components connected between the switch nodes of the phases and the output of the DC-DC converter.

Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

Confidential- Oracle Restricted

Task 3: Output Response to Input Voltage Transient Test Setup

Typical block schematics of the test setup:

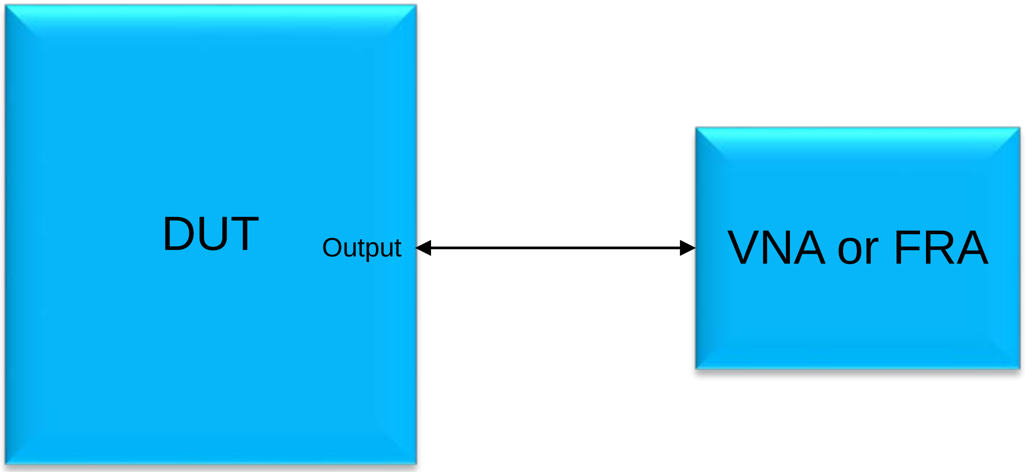


Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

Confidential- Oracle Restricted

Task 4: Output Impedance Test Setup

Typical block schematics of the test setup:



VNA: Vector Network Analyzer

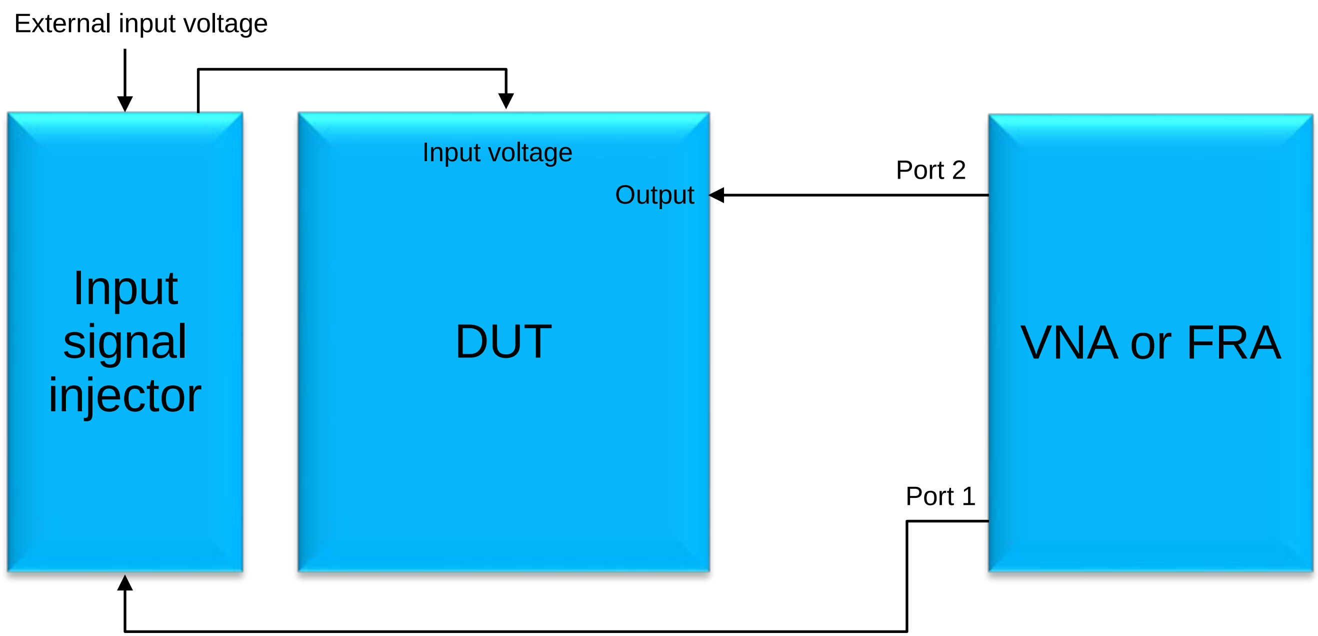
FRA: Frequency Response Analyzer

Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

Confidential- Oracle Restricted

Task 5: Input-to-output Transfer Function Test Setup

Typical block schematics of the test setup:



VNA: Vector Network Analyzer

FRA: Frequency Response Analyzer

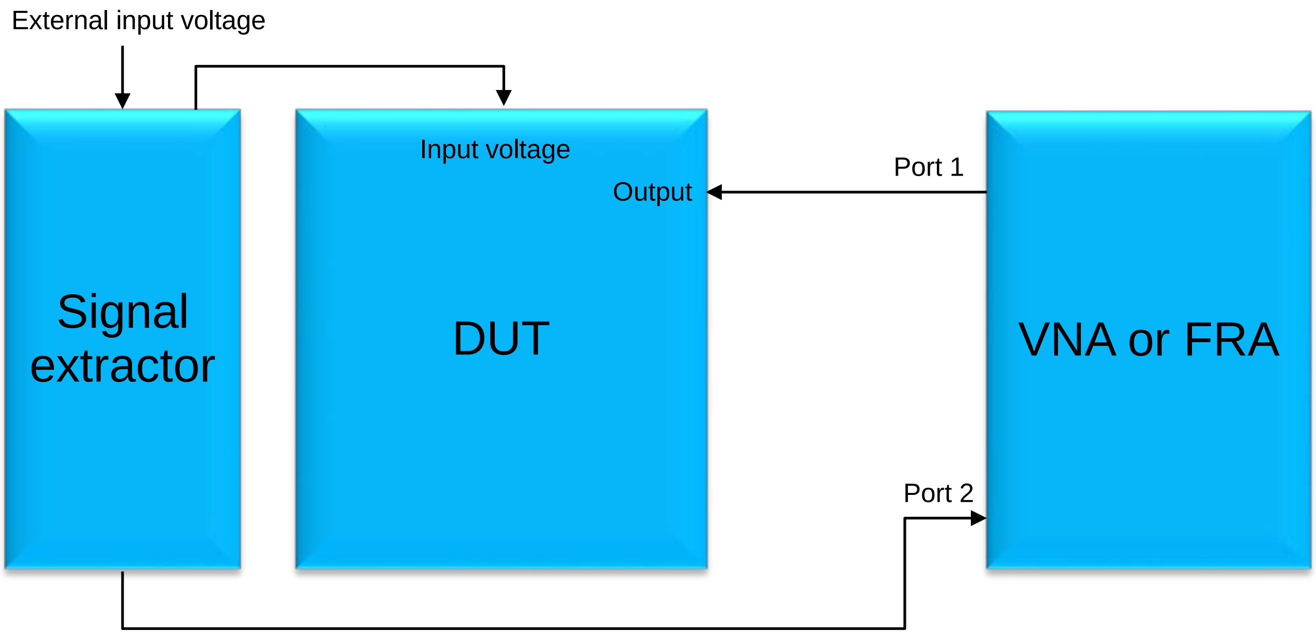
Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

ORACLE

Confidential- Oracle Restricted

Task 6: Output-to-input Transfer Function Test Setup

Typical block schematics of the test setup:



VNA: Vector Network Analyzer

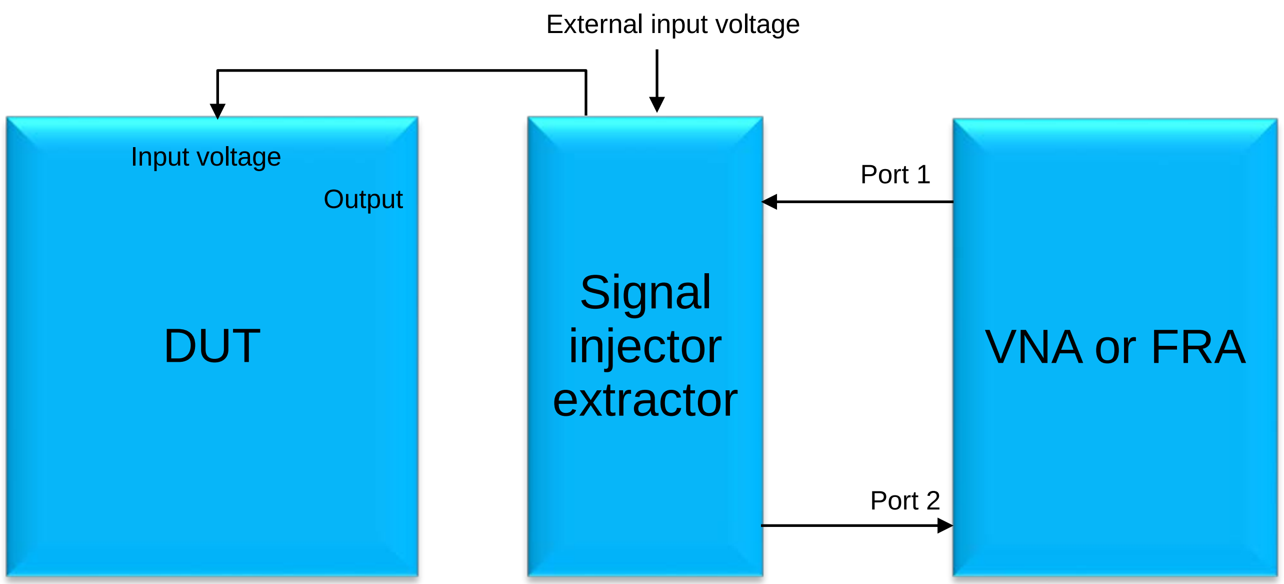
FRA: Frequency Response Analyzer

Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

Confidential- Oracle Restricted

Task 7: Input Impedance Test Setup

Typical block schematics of the test setup:



VNA: Vector Network Analyzer

FRA: Frequency Response Analyzer

Note: for sake of simplicity, power supplies and DC electronic loads are not shown.

The Goals

To create a test setup and methodology that allows the user to

- Perform any or all of the tasks with the same instrumentation and setting: time and frequency domain, on linear or nonlinear DUTs
- Is based on time-domain measurements, requiring no or minimal calibration setups
- Optionally run the shell software on the time-domain instrument, without the need for an external controlling computer

ORACLE
Confidential- Oracle Restricted

The Enablers

The suggested solution is based on the following enablers

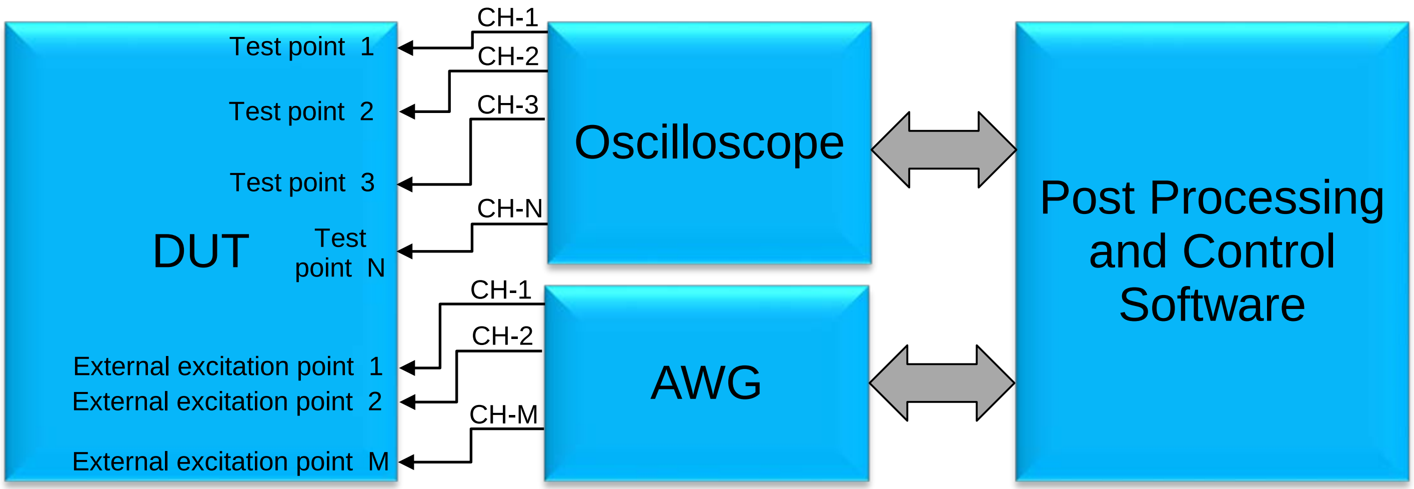
- Time-domain measurements can process both linear and nonlinear responses
- Post-processing of high-resolution time-domain instrument output data can provide frequency-domain results with sufficient dynamic range, eliminating the need for Vector Network Analyzers
- Recent advances in oscilloscope and Arbitrary Waveform Generator technology yield sufficiently high dynamic range and accuracy
- Oscilloscopes require less skilled operators
- Recent advances in oscilloscope technology put powerful computers into the oscilloscope boxes and allow the vendor or user to create different customized and targeted measurement ‘skins’
- As opposed to Vector Network Analyzers, oscilloscopes are inherently wide band, starting at DC.
- High-resolution multi-input oscilloscopes are available with multiple inputs (in contrast, currently the low-frequency Vector Network Analyzers are available only with two ports).

The Suggested Solution

The suggested solution is based on

- A high-resolution multi-channel oscilloscope with N (N>=1) channels
- Optional high-resolution arbitrary waveform generator with or without booster amplifier with M (M>=1) channels
- Control and data post-processing software to create the various functions

Block schematics of the suggested test setup:



Note: the DUT can be passive (unpowered) or active (powered) running user code or custom test code

References

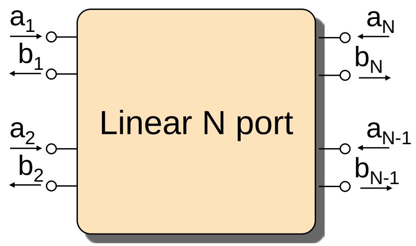
[1] Steve Sandler, Heidi Barnes, “Introduction to Power Integrity,” DesignCon 2016, January 19-21, 2016, Santa Clara, CA

[2] Radhakrishnan, et al, “Optimization of Package Power Delivery and Power Removal Solutions to meet Platform level Challenges,” Intel Developer Forum, 2004.

[3] Istvan Novak, Jason Miller: Frequency-Domain Characterization of Power Distribution Networks. Artech House, 2007.

Confidential- Oracle Restricted

Appendix A
Conversion Between Time and Frequency Domains



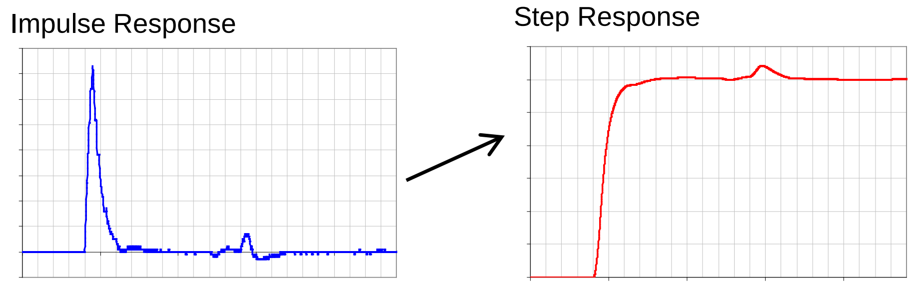
$$h(t) = InverseFourier\{H(\omega)\}$$

The network response function and the Impulse Response function create a Fourier pair.

$$h(t) = IFFT\{Z(f)\}$$

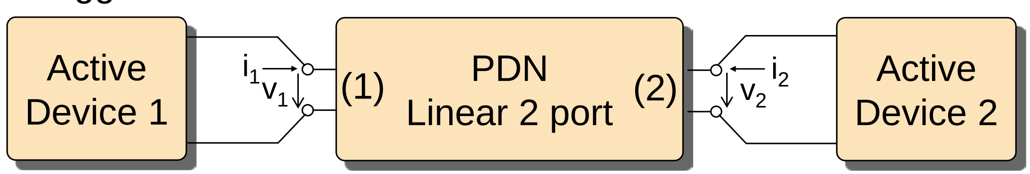
$$s(t) = \int h(t)dt$$

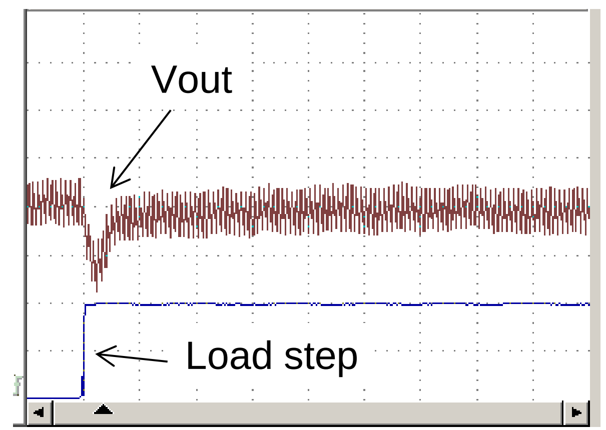
The Step Response is the time integral of the Impulse Response



Switching device: aggressor

Quiet device: victim





Transfer function for self-inflicted noise: $v_1/i_1 = Z_{11}$

Transfer function for propagated noise: $v_2/i_1 = Z_{21}$

Appendix B
Measuring Current in DC-DC Converters

Popular solutions

- Measuring voltage drop across low-side FET Rdson
- Measuring voltage drop across high-side FEDT Rdson
- Measuring integrated switch-node voltage (voltage across inductor R_L)

A Simple Current-Sense Technique Eliminating A Sense Resistor

Introduction

A sense resistor R_S, as shown in Figure 1, is often used for the purpose of over-current protection (OCP). R_S is usually a power device because it needs to handle the large current flowing through it. Therefore, it can be costly, bulky, and inefficient. Even though the $R_{DS(ON)}$ of the MOSFET or monitoring the output voltage are also used in OCP, those two techniques have very poor accuracy and are good only for output short-circuit protection. They can not protect the power supply when there is a weak short circuit at the output or the output is over current.

This application note introduces a simple current-sense technique that eliminates that sense resistor, resulting in system-cost reduction, PCB space saving, and power-efficiency improvement. Furthermore, the new current-sensing mechanism allows higher dynamic tripping current than the static one (built-in low-pass filtering) to improve current-sense noise immunity.

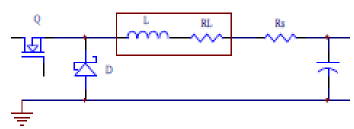


Figure 1 – A buck converter with a resistor Rs for sensing the inductor current. The resistor R_L is the parasitic resistance of the inductor.

The New Sensing Technique

This new sense technique utilizes the inductor parasitic resistance, R_L, to sense the inductor current. Figure 2 shows the new sensor circuitry with the original sensing resistor R_S eliminated. The new sensor consists of a resistor R and a small ceramic capacitor C_S, in parallel directly with the inductor. The voltage V_{Cs} across C_S is the sensor's output.

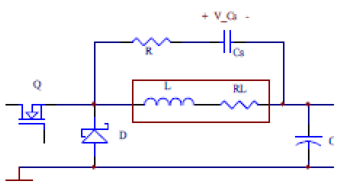


Figure 2 - The new current sense technique

The operation of the new sensor can be understood by examining the inductor current and the capacitor C_S voltage. When the buck converter is operating, the voltage on the left side of the inductor is a chopped voltage while the one on the right side is constant. The equivalent voltage across the inductor and the RC sensor is a square wave, as shown in Figure 3 (a) and (c).

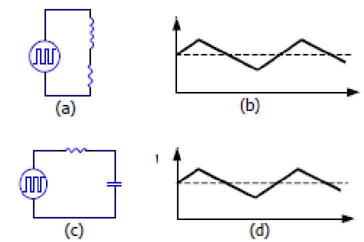


Figure 3 – The equivalent circuits and waveforms for the inductor and the sensing circuitry.

When L/R_L is much greater than the switching period T_S, i.e.

$$L/R_L >> Ts\ , \qquad (1)$$

the inductor current is a triangular wave, as shown in Figure 3 (b). If values are selected such that

$$R \cdot Cs = L/R_L\ , \qquad (2)$$

one can find that the capacitor voltage is directly proportional to the inductor current, as shown in Figure 3 (d). In fact,

$$V\_Cs = i_L R_L \qquad (3)$$

where i_L is the inductor current. Therefore, one can use the capacitor voltage for OCP.

Copyright © 1998
Rev 1.1 07/98

Confidential- Oracle Restricted

Appendix C
Current Measurement Challenges in DC-DC Converters

When using only one of the three methods

- Not all of the possible mis-operations can be detected
- Second and third options require very good common-mode rejection, otherwise noticeable error occurs
- The proposed method allows simultaneous measurement of two or all three options

There is no measurement procedure to test/validate the time or frequency domain response and/or the stability of current-sharing loops in multi-phase converters

>> New market opportunity for multi-channel oscilloscopes

Appendix D
Bandwidth Requirement

- Most DC-DC converters today run at or below one megahertz per-phase switching frequency
- For most measurements a 100MHz analog BW quantization should be enough, which allows the use of high bit count quantization
- Note: high-frequency burst ringing may be present on the switch nodes, requiring good anti-aliasing HW filters

Confidential- Oracle Restricted