

Edgar Reyes-Rivera

Cincinnati, Ohio

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Education

Miami University

Bachelor of Science in Computer Engineering

Bachelor of Science in Computer Science

Oxford, OH

Expected May 2027

GPA: 3.26

Relevant Coursework

Computer Science: Data Abstractions & Structures, Algorithms I, Object-Oriented Programming, Systems I & II, Database Systems, Comparative Programming Languages

Computer Engineering: Digital Systems Design, Computer Organization, Embedded Systems Design, Electric Circuit Analysis I

Skills & Certifications

Languages: C++ (Proficient), Java (Proficient), C# (Intermediate), Python (Intermediate), Verilog (Intermediate), MIPS Assembly (Intermediate), SQL, Scheme, Prolog

Hardware & Systems: FPGA Development, Digital Circuit Design, Embedded Systems, RISC-V Architecture, Quartus

Developer Tools: Git, GitHub, JIRA, Bitbucket, Confluence, Agile Methodologies, Multi-threading

Certifications: Ohio Southwest Alliance on Semiconductors and Integrated Scalable Manufacturing (O.A.S.I.S)

Experience

Synchrony

Software Engineer Intern

Cincinnati, OH

July 2024 – September 2024

- Engineered and delivered technical solutions as a member of a remote, agile Enablement Architecture team.
- Researched and prototyped software packages, providing data-driven recommendations to meet team requirements.
- Contributed to the development of B2B software for loan processing and private label credit cards.
- Utilized Atlassian tools (JIRA, Bitbucket, Confluence) to manage project tasks and collaborate on code development.

Projects

TinyRISC-V RV1 Processor

 Project Details

- Designed and implemented a single-cycle 32-bit RISC-V processor (RV1) in Verilog, supporting a subset of the RISC-V ISA including arithmetic, logical, and memory access operations.
- Developed a custom assembler in Python to convert RISC-V assembly into machine-readable binary for the processor.
- Verified processor functionality and instruction execution through extensive testing.

FPGA-Based Gaussian Blur Image Processing

 Project Details

- Engineered a Gaussian blur filter on a Cyclone V SoC FPGA using Verilog on Quartus.
- Processed a 160x120 .mif image through a 3x3 Gaussian kernel and scaled the output to a 640x480 VGA display.
- Implemented efficient memory management with double buffering and fixed-point arithmetic, achieving approximately 16ms processing time per frame.

Leadership & Service

President, Society of Hispanic Professional Engineers (SHPE)

August 2023 – Present

- Lead student chapter, delegate roles to the executive board, and represent SHPE at university-wide meetings.
- Establish and maintain collaborations with corporate sponsors and other campus organizations.

Student Intern, A.S.P.I.R.E.

March 2024 – Present

- Analyze data on university diversity initiatives to create reports for state and federal representatives, advocating for program funding and support.

Judge, FIRST Tech Challenge

Oxford, OH

- Evaluated 27 high school robotics teams on project design, innovation, and teamwork.