

1. Description

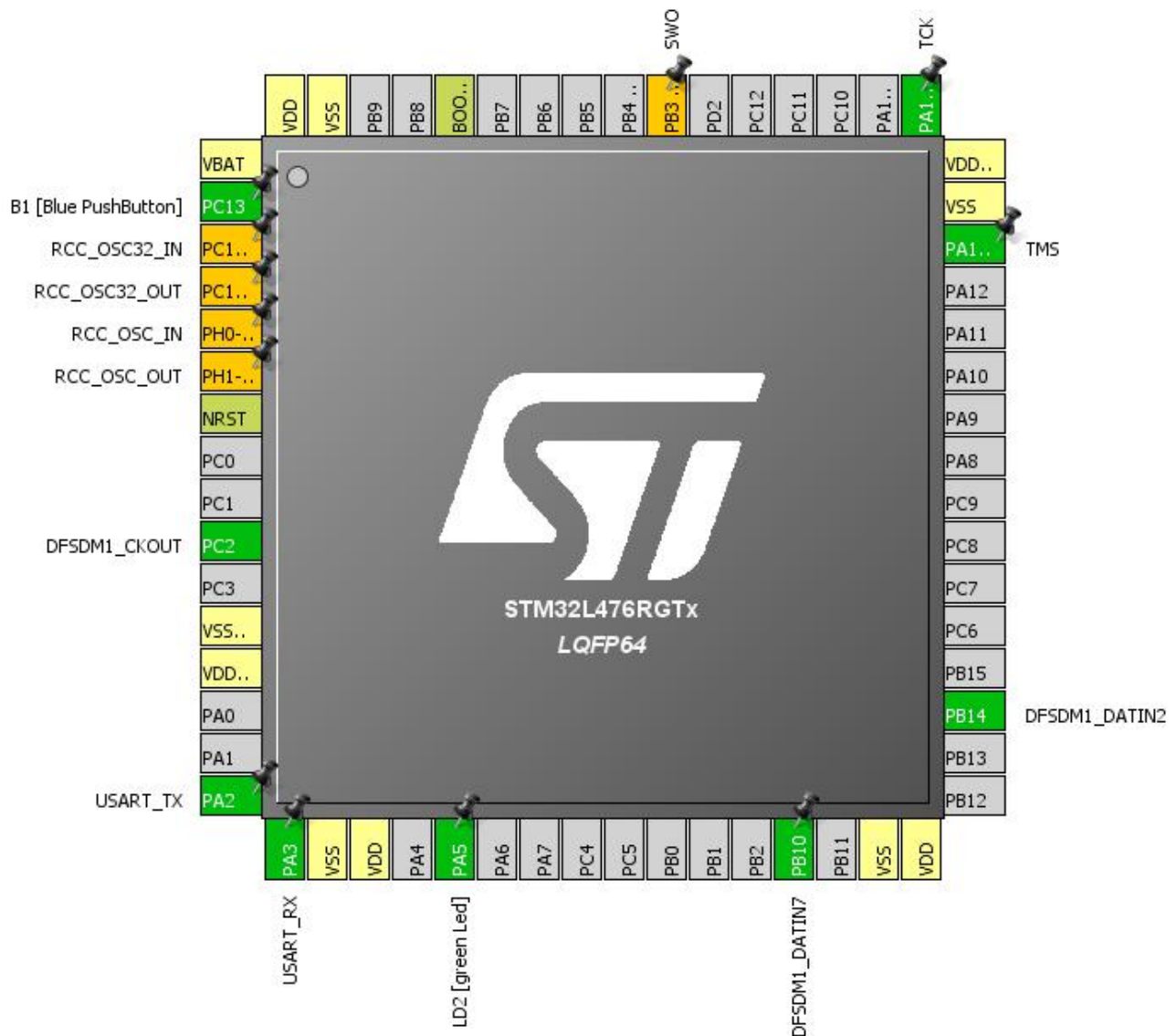
1.1. Project

Project Name	basic
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 4.25.1
Date	05/27/2018

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



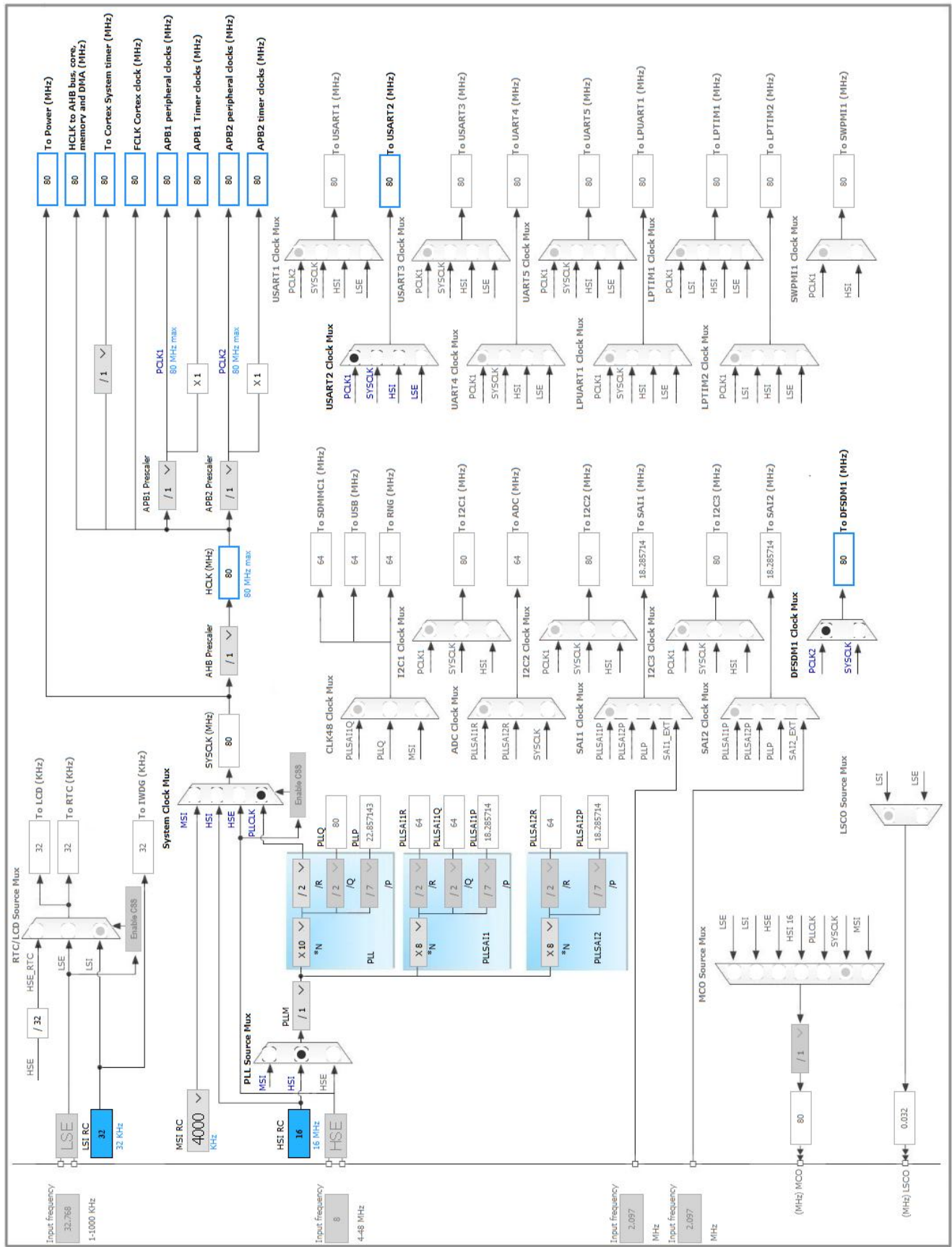
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14) *	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15) *	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
10	PC2	I/O	DFSDM1_CKOUT	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 **	I/O	GPIO_Output	LD2 [green Led]
29	PB10	I/O	DFSDM1_DATIN7	
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	DFSDM1_DATIN2	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO-TRACESWO) *	I/O	SYS_JTDO-SWO	SWO
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. DFSDM1

mode: PDM/SPI Input from ch2 and Internal Clock

mode: PDM/SPI input from ch2 and internal clock

mode: PDM/SPI input from ch7 and internal clock

mode: CKOUT

5.1.1. Filter 0:

regular channel selection:

regular channel selection

Continuous Mode

Trigger to start regular conversion

Fast Mode

Dma Mode

Channel 2 *

Continuous Mode

Software trigger

Enable *

Enable *

injected channel selection:

Channel0 as injected channel

Channel1 as injected channel

Channel2 as injected channel

Channel3 as injected channel

Channel4 as injected channel

Channel5 as injected channel

Channel6 as injected channel

Channel7 as injected channel

Disable

Disable

Disable

Disable

Disable

Disable

Disable

Disable

Filter parameters:

Sinc Order

Fosr

losr

Sinc 3 filter type *

32 *

1

5.1.2. Filter 1:

regular channel selection:

regular channel selection

Continuous Mode

Trigger to start regular conversion

Fast Mode

Channel 7 *

Continuous Mode

Software trigger

Enable *

Dma Mode	Enable *
injected channel selection:	
Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable
Filter parameters:	
Sinc Order	Sinc 3 filter type *
Fosr	32 *
losr	1

5.1.3. Filter 2:

regular channel selection:	
regular channel selection	Channel 1 *
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	Enable *
Dma Mode	Enable *
injected channel selection:	
Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable
Filter parameters:	
Sinc Order	Sinc 3 filter type *
Fosr	32 *
losr	1

5.1.4. Filter 3:

regular channel selection:

regular channel selection - None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

5.1.5. Output Clock:

Output Clock parameters:

Selection	Source for output clock is system clock
Divider	52 *

5.1.6. Channel 1:

Channel 1 parameters:

Type	SPI with falling edge *
Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	0x02 *

Analog watchdog parameters:

Filter Order	FastSinc filter type
Oversampling	10 *

5.1.7. Channel 2:

Analog watchdog parameters:

Filter Order	FastSinc filter type
Oversampling	10 *

Channel 2 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock
Offset	0

Right Bit Shift **0x02 ***

5.1.8. Channel 7:

Analog watchdog parameters:

Filter Order	FastSinc filter type
1	FastSinc1
2	FastSinc2
3	FastSinc3
4	FastSinc4
5	FastSinc5
6	FastSinc6
7	FastSinc7
8	FastSinc8
9	FastSinc9
10	FastSinc10
11	FastSinc11
12	FastSinc12
13	FastSinc13
14	FastSinc14
15	FastSinc15
16	FastSinc16
17	FastSinc17
18	FastSinc18
19	FastSinc19
20	FastSinc20
21	FastSinc21
22	FastSinc22
23	FastSinc23
24	FastSinc24
25	FastSinc25
26	FastSinc26
27	FastSinc27
28	FastSinc28
29	FastSinc29
30	FastSinc30
31	FastSinc31
32	FastSinc32
33	FastSinc33
34	FastSinc34
35	FastSinc35
36	FastSinc36
37	FastSinc37
38	FastSinc38
39	FastSinc39
40	FastSinc40
41	FastSinc41
42	FastSinc42
43	FastSinc43
44	FastSinc44
45	FastSinc45
46	FastSinc46
47	FastSinc47
48	FastSinc48
49	FastSinc49
50	FastSinc50
51	FastSinc51
52	FastSinc52
53	FastSinc53
54	FastSinc54
55	FastSinc55
56	FastSinc56
57	FastSinc57
58	FastSinc58
59	FastSinc59
60	FastSinc60
61	FastSinc61
62	FastSinc62
63	FastSinc63
64	FastSinc64
65	FastSinc65
66	FastSinc66
67	FastSinc67
68	FastSinc68
69	FastSinc69
70	FastSinc70
71	FastSinc71
72	FastSinc72
73	FastSinc73
74	FastSinc74
75	FastSinc75
76	FastSinc76
77	FastSinc77
78	FastSinc78
79	FastSinc79
80	FastSinc80
81	FastSinc81
82	FastSinc82
83	FastSinc83
84	FastSinc84
85	FastSinc85
86	FastSinc86
87	FastSinc87
88	FastSinc88
89	FastSinc89
90	FastSinc90
91	FastSinc91
92	FastSinc92
93	FastSinc93
94	FastSinc94
95	FastSinc95
96	FastSinc96
97	FastSinc97
98	FastSinc98
99	FastSinc99
100	FastSinc100

Oversampling **10 ***

Channel 7 parameters:

Type **SPI with falling edge ***

Spi Clock Internal SPI clock

Offset	0
--------	---

Right Bit Shift **0x02 ***

5.2. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.3. USART2

Mode: Asynchronous

5.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
-----------	--------

Word Length **8 Bits (including Parity) ***

Parity None

Stop Bits	1
-----------	---

Advanced Parameters:

Data Direction	Receive and Transmit
----------------	----------------------

Over Sampling 16 Samples

Single Sample Disable

Advanced Features:

Auto Baudrate Disable

TX Pin Active Level Inversion	Disable
-------------------------------	---------

RX Pin Active Level Inversion	Disable
-------------------------------	---------

Data Inversion Disable

TX and RX Pins Swapping	Disable
-------------------------	---------

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* **User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DFSDM1	PC2	DFSDM1_CKOUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	DFSDM1_DATIN7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB14	DFSDM1_DATIN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_TX
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART_RX
Single Mapped Signals	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3 (JTDO-TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green Led]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
DFSDM1_FLT0	DMA1_Channel4	Peripheral To Memory	Medium *
DFSDM1_FLT1	DMA1_Channel5	Peripheral To Memory	Medium *
DFSDM1_FLT2	DMA1_Channel6	Peripheral To Memory	Medium *

DFSDM1_FLT0: DMA1_Channel4 DMA request Settings:

Mode: **Circular ***
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Word
 Memory Data Width: Word

DFSDM1_FLT1: DMA1_Channel5 DMA request Settings:

Mode: **Circular ***
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Word
 Memory Data Width: Word

DFSDM1_FLT2: DMA1_Channel6 DMA request Settings:

Mode: **Circular ***
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Word
 Memory Data Width: Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART2 global interrupt	unused		
DFSDM1 filter0 global interrupt	unused		
DFSDM1 filter1 global interrupt	unused		
DFSDM1 filter2 global interrupt	unused		
FPU global interrupt	unused		

* User modified value

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	025976_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.0

8. Software Project

8.1. Project Settings

Name	Value
Project Name	basic
Project Folder	C:\Users\shiny\Documents\GitHub\ultrasonic-communication\basic
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_L4 V1.11.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report