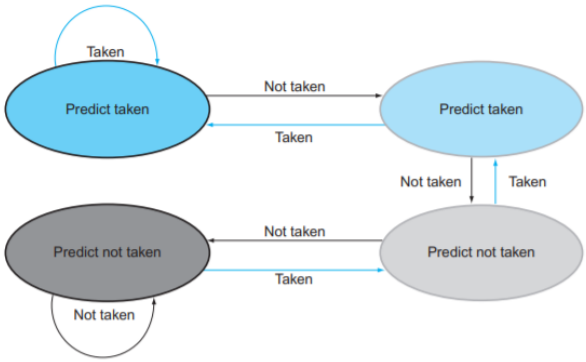
CA LAB2 Report

1 Module Explanation

- branch_predictor
  The module can give the branch prediction based on the current state. The state is updated at the positive edge of the clock signal and only when a branch signal occurs.



- ALU_Control and ALU
  ALU_Control is modified to make ALU preform "substraction" when the operation is "beq".

- Additional Flushes
  When the branch predictor gives a prediction, the result is verified in the next stage. When the prediction is verified to be wrong, it has to flush both IF_ID and ID_EX and update the correct PC.

2 Difficulties Encountered and Solutions in This Lab

- Modification on complex datapath of lab1
  Lab2 is based on the work of lab1. With the already complex datapath in lab1, it would be even more confusing when adding new components. And it could be a big tragedy when misedit a wrong wire. With git and VS Code, it can highlight the modifications of lab2 I've made, so that the chances of misedit can be largely reduced.

- Datapath of the new component is not given
  Unlike HW3 and lab1, lab2 does not provide a datapath in spec. It would be necessary to figure out an appropriate datapath for branch predictor by our own. By drawing the datapath before implementation, the problem can be solved more easily.

3 Development Environment

- OS: Ubuntu20.04
- Compiler: iverilog