Experiment No. 2b

Date:

Series-fed Class A Power Amplifier using LT Spice

Aim:

To simulate a series-fed class A power amplifier using LT Spice

Theory

A series-fed Class A power amplifier is a simple amplifier where the load resistor is connected in series with the transistor's collector and the power supply. It is a Class A amplifier because the transistor conducts for the entire 360 degree (full cycle) of the input signal, resulting in good linearity but poor efficiency, with a maximum theoretical efficiency of 25%.

. How it works

- **Class A operation:** The transistor is biased to remain in its active region for the entire input signal cycle, meaning it is always "on".
- **Series-fed connection:** The load (like a resistor or speaker) is placed directly in the path of the collector current, in series with the DC supply
- **Amplification:** An input signal to the base (or gate) causes the collector current to vary. Since the load is in series, the voltage across the load resistor changes in proportion to this current, producing an amplified output.
- **Bias point:** The quiescent (no-signal) operating point is set in the center of the load line to allow for the largest possible output swing without distortion.

Key characteristics

- **High linearity:** The full-cycle conduction of Class A amplifiers results in very low distortion.
- **Low efficiency:** A significant amount of power is constantly being dissipated in the transistor, making it inefficient. In this series-fed configuration, the maximum theoretical efficiency is only 25%
- **Simple design:** The series-fed configuration is straightforward to build, without the need for a more complex transformer.

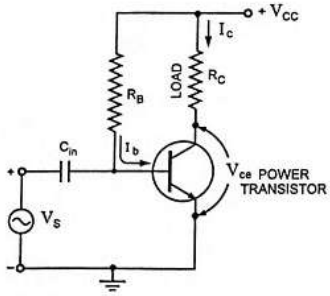
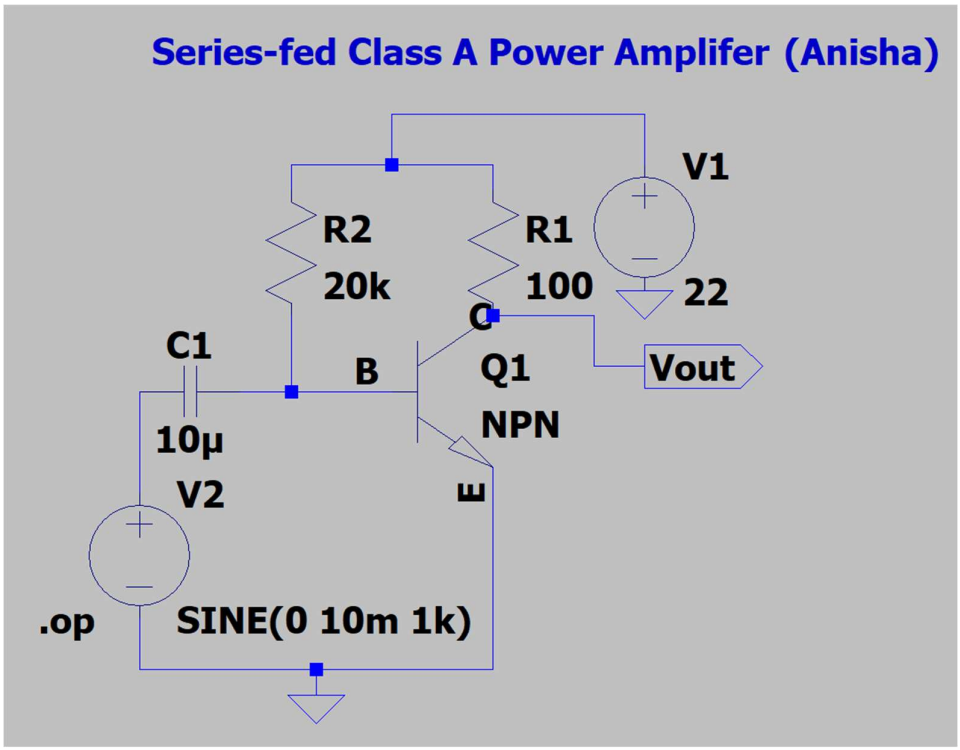
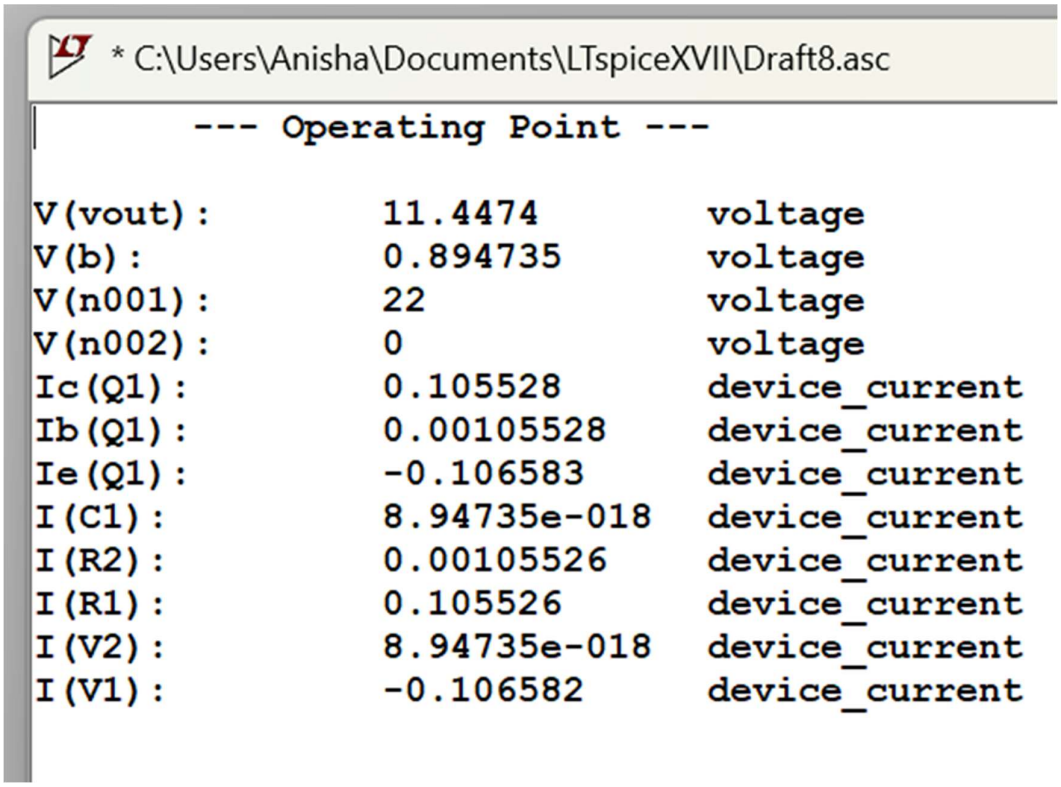


Fig. 17.5 *Series Fed Class A Large Signal Amplifier*

DC Operating Point Analysis



Simulation output

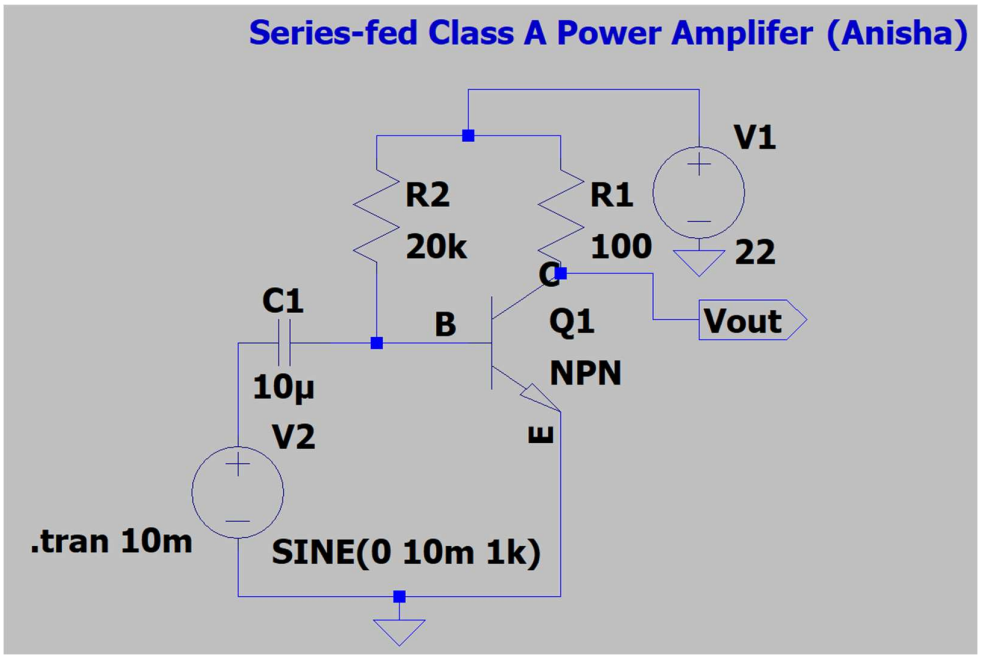


* C:\Users\Anisha\Documents\LTspiceXVII\Draft8.asc

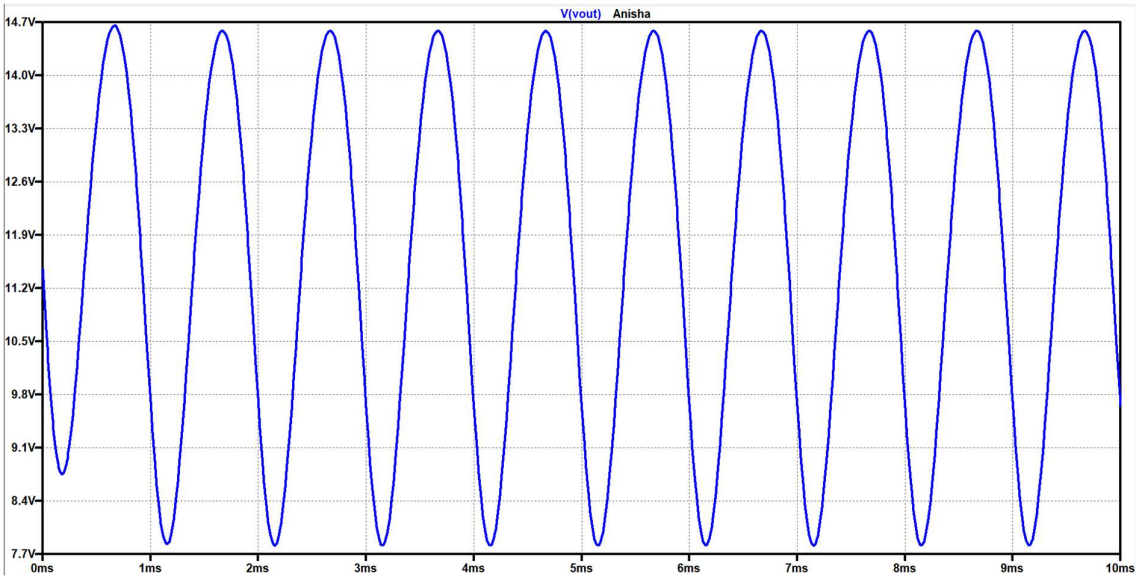
--- Operating Point ---

V(vout):	11.4474	voltage
V(b):	0.894735	voltage
V(n001):	22	voltage
V(n002):	0	voltage
Ic(Q1):	0.105528	device_current
Ib(Q1):	0.00105528	device_current
Ie(Q1):	-0.106583	device_current
I(C1):	8.94735e-018	device_current
I(R2):	0.00105526	device_current
I(R1):	0.105526	device_current
I(V2):	8.94735e-018	device_current
I(V1):	-0.106582	device_current

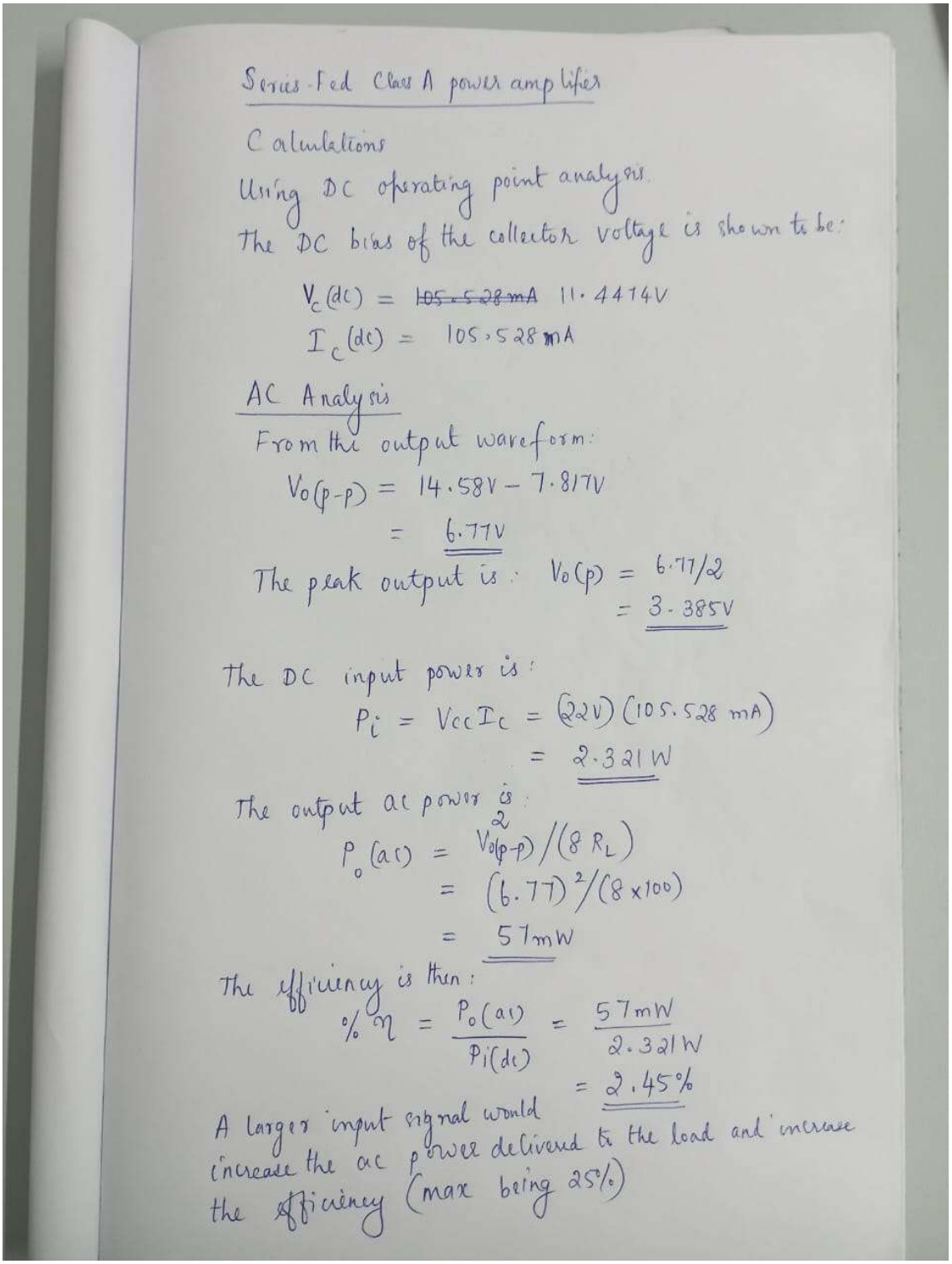
Transient Analysis



Simulation output



Calculations



Series-Fed Class A power amplifier

Calculations

Using DC operating point analysis

The DC bias of the collector voltage is shown to be:

$V_C(dc) = 105.528\,mA$ 11.4414V

$I_C(dc) = 105.528\,mA$

AC Analysis

From the output waveform:

$V_{o(p-p)} = 14.58V - 7.817V$

$= 6.77V$

The peak output is: $V_{o(p)} = 6.77/2$

$= 3.385V$

The DC input power is:

$P_i = V_{cc} I_C = (22V)(105.528\,mA)$

$= 2.321W$

The output ac power is:

$P_{o(ac)} = V_{o(p-p)}^2 / (8 R_L)$

$= (6.77)^2 / (8 \times 100)$

$= 57mW$

The efficiency is then:

$\%\eta = \frac{P_{o(ac)}}{P_{i(dc)}} = \frac{57mW}{2.321W}$

$= 2.45\%$

A larger input signal would increase the ac power delivered to the load and increase the efficiency (max being 25%)

Result:

Class A power amplifier was simulated using LT Spice. The efficiency obtained is……..

Additional question

Simulate a class B power amplifier and calculate its efficiency

Circuit diagram (reference: Robert L Boylestad)

Figure 16.31shows a quasi-complementary push-pull class B power amplifier. For the input of $V_i = 20$ V(p), the output waveform obtained using **probe** is shown in Fig. 16.32.

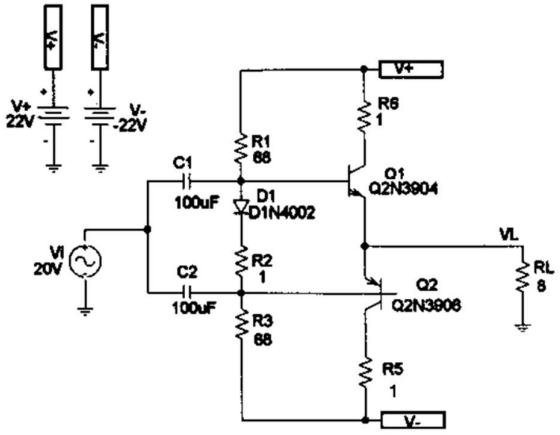


Figure 16.31 Quasi-complementary class B power amplifier.

Expected output:

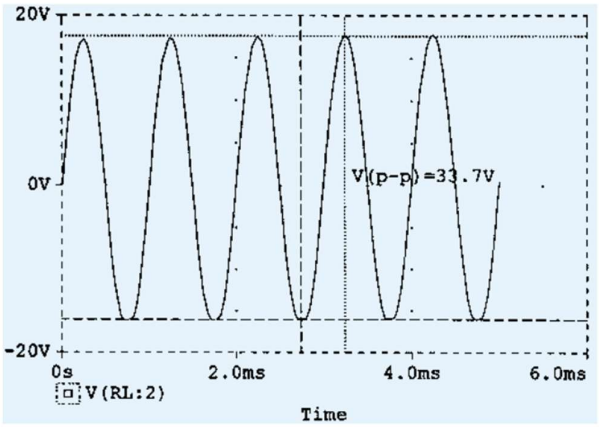


Figure 16.32 Probe output of the circuit in Fig. 16.31.

Sample calculations

The resulting ac output voltage is seen to be

$$V_o(\text{p-p}) = 33.7\ \text{V}$$

so that

$$P_o = V_o^2(\text{p-p})/(8 \cdot R_L) = (33.7\ \text{V})^2/(8 \cdot 8\ \Omega) = 17.7\ \text{W}$$

The input power for that amplitude signal is

$$P_i = V_{CC} I_{\text{dc}} = V_{CC}[(2/\pi)(V_o(\text{p-p})/2)R_L)]$$

$$= (22\ \text{V}) \cdot [[(2/\pi)(33.7\ \text{V}/2)/8] = 29.5\ \text{W}$$

The circuit efficiency is then

$$\%\eta = P_o/P_i \cdot 100\% = (17.7\ \text{W}/29.5\ \text{W}) \cdot 100\% = 60\%$$