Digital Laboratory

Nama	Edgrant Henderson Suryajaya	**Kode Asisten**	JJ
NPM	2206025016	**Jenis Tugas**	CS

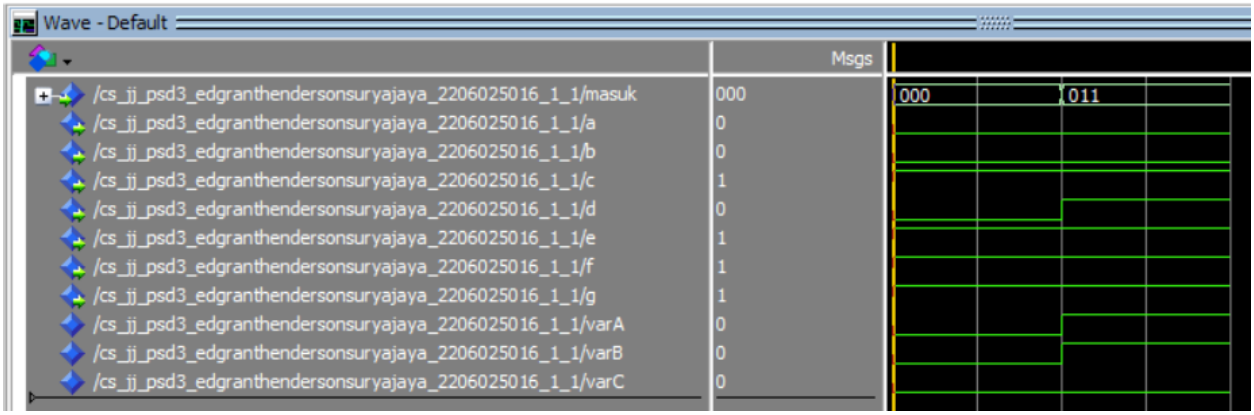
Jawaban

Part 1

1. .

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_1 is
    port (
        masuk : in std_logic_vector (2 downto 0);
        a, b, c, d, e, f, g : out std_logic
    );
end entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_1;

architecture rtl of CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_1 is
    signal varA, varB, varC: std_logic;
begin
    varA <= masuk(0);
    varB <= masuk(1);
    varC <= masuk(2);

    g <= '1';
    f <= (not varA) or (varB and not varC);
    e <= varA or varB or not varC;
    d <= varA or varC;
    c <= (varA xnor varB) or (varA and not varC);
    b <= (varB and varC) or (not varA and varC) or (varA and not varB and not
varC);
    a <= (not varA and varC) or (not varA and varB) or (varB and varC);
end architecture rtl;
```

2. Gambar simulasi di vhdl



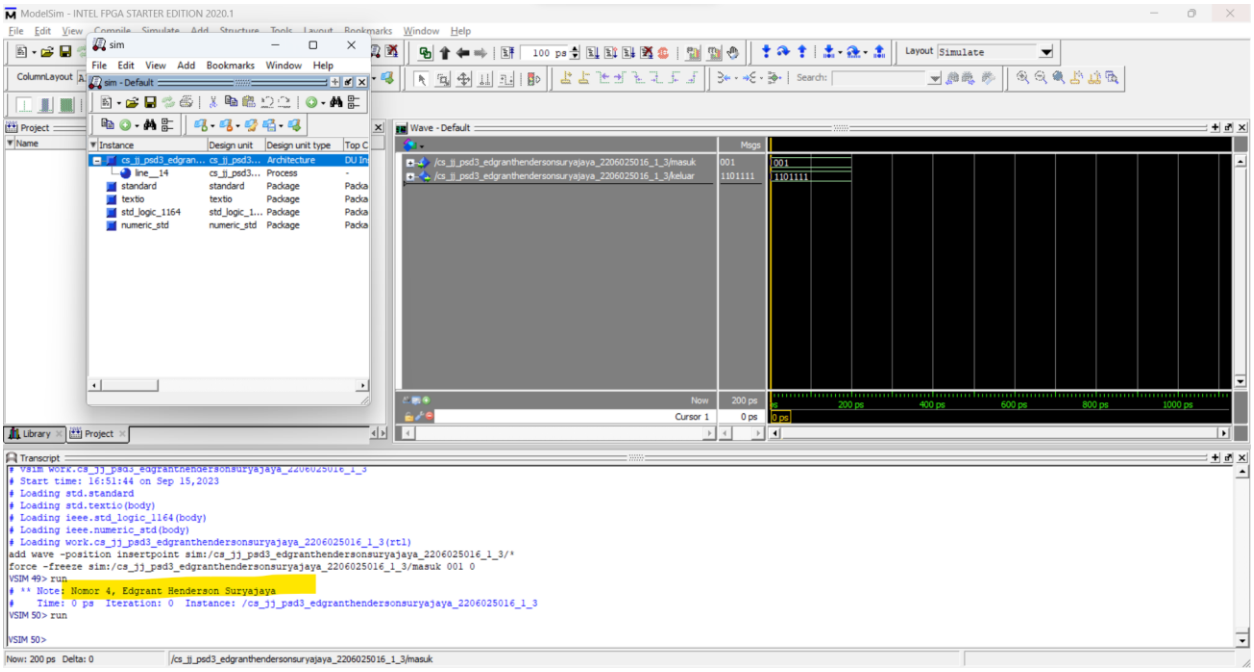
3. .

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_3 is
    port (
        masuk : in std_logic_vector (2 downto 0);
        keluar : out  std_logic_vector (6 downto 0)
    );
end entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_3;

architecture rtl of CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_3 is
begin
    process(masuk)
    begin
        case masuk is
            when "000" => keluar <= "1110100";
            when "001" => keluar <= "1101111";
            when "010" => keluar <= "1110001";
            when "011" => keluar <= "1111011";
            when "100" => keluar <= "1011110";
            when "101" => keluar <= "1011000";
            when "110" => keluar <= "1111100";
            when "111" => keluar <= "1011111";

            when others => keluar <= "0000000";
        end case;
    end process;

end architecture rtl;
```

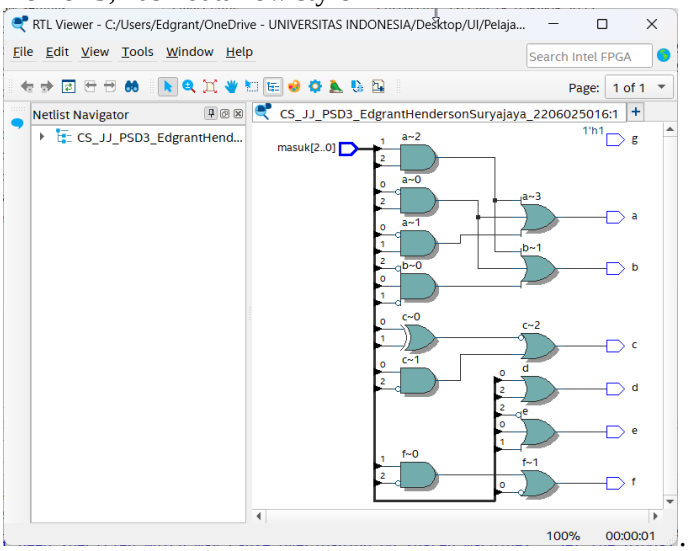
4. .

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_3 is
    port (
        masuk : in std_logic_vector (2 downto 0);
        keluar : out  std_logic_vector (6 downto 0)
    );
end entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_3;

architecture rtl of CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_1_3 is
begin
    process(masuk)
    begin
        REPORT "Nomor 4, Edgrant Henderson Suryajaya";
        case masuk is
            when "000" => keluar <= "1110100";
            when "001" => keluar <= "1101111";
            when "010" => keluar <= "1110001";
            when "011" => keluar <= "1111011";
            when "100" => keluar <= "1011110";
            when "101" => keluar <= "1011000";
            when "110" => keluar <= "1111100";
            when "111" => keluar <= "1011111";

            when others => keluar <= "0000000";
        end case;
    end process;

end architecture rtl;
```

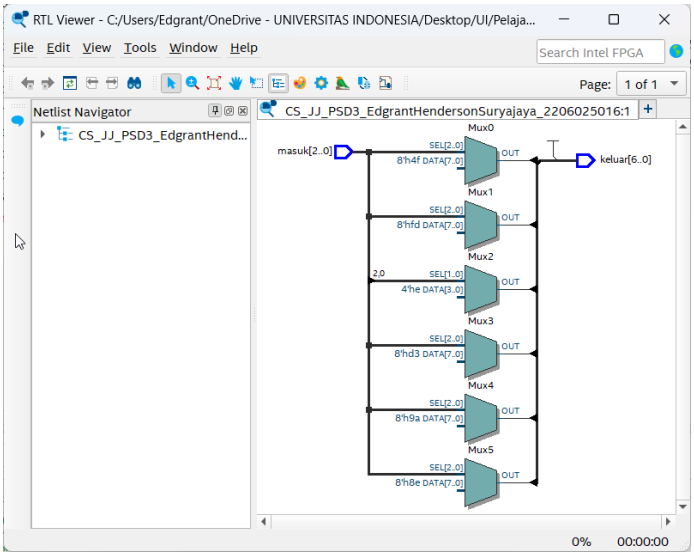
5. .


ModelSim - INTEL FPGA STARTER EDITION 2020.1
sim
Wave - Default
Transcript
Start time: 16:51:44 on Sep 15,2023
Loading std.standard
Loading std.textio(body)
Loading ieee.std_logic_1164(body)
Loading ieee.numeric_std(body)
Loading work.cs_jj_psd3_edgranthendersonsuryajaya_2206025016_1_3(rtl)
add wave -position insertpoint sim:/cs_jj_psd3_edgranthendersonsuryajaya_2206025016_1_3/*
force -freeze sim:/cs_jj_psd3_edgranthendersonsuryajaya_2206025016_1_3/masuk 001 0
VSIM 49> run
** Note: Nomor 4, Edgrant Henderson Suryajaya
Time: 0 ps Iteration: 0 Instance: /cs_jj_psd3_edgranthendersonsuryajaya_2206025016_1_3
VSIM 50> run
VSIM 50>

6. Nomor 3, hasil dataflow style



Nomor 6, hasil behavioural style



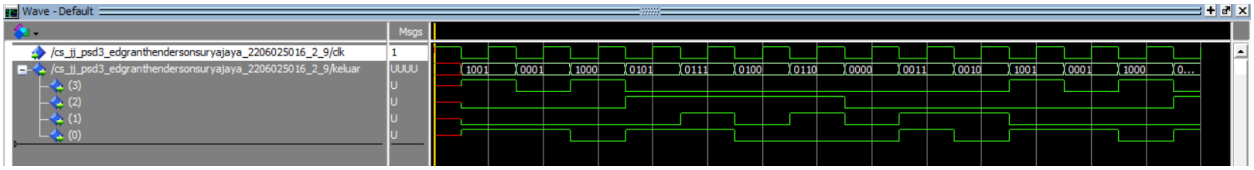
7. Rangkaian dataflow syle menggunakan gerbang logika karena memang sudah dibuat setiap persamaannya outputnya menggunakan gerbang logika, sedangkan rangkaian behavioural style menggunakan multiplexer yang dirancang dari switch case pada kode vhdl.
8. Oke bang

Part 2

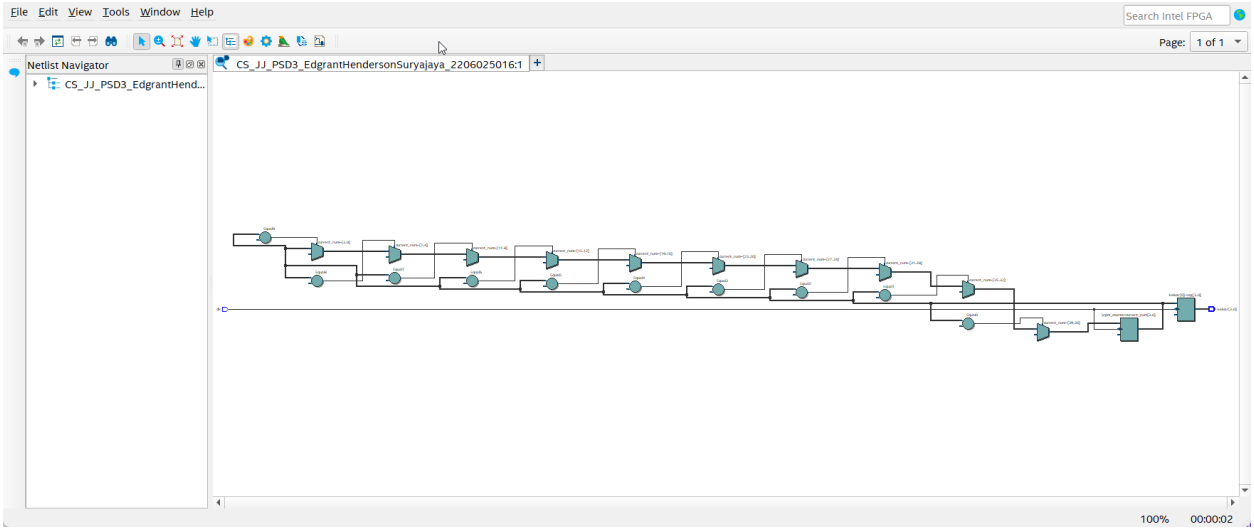
9. npm = 2306475819

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_2_9 is
    port (
        clk : in std_logic;
        keluar : out std_logic_vector (3 downto 0)
    );
end entity CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_2_9;

architecture rtl of CS_JJ_PSD3_EdgrantHendersonSuryajaya_2206025016_2_9 is
begin
    npm_counter: process(clk)
        variable current_num : std_logic_vector (3 downto 0) := "1001";
    begin
        if falling_edge(clk) then
            keluar <= current_num;
            if (current_num = "1001") then
                current_num := "0001";
            elsif (current_num = "0001") then
                current_num := "1000";
            elsif (current_num = "1000") then
                current_num := "0101";
            elsif (current_num = "0101") then
                current_num := "0111";
            elsif (current_num = "0111") then
                current_num := "0100";
            elsif (current_num = "0100") then
                current_num := "0110";
            elsif (current_num = "0110") then
                current_num := "0000";
            elsif (current_num = "0000") then
                current_num := "0011";
            elsif (current_num = "0011") then
                current_num := "0010";
            elsif (current_num = "0010") then
                current_num := "1001";
            end if;
        end if;
    end process npm_counter;

end architecture rtl;
```

10.



11. .



12. Kesimpulan:
    a. Dataflow style dan behavioural style adalah cara penulisan dalam vhdl
        a. Dataflow style menulis hasil dengan gerbang logika
        b. Behavioral style menulis secara sekuensial dan menggunakan conditional statement
    b. Implementasi dari dataflow style menggunakan quartus adalah dengan gerbang logika sedangkan behavioral style menggunakan multiplexer
    c. Proses digunakan pada behavioral style untuk menunjukan sebuah blok sekuensial
    d. Pada proses dapat ada conditional statement. Conditional statement juga dapat merujuk ke state sebelumnya untuk membentuk rangkaian sekuensial