Digital Laboratory

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|---|---|---|---|
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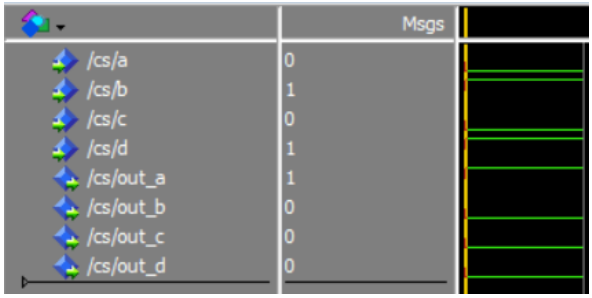
**Jawaban**

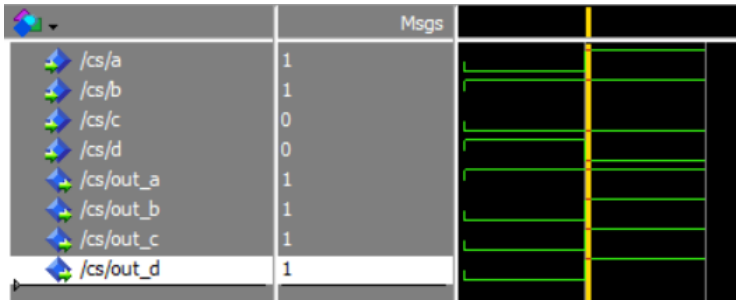
1. .

```
library ieee;
use ieee.std_logic_1164.all;

entity adder_3 is
    port(
        -- Input
        a : IN STD_LOGIC; --MSB
        b : IN STD_LOGIC;
        c : IN STD_LOGIC;
        d : IN STD_LOGIC; --LSB

        --output
        out_a : OUT STD_LOGIC;
        out_b : OUT STD_LOGIC;
        out_c : OUT STD_LOGIC;
        out_d : OUT STD_LOGIC
    );
end entity;

architecture adder_3_archi of adder_3 is
begin
    out_a <= a OR (b AND c) OR (b AND d);
    out_b <= (NOT b AND c) OR (NOT b AND d) OR (b AND NOT c AND NOT d);
    out_c <= (b AND NOT d) OR (c AND d) OR (NOT a AND NOT c AND NOT d);
    out_d <= (c AND NOT d) OR (NOT c AND NOT d);
end architecture;
```

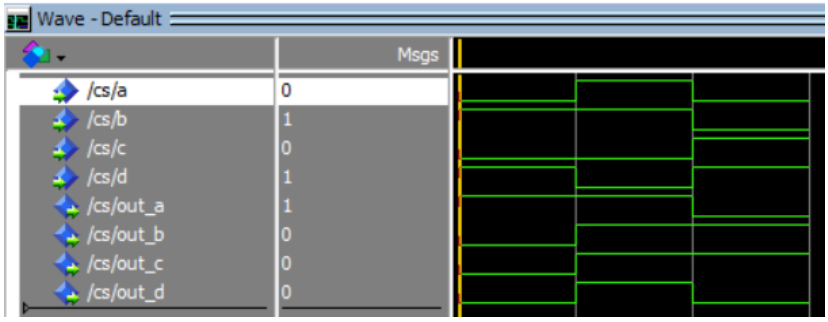
2. .
   a. 0101




   b. 1100

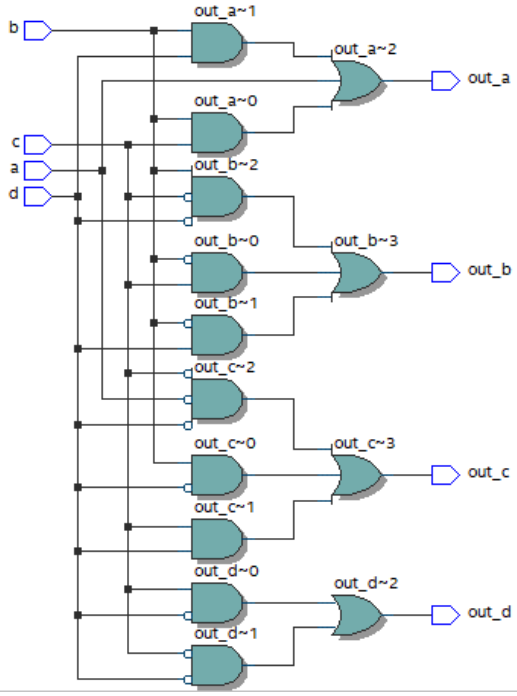


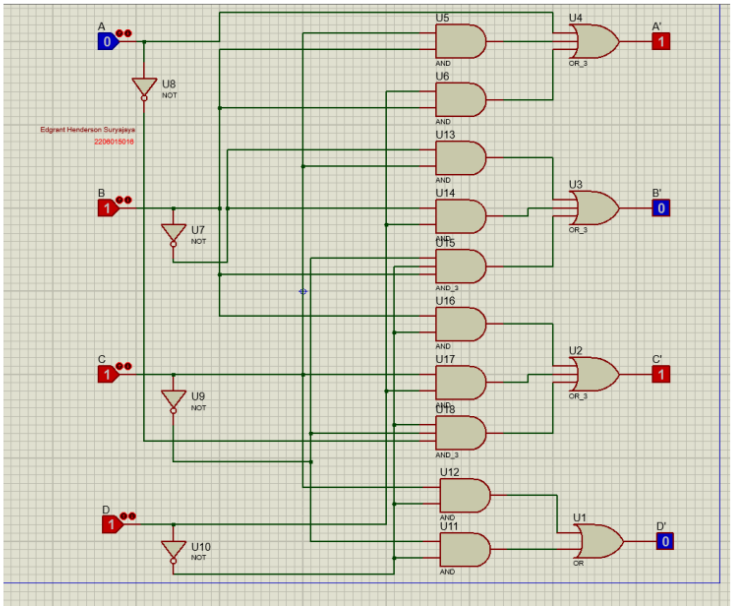

   c. 0011




   d. 1010

3. .



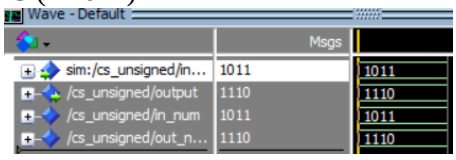




Keduanya sama intinya, tetapi pada sintesis RTL tidak menggunakan NOT, tetapi langsung NOT-nya di AND gatenya.

4. .

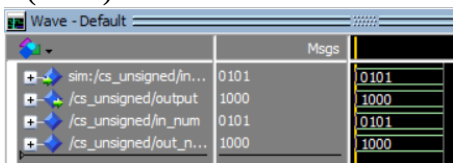
```
library ieee;
use ieee.std_logic_1164.all;
use  IEEE.STD_LOGIC_ARITH.ALL;

entity CS_unsigned is
    port(
        -- Input
        input : IN STD_LOGIC_VECTOR (3 DOWNTO 0); --ini 4 bit, karena bit pertama
dipake utk sign

        --output
        output : OUT STD_LOGIC_VECTOR (3 DOWNTO 0) --sama kayak input
    );
end entity;

architecture adder_3_archi of CS_unsigned is
    signal in_num : SIGNED (3 DOWNTO 0);
    signal out_num: SIGNED (3 DOWNTO 0);
begin
    in_num <= signed(input);
    out_num <= in_num + 3;
    output <= std_logic_vector(out_num);
end architecture;
```

5. .
   a. -5 (1 1011)



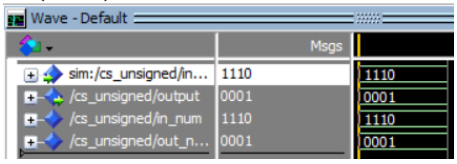

Hasil 1110 (-2)

   b. 5 ( 0101)



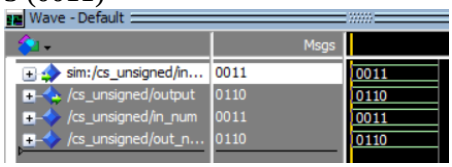

Hasil 1000 (8)

   c. -2 (1110)




Hasil 0001 (1)

   d. 3 (0011)




Hasil 0110 (6)

6. .
   - VHDL digunakan untuk buat rangkaian dengan kode
   - STD_LOGIC digunakan untuk menyimpan 1 bit data
   - STD_LOGIC_VECTOR digunakan untuk menyimpan banyak bit data
   - SIGN dan UNSIGN digunakan utk aritmatika, STD_LOGIC_VECTOR gak bisa aritmatika
   - MODELSIM digunakan utk simulasi kode
   - QUARTUS digunakan untuk melihat rangkaian yg dibuat