

[PETUNJUK Pengerjaan Case Study]

1. Hapus bagian PETUNJUK Pengerjaan ini ketika mengerjakan Case Study.
2. Kerjakan Case Study dengan template yang telah diberikan pada laman emas2.
3. Sertakan screenshot dari source code kalian untuk soal pemrograman.
4. Sertakan screenshot hasil simulasi rangkaian kalian untuk soal pemrograman.
5. Sertakan comment jika menurut kalian diperlukan.
6. Contoh:

```
-- Write your libraries / packages here
library ieee;
use ieee.std_logic_1164.all;

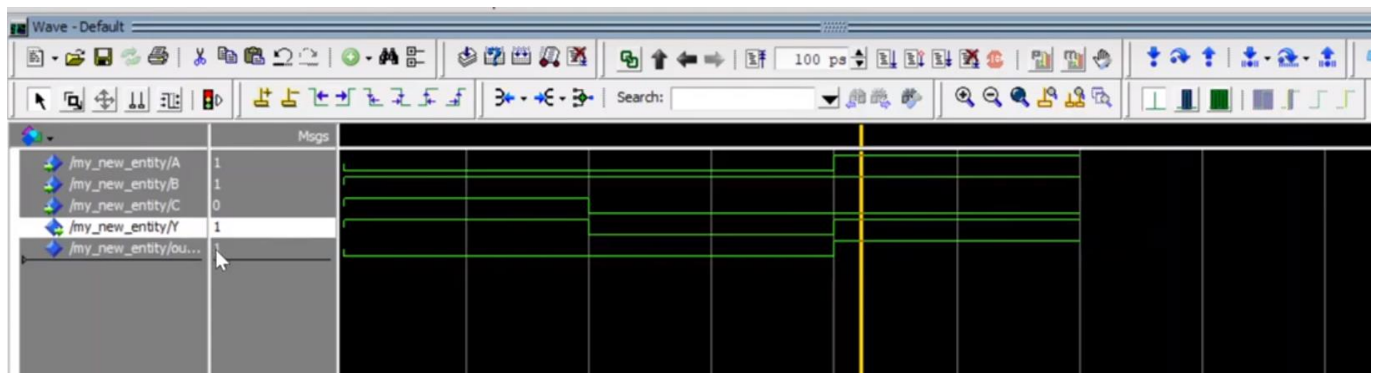
-- Write your entity here
entity my_new_entity is
port(
    -- Input
    A, B, C : IN STD_LOGIC;

    -- Output
    Y : OUT STD_LOGIC
);
end my_new_entity;

-- Write your architecture here
architecture new_architecture of my_new_entity is
    signal out_and : STD_LOGIC;
begin

    out_and <= A AND B;
    Y <= out_and OR C;

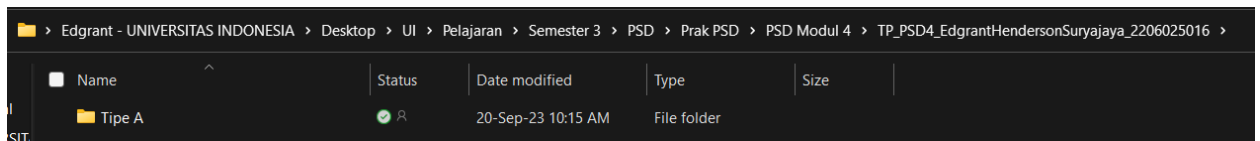
end new_architecture;
```



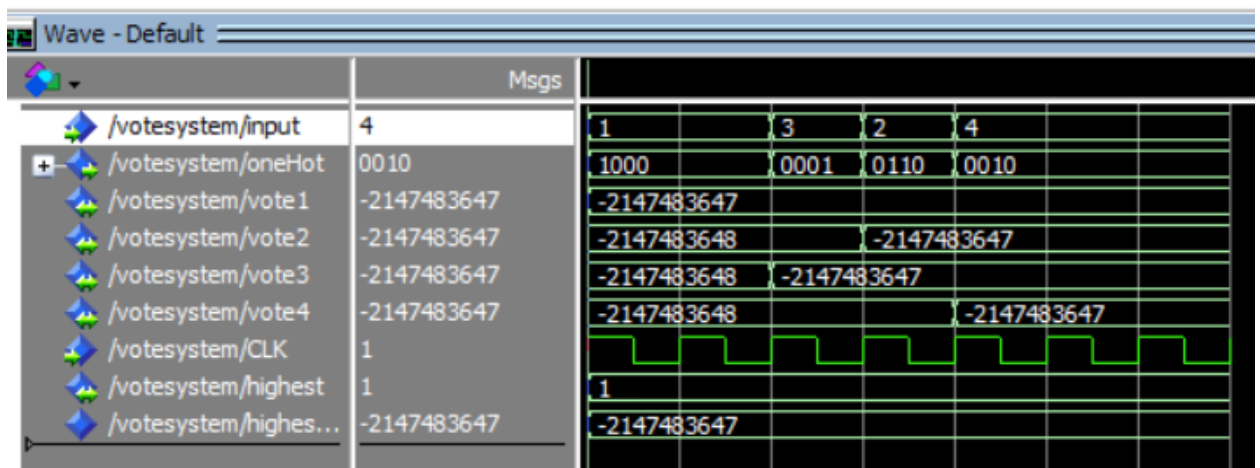
Case Study

Modul 4 : Testbench

1. Sudah didownload



2. Simulasi di model sim(1 → 1 → 3 → 2 → 4 → 4 → 4)



3. File testbench telah dibuat

Name	Status	Date modified	Type	Size
stimulus.txt	✓	20-Sep-23 10:09 AM	TXT File	1 KB
voteSystem.vhd	✓	20-Sep-23 10:09 AM	VHD File	2 KB
voteSystem_tb.vhd	✓	20-Sep-23 10:37 AM	VHD File	2 KB

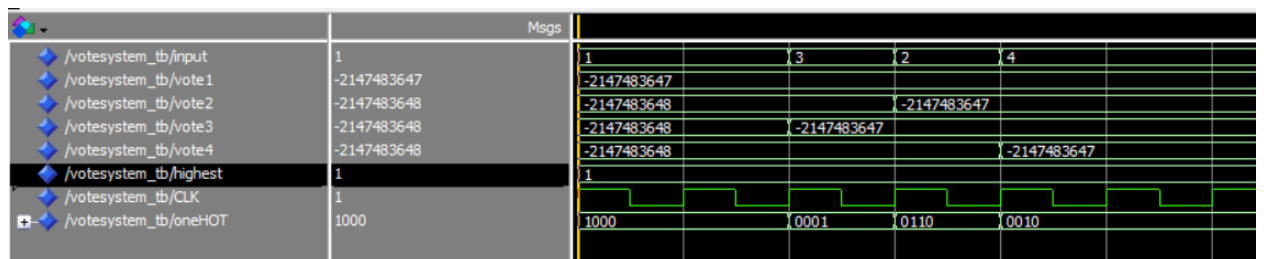
4. Pembuatan kode testbench

```

stimulus.txt  voteSystem.vhd  voteSystem_tb.vhd  ...  voteSystem_tb.vhd
C:\Users\Edgrant> OneDrive - UNIVERSITAS INDONESIA > Desktop > UI > Pelajaran > Semester 3 > PSD >
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  use IEEE.numeric_std.all;
4
5  entity votesystem_tb is
6  end entity votesystem_tb;
7
8  architecture rtl of votesystem_tb is
9      component voteSystem is
10         port (
11             input : IN integer;
12             oneHot : OUT STD_LOGIC_VECTOR(3 downto 0);
13             vote1 : INOUT integer;
14             vote2 : INOUT integer;
15             vote3 : INOUT integer;
16             vote4 : INOUT integer;
17             CLK : IN STD_LOGIC;
18             highest : INOUT integer
19         );
20     end component voteSystem;
21
22     signal input : integer; --input
23     signal vote1, vote2, vote3, vote4, highest : integer; --output
24     signal CLK : STD_LOGIC;
25     signal oneHOT : STD_LOGIC_VECTOR(3 downto 0);
26
27     -- constant input stream : integer --array of integer, tapi gak jadi
28     constant DELAY : time := 100 ps;
29
30     begin
31         -- membuat unit under test
32         UUT : voteSystem port map (
33             input => input,
34             oneHOT => oneHOT,
35             vote1 => vote1,
36             vote2 => vote2,
37             vote3 => vote3,
38             vote4 => vote4,
39             CLK => CLK,
40             highest => highest
41         );
42
43         tb_1: process
44         begin
45             input <= 1;
46             wait for DELAY;
47             input <= 1;
48             wait for DELAY;
49             input <= 3;
50             wait for DELAY;
51             input <= 2;
52             wait for DELAY;
53             input <= 4;
54             wait for DELAY;
55             input <= 4;
56             wait for DELAY;
57             input <= 4;
58             wait for DELAY;
59             wait;
60         end process tb_1;
61
62     end architecture rtl;
63

```

5. SS-an simulasi testbench



6. Kode revisi

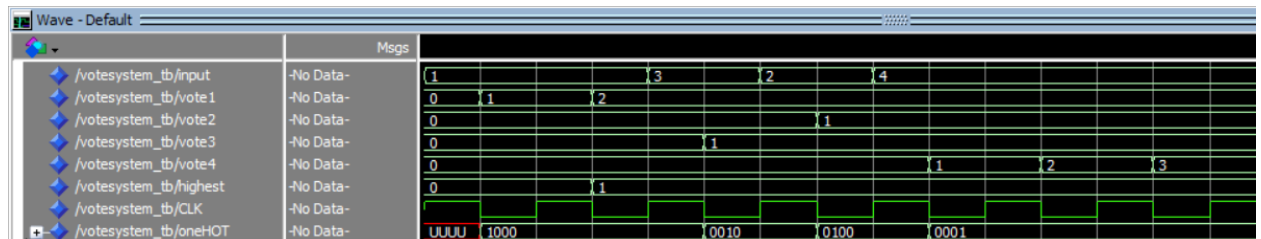
```

stimulus.txt  voteSystem.vhd  voteSystem_tb.vhd  voteSystem.vhd
RSITAS INDONESIA > Desktop > UI > Pelajaran > Semester 3 > PSD > Prak PSD > PSD Modul 4 > TP_PSD4_Edgr... C:\Users > Edgrant > OneDrive - UNIVERSITAS INDONESIA > Desktop > UI > Pelajaran > Semester 3 > PSD >

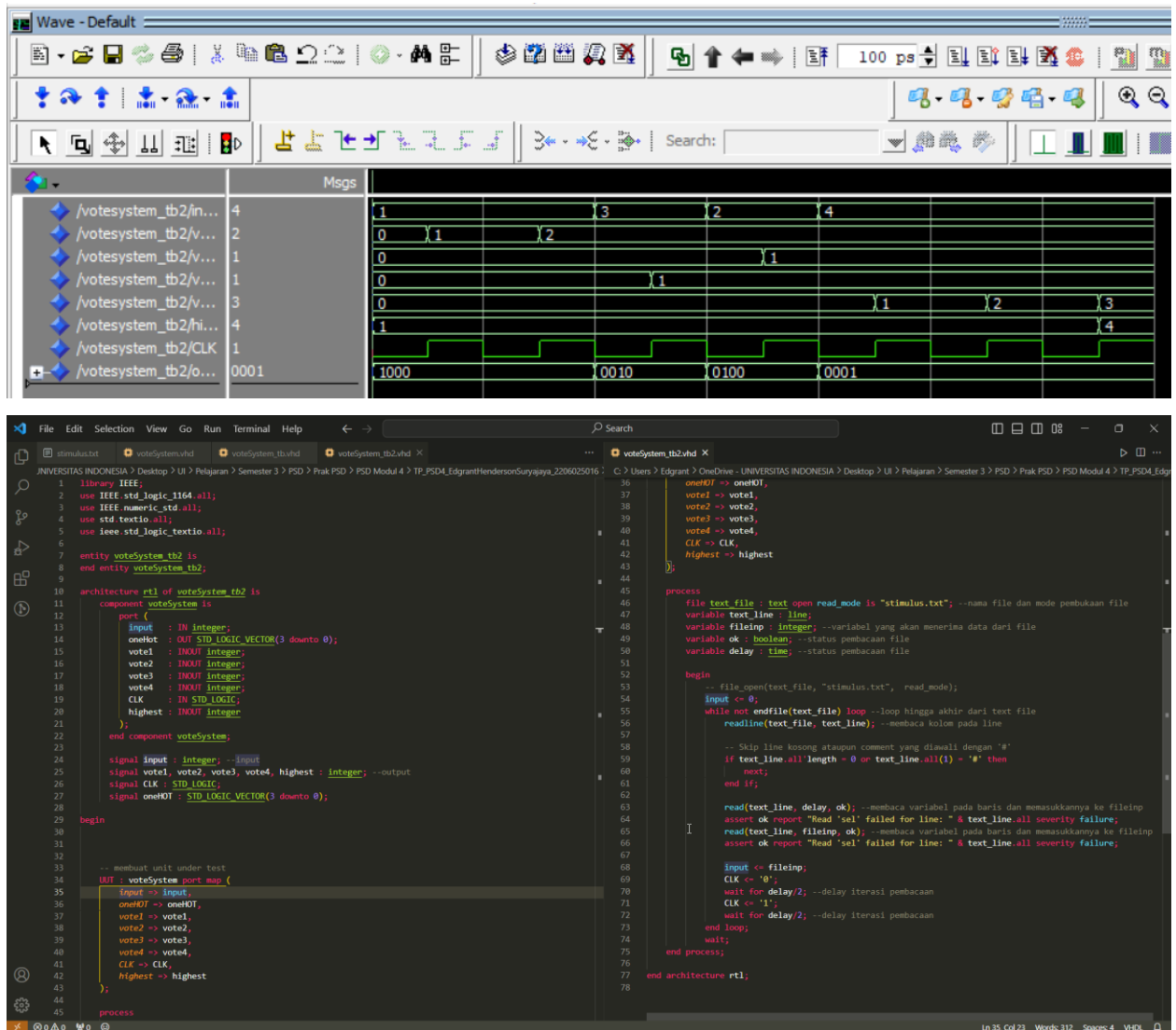
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  use IEEE.numeric_std.all;
4
5  entity voteSystem is
6  port (
7      input : IN integer;
8      oneHot : OUT STD_LOGIC_VECTOR(3 downto 0);
9      vote1 : INOUT integer := 0;
10     vote2 : INOUT integer := 0;
11     vote3 : INOUT integer := 0;
12     vote4 : INOUT integer := 0;
13     CLK : IN STD_LOGIC;
14     highest : INOUT integer := 0
15 );
16 end entity voteSystem;
17
18 architecture rtl of voteSystem is
19     signal highestVote : integer := 0;
20 begin
21
22     -- highestVote <= vote1; --# Error: voteSystem.vhd(23): near "highestVo
23     process(CLK)
24     begin
25         if falling_edge(CLK) then
26             if input = 1 then
27                 oneHot <= "1000";
28                 vote1 <= vote1 + 1;
29             elsif input = 2 then
30                 oneHot <= "0100";
31                 vote2 <= vote2 + 1;
32             elsif input = 3 then
33                 oneHot <= "0010";
34                 vote3 <= vote3 + 1;
35             elsif input = 4 then
36                 oneHot <= "0001";
37                 vote4 <= vote4 + 1;
38
39                 vote2 <= vote2 + 1;
40                 elsif input = 3 then
41                     oneHot <= "0010";
42                     vote3 <= vote3 + 1;
43                 elsif input = 4 then
44                     oneHot <= "0001";
45                     vote4 <= vote4 + 1;
46             else
47                 oneHot <= "0000";
48                 report "Input invalid" severity WARNING;
49             end if;
50
51             -- Check and update highestVote for all candidates
52             if vote1 > highestVote then
53                 highestVote <= vote1;
54                 highest <= 1;
55             end if;
56             if vote2 > highestVote then
57                 highestVote <= vote2;
58                 highest <= 2;
59             end if;
60             if vote3 > highestVote then
61                 highestVote <= vote3;
62                 highest <= 3;
63             end if;
64             if vote4 > highestVote then
65                 highestVote <= vote4;
66                 highest <= 4;
67             end if;
68         end if;
69     end process;
70 end architecture rtl;

```

Hasil running revisi



7. Buatlah sebuah testbench baru yang akan menguji rangkaian yang sama, tetapi kali ini inputnya menggunakan file “stimulus.txt” yang telah disediakan pada resource Emas! Sertakan code dan screenshot output pada modelsim!



8. Berdasarkan tiga metode pengujian yang dilakukan pada case study kali ini, metode mana yang menurut Anda paling efisien? Jelaskan!

Metode pengujian yang paling efisien adalah menggunakan file untuk membaca input, hal ini karena dengan menggunakan file, jika ingin diubah, sangat mudah, tinggal ubah nilai dalam file txt, tidak usah mengubah codingan.

9. Berikan kesimpulan pada praktikum kali ini dalam bentuk poin-poin!

- Testbench digunakan memberi nilai input untuk pengujian sebuah component vhdl
- Pada vhdl file dapat digunakan untuk membaca input
- Assert digunakan untuk menguji sebuah statment, jika statement false, assert akan mengeluarkan error dengan severitas tertentu
- Report untuk print dan dapat dikeluarkan saat statement di assert false.