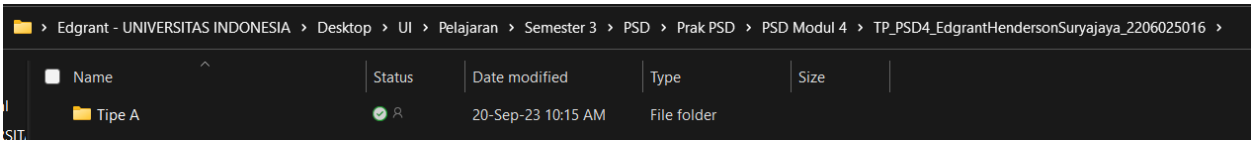
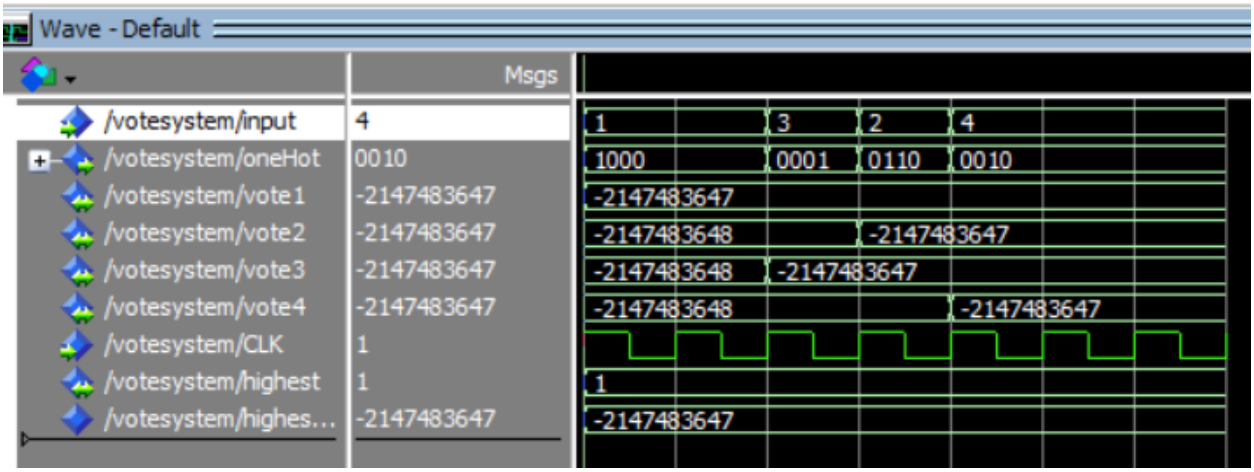
Case Study

Modul 4 : Testbench

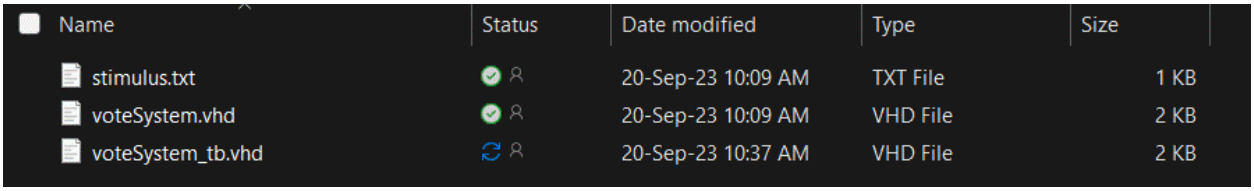
1. Sudah didownload



2. Simulasi di model sim(1 → 1 → 3 → 2 → 4 → 4 → 4)



3. File testbench telah dibuat



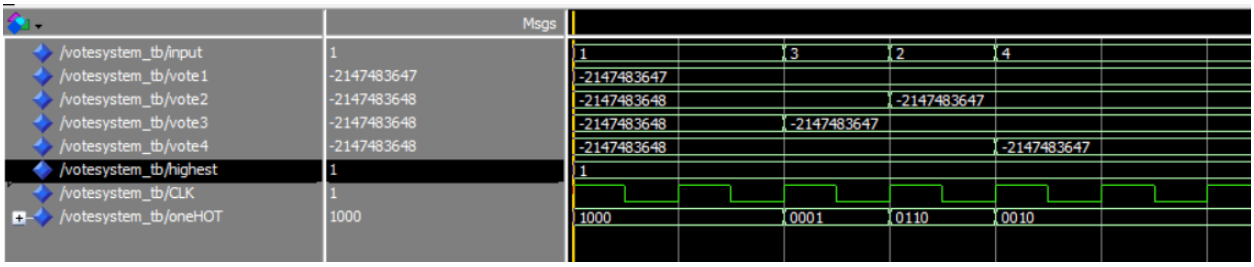
4. Pembuatan kode testbench

stimulus.txt | voteSystem.vhd | voteSystem_tb.vhd

C: > Users > Edgrant > OneDrive - UNIVERSITAS INDONESIA > Desktop > UI > Pelajaran > Semester 3 > PSD >

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity voteSystem_tb is
end entity voteSystem_tb;

architecture rtl of voteSystem_tb is
    component voteSystem is
        port (
          input   : IN integer;
          oneHot  : OUT STD_LOGIC_VECTOR(3 downto 0);
          vote1   : INOUT integer;
          vote2   : INOUT integer;
          vote3   : INOUT integer;
          vote4   : INOUT integer;
          CLK     : IN STD_LOGIC;
          highest : INOUT integer
        );
    end component voteSystem;

    signal input : integer; --input
    signal vote1, vote2, vote3, vote4, highest : integer; --output
    signal CLK : STD_LOGIC;
    signal oneHOT : STD_LOGIC_VECTOR(3 downto 0);

    --   constant input_stream : integer --array of integer, tapi gak jadi
    constant DELAY : time := 100 ps;

begin
    -- membuat unit under test
    UUT : voteSystem port map (
        input => input,
        oneHOT => oneHOT,
        vote1 => vote1,
        vote2 => vote2,
        vote3 => vote3,
        vote4 => vote4,
        CLK => CLK,
        highest => highest
    );

    tb_1: process
    begin
        input <= 1;
        wait for DELAY;
        input <= 1;
        wait for DELAY;
        input <= 3;
        wait for DELAY;
        input <= 2;
        wait for DELAY;
        input <= 4;
        wait for DELAY;
        input <= 4;
        wait for DELAY;
        input <= 4;
        wait for DELAY;
        wait;
    end process tb_1;

end architecture rtl;
```

5. SS-an simulasi testbench



6. Kode revisi

stimulus.txt | voteSystem.vhd | voteSystem_tb.vhd

RSITAS INDONESIA > Desktop > UI > Pelajaran > Semester 3 > PSD > Prak PSD > PSD Modul 4 > TP_PSD4_Edgr

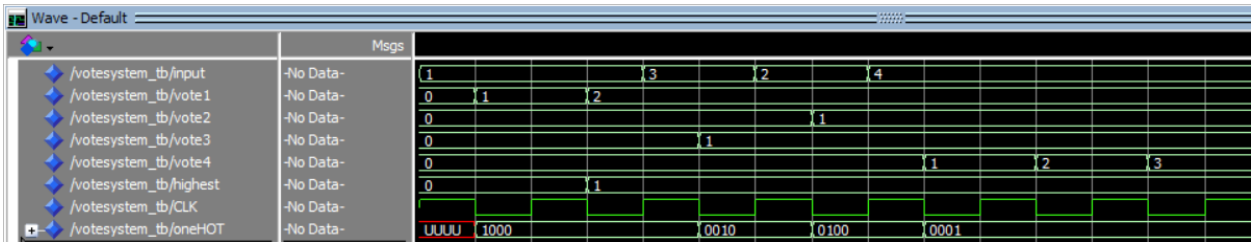
```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity voteSystem is
  port (
    input   : IN integer;
    oneHot  : OUT STD_LOGIC_VECTOR(3 downto 0);
    vote1   : INOUT integer := 0;
    vote2   : INOUT integer := 0;
    vote3   : INOUT integer := 0;
    vote4   : INOUT integer := 0;
    CLK     : IN STD_LOGIC;
    highest : INOUT integer := 0
  );
end entity voteSystem;

architecture rtl of voteSystem is
  signal highestVote : integer := 0;
begin

  -- highestVote <= vote1; --# ** Error: voteSystem.vhd(23): near "highestVo
  process(CLK)
  begin
    if falling_edge(CLK) then
      if input = 1 then
        oneHot <= "1000";
        vote1 <= vote1 + 1;
      elsif input = 2 then
        oneHot <= "0100";
        vote2 <= vote2 + 1;
      elsif input = 3 then
        oneHot <= "0010";
        vote3 <= vote3 + 1;
      elsif input = 4 then
        oneHot <= "0001";
        vote4 <= vote4 + 1;
```

voteSystem.vhd

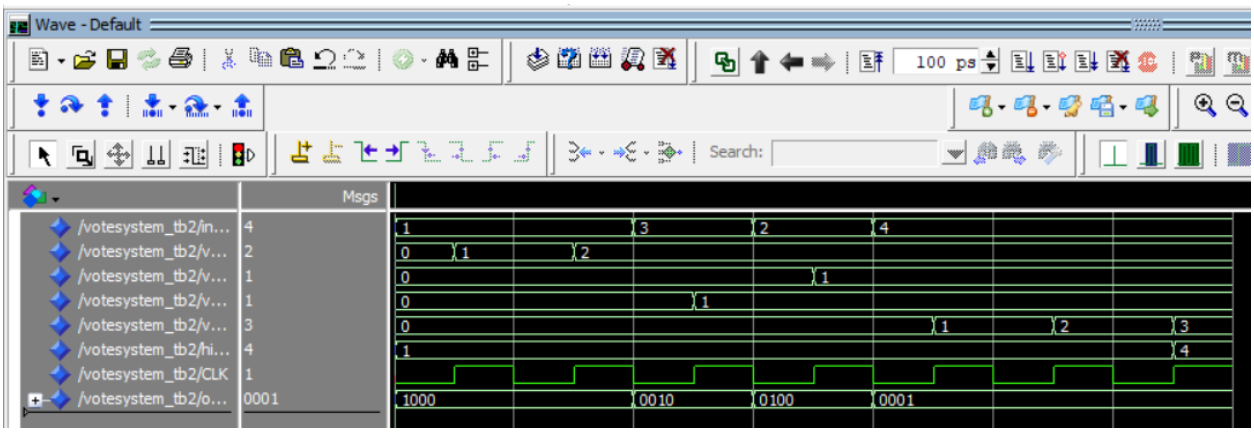
C: > Users > Edgrant > OneDrive - UNIVERSITAS INDONESIA > Desktop > UI > Pelajaran > Semester 3 > PSD >

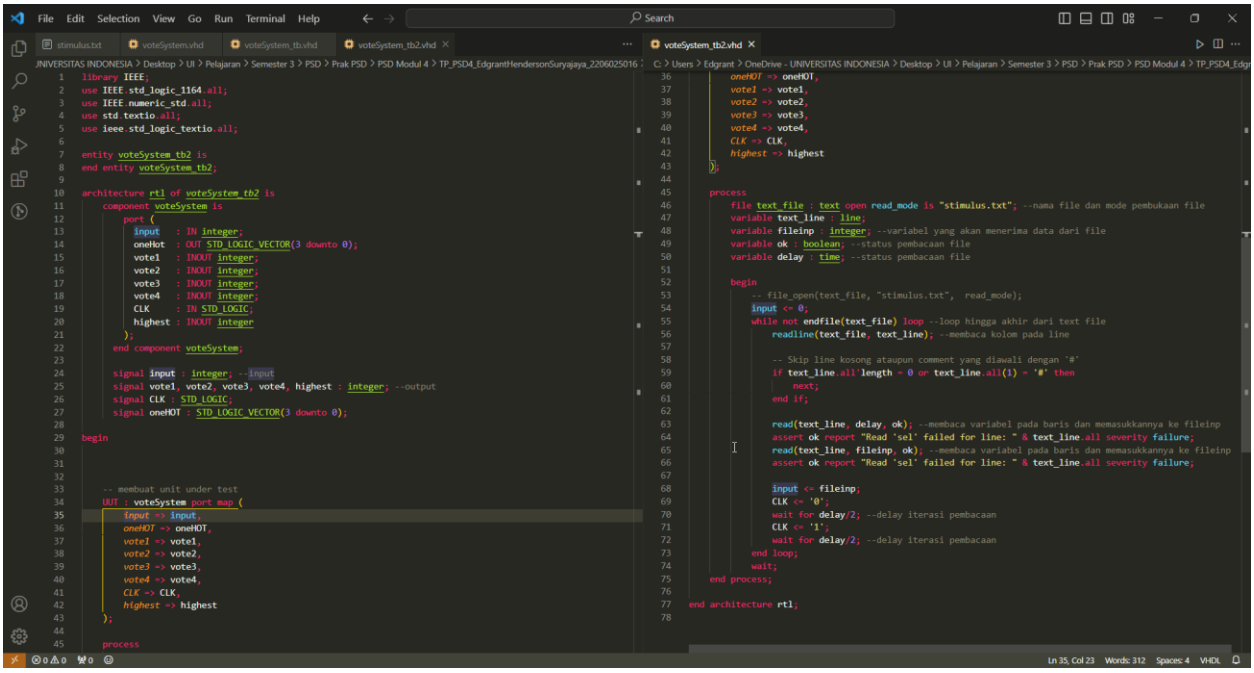
```
        vote2 <= vote2 + 1;
      elsif input = 3 then
        oneHot <= "0010";
        vote3 <= vote3 + 1;
      elsif input = 4 then
        oneHot <= "0001";
        vote4 <= vote4 + 1;
      else
        oneHot <= "0000";
        report "Input invalid" severity WARNING;
      end if;

      -- Check and update highestVote for all candidates
      if vote1 > highestVote then
        highestVote <= vote1;
        highest <= 1;
      end if;
      if vote2 > highestVote then
        highestVote <= vote2;
        highest <= 2;
      end if;
      if vote3 > highestVote then
        highestVote <= vote3;
        highest <= 3;
      end if;
      if vote4 > highestVote then
        highestVote <= vote4;
        highest <= 4;
      end if;
    end if;
  end process;
end architecture rtl;
```

Hasil running revisi



7. Buatlah sebuah testbench baru yang akan menguji rangkaian yang sama, tetapi kali ini inputnya menggunakan file “stimulus.txt” yang telah disediakan pada resource Emas! Sertakan code dan screenshot output pada modelsim!





8. Berdasarkan tiga metode pengujian yang dilakukan pada case study kali ini, metode mana yang menurut Anda paling efisien? Jelaskan!

Metode pengujian yang paling efisien adalah menggunakan file untuk membaca input, hal ini karena dengan menggunakan file, jika ingin diubah, sangat mudah, tinggal ubah nilai dalam file txt, tidak usah mengubah codingan.

9. Berikan kesimpulan pada praktikum kali ini dalam bentuk poin-poin!
    - Testbench digunakan memberi nilai input untuk pengujian sebuah component vhdl
    - Pada vhdl file dapat digunakan untuk membaca input
    - Assert digunakan untuk menguji sebuah statment, jika statement false, assert akan mengeluarkan error dengan severitas tertuntu
    - Report untuk print dan dapat dikeluarkan saat statement di assert false.