Digital Laboratory

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1. Nomor satu

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity TP_PSD5_EdgrantHendersonSuryajaya_2206025016 is
    port (
        a, b        : IN std_logic_vector (7 downto 0);
        alu_control : IN std_logic_vector (2 downto 0);
        alu_result  : OUT std_logic_vector (7 downto 0);
        zeroflag    : OUT std_logic
    );
end entity TP_PSD5_EdgrantHendersonSuryajaya_2206025016;

architecture rtl of TP_PSD5_EdgrantHendersonSuryajaya_2206025016 is
    signal aNum, bNum, result : signed (7 downto 0);
begin
    aNum <= signed(a);
    bNum <= signed(b);

    process(aNum, bNum, alu_control)
    begin
        case alu_control is
            when "000" => result <= aNum + bNum;
            when "001" => result <= aNum - bNum;
            when "010" => result <= aNum and bNum;
            when "011" => result <= aNum or bNum;
            when "100" => result <= aNum xor bNum;
            when "101" => result <= -aNum;
            when "110" => result <= aNum + 1;
            when "111" => result <= aNum - 1;
            when others => result <= "00000000";
        end case;
    end process;

    zeroflag <= '1' when result = "00000000" else '0';
    alu_result <= std_logic_vector(result);
end architecture rtl;
```

2. Nomor dua

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity TP_PSD5_EdgrantHendersonSuryajaya_2206025016_2 is
    port (
        clk, reset      : IN std_logic;
        reg_write_en    : IN std_logic := '0';
        reg_write_dest  : IN std_logic_vector (1 downto 0) := (others => '0');
        reg_write_data  : IN std_logic_vector (7 downto 0) := (others => '0');
        reg_read_addrA  : IN std_logic_vector (1 downto 0) := (others => '0');
        reg_read_addrB  : IN std_logic_vector (1 downto 0) := (others => '0');
        reg_read_dataA  : OUT std_logic_vector (7 downto 0);
        reg_read_dataB  : OUT std_logic_vector (7 downto 0)
    );
end entity TP_PSD5_EdgrantHendersonSuryajaya_2206025016_2;

architecture rtl of TP_PSD5_EdgrantHendersonSuryajaya_2206025016_2 is
    type RegisterArray is array (0 to 3) of std_logic_vector (7 downto 0);
    signal registers: RegisterArray := (others => (others => '0'));
begin
    TP_B: process(clk, reset)
    begin
        if reset = '1' then
            registers <= (others => (others => '0'));
        elsif rising_edge(clk) then
            if reg_write_en = '1' then
                registers(to_integer(unsigned(reg_write_dest))) <= reg_write_data;
            end if;
        end if;
    end process TP_B;
    TP_C: process(clk)
    begin
        if rising_edge(clk) then
            reg_read_dataA <= registers(to_integer(unsigned(reg_read_addrA)));
            reg_read_dataB <= registers(to_integer(unsigned(reg_read_addrB)));
        end if;
    end process TP_C;
end architecture rtl;
```