SMP CACHE SIMULATOR

1. What is Cache Memory and why it is important.

Cache Memory it is a fast, volatile memory storing frequently accessed data to boost system performance. Acts as a bridge, reducing the data access time gap between CPU and main memory (GeeksforGeeks, 2021).
Cache Memory it is important because is crucial for designing efficient computer architectures. Improves the speed and the performance of computing task by reducing latency (GeeksforGeeks, 2021).

1.1 Key Features of Cache Memory

- **Efficiency:** Cache memory runs at a higher speed compared to the main memory, enabling quicker data retrieval for the CPU (GeeksforGeeks, 2021).
- **Location:** Located near the CPU, typically on the CPU chip itself, to cut down data access time (GeeksforGeeks, 2021).
- **Purpose:** Holds frequently accessed data and instructions temporarily, reducing reliance on the slower main memory (GeeksforGeeks, 2021).

1.2 Role of Cache Memory

- Cache memory is essential for computer efficiency, offering quicker data access (GeeksforGeeks, 2021).
- It serves as a mediator between the CPU and RAM (GeeksforGeeks, 2021).
- Its main function is to lower the average data access time, boosting system performance (GeeksforGeeks, 2021).

1.3 Benefits of Cache Memory

- **Quick Access:** Positioned close to the CPU, cache memory is faster than main memory and stores a portion of data and instructions (GeeksforGeeks, 2021).

- **Minimizing Latency:** Utilizes locality principles to shorten data retrieval times (GeeksforGeeks, 2021).
- **Decreasing Traffic:** By minimizing main memory access, it cuts down on bus traffic, enhancing system efficiency (GeeksforGeeks, 2021).
- **Boosting CPU Efficiency:** The CPU operates more effectively, executing more instructions and waiting less for memory access (GeeksforGeeks, 2021).
- **Improving Scalability:** Diminishes the effects of memory latency, helping improve system scalability (GeeksforGeeks, 2021).

1.4 Types of Cache Memory

- **L1 or Level 1 Cache:** The first level of cache memory, located inside the processor. Each core of the processor has its own small L1 cache, typically ranging from 2KB to 64KB (GeeksforGeeks, 2021).
- **L2 or Level 2 Cache:** The second level of cache, which can be inside or outside the CPU. If external to the core, it may be shared between two cores, depending on the architecture. Connected to the processor via a high-speed bus, with sizes typically between 256KB and 512KB (GeeksforGeeks, 2021).
- **L3 or Level 3 Cache:** The third level of cache, fount outside the CPU shared by all CPU cores. Present in high-end the processors to enhance the performance of L1 and L2 caches. Usually ranges in size from 1MB to 8 MB (GeeksforGeeks, 2021).]

Cache Memory in Modern Computer Systems

In contemporary computer systems, cache memory plays a crucial role by boosting CPU performance and efficiency. By keeping frequently used data close to the CPU, it cuts down on retrieval times and reduces latency. This tiered storage approach allows essential data to be accessed swiftly, thereby enhancing the overall speed of computing task (Redis, 2024).

2.1 Real World Examples of Cache Memory Usage

Cache memory finds extensive use in many practical applications to improve efficiency for example:

- **Web Browser:** Cache recently visited web pages, enabling quicker load times on future visits (Redis, 2024).
- **Database Management Systems:** Utilise cache to keep often-accessed data, enhancing the speed of database queries (Redis, 2024).
- **Operating Systems:** Implement cache for rapid access for frequently used files and programs, boosting overall system performance (Redis, 2024).

2.2 Future Trends in Cache Memory

The outlook for cache memory is bright with emerging trends:

- **Non-Volatile Memory (NVM):** Innovations like MRAM and RRAM promise to blend the speed of cache with the durability of storage (Redis, 2024).
- **3D-Stacked Memory:** Aims to enhance storage capacity and cut down latency trough vertical stacking of memory layers (Redis, 2024).
- **AI and Machine Learning:** Cutting-edge algorithms are being created to better predict data access, thus optimising cache utilisation (Redis, 2024).
- **Quantum Computing:** Efforts are underway to tailor cache memory for quantum computers, which could drastically alter data processing methods (Redis, 2024).

Tools for Simulating and Analysing Cache Memory

To effectively simulate analyse cache memory performance, several tools and software packages are available. These tools help in understanding cache behaviour, evaluating performance metrics, and optimising cache configurations (Technowriteups, 2023)

3.1 Common Tools for Cache Memory Simulation

- **SMPCache:** This is a specialised tool designed for simulating multi-level cache memory systems. It allows users to configure various cache parameters, run simulations, and analyse performance metrics such as hit rate, miss rate, and access time (Technowriteups, 2023).

  Features and Benefits:

  - User-Friendly Interface: Simplifies the process of setting up and running simulations (Technowriteups, 2023).
  - Comprehensive Analysis: Provides detailed performance metrics to evaluate cache system performance (Technowriteups, 2023).
  - Educational Value: Ideal for coursework and research projects, aligning well with advanced computer architecture lectures (Technowriteups, 2023).

- **Redis:** This is an-in-memory data structure store that can be used as a cache, database, and message broker. It supports various data structures such as strings, hashes, lists, sets, and more (Technowriteups, 2023).

  Features and Benefits:

  - High Performance: Provides low-latency and high-throughput data access (Technowriteups, 2023).
  - Versatile Usage: Can be used for caching, session management, real-time analytics, and more (Technowriteups, 2023).
  - Scalability: Supports data replication, persistence, and partitioning (Technowriteups, 2023).

- **Memcached:** This is a distributed memory caching system used to speed up dynamic web applications by alleviating database load (Technowriteups, 2023).

  Features and Benefits:

- Simple Design: Easy to deploy and maintain (Technowriteups, 2023).
- High Performance: Provides quick and efficient data retrieval from memory (Technowriteups, 2023).
- Scalability: Can be deployed across multiple servers for improved performance (Technowriteups, 2023).

- **Varnish Cache:** This is a web application accelerator designed to cache and speed up web content delivery (Technowriteups, 2023).

  Features and Benefits:

  - High Efficiency: Caches HTTP content to improve web application performance (Technowriteups, 2023).
  - Flexibility: Configurable using Varnish Configuration Language (VCL) (Technowriteups, 2023).
  - Improved User Experience: Reduces server load and enhances response times for web users (Technowriteups, 2023).

- **Apache Ignite:** This is an-in-memory computing that includes and in-memory data grid and caching capabilities (Technowriteups, 2023).

  Features and Benefits:

  - Integrated Platform: Combines in-memory data grid, compute grid, and streaming (Technowriteups, 2023).
  - High Performance: Supports real-time processing and low-latency data access (Technowriteups, 2023).
  - Scalability: Can scale horizontally by adding more nodes to the cluster (Technowriteups, 2023).

SMPCache Simulator Project

This project is to understand cache memory system design and evaluate its performance using the SMPCache Simulator. The project explores the configuration of cache systems, runs simulations for different coherence

protocols, and analyzes results to compare the effectiveness of various configurations.

System Configuration

The simulation was performed using SMPCache Simulator on Windows 11 in a UTM virtualised environment. The following configuration was used:

- **Cache Configuration**
  - Cache Levels: 3 (L1, L2, L3)
  - Cache Sizes:

    L1: 2KB (64 blocks)

    L2: 16KB (512 blocks)

    L3: 64KB (2048 blocks)
  - Block Size: 32 bytes
  - Replacement Policy: LRU
  - Mapping: Set-associative
- **Main Memory Configuration**
  - Total Memory Size: 1MB (32,768 blocks)
  - Word Size: 32 bits
  - Block Size: 32 bytes
- **Multiprocessor Configuration**
  - Protocols Tested: MSI, MESI, DRAGON
  - Number of Processors: 4
  - Snoopy Protocol: MSI
  - Bus Arbitration: Random

Simulation Results

Performance Metrics

The Following results were recorded for each protocol:

Protocol	Global Read Hits	Global Read Misses	Global Write Hits	Global Write Misses	Local Read Hits	Local Read Misses	Local Write Hits	Local Write Misses
MSI	4	2	5	1	4	2	5	1
MESI	4	2	5	1	0	2	0	1
DRAGON	4	2	5	1	0	2	0	1

Calculate Key Metrics

Hits Rate Formula:

$$\text{Hit Rate} = \frac{\text{Hits}}{\text{Hits} + \text{Misses}} \text{ X } 100$$

Global (%)

- **MSI:**

$$\text{Global Read Hit Rate} = \frac{4}{4+2} \text{ X } 100 = 66.67\%$$

$$\text{Global Write Hit Rate} = \frac{5}{5+1} \text{ X } 100 = 83.33\%$$

- **MESI and DRAGON:** The global hit rates remain the same as MSI since the global reading do not differ.

Local (%)

- **MSI:**

$$\text{Local Read Hit Rate} = \frac{4}{4+2} \text{ X } 100 = 66.67\%$$

$$\text{Local Write Hit Rate} = \frac{5}{5+1} \text{ X } 100 = 83.33\%$$

- **MESI and DRAGON:**

$$\text{Local Read Hit Rate} = \frac{0}{0+2} \text{ X } 100 = 0\%$$

$$\text{Local Write Hit Rate} = \frac{0}{0+1} \text{ X } 100 = 0\%$$

Miss Rate Formula:

Read Miss Rate = 100 – Read Hit Rate

Write Miss Rate = 100 – Read Hit Rate

Global (%)

- **MSI:**

Read Miss Rate = 100 – 66.67 = 33.33%

Write Miss Rate = 100 – 83.33 = 16.67%

- **MESI and DRAGON:**

Read Miss Rate = 100 – 0 = 100%

Write Miss Rate = 100 – 0 = 100%

Key Observations

Global Performance:

- All protocols exhibit the same global read/write hit rates (66.67% and 83.33%, respectively).
- This indicates similar performance for global cache operations across protocols.

Local Performance:

- MSI significantly outperforms MESI and DRAGON in local cache hit rates.
- MESI and DRAGON rely more on coherence mechanisms, resulting in 0% local hit rates for reads and writes.

Implications of Protocols:

- MSI prioritizes local cache usage, leading to higher hit rates locally.
- MESI and DRAGON reduce bus traffic but may incur higher latencies due to remote data fetching.

BUS Transactions Analysis

While bus transactions like BusRd, BusRdX, BusWb, and BusUpd were not detailed in this report, these metrics provide insights into coherence overhead. Future analysis should include:

- Counting the number of each transaction type.
- Comparing bus traffic for different protocols.

Conclusion

The SMPCache Simulator project has successfully demonstrated the complexities and performance implications of cache memory systems. By simulating various cache configurations, we have been able to analyse key metrics such as hit rate, miss rate, and overall system performance. Through careful design and simulation, we gained valuable insights into how different cache parameters, like size, associativity, and replacement policies, affect the efficiency of memory access.

This project provided a deep understanding of the trade-offs involved in cache memory design, offering a foundation for optimizing system performance in real-world applications. The results obtained from the simulations serve as a useful reference for future hardware and software optimizations, as well as for further exploration into more advanced cache architectures.

Ultimately, the SMPCache Simulator has been an effective tool in enhancing our understanding of cache memory dynamics and its critical role in modern computing systems. This work contributes to the broader field of computer architecture and lays the groundwork for future advancements in memory systems design.

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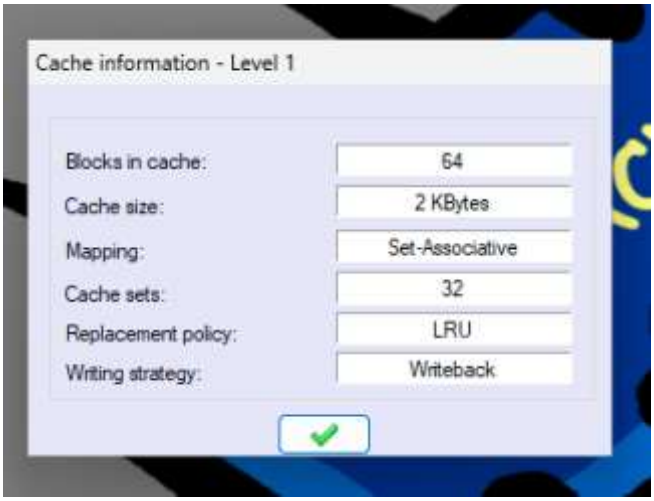
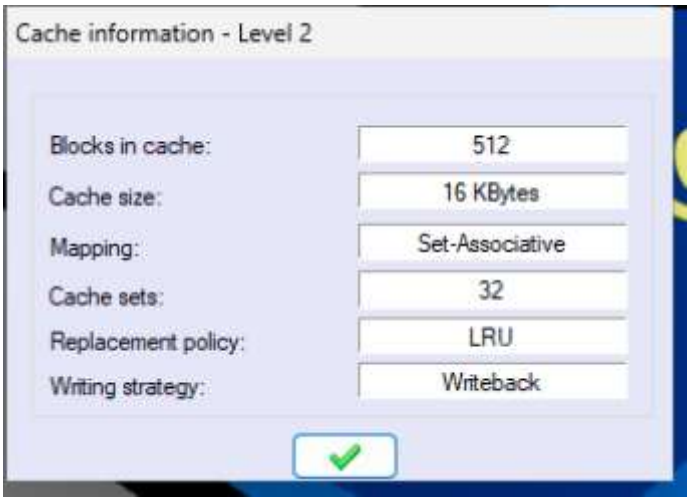
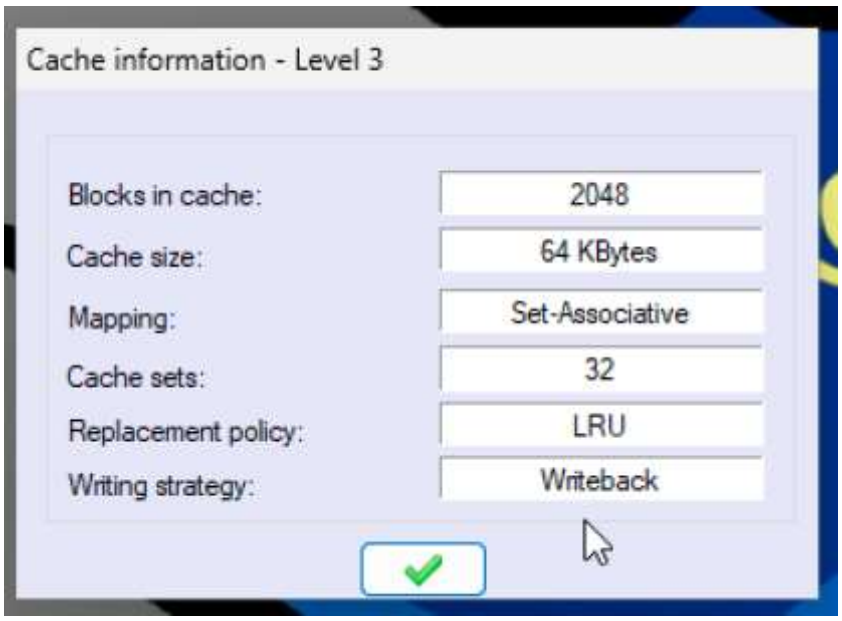
- GeeksforGeeks. (2021). Cache Memory. [online] Available at: https://www.geeksforgeeks.org/cache-memory/..
- Redis. (2024). Cache Memory - Definition and general information. [online] Available at: https://redis.io/glossary/cache-memory/
- Technowriteups (2023). 8 Top Open-Source Caching Tools in 2023 - Technowriteups - Medium. [online] Medium. Available at: https://medium.com/@technowriteups/8-top-open-source-caching-tools-in-2023-3f0910abc682

APENDIX A

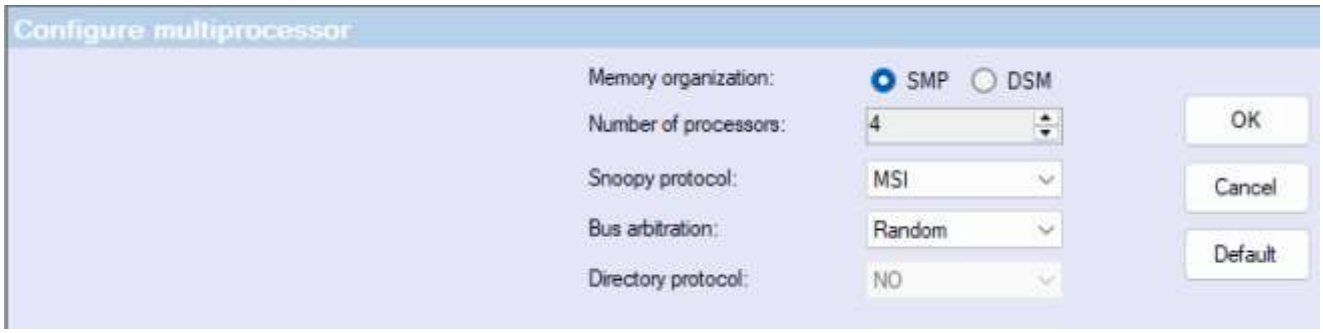
CACHE CONFIGURATION:



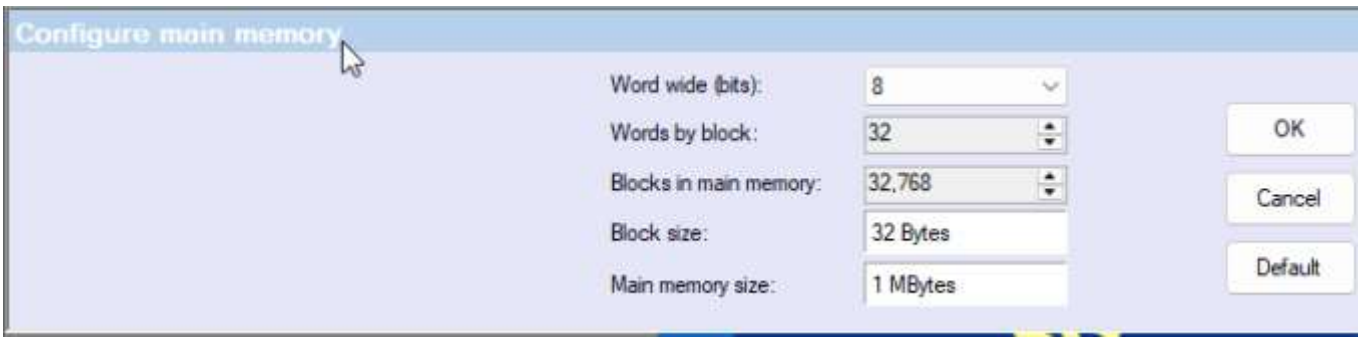




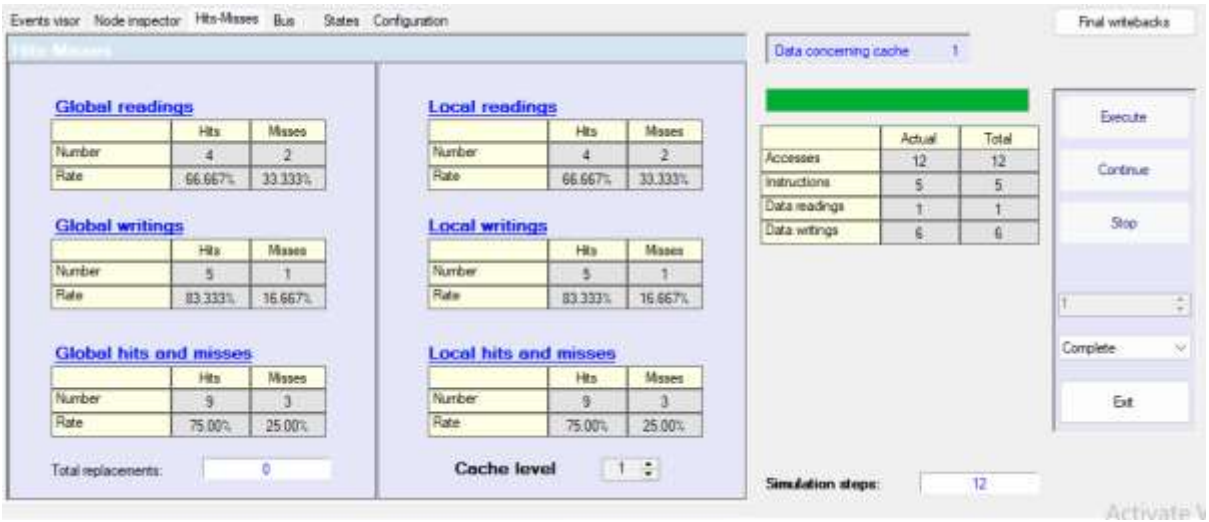
Multiprocessor Configuration



Main Memory Configuration



MSI LEVEL 1



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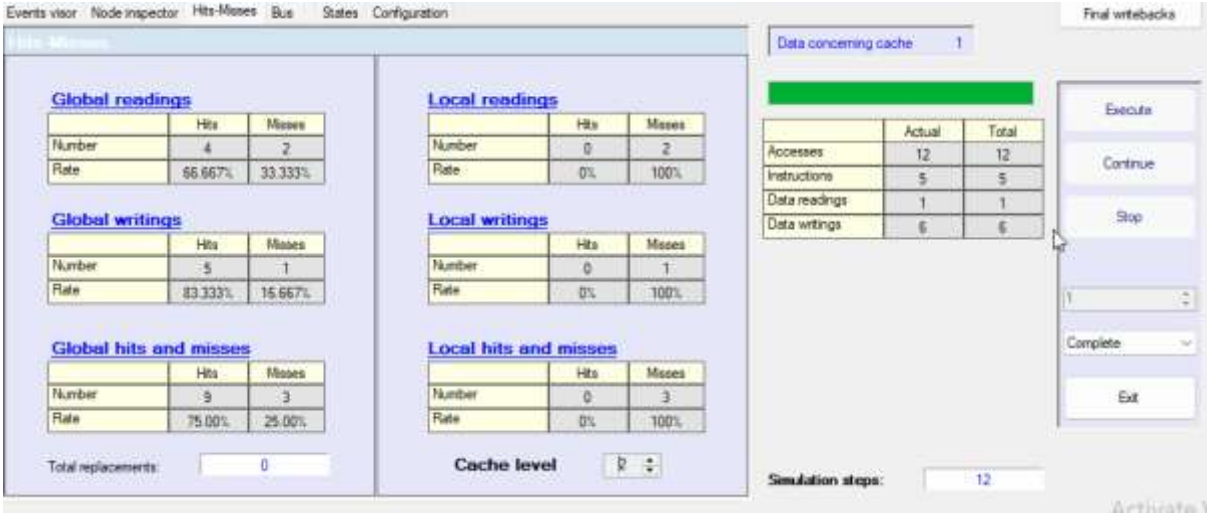

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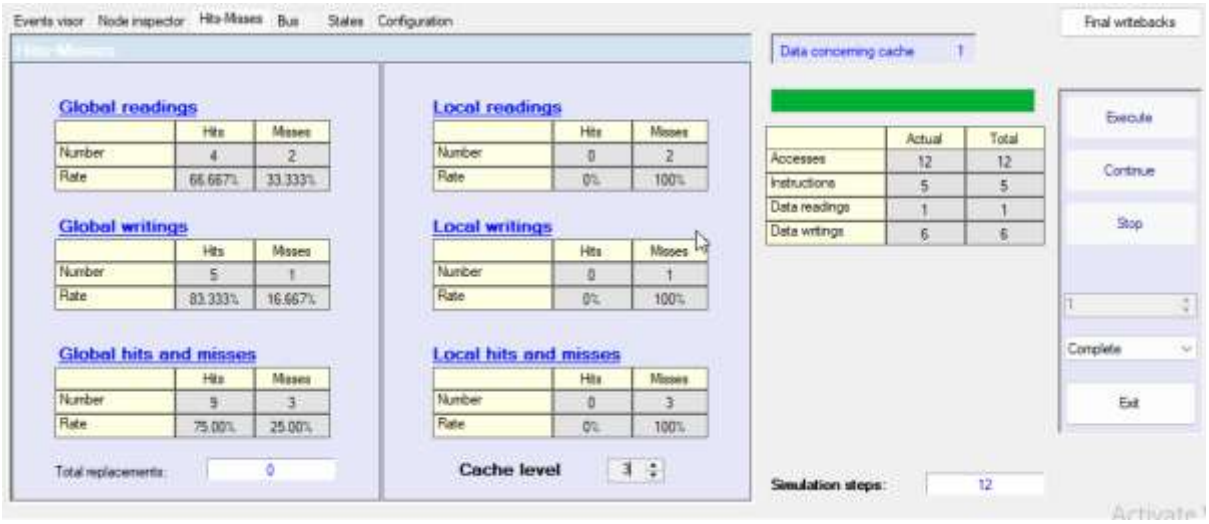
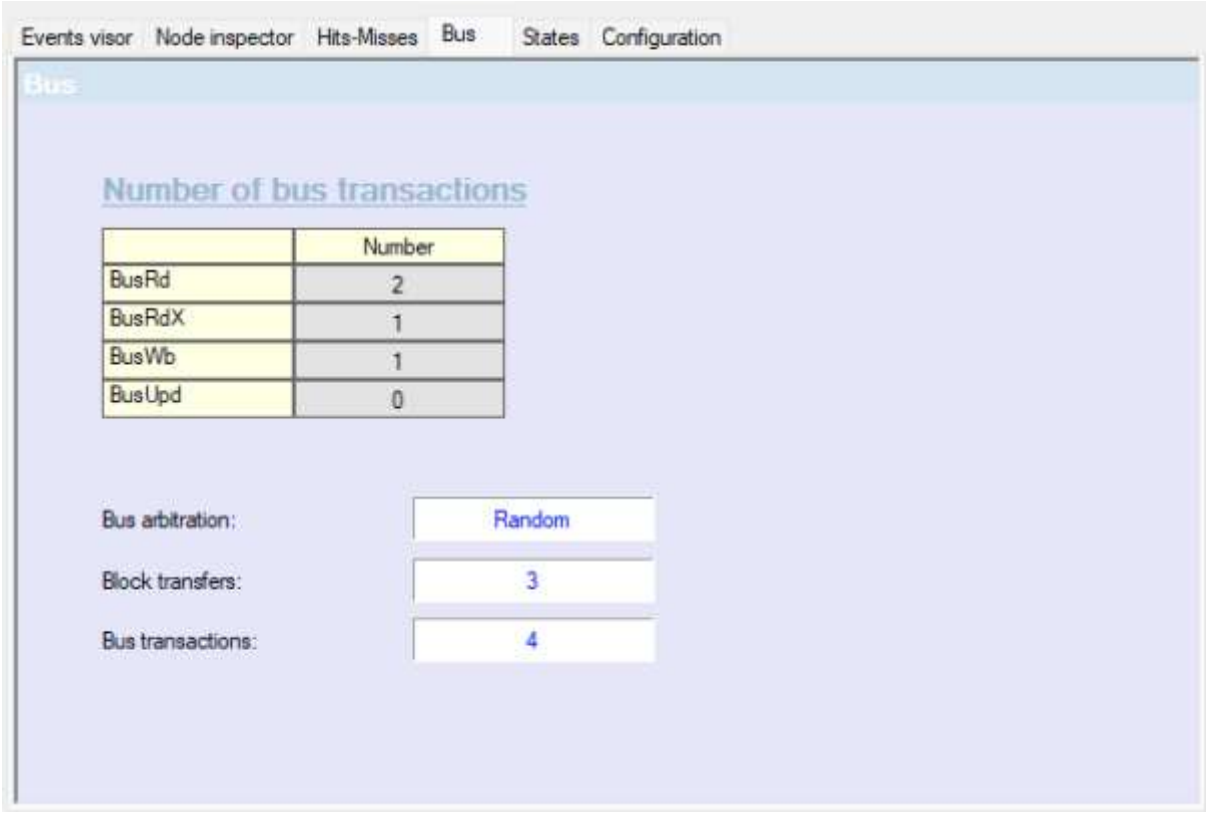
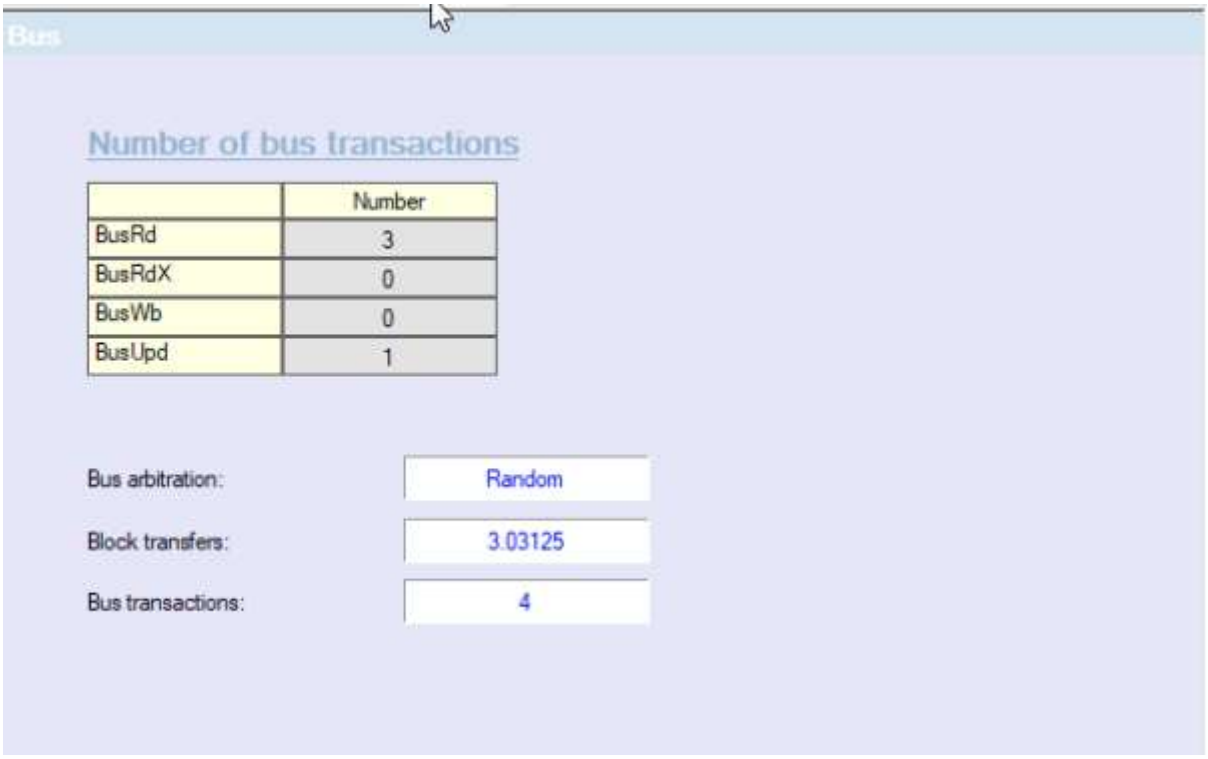


BUS MSI

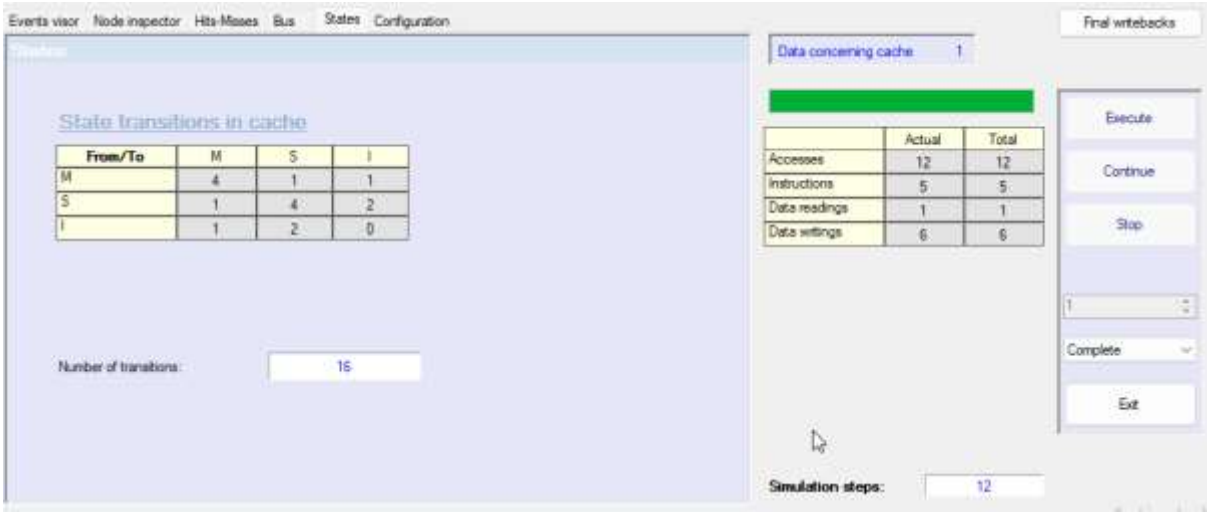
BUS MESI



BUS DRAGON

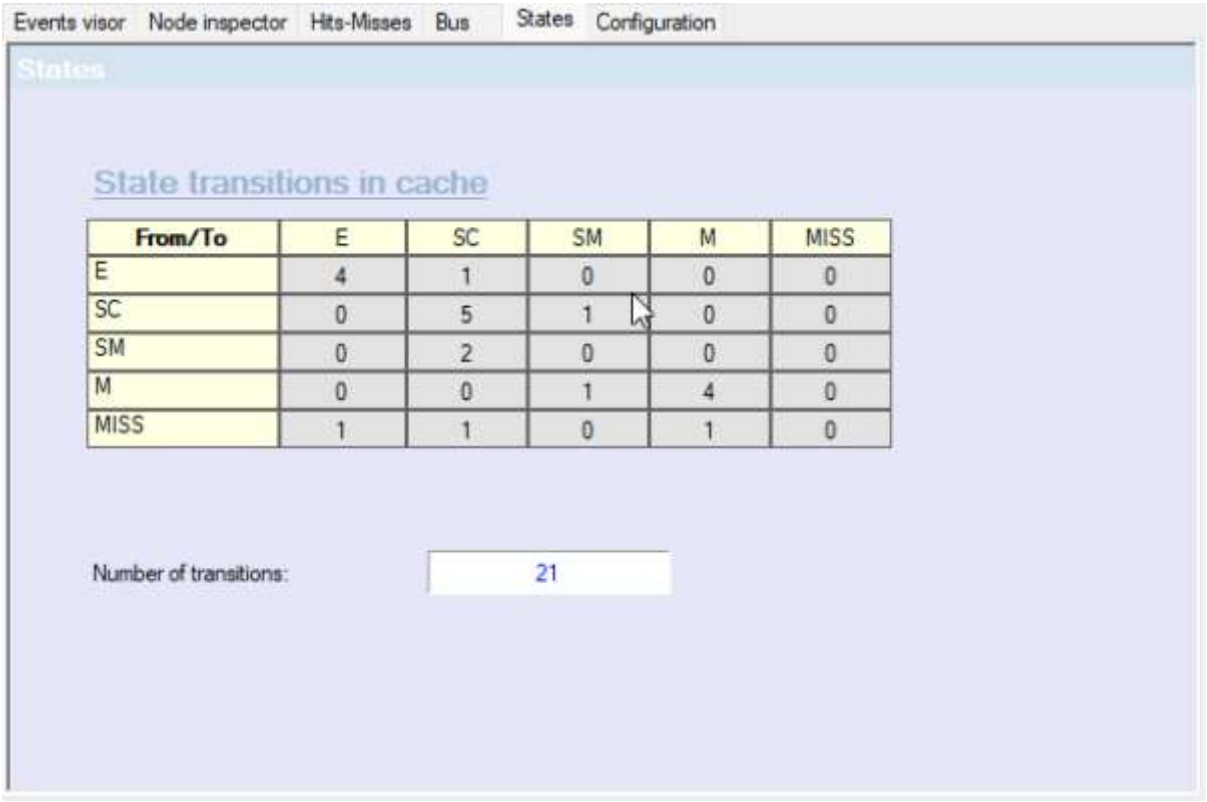


STATES MSI

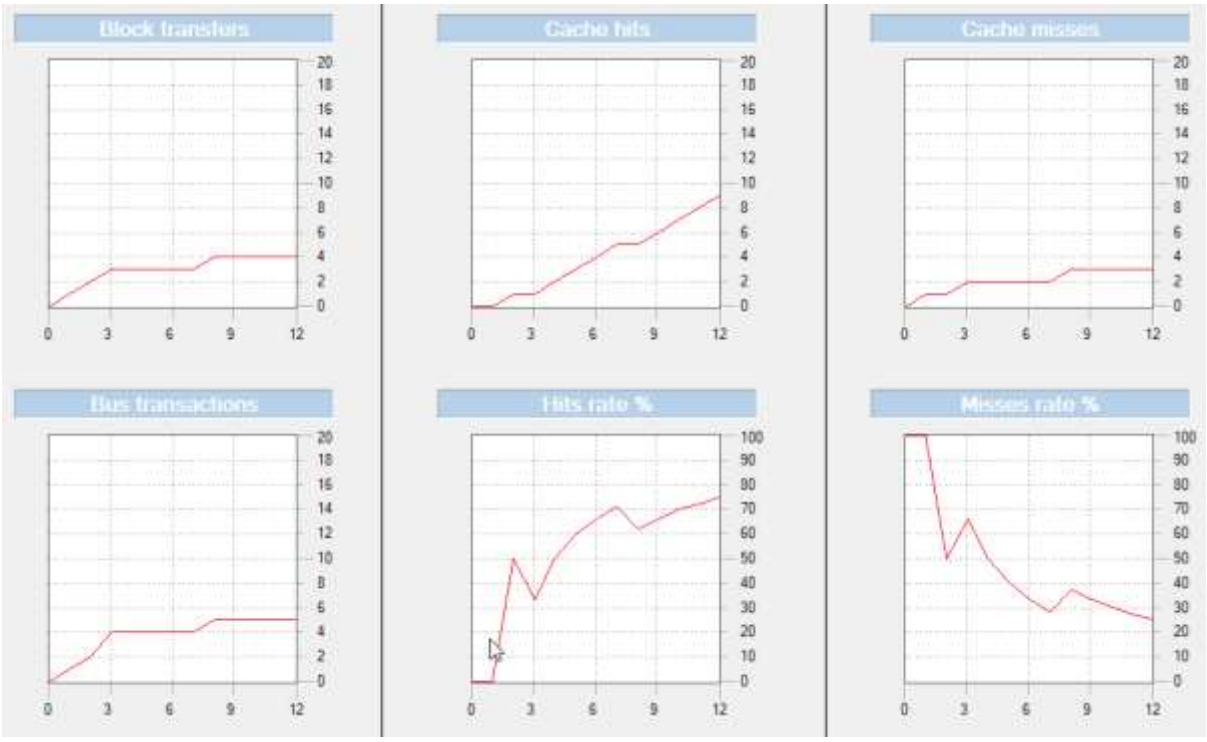


STATES MESI

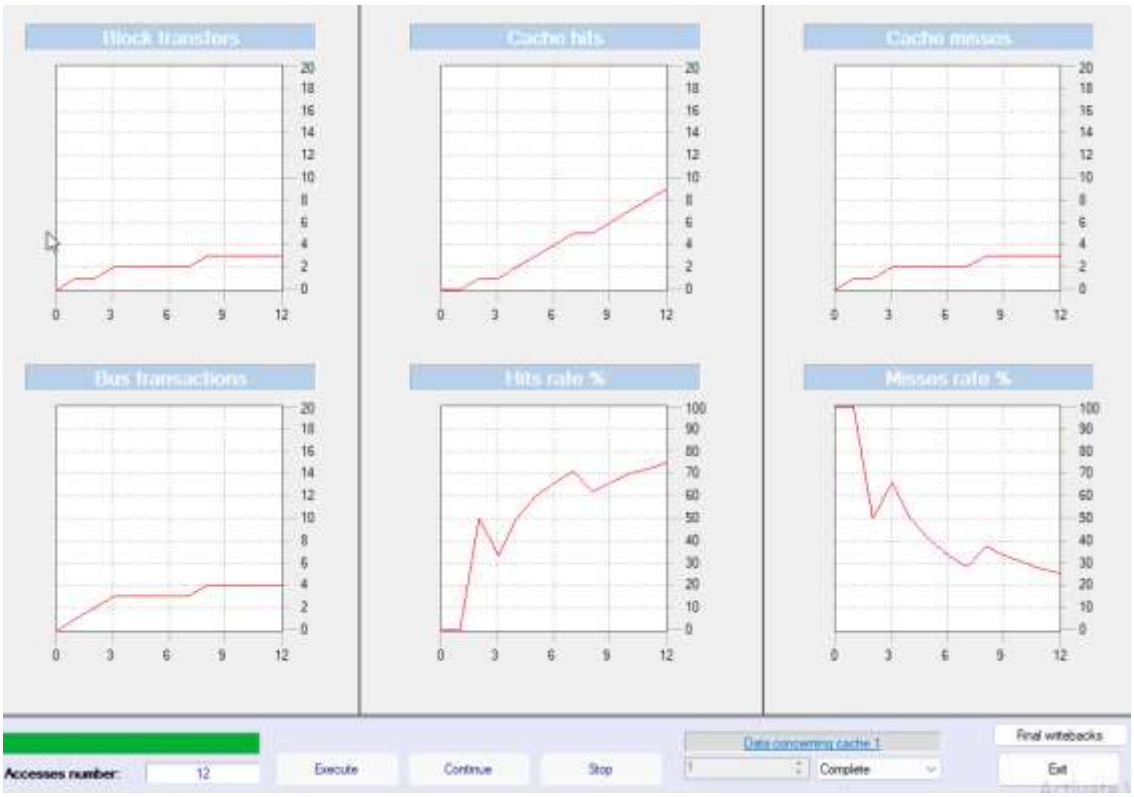
STATES DRAGON



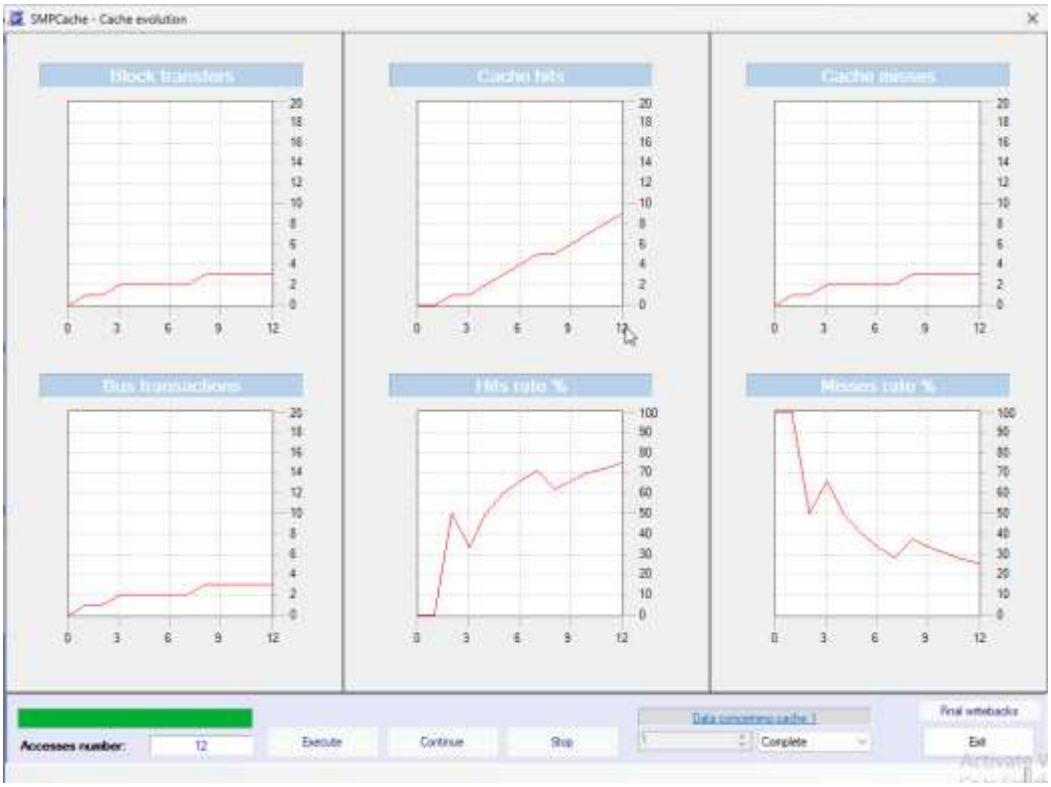
GRAPHIC MSI



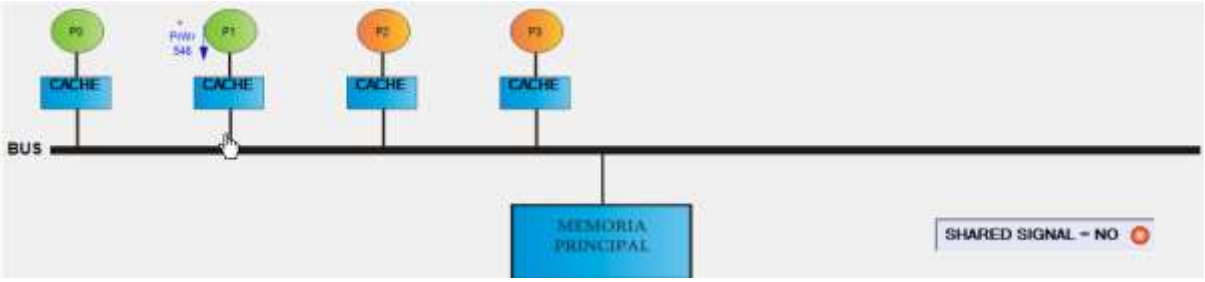
GRAPHIC MESI



GRAPHIC DRAGON



P0 – P3


P0
P1
P2
P3
CACHE
CACHE
CACHE
CACHE
BUS
MEMORIA
PRINCIPAL
SHARED SIGNAL – NO