**The instruction set of the RISC**[**processor**](https://www.fpga4student.com/2017/01/verilog-code-for-single-cycle-MIPS-processor.html)**:**

1. **Memory Instructions**

* Load

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 000000 | 0 | xxxxxxxxx | X |
| 000000 | 1 | xxxxxxxxx | Y |

* Store

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 000001 | 0 | xxxxxxxxx | X |
| 000001 | 1 | xxxxxxxxx | Y |

1. **Branch Instructions**

* BRZ = branch if zero

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100000 | xxxxxxxxxx | 0001 |

* BRN = branch if negative

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100001 | xxxxxxxxxx | 0010 |

* BRC = branch if carry

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100010 | xxxxxxxxxx | 0100 |

* BRO = branch if overflow

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100011 | xxxxxxxxxx | 1000 |

* BRA = branch always (unconditional branch)

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100100 | xxxxxxxxxx | xxxx |

* JMP = call procedure

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100101 | xxxxxxxxxx | xxxx |

* RET = return from procedure

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | ADDRESS (10 bit) | FLAGS (4 bit) |
| 100000 | xxxxxxxxxx | xxxx |

**C. Arithmetic and Logic Instructions**

* ADD

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001000 | 0 | xxxxxxxxx | X |
| 001000 | 1 | xxxxxxxxx | Y |

* SUB

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001001 | 0 | xxxxxxxxx | X |
| 001001 | 1 | xxxxxxxxx | Y |

* LSR

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001010 | 0 | xxxxxxxxx | X |
| 001010 | 1 | xxxxxxxxx | Y |

* LSL

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001011 | 0 | xxxxxxxxx | X |
| 001011 | 1 | xxxxxxxxx | Y |

* RSR

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001100 | 0 | xxxxxxxxx | X |
| 001100 | 1 | xxxxxxxxx | Y |

* RSL

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001101 | 0 | xxxxxxxxx | X |
| 001101 | 1 | xxxxxxxxx | Y |

* MOV

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001110 | 0 | xxxxxxxxx | X |
| 001110 | 1 | xxxxxxxxx | Y |

* MUL

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 001111 | 0 | xxxxxxxxx | X |
| 001111 | 1 | xxxxxxxxx | Y |

* DIV

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010000 | 0 | xxxxxxxxx | X |
| 010000 | 1 | xxxxxxxxx | Y |

* MOD

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010001 | 0 | xxxxxxxxx | X |
| 010001 | 1 | xxxxxxxxx | Y |

* AND

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010010 | 0 | xxxxxxxxx | X |
| 010010 | 1 | xxxxxxxxx | Y |

* OR

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010011 | 0 | xxxxxxxxx | X |
| 010011 | 1 | xxxxxxxxx | Y |

* XOR

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010100 | 0 | xxxxxxxxx | X |
| 010100 | 1 | xxxxxxxxx | Y |

* NOT

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) |
| 010101 | x | xxxxxxxxx |

* CMP

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010110 | 0 | xxxxxxxxx | X |
| 010110 | 1 | xxxxxxxxx | Y |

* TST

|  |  |  |  |
| --- | --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) | REGISTER USED |
| 010111 | 0 | xxxxxxxxx | X |
| 010111 | 1 | xxxxxxxxx | Y |

* INC

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) |
| 011000 | x | xxxxxxxxx |

* DEC

|  |  |  |
| --- | --- | --- |
| OPCODE (6 bit) | REGISTER ADDRESS (1 bit) | IMMEDIATE (9 bit) |
| 011001 | x | xxxxxxxxx |