Comparative Performance Analysis Of Single Stage Differential Amplifier At 32 Nanometer Regime

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***Abstract*—The MOSFET scaling approaches on the road to limitations alternatives are upcoming, to overcome these limitations. This paper deals with the design of single stage differential amplifier featuring 32nm gate length. Due to the shrunken size of devices, it inhabits less die-area. There are various Nano devices such as CNFET and FinFET. In this paper, we begin to talk over the role of MOSFET, FinFET and CNFET in the design of single stage differential amplifier and its contribution towards Gain, CMRR, Slew Rate and power consumption. The proposed conventional single stage differential amplifier using FinFET yields an open loop Gain 18.5 dB, Slew Rate 19.2E+06 V/µsec, CMRR 11.34 dB the circuit is operated at 1.8 V using Hspice simulation software. The simulations best part is that, at the existing stage of the technology scaling, the FinFET circuit seems to perform best than the MOSFET and CNFET at the cost of power consumption.**

Keywords—MOSFET; CNFET; FinFET; Differential amplifier; Slew Rate; CMRR

I. INTRODUCTION

Gordon Moore, foreseen that the transistors counts that might be found On-chip would twice over after each eighteen months. Modern electronics gets advantages of process scaling. The objective line of scaling more rapidly is towards shape a distinct transistor that is cheaper, less power is consumed and smaller. Wafer builders ensure trust on the sustained scale down of the transistor dimension to attain the exponential development in counts of transistor; nonetheless the scaling will be rapidly to the termination. Three hindrances position in the approach: the increasing price of manufacture, the bounds of lithography and the transistor dimension. Owing to these technical hitches, a novel technology must be accepted. Unique likely inheritor to lithography ICs is Nano scale technology [1].

The CMOS technology has constantly pushed for the increased density by scaling down the length. Even though many performance metrics like total power consumption, speed, cost, gain etc. have enhanced by means of scaling, the short-channel effects has become worsened, which leads to greater leakage currents. This necessitates new device structural design such as FinFET [2].

Numerous hi-tech device structure variants have been projected, similar to ultra-thin body single and multiple-gate FETs, SOI FETs, and CNFETs etc. to offer enhancements in static electricity and stability above CMOS. In the middle of that, CNFETs and FinFETs has been in recent times becoming a vital technology for low voltage analog and digital applications along with low power. Multi Gate based transistors are adept to swap CMOS in the future, owing to its superior static electricity property, greater mobility and stability. Differential amplifiers are important elements of the analog and mixed signal circuit [3].

Carbon nanotubes present a distinctive prospect as one of the rare systems where the investigational device size may reach the atomic-size models and may counterpart the estimates, thus in standard letting experimental authentication of computational methodologies and computational device design is realized [4].

Silicon-based technology has proficient remarkable evolution in the past few eras. A huge portion of the realization of the MOS transistor is outstanding to the fact that it can be scaled to smaller dimensions, which results in greater performance. However this development still continues bulk MOSFET will shortly reach its restraining size. Designed for this motive, the semiconductor manufacturers are viewing for different materials, devices to incorporate with existing silicon-based technology and in the elongated route, perhaps replace it. The carbon nanotube field effect transistor is one amongst capable substitutes owing to its electrical properties [5].

This possess essential to progress high-performance with reduced supply voltages analog integrated circuits. At large supply voltages, there is a compromise among speed, cost, power, slew rate, bandwidth and gain. In this paper, we designed single stage differential amplifier using FinFET technology, CNFET technology and MOSFET technology. Modeled features of FinFET created single stage differential amplifier compared with conventional CMOS single stage differential amplifier.

There are limitations of MOSFET scaling these are leakage current, total chip power, Process variation cost. Several ways out are projected to solve these topics which emphasis on given solutions are using FinFET, CNFET technology. From the comparison result, we stand up to the end that FinFET has benefits of high gain, high slew rate and better CMRR.

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II. CNFET AND FINFET STRUCTURE

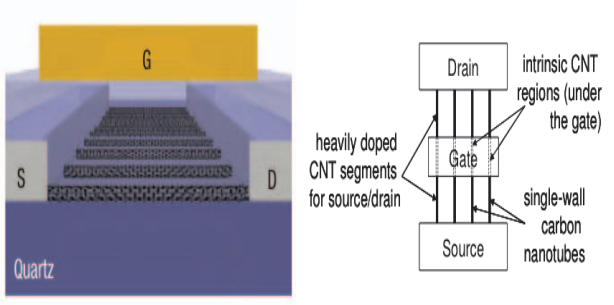

Fig. 1. Structure of CNFET [1]

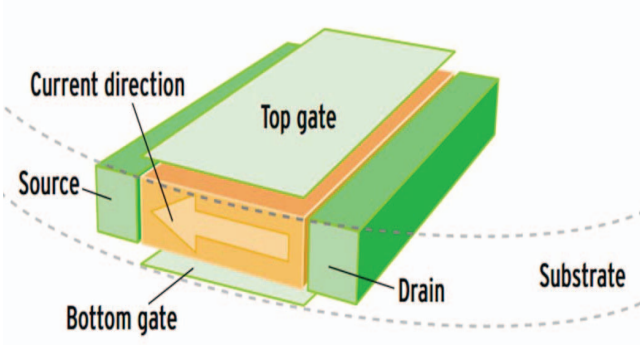

Fig. 2. Structure of FinFET [1]

CNTs are the utmost promising transistor module. The carbon nanotube field effect transistors (CNFET) seem actually alike to MOSFETs, by means of the silicon channel substituted using a CNT. CNFET and MOSFET V-I characteristics are related. The threshold voltage is least electrical energy necessary to make the transistor turn-on.

Reducing the dimension of devices to nanometer regime has impact on trustworthiness & enactment of the devices. Deprived of negotiating the reliability and performance FinFET is a better technology. The device thickness of the fin decides the effect on the length of channel [1].

Owing to the vertical gate structure width of a FinFET is quantized. The fin height (H_{fin}) regulates the minimum transistor width (W_{min}). With the two gates of a single - FinFET tied together, W_{min} is

$$W_{\min} = 2(H_{fin}) + t_{si} \quad (1)$$

Where, t_{si} is the thickness of the silicon body. A SWCNT can be envisioned as a piece of graphite which is roll along and linked together along wrapping vector $C_h = n_1 * a_1 + n_2 * a_2$, where $[a_1; a_2]$ is a lattice unit vectors, and the positive integers indices (n_1, n_2) that insist on the chirality of the tube [6]. The length C_l is therefore the bounds of the CNT, which is given in equation (2) and the CNT diameter is given in equation (3).

$$C_l = a\sqrt{n_1^2 + n_2^2 + (n_1 * n_2)} \quad (2)$$

$$D_{cnt} = (C_l / \pi) \quad (3)$$

III. DESIGN OF SINGLE STAGE DIFFERENTIAL AMPLIFIER CIRCUIT AT 32NM NODE

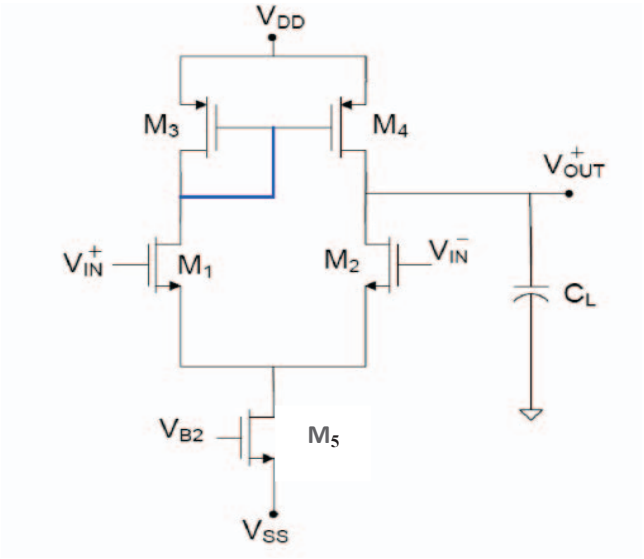

Fig. 3. Single stage differential amplifier

TABLE I. PARAMETERS OF OPTIMIZED CIRCUIT

Parameter	CMOS design		CNFET design		FinFET design	
	L nm	*W* µm	*S*	*N*	*L* nm	*W* µm
M_1	32	12	20	3	32	50
M_2	32	12	20	3	32	50
M_3	32	60	20	3	32	10
M_4	32	60	20	3	32	10
M_5	32	150	20	3	32	150
I Bias	3.05E-05		1.53E-04		1.92E-02	
C_L	1 FF					
V_{DD}	1.8 V					

In this segment, we employed three forms of the differential amplifiers with current mirror load based on the at 32nm technology CMOS, FinFET and CNFET. The electrical circuit simulant Synopsys HSPICE is used. Fig. 3 shows general single stage differential amplifier. In this M_1 and M_2 is differential pair transistor. M_3 and M_4 are active loads. The transistor M_2 and M_4 operates in saturation region which is the region of operation.

CNFET created differential amplifier circuit is intended in terms of best device parameters are diameter of CNT, uniform inter-nanotube spacing pitch (S), Number of nanotubes (N) and input supply voltage (V) [2].

The I Bias is the biasing current. The differential amplifier parameter values of design are selected from the literature for the both CMOS and CNFET [4], [7]–[9] kinds which are

shown in TABLE I. Differential amplifier performance parameter as also stated.

- CMRR: The ability to reject the signal on both terminals such as noise is known as common mode rejection ratio. Where A_{dm} is differential gain and A_{cm} is common mode gain.

$$CMRR\left(dB\right) = 20 * \log(\frac{A_{dm}}{A_{cm}}) \quad (4)$$

- Slew Rate: Slew Rate is defined as the amount of change in output voltage produced by a step input voltage and specified in V/µsec. Where V_m is amplitude, V_o is output voltage, I_{max} is maximum current and SR is Slew Rate.

$$V_S = V_m Sin\omega t \quad (5)$$

$$V_o = V_m Sin\omega t \quad (6)$$

$$\frac{d}{dt}V_o = V_m \omega Cos\omega t \quad (7)$$

$$SR = V_o \frac{d}{dt}\mathrm{I}_{m\,ax} \quad (8)$$

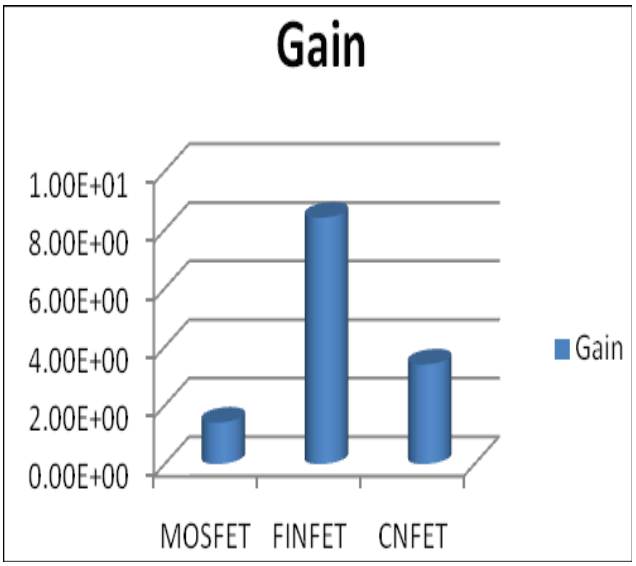

Fig. 4. Gain of Differential Amplifier

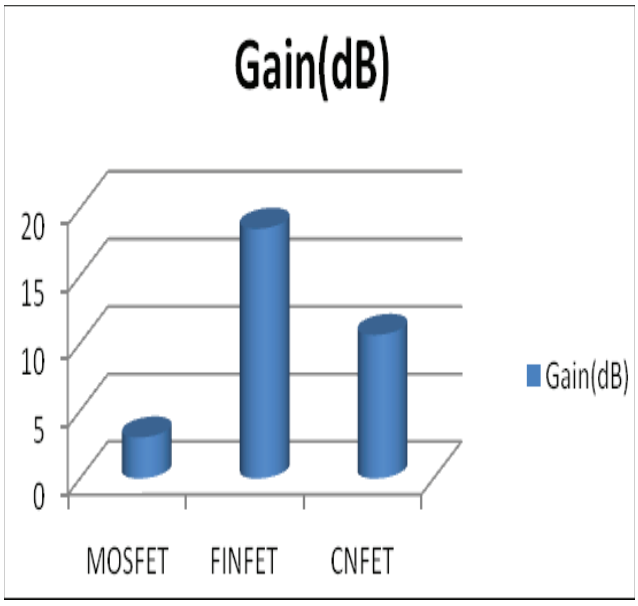

Fig. 5. Gain of Differential Amplifier in dB

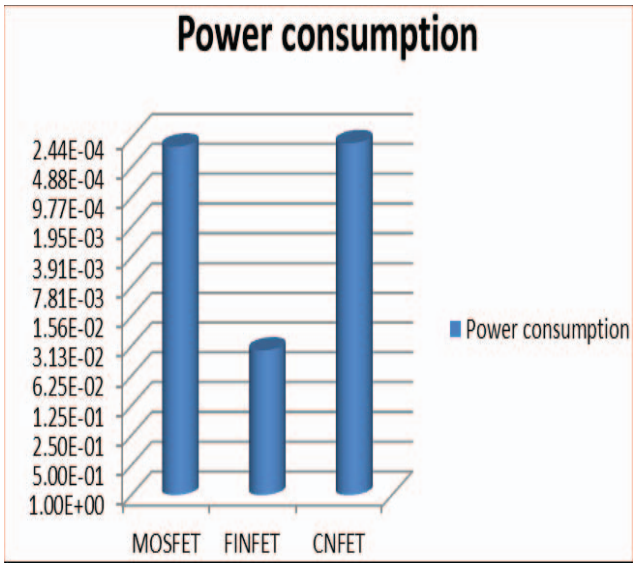

Fig. 6. Power Consumption of Differential Amplifier

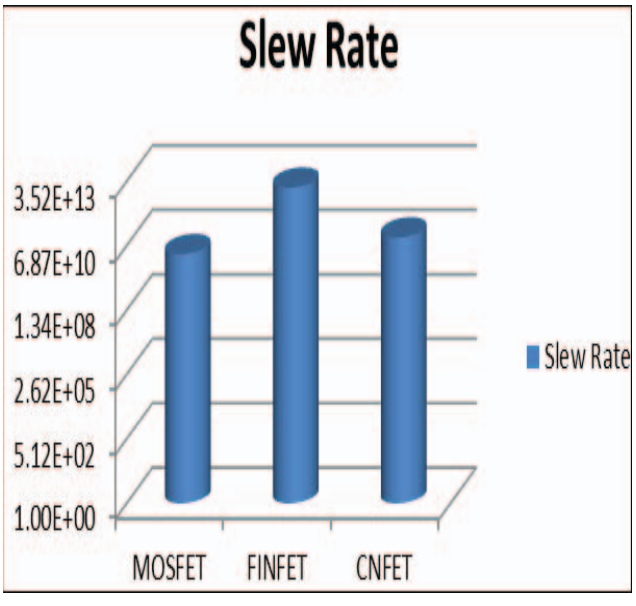

Fig. 7. Slew Rate of Differential Amplifier

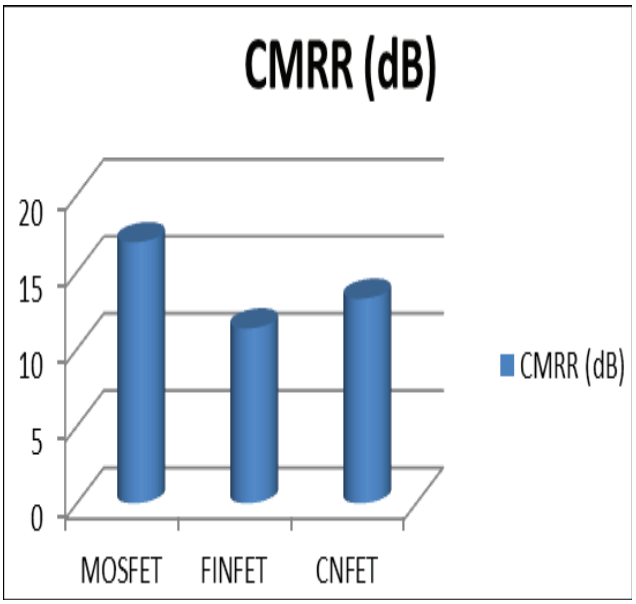

Fig. 8. CMRR of Differential Amplifier

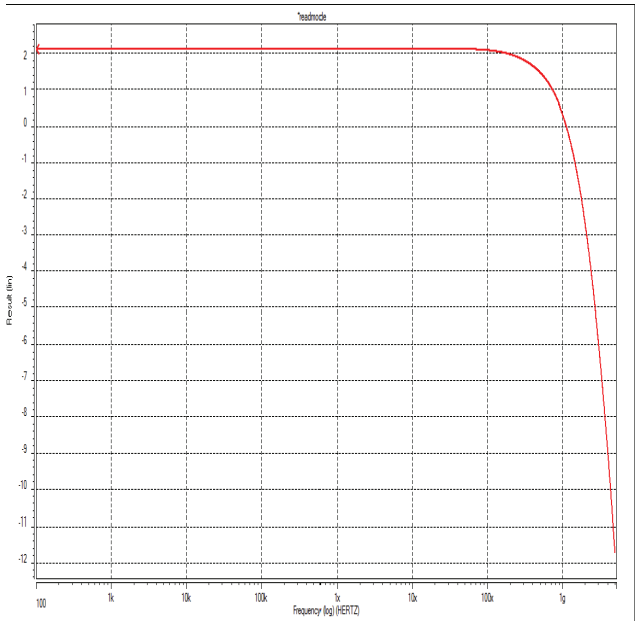

Fig. 9. MOSFET Frequency Response

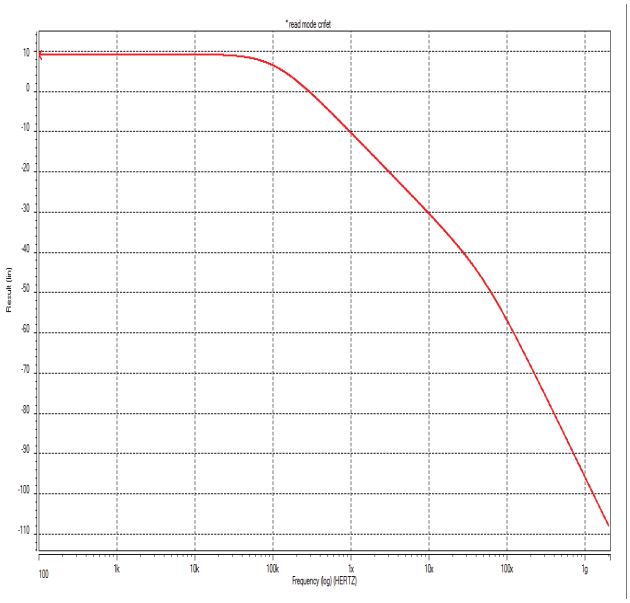

Fig. 10. CNFET Frequency Response

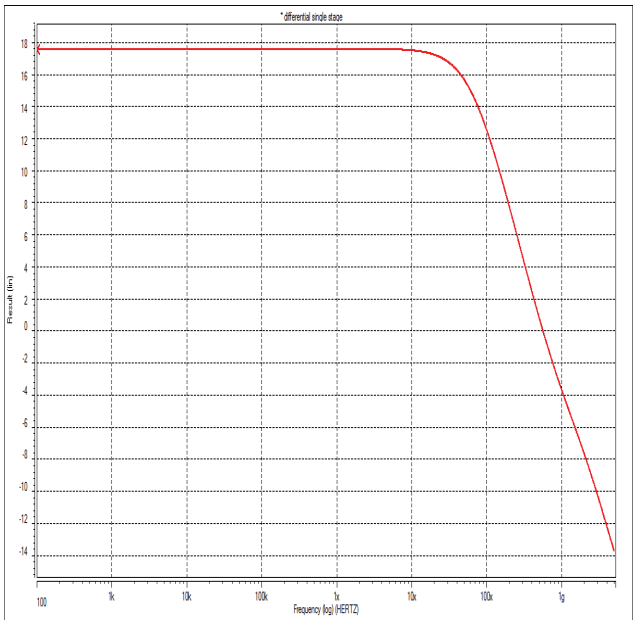

Fig. 11. FinFET Frequency Response

- Frequency response: The plot screening the variants in magnitude and phase angle of the gain owing to the alteration in frequency is known frequency response of amplifier.
- Unity Gain Bandwidth: As soon as voltage gain is unity that bandwidth of differential amplifier is known as unity gain bandwidth. Besides this it is also known as Gain Bandwidth Product.
- Power consumption: It is an addition of both dynamic and static power. In supreme circumstances, it depends on dynamic power. In equation (9), α is activity factor, I_{SC} is the short circuit current, V_{DD} is the supply voltage; t_{SC} is switching time, f is the switching frequency and C_{out} is output capacitance.

$$P_{total} = \alpha I_{sc} V_{DD} f .t_{sc} + \alpha V_{DD}^2 f C_{out} \quad (9)$$

IV. Simulation Results Analysis And Comparison

The FinFET based differential amplifier's enactments features are inspected widely in rapports of the circuit specifications, such as slew rate, common-mode rejection ratio and gain and frequency response and power consumption. The enactment features of the differential amplifier are studied using state of the art 32nm-CMOS and 32nm-CNFET technology.

TABLE II. COMPARISON OF DIFFERENTIAL AMPLIFIER

Parameters	This Work			[7]	[10]	[11]
	32nm CNFET	*32nm MOSFET*	*32nm FinFET*			
V_{DD} (V)	1.8	1.8	1.8	1.0	1.0	1.0
Gain	3.41	1.42	8.42	25.11	…..	…..
Gain (dB)	10.64	3.04	18.5	28	59	55.9
Frequency Response(Hz)	98.7K	479M	223M	10G	…..	….
Slew Rate (V/µsec)	153000	30500	192E+5	.....	…..	500
CMRR(dB)	13.27	16.93	11.34	70-90	…..	63
Unity Gain Bandwidth (Hz)	287K	1100 M	562 M	…..	3.5G	656
Power Consumption (µWatt)	275	299	34400	77	10	….

The simulation outcome of the projected MOSFET, CNFET and FinFET based differential amplifiers frequency response are shown in figure 9, 10 and 11 respectively. Fig. 4, 5, 6, 7 and 8 shows the performance results of gain, gain in dB, power consumption, slew rate and CMRR. Consequences of the simulation prove that FinFET based differential amplifier have enhancement in relations of gain, and Slew rate but more power consumption. Differential amplifier with 32nm CNFET has significantly lesser power consumption.

V. CONCLUSION

This paper sees the place of interest that is boon achieved from emergent FinFET technology above the CMOS technology and CNFET technology. Differential amplifier with FinFET offers good performance Gain, CMRR and Slew at the price of power consumption. V_{DD} 1.8V is used for the circuit simulation.

The differential amplifier design using MOSFET has unity gain bandwidth 1100MHz which is good compared to the designs using CNFET and FinFET. The CNFET based differential amplifier gives better results for gain than MOSFET.

The foremost role of this paper is the straight forward comparison amongst emergent technologies. Furthermore, as a future scope of this work, efforts can be noting the performance by supply voltage scaling.

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