Performance Analysis of Classical Two Stage Opamp Using CMOS and CNFET at 32nm Technology

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***Abstract*— This paper presents performance analysis for the two-stage CMOS operational transconductance amplifier using conventional CMOS technology and emerging carbon nanotube technology. Both the theoretical calculations and computer aided simulation analysis have been given in detail. Designs have been carried out on backend tool of Mentor graphics using PTM 32nm CMOS process. Schematic simulations have been carried out using 'Pyxis Schematic' and simulations have been done using simulator 'ELDO', version 11.2. For CNFET implementation 32nm CNFET model from Stanford University is used and simulations are carried out using Hspice. The a. c. analysis demonstrates that gain of the CMOS amplifier is very low i.e. 15.6 dB, Phase Margin is 80.2°, & Unity Gain Bandwidth is 7 MHz. The output swings up to 1.15V and the op-amp dissipates power of 336.5µW under supply voltage of 1.2V. The comparative performance analysis with CNFET shows that there is improvement of 264 percent in gain while maintaining the complete stable performance in both the case. Further results show the tremendous increase in unity gain bandwidth while significantly saving in power.**

Keywords*— *Moore law, Non-ideal effects, Carbon nanotubes, MOSFET, CNFET, Opamp, 32nm technology etc.

I. INTRODUCTION

Over the last few years, the electronics industries have exploded. Low power and efficient portable equipment demands are rising in day-to-day life. The common trend for analyzing low power circuits is the lowering of supply voltage. But the threshold voltage of metal-oxide semiconductor (MOS) transistor acts as a main obstacle in lowering of voltage supply after certain limit. The supply must be at least equal to or greater than the threshold of MOS transistors used in circuit realization. The rapid scaling of CMOS processes in nanometer demand low supply which helped digital circuit realization at very low power consumption but it is not true for analog circuit realization. The associated drawback is short channel effect which results in low gain stages, decreased impedance etc. [1].

The minimum channel length for conventional planar CMOS is 10nm where the non-ideal effects severely affects the performance of transistor and further reduction leads to tunneling effect. As the tunneling effect comes into the picture, the gate leakage current and sub threshold leakage current increases, this makes the stand-by power to increase which is required by the device [2]. With these effects arising due to scaling and to overcome these limitations of conventional CMOS in nanometer regime, many solutions have been proposed by researchers. One of the beyond CMOS alternatives is carbon nanotube field effect transistor (CNTFET) which have circular structure of graphene rolled up [3, 4]. In CNTFET, the conducting channel is now replaced with carbon nanotubes (CNT) in deep sub-micron levels. Its structure, behaviour, electrical and mechanical properties makes it distinctive from other FETs making it as future of nanoelectronics. Some of to mention about the properties are high carrier mobility, ballistic conduction, suitable contact resistance, fast switching speed and less heat dissipation, very high k gate dielectric, higher drive current, and higher average carrier velocity. When we have CMOS scaling to an end and replacing it with CNTFET we have to see that even CNTFET have various challenges and have to be considered before using it. Some of the challenges include quality of CNTs, effect of chirality on tube diameter, difficulty in mass production and reliability issues due to varying environmental conditions [4].

Operational amplifiers are key elements in analog processing systems. Operational amplifiers are an integral part of many analog and mixed-signal systems. As the demand for mixed mode integrated circuits increases for low voltage low power operation, the design of analog circuits such as operational amplifiers (op-amps) in CMOS technology becomes more critical [5].

This study is a step forward to address various trade-offs related to performance comparison of conventional two stage CMOS op-amp and CNTFET op-amp at 32nm technology node. Since two stage conventional op-amp is well known and its design is also available in various books, its discussion is omitted here. Section II describes theory of carbon nanotubes and its properties in detail. Carbon Nanotube Field Effect Transistor, its design considerations and parameters are given in Section III. The specifications and the formula and calculations for design of two stage CMOS op-amp as well as CNTFET op-amp are explained in section IV. Section V presents the simulation results for various performance parameters & its comparative analysis for conventional gate driven CMOS and CNTFET op-amp operating at 1V supply voltage and 32nm process & some concluding remarks appear in Section VI.

II. CARBON NANOTUBES

The word carbon nanotube (CNT) has come from Latin word "carbo" which is derived from French word "charbon", meaning charcoal. Carbon nanotubes were discovered by S. Ijiima in NEC Laboratory, Tsukuba 1991. Carbon nanotubes have a cylindrical structure which have strength, electrical properties which are extraordinary and also efficient conductors of heat. Thick sheets of carbon collectively called as graphene, forms long, hollow structures to form carbon

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nanotubes. Carbon nanotubes mainly depend on chirality and chiral vector which classifies CNTs into various types depending upon value of chiral vector. CNTFET are same as MOSFET of today where they have three terminals such as source, gate, and drain. The main difference between CNTFETs and MOSFETs is that CNTFETS use their carbon nanotubes as the channel, where MOSFETs channel is made from heavily doped silicon [4].

Classification of Carbon Nanotubes:

This chiral vector defines the length and diameter which decides the feature size of nanotubes. The diameter size ranges from less than 100nm with minimum 1 or 2 nm thickness. They can be classified based on conductivity, chirality and layers with high aspect ratio hollow cylinders in a honeycomb lattice arrangement [4].

Based on number of layers, carbon nanotubes are divided into three types:

A. Single Walled Nano Tubes (SWNT)
B. Multi Walled Nano Tubes (MWNT)
C. Mixed Walled Nano Tubes

A. Single Walled Nano Tube (SWNT)

Single walled carbon nanotube (SWNT) is formed by wrapping a graphene sheet into a single layer cylinder which has diameter around 1nm with length longer as defined. The representation of graphene sheet rolled is denoted by pair of indices (n, m) called the chiral vector. It denotes number of unit vector in two directions in honeycomb lattice structure of graphene. Further classification of SWNT is based on chiral vector which exhibit electric properties that are not given by multi walled carbon nanotube (MWNT).

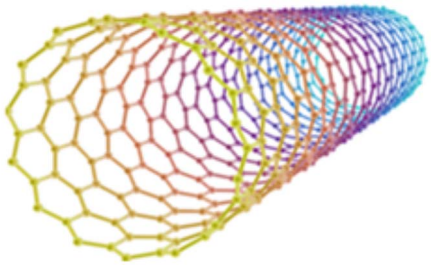


Fig 1. Single walled carbon nanotube (SWNT) [4]

B. Multi Walled Nano Tube (MWNT)

Multi walled carbon nanotube (MWNT) are made from multiple layers of graphene sheets rolled to form tube. They can be identified by two types of models in which they define its structure [2]. First is the Russian model, where the graphene sheets are fashioned as concentric cylinders means a carbon nanotube have another nanotube in which the diameter differs from inner nanotube than the outer nanotube. Second is the Parchment model, where the graphene sheet is rolled up multiple times around itself such as rolled up newspaper. As they are rolled multiple times the outer layers protect the inner layers from any interactions with outside materials. One advantage of MWNT over SWNT is that they have higher tensile strength.

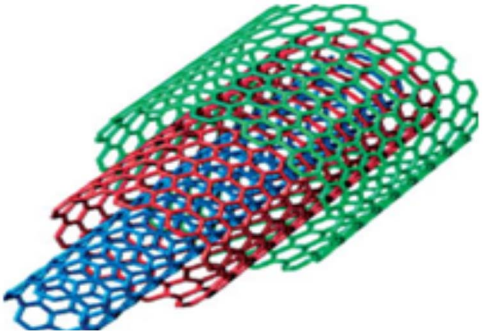


Fig 2. Multi walled carbon nanotube (MWNT) [4]

C. Mixed Walled Nano Tubes

Single walled carbon nanotube and Multi walled carbon nanotube together combinedly forms Mixed walled carbon nanotube which have different dimensions. It is the combination of both, where empty spaces generated in graphene sheet rolled up in concentric circles are filled up by single walled carbon nanotubes (SWNT) [2].

Based on chirality carbon nanotubes are classified as:

A. ZigZig
B. Armchair
C. Chiral.

One of the property of nanotube is the chirality which decides whether the nanotube is semiconducting or metallic. The electrons in the graphene sheet are bonded together to have a circular shape and confined to circumference of nanotube when it is rolled. All the above nanotubes mentioned based on chirality have symmetrical classification of nanotube. Zigzag and armchair have the same achiral structure that is a mirror image of the original one but chiral angle separates them out, whereas chiral have spiral symmetry which does not give it an identically structured mirror image. Chirality vector, or chiral vector, is defined as C = na1 + ma2 where a1 and a2 are unit cell vectors and n, m are integers. If the chiral vector R which is the addition of two vectors a1 and a2 where a2 has different magnitude over a1 but its direction is reflection of a1 over armchair line is called one of the nanotubes defined given by condition as:

a) If R lies along the Armchair line $\phi=0$ then it is called armchair else
b) zigzag if $\phi=30^{o}$
c) and if $\phi=0< \phi<30$ then called as chiral.

The values of n and m determine the chirality, or twist of the nanotube. If the value obtained by having the difference between n-m is divisible by 3 we can say that SWNT is metallic in nature otherwise it is semiconducting.

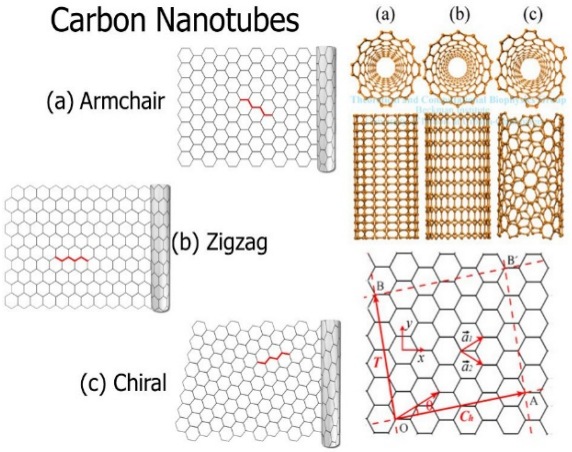


Fig 3. The principle of CNT construction from graphene sheet along the chiral vector [4]

III. Carbon Nanotube Field Effect Transistor (CNFET)

Same as MOSFETs the scientists have developed Carbon nanotube field-effect transistors which require same three terminals namely, drain, source and gate. Gate playing the important part controls the flow of current across source and rain. The switching activity of gate i.e. on and off enables the current to flow through channel. Carbon nanotubes are used as the channel in CNTFETs whereas silicon is used as channel in MOSFETs [4].

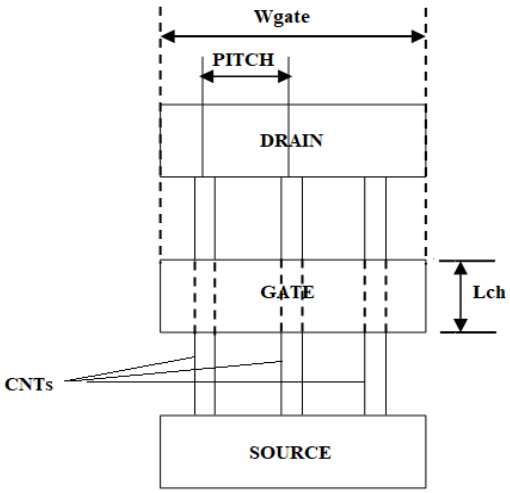


Fig 5. Structure of Carbon nanotube field effect transistor

Above figure shows the structure of CNTFET where, carbon nanotubes are inserted on silicon oxide film on silicon substrate and source and drain connections are formed to carry out the current flow. Some of the design parameters for CNTFET devices are represented in TABLE I.

TABLE I. CNTFET design parameters

Chiral vector (C)	$n\widehat{a1} + m\widehat{a2}$
Chiral angle (θ)	$\sin^{-1}(\frac{3m}{2\sqrt{n^2+m^2+nm}})$
Length of chiral vector (L)	$a\sqrt{n^2+m^2+nm}$
Diameter (D)	$\frac{\sqrt{3}a}{\pi}\sqrt{n^2+m^2+nm}$
Width of CNFET (W)	(N-1) *S + D

IV. Design Considerations of Opamp

For the design of analog circuits, it is mandatory to have specifications for its customization. Specifications are divided into two categories. First is circuit specification which is given by the designer or manufacturer for its design, and second is EDA tool specification which is provided by the EDA tool vendor.

A. *Circuit Specifications:*

1) Supply Voltage, V_{DD} = 1 V
2) Open loop gain, AV =100 = 40 dB
3) Phase Margin = 45°
4) Load Capacitance, C_L= 2 pf
5) Maximum Input Common Mode Range, ICMR (+) = 1V
6) Minimum Input Common Mode Range, ICMR (-) = 0.8V
7) Slew rate = 20V/µsec
8) Gain Bandwidth Product, GBW = 30 MHz

B. *EDA Tool Specifications for CMOS design:*

1) $\mu_n C_{ox}$ = 814.1µA/V^2
2) Vth_n = 0.51 V
3) $\mu_p C_{ox}$ = 70.05 µA/ V^2
4) Vth_p = - 0.45 V

C. *Model file specifications for CNTFET design:*

1) The carbon PI-PI bond energy Vpi = 3.033
2) The carbon PI-PI bond distance d = 0.144e-9
3) The carbon atom distance a = 0.2495e-9
4) The diameter, d = 1.49nm
5) The inter-nanotube spacing, pitch s = 8nm
6) The number of nanotubes in each transistor = 3

Designing has been conceived on the basis of fundamental equations which are used for the calculations of aspect ratios and device dimensions.

V. SIMULATION RESULTS

A. *Differential amplifier:*

A circuit that increases the amplitude of the given input signal is an amplifier. A small AC signal fed to the amplifier is obtained as large AC signal of the same of frequency at output [5]. In most operational amplifier topologies, the input stage is realized by a differentia pair. It is, without doubt, the most commonly used building block in analog processing system. Therefore, we examine its small signal behaviour, which serves as the background material for the next section. It consists of a current source with value I bias and two equal or matched transistors Ml and M2. For differential output, transistors M3 and M4 are implemented as current source/sink loads or active loads; while for single ended, they are connected as a current mirror. Here, it is assumed that M3 and M4 are current source loads for the analysis, but similar analysis can also be applied to the current mirror load.

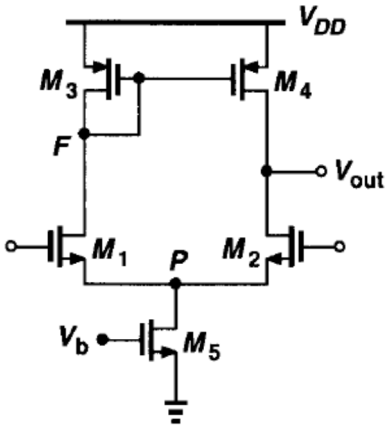


Fig 6. Differential amplifier [5]

B. *Two stage opamp:*

An op-amp is a multistage amplifier which provides high gain with differential amplifier as input stage and concluded with level translator at output stage. Input signals can be given through provided inverting and non-inverting terminals for observing the output at its output node. Amplifiers are important blocks of analog and digital systems. Some of the advantages can be given as:

1) To amplify the given input signal.
2) To reduce the noise impact through the building stages of op-amp.

Key issue of two-stages leads to two poles that are relatively close to each other. This leads to very poor phase margin unless very large CL is used. Inclusion of a compensation capacitor across the second stage leads to pole splitting such that stable performance can be achieved with reasonable area.

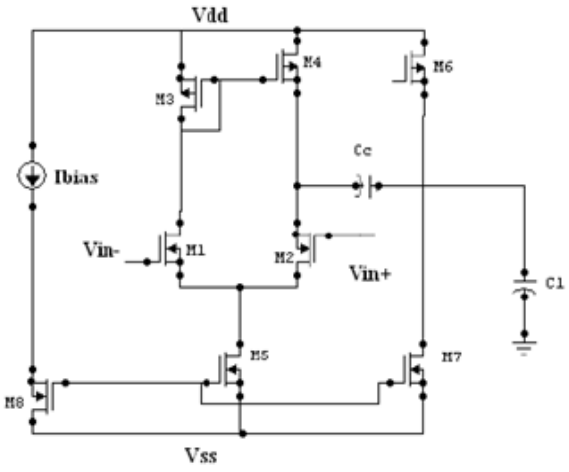


Fig 7. Two Stage Op-Amp [5]

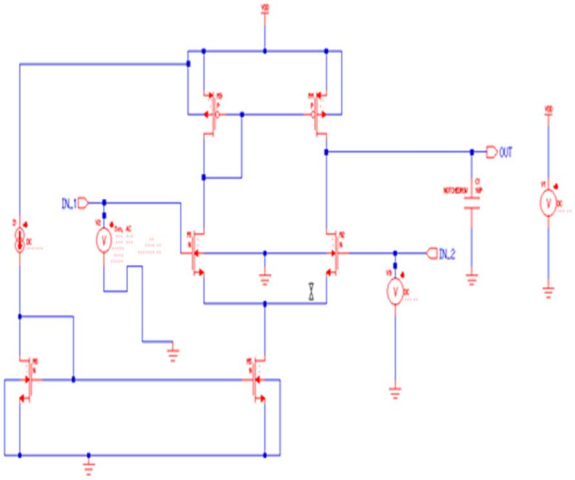


Fig 8. Schematic of Differential amplifier using CMOS

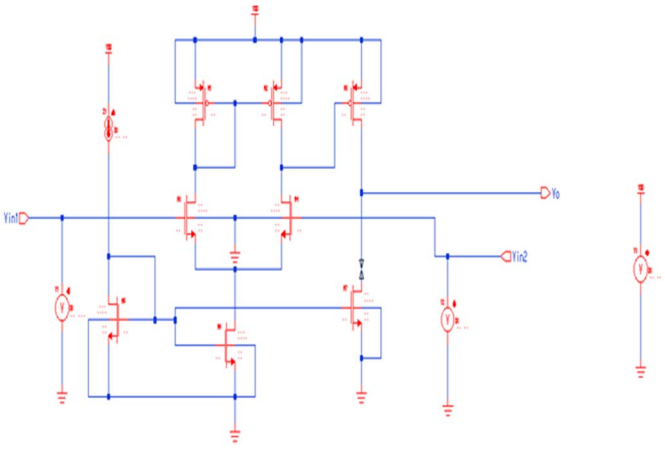


Fig 9. Schematic of Two stage opamp using CMOS

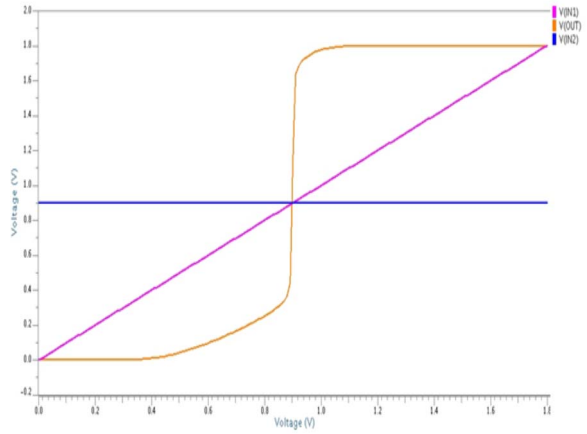
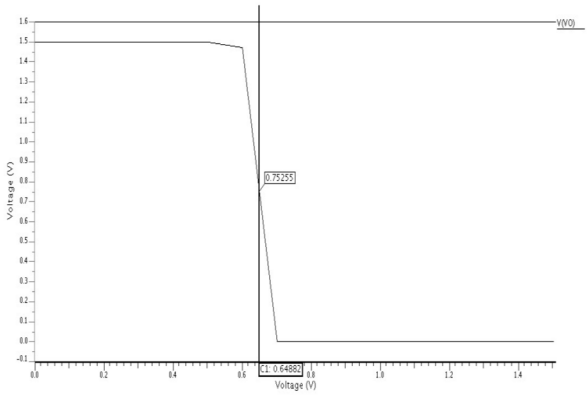


Fig 10. DC response of Differential amplifier using CMOS



Fib 11. DC response of Two stage opamp using CMOS

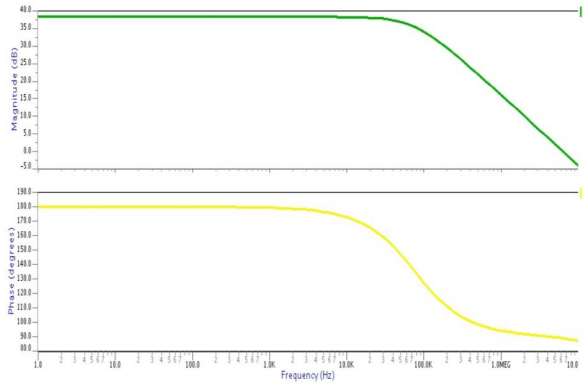


Fig 12. AC response of Differential amplifier using CMOS

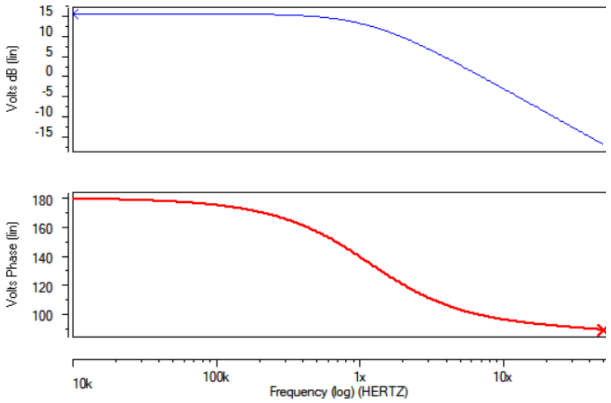


Fig 13. AC response of Two stage opamp using CMOS

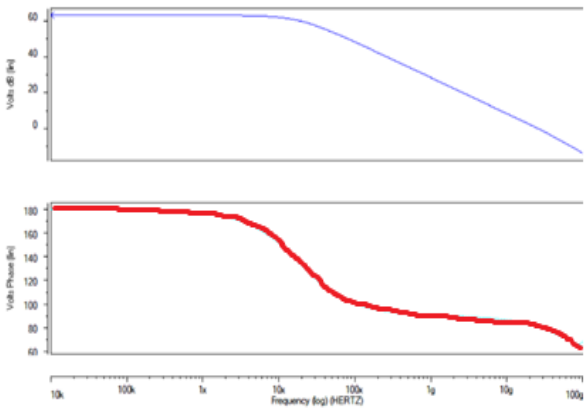


Fig 14. AC response of Differential amplifier using CNFET

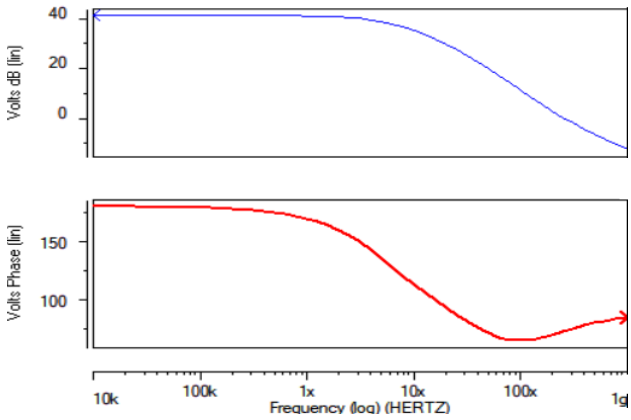


Fig 15. AC response of Two stage opamp using CNFET

VI. RESULTS

From the simulation graphs of figures (9) & (10) we can say that under same technology parameters considerations, CNFET amplifiers ac frequency response improves in comparison to CMOS amplifiers under similar area constraints with the exception that phase margin is slightly tangled for both the conditions. As we try to improve the gain we have battle with phase margin as we need phase margin greater than 45º for stable operation of amplifier.

TABLE II. Comparison of performance parameters at 32nm technology level

Design	Gain (dB)	UGB (MHz)	Phase Margin (º)
Differential amplifier using CMOS	38.43	7	88.77
Differential amplifier using CNFET	63.2	10	82.38
Two stage opamp using CMOS	12.5	58.1	52
Two stage opamp using CNFET	32.3	89.1	49.3

The following graphs shows us the output response of differential amplifier and two stage opamp using CMOS and CNFET design methodology having specification as V_{DD}=1V and room temperature=25ºC as room temperature at 32nm technology level.

VII. Conclusion

A classical two stage operational amplifier has been realized in 32 nm technology & it's performance has been analyzed in this paper with respect to CNFET implementation at same technology node. Results show that designed op-amp shows improved performance with CNFET than that of CMOS. This is due to the fact that at deep nanometer regime, CMOS performance degrades due to severe non-ideal effects especially tunneling and subthreshold conduction. However, due to quasi 1D transport of carriers in CNFET, performance is improved with CNFET implementation. So CNFET has a potential to emerge as one of the replacement of CMOS in future.

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