LOW POWER LOW VOLTAGE CNTFET-BASED CURRENT DIFFERENCING BUFFERED AMPLIFIER

Dinesh Prasad[1],
[1]Department of ECE, Jamia Millia Islamia, New Delhi, India
Laxya[2],
[2]Department of EEE, GCET, Greater Noida, India

Mainuddin[1]
[1]Department of ECE, Jamia Millia Islamia, New Delhi, India,
S. S. Islam[3]
[4] Centre for Nanoscience and Nanotechnology, Jamia Millia Islamia,

Abstract: Problems met by CMOS Technology mainly includes dopant fluctuation, tunnelling effect and line edge roughness below 45nm technology. Carbo nanotube based structures is better option for extending the Moore's law due to its scalability, higher mobility and channel electrostatics. In this manuscript we demonstrate an optimum design for low power low voltage CNTFET based CDBA at 32nm technology node. The proposed circuit consist of CDBA with CNTFET and flipped voltage follower current sources (FVSCF) designed technique to obtain the high performance. The minimum supply voltages of ±0.6V with 32nm technology mode is used. The performance of the CNTFET-CDBA is verified with HSPICE. In this paper CNFET-based CDBA provides results at higher frequency with less power consumption as compared with CMOS. All the simulation results are tested on HSPICE.

Keywords: Current differencing buffered amplifiers (CDBA), Low power, Low voltage operation, carbon nanotube field effect transistor (CNFET) Carbon nanotube (CNT).

I. INTRODUCTION

In the field of mobile communication system with the beginning of portable electronic the design of low voltage circuit has achieved alot of importance. In last few year there has been lot of focus on reduction of supply voltage in order to reduce the power consumed by the circuit. For the purpose of low voltage operation in analog signal processing, CM and VM circuits have found great importance. In addition to low voltage operations these circuits contribute low power consumption, large dynamic range high speed and low impedance level. We have many active elements which contribute as current mode circuits such as operational trans-resistance amplifier (OTRA), current operational amplifier (COA), current conveyor, current differencing buffered amplifier (CDBA) and have suitably met the requirements. Brief introduction of this work can be found in [2].

The current differencing buffered amplifier (CDBA) was initially given by Acar and Ozoguz [3]. Better flexibility can be provided because it is operational in both voltage as well as current mode, work at high frequency operation, free from parasitic capacitances

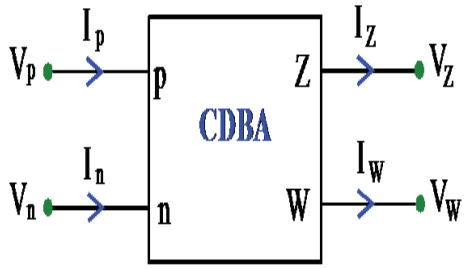

Figure 1. Symbolic Notation of CDBA

There are various methods to design CDBA. one of the possible method is based on (CFOA) current feedback operational amplifier[3].CDBA is also implemented by bipolar technology[4]. A large no of CDBA implemented based on CMOS is already reported in literature survey[5-6] where the terminal resistance of CDBA based on CMOS is very high i.e several hundred ohms and their transfer ratio of voltage and current are small. CDBA currently in use are working at higher supply voltage, consuming higher power and our

This research is supported by the "Young Faculty Research Fellowship and Research/Contingency Grant" to Jamia Millia Islamia, under "Visvesvaraya PhD Scheme for Electronics and IT" in 2016-17.

978-1-5090-2797-2/17/$31.00 ©2017 IEEE

goal is to reduce the power supply and consumption so we proposed CNTFET based CDBA.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

Ijima of NEC Japan had discovered Carbon nanotube in 1993 which is the allotrope of carbon . Carbon nanotube is taken as a promising material which can be replace the use of silicon due to its property. Carbon nanotube have unique feature like higher electrical conductivity than silver, high tensile strength more then steel and large thermal conductivity than diamond. The most important property of of carbon nanotube is 1D ballistic transport capability. Due to these exceptional properties CNT have wide number of applications in the field of nano-electronics and nano-science. Carbon nanotube available in two forms : Single wall carbon nanotube (SWCNT) and (ii) Multiwall carbon nanotube (MWCNT) as demonstrate in Figure 2(a). SWCNT are normally placed at the ends [9-11]. The diameter of SWCNT varies from 1 nm to few micro meter based on the value of (m,n) or type of SWCNT. MWCNT are better than SWCNT but they are costly and they are like co-axial cable. Whereas the diameter of MWCNT varies from 5nm to 50nm with the inter layer spacing of is 3.4Å.. The pair of indices (m,n) is represented by wrapping of sheet which are called Charality vector as demonstrate in figure 2(b). Depending upon the pair of indices the SWCNT is categories in three types:[12-13]

(i) Armchair if ($n = m = 0$ and $\theta = 30^o$)
(ii) Zig-Zag if ($n = m = 0$ and $\theta = 0^o$)
(iii) Chiral if ($m = n=0$ and θ lies between 0^o to $\theta=30^o$)

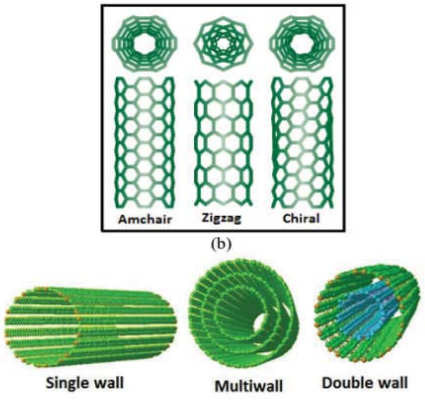

Figure 2. Structural of Carbon NanoTubes

Figure 3 demonstrates the layout diagram of CNTFET, that is, carbon nanotube field effect transistor (CNTFET). In In a CNTFET, the parallel combination of SWCNTs are used to mage channels. Whereas drain and source terminal of CNTFET are highly doped and and channel is undoped. The most important advantage of carbon nanotube is 1D ballistic transport capability and large current driving capacity with low power consumption and high mobility. For improvement in the performance of the device below the 45nm technology we use some alternative technique apart from use of silicon CMOS technology because it reaches its scaling limit .so the Nanotechnology based devices or fabrication exhibits large density and performance of electronic circuits , electronic characteristic of CNTFET has made it appear brighter [14]. The usual and the basic problems such as leakage currents, lithographic limits, high field effects, extreme short channel effects, and quantum confinement effect associated with silicon CMOS are solved to a great extent in CNFET [15]. To enhancing the efficiency of the circuit the width can be channel reduced to 4nm and channel length can be reduce up to 10nm. A large number of issues in fabrication of CNTFET can be resolved now and it look good [16-19].

.

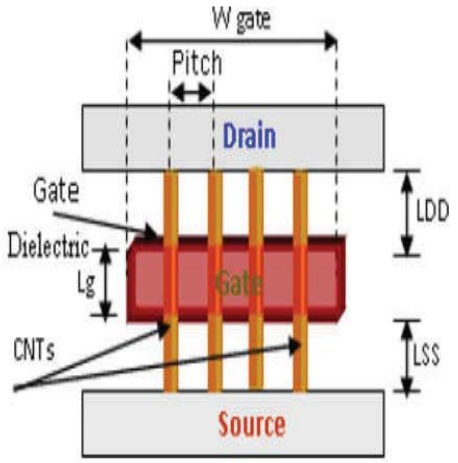

Figure 3. Layout diagram CNTFET

In the conventional MOSFET the channel is replaced by CNTFET as demonstrate in Figure 3(layout of CNTFET). Ijima had discovered that CNT's are long and allotropes of carbon.

When they are made up of single shell they are called single wall Carbon nanotube(SWCNT)[20]. They are formed by folding of graphite layer and having quasi 1-D molecular structure. Due to this 1-D structure CNTFET give better control over 2-D and 3-d devices[21].

Table1: Technology parameter of CNTFET[22]

Parameters of CNTFET	Value
Oxide thickness(TOX)	4mm
Physical channel Length(Lch)	32nm
Power supply	±0.9v
Gate oxide	HFO_2
Dielectric constant	16
Mean free path: Intrinsic CNT	200NM
Mean free path: doped CNT	12.5NM
Work function(CNT)	4.5eV

III. CNTFET Based CDBA

Generally, When we are designing the circuit in CMOS technology, ratio of PMOS/NMOS is taken as 2-4 toi match the properties of p-type and n-type MOSFET. However there is no such restriction in Carbon nanotube Field Effect technology (CNTFET). In CNTFET we may take the ration of p-type and n-type as "1" so the both PMOS and NMOS have same capabilities of driving current [22-23]

Moreover, differing in CMOS, in which the aspect ratio of the transistor are adjusted to change the PMOS/NMOS ratio, a CNTFET-based CDBA is proposed in terms of the following optimal structural parameters.

1) Number of CNTs (N): Since single nanotube based transistor is unable to provide sufficiently good performance over CMOS so in order to give proper current supply for the purpose of driving the fixed capacitive load, it is very much necessary to determine the number of CNTs used in the array.
2) Inter-CNT Pitch (S): When the two CNTs are lying beside each other in the channel then the distance between their center is said to be inter CNT pitch. It is denoted by "S" and one of the factor that can not be ignored when deciding the performance of CNTFET.
3) Diameter of CNT (Dcnt): The threshold voltage of the device is directly affected by the D_{CNT}, hence requiring careful selection mechanism[24].

$$\text{Dcnt} = \frac{A\sqrt{(n^2+m^2+mn)}}{\pi} \quad (1)$$

$$\text{Vth} = \frac{aV_\pi}{\sqrt{3q\text{Dcnt}}} \quad (2)$$

$$W = (N \quad 1) \quad S + \text{Dcnt} \quad (3)$$

Figure 4 demonstrate the proposed diagram of the low power low voltage CNTFET-CDBA circuit, which is based on the use of the current differencing circuit (M_1–M_8) and the voltage buffer (M_9–M_{14}) and implemented the CNT in it. The proposed circuit is supplied by the voltages of ±0.6 V which is simulated at 32nm technology node and the configuration and parameters of the CNT is given in table 1 and the bias current Ib1 and Ib2 are selected at 56uA and 84uA respectively. The proposed circuit contains NCNT and PCNT with oxide thickness 4nm, dielectric constant 16, power supply ±0.6 V, Inter-CNT pitch 40nm, Diameter of CNT 1.5nm, chirality vector (19,0) and threshold voltage 0.49.

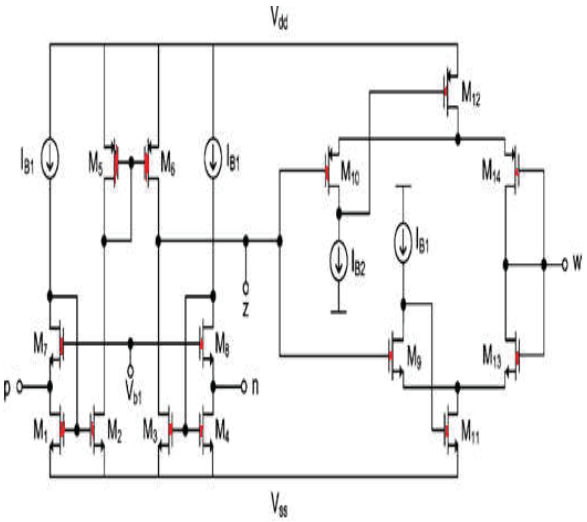

Figure 4. Schematic diagram of Proposed CNTFET Based CDBA

In this paper the technology used (FVFCS) flipped voltage follower current sources will give current subtractor circuit which result in low input resistance at the input terminal [7] as demonstrate in figure 5.

$$Rx = \frac{2}{gm_1 gm_2 ro_2} \quad (4)$$

The proposed circuit shows that input impedance of terminal N and P are varying from few ohms to

37.6 Ω over a wide frequency range as shown in figure 6.

The output current is defined by terminal z which has identically infinite output impedance.

The FVFCS is shown in Figure 5

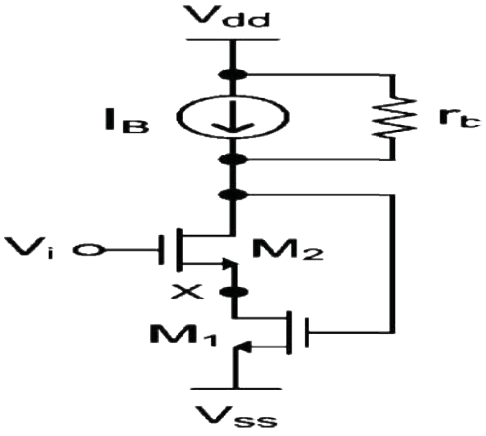

Figure 5. Fliped Voltage Follower Current Source

Terminal Z resistance is calculated as :

$$Rz = ro_3 // ro_6 \quad (5)$$

Table2: CNFET Based Transistor Dimension

Transistor	Diameter	Inter - Pitch
M1,M2,M3,M4,M7,M8 ,M9,M11,M13	1.5nm	40nm
M5,M6,M10,M12,M14	1.5nm	20nm

The propose circuit at terminal z give output impedance 179.1KΩ up to the frequency of 1Mhz shown in figure 7

The frequency characteristics of terminal w impedance is given as 10.5KΩ up to 10mhz of frequency shown in figure 8

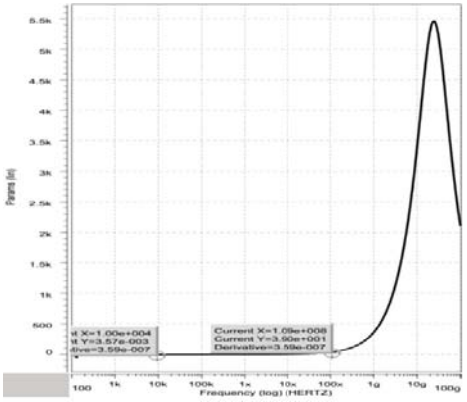

Figure 6 Input impedance of N&P wrt frequency.

Parameter of Circuit	Ref.[5]	Ref.[6]	Ref[7]	This work(CNT Based)
Supply voltage	±5v	±0.9v	±0.6v	±0.6v
Transistor count	45	28	18	18
Terminal-p resistance	645Ω	14Ω	56.4Ω	Few Ω to 37.4Ω
Terminal-n resistance	645Ω	14Ω	56.4Ω	Few Ω to 37.4Ω
Terminal-z resistance	678MΩ	290kΩ	157kΩ	179.1kΩ
Terminal-w resistance	49Ω	14Ω	270Ω	10.5kΩ
Power dissipation	NA	1.15mw	565.25uw	128.273uw

Table 3: Propose Results based on CNTFET-CDBA

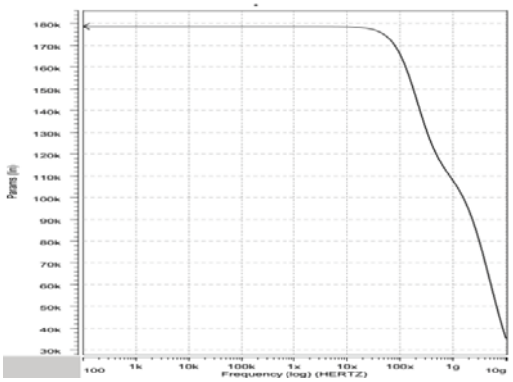

Figure 7. Input impedance of Z wrt Frequency

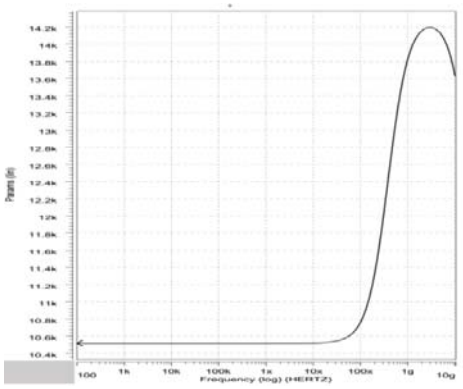

Figure 8. Input impedance of W wrt frequency

IV. CONCLUSION

In this paper CDBA based on CNTFET is proposed which is appropriate for low power low voltage operation at 32nm technology node. The paper has successfully shown the design of CNTFET-CDBA for low voltage and low power along with better port resistance shown in table 3. Further we can improve the circuit by variation in the parameter of CNTFET.

REFERENCES

[1] Toumazou, C., Lidgey, F. J., & Haigh, D. G. (1990). Analogue IC design: The current-mode approach. London: Peter Peregrinus

[2] Cakir, C., & Cicekoglu, O. (2008). Low-voltage high-performance CMOS current differencing buffered amplifier (CDBA). In Pro-ceedings of the 4th IEEE conference on Ph.D. research in microelectronics and electronics (PRIME 2008) Istanbul, Turkey, pp 37–40.

[3] Acar, C., & Ozoguz, S. (1999). A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters. Microelectronics Journal, 30, 157–160.

[4] Sawangarom,V., Tangsrirat, W., & Surakampontorn, W. (2006). NPN-based current differencing buffered amplifier and its appli-cation. In SICE-ICASE international joint conference, Bexco, Busan, Korea.

[5] Tarim, N., & Kuntman, H. (2001). A high performance current differencing buffered amplifier. In Proceedings of the 13th international conference on microelectronics Rabat, Morocco,pp 153–156

[6] Tangsrirat, W., Klahan, K., Dumawipata, T., & Surakampontorn, W. (2006). Low-voltage NMOS-based current differencing buf-fered amplifier and its application to current-mode ladder filter design. International Journal of Electronics, 93(11), 777–791

[7] Cakir, C., Menaei .S & Cicekoglu, O.(2010). Low voltage low power CMOS CDBA. Analog integr. Circ. Signal Processing.pp-237-244

[8] Sumio Iijima," Helical microtubules of graphitic carbon", *Nature, Vol 354, 7th November, 1991*

[9] R.Saito, G.Dresselhaus, M.Dresselhaus, "Physical properties of carbon nanotubes", *World Scientific Publishing Co. Inc.(1998).*

[10] Yong-Bin Kim, "Integrated Circuit Design Based on Carbon Nanotube Field Effect Transistor", *Transactions on Electrical and Electronic Materials, Vol. 12, No. 5, Pp. 175-188,October 25, 2011*

[11]] A. Raychowdhury, K.Roy, "Carbon nanotube electronics : Design of high- performance and low power digital circuits ,*IEEE Transactions on Circuits and Systems-I: Regular Papers 54(11) (2007)*

[12] K. Navi et. al," High Speed Capacitor-Inverter Based Carbon Nanotube Full Adder", *Nanoscale Res Lett (2010) 5,859–862.*

[13] Ali Keshavarzi, et. al ,"Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits Transient Analysis, Parasitics, and Scalability", 2718-2726, IEEE Transactions on Electron Devices, Vol. 53, No. 11,November2006.

[14] J. Appenzeller, "CarbonNanotubes for high performance electronics-progress & prospect," Proc. IEEE, vol. 96, no. 2, pp. 201–211, Feb. 2008.

[15] N. Patil, J. Deng, S. Mitra, and H.-S. P. Wong, "Circuit-level perfor-mance benchmarking and scalability of carbon nanotube transistor cir-cuits," IEEE Trans. Nanotechnol., vol. 8, no. 1, pp. 37–45, Jan. 2009.

[16] N. Patil, A. Lin, E R. Myers, and H.-S. P. Wong, "Integrated wafer-scale growth and transfer of directional carbon nanotubes and misaligned-carbon-nanotube-immune logic structures," in Proc. Symp. VLSI Techno. Dig. Tech. Papers, Jun. 2008, pp. 205–206.

[17] N. Patil, J. Deng, A. Lin, H.-S. P. Wong, and S. Mitra, "Designed meth-ods for misaligned and mispositined carbon nanotube immune circuits," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 27, no. 10, pp. 1725–1736, Oct. 2008. N. Patil, A. Lin, E. R. Myers,

[18] R. Koungmin, A. Badmaev, C. Zhou, H.- P. Wong, and S. Mitra, "Wafer-scale growth and transfer of aligned single-wall carbon nanotubes," IEEE Trans. Nanotechnol., vol. 8, no. 4, pp. 498–504, Jul. 2009.

[19] S. J. Kang, C. Kocabas, T. Ozel, S. Moonsub, N. Pimparkar, M. A. Alam, V. Rotkin, and J. A. Rogers, "High performance electronics using dense perfectly aligned arrays of single walled carbon nanotube," Nat. Nanotechnol, vol. 2, pp. 230–236, 2007.

[20] S. Iijima, "Hellical microtubes of graphite," Nature, vol. 354, pp. 56–58, 1991.

[21] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High perfor-mance silicon nanowire field effect transistors," Nano Lett., vol. 3, no. 2, pp. 149–152, 2003.

[22] Stanford University. (2008). CNFET Model Website, [Online]. Available: http://nano.stanford.edu./model.php.? Id = 23.

[23] J. W. Mintmire and C. T. White, "Universal density of states for carbon nanotubes," Phys. Rev. Lett., vol. 81, no. 12, pp. 2506–2508, 1998.

[24] Z. Yao, C. L. Kane, and C. Dekker, "High-field electrical transport in single-wall carbon nanotubes," Phys. Rev. Lett., vol. 84, no. 13, pp. 1941– 2944, 2000.

[25] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including

nonidealities and its application-part I: model of the intrinsic channel region," IEEE Trans. Electron. Devices, vol. 54, no. 12, pp. 3186–3194, Dec. 2007.

[26] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field effect transistors including nonidealities and application—Part II: Full device model and circuit benchmarking," IEEE Trans. Electron. Devices, vol. 54, no. 12, pp. 3195–3205, Dec. 2007.

[27] A. Javey, J. Guo, D. B. Farmer, Q. Wang, Y. Erhan, R. G., Gordon, Lundstrom, and H. Dai, "Self-alligned ballistic molecular transis-tors and electrically parallel nanotube arrays," Nano Lett., vol. 4, no. 7, pp. 1319–1322, 2004.

[28] J. Deng and H.-S. P. Wong, "A circuit-compatabile spice model for en-hancement mode carbon nanotube field effect transistors," in Proc. Int. Conf. Simul. Semicond. Process Devices, Sep. 2006, pp. 166–169.

[29] J. Deng, N. Patil, K. Ryu, A. Badmaev, C. Zhou, S. Mitra, and H.-S. P. Wong, "Carbon nanotube transistor circuits: circuit-level performance benchmarking and design options for living with imperfections," in Proc. Int. Solid State Circuit Conf., San Fransisco, CA, Feb. 2007, pp. 70–588.