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Performance Investigation of Emerging Nano Devices for Low Power Analog Circuits

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Abstract—**Differential amplifiers are essential part of several analog systems. This paper proposes a design of Single Stage Differential Amplifier based on the 32 nm FinFET technologies. We have designed a differential amplifier for certain specifications such as Slew Rate, Gain, CMRR, Unity Gain Bandwidth and Frequency Response and its comparison with 32 nm differential amplifiers using conventional MOSFET, FinFET and CNFET is made. The proposed typical Single Stage Differential Amplifier is given a supply voltage of 1.0V and it generates an open loop Gain of 19.39 dB, Slew Rate of 8.74E+6 V/µsec, Unity Gain Bandwidth of 256 MHz. All Simulations are done on Hspice simulation software. The simulations focus that, at the existing stage, the FinFET circuit performs best than the MOSFET and CNFET in terms of Gain, CMRR and Slew Rate.**

Keywords- CNFET; Differential amplifier; MOSFET; Slew Rate; Cutoff frequency; Independently Driven Double Gate (IDDG); C_L (Load Capacitance).

I. INTRODUCTION

The movement in CMOS scaling is pushing device dimensions to the Decca-nanometer. This needs to present novel materials and novel device structures to take of the advantages as far as device performance connected with device scaling [1].

Voluminous technological and device structure variants will be proposed, like Single gate FETs, SOI FETs, multiple-gate FETs and CNFETs etc and so forth to make accessible extensions. Amongst that, FinFETs and CNFETs have been as of late turning into an essential innovation for low power, little voltage applications. Double Gate based transistors are capable to substitute CMOS later on, because of its higher electrostatics, higher versatility and stability. Differential amplifiers are key component of the analog circuits [2].

The Carbon nanotubes existing are exclusive prospect as one and only of the rare schemes where the investigational device dimensions will extent to the very small models. Might equal the forecasts, thus in belief permitting the experimental justification of computational methods and computational device scheme [3].

It is fundamental to create extraordinary enactment analog integrated circuits with diminished supply voltages. At tremendous supply voltages, there is a trade-off amongst Power, Slew Rate and Gain and other performance parameters. During this paper, we tend to concentrate on projected style and examination of low-power, low-voltage Single Stage Differential Amplifier utilizing MOSFET, CNFET and FinFET technology. Simulation characteristics of FinFET based differential amplifier is compared with conventional CMOS and CNFET based differential amplifier.

The simulations are done on all the device types namely MOSFET, CNFET and FinFET and are compared accordingly for best result on device type.

II. DG-FINFET AND CNFET DEVICE STRUCTURE

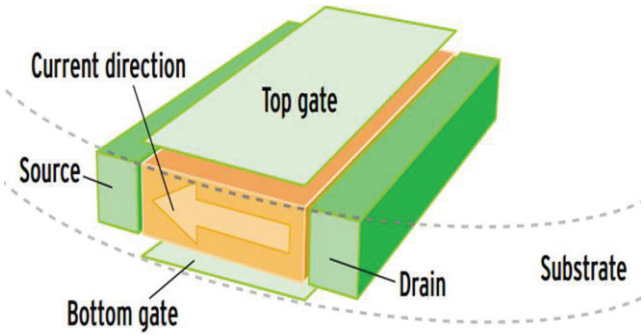

Figure 1(a). FinFET Structure [4].

A FinFET transistor at Nano meter technology has a potential to interchange bulk devices [4, 5]. The dual gated MOS scheme FinFET which contributes higher enactment since they are fewer prone to short channel effect [14]. FinFET assures to substitute MOSFETs since it has more ability in regulating drip and decreasing short channel effects however providing a robust current [15]. The FinFET structure is as appeared in Figure 1 (a). FinFET is designed as a 3T (three-terminal), shorted both gates, and 4T (four-terminal), where one gate is fix, gate bias and the control terminal the facade gate [11, 16]. Prior research works have assessed the upgrade of FinFET advances, determining that FinFETs are alluring for RF, low power and low frequency applications [1, 5]. The three-terminal symmetric FinFET is well thought-out in line for its improved drive current capability as matched to other structures [4, 18].

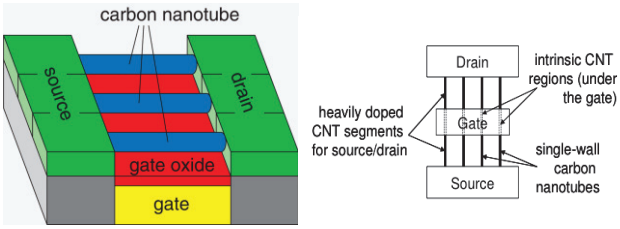

Figure 1(b). CNFET Structure [6,13].

A pane of graphite is roll along a wrap vector to form CNT. Depending on chirality vector metallic or semiconducting Single-walled CNT (SWCNTs) could be available [6]. In Carbon Nanotube Field Effect Transistor, single or many semiconducting SWCNTs are castoff. Figure 1 (b) shows the channel of the device. The carbon Nano-tube diameter is mentioned in terms of a chirality vector. The arrangement is specified in terms of an index (n, m) where m, n is the pair of integers that express its chirality vector. The Nano tube diameter D_t in terms of n and m is given below, Where a_o = 0.142nm in the inter molecular distance in the middle of each carbon atom and another adjacent atom [9, 12].

$$D_t = \frac{\sqrt{3}a_0}{\pi}\sqrt{m^2 + mn + n^2} \quad (1)$$

Relating the circuits utilizing CMOS and the circuits utilizing CNFET with per device 1 to 10 carbon nanotubes is around two to ten times speedier, the per cycle expending vitality is around seven to two times lesser, and Power delay product exists adjacent twenty to fifteen times second rate, in perspective of the precise format example and capacitance of interconnect wiring [7].

III. Scheme Of Single Stage Differential Amplifier Circuit.

In this area, we understood three adaptations of the differential amplifiers supported the CMOS, CNFET and FinFET technology at 32nm node. Circuit simulator used is Synopsys HSPICE. FinFET based Single Stage Differential Amplifier is appeared in Figure 2. CNFET centred differential amplifier circuit is appeared as far as ideal basic device parameters to be specific Number of nanotubes (N), inter nanotube spacing pitch (S), diameter of CNT, and input supply voltage (V) [2, 17].

The chief outline issue for the analog designer, when managing a CNFET technology, is the sizing of the transistors to meet the desired performance and electrical characteristics. In the CMOS and FinFET, the optimization variables are the W and L of the transistors and in the CNFET N, S and V are the variables. The differential amplifier scheme factors values are selected for FinFET, CMOS and CNFET as listed in TABLE I.

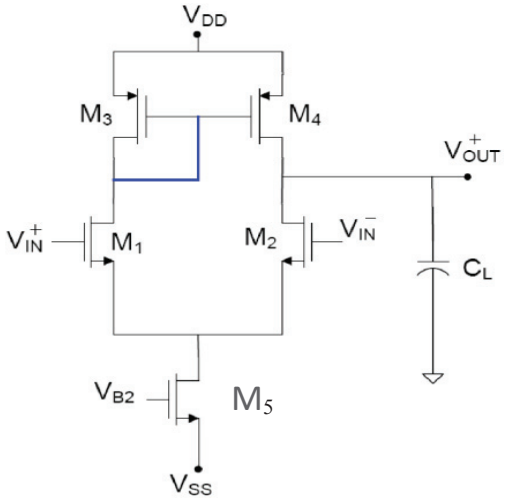

Figure 2. Single-Stage Differential Amplifier.

TABLE I
OPTIMIZED CIRCUIT PARAMETERS AND ITS VALUE OF CMOS, CNFET and FinFET.

Parameter	CMOS 32nm		CNFET 32nm		FinFET 32nm	
	L	W	S	N	L	W
M_1	32 nm	12 µm	20	3	32 nm	50 µm
M_2	32 nm	12 µm	20	3	32 nm	50 µm
M_3	32 nm	60 µm	20	3	32 nm	10 µm
M_4	32 nm	60 µm	20	3	32 nm	10 µm
M_5	32 nm	150 µm	20	3	32 nm	150 µm
C_L	1 FF		1 FF		1 FF	

IV. Simulation Results Analysis And Comparsion

All these above mentioned parameters are the performance measure of differential amplifier. The performances features and robustness of the three differential amplifiers (utilizing 32nm-CNFET, 32nm FinFET and 32nm-CMOS technology) are investigated comprehensively as far as the circuit specifications, for example, SR (Slew Rate), open loop Gain, CMRR (common-mode rejection ratio), Frequency Response, Unity Gain Bandwidth. The performance characteristics of the differential amplifier is obtained by simulating the circuits at 1.0 V and 1.8 V V_{DD} supply. All the stimulated graphs are shown below.

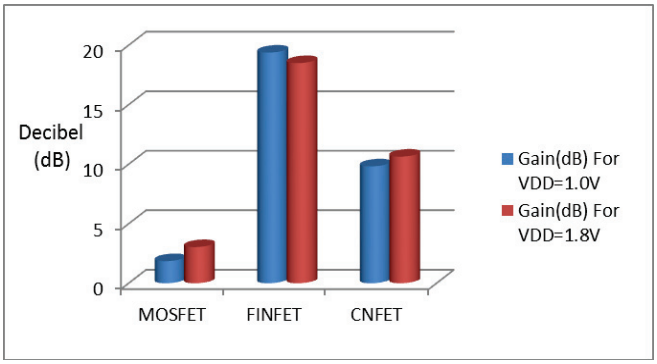

Figure 3. Gain of Differential Amplifier in dB.

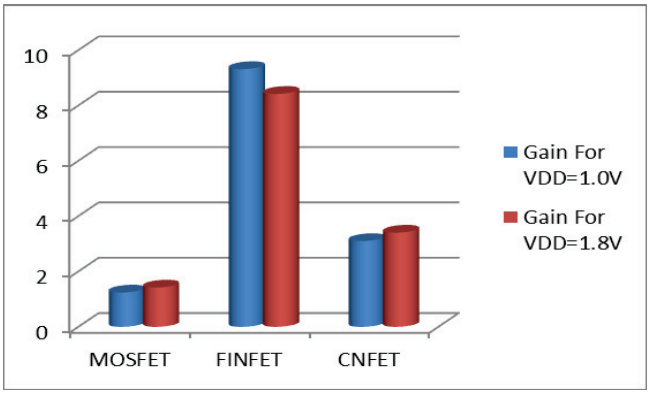

Figure 4. Gain of Differential Amplifier.

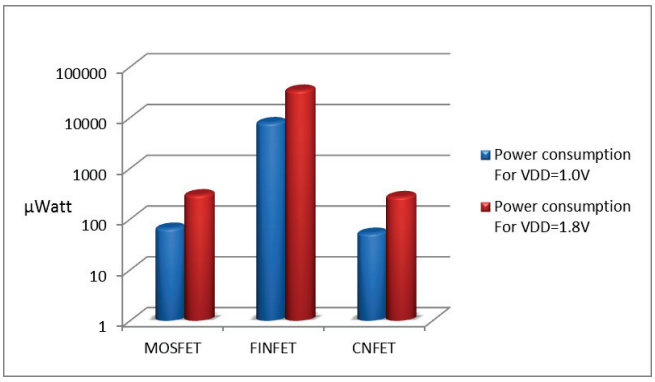

Figure 5. Power Consumption of Differential Amplifier.

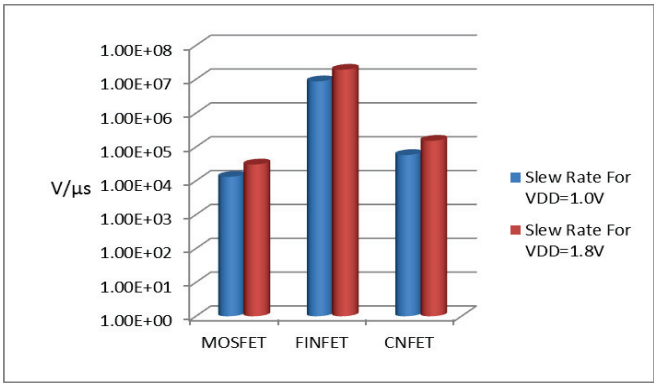

Figure 6. Slew Rate of Differential Amplifier.

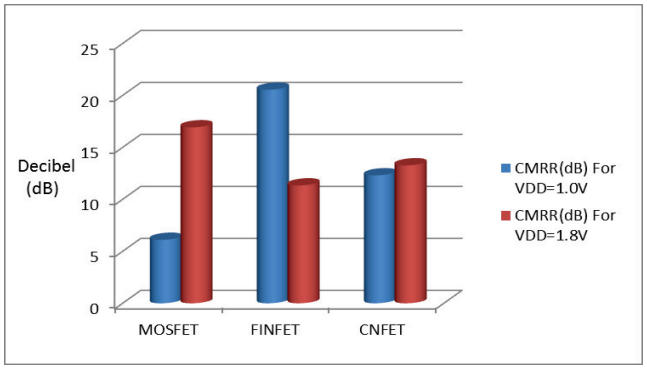

Figure 7. CMRR of Differential Amplifier.

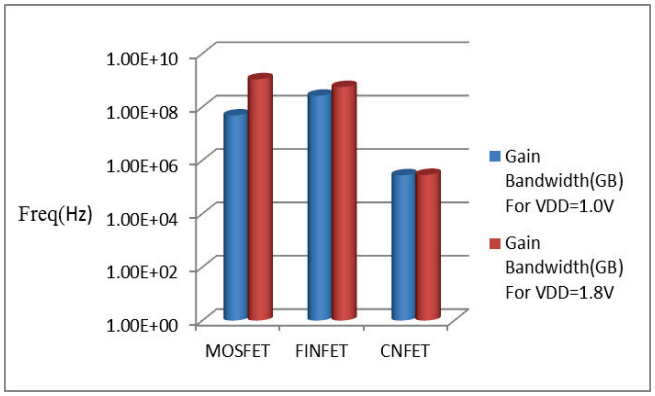

Figure 8. Gain Bandwidth product of Differential Amplifier.

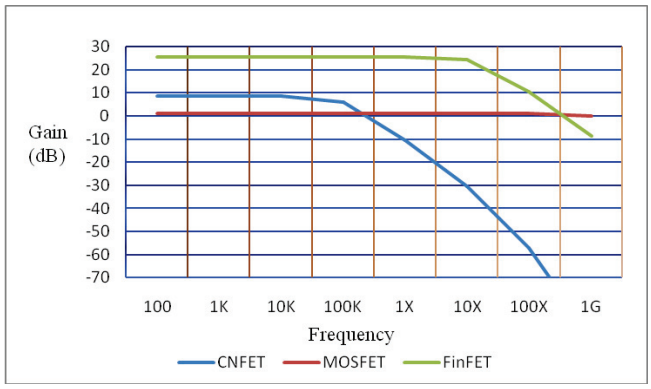

Figure 9. Frequency Response for V_{DD}=1.0V.

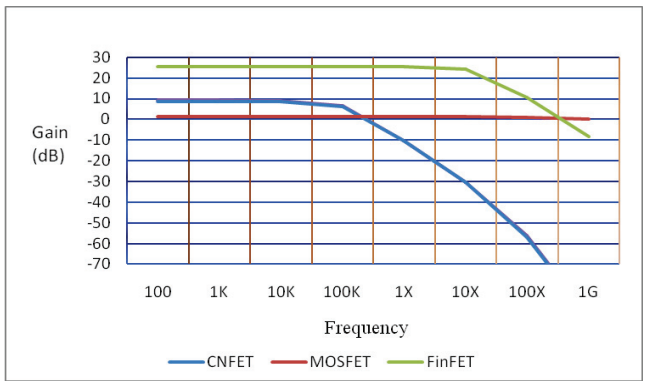

Figure 10 Frequency Response for V_{DD}=1.8V

The modelled results of the proposed FinFET, CNFET and MOSFET centred differential amplifiers is shown in TABLE II and comparative graphs of Gain (dB), Gain, Power Consumption, Slew Rate, CMRR, and Unity Gain Bandwidth and Frequency Response waveforms are shown in Figure 3, 4, 5, 6, 7, 8, 9 and 10 respectively. Consequences of the simulation confirm that FinFET constructed differential amplifier have a substantial enhancement in terms of Gain, Slew Rate, CMRR but Power Consumption is greater in comparison with the other conventional 32-nm CMOS and CNFET. At lower supply voltage the Gain and Slew Rate of Differential amplifier using FinFET increases than at 1.8 V_{DD} supply. Furthermore at lower supply voltage, there is reduction in differential amplifier power consumption. Differential amplifier utilizing 32nm CNFET has low Power Consumption. The Power Consumption in Differential Amplifier mostly relies on the biasing current. Along these lines Power Consumption of FinFET device can further be lessened by diminishing the biasing current and modifying the W/L proportion suitably.

The one-dimensional nature of carbon Nanotubes eliminates the problem of carrier scattering and dangling bonds, reducing the power consumption of CNFET devices.

TABLE II COMPARISON OF CNFET, MOSFET AND FinFET DIFFERENTIAL AMPLIFIER.

Parameters	32 nm CNFET		32 nm MOSFET		32 nm FinFET		[8]	[10]
V_{DD} (V)	1.0	1.8	1.0	1.8	1.0	1.8	1.0	1.0
Gain	3.1	3.41	1.25	1.42	9.325	8.42	25.11	…..
Gain (dB)	9.82	10.64	1.87	3.04	19.39	18.5	28	59
Frequency Response(Hz)	107K	98.7K	25.6M	479M	55.2M	223M	10 G	….
Slew Rate (V/µsec)	58100	153000	13200	30500	8.74E+6	192e+5	.....	….
CMRR(dB)	12.31	13.27	6.1050	16.93	20.55	11.34	70-90	…..
Unity Gain Bandwidth(Hz)	278K	287K	48.3M	1100 M	256M	562 M	.....	3.5G
Power Consumption (µWatt)	52.3	275	65.6	299	7870	34400	77	10

V. CONCLUSION

This paper investigates the advantages offered by rising FinFET technology over the current CMOS technology in analog circuits. CNFETs absolutely have arisen an extended way meanwhile the main innovation, to entitlement their supremacy above conventional devices. We conclude that CNFET version has low Power Consumption with improved Gain and Slew Rate than MOSFET and Frequency Response of CNFET based differential amplifier is lower than MOSFET based amplifier. The principle impact of this paper is the straight forward correlation among rising innovations; characteristic of that CNFET and FinFET are contender to challenge with the CMOS devices intended for the low-power analog circuits. A further research can be investigated by method for decreasing the power utilization in FinFET and enhancing the frequency reaction of CNFET for differential amplifiers.

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