Carbon Nanotube CMOS Analog Circuitry

Rebecca Ho, Christian Lau, Gage Hills, Max M. Shulaker

***Abstract*— Carbon nanotube (CNT) field-effect transistors (CNFETs) promise significant energy efficiency benefits versus today's silicon-based FETs. Yet despite this promise, complementary (CMOS) CNFET analog circuitry has never been experimentally demonstrated. Here we show the first reported demonstration of full CNFET CMOS analog circuits. For characterization, we fabricate analog building block circuits: multiple instances of two-stage op-amps. These CNFET CMOS op-amps achieve gain >700 (maximum derivative of output voltage with respect to differential input voltage), operate at a scaled sub-500 mV supply voltage, achieve high linearity (even when operating at these scaled voltages), and are robust over time (minimal drift over >10,000 cycled measurements over 12 hours). Additionally, we demonstrate a front-end analog sub-system that integrates a CNFET-based breath sensor with an analog sensor interface circuit (transimpedance amplifier followed by a voltage follower to convert resistance change of the chemoresistive CNFET sensor into a buffered output voltage). These experimental demonstrations are the first reports of CNFET CMOS analog functionality that is essential for a future CNT CMOS technology.**

***Index Terms*— carbon nanotubes, CNFETs, analog, CMOS**

I. Introduction

Carbon nanotubes (CNTs) are an emerging nanotechnology for next-generation electronics [1], [2]. CNTs can be used to form CNT field-effect transistors (CNFETs), which owing to their nanometer thin body (~1 nm CNT diameter) exhibit excellent electrostatic control and simultaneously high carrier transport [3]–[5]. Due to these properties, digital circuits fabricated with CNFETs promise a 10× improvement in energy-delay product (EDP: a metric of energy efficiency), versus silicon FETs [1].

Despite these advantages, there remain major challenges towards realizing a future CNFET technology. While a full complementary (CMOS) CNFET technology is required to realize the above energy-efficiency benefits [6], all complete digital CNFET systems have been fabricated from PMOS-only CNFETs [2], [7]–[9], and all reported CNFET CMOS demonstrations have been limited to only individual devices, small-scale circuits, or digital logic [10]–[15]. Importantly, due to the lack of a robust CNFET CMOS process, there has been no reported demonstration of CNFET CMOS analog circuitry (while the vast majority of circuitry in a system today is digital logic, analog circuits are still essential for applications ranging from sense amplifiers for memory arrays to high speed input/output links [16]). Moreover, similar to benefits for digital logic, CNFET CMOS promise analog circuit performance benefits, providing additional motivation to realize CNFET CMOS for analog circuitry (Fig. 1).

In this work, we experimentally demonstrate the first reported CNFET CMOS analog circuit blocks. We show multiple examples of analog circuits blocks (two-stage op-amps), which achieve gain of >700 and can also operate at scaled sub-500 mV supply voltages (with simultaneously high linearity, see Sec. III). Moreover, we integrate these analog circuit blocks to create a complete front-end analog sub-system: a CNFET-based breath sensor integrated within an analog sensor interface circuit. Taken together, this work illustrates the feasibility of a future CNFET CMOS technology.

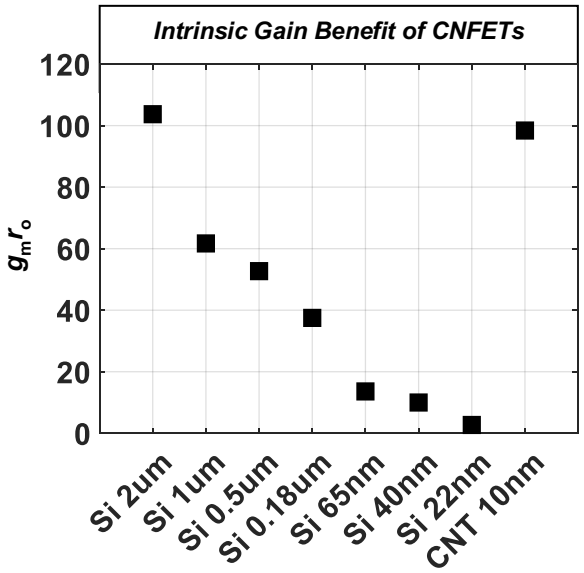

Fig. 1. Intrinsic gain ($g_m r_o$) [17] benefits of CNFETs. For silicon CMOS, intrinsic gain degrades as technology node scales [18], [19]. However, the intrinsically higher transconductance (g_m) of CNTs results in CNFETs at aggressive 10 nm technology nodes still achieving the same intrinsic gain as silicon FETs at relaxed >1 μm technology nodes. Thus, CNFETs can enable implementation of analog circuits at aggressive technology nodes while simultaneously achieving high intrinsic gain, enabling substantial area scaling of analog circuitry. The intrinsic gain is extracted from circuit simulations (Cadence Spectre®) using commercial process design kits (PDKs) for silicon CMOS, and using an experimentally calibrated compact model for CNFETs (calibrated using CNFETs with sub-10 nm channel length) [20].

II. CNFET CMOS Process Flow

Fig. 2 shows our CNFET CMOS fabrication flow [10]. The CNFETs are fabricated with a back-gate device structure with a metal gate (Pt) and high-*k* gate dielectric (20 nm HfO_2 deposited through atomic layer deposition, ALD). Post gate-stack fabrication, the CNTs are deposited through a solution-based incubation process [21]. This solution-based CNT deposition enables the entire CNFET fabrication process to be low temperature (<250 °C)[1]. To fabricate the PMOS and NMOS CNFETs, we leverage a dual doping strategy which uses both source and drain metal contact work function

[1] The high-temperature growth process of CNTs is decoupled from the wafer substrate by using a solution-based incubation process to deposit CNTs. Such low-temperature fabrication enables greater CNFET integration, as the CNFETs can be fabricated in the back-end-of-line (BEOL) directly over silicon CMOS substrates.

engineering as well as oxide-based electrostatic doping. The source and drain are lithographically patterned (0.5 nm Ti / 45 nm Pt for PMOS, 75 nm Ti for NMOS), and the PMOS CNFETs are encapsulated with SiO_X while the NMOS devices are encapsulated with ALD-deposited HfO_X (the stoichiometry of the SiO_X and HfO_X sets the threshold voltage of the PMOS and NMOS, respectively). This CNFET CMOS process leverages only solid-state and silicon CMOS compatible materials, and results in well-matched PMOS and NMOS CNFETs (Fig. 3).

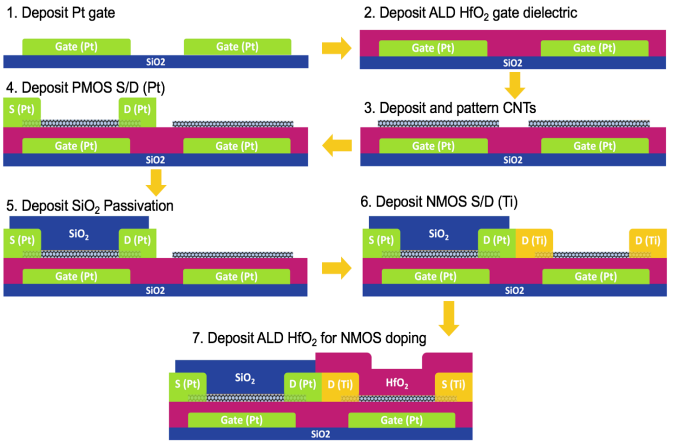

Fig. 2. CNFET CMOS process flow. A back-gate geometry is used for both the PMOS and NMOS CNFETs. All low-temperature (<250 °C) processing is performed with solid-state and silicon CMOS compatible materials.

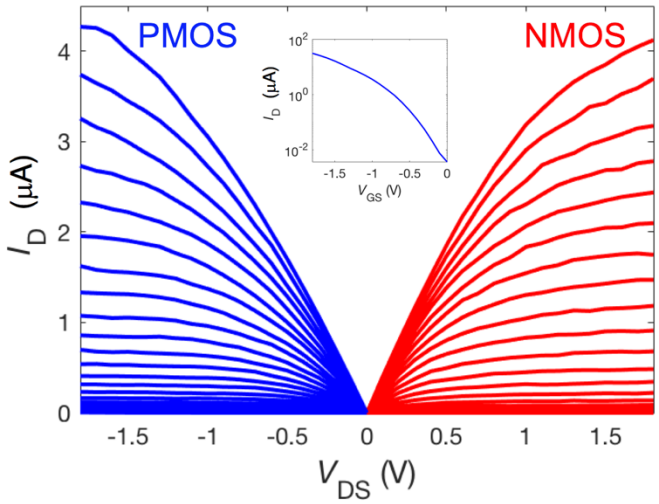

Fig. 3. Characteristics of PMOS and NMOS CNFETs with a channel length of ~2.5 μm and width of ~4 μm. I_D-V_{DS} curves show well-matched CNFET CMOS (i.e., with similar on-current for both NMOS and PMOS). V_{GS} range from 0 V to V_{DD} (1.8 V) with an increment of 0.1 V (for NMOS, V_{GS} from 0 to -V_{DD} for PMOS). Inset shows an I_D-V_{GS} curve of a PMOS CNFET with I_{ON}/I_{OFF} > 8000.

III. Experimental Results

As an initial demonstration, we fabricate a fundamental building block of analog circuits: an op-amp [17]. Fig. 4a shows the circuit schematic of our 2-stage op-amp, while Fig. 4b shows a scanning electron microscopy (SEM) image of a fabricated CNFET CMOS op-amp. Fig. 4c displays the voltage transfer curve for a 1-stage op-amp (the first stage of the op-amp shown in Fig. 4a). Measurements from multiple fabricated 2-stage op-amps are overlaid in Fig. 4d, showing gain >700 (Fig. 4e) with minimal device mismatch (the average offset voltage, V_{OFFSET}, defined as the differential input voltage that achieves maximum gain (ideally 0 V), is <12 mV for all op-amps shown in Fig. 4d).

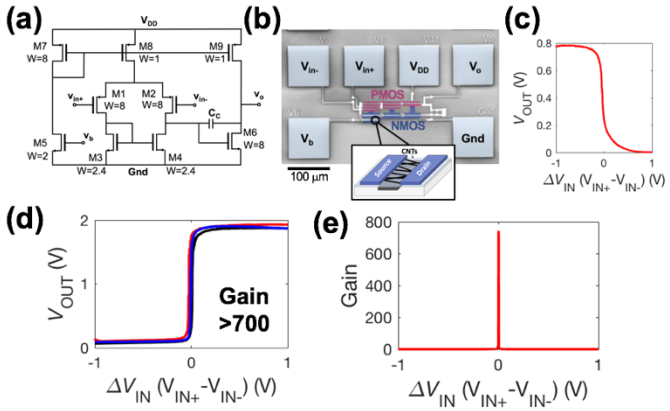

Fig. 4. CNFET CMOS 2-stage op-amp. (a) Schematic of op-amp. All widths are multiples of minimum width FET (W_{MIN} = 5 μm, $L_{channel}$ = 3 μm). (b) Scanning electron microscopy (SEM) image of fabricated 2-stage op-amp, false-colored to show the PMOS and NMOS CNFETs in the circuit. (c) Measured waveform of a fabricated 1-stage op-amp (first stage of the 2-stage op-amp) and (d) overlaid measured waveforms of multiple (three) fabricated 2-stage op-amps, showing output voltage as a function of the differential input voltage (V_{IN+} - V_{IN-}). (e) Derivative of V_{OUT} with respect to ΔV_{IN} (showing maximum gain). For the 2-stage op-amp, maximum gain is >700, output swing >90% of V_{DD}, and the well-matched CNFETs result in average V_{OFFSET} < 12 mV.

Leveraging this building block, we demonstrate a CNFET-based analog sub-system: a front-end integrated sensor and sensor interface circuit that converts the resistance change of a chemoresistive CNFET sensor into a buffered output voltage. The sub-system consists of a transimpedance amplifier (TIA) to convert the input current (a function of the chemoresistive CNFET sensor) to a voltage, cascaded to a voltage buffer. To characterize the sub-system, we initially fabricate the circuit shown in Fig. 5a. The CNFET chemoresistive gas sensor is replaced with an externally controlled current source (I_{IN}) to remove any variability introduced by the sensor itself. A SEM (false-colored for clarity) of the fabricated circuit is shown in Fig. 5b. To characterize the circuit, we sweep a DC current at the input of the system and measure the corresponding voltage output from the voltage buffer. Fig. 5c shows the measured output (with a 2 V supply voltage); as expected, the output voltage changes linearly with the input current over the entire input range (10 μA to 50 μA, designed the match the chemoresistive sensor). To quantify the linearity of the response, we calculate the coefficient of determination, R^2, for the measured response to a best-fit linear line [22]. The average R^2 across the entire input range is 0.999, illustrating high linearity (*e.g.*, the measured response closely follows a linear relationship to input current). Moreover, Fig. 5d shows 100 repeated measured waveforms overlaid on top of one-another, illustrating robust operation with minimal drift.

Additionally, we show the CNFET CMOS circuitry can operate at scaled supply voltages without degrading key circuit performance metrics. Fig. 5(e-f) shows the response of the system with a scaled 480 mV supply voltage. The measured response still exhibits high linearity (R^2 value of 0.998 to a best-fit linear line), as well as similarly minimal drift over 100 repeated measurements.

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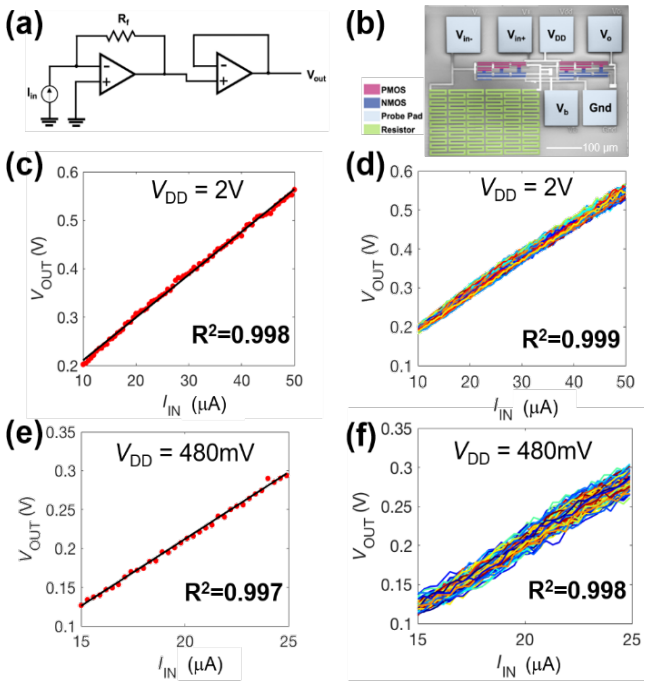

Fig. 5. Characterization of analog sub-system, with the CNFET sensor replaced with an external current source. (a-b) schematic and SEM. (c) measured linear response of the sub-system, converting input current to output voltage. (d) 100 repeated measurement cycles, illustrating minimum drift. (e-f) repeated measurements of (c-d), with supply voltage reduced from 2 V to 480 mV. Functionality and linearity are not sacrificed even at scaled <500 mV supply voltages.

Fig. 6 shows the complete integrated sensor and sensor interface sub-system. As shown in the schematic in Fig. 6a, an on-chip integrated CNFET chemoresistive gas sensor replaces the external DC current supply at the input of the TIA. The CNFET chemoresistive gas sensor is fabricated using the same process flow shown in Fig. 2,[2] but all of the oxide covering the CNFET chemoresistive gas sensor is removed with a dilute HF wet etch[3]. Thus, the CNFET chemoresistive gas sensor is exposed to the environment, while all other CNFETs (e.g., the CNFETs comprising the amplifiers) are encapsulated with a dielectric and are thus protected from the ambient. An SEM of the fabricated sub-system is shown in Fig. 6b. To characterize the response of the sub-system, the sensor is kept in a controlled constant ambient (*e.g.*, dry air), and the input voltage (V_{IN}, Fig. 6c-d) applied across the sensor is swept. Similar to the sub-system in Fig. 5 with a constant current source as the input, the measured output voltage (V_{OUT}) of the sub-system exhibits high linearity (R^2 value of 0.999 to a best-fit linear line). Moreover, Fig. 6d shows the circuit is robust and air-stable: 10,000 repeated DC measurements performed over 12 hours illustrate minimal drift.

To test the full integrated sensor and sensor interface circuitry, we alternate between one-minute intervals of breathing and blowing N_2 gas directly over the sensor. The CNFET gas sensor reversibly responds to warm breath, resulting in the front-end sub-system voltage output toggling between ~0 V and ~2 V, illustrating correct functionality of the circuit with successful detection and response to breath.

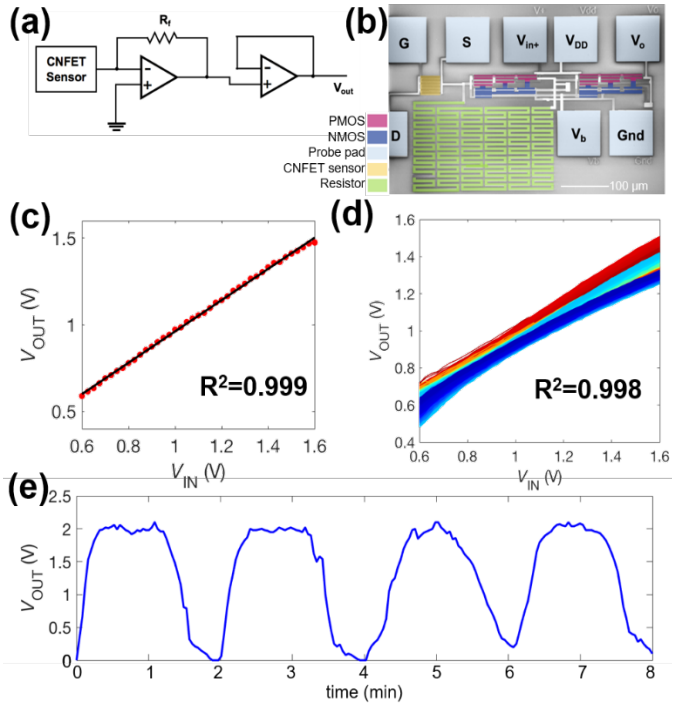

Fig. 6. Characterization of analog sub-system, with an on-chip integrated CNFET chemoresistive breath sensor. (a-b) schematic and SEM. (c) Measured linear response of the sub-system, measured by keeping the sensor in N_2 ambient air and sweeping the input voltage, V_{IN+}, applied across the sensor. The response is highly linear with a R^2 value of 0.999. (d) 10,000 repeated measurement cycles, illustrating minimum drift. The first 2500 cycles are red, the next 2500 cycles are yellow, the next 2500 cycles and light blue, and the last 2500 cycles are dark blue. The spread in the measured outputs is not random noise, but rather minor slow drift of the circuit after constant measuring for 12 hours. Future work can improve upon stability by optimizing the gate stack to minimize interface traps at the CNT-gate dielectric interface. (e) Measured response of the sub-system in response to alternative exposures to warm breath and N_2. The oscillating response in the circuit illustrates correct function of the integrated sensor/ sensor interface circuit.

IV. Conclusion

This work reports the first demonstration of CNFET CMOS analog circuits. We fabricate foundational building block op-amps up to an analog-based sensor interface circuit. As an experimental demonstration, we integrate the sensor interface circuit with an on-chip chemoresistive CNFET gas sensor, illustrating response and detection of breath. The CNFET CMOS analog circuits achieve high gain (>700) and linearity and operate at scaled sub-500 mV supply voltages (without sacrificing gain or linearity). Thus, this experimental work is a key step towards demonstrating analog functionality that is essential for a future CNFET CMOS technology.

Acknowledgments

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[2] The CNFET chemoresistive gas sensor is also functionalized with a polymer to increase its sensitivity to ambient conditions. There is rich literature describing the design and fabrication of CNFET gas sensors [23]–[25].

[3] The dilute HF wet etch has a high etch selectivity of SiO_X over HfO_X and does not etch or degrade the CNTs.

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