Design of a Novel Ternary SRAM Sense Amplifier Using CNFET

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Abstract

This paper presents a novel design of a ternary SRAM sense amplifier using carbon nanotube field-effect transistors (CNFETs). Chirality of CNFET is used to control the threshold voltage to realize the ternary logic. Simulation results using HSPICE shows that the proposed SRAM sense amplifier perform correctly at 0.9V supply voltage in the ternary SRAM read process. And it can achieve 87.5% and 88.5% enhancement in speed, 84.2% and 85.6% in PDP, compared with a ternary DRAM sense amplifier and the ternary SRAM without sense amplifier.

Keywords—ternary; CNFET; sense amplifier

1. Introduction

In the traditional digital design, the two-valued logic (0 or 1, true or false) is always used. Recently, multiple-valued logic (MVL), especially the ternary logic, has attracted many interests for its advantages over binary logic [1]. Compared to the binary logic design, the ternary logic circuit has fewer operations, less gates, and signal lines. So, it can achieve low power consumption and chip area reduced [2]. In a ternary system, it uses $\log_3(2^n)$ bits to replace n-bit binary number. With more and more information and complex computation in today's computers, ternary logic systems are capable of providing significant power and area efficiency compared to traditional binary systems. Furthermore, serial and serial-parallel arithmetic operations can be carried out faster if ternary logic is employed.

Recently, there are some researches on the design of ternary logic using traditional complementary metal-oxide semiconductor (CMOS) [2][3]. Power consumption and chip area have been reduced a lot. In all these researches, the ternary memory design has been studied for years. However, the design of a simple and robust CMOS ternary memory cell has been very challenging and mostly elusive.

The carbon nanotube field-effect transistor (CNFET) is an excellent alternate to a traditional bulk transistor for low-power consumption and high-performance [4][5]. It has higher ON current compared to MOSFET for the same OFF current. Moreover, the CNFET's threshold voltage is determined by the CNT diameter. Hence, a multi-threshold design can be achieved by using CNFETs which have different diameters. Ternary inverter and SRAM cell has been proposed in [6] and [7]. Simulation results show that the CNFET-based ternary SRAM cell performs the correct function during the read and write operations. And it also achieves high SUN, lower power consumption and low area compared with traditional binary CMOS SRAM cell.

SRAM sense amplifier is one of the most important peripheral circuits in SRAM as it strongly influences the sensing delay and power dissipation of SRAM. It outputs the data in the memory cell by sampling and amplifying the micro differential signal on the bit-lines. In this paper, we propose a novel ternary SRAM sense amplifier based on CNFET. It can sense the three-valued signal on the bit-lines rapidly.

The rest of this paper is organized as follows. Section II starts with an introduction of carbon nanotube field-effect transistor, and the ternary SRAM design in Section III. The novel ternary SRAM sense amplifier is proposed in Section IV. The design is simulated by HSPICE in Section V, which is followed by conclusion in Section VI.

2. Carbon Nanotube Field-Effect Transistor

Carbon Nanotube (CNT) can be divided into multi-walled (MWCNT) and single-walled (SWCNT) [8]. CNTFETs utilize semiconducting single-wall CNTs to assemble electronic devices. A SWCNT could be semi-conductor or conductor, depending on its chirality vector which is represented by the integer pair (n, m). When n = m or n-m = 3i (i is an integer), the CNT is metallic. Otherwise, it is semiconducting. The diameter of CNT is determined by the chirality vector [9]-[11].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (1)$$

where $a_0 = 0.142$ nm is the inter-atomic distance between each carbon atom and its neighbor. The schematic of

CNFET is shown in Fig. 1. Similar to a traditional silicon-based device, the CNFET has four terminals too.

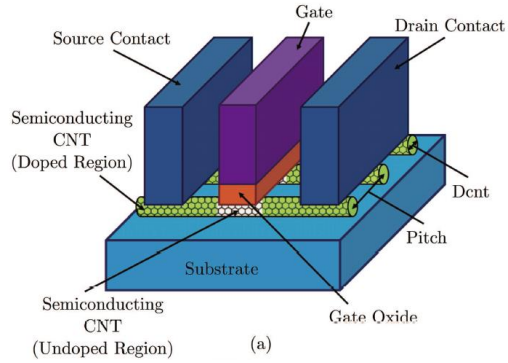

Figure. 1. Schematic of MOSFET-like CNFET [8]

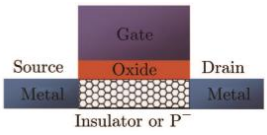

Figure. 2. Schottky Barrier CNFET

Figure. 3. Band-to-band tunneling CNFET

Figure. 4. MOSFET-like CNFET

The CNFET can be divided into three types, Schottky Barrier CNFET, band-to-band tunneling CNFET and MOSFET-like CNFET [8], which are shown in Fig.2, Fig.3 and Fig.4. We often use the MOSFET-like CNFET whose current-voltage (I-V) characteristics are similar to those of MOSFET. This kind CNFET can also be divided into two types, P-type CNFET and N-type CNFET. However, unlike MOSFET devices, P-type CNFET and N-type CNFET have same mobilities and as a result same drive capabilities. As the most important parameter, the threshold voltage of CNFET is approximately considered as the half bandgap and can be calculated by the following equation [9][10]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \qquad (2)$$

where a = 2.49 $\mathring{A}$ is the carbon to carbon atom distance, $V\pi$ = 3.033 eV is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, and DCNT is the diameter of CNT. For example, for a CNTFET with the (n, m) = (19, 0), DCNT is 1.487 nm and its threshold voltages is 0.293 V. Its changeable threshold voltage is the reason why we use CNFET to realize MVL logic.

3. Ternary SRAM Design

Ternary logic is a type of MVL, which consists of three significant logic values. In this paper, V_{dd}, half V_{dd} and 0 represents logic 2, logic 1 and logic 0, respectively, which is shown in Table 1.

Table 1. Logic Symbol

Voltage Level	Logic Value
0	0
1/2 V_{dd}	1
V_{dd}	2

As shown in Fig. 5, a CNFET-based ternary SRAM cell has been proposed in [7]. We only focus on the memory cell (T5-T16) and the read circuits (T1-T4, T17-T20). The threshold voltages of N-type CNFET (T9 and T16, T10 and T15, T8 and T14), P-type CNFETs (T5 and T12, T6 and T11, T7 and T13) which belonging to the memory cell are 0.289V, 0.559V, and 0.428V, −0.289V, −0.559V, and −0.428V, respectively.

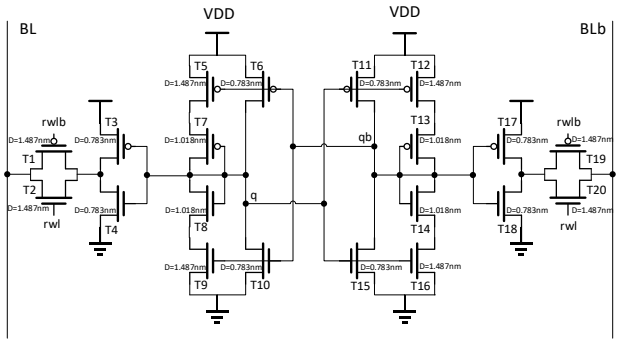

Figure. 5. CNFET-based ternary SRAM cell and read ciucuits

The operation of the memory cell can be described as follows.

1) When holding logic “1”, transistors T5, T7, T8, T9, T12, T13, T14, T16 are ON to hold both nodes q and qb to 1/2 V_{dd};

2) When holding logic “0”, transistors T8, T9, T10, T11, T12, T13 are ON to hold node q to 0 and node qb to V_{dd};

3) When holding logic “2”, transistors T5, T6, T7, T14, T15, T16 are ON to hold node q to V_{dd} and node qb to 0.
On one side, the read buffer is made up of one P-CNTFET (T3 or T17) and one N-CNTFET (T4 or T18) whose threshold voltages is -0.559V and 0.559V, respectively. Before reading, the BL and BLb are charged to 1/2 V_{dd}.
When the rwl is effective, T1, T2, T19 and T20 are ON to charge or discharge BL and BLb. The read operation can be described as follows.
1) When reading logic “1”, T3, T4, T17 and T18 are OFF. BL and BLb remain 1/2 V_{dd}.
2) When reading logic “0”, T3 and T18 are ON, T4 and T17 are OFF to charge BLb to V_{dd} and discharge BL to 0.
3) When reading logic “2”, T4 and T17 are ON, T3 and T18 are OFF to charge BL to V_{dd} and discharge BLb to 0.

4. Proposed Design

Although the read operation of ternary SRAM cell is correct, the speed of it is not very fast. So just as two-valued SRAM circuits, sense amplifier is useful to enhance the performance. Based on the ternary logic circuits, a novel ternary SRAM sense amplifier is proposed in this paper. As shown in Fig. 6, the proposed sense amplifier has eight N-type CNFETs and eight P-type CNFETs. T1 and T9, T8 and T16 whose threshold voltages are −0.508V and 0.508V are control gates to control the sense amplifier to work (charge or discharge). When the voltage of BL or BLb gets higher than 0.508V or lower than 0.392V, the proposed sense amplifier starts to work. The threshold voltages of N-type CNFETs (T6 and T15, T7 and T14, T5 and T13), and P-type CNFETs (T2 and T11, T3 and T10, T4 and T12) belonging to the sensing part are 0.289V, 0.559V, and 0.428V, −0.289V, −0.559V, and −0.428V, respectively.
During the prepared time, two bitlines and two output points are charged to 1/2 V_{dd}. After the read signal is effective, the read buffers begin to read the data in the SRAM cell which leads the voltage changes on the bitlines. And at the same time, the proposed sense amplifier senses the little changes on the bitlines and amplifies them quickly.
The operation of the proposed sense amplifier can be described as follows.
1) When reading the logic “1” in the SRAM cell, the voltage of the BL and BLb is 1/2 V_{dd}. Transistors T1, T8, T9 and T16 are OFF, T2, T4, T5, T6, T11, T12, T13, T15 are ON to keep both nodes OUT and OUTb to 1/2 V_{dd}.

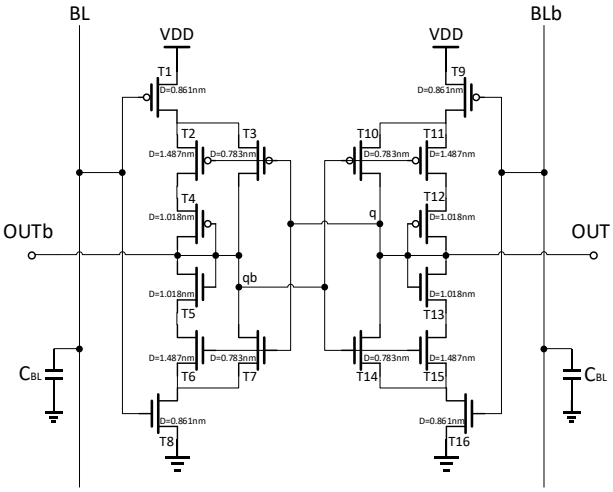

Figure. 6. Proposed ternary SRAM sense amplifier

2) When reading the logic “0” in the SRAM cell, the voltage of BL is getting higher than 0.508V and that of BLb is getting lower than 0.392V. Then transistors T1 and T16 are ON, T8 and T9 are OFF, T2, T3, T4, T13, T14 and T15 are ON to charge the node OUTb to V_{dd} and discharge the node OUT to 0.
3) When reading the logic “2” in the SRAM cell, the voltage of BLb is getting higher than 0.508V and that of BL is getting lower than 0.392V. Then, transistors T8 and T9 are ON, T1 and T16 are OFF, T5, T6, T7, T10, T11 and T12 are ON to charge the node OUT to V_{dd} and discharge the node OUTb to 0.

5. Simulation

In this section, the proposed ternary SRAM sense amplifier is simulated by HSPICE with the CNFET model from Stanford University [9]. The proposed design is compared with a ternary DRAM sense amplifier which is shown in Fig. 7 at 32nm CNFET technology. The supply voltage (V_{DD}) is 0.9V and the capacitance of bitline (C_{BL}) is 100fF which represents the capacitance of more than 16000 memory cells.

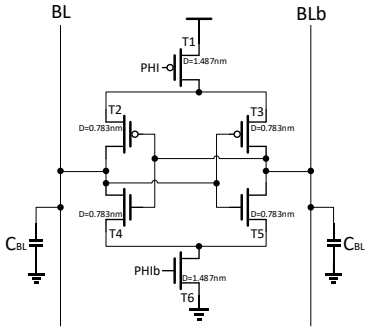

Figure. 7. Ternary DRAM sense amplifier [11]

The simulation result of the proposed sense amplifier is shown in Fig. 8. We can see that the proposed sense amplifier performs correctly and efficiently. It can read and output the data in the cell by sensing the voltage changes in the bitlines.

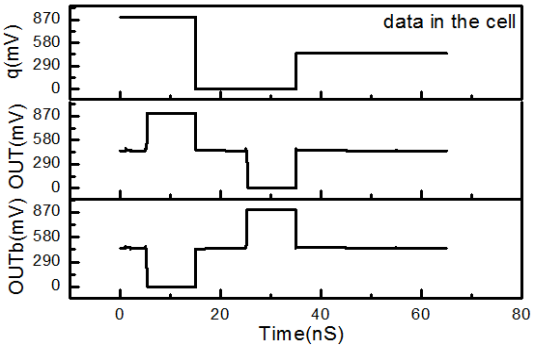

Figure. 8. Simulation of the proposed design

Table 2. Simulation Results

	Proposed SA	DRAM SA	Without SA
Delay-read 2 (pS)	254	2065	2237
Delay-read 1 (pS)	NA	NA	NA
Delay-read 0 (pS)	267	2058	2227
Delay-average (pS)	260.5	2061.5	2232
Power-read 2 (uW)	1.41	1.24	1.26
Power-read 1 (uW)	0.35	0.04	0.03
Power-read 0 (uW)	1.41	1.24	1.26
Power-average (uW)	1.05	0.84	0.85
PDP	273.5	1731.7	1897.2

The simulation results are shown in Table 2. We separate the simulation results into three parts: read 2, read 1 and read 0. We could not get the delay time of read 1 part for the reason that the voltages of OUT and OUTb are same as that of prepared time. Compared with the DRAM sense amplifier and ternary SRAM without using sense amplifier, the proposed design enhances about 87.5% and 88.5% in average speed, 84.2% and 85.6% in PDP, respectively, although costs only a little more in power consumption.

6. Summary

This paper has presented the first design of a ternary SRAM sense amplifier based on the multi-diameter (multi-threshold voltage) CNFETs. Simulation results using HSPICE shows that the proposed design can work correctly and efficiently. It can achieve about 87.5% and 88.5% enhancement in average speed, 84.2% and 85.6% in PDP, comparing with the ternary DRAM sense amplifier and ternary SRAM without using sense amplifier. In conclusion, the proposed ternary SRAM sense amplifier using CNFET can achieve high performance in speed, PDP and chip area.

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