Design and Simulation of Carbon Nanotube Based Current Source Load Differential Amplifier

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Abstract-In this paper, we design and simulate a current source load differential amplifier (CSL-DA) employing n-type carbon-nanotube field effect transistors (CNTFET). The proposed DA employs current source load and is based on 45nm technology node CNTFETs. The performance of the proposed CNTFET based DA has been compared with the conventional metal oxide semiconductor FET (MOSFET) based DA. The HSPICE simulation study has shown a substantial improvement in various important performance measuring parameters in the proposed DA in comparison to the conventional DA. The performance enhancement in the proposed device can be attributed to the unique properties of CNTs. It has been observed that the CNTFET based DA has got 2.7 times enhancement in gain, three orders increase in bandwidth, 1180 times increase in unity gain bandwidth and ~70% reduction in power consumption compared to the conventional MOS based counterpart. Further, optimizing various CNT parameters like number of CNTs (N), CNT pitch (S), CNT diameter can optimize the performance of the proposed DA further.

Keywords— Nanotechnology, Carbon Nanotubes (CNT), Operational amplifier, Differential amplifier

I. INTRODUCTION

Operational amplifier (OP-AMP) is an important and well known analog building block with a wide range of applications. Differential amplifier is an important part of an operational amplifier, as it amplifies the difference of input signals [1-2]. There are three types of differential amplifiers (DA); source coupled pair (SCP), source cross-coupled pair (SCCP) and the current source lead differential amplifier (CSL-DA). These differential amplifiers have been designed in the conventional bipolar and CMOS technologies [3-4]. However, these technologies have their own limitations, like high power consumption in bipolar technology, speed issues in MOS technologies. The conventional MOSFET has been used to realize these blocks till date. However, nano scaled MOSFET has many limitations, which restrict their use in realizing high performance analog and digital blocks. The various issues associated with a nano scaled MOSFET like short channel effects (SCE), leakage current, reliability issues, self-heating etc. restrict its applications [5-7]. Therefore, it is the need of the hour to replace silicon as a material and CMOS as a circuit design approach to extract more and more performance and to keep Moore's law valid. Many new materials like GaN, SiC, GaAs etc. have been used and new and advanced device structures, like FinFETs, double gate (DG) MOSFETs, Trigate devices, have been designed and developed. They have indeed shown better performance; however, they are complex, costly and have fabrication issues [8-12]. CNTFET has a potential to be the future device of choice and can be scaled further and further. The unique properties of CNTs result in reduced power consumption, high processing speed, thermally efficient dense, highly dense integrated circuits (IC) [13-20]. In this work, we design and simulate a differential amplifier with current source load, employing n-type CNTFETs with 45 nm technology node, with 1V supply. The conventional MOSFETs in the differential amplifier have been replaced by the n-type CNTFETs. Since CNTFET has unique properties in terms of large mobility, large driving capability, very low power consumption, large tensile strength, large thermal conductivity etc. therefore all these advantages are reflected in the proposed CNTFET based current source differential amplifier. The proposed CNTFET based DA has been compared with the conventional MOSFET based current source lead DA. The comparative analyses have displayed a substantial improvement in various performance measuring parameters in the proposed circuitry (CNT based) in comparison to the conventional MOS based circuitry. There is a ~70% reduction in power consumption, 2.7 times enhancement in gain, three orders increase in bandwidth, 1180 times increase in unity gain bandwidth in the proposed CNTFET based DA in comparison to the conventional MOS based DA. The rest of the paper is divided into three sections. In Section II carbon nanotubes are discussed in detail. The results related to the CNT based current source load DA are discussed in Section III. The paper is concluded in Section IV.

II. CARBON NANOTUBES

The Carbon nanotubes were originally named as "buckytubes" and are actually graphene sheets rolled into a tubes. They are being considered as the fourth allotropic form of carbon, after diamond, graphite and coal. CNTs exit in two forms, multiwall and single wall, as shown in Figure 1(a, b). They have unique electrical, mechanical, and optoelectronics properties. Sumio Iijima gets the credit of the discovery of multiwall (MW) CNT in 1991. He and Donald Bethune have independently discovered single wall (SW) CNT in 1993. CNTs are actually graphite sheets which are rolled into cylindrical shapes. They have diameters ranging from <1 nm to 50 nm and length runs into few micrometers (μm). They have huge aspect ratio which is one of the reasons of their unique electrical, mechanical, chemical, thermal and photonic properties. Their thermal conductivity is more than that of diamond and the tensile strength is 100 × more than that of steel. They can maintain a huge current density of the order of 10^9 A/cm^2 with excellent field emission properties. CNTs are capable of showing dual characteristics, metallic and semiconducting,

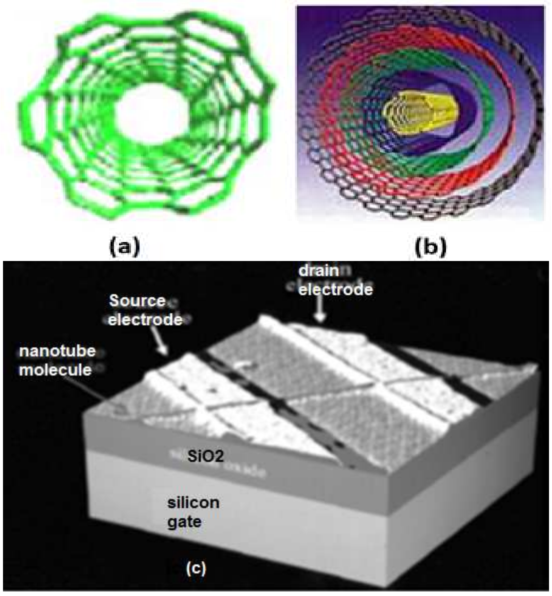


Figure 1: (a) single wall (b) Multiwall CNT (c) CNTFET [3]

depending on their chirality or chirality vector. An important and an impactful application of CNTs is the CNT field effect transistor (CNTFET) realization [1-2]. Dekker Cees et. al. [3] have fabricated the first CNTFET, as shown in Figure 1(c). CNTFET is a promising device and can be used to extend the validity of Gordan Moore's well known law further. It has been found that the intrinsic CNTFET has CV/I characteristics ~13× higher than that of a conventional n-MOSFET. This can be due to the ballistic transport mechanism in CNTs, resulting in reduced effective gate-capacitance (C_G) and large driving-capability. The extraordinary transport properties make CNTFETs promising and desirable candidate for the future integrated circuit technology[18-21]. To demonstrate the CNTFET advantages, digital and analog circuits have been designed using *N* and *P* type CNTFETs. It has been seen that the use of CNTFETs have improved the performance of electronic circuitry, both analog and digital, substantially [3-5, 18-25].

III. CARBON NANOTUBE BASED DIFFERENTIAL AMPLFIER WITH CURRENT SOURCE LOAD

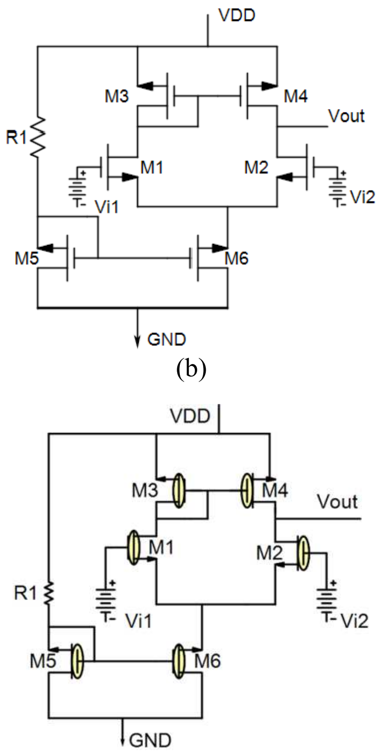
The proposed CNTFET based differential amplifier with current source load (CNT-DA-CSL) is shown in Figure 2(a) and the conventional MOSFET based DA with CSL is shown in Figure 2(b). In the proposed structure, n-type CNTFETs with 45 nm technology node have been used with 1V operating voltage. The simulations have been done by using HSPICE invoking Verilog-A Stanford models CNTFETs. The BSIMv4.6.1 Berkeley Predictive Technology model at 45 nm technology node has been invoked for MOSFETs used in the simulation study [17-20]. Table 1 shows aspect ratio of transistors used simulation study. It is clear that the aspect ratio of all the CNTFETs used is same. It can be attributed to the fact that N and P CNTFETs have the same mobility (both electron and hole) and hence possessing the same driving capability and hence the same aspect ratio (AR). The width of CNTFETs is computed from equation (1) with N=20 and m=19. The aspect ratio of conventional MOSFETs is selected to have the optimum performance for the conventional MOS based DA-CSL.

$$W = (N-1)*S+D_{CNT} \qquad (1).$$

The influence of various parameters of CNTFET like, N, S and D_{CNT} has been rigorously discussed below:

A. Effect of N on the performance of the CNT-DA-CSL.

Figure 3 shows how the performance of the proposed CNT-DA-CSL gets affected by the number of CNT (N). Figure 3(a) shows that as N increases from 5 to 30, the gain initially increases linearly and then saturates. This can be attributed to the increase in current initially and later on the saturation of drain current by the screening effect. The increase in N is equal the increase in the width of CNTFET and hence increases the current. Figure 3(b) shows that the power consumption in the proposed circuit increases substantially with the increase in N. This can be because of the enhancement in ON current (I_{ON}) which increases the power consumption. Figure 3(c) shows that N also changes the bandwidth of the proposed device. Since we have seen that the increase in N enhances the gain of the proposed DA, therefore, the bandwidth (BW) decreases to have Gain-Bandwidth product constant. Further, the use of high dielectric constant gate oxide in CNTFETs increases the gate capacitance and hence reduces the bandwidth. Further, it has been observed that Ro more or less remains constant with the increase in N. Figure 3(d) shows the unity gain frequency (UGF) also decreases with the increase in the number to CNTs, due to increase in overall capacitance with the increase in N.



(a)

Figure 2. (a) Proposed CNTFET based current source load DA. (b) Conventional MOS based current source load DA.

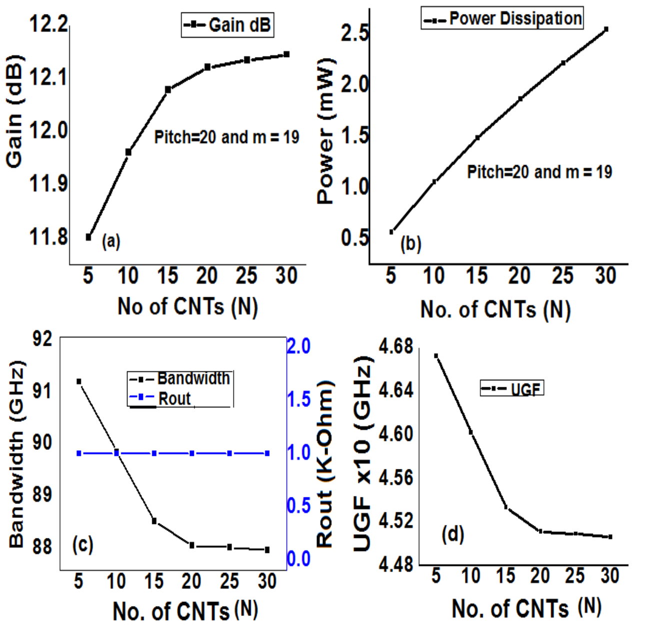


Figure 3: Variation of (a) Current gain (b) Power dissipation (c) Bandwidth and R_{OUT} (d) Unity Gain frequency with N in the proposed CNT-based CSL-DA

B. *Effect of CNT-Pitch (S) on the performance of the proposed CNTFET based CS DA.*

The distance between the centers of two CNTs is the CNT pitch (s). It is an important parameter and needs to be optimized to optimize the performance of the proposed circuit. Figure 4 shows the effect of S on gain, bandwidth, power dissipation and the output resistance of the proposed CNT-DA-CSL. Figure 4(a) shows that DC gain of the proposed circuitry decreases with the increase in S. As S increases, the screening effect between the CNTs increases, which decreases the gain.

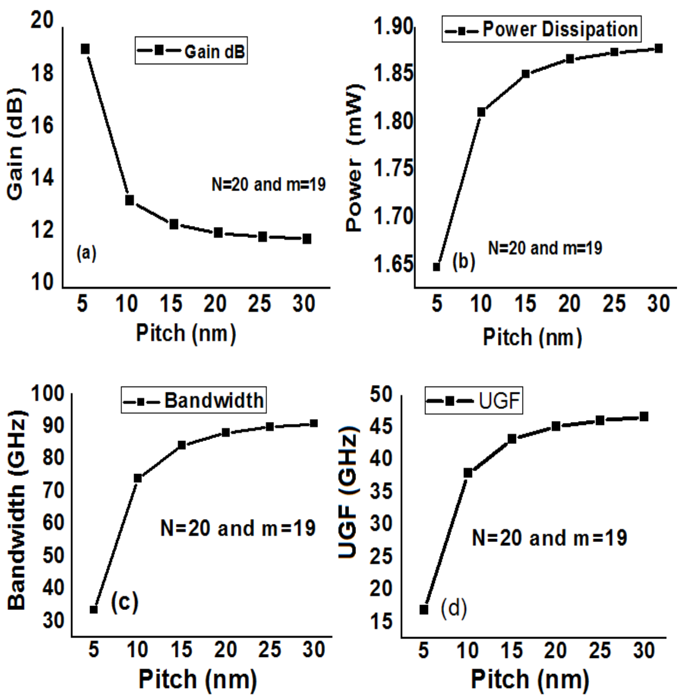


Figure 4: Variation of (a) current gain (b) Power dissipation (c) Bandwidth (d) Unity Gain frequency with respect to pitch of CNT-DA-CSL.

Figure 4(c) shows that the bandwidth of the proposed devices increases with the increase in the pitch. It can be due to the reduction in overall capacitances of circuit and hence increases the bandwidth. Because of the overall capacitance reduction the unity gain frequency (UGF) increases with the increase in pitch, as shown in Figure 4(d). Further, it is clear from Figure 4(b) that the pitch increase also increases the power consumption in the proposed CNT-DA-CSL.

C. *Effect of CNT diameter (D_{CNT}) on the performance of the proposed CNT-DA-CSL*

Like N and S, D_{CNT} is also an important parameter, which needs to be optimized. The diameter of a CNT has a strong effect on improving the performance of proposed CNTFET based CSL-DA. The D_{CNT} directly changes the band gap, as given by equation (2) [17-20].

$$Bandgap = {}^{0.8\,eV}/_{D_{CNT}} \qquad (2)$$

Figure 5(a) shows that the increase in D_{CNT} degrades the DC gain. This can be attributed to the fact that D_{CNT} increase pushes up the screening and scattering effects, which are responsible for the gain degradation. Initially the value of gain is large due to less scattering. Figure 5(b) shows that the power consumption increases with the increase in D_{CNT}. This can be due to the increase in transconductance, which increases the drive capability and hence the power consumption. Further, D_{CNT} increase reduces the band gap, which in turn increases the leakage and hence the static power dissipation. Further, the increase in D_{CNT}, decreases the bandgap as per equation (I), which increases transconductance and hence the drain current. The ultimate effect is the increase in and increases the bandwidth and UGF as shown in figure 5(c) and (d).

Table 2 compares the performance of the conventional CSL-DA and the proposed CNTFET based CSL-DA. It clearly shows that the CNT based proposed circuitry significantly outperforms the conventional one in each and every parameter. The performance enhancement in the proposed circuitry can be attributed the unique parameters of the CNTs and CNTFETs used.

Table-I Aspect ratio for transistors (MOSFETs and CNTFETs)

Transistor	W/L (MOS)	W/L(CNTFET)
M1,M2	0.25µm/45nm	0.38µm/45nm
M3,M4,M5,M6	10 µm/0.25 µm	0.38µm/45nm

Table-II Comparative Analysis of performance measuring parameters of the proposed and the conventional DAs.

Performance Parameter	CMOS- DA-CSL	CNT-DA-CSL
Gain(dB)	3.26	12.1
3-db Bandwidth	74MHz	88GHz
Unity Gain Bandwidth	38.3MHz	45.2GHz
Output Resistance	13.81K Ω	1K Ω
Power Dissipation	2.56mW	1.8 mW

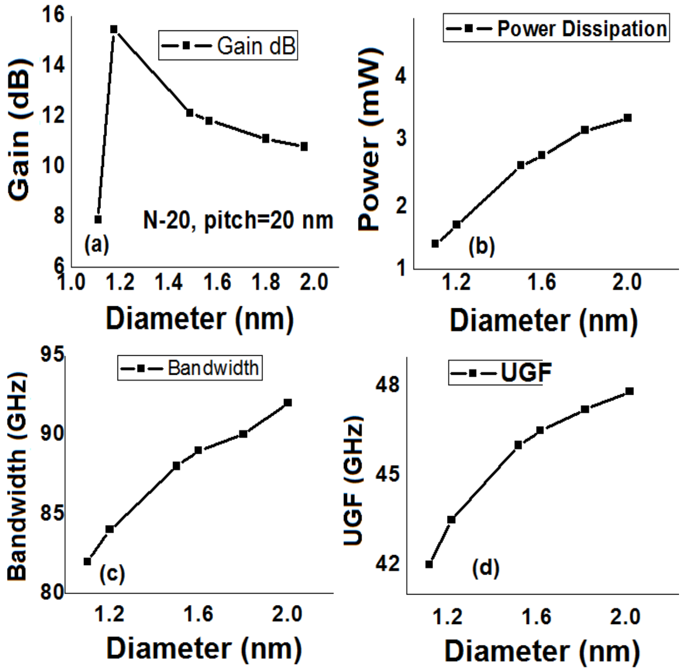


Figure 5: Variation of (a) Gain (b) Power dissipation (c) Bandwidth (d) Unity Gain frequency with respect to diameter of CNT-DA-CSL.

IV. Conclusion

In this work, CNTFET based current source load differential amplifier has been designed and simulated using HSPICE. Here 45 nm technology node based n-CNTFETs have been used in designing the CNT-DA-CSL. Since differential amplifier is an important part of an operational amplifier and provides the input and gain to the OP-AMP, therefore, current source load differential amplifier is preferred, as it provides high gain. Since CNTFETs are unique and results in high speed, reduced power consumption, high packing density etc, therefore, in the proposed circuitry CNTFETs have been used instead of the conventional MOSFETs. It has been observed that the proposed CNTFET based differential amplifier has got improved gain, bandwidth, unity gain bandwidth frequency and significantly reduced power consumption. Further, it has been observed that by optimizing N, S and DCNT, the performance of the proposed CNT-DA-CSL can be improved further.

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