Design and Fabrication of Single-chip Carbon Nanotubes Vacuum Field Emission Differential Amplifier

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Even though decades of research and development on vacuum microelectronics has *not* achieved the technology to perform at circuit level, recent developments with diamond [1] and carbon nanotubes (CNTs) [2,3] vacuum transistors, with high gain and stable emission current, has indicated the potential of these devices in integrated circuit form. In this paper, the design and fabrication of a single chip CNT vacuum field emission differential amplifier (VFE diff-amp) is presented for the first time. The differential amplifier is the most widely used circuit building block in integrated circuits. The implementation of a vacuum field emission transistor in the differential amplifier configuration will promote the development of VFE ultra-high-speed integrated circuits, logic gates and systems. Moreover, the VFE diff-amp will be valuable for applications requiring temperature-immunity and radiation-hardness such as advanced telecommunication, military and space electronics. In this study, a dual-mask microfabrication process is employed to achieve the single-chip VFE diff-amp that integrates two identical VFE transistors with built-in split gates and integrated anodes.

In the fabrication process, the first mask defines and patterns the self-aligned gate with minimum gate capacitance for high frequency operation, as shown in Fig. 1. The next mask is used to align and pattern the microcathode array within the gate area. In both cases, the a-Si gate electrode is dry-etched by a gas mixture of SF_6/O_2 in a reactive-ion-etch (RIE) system. A SEM picture of the CNTs VFE diff-amp after gate patterning and microcathodes alignment is shown in Fig. 2(a). Following wet-etch of the thermal oxide, a thin film of titanium (as a diffusion barrier layer) and nickel (as the CNT growth catalyst) are sputter-deposited in sequence on the VFE diff-amp pattern. The surplus catalyst on the gate-electrode is then removed by photoresist lift-off technique and subsequently selective growth of vertically aligned CNTs by microwave plasma chemical vapor deposition (MPCVD) is performed. A portion of a microcathode array with self-aligned gate with 4μm gate aperture is illustrated in Fig. 2(b). During the growth process, a critical plasma pretreatment technique is applied to synthesize gated CNT microcathodes with a convex-shaped surface profile, Fig. 2(c). This surface profile is important in preventing cathode-gate leakage without resorting to more complicated fabrication processes such as a sidewall protector [4-7] or gate over-etching method [2,8] that result in higher turn-on voltage. Per simulation [9,10], CNT microcathode with convex surface profile has more quasi-uniform electric fields on CNT tips than one with uniform CNT height. As a result, the microcathodes with a convex surface profile are more capable of delivering higher emission current density.

We demonstrated recently an aligned CNT triode amplifier in a common emitter configuration capable of delivering large *DC* gain, amplification factor (~352) and low gate turn-on voltage, ~25 V [3]. In these single-ended amplifiers, however, the bias point, gain and impedance are sensitive to device parameters and noises. Beside low noise and low distortion, the major benefit of the VFE diff-amp is that it amplifies the difference between two input signals and rejects the components common to both signals. Thus, an important figure-of-merit of the VFE diff-amp is the common-mode rejection ratio (CMRR) given by the ratio of the differential mode gain to the common mode gain. CMRR determines the capability of the diff-amp in rejecting noise that is common to both inputs. A schematic diagram of the CNTs VFE diff-amp test circuit is shown in Fig. 3. Detailed design issues, fabrication results and device characteristics will be presented in this paper.

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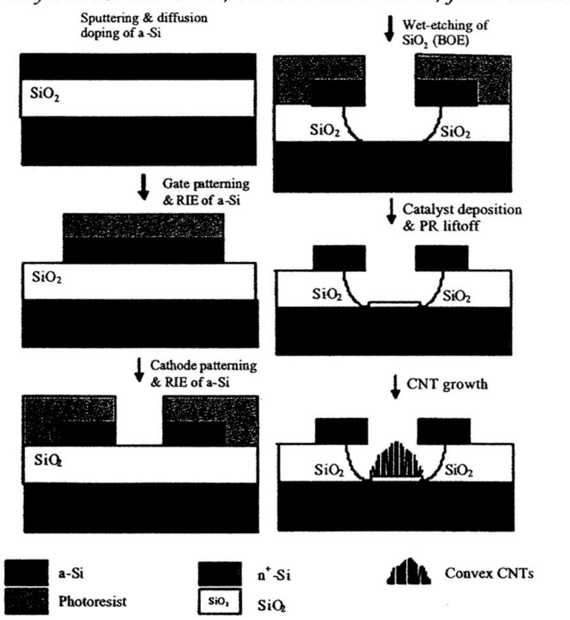

Fig. 1: Schematic diagram of the fabrication process flow of the CNT field emission differential amplifier

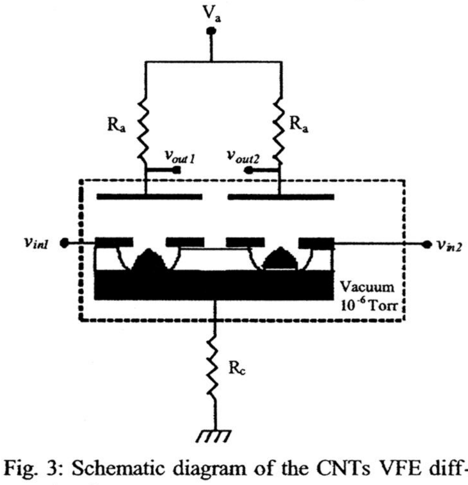

Fig. 3: Schematic diagram of the CNTs VFE diff-amp test circuit.

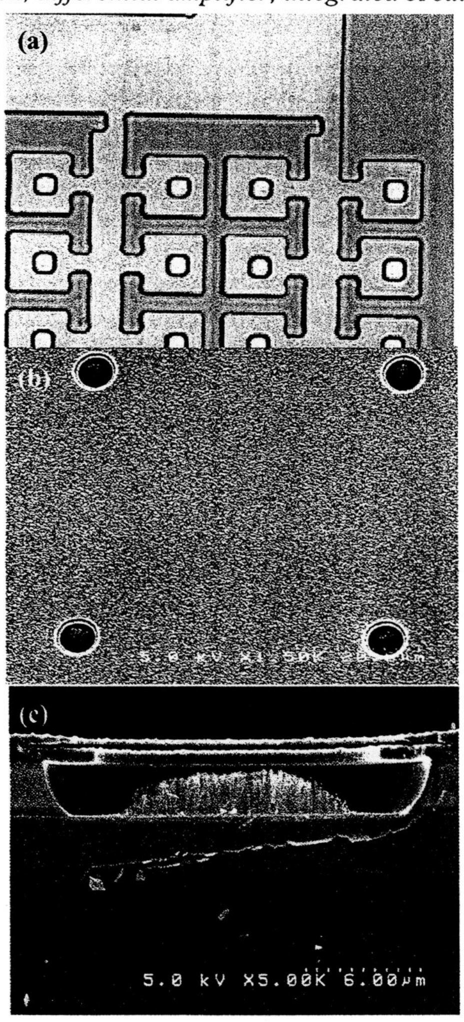

Fig. 2: (a) SEM of the CNTs VFE diff-amp with patterned gate and aligned microcathode array. (b) SEM of a portion of the vertically aligned gated CNT array, and (c) cross-sectional view of a gated CNTs microcathode with convex-shaped surface profile.