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Sandip B. Rahane
Matoshri College of Engineering and Research Center Nasik,
S.P.P.U., Pune, India
rahanesandip@gmail.com

A.K. Kureshi
Vishwabharati Academy's College of Engineering, Ahemadnagar,
S.P.P.U., Pune, India
akkureshi@rediffmail.com

S.D. Pable
Matoshri College of Engineering and Research Center Nasik,
S.P.P.U., Pune, India
sachinp_79@yahoo.co.in

***Abstract*—This paper proposes a novel hybrid CMOS-CNFET bandgap reference circuit consisting of a CMOS bandgap core and a CNFET error amplifier. Both CMOS and CNFET circuits are based on 32nm technology node. Resulting hybrid topology utilizes resistive subdivision method and low threshold CNFET devices to lower the common mode input voltage of the error amplifier. The proposed bandgap reference achieves temperature coefficient of 6.8 ppm/°C at 1.4V power supply over the temperature range of -25°C to 125°C. The circuit produces a reference voltage of around 500mV with line sensitivity of ±2.25mV/V and dissipates 26µW power.**

Keywords—Hybrid nanoelectronics; bandgap reference; carbon nanotube field effect transistor.

I. INTRODUCTION

Reference voltage sources are circuits that should provide voltage signal that is insensitive to temperature and power supply variations, possess good thermal stability and high power-supply rejection. Bandgap reference circuit is the one which satisfy this requirement and hence is an essential component required in many analog, digital and mixed-signal systems such as voltage regulators, ADC's, DAC's, radio frequency (RF) systems and data acquisition systems [1-3]. Most of the traditional bandgap references rely on long channel designs to reduce the impact of temperature and process variations. This is because scaling does not provide significant benefits in analog circuit designs such as bandgap references due to non-idealities such as short channel effects and gate leakage [4-5]. Therefore with the aggressive scaling, it has become more difficult to design precise bandgap references in nanometer regime. In this paper we propose a hybrid bandgap reference in a 32nm technology node incorporating a CMOS bandgap circuit with a CNFET based error amplifier.

This paper is organized as follows. Section II takes a review of various CMOS-CNFET hybrid implementations. Proposed hybrid bandgap reference circuit is described in Section III. HSPICE simulation results are discussed in Section IV and the conclusion is given in Section V.

The first prototype system for a silicon bandgap reference voltage source was proposed by Hilbiber in [6]. He proposed a technique that compensated first order temperature dependence of the base to emitter voltage with a simple circuit that used two different types of diodes. Widlar et al. [7] proposed a new topology of the bandgap reference. This circuit required lower supply voltage and used a technique that adds base to emitter voltage with a differential base to emitter voltage of two transistors possessing different current densities. Kuijk et al.[8] developed bandgap reference which used same principle as that of [6]. In his circuit output voltages, other than the bandgap voltage, could also be realized. Brokaw et. al. [9] presented a bandgap reference which, combined methods reported in [6] and [7]. A switched capacitor bandgap reference employing curvature correction was proposed by Song et.al. [10]. Vittoz et. al. [11] published a CMOS bandgap reference. Banba et.al. [12] proposed a sub 1-V CMOS bandgap reference circuit, with minimum supply voltage of 0.84V. Leung et. al. in [13] proposed a modified version of the Banba reference[12]. This circuit uses pMOS input stage in the error amplifier and the inputs of the error amplifier are received after resistive division. The curvature problem in the bandgap reference can be dealt with different curvature compensation techniques as reported in [1-4].

II. HYBRID NANOELECTRONICS

Several researchers have proposed circuits using hybridization of conventional CMOS with emerging nanoelectronic devices such as CNFETs. A hybrid technology demonstrating three dimensional integration of CMOS and CNFET device for a simple hybrid CMOS-CNFET inverter is reported by Meric et.al. [14]. Usmani et al. [15] presented performance optimization of a hybrid CMOS-CNFET inverting amplifier and compared the proposed hybrid circuit performance with that of a planar CMOS inverting amplifier. The first RF circuit with nMOS-pCNFET co-integration for a cascode amplifier was demonstrated by Stanford researchers in [16]. A hybrid cascode configuration is obtained by utilizing both CMOS and CNFET on the same chip. Application of CNT-CMOS hybrid system for chemical sensing is reported in [17]. A power gating scheme with CNFETs as sleep transistors for a conventional CMOS logic cell was proposed by Kim et al. [18]. Zhou in [19] describes a hybrid FPGA design using carbon nanotube based nano electromechanical (NEM) switches as a replacement for SRAM cells in look up tables. Chakraborty et. al.[20] proposed

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a leakage control scheme utilizing CNT-based nano-electromechanical switch for conventional CMOS logic and memory circuits.

Though, CNFETS are proposed as an alternative to silicon MOSFET by the different researchers, but in near future it is very difficult to replace the CMOS technology because of research advancement and economic impact of CMOS based devices [17]. One of the developments in this direction is hybrid nano-electronics wherein CNFET technology can be combined with proven CMOS technology. The resulting hybrid CMOS-CNFET circuits can form the basis of variety of circuits and systems. [15-18].The proposed bandgap reference achieves hybridization of CMOS with emerging CNFET technology in complementary manner.

III. PROPOSED HYBRID BANDGAP REFERENCE CIRCUIT

Fig. 1 shows proposed bandgap reference which uses hybridization of conventional CMOS technology with carbon nanotube field effect transistors (CNFETs).The basic bandgap itself is a kind of hybrid circuit wherein parasitic BJTs are used out of CMOS technology. The proposed reference uses three conventional PMOS transistors, parasitic BJTs and error amplifier which is a differential amplifier utilizing CNFETs.

Bandgap reference works on a principal of cancelling the negative temperature dependence of a p-n Junction with a positive temperature dependence circuit [8, 13]. The voltage across the base emitter V_{BE} of bipolar junction transistor (BJT) has a negative temperature coefficient of about $-2mV/^{0}C$. The thermal voltage V_T has a positive temperature coefficient of $0.086mV/^{0}C$ is multiplied by a constant, which is proportional to absolute temperature. Since p-n junction V_{BE} decreases approximately linear with temperature while V_T increases linearly with temperature. A temperature independent reference can be obtained by multiplying V_T by a constant and summing it with V_{BE}. This concept can be realized with the current mode bandgap reference circuit [13] as shown in Fig 1. The voltages at nodes A and B are forced to be equal and are given by equation (1). The reference voltage V_{ref} across the resistor R_3 is given by equation (2).

$$V_A = V_B = \left(\frac{R_2}{R_1+R_2}\right) V_{Q1} \quad (1)$$

$$Vref = \left[\frac{R_3}{R_1+R_2}\right]\left[\left(\frac{R_1+R_2}{R}\right)\ln(K)\, V_T + V_{Q1}\right] \quad (2)$$

The term V_{Q1} (V_{BE} of the transistor) in the equation (2) has a negative temperature coefficient, the second term $ln(K)\ V_T$ has a positive temperature coefficient. The K=8 is found to be optimum for our hybrid circuit. A reference voltage with theoretically zero temperature coefficient can thus be obtained by selecting proper value for the resistor ratio. The optimum value of resistor ratio is obtained by choosing R_1=150KΩ, R_2=320KΩ, R_3=165KΩ and R=40KΩ. Equally sized PMOS devices (W/L=10) operating in saturation region with their gates tied together results in a current mirror connection. Since the currents flowing through all the three PMOS devices are equal and are temperature independent, reference voltage (V_{ref}) across the resistance is also temperature independent.

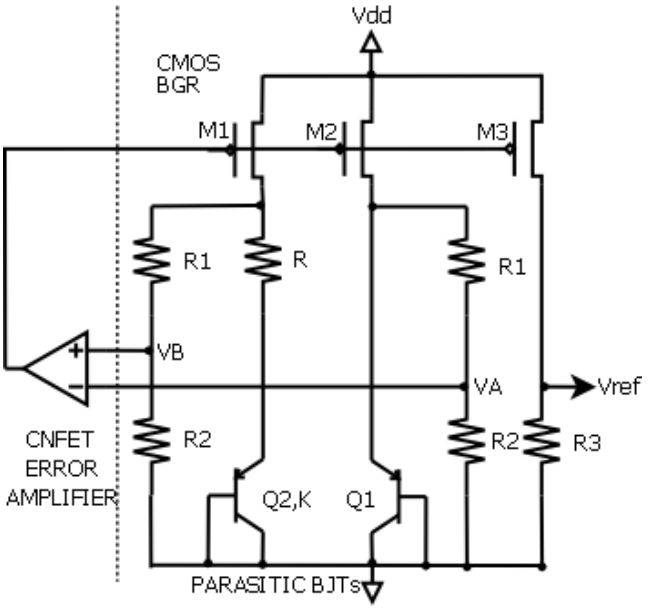

Fig. 1. Proposed CMOS-CNFET hybrid bandgap reference

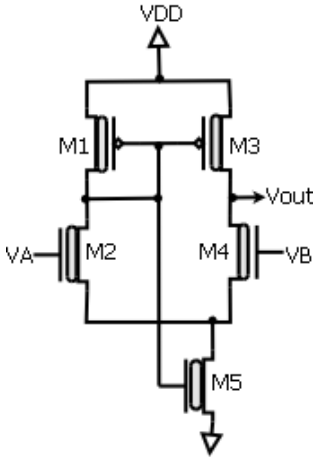

Fig. 2. CNFET based error amplifier used in bandgap reference circuit

The Fig. 2 shows the CNFET based error amplifier used in the bandgap reference. This circuit is a differential amplifier and does not need separate biasing circuit to set the currents. The two voltage dividers in the bandgap core provides the differential input between input nodes V_A and V_B. Ideally V_A is supposed to be equal to V_B, but practically there is always a mismatch and $V_A \neq V_B$. The difference V_A-V_B called as error voltage is amplified by the error amplifier. This error amplifier must satisfy a condition that its common mode input voltage should not fall below a voltage drop across a single diode. This can be achieved using low-threshold devices as reported in [12] and with transistors in weak inversion [21], as well as with BiCMOS technologies [22]. This work presents a resistive division method to lower the common mode input voltage of the error amplifier which uses low threshold CNFETs. CNFETs with tube chirality (19,0) , number of tubes=3 have been used.

IV. SIMULATION RESULTS

The HSPICE simulations are carried out to determine performance metrics of the voltage reference such as line sensitivity, temperature coefficient and power supply rejection ratio (PSRR). A wide temperature variation between -25^{0}C to 125^{0}C and VDD sweep of 0 to 2V is chosen. Stanford University carbon nanotube field effect transistors (CNFET) HSPICE model [23] is used to simulate the proposed hybrid circuit.

A. Power Supply Dependence(Line Sensitivity)

Fig. 3 shows reference voltage variation, as the supply voltage is swept between 0V to 2.0V. The legends show different operating temperatures at which simulation is carried out. Fig. 4 depicts a close-up/magnified view for supply voltage between 1.2V to 1.6V. Simulation results shows that the reference has got excellent temperature independence for the Vdd around 1.4V. Mean reference voltage is about 500.5mV and changes by +1mV to -2.7mV when Vdd is varied from 1.1V to 1.6V.The line sensitivity achieved by the reference is ±2.25mV/V.

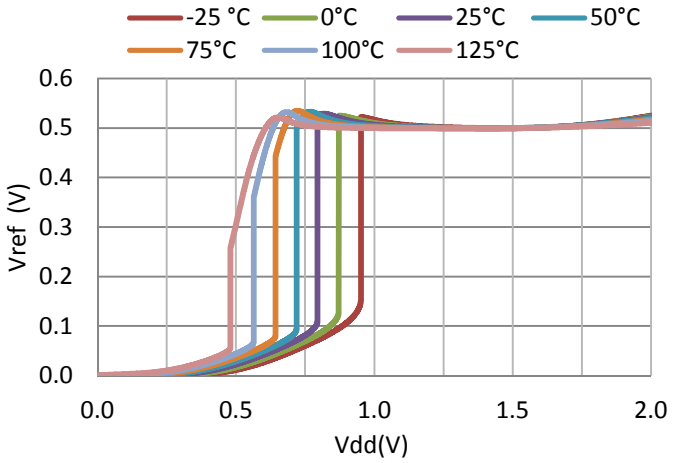

Fig. 3. Reference voltage variation for Vdd sweep of 0V to 2.0V

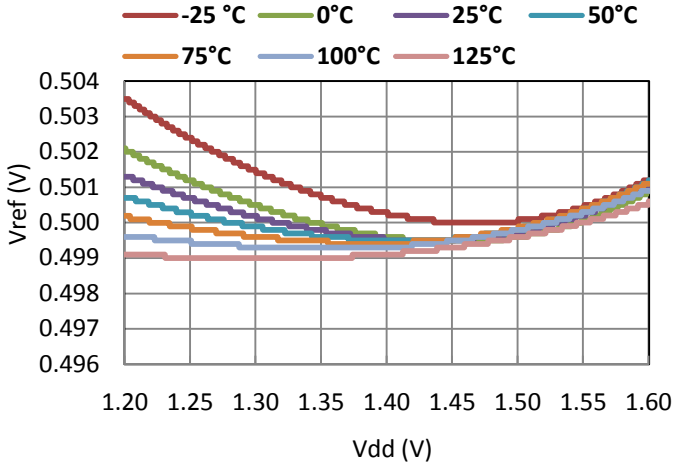

Fig. 4. A close-up/magnified view for variation in reference voltage for Vdd between 1.2 V to 1.6 V

B. Temperature Dependence of the Bandgap Reference

A true temperature independent reference cancels a positive temperature coefficient with a negative temperature coefficient. Bandgap reference circuit generates voltage that is linear function of temperature, and voltage that is complementary to absolute temperature which is nonlinear because of inherent nonlinearity in a pn junction diode. Therefore a linear voltage can't be perfectly cancelled by the nonlinear voltage. This causes a curvature in the bandgap voltage and is called curvature problem [3-4]. Fig. 4 which shows a close-up view for V_{DD} between 1.2V to 1.6V depicts such curvature. Temperature dependence of the bandgap reference for different supply voltages is shown in Fig. 5. The temperature coefficient achieved by our circuit is 6.8 ppm/°C at supply voltage of 1.4V and 5.3ppm/°C at 1.5V. A temperature coefficient is 8ppm/°C for 1.6V and degrades to 33ppm/°C for 1.3V.

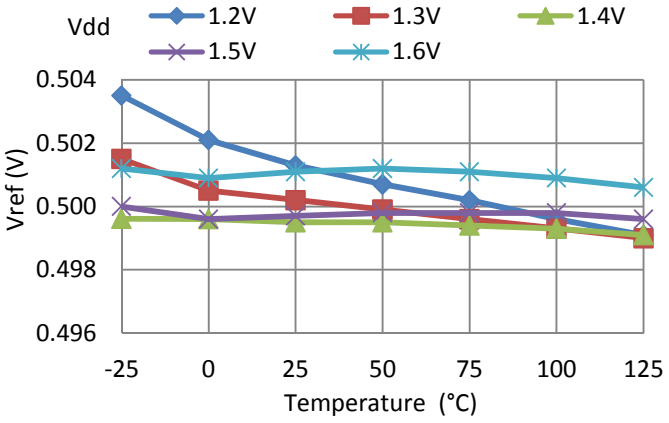

Fig. 5 Temperature dependence of the bandgap reference

C. Power Supply Rejection Ratio (PSRR)

Apart from good temperature independence it is also expected that a bandgap reference circuit provides high power supply rejection ratio (PSRR) over a wide frequency range. A high PSRR ensures the ability to reject noise. The PSSR performance of the bandgap reference is shown in Fig. 6. The circuit exhibits a PSRR of -44dB at 10 KHz frequency , 25^o C temperature and for Vdd of 1.4V. Similarly PSRR is of -38dB at 10MHz frequency.

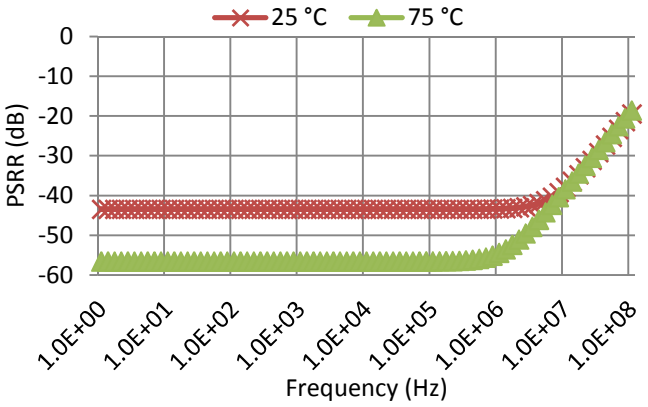

Fig. 6. PSRR at 25ºC and 75ºC, Vdd=1.4V

D. Stability Analysis

Fig. 7 and Fig. 8 show transient analysis of the proposed circuit. The output voltage settles to 500mV within 240nS with maximum overshoot of 7mV at 25°C.

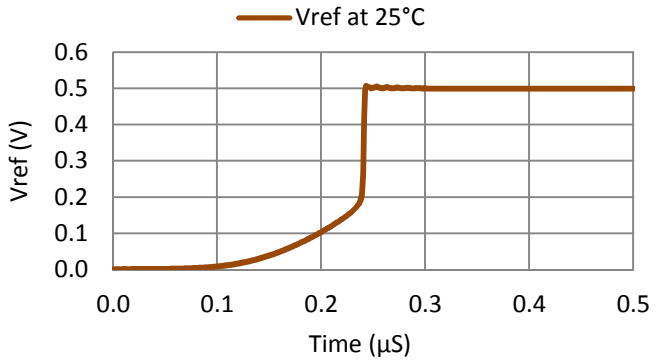

Fig. 7. Stability / Transient analysis

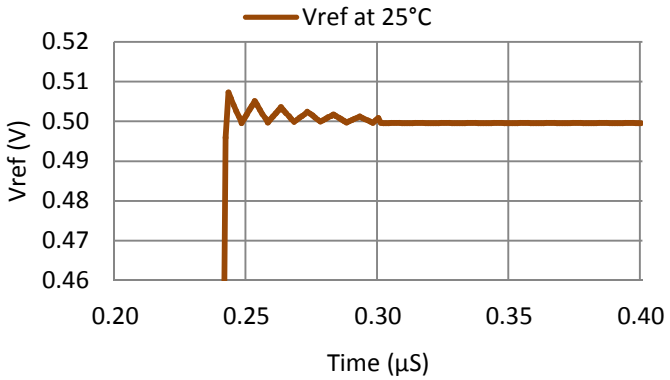

Fig. 8. A close-up of transient analysis

V. CONCLUSION

Hybrid CMOS-CNFET bandgap reference has been presented in this paper. The hybrid approach utilizing proven CMOS technology with an emerging CNFET technology in a complementary manner is proposed with HSPICE simulations. The simulation results confirm robustness of the reference for variations in temperature and power supply. A precision bandgap reference with a nominal output of 500mV, 6.8 ppm/°C temperature coefficient, ±2.25mV/V line sensitivity and 26µW power dissipation is presented. The circuit exhibits stable operation without compensating capacitors with a startup time of 240nS at 25°C. A PSRR of -44dB is achieved at 25°C for 1.4V power supply. A satisfactory 6.8 ppm/°C temperature coefficient is achieved without any special curvature compensation.

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