

Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI

Gage Hills, Marie Garcia Bardon, Gerben Doornbos, Dmitry Yakimets, Pieter Schuddinck, Rogier Baert, Doyoung Jang, Luca Mattii, Syed Muhammed Yasser Sherazi, Dimitrios Rodopoulos, Romain Ritzenhaler, Chi-Shuen Lee, Aaron Voon-Yew Thean, Iuliana Radu, Alessio Spessot, Peter Debacker, Francky Catthoor, Praveen Raghavan, Max M. Shulaker, H.-S. Philip Wong, and Subhasish Mitra

Abstract—Carbon Nanotube Field-Effect Transistors (CNFETs) are highly promising to improve the energy efficiency of digital logic circuits. Here, we quantify the Very-Large-Scale Integrated (VLSI) circuit-level energy efficiency of CNFETs vs. advanced technology options (ATOs) currently under consideration (e.g., silicon-germanium (SiGe) channels and progressing from today’s FinFETs to gate-all-around nanowires/nanosheets). We use industry-practice physical designs of digital VLSI processor cores in future technology nodes with millions of transistors (including effects from parasitics and interconnect wires) and technology parameters extracted from experimental data. Our analysis shows that CNFETs are projected to offer 9 \times energy-delay product (EDP) benefit (~3 \times faster while simultaneously consuming ~3 \times less energy) compared to Si/SiGe FinFET. The ATOs provide <50% EDP benefits. All analyses are performed at the same off-state leakage current density (≤ 100 nA per micron of FET width) and power density (≤ 100 Watts per cm^2 of chip area). This analysis provides insights into the sources of CNFET EDP benefits and addresses key questions for deeply-scaled technologies. For instance, while contact resistance is a concern for sub-10 nm nodes, CNFETs still provide up to 6.0 \times EDP benefit (vs. Si/SiGe FinFETs) using CNFET contact resistance values already experimentally achieved for 9 nm contact length.

Index Terms—Carbon nanotube (CNT), carbon nanotube field-effect transistor (CNFET), energy-efficient digital very-large-scale integrated (VLSI) circuits.

I. INTRODUCTION

To enable significant improvement in energy efficiency for digital logic circuits (EDP is a widely-used metric [1]), multiple potential technology options are being explored. For example, CNFETs promise to improve energy efficiency of digital VLSI circuits. Experimental demonstrations have shown high-performance / energy-efficient CNFETs [2], [3], [4], [5], and CNFET-based processors and nanosystems [6],

G. Hills, C.-S. Lee, H.-S. P. Wong, and S. Mitra are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (email: ghills@alumni.stanford.edu).

M. Garcia Bardon, D. Yakimets, P. Schuddinck, D. Jang, Y. Sherazi, D. Rodopoulos, R. Ritzenhaler, I. Radu, A. Spessot, P. Debacker, F. Catthoor, and P. Raghavan are with imec, Leuven, Belgium.

G. Doornbos is with the Exploratory Transistor Program, Taiwan Semiconductor Manufacturing Company, Leuven 3001, Belgium.

L. Matti is with Cadence, Leuven 3001, Belgium.

A. Thean is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore.

M. M. Shulaker is with the Department of Electrical Engineering, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

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[7]. Previous publications on CNFET EDP benefits relied on at least one of: simplified transistor models (e.g., fixed on-current (I_{ON}) and off-current (I_{OFF}) for fixed technology parameters such as fixed gate length (L_G)), simplified circuit models (e.g., no parasitics from physical layouts), and small circuit blocks (e.g., adder) [4], [8], [9] that may not capture effects of long wires. Detailed analysis accounting for important effects present in realistic VLSI circuits (e.g., wire parasitics, routing congestion, timing constraints for sequential logic) is required. Also, by fixing key parameters across technologies (e.g., L_G , I_{OFF} , supply voltage: V_{DD}), previous publications (e.g., [3], [4]) did not exploit technology-specific optimization of these parameters.

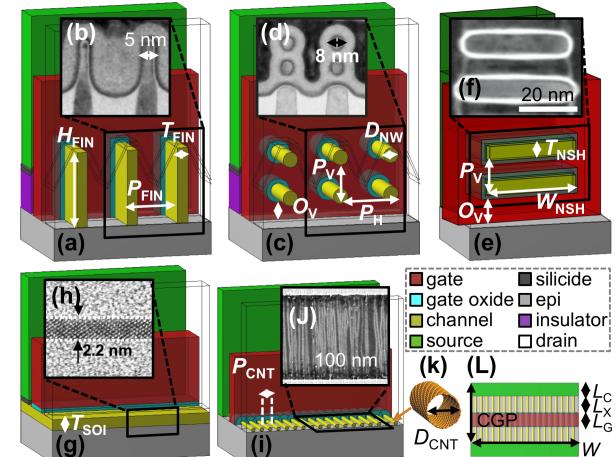


Fig. 1. FET technology candidates. (a) FinFET (side view through a transparent drain) with multiple fins (pitch: P_{FIN} , height: H_{FIN} , thickness: T_{FIN}). (b) Cross-section transmission electron microscope (TEM) image of FinFET channel [10]. (c) Nanowire (NW) FET (NWFET) with multiple NWs (horizontal pitch: P_h , vertical pitch: P_v , vertical offset: O_v). (d) Cross-section TEM of NWFET channel (NW diameter: D_{NW}) [11]. (e) Nanosheet (NShFET) with multiple nanosheets (thickness: T_{NSH} , width: W_{NSH} , vertical pitch: P_v , vertical offset: O_v). (f) Cross-section TEM of NShFET channel [12]. (g) Extremely-thin silicon-on-insulator (ETSOI). (h) Cross-section TEM of silicon channel (thickness: T_{SOI}) [13]. (i) CNFET with multiple parallel CNTs (CNT pitch: P_{CNT}). (j) Scanning electron microscope (SEM) image of CNFET channel (top view) [5]. (k) CNT (diameter: D_{CNT}). (l) top-view FET schematic (shown for CNFET), indicating width: W , gate length: L_G , source/drain contact length: L_C , extension region length: L_X , contacted gate pitch: $CGP = L_G + L_C + 2L_X$.

Here, we present the first EDP comparison of various promising technology candidates (Fig. 1) for future technology nodes, using physical designs of VLSI processor cores (additional technology options include negative capacitance effects of ferroelectric materials in FET gate stacks [14]; these can potentially be combined with the technology candidates in Fig. 1 to achieve additional EDP benefits [15]). We leverage industry-practice VLSI designs

and design flows, and technology parameters calibrated to experimental data (details of our methodology are in the Appendix) to: 1) quantify the EDP benefits of each technology (Sec. II), and 2) provide insight into the sources of CNFET benefits (Sec. III). We also address several key questions for deeply-scaled technologies (Sec. IV).

In the following sections, we analyze digital circuits with realistic process assumptions for two future sub-10 nm technology nodes. Table I and II present technology details and transistor performance metrics for what we will hereafter label as “7 nm node” and “5 nm node”, respectively [16].

II. RESULTS: ENERGY EFFICIENCY COMPARISONS

A. Results: 7 nm Technology Node

Fig. 2 quantifies the speed and energy of the processor core of OpenSPARC T2 (7 nm node), a large multi-core chip that closely resembles the commercial Oracle/SUN Niagara 2 [17] (results for a 32-bit commercial processor core at the 5 nm node are shown in Fig. 3). 7 nm node technology details and FET performance metrics are summarized in Table I (5 nm node details in Table II). For CNFETs and ATOs, we analyze technologies calibrated to experimental data [3], [10], [18], [19], [20], [21], [22], [23], [24], [25], [26] (referred to as *experimental* technologies), and also *projected* technologies, which exceed the best experimental results to-date (while adhering to physical limits, e.g., for contact resistance [27]; details in Table I and Table II). Projected technologies explore potential EDP benefits beyond what can be achieved today.

- 1) Experimental Si/SiGe nanowire FET (NWFET) offers <30% EDP benefit vs. experimental Si/SiGe FinFET, projected Si/SiGe NWFET offers <40% EDP benefit vs. experimental Si/SiGe FinFET, and projected Si/SiGe FinFET offers <50% EDP benefit vs. experimental Si/SiGe FinFET.
- 2) Projected CNFET offers 9.0× benefit vs. experimental Si/SiGe FinFET: 3.0× faster clock frequency while simultaneously consuming 3.0× less energy per clock cycle; these EDP-optimal designs for projected CNFET and experimental Si/SiGe FinFET have the same I_{OFF} density (100 nA/ μ m: typical for high-performance/low threshold voltage technology options [28]) and power density (\sim 65 W/cm 2 , which satisfies the \leq 100 W/cm 2 constraint [28]).
- 3) Experimental CNFET – with carbon nanotube (CNT)-metal contact resistance $R_C = 18.25$ k Ω /CNT (at each source/drain contact), experimentally demonstrated for PMOS CNFETs with 9 nm contact length (L_C) [29] – offers 5.6× EDP benefit vs. experimental Si/SiGe FinFET. Projected CNFET 9.0× EDP benefit is for $R_C = 3.25$ k Ω /CNT (the projected physical limit for contact resistance to a one-dimensional quasi-ballistic nanotube/nanowire for a single sub-band [27], which has been approached experimentally for $L_C > 9$ nm [18]). Note that, $R_C < 3.25$ k Ω /CNT may also be achieved by accessing multiple sub-bands, e.g., with future advances in contact doping^{*}). CNT pitch (P_{CNT}) of 4 nm [30] is used for both experimental and projected CNFET ($P_{CNT} < 2$ nm has been achieved experimentally in [31]).

* In this limit, $R_C = R_Q = h/2n_Ve^2$, where R_Q : the resistance quantum, h : Planck's constant, e : electron's charge, n_V : band degeneracy [27].

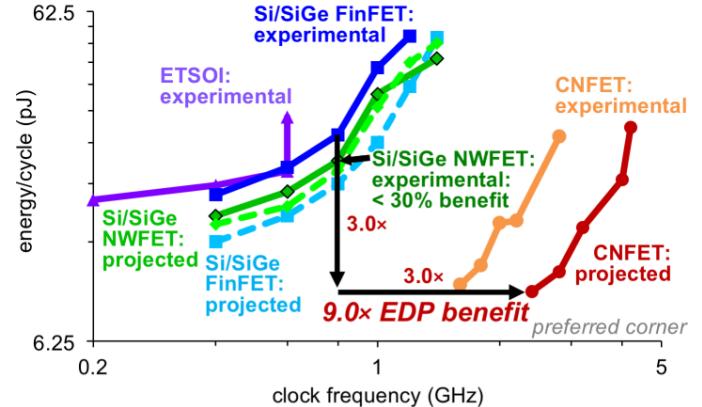


Fig. 2. OpenSPARC T2 processor core energy vs. clock frequency across FET technologies: 7 nm node. Projected CNFET offers 9.0× EDP benefit vs. experimental Si/SiGe FinFET for the same I_{OFF} density (100 nA/ μ m) and power density (\sim 65 W/cm 2); experimental Si/SiGe NWFET offers <30% EDP benefit.

B. Results: 5 nm Technology Node

Fig. 3 quantifies the speed and energy of a 32-bit commercial processor core at the 5 nm node, for both experimental and projected technologies. FET parameters are in Table II.

- 1) Projected Si/SiGe FinFET offers <20% EDP benefit vs. experimental Si/SiGe FinFET, and projected Si/SiGe Nanosheet FET (NShFET) offers <50% EDP benefit vs. experimental Si/SiGe FinFET.
- 2) Projected CNFET offers 9.3× EDP benefit vs. experimental Si/SiGe FinFET: 3.1× faster clock frequency while simultaneously consuming 3.0× less energy per clock cycle; the same constraints described for the 7 nm node results are also satisfied (i.e., I_{OFF} density \leq 100 nA/ μ m and power density \leq 100 W/cm 2).
- 3) Experimental CNFET (with $R_C = 18.25$ k Ω /CNT) offers 6.0× EDP benefit vs. experimental Si/SiGe FinFET (projected CNFET 9.3× EDP benefit is for $R_C = 3.25$ k Ω /CNT: Table II).

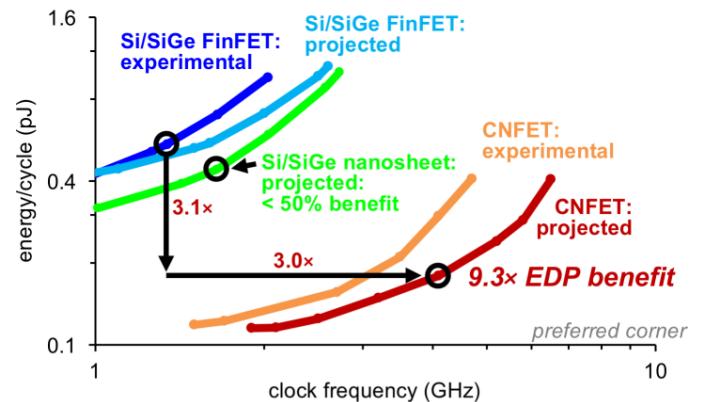


Fig. 3. 32-bit commercial processor core energy vs. clock frequency results across FET technologies: 5 nm node. Projected CNFET offers 9.3× EDP benefit vs. experimental Si/SiGe FinFET for the same I_{OFF} density and power density constraints (I_{OFF} density \leq 100 nA/ μ m, power density \leq 100 W/cm 2); projected Si/SiGe NShFET offers <50% EDP benefit. Note that, the energy and clock frequency values for the 32-bit commercial processor core here are not related the energy and clock frequency values for the OpenSPARC T2 processor core in Fig. 2, since the architectures of the two processor cores are distinct (in particular, the 32-bit commercial processor core here comprises \sim 30× fewer logic gates, contributing to smaller energy per cycle).

III. CNFET ENERGY EFFICIENCY BENEFITS

To quantify key CNFET EDP that enable energy-efficient digital VLSI logic circuits, a useful metric is the electrostatic scale length (λ) [32], which quantifies how susceptible a FET is to short-channel effects [33]; it should be small to enable shorter L_G (thus improving gate capacitance: C_G) without degrading sub-threshold slope (SS). Two approaches for reducing λ are: 1) improve FET geometry (e.g., from top-gate to gate-all-around (GAA)), and 2) reduce the semiconductor body thickness (T_{BODY}). While evolving from planar Si FET to 3D FinFET to GAA NWFET reduces λ (Fig. 4a), continued significant λ reduction requires reducing T_{BODY} . However, for bulk materials (e.g., all Si-, Ge-, and III-V-based semiconductors), carrier transport severely degrades as T_{BODY} scales to sub-10 nm dimensions [10], [19], [20], [21], [24], [25] (Fig. 4b) due to enhanced phonon and surface roughness scattering, resulting in degraded effective drive current (I_{EFF}).

Here is the key advantage of CNFET: CNTs inherently maintain superior carrier transport even at very thin (~1-2 nm) T_{BODY} (experimental hole mobility: $>2,500 \text{ cm}^2/\text{V.s}$ [26]), and experimental hole virtual source velocity $v_{X0} = 4.1 \times 10^7 \text{ cm/s}$ [22], for $D_{CNT} < 2 \text{ nm}$). In contrast, experimental Si FinFET demonstrations with $T_{BODY} < 3 \text{ nm}$ exhibit mobility $<300 \text{ cm}^2/\text{V.s}$ (Fig. 4b)[†]. This leads to major energy efficiency benefits for CNFETs:

- 1) CNFET VLSI circuits can operate at reduced V_{DD} with simultaneously higher I_{EFF} vs. FinFET (e.g., 20% lower V_{DD} with 25% higher I_{EFF} at the same I_{OFF} for projected CNFET vs. experimental Si/SiGe FinFET: Fig. 4c)[‡].
- 2) Thin T_{BODY} results in very short λ (Fig. 4a). Therefore, experimental CNFETs maintain steep sub-threshold slope (SS) with deeply-scaled L_G (e.g., SS = 70 mV/decade with $L_G = 5 \text{ nm}$, which has been shown for both PMOS and NMOS CNFETs experimentally [4]).
- 3) Scaled CNFET L_G enables low total circuit capacitance (e.g., 2x lower for projected CNFET vs. experimental Si/SiGe FinFET: Fig. 4c). Due to high I_{EFF} , electronic design automation (EDA) tools can meet circuit-level timing constraints using planar CNFETs, which have lower gate capacitance ($C_G < 1.0 \text{ fF}/\mu\text{m}$)[§] vs. FinFETs, NWFETs, and NShFETs. In contrast, FinFETs, NWFETs, and NShFETs leverage channels that extend vertically above the substrate to increase I_{EFF} at the cost of higher parasitic $C_{GS,\text{PARASITIC}}$ and $C_{GD,\text{PARASITIC}}$ (these parameters are illustrated in Fig. 9b).

[†] While efficient carrier transport is required for high I_{EFF} , density of states must be sufficient to provide available carriers. CNTs do not suffer from a limited density of states, as they exhibit quantum capacitance (proportional to density of states) of 0.1-0.2 F/m² (for $P_{CNT} = 4 \text{ nm}$, $D_{CNT} = 1.7 \text{ nm}$) [22], comparable to Si (~0.1 F/m²) [34].

[‡] In addition to carrier mobility, other metrics for carrier transport, e.g., injection velocity (Fig. 4c), also degrade as T_{BODY} scales [22].

[§] Intrinsic gate-to-channel capacitance (C_{GC} : Fig. 9b) is proportional to L_G , and parasitic gate-to-source/drain capacitance ($C_{GS,\text{PARASITIC}} = C_{GD,\text{PARASITIC}} = C_{SP} + C_{IF} + C_{OF}$: Fig. 9b) is inversely proportional to source/drain extension length: L_X (Fig. 9b); thus, shorter L_G reduces C_{GC} and also reduces $C_{GS,\text{PARASITIC}}$ and $C_{GD,\text{PARASITIC}}$ (as it enables larger L_X for fixed CGP (often fixed for a technology node)).

4) Despite R_C non-idealities in experimental CNFETs today ($R_C = 18.25 \text{ k}\Omega/\text{CNT}$ for $L_C = 9 \text{ nm}$) [29], experimental CNFET offers 5.6x EDP benefit vs. experimental Si/SiGe FinFET.

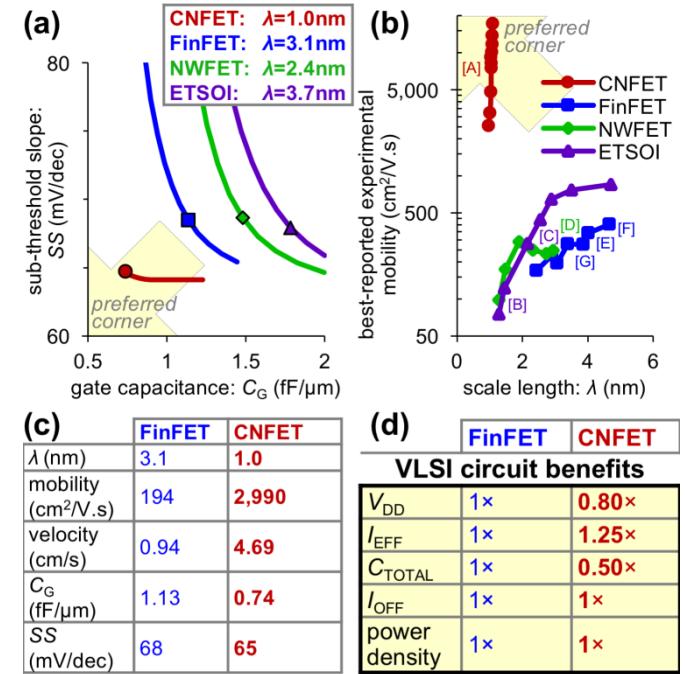


Fig. 4. Key CNFET technology advantages. (a) Trade-off between SS and C_G , illustrating the importance of small electrostatic scale length (λ). For each technology, the marked point indicates SS and C_G for the EDP-optimal design in Fig. 2, and then each trade-off curve illustrates the effect of sweeping L_G (from 9 nm to 22 nm with fixed CGP and fixed L_C : larger L_G improves SS at the cost of increased C_G). Both intrinsic and parasitic components are included in C_G : the total gate capacitance per micron of effective channel width (W_{EFF} : which accounts for the three-dimensional (3D) topology of the semiconductor channel, e.g., the effective width of a FinFET is proportional to $T_{FIN} + 2H_{FIN}$, which may exceed the width per unit footprint). (b) Despite the benefit of small λ to achieve steep SS and small C_G , scaled λ significantly degrades experimentally-measured carrier mobility: references (details below) indicate the best-reported experimentally-measured long channel peak mobility vs. body thickness data (see [35] for the relationship between long channel mobility and “apparent mobility” for short-channel FETs), and λ is determined from the T_{BODY} using additional technology parameters (e.g., T_{OX} : see Table I). (c) Optimized λ , mobility, velocity, C_G , and SS, and resulting VLSI circuit benefits for the EDP-optimal design in Fig. 2: CNFETs can deliver higher I_{EFF} with lower V_{DD} and lower total circuit capacitance (C_{TOTAL}), for the same I_{OFF} and power density. References in (b) are: [A]: [26], [B]: [25], [C]: [19], [D]: [24], [E]: [20], [F]: [21], [G]: [10].

IV. CONSIDERATIONS FOR DEEPLY-SCALDED TECHNOLOGIES

A. CNT-metal contact resistance

CNFETs can deliver higher drive current vs. FinFETs (for the same I_{OFF}) despite higher contact resistance ($R_C = 18.25 \text{ k}\Omega/\text{CNT}$ at each source/drain contact: shown experimentally for $L_C = 9 \text{ nm}$ [29]), corresponding to $75 \Omega.\mu\text{m}$ for 4 nm P_{CNT} , vs. $14.3 \Omega.\mu\text{m}$ for experimental Si/SiGe FinFET (for $L_C = 14 \text{ nm}$ and $2 \times 10^{-9} \Omega.\text{cm}^2$ contact resistivity: Table I). For both CNFET and FinFET, drive current is affected by both parasitic series resistance (including contact resistance) and the resistance of the FET channel. For example, in the linear regime, i.e., with $V_{GS} \gg V_{DS}$, drain current (I_D) is strongly impacted by both contact resistance and by carrier mobility; superior mobility for CNFETs leads to

higher I_D in the linear regime ($I_{D,\text{LINEAR}}$) despite higher contact resistance. For example, Fig. 5a shows I_D vs. V_{DS} characteristics for CNFET with $R_C = 3.25 \text{ k}\Omega/\text{CNT}$ and $R_C = 18.25 \text{ k}\Omega/\text{CNT}$, as well as FinFET (with $2 \times 10^{-9} \Omega\cdot\text{cm}^2$ contact resistivity). For each case, it illustrates $I_{D,\text{LINEAR}}$ at $V_{DS,\text{LINEAR}} = 0.05 \text{ V}$ with $V_{GS} = 0.5 \text{ V}$. For CNFET with $R_C = 3.25 \text{ k}\Omega/\text{CNT}$, $I_{D,\text{LINEAR}} = 0.75 \text{ mA}/\mu\text{m}$, which exceeds $0.35 \text{ mA}/\mu\text{m}$ for FinFET. Even for CNFET with $R_C = 18.25 \text{ k}\Omega/\text{CNT}$, $I_{D,\text{LINEAR}} = 0.27 \text{ mA}/\mu\text{m}$, but superior virtual source velocity for CNFET (Table I) leads to higher I_D in the saturation regime: $1.49 \text{ mA}/\mu\text{m}$ vs. $1.12 \text{ mA}/\mu\text{m}$ for FinFET, at $V_{DS} = V_{GS} = 0.5 \text{ V}$. This contributes to significant CNFET EDP benefits vs. FinFET even with degraded R_C vs. values shown experimentally, as shown in Fig. 5b. Continued R_C improvements (e.g., $R_C = 3.25 \text{ k}\Omega/\text{CNT}$, as described in Sec. II) further improve EDP.

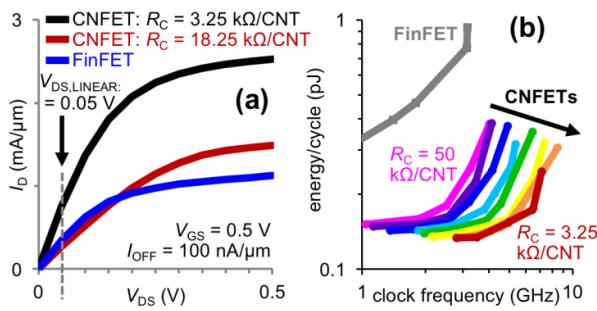


Fig. 5. CNFET EDP benefits vs. CNT-metal contact resistance. (a) I_D vs. V_{DS} , where the threshold voltage is shifted to achieve I_{OFF} density = 100 nA/ μm for $V_{GS} = 0 \text{ V}$ and $V_{DS} = V_{DD}$ (b) Even with severely degraded $R_C = 50 \text{ k}\Omega/\text{CNT}$ (for $L_C = 9 \text{ nm}$, larger than experimentally demonstrated $R_C = 18.25 \text{ k}\Omega/\text{CNT}$ for the same L_C [29]), CNFET VLSI circuits offer significant energy efficiency benefits vs. FinFET (shown for the OpenSPARC core module: “lsu”), using the same VLSI circuit design and analysis methodology in Sec. II to derive results in Fig. 2 & Fig. 3.

B. Interconnect

While interconnect wire parasitics are significant for VLSI circuits, interconnect delay and energy improve in CNFET circuits (despite no material changes in interconnect technology in this paper) due to the improved I_{EFF} , C_G , and V_{DD} of CNFETs (Fig. 4c-d). Further back-end-of-line (BEOL) technology improvements (e.g., thinning copper (Cu) diffusion barrier [36], or Cu replacement by Co or Ru) can result in additional EDP benefits.

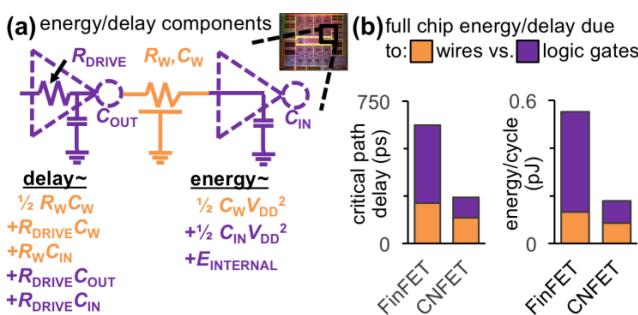


Fig. 6. Wire energy and delay in both Si- and CNFET-based circuits. (a) Example schematic showing energy/delay components attributed to interconnect wires vs. logic gates. (b) Critical path delay and energy per cycle, separated into energy/delay attributed to interconnects vs. logic gates (for the 32-bit commercial processor core in Fig. 3); BEOL interconnect accounts for 34% of the critical path delay and 24% of the total energy for FinFET, vs. 56% of the critical path delay and 49% of the total energy for CNFET.

C. Two-Dimensional (2D) material FETs

While 2D material FETs also enable thin T_{BODY} [37], their carrier transport is lower vs. CNFETs (mobility: $380 \text{ cm}^2/\text{V}\cdot\text{s}$ vs. $>2,500 \text{ cm}^2/\text{V}\cdot\text{s}$, and virtual source velocity: $2.0 \times 10^7 \text{ cm/s}$ for black phosphorous [36] vs. $4.1 \times 10^7 \text{ cm/s}$ for CNFET [22]). This limits potential benefits for 2D materials FETs to $2.2 \times$ [36] even for projected contact resistivity $\rho_{CON} = 1.0 \times 10^8 \Omega\cdot\text{cm}^2$ (vs. the lowest-reported $\rho_{CON} = 3.0 \times 10^7 \Omega\cdot\text{cm}^2$ for few-layer MoS₂ [38]); Table I and Table II show ρ_{CON} for technologies in this work.

D. CNT imperfections and variations

CNFETs are subject to CNT imperfections and variations [30] (e.g., mis-positioned CNTs, metallic CNTs, CNT density and diameter variations). These challenges are overcome in a VLSI-compatible manner by a combination of processing and design techniques: the imperfection-immune paradigm [30], [39], [40], which enabled large-scale CNFET circuit demonstrations [6], [7]. This approach preserves $>90\%$ of projected $9\times$ CNFET EDP benefits (despite CNT variations) [39], while simultaneously meeting circuit-level yield and noise margin constraints [39].

V. CONCLUSION

We demonstrate that CNFETs are projected to offer $9\times$ EDP benefit vs. Si/SiGe FinFET for VLSI circuits. ATOs are projected to provide $<50\%$ EDP benefits. We also provide insights into the sources of these major CNFET benefits, and address key questions for deeply-scaled technologies. With CNFETs, further EDP benefits are possible: 1) new gate stacks leveraging negative capacitance [14]; 2) new monolithic 3D architectures (enabled by low-temperature fabrication of CNFETs) that vertically interleave layers of logic and memory with ultra-dense vertical connectivity (e.g., demonstrated in [7]), which promise computing system-level energy efficiency benefits in the range of $1,000\times$ [41], [42].

APPENDIX

Three key features of our VLSI design flow and analysis methodology (available for download: [43]) include:

- 1) SPICE-compatible FET compact models that are calibrated to experimental FET data for sub-10 nm nodes (i.e., with physical dimensions applicable for sub-10 nm node CGP and metal pitch), and that include FET- and standard cell-level parasitics (inverter shown in Fig. 8). These compact models account for several non-idealities, including (but not limited to): direct source-to-drain tunneling leakage current, parasitic gate-to-plug capacitance, fringing capacitance, and parasitic series resistance such as source/drain extension region resistance and contact resistance. Intrinsic parameters for carrier transport in the FET channel (e.g., mobility and injection velocity), have been calibrated using experimental data [3], [10], [18], [19], [20], [21], [22], [23], [24], [25], [26] for sub-20 nm L_G for the technologies analyzed, including CNFETs scaled to 9 nm L_G . FET characterization results are in Table I (7 nm node) and Table II (5 nm node).

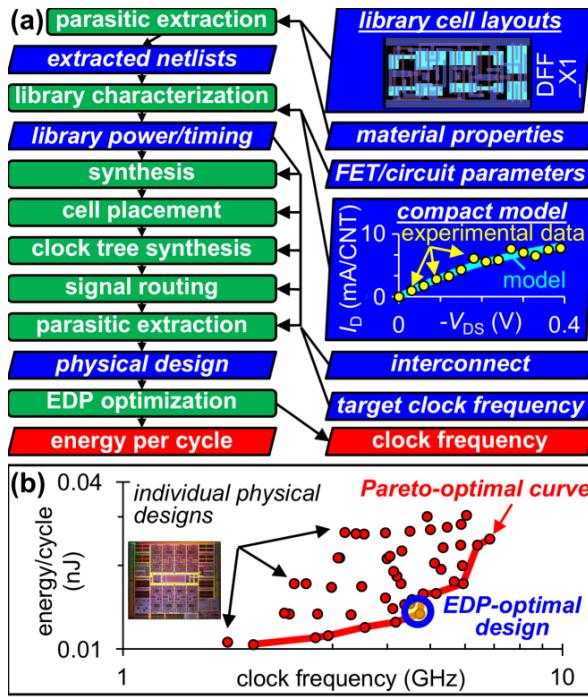


Fig. 7. (a) VLSI design and analysis flow, including experimentally measured CNFET drain current vs. drain-to-source voltage (I_D vs. V_{DS}) to calibrate the CNFET compact model [22]. (b) Energy vs. clock frequency, showing the Pareto-optimal trade-off curve and EDP-optimal design (over many designs).

2) Timing and power characterization of standard cell libraries over a range of FET- and circuit-level parameters including supply voltage (V_{DD} : 0.35-0.60 V), off-state leakage current density (I_{OFF} density: 0.015-100 nA/ μm), and gate length (L_G : 9-22 nm). These libraries are then used in conjunction with industry-practice electronic design automation (EDA) tools for synthesis (Synopsys Design Compiler) and place-and-route (Synopsys IC Compiler, Cadence Encounter) of processor core physical designs (OpenSPARC T2 [17], and a commercial 32-bit processor core targeting low power applications). These designs include parasitics extracted from standard cell layouts, as well as local and global metal interconnects. Back-end-of-line (BEOL) wire capacitances are determined using a commercial 3D extraction tool (Synopsys StarRC) using wire dimensions and inter-layer dielectric constants. Wire resistance is computed using the Steinhögl model with wire cross-section-area-dependent Cu resistivity calibrated to experimental data (details in [36]).

3) VLSI processor core (including wire interconnects) EDP optimization for each technology, selecting the set of Pareto-optimal designs from over 200 design candidates (of the above processor core physical designs; a design is Pareto-optimal if no other design operates a higher clock frequency for less energy (Fig. 7b)). For each standard cell library (characterized over multiple V_{DD} , I_{OFF} , and technology parameters such as L_G (as described in #2 above)), we perform synthesis, place-and-route, and power/timing characterization for multiple target clock frequencies (i.e., to set timing constraints: 100 MHz to 10 GHz in steps of 100 MHz), thus enabling EDA tools to trade-off energy vs. clock frequency, e.g., through logic gate sizing and buffer insertion. Each power/timing analysis result is represented by a single point on the energy vs. frequency

plot in Fig. 7b, and then only the Pareto-optimal designs are recorded. In addition to this family of Pareto-optimal designs, the design with minimum EDP, which also satisfies a maximum power density of 100 W/cm² [28] is used to quantify the relative energy efficiency of each technology. Fig. 8 shows the distribution of wire capacitance: C_W and wire resistance: R_W (per unit length) extracted from physical designs of process cores at the 7 nm and 5 nm nodes (after place-and-route; results correspond to the EDP-optimal design using CNFETs).

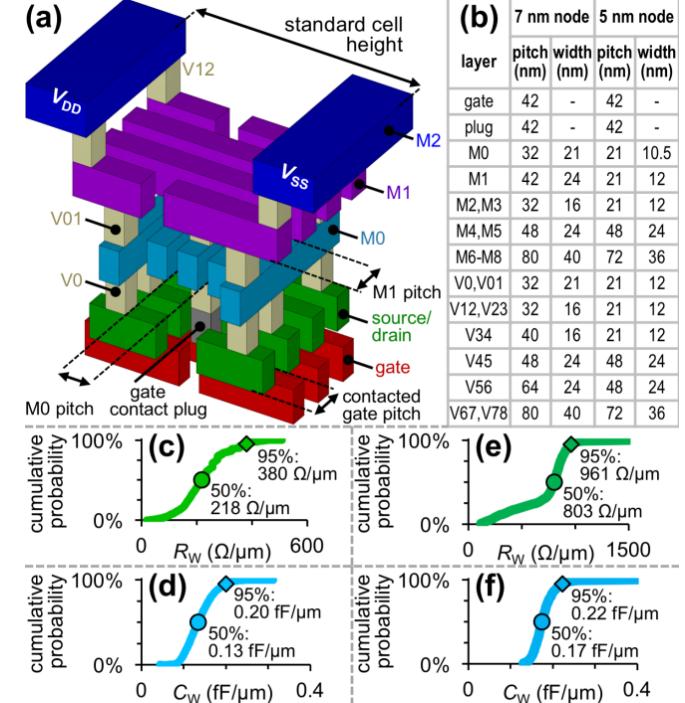


Fig. 8. Interconnect summary. (a) 3D illustration of 7 nm node inverter. (b) Wire dimensions for the 7 nm and 5 nm nodes. (c) Cumulative distribution of wire resistance per unit length (R_W) for the 7 nm node OpenSPARC T2 core (for the EDP-optimal design using CNFETs in Fig. 2; cumulative distribution of wire capacitance per unit length (C_W) shown in (d)). (e) Distribution of R_W for the 5 nm node 32-bit commercial processor core (for the EDP-optimal design using CNFETs in Fig. 3; distribution of C_W shown in (f)).

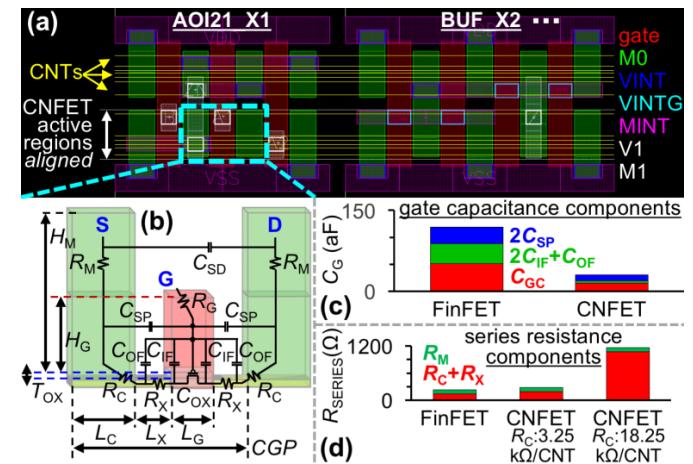


Fig. 9. Process design kit (PDK) summary, illustrated for CNFET. (a) 5 nm node standard cell layouts (example library cells: AOI21_X1, BUF_X2), with standard cell height equivalent to 5.5 metal routing tracks [16]. (b) Parasitic components in FET compact models (shown for CNFET). (c) FET gate capacitance components and (d) FET series resistance components (relevant parameters in Table II).

TABLE I

CHARACTERISTICS OF FETS: 7 NM NODE. N = “NFET”, P = “PFET” (UNSPECIFIED N/P APPLIES TO BOTH NFET AND PFET), CORRESPONDING TO THE TECHNOLOGIES IN FIG. 1. ON-CURRENT DENSITY (I_{ON} : FET DRAIN CURRENT FOR $V_{GS} = V_{DS} = V_{DD}$) AND SUB-THRESHOLD SLOPE (SS_{SAT} : MEASURED AT $V_{GS} = 0$ V WITH $V_{DS} = V_{DD}$) CORRESPONDING TO THE EDP-OPTIMAL DESIGNS FOR EACH TECHNOLOGY IN FIG. 2 (E.G., WITH DIFFERENT V_{DD} FOR EACH TECHNOLOGY). **BOLD BLUE TEXT** IS FOR PROJECTED TECHNOLOGIES (DESCRIBED IN SEC. II), PLAIN TEXT CORRESPONDS TO EXPERIMENTAL TECHNOLOGIES (SEC. II). MANY PARAMETERS ARE FIXED VS. FET TYPE TO FAIRLY COMPARE EDP, INCLUDING: CGP , M1 PITCH, T_{OX} , EQUIVALENT OXIDE THICKNESS (EOT), CAPACITANCE EQUIVALENT THICKNESS (CET , WHICH ACCOUNTS FOR THE “INVERSION LAYER THICKNESS,” I.E., DUE TO THE QUANTUM MECHANICAL EFFECT THAT THE INVERSION CHARGE IS NOT LOCATED AT THE INTERFACE BETWEEN THE SEMICONDUCTOR AND THE GATE OXIDE). FOR T_{OX} AND EOT : SILICON-BASED FETS COMPRIZE 0.5 NM SiO_2 ($K = 3.9$) AND 1.5 NM HfO_2 ($K = 23$), THE SAME IS USED FOR CNFET. FOR CNFET, QUANTUM CAPACITANCE IS INCLUDED IN THE CNFET COMPACT MODEL AND SO CET IS NOT APPLICABLE HERE. STANDARD CELL HEIGHT IS QUANTIFIED BY THE NUMBER OF M1 ROUTING TRACKS: 7.5 TRACKS FOR THE 7 NM NODE ANALYZED HERE. NOTE THAT, THE 5 NM NODE ANALYZED IN THIS WORK (DETAILS IN TABLE II) LEVERAGES MORE HIGHLY-SCALED STANDARD CELL HEIGHT WITH 5.5 METAL TRACKS, AND 4.5 METAL TRACKS FOR WHICH NSHFET IS USED INSTEAD OF NWFET TO INCREASE DRIVE CURRENT FOR FETS WITH SMALL WIDTH (NOTE THAT, FET WIDTH IS LIMITED BY THE STANDARD CELL HEIGHT) [44]. K_{SPACER} : DIELECTRIC CONSTANT OF OXIDE BETWEEN THE GATE AND SOURCE/DRAIN. PARAMETERS FOR BODY THICKNESS, CHANNEL PITCH, AND HEIGHT ARE SHOWN IN FIG. 1. LVT: “LOW” THRESHOLD VOLTAGE (VT) TECHNOLOGY. PROJECTED CNFET HAS IMPROVED CONTACT RESISTANCE VS. EXPERIMENTAL CNFET. PROJECTED Si/SiGe FINFET AND PROJECTED Si/SiGe NWFET HAVE THINNER BODIES (T_{FIN} AND D_{NW} , RESPECTIVELY, ILLUSTRATED IN FIG. 1) FOR IMPROVED ELECTROSTATIC CONTROL, AND UNREALISTICALLY SUFFER NO MOBILITY OR VELOCITY DEGRADATION DESPITE THE THINNER BODIES. GIVEN MANY OPTIONS FOR FUTURE MEMORY TECHNOLOGIES – ESPECIALLY THOSE WHICH CAN BE MONOLITHICALLY INTEGRATED IN THREE DIMENSIONS ENABLING COMPUTATION IMMERSED IN MEMORY [41] – ENERGY AND FREQUENCY IN THIS WORK ARE REPORTED FOR LOGIC (CACHES AND OTHER MEMORIES WARRANT SEPARATE ANALYSES). FOR DIRECT COMPARISON OF FET-LEVEL PERFORMANCE METRICS, I_{ON} AND SS_{SAT} RESULTS ARE PROVIDED FOR $V_{DD} = 0.5$ V.

experimental & projected	Si/SiGe FinFET	ETSOI	Si/SiGe NWFET	CNFET
Technology node label	“7 nm node”	“7 nm node”	“7 nm node”	“7 nm node”
CGP (nm)	42	42	42	42
M1 pitch, width (nm)	32	32	32	32
Standard cell height (metal tracks)	7.5	7.5	7.5	7.5
L_C, L_C, L_x (nm)	18, 14, 5	20, 12, 5	14, 18, 5	9, 9, 12
Gate height (nm)	30	30	30	30
Gate oxide T_{OX} (nm)	2.0	2.0	2.0	2.0
Gate oxide EOT (nm)	0.75	0.75	0.75	0.75
Gate oxide CET (nm)	1.15	1.15	1.15	-
Gate oxide K_{OX}	10.3	10.3	10.3	10.3
Spacer oxide K_{SPACER}	5.0	5.0	5.0	5.0
Body thickness (nm)	$T_{FIN} = 5$	$T_{SOI} = 5$	$D_{NW} = 7$	$D_{CNT} = 1.7$
Channel pitch (nm)	$P_{FIN} = 24$	-	$P_H = 24, P_V = 18$	$P_{CNT} = 4$
Channel height (nm)	$H_{FIN} = 35$	-	$N_{NW,V} = 2, O_V = 10$	-
I_{OFF} : LVT	100 (2.4 nA/fin for $P_{FIN} = 24$ nm)	100	100 (1.2 nA/NW for $P_H = 24$ nm, $N_{NW,V} = 2$)	100 (0.4 nA/CNT for $P_{CNT} = 4$ nm)
Contact resistivity	$2 \times 10^{-9} \Omega \cdot \text{cm}^2$ (14.3 $\Omega \cdot \mu\text{m}$ for $L_c = 14$ nm)	$2 \times 10^{-9} \Omega \cdot \text{cm}^2$ (16.7 $\Omega \cdot \mu\text{m}$ for $L_c = 12$ nm)	$2 \times 10^{-9} \Omega \cdot \text{cm}^2$ (11.1 $\Omega \cdot \mu\text{m}$ for $L_c = 18$ nm)	18.25 k Ω /CNT (73 $\Omega \cdot \mu\text{m}$ for $P_{CNT} = 4$ nm) [29] 3.25 kΩ/CNT (13 $\Omega \cdot \mu\text{m}$ for $P_{CNT} = 4$ nm) [27]
Apparent mobility [35] ($\text{cm}^2/\text{V.s}$)	N: 67, P: 80 for $T_{FIN} = 5$ nm, maintained for $T_{FIN} = 3$ nm	100 for $T_{SOI} = 5$ nm	N: 92, P: 100 for $D_{NW} = 7$ nm, maintained for $D_{NW} = 5$ nm	358 for $D_{CNT} = 1.7$ nm [22]
Injection velocity (10^7 cm/s)	N: 0.62, P: 0.94 for $T_{FIN} = 5$ nm, N: 0.62, P: 0.94 for $T_{FIN} = 3$ nm	0.60 for $T_{SOI} = 5$ nm	N: 1.11, P: 1.67 for $D_{NW} = 7$ nm, maintained for $D_{NW} = 5$ nm	4.69 for $D_{CNT} = 1.7$ nm [22]
I_{ON} (mA/ μm)	N: 1.122, P: 1.404 (26.9, 33.7 $\mu\text{A}/\text{fin}$) N: 1.239, P: 1.547 (29.7, 37.1 $\mu\text{A}/\text{fin}$)	N: 0.377, P: 0.377	N: 0.942, P: 1.089 (11.3, 13.1 $\mu\text{A}/\text{NW}$) N: 0.765, P: 0.879 (9.2, 10.6 $\mu\text{A}/\text{NW}$)	1.192 (4.8 $\mu\text{A}/\text{CNT}$) 2.012 (8.0 $\mu\text{A}/\text{CNT}$)
Sub-threshold slope: SS_{SAT} (mV/decade)	N: 68.5, P: 68.4 N: 63.4, P: 63.3	78.7	N: 68.7, P: 68.6 N: 65.1, P: 65.2	64.7

TABLE II

CHARACTERISTICS OF FETS: 5 NM NODE. AS IN TABLE I, N = "NFET", P = "PFET", AND UNSPECIFIED N/P APPLIES TO BOTH NFET AND PFET; FOR EACH TECHNOLOGY, VALUES CORRESPOND TO THE EDP-OPTIMAL DESIGN IN FIG. 3. COMPARED TO STANDARD CELL HEIGHT OF 7.5 M1 TRACKS FOR THE 7 NM NODE TECHNOLOGIES IN TABLE I, CELL HEIGHT IS MORE HIGHLY SCALED TO 5.5 M1 TRACKS AND TO 4.5 M1 TRACKS, FOR WHICH NSHFET IS USED INSTEAD OF NWFET TO IMPROVE FET DRIVE CURRENT FOR FETS WITH HIGHLY-SCALED WIDTH [44]. PROJECTED CNFET HAS IMPROVED CONTACT RESISTANCE VS. EXPERIMENTAL CNFET. PROJECTED Si/SiGe FINFET AND PROJECTED Si/SiGe NANOSHEET FET EXHIBIT IMPROVED MOBILITY (DUE TO HIGHER STRESS IN THE CHANNEL (1.6 GPA FOR BOTH NFET AND PFET) USING STRAIN RELAXED BUFFER (SRB) [45]). PROJECTED Si/SiGe FINFET ALSO USES A WRAP-AROUND CONTACT (WAC) INSTEAD OF A DIAMOND-EPI CONTACT (DEC) TO IMPROVE CONTACT RESISTANCE BY INCREASING THE CONTACT AREA WITH THE SAME FOOTPRINT [46]. AS IN TABLE I, FOR DIRECT COMPARISON OF FET-LEVEL PERFORMANCE METRICS, I_{ON} AND SS_{SAT} RESULTS ARE PROVIDED FOR $V_{DD} = 0.5$ V.

experimental & projected	Si/SiGe FinFET	Si/SiGe Nanosheet FET	CNFET
Technology node label	"5 nm node"	"5 nm node"	"5 nm node"
CGP (nm)	42	42	42
M1 pitch, width (nm)	21	21	21
Standard cell height (metal tracks)	5.5	4.5	5.5
L_c, L_c, L_x (nm)	15, 15, 6	12, 18, 6	10, 15, 8.5
Gate height (nm)	20	20	20
Gate oxide T_{ox} (nm)	1.9	1.9	1.9
Gate oxide EOT (nm)	0.70	0.70	0.70
Gate oxide CET (nm)	1.10	1.10	-
Gate oxide K_{ox}	10.6	10.6	10.6
Spacer oxide K_{SPACER}	4.0	4.0	4.0
Body thickness (nm)	$T_{FIN} = 5$	$T_{NSH} = 5, W_{NSH} = 11$	$D_{CNT} = 1.8$
Channel pitch (nm)	$P_{FIN} = 21$	$P_V = 12, P_H = 21$	$P_{CNT} = 2$
Channel height (nm)	$H_{FIN} = 40$	$N_{NSH,V} = 2, O_V = 10$	-
I_{OFF} : LVT (nA/ μ m)	84 (2.0 nA/fin for $P_{FIN} = 21$ nm)	84 (2.0 nA/NSh for $N_{NSH,V} = 2$)	84 (0.042 nA/CNT for $P_{CNT} = 2$ nm)
Contact resistivity	$0.5 \times 10^{-9} \Omega \cdot \text{cm}^2$ ($3.3 \Omega \cdot \mu\text{m}$ for $L_c = 15$ nm) for diamond epi contact (DEC), maintained for wrap-around contact (WAC)	$0.5 \times 10^{-9} \Omega \cdot \text{cm}^2$ ($2.8 \Omega \cdot \mu\text{m}$ for $L_c = 18$ nm) for wrap-around contact (WAC)	18.25 k Ω /CNT ($36.5 \Omega \cdot \mu\text{m}$ for $P_{CNT} = 2$ nm) [29], 3.25 kΩ/CNT (6.5 $\Omega \cdot \mu\text{m}$ for $P_{CNT} = 2$ nm) [So11][27]
Apparent mobility [35] ($\text{cm}^2/\text{V.s}$)	N: 54.4, P: 110.2 for stress = 1.6 GPa (N), 0.6 GPa (P), N: 78.6, P: 110.2 for strain-relaxed buffer (SRB) with stress = 1.6 GPa (N & P)	N: 67.6, P: 93.1 for strain-relaxed buffer (SRB) with stress = 1.6 GPa (N & P)	427.8 for $D_{CNT} = 1.8$ nm [22]
Injection velocity (10^7 cm/s)	N: 1.15, P: 1.56	N: 1.15, P: 1.56	4.80 for $D_{CNT} = 1.8$ nm [22]
I_{ON} (mA/ μ m)	N: 1.094, P: 1.442 (22.9, 30.2 $\mu\text{A}/\text{fin}$) N: 1.215, P: 1.518 (25.5, 31.9 $\mu\text{A}/\text{fin}$)	N: 1.020, P: 1.177 (10.7, 12.4 $\mu\text{A}/\text{NSh}$ for $N_{NSH,V} = 2, P_H = 21$)	1.365 (2.7 $\mu\text{A}/\text{CNT}$) 1.958 (3.9 $\mu\text{A}/\text{CNT}$)
Sub-threshold slope: SS_{SAT} (mV/decade)	N: 80.5, P: 80.5	N: 80.2, P: 80.2	63.8

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REFERENCES

- [1] Gonzalez, Ricardo, and Mark Horowitz. "Energy dissipation in general purpose microprocessors." *IEEE Journal of solid-state circuits* 31, no. 9 (1996): 1277-1284.
- [2] Brady, Gerald J., Austin J. Way, Nathaniel S. Safron, Harold T. Evensen, Padma Gopalan, and Michael S. Arnold. "Quasi-ballistic carbon nanotube array transistors with current density exceeding Si and GaAs." *Science advances* 2, no. 9 (2016): e1601240.
- [3] Franklin, Aaron D., Mathieu Luisier, Shu-Jen Han, George Tulevski, Chris M. Breslin, Lynne Gignac, Mark S. Lundstrom, and Wilfried Haensch. "Sub-10 nm carbon nanotube transistor." *Nano letters* 12, no. 2 (2012): 758-762.
- [4] Qiu, Chenguang, Zhiyong Zhang, Mengmeng Xiao, Yingjun Yang, Donglai Zhong, and Lian-Mao Peng. "Scaling carbon nanotube complementary transistors to 5-nm gate lengths." *Science* 355, no. 6322 (2017): 271-276.
- [5] Shulaker, Max M., Gregory Pitner, Gage Hills, Marta Giachino, H-S. Philip Wong, and Subhasish Mitra. "High-performance carbon nanotube field-effect transistors." In *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 33-6. IEEE, 2014.
- [6] Shulaker, Max M., Gage Hills, Nishant Patil, Hai Wei, Hong-Yu Chen, H-S. Philip Wong, and Subhasish Mitra. "Carbon nanotube computer." *Nature* 501, no. 7468 (2013): 526-530.
- [7] Shulaker, Max M., Gage Hills, Rebecca S. Park, Roger T. Howe, Krishna Saraswat, H-S. Philip Wong, and Subhasish Mitra. "Three-dimensional integration of nanotechnologies for computing and data storage on a single chip." *Nature* 547, no. 7661 (2017): 74-78.
- [8] Nikonorov, Dmitri E., and Ian A. Young. "Uniform methodology for benchmarking beyond-CMOS logic devices." In *Electron Devices Meeting (IEDM), 2012 IEEE International*, pp. 25-4. IEEE, 2012.
- [9] Tulevski, George S., Aaron D. Franklin, David Frank, Jose M. Lobez, Qing Cao, Hongsik Park, Ali Afzali, Shu-Jen Han, James B. Hannan, and Wilfried Haensch. "Toward high-performance digital logic technology with carbon nanotubes." *ACS nano* 8, no. 9 (2014): 8730-8745.
- [10] Sasaki, Y., R. Ritzenthaler, Y. Kimura, D. De Roest, X. Shi, A. De Keersgieter, M. S. Kim et al. "Novel junction design for NMOS Si Bulk-FinFETs with extension doping by PEALD phosphorus doped silicate glass." In *Electron Devices Meeting (IEDM), 2015 IEEE International*, pp. 21-8. IEEE, 2015.
- [11] Mertens, Hans, Romain Ritzenthaler, Andriy Hikavyy, Min-Soo Kim, Zheng Tao, Kurt Wostyn, Soon Aik Chew et al. "Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates." In *VLSI Technology, 2016 IEEE Symposium on*, pp. 1-2. IEEE, 2016.
- [12] Loubet, N., T. Hook, P. Montanini, C-W. Yeung, S. Kanakasabapathy, M. Guillom, T. Yamashita et al. "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET." In *VLSI Technology, 2017 Symposium on*, pp. T230-T231. IEEE, 2017.

- [13] Tsutsui, Gen, Masumi Saitoh, Takuya Saraya, Toshiharu Nagumo, and Toshiro Hiramoto. "Mobility enhancement due to volume inversion in [110]-oriented ultra-thin body double-gate nMOSFETs with body thickness less than 5 nm." In *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 729-732. IEEE, 2005.
- [14] Salahuddin, Sayeef, and Supriyo Datta. "Use of negative capacitance to provide voltage amplification for low power nanoscale devices." *Nano letters* 8, no. 2 (2008): 405-410.
- [15] Srimani, Tathagata, Gage Hills, Mindy D. Bishop, Ujwal Radhakrishna, Ahmad Zubair, Rebecca S. Park, Yosi Stein, Tomas Palacios, Dimitri Antoniadis, and Max Shulaker, "Negative Capacitance Carbon Nanotube FETs." *IEEE Electron Device Letters* (2017).
- [16] Garcia Bardon, Marie, Y. Sherazi, P. Schuddinck, D. Jang, D. Yakimets, P. Debacker, R. Baert et al. "Extreme scaling enabled by 5 tracks cells: Holistic design-device co-optimization for FinFETs and lateral nanowires." In *Electron Devices Meeting (IEDM), 2016 IEEE International*, pp. 28-2. IEEE, 2016.
- [17] (December 2011). *OpenSPARC T2 Processor Core*. [Online]. Available: <http://www.opensparc.net/opensparc-t2>.
- [18] Franklin, Aaron D., and Zhihong Chen. "Length scaling of carbon nanotube transistors." *Nature nanotechnology* 5, no. 12 (2010): 858-862.
- [19] Gomez, Leonardo, I. Aberg, and J. L. Hoyt. "Electron transport in strained-silicon directly on insulator ultrathin-body n-MOSFETs with body thickness ranging from 2 to 25 nm." *IEEE electron device letters* 28, no. 4 (2007): 285-287.
- [20] Hashemi, Pouya, Karthik Balakrishnan, Amlan Majumdar, Ali Khakifirooz, Wanki Kim, Ashish Baraskar, Li A. Yang et al. "Strained Si 1-x Ge x-on-insulator PMOS FinFETs with excellent sub-threshold leakage, extremely-high short-channel performance and source injection velocity for 10nm node and beyond." In *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on*, pp. 1-2. IEEE, 2014.
- [21] Hashemi, Pouya, Karthik Balakrishnan, Sebastian U. Engelmann, John A. Ott, Ali Khakifirooz, Ashish Baraskar, Marinus Hopstaken et al. "First demonstration of high-Ge-content strained-Si_{1-x}Ge_x (x=0.5) on insulator PMOS FinFETs with high hole mobility and aggressively scaled fin dimensions and gate lengths for high-performance applications." In *Electron Devices Meeting (IEDM), 2014 IEEE International*, pp. 16-1. IEEE, 2014.
- [22] Lee, C-S., Eric Pop, Aaron D. Franklin, Wilfried Haensch, and H-SP Wong. "A compact virtual-source model for carbon nanotube FETs in the sub-10-nm regime—Part I: Intrinsic elements." *IEEE transactions on electron devices* 62, no. 9 (2015): 3061-3069.
- [23] Lee, Chi-Shuen, Eric Pop, Aaron D. Franklin, Wilfried Haensch, and Hon-Sum Philip Wong. "A compact virtual-source model for carbon nanotube FETs in the sub-10-nm regime—part II: Extrinsic elements, performance assessment, and design optimization." *IEEE Transactions on Electron Devices* 62, no. 9 (2015): 3070-3078.
- [24] Suk, Sung Dae, Ming Li, Yun Young Yeoh, Kyoung Hwan Yeo, Keun Hwi Cho, In Kyung Ku, Hong Cho et al. "Investigation of nanowire size dependency on TSNWFET." In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pp. 891-894. IEEE, 2007.
- [25] Uchida, Ken, Junji Koga, and Shin-ichi Takagi. "Experimental study on carrier transport mechanisms in double-and single-gate ultrathin-body MOSFETs-Coulomb scattering, volume inversion, and/or δT_{SOI} -induced scattering." In *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*, pp. 33-5. IEEE, 2003.
- [26] Zhou, Xinjian, Ji-Yong Park, Shaoming Huang, Jie Liu, and Paul L. McEuen. "Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors." *Physical Review Letters* 95, no. 14 (2005): 146805.
- [27] Solomon, Paul M. "Contact resistance to a one-dimensional quasi-ballistic nanotube/wire." *IEEE Electron Device Letters* 32, no. 3 (2011): 246-248.
- [28] (2013). *ITRS Roadmap*. [Online]. Available: <http://www.itrs.net/Links/2013ITRS/Home2013.htm>.
- [29] Cao, Qing, Shu-Jen Han, Jerry Tersoff, Aaron D. Franklin, Yu Zhu, Zhen Zhang, George S. Tulevski, Jianshi Tang, and Wilfried Haensch. "End-bonded contacts for carbon nanotube transistors with low, size-independent resistance." *Science* 350, no. 6256 (2015): 68-72.
- [30] Zhang, Jie, Albert Lin, Nishant Patil, Hai Wei, Lan Wei, H. S. Wong, and Subhasish Mitra. "Robust digital VLSI using carbon nanotubes." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 31, no. 4 (2012): 453-471.
- [31] Cao, Qing, Shu-jen Han, George S. Tulevski, Yu Zhu, Darsen D. Lu, and Wilfried Haensch. "Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics." *Nature Nanotechnology* 8, no. 3 (2013): 180-186.
- [32] Frank, David J., Yuan Taur, and H-SP Wong. "Generalized scale length for two-dimensional effects in MOSFETs." *IEEE Electron Device Letters* 19, no. 10 (1998): 385-387.
- [33] Kuhn, Kelin J. "Considerations for ultimate CMOS scaling." *IEEE transactions on Electron Devices* 59, no. 7 (2012): 1813-1828.
- [34] Takagi, S. I., & Toriumi, A. (1995). Quantitative understanding of inversion-layer capacitance in Si MOSFET's. *IEEE Transactions on Electron Devices*, 42(12), 2125-2130.
- [35] Shur, Michael S. "Low ballistic mobility in submicron HEMTs." *IEEE Electron Device Letters* 23, no. 9 (2002): 511-513.
- [36] Lee, Chi-Shuen, Brian Cline, Saurabh Sinha, Greg Yeric, and H-S. Philip Wong. "32-bit Processor core at 5-nm technology: Analysis of transistor and interconnect impact on VLSI system performance." In *Electron Devices Meeting (IEDM), 2016 IEEE International*, pp. 28-3. IEEE, 2016.
- [37] Fiori, Gianluca, Francesco Bonaccorso, Giuseppe Iannaccone, Tomás Palacios, Daniel Neumaier, Alan Seabaugh, Sanjay K. Banerjee, and Luigi Colombo. "Electronics based on two-dimensional materials." *Nature nanotechnology* 9, no. 10 (2014): 768.
- [38] English, Chris D., Gautam Shine, Vincent E. Dorgan, Krishna C. Saraswat, and Eric Pop. "Improved contacts to MoS₂ transistors by ultra-high vacuum metal deposition." *Nano letters* 16, no. 6 (2016): 3824-3830.
- [39] Hills, Gage, Jie Zhang, Max Marcel Shulaker, Hai Wei, Chi-Shuen Lee, Arjun Balasingam, H-S. Philip Wong, and Subhasish Mitra. "Rapid co-optimization of processing and circuit design to overcome carbon nanotube variations." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 34, no. 7 (2015): 1082-1095.
- [40] Shulaker, Max M., Gage Hills, Tony F. Wu, Zhenan Bao, H-S. Philip Wong, and Subhasish Mitra. "Efficient metallic carbon nanotube removal for highly-scaled technologies." In *Electron Devices Meeting (IEDM), 2015 IEEE International*, pp. 32-4. IEEE, 2015.
- [41] Aly, Mohamed M. Sabry, Mingyu Gao, Gage Hills, Chi-Shuen Lee, Greg Pitner, Max M. Shulaker, Tony F. Wu et al. "Energy-efficient abundant-data computing: The n3xt 1,000x." *Computer* 48, no. 12 (2015): 24-33.
- [42] Hwang, William, Mohamed M. Sabry Aly, Yash H. Malviya, Mingyu Gao, Tony F. Wu, Christos Kozyrakis, H.-S. Philip Wong, and Subhasish Mitra. "3D Nanosystems Enable Embedded Abundant-Data Computing." *IEEE/ACM Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 1-2. IEEE, 2017.
- [43] Gage Hills (2015), "Variation-Aware Nanosystem Design Kit (NDK)," <https://nanohub.org/resources/22582>.
- [44] Jang, Doyoung, Dmitry Yakimets, Geert Eneman, Pieter Schuddinck, Marie García Bardon, Praveen Raghavan, Alessio Spessot, Diederik Verkest, and Anda Mocuta. "Device Exploration of NanoSheet Transistors for Sub-7-nm Technology Node." *IEEE Transactions on Electron Devices* 64, no. 6 (2017): 2707-2713.
- [45] Witters, L., J. Mitard, R. Loo, G. Eneman, H. Mertens, D. P. Brunco, S. H. Lee et al. "Strained germanium quantum well pMOS FinFETs fabricated on *in situ* phosphorus-doped SiGe strain relaxed buffer layers using a replacement Fin process." In *Electron Devices Meeting (IEDM), 2013 IEEE International*, pp. 20-4. IEEE, 2013.
- [46] Chou, Chen-Han, Chung-Chun Hsu, Wen-Kuan Yeh, Steve S. Chung, and Chao-Hsin Chien. "3D-TCAD simulation study of the contact all around T-FinFET structure for 10nm metal-oxide-semiconductor field-effect transistor." In *Silicon Nanoelectronics Workshop (SNW), 2016 IEEE*, pp. 190-191. IEEE, 2016.



Gage Hills is a post-doctoral researcher at Massachusetts Institute of Technology. He received his Ph.D. from Stanford University in 2018, advised by Prof. Subhasish Mitra and co-advised by Prof. H.-S. Philip Wong. His current research interests include development of very-large-scale integrated circuits using nanotechnologies, such as carbon nanotube field-effect transistors.



Marie Garcia Bardon received her M.Sc. degree in engineering from Université Catholique de Louvain, Belgium, in 2004, and her Ph.D. degree in electronics from Katholieke Universiteit Leuven in collaboration with imec, Belgium, in 2010. She is currently a Senior Research Scientist at imec, where she has continuously worked on emerging technologies targeting ultra-scaled nodes. Her interests include analysis and modelling of CMOS and beyond CMOS devices (FinFETs, nanosheets, Tunnel FETs, FerroFETs, CNTs), power-performance-area (PPA) analysis and benchmarking of digital circuits, design/technology cooptimization.



Gerben Doornbos received the Ph.D. degree in physics from the Vrije Universiteit, Amsterdam, The Netherlands, in 2001. From 2000 until 2009 he was with Philips Research, which transitioned to NXP Semiconductors in 2006. Since 2009 he is with TSMC Europe B.V., Leuven, Belgium, working on technology computer-aided design (TCAD) of advanced logic technologies.



Dmitry Yakimets (M) received the B. Eng. Degree from Bauman Moscow State Technical University, Russia, in 2010, the M.Sc. degree from the Institut Polytechnique de Grenoble, France, in 2012, and the Ph.D. degree from the Katholieke Universiteit Leuven, Belgium, in 2016. Currently, he works at imec, Belgium as R&D Engineer, focusing on power, performance and area benchmarking of emerging devices for advanced technology nodes.



Pieter Schuddinck (M'12) received the M.Sc. degree in electrotechnical engineering from Ghent University, Ghent, Belgium, in 2005. He has been involved in electronics research in both private and academic institutions. He joined imec, Leuven, Belgium, as a Design Engineer, in 2011, where he has focused on modeling and evaluation of FE/MOL parasitic impedances in advanced technology nodes.



Rogier Baert received the M.Sc. degree in electrical engineering from the Eindhoven University of Technology, the Netherlands. He is currently a senior R&D engineer with the Semiconductor Technology and Systems unit at imec, Leuven, Belgium. His research interests include modeling and analysis of on-chip interconnect, and system technology co-optimization for future process nodes.



Doyoung Jang received the Ph.D. degree in electrical engineering from Korea University, Seoul, South Korea, and the International Dual Degree from the Institut Polytechnique de Grenoble, Grenoble, France, in 2012. Since 2012, he has been with imec, Leuven, Belgium. His current research interests include device modeling, characterization, and circuit benchmark for design-enabled advanced CMOS technology scaling.



Luca Mattii is an electrical engineer working as a corporate consultant for Cadence Design Systems, currently supporting imec on physical implementation at advanced nodes. He received his BS and MS degrees in electronic engineering from the University of Pisa in 2011 and 2014, respectively, and he is now also enrolled in an industrial PhD at Braunschweig University. His current research interests include advanced nodes, design-technology co-optimization, and EDA.



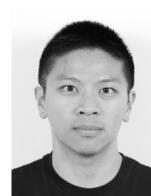
Syed Muhammed Yasser Sherazi received his BSc degree in computer engineering from COMSATS Institute of Information Technology, Islamabad, Pakistan, in 2005, and a master's degree in system-on-chip from Linköping University, Linköping, Sweden, in 2008. In 2014, he completed his PhD in digital ASIC design from the EIT Department, Lund University, Lund, Sweden, where he worked on design space analysis and construction of ultralow energy digital circuits focusing on digital base-band for wireless devices. He is currently working as a postdoc in IMEC, Belgium, where he is looking into digital gates and design technology co-optimization for 10- and 7-nm technologies.



Dimitrios Rodopoulos completed a Dual Doctorate between NTUA, Greece and KU Leuven, Belgium, on reliable integrated circuit design in 2016. During his PhD, he served as Principle Investigator on the Intel SCC chip, supervised more than 10 NTUA Thesis students and contributed to European Commission projects HARPA, VINEYARD and TRAMS, as well as the Erasmus Brain Project. He has co-authored more than 30 papers and 5 EPO/USPTO applications. Since February 2016, Dimitrios serves as RnD Engineer at imec, Belgium, focusing on design enablement of future technology nodes and design of machine learning chips with non-volatile memories.



Romain Ritzenthaler (M'09) received the M.Sc. degree from the Ecole Nationale Supérieure de Physique de Grenoble, Grenoble, France, in 2003, and the Ph.D. degree from the Institut National Polytechnique de Grenoble, Grenoble, and the Laboratoire d'Électronique et Technologies de l'Information, Grenoble, in 2006. Since 2011, he has been a Device Engineer with imec, Leuven, Belgium, where he is involved in the process and characterization of DRAM periphery and bulk FinFET transistors.



Chi-Shuen Lee received the B.S. degree from National Taiwan University, Taipei, Taiwan in 2011, and the Ph.D. degree from Stanford University, CA, in 2018, both in electrical engineering. His research interests include modeling and simulation of nanoscale MOSFETs and CMOS technology benchmarking.



Aaron Voon-Yew Thean is a Professor of Electrical and Computer Engineering at the National University of Singapore (NUS). He is also a consulting Fellow to IMEC, a Nano-electronic Research Center, based in Belgium. Prior to joining NUS in 2016, Aaron served as IMEC's Vice President of Logic Technologies and the Director of the Logic Devices Research. At IMEC, he directed the research and development of advanced device technologies ranging from ultra-scaled FinFETs, Nanowire FETs, to III-V/Ge Channels, Tunnel FETs to emerging Beyond CMOS logic nano-device architectures based on Spintronics and 2-D materials. He has been involved in Design and Process Technology Co-optimizations (DTCO) of emerging technologies targeting 7nm, 5nm, and beyond. Before 2011, he was with Qualcomm's CDMA technologies in San Diego, California, USA.

Aaron graduated from the University of Illinois at Champaign-Urbana, USA, where he received his B.Sc. (Highest Honors & Graduated as Edmund J. James' Scholar), M.Sc., and Ph.D. degrees in Electrical Engineering. He has published over 300 technical papers and holds more than 50 U.S. patents



Iuliana Radu received the B.Sc. and M.Sc. degrees from the University of Bucharest, Bucharest, Romania, and the Ph.D. degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2009, all in physics. She is currently the Manager with the Logic Program, imec, Leuven, Belgium, where she is leading the Beyond CMOS activities. She has authored over 30 papers in leading peer-reviewed journals and conferences.



Alessio Spessot received his M.S. degree (“magna cum laude”) in Physics from the University of Trieste, Italy in 2003 and the Ph.D. degree in Solid State Physics from the University of Modena, Italy, in 2007. He earned an EMBA from Vlerick Business School (Belgium) in 2014 with great distinction. He worked for STMicroelectronics (from 2006), Numonyx (from 2008), and Micron (from 2010). As from 2016, he is managing the imec Insite program, which focus on establishing roadmap for emerging logic technologies. His current interest are Design Technology Co Optimization (DTCO) and System Technology Co Optimization for Logic and memories. Dr Spessot has authored or co-authored more than 90 papers, and holds 10 issued patents. He served as member of E-MRS Scientific Committee, reviewer for IEEE and Elsevier, and technical expert for European projects.



Peter Debacker (M) received the M.Sc. (Hons.) degree in electrical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 2004. He was with Essensium, Leuven. He joined IMEC, Leuven, in 2011, where he is currently a R&D Team Leader in the Semiconductor Technology and Systems division. He leads a team that evaluates key power-performance-area (PPA) benefits of scaled CMOS technologies (5nm, 3nm and beyond) and beyond CMOS technologies, and develops technology, architecture and algorithms for various machine learning techniques like ConvNets, Temporal Predictions, Anomaly Prediction etc. In his past he has worked on IMEC’s low-power digital chip and processor architectures and implementation in advanced technology nodes. His current research interests include machine learning and neuromorphic computing, computer architectures, design methodologies, design-technology co-optimization, reliability, variability and low power design.



Francky Catthoor received the engineering degree and Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium in 1982 and 1987 respectively. Between 1987 and 2000, he has headed several research domains in the area of high-level and system synthesis techniques and architectural methodologies. Since 2000 he is also strongly involved in other activities at IMEC including related application and deep submicron technology aspects, biomedical imaging and sensor nodes, and smart photo-voltaic modules, all at the Inter-university Micro-Electronics Center (IMEC), Heverlee, Belgium. Currently he is an IMEC fellow. He is part-time full professor at the EE department of the K. U. Leuven. In 1986, he received the Young Scientist Award from the Marconi International Fellowship Council. He has been associate editor for several IEEE and ACM journals, like Trans. on VLSI Signal Processing, Trans. on Multi-media, and ACM TODAES. He was the program chair of several conferences including ISSS’97 and SIPS’01. He has been elected an IEEE fellow in 2005.



Praveen Raghavan obtained his PhD from KU Leuven in 2009 and his Masters from Arizona State University, USA. He received his Bachelor’s Degree in Electrical Engineering from Regional Engineering College Trichy, India. In 2007, he was also a visiting researcher at Berkeley Wireless Research Center (BWRC), University of Berkeley, California. He is currently leads the group for design enabled technology exploration at IMEC, where he manages the research on device-design co-optimization on CMOS and beyond CMOS technologies. In his past he has been the lead architect of IMEC’s multi-gigabit software-defined radio baseband chip set. His research interests include DTCO, PPAC, Device modeling, design methodologies, reliability, variability and low power design. He has published over 150 conference and journal papers and holds more than 30 patents.



Max M. Shulaker is a Professor with the Department of EECS at MIT, where he leads the Novel Electronic Systems Group (NOVELS). His research interests include the broad area of nanosystems. His research group focuses on understanding and optimizing multidisciplinary interactions across the entire computing stack – from low-level synthesis of nanomaterials, to fabrication processes and circuit design for emerging nanotechnologies, up to new architectures – to enable the next generation of high-performance and energy-efficient computing systems. His group focuses on practically implementing new technologies to enable useful and impactful applications;

the group has successfully performed technology transfer with industrial fabrication facilities. He personally designed and fabricated the most complex nanosystems to-date, including multiple demonstrations of monolithic 3D ICs leveraging CNFETs and RRAM.



H.-S. Philip Wong is the Willard R. and Inez Kerr Bell Professor in the School of Engineering. He joined Stanford University as Professor of Electrical Engineering in September, 2004. From 1988 to 2004, he was with the IBM T.J. Watson Research Center.

At IBM, he held various positions from Research Staff Member to Senior Manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM’s strategy on nanoscale science and technology as well as exploratory silicon devices and semiconductor technology. During his time at IBM, he managed pathfinding research on high-k/metal gate, strained silicon, alternative channel materials such as Ge and III-V, multi-gate FinFET, ultra-thin SOI – many of these have now become product technology at various companies.

Professor Wong’s research aims at translating discoveries in science into practical technologies. His works have contributed to advancements in nanoscale science and technology, semiconductor technology, solid-state devices, and electronic imaging. His present research covers a broad range of topics including carbon electronics, 2D layered materials, wireless implantable biosensors, directed self-assembly, device modeling, brain-inspired computing, non-volatile memory, and monolithic 3D integration.

He is a Fellow of the IEEE. He served as the Editor-in-Chief of the IEEE Transactions on Nanotechnology (2005 – 2006), sub-committee Chair of the ISSCC (2003 – 2004), General Chair of the IEDM (2007), and is currently the Chair of the IEEE Executive Committee of the Symposia of VLSI Technology and Circuits. He is the faculty director of the Stanford Non-Volatile Memory Technology Research Initiative (NMTRI), and is the founding Faculty Co-Director of the Stanford SystemX Alliance – an industrial affiliate program focused on building systems.



Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University, where he directs the Stanford Robust Systems Group and co-leads the Computation focus area of the Stanford SystemX Alliance. He is also a faculty member of the Stanford Neurosciences Institute. Prof. Mitra holds the Carnot Chair of Excellence in Nanosystems at CEA-LETI in Grenoble, France. Before joining the Stanford faculty, he was a Principal Engineer at Intel Corporation.

Prof. Mitra’s research interests range broadly across robust computing, nanosystems, VLSI design, validation, test and electronic design automation, and neurosciences. He, jointly with his students and collaborators, demonstrated the first carbon nanotube computer and the first three-dimensional nanosystem with computation immersed in data storage. These demonstrations received wide-spread recognitions (cover of NATURE, Research Highlight to the United States Congress by the National Science Foundation, highlight as “important, scientific breakthrough” by the BBC, Economist, EE Times, IEEE Spectrum, MIT Technology Review, National Public Radio, New York Times, Scientific American, Time, Wall Street Journal, Washington Post and numerous others worldwide). His earlier work on X-Compact test compression has been key to cost-effective manufacturing and high-quality testing of almost all electronic systems. X-Compact and its derivatives have been implemented in widely-used commercial Electronic Design Automation tools.

Prof. Mitra’s honors include the ACM SIGDA/IEEE CEDA A. Richard Newton Technical Impact Award in Electronic Design Automation (a test of time honor), the Semiconductor Research Corporation’s Technical Excellence Award, the Intel Achievement Award (Intel’s highest corporate honor), and the Presidential Early Career Award for Scientists and Engineers from the White House (the highest United States honor for early-career outstanding scientists and engineers). He and his students published several award-winning papers at major venues: ACM/IEEE Design Automation Conference, IEEE International Solid-State Circuits Conference, IEEE International Test Conference, IEEE Transactions on CAD, IEEE VLSI Test Symposium, and the Symposium on VLSI Technology. At Stanford, he has been honored several times by graduating seniors “for being important to them during their time at Stanford.”

Prof. Mitra served on the Defense Advanced Research Projects Agency’s (DARPA) Information Science and Technology Board as an invited member. He is a Fellow of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE).