Project 3 - Report

ELECENG 2EI4 Dr. Yaser Haddara

March 23rd, 2025 Edison He (400449140)

As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by [Edison He,hee6, 400449140]

Appear on the video stating your name and the date of the recording.

- 2. (3 minutes) Share your screen to show your circuit schematic. Explain:
- a. (5) What type of transistor did you choose (MOSFET/BJT)? Why?

I decided to go with a npn BJT circuit rather than a mosfet circuit. This is because BJT circuits are able to achieve a higher gain which in this case should be near 1. BJTs also have a more linear gain in the forward active mode in addition to a lower input resistance. This makes them more ideal for high frequency low voltage applications.

b. (5) What amplifier topology (CE/CS/CD/etc.) did you choose? Why?

I used a common collector topology instead over the common emitter and common base topologies. This provides a moderate to high input resistance which eliminates the common base topology. It also allows for a gain close to 1 which adheres to the project specification. This is and its ability to be used with large voltage swings is beneficial to the voltage range of +- 5V

c. (5) What calculations did you use to determine the required component values?

Step 1

Using the design constraints and the common collector topology, I determined that Gm should be greater than 990.

Step 2 is to determine the input resistance Rn

Given that the gain must be greater than 0.9, I calculated Rn must be greater than 1k Ohm

Step 3 is to select resistance values for R1 and R2

Using small signal analysis, I found that Rin was parallel to R1 and R2. After solving, I determined that R1 and R2 are both equal to 10K ohms which satisfies the constraints.

Step 4 is solving the capacitor values.

These values were chosen experimentally. This is as these capacitors are primarily used as decoupling capacitors. In addition, their values do not impact the small signal operations

- 3. (5 minutes) Share your screen to show your simulations. Explain:
- a. (5) How did you model the transistor in the simulator you used?
- b. (5) What settings did you use for each simulation (transient/dc sweep/frequency sweep/etc.)?
- c. (5) The overall gain determined from the simulations.

to

- d. (5) Other performance parameters determined from the simulations.
- 4. (2 minutes) Show your physical circuit on camera. Point to the wires from input to output

show how the circuit is connected in a way corresponding to your schematic.

- 5. (5 minutes) Share your screen to show your waveforms measurements. Explain:
- a. (5) What measurements did you do? (E.g. waveforms as functions of time, XY plot, network analyzer, etc. You decide which measurements are beneficial and explain why you used them.)
- b. (5) How did you determine the midband gain for your amplifier? What value did you obtain? Compare your value with what was expected from calculations and simulations.
- c. (5) Demonstrate linearity at an input amplitude of 0.5V.

$$A_{v} = \frac{g_{m}R_{L}}{1+g_{m}R_{L}} \left(\frac{R_{in}}{R_{t}+R_{in}}\right)$$

$$0.9 \le \frac{g_{m}R_{L}}{1+g_{m}R_{L}}$$

$$g_{m} \ge 90mS$$

$$V_{in} = 0.2V_{T}(1+g_{m}R_{L}) \ge 0.5mS$$

$$0.2(0.025)(1+g_{m}(100)) \ge 0.5mS$$

$$g_{m} \ge 990S$$

Input Resistance

$$0.9 \le \frac{g_{m}R_{L}}{1+g_{m}R_{L}} \left(\frac{R_{in}}{R_{t}+R_{in}}\right)$$

$$R_{in} \ge 900\Omega$$

Component Values

$$\begin{split} R_{in} &= R_{eq} || (R_{\pi}(1 + g_m R_L)) \\ R_{\pi} &= \frac{\beta}{g_m} = \frac{100}{0.99} = 101\Omega \\ R_{in} &= R_{eq} || (R_{\pi}(1 + g_m R_L)) \\ 900 &= R_{eq} || (100(1 + 0.99(100))) \\ R_{eq} &\geq 988 \\ A_v &= 0.923 \end{split}$$