Project 4 - Report

ELECENG 2EI4

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Edison He,hee6, 400449140]**

Circuit Schematic

The circuit schematic used in this project used 12 MOSFETS, 6 PMOS and 6 NMOS. The figures 4 and 5 below show the circuit schematics that represent the XOR gate in CMOS in addition to an inverter. MOSFET transistors were used as they act like voltage controlled switches. For the pull down network, DeMorgan's theorem was used to derive a boolean expression for an XOR gate.

$$Y = A \oplus B = A'B + B'A = (A'B + B'A)''$$
$$= ((A'B)' + (B'A)')' = ((A + B') \cdot (B + A'))'$$
$$= ((AB + (AB)')'$$

This means the pull down network would include A in series with B. This would be in parallel with A' in series with B'. In the pull down network, the structure would be the same. The PDN uses 4 N-MOS transistors and the PUN uses 4 PMOS transistors. In addition, 2 more CMOS inverters are needed for complemented inputs. Therefore 2 NMOS and 2 PMOS transistors were needed additionally.

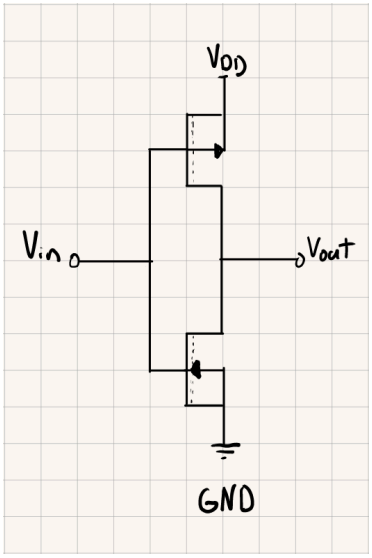

Figure 1: CMOS Inverter

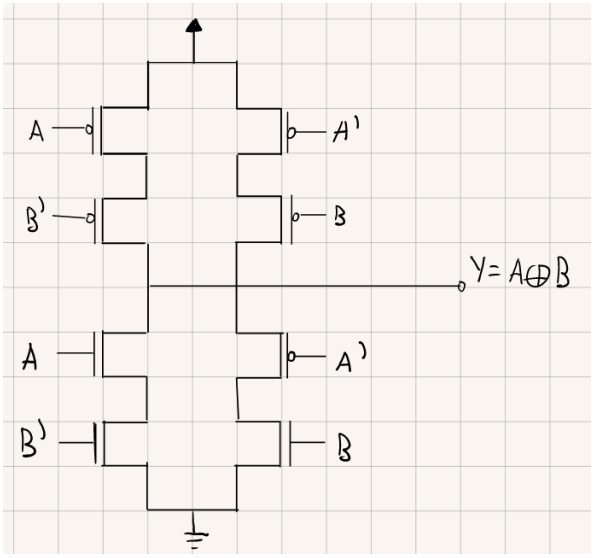

Figure 2: CMOS XOR Gate

Ideal Sizing

The average size for a PMOS is $(\frac{W}{L})_P = (\frac{5}{1})$ and the average sizing for an NMOS is $(\frac{W}{L})_N = (\frac{2}{1})$. The longest path in the PDN and PUD travels through 2 MOSFETs. Therefore, R_{eq} for the entire path is $\frac{n}{2}$ and $\frac{p}{1}$ for the pulldown and pullup networks respectively. A ratio of 1:1 will ensure symmetry between both networks and a shortest delay possible. Finally, we know that R is inversely proportional to sizing. This means that the size of the P and N MOSFETs must

be doubled in comparison to the reference inverter. The ideal ratio can be found with $\frac{2\times PMOS}{2\times NMOS} = \frac{5}{2} = 2.5$.

Feasibility of Ideal Sizing

The circuit schematic has 2 PMOS transistors and 2 NMOS transistors. This path is from VDD to GND meaning that the sizing for this circuit is also $\frac{2\times PMOS}{2\times NMOS} = \frac{5}{2} = 2.5$, the same value as the ideal sizing. Because of this, the design will be feasible to implement and that symmetry will help play a role in the implementation.

Physical Circuit

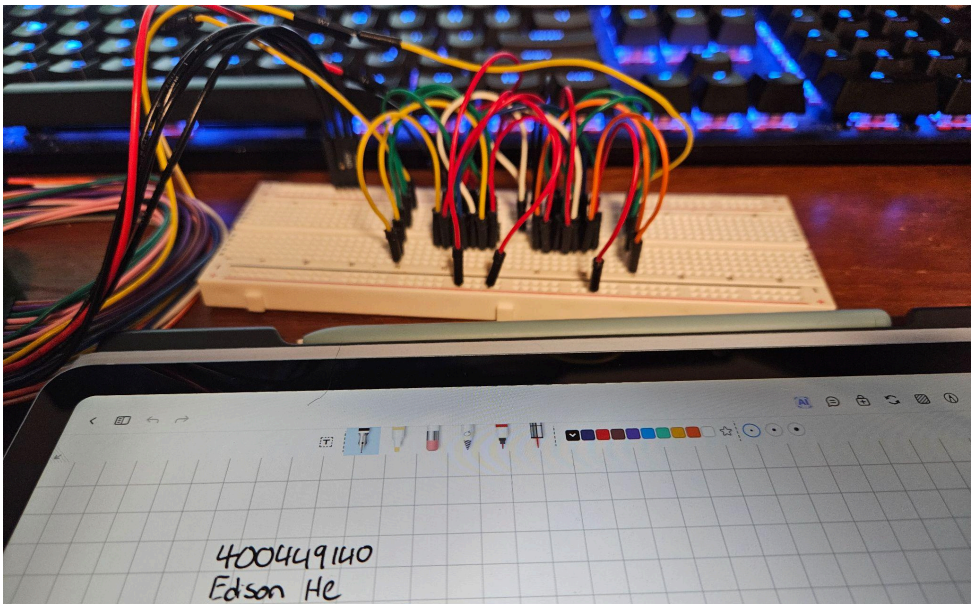

Figure 3: Physical Circuit

Functional Testing

The functionality of the circuit is shown in both figures below. DIO 0 and DIO1 represent A and B respectively. DIO2 represents the output given by XOR resulting from DIO 0 and 1. DIO 0 was set to 1kHz while DIO1 was set to 2kHz. DIO 2 from left to right in Figure 5 verifies the XOR truth table in Figure 4.

A	B	Output
0	0	0
1	0	1
0	1	1
1	1	0

Figure 4: XOR Truth Table

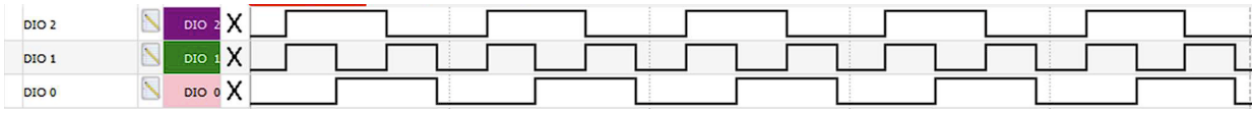

Figure 5: AD3 output

Static Level Testing

Figure 5 below represents input A using 5V and B between 0V and 5V in a square wave. It can be seen below that V_L has a value of around -9.24 mV and V_H has a value of around 4.01V. When the inputs A and B were switched, it can be seen that V_L is -9.26 mV and V_H is 4.016V. This reveals that the values stayed the same when compared to the original measurement. In other words, the value of VH and VL did not change.

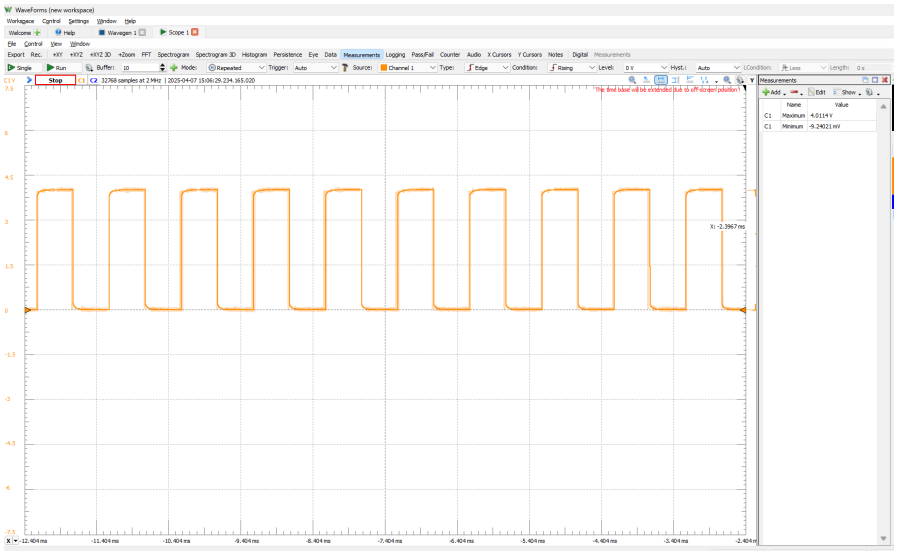

Figure 6: Output, Input A 5V, B 0V-5V Square Wave

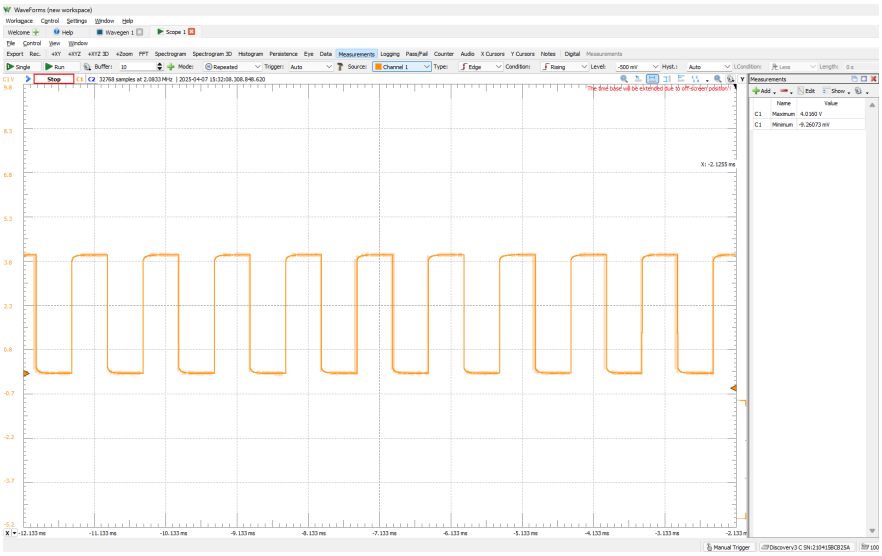

Figure 7: Output, Input 5V, B 0V-5V Square Wave

Timing

The rise and fall times were 81.3 us and 184.9 us. This was done by adding a 100nF load capacitor. W1 was set to 5V and W2 was a square wave from 0V to 5V. The results can be seen below in Figure 8.

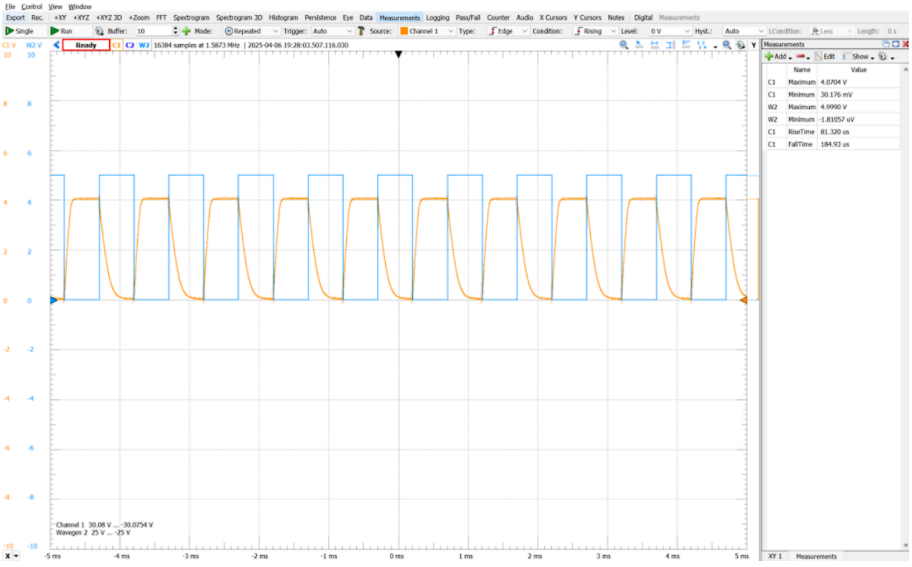

Figure 8: Time Constant Parameters

Time Constant Parameters

Figure 8 above was used to calculate the additional parameters. Once again, the rise and fall times are 81.3 us and 184.9 us respectively. The propagation delay for both low to high and high to low can be estimated by using the fall and rise times.

τ_{phl} = 184.9 us τ_{plh} = 81.3 us

$$\tau_p = \frac{\tau_{phl} + \tau_{plg}}{2} = \frac{184.9 + 81.3}{2} = 133.1\ us$$