

MOSFET – P-Channel, QFET

-150 V, -3 A, 1.5 Ω

FDMC2523P

General Description

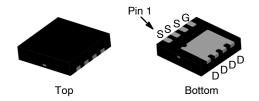
These P-Channel MOSFET enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC-DC converters, and DC motor control.

Features

- Max $R_{DS(on)} = 1.5 \Omega$ at $V_{GS} = -10 \text{ V}$, $I_D = -1.5 \text{ A}$
- Low C_{rss} (Typical 10 pF)
- Fast Switching
- Low Gate Charge (Typical 6.2 nC)
- Improved dv / dt Capability
- This Device is Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

• Active Clamp Switch

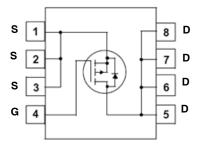


WDFN8 3.3x3.3, 0.65P CASE 511DH

MARKING DIAGRAM

ZXYKK 2523P

Z = Assembly Plant Code
XY = Date Code (Year &Week)
KK = Lot Traceability Code
2523P = Specific Device Code



ORDERING INFORMATION

Device	Package	Shipping [†]
FDMC2523P	WDFN8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1

MOSFET MAXIMUM RATINGS ($T_A = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter			Ratings	Unit
V _{DS}	Drain to Source Voltage			-150	٧
V_{GS}	Gate to Source Voltage			±30	V
I _D	Drain Current Continuous T _C = 25°C		-3	А	
		Continuous	T _C = 100°C	-1.8	1
		Pulsed	-	-12	1
P_{D}	Power Dissipation (Steady State) T _C = 25°C			42	W
E _{AS}	Single Pulse Avalanche Energy (Note 5)			3.3	mJ
T _J , T _{STG}	Operating and Storage Junction Temperature Range			−55 to +150	°C
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C
dv/dt	Peak Diode Recovery dv/dt	(Note 2)		- 5	V/ns

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	60	

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
		rest conditions	IVIIII	קעי	IVIAA	Oilit
OFF CHARA	CTERISTICS					
BV _{DSS}	Drain-to-Source Breakdown Voltage	$I_D = -250 \ \mu A, \ V_{GS} = 0 \ V$	-150	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage $I_D = -250~\mu A$, referenced to 25°C Temperature Coefficient		-	-138	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -150 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	-1	μΑ
		V_{DS} = -150 V, V_{GS} = 0 V, T_J = 125 °C	-	-	-10	μΑ
I _{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA
ON CHARAC	ON CHARACTERISTICS					
V _{GS(th)}	Gate-to-Source Threshold Voltage	ource Threshold Voltage V _{GS} = V _{DS} , I _D = -250 μA		-3.8	-5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25°C	-	6	-	mV/°C
R _{DS(on)}	Static Drain-to-Source	$V_{GS} = -10 \text{ V}, I_D = -1.5 \text{ A}$	-	1.1	1.5	Ω
	On Resistance	$V_{GS} = -10 \text{ V}, I_D = -1.5 \text{ A}, T_J = 125^{\circ}\text{C}$	-	2.0	3.6]
9FS	Forward Transconductance	$V_{DS} = -40 \text{ V}, I_D = -1.5 \text{ A (Note 4)}$	-	1.4	-	S
DYNAMIC C	HARACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	200	270	pF
C _{oss}	Output Capacitance		-	60	80	
C _{rss}	Reverse Transfer Capacitance		-	10	15	
R_g	Gate Resistance	f = 1 MHz	0.1	7.5	15	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
SWITCHING	CHARACTERISTICS	•				
t _{d(on)}	Turn-On Delay Time	V_{DD} = -75 V, I_{D} = -3 A, V_{GS} = -10 V, R_{GEN} = 25 Ω (Note 3, 4)	_	15	27	ns
t _r	Rise Time		-	11	20	
t _{d(off)}	Turn-Off Delay Time		_	19	35	
t _f	Fall Time		_	13	24	
Qg	Total Gate Charge	$V_{GS} = -10 \text{ V}, V_{DD} = -75 \text{ V}, I_D = -3 \text{ A}$	_	6.2	9	nC
Q _{gs}	Gate-to-Source Charge	(Note 3, 4)	-	1.4	-	
Q_{gd}	Gate-to-Drain "Miller" Charge		_	3.3	-	

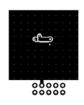
DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain - Source Diode Forward Current		-	-	-3	Α
I _{SM}	Maximum Pulse Drain - Source Doide Forward Current		-	-	-12	
V _{SD}	Source–to–Drain Diode Forward $V_{GS} = 0 \text{ V}, I_S = -3.0 \text{ A}$ Voltage		ı	-1.8	-5	V
t _{rr}	Reverse Recovery Time	I _F = -3.0 A, di/dt = 100 A/μs (Note 3)	-	93	_	ns
Q _{rr}	Reverse Recovery Charge		_	0.27	_	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. R_{0JA} is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta,IC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 60°C/W when mounted on a 1 in² pad of 2 oz copper



b) 135°C/W when mounted on a minimum pad of 2 oz copper

- 2. $I_{SD} \le -3$ A, $dI/dt \le 300$ A/ μ s, $V_{DD} \le B_{VDSS}$, Starting $T_J = 25^{\circ}C$.
 3. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
 4. Essentially independent of operating temperature.

- 5. E_{AS} of 3.3 mJ is based on starting $T_J = 25$ °C, P-ch: L = 3 mH, $I_{AS} = -1.5$ A, $V_{DD} = -150$ V, $V_{GS} = -10$ V.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

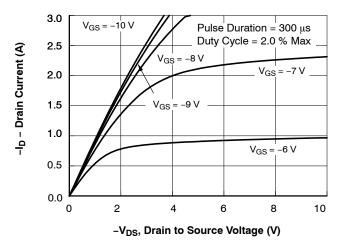


Figure 1. On-Region Characteristics

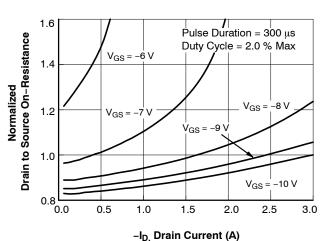


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

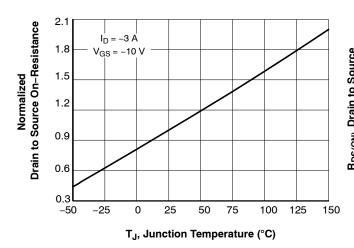


Figure 3. Normalized On-Resistance vs. Junction Temperature

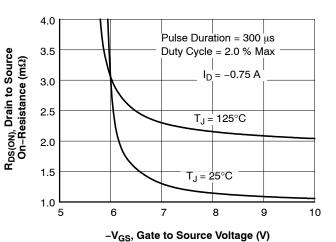


Figure 4. On-Resistance vs.
Gate to Source Voltage

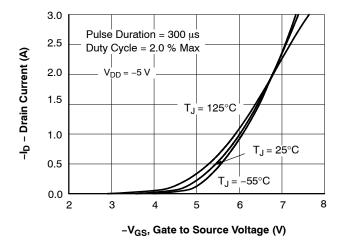
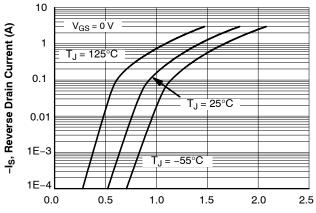


Figure 5. Transfer Characteristics



-V_{SD}, Body Diode Forward Voltage (V)

Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

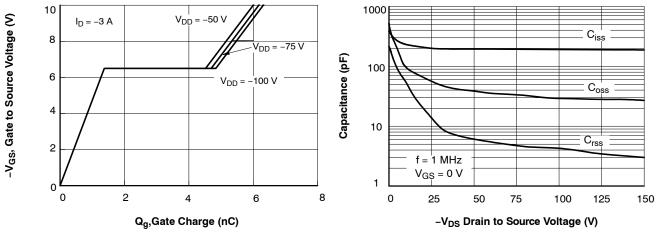


Figure 7. Gate Charge Characteristics



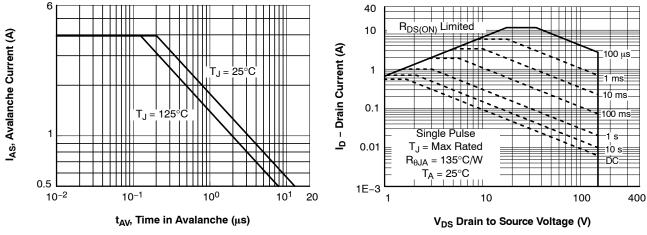


Figure 9. Unclamped Inductive Switching Capability

Figure 10. Forward Bias Safe Operating Area

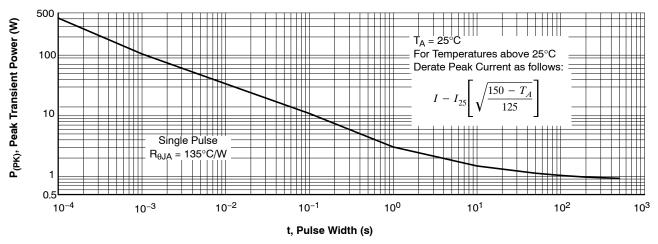


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

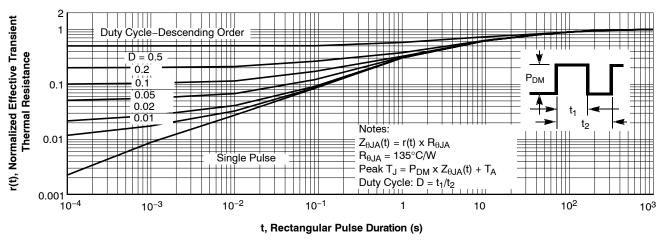
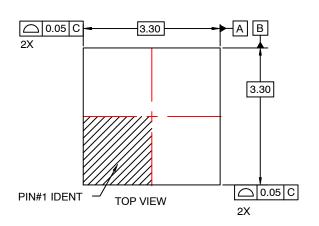


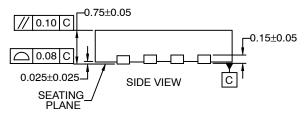
Figure 12. Transient Thermal Response Curve

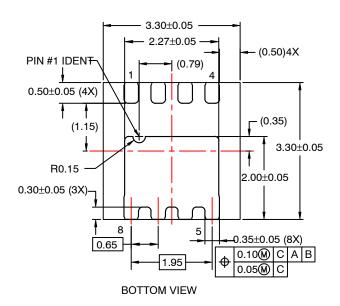


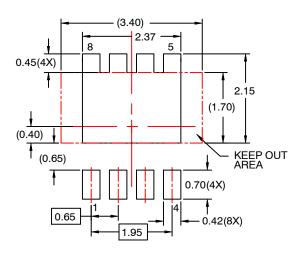
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DATE 31 JUL 2016









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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