Eletrônica Digital II

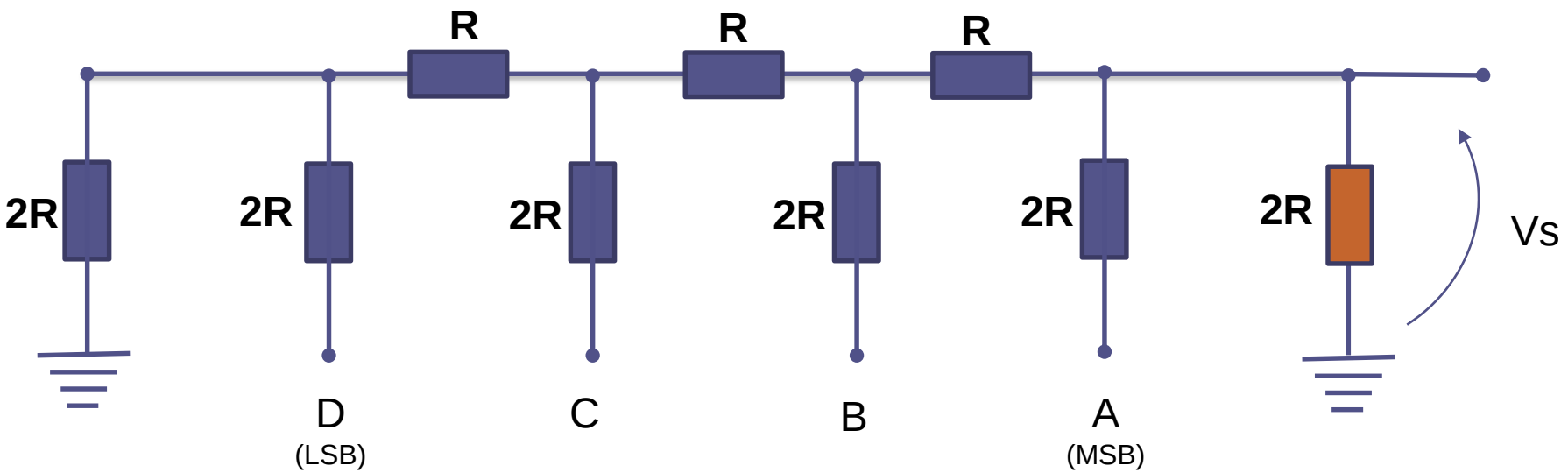
Aula M – Exercício de Conversor D/A com Contador Síncrono

Prof. MSc. Bruno de Oliveira Monteiro

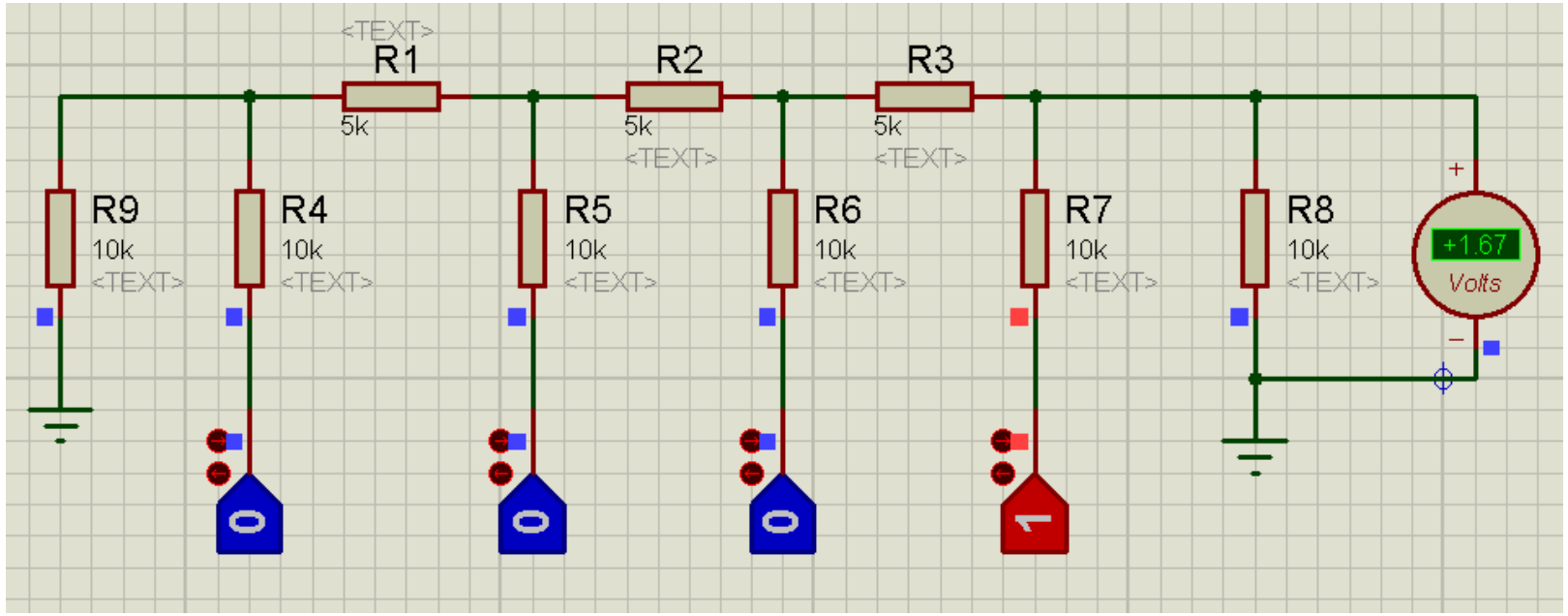
Inatel

Conversor Digital/Analógico – Rede R-2R

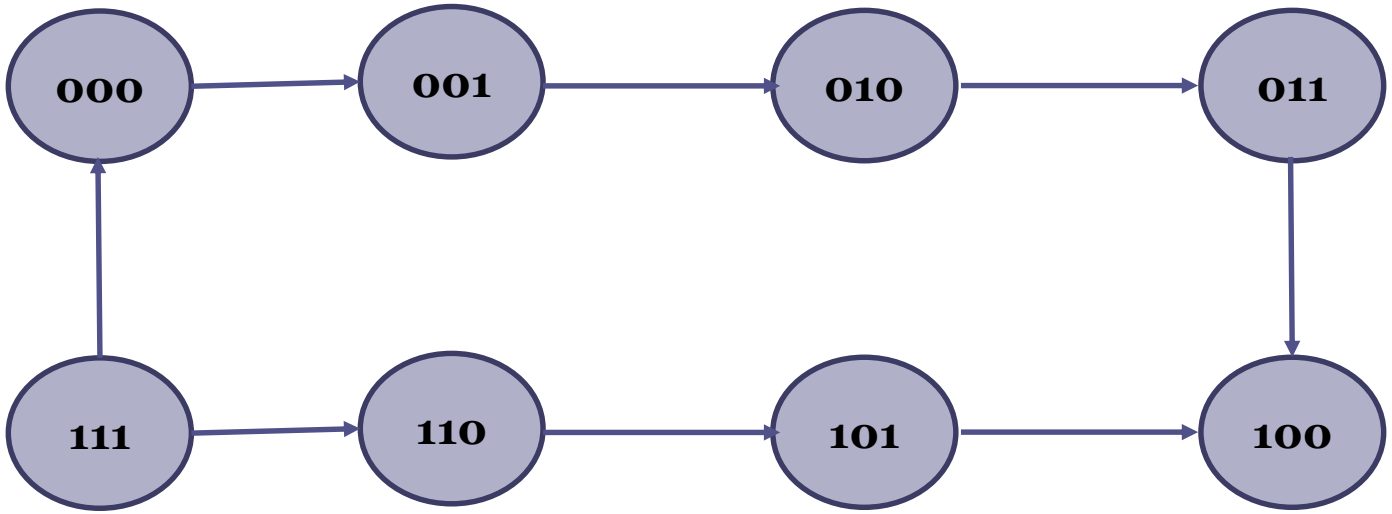
O circuito de conversão Digital / Analógico usando Rede R-2R



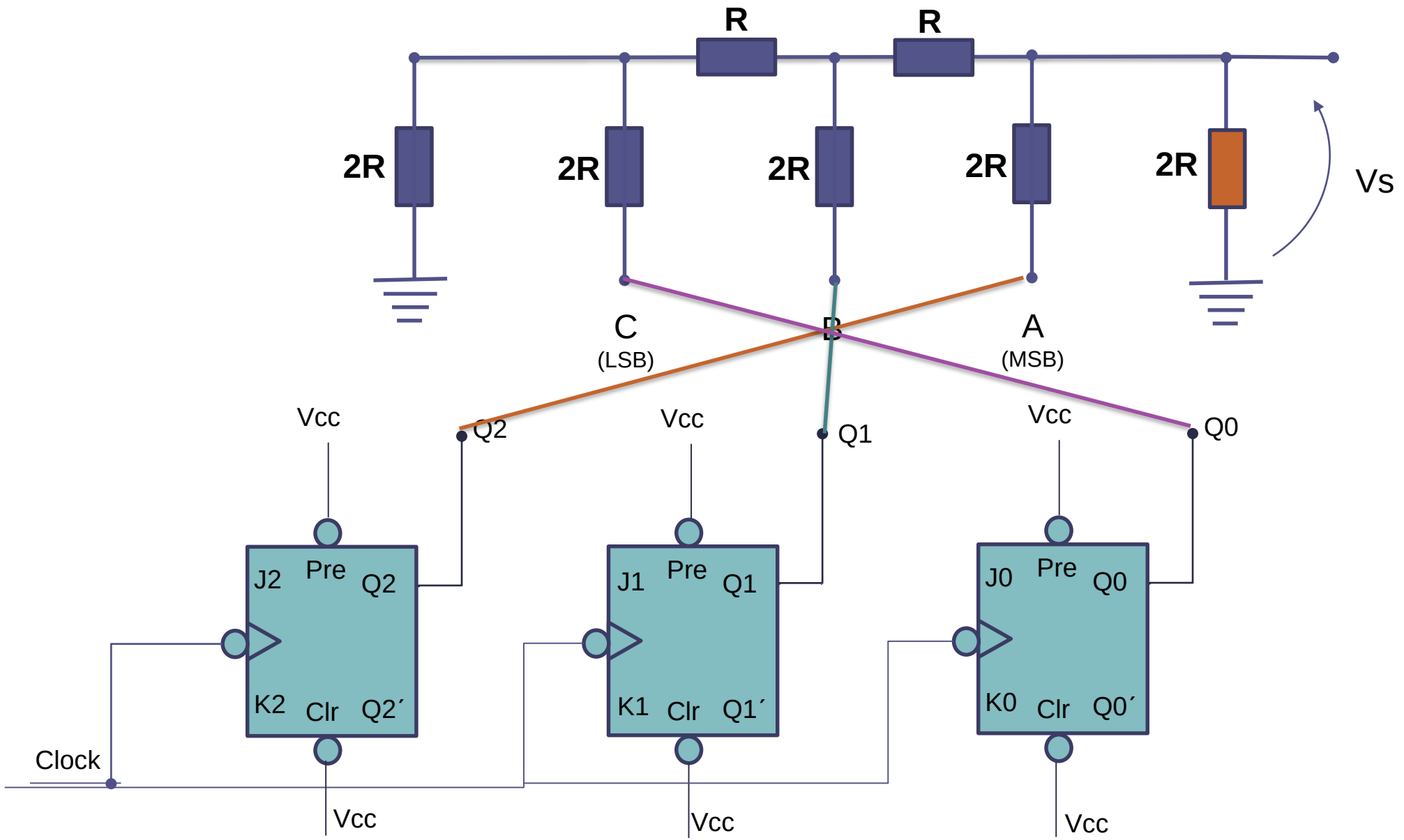
Conversor Digital/Analógico – Rede R-2R



Exercício:
Desenvolva um circuito contador Síncrono capaz de realizar o Diagrama de estado abaixo



Máquina de Estado

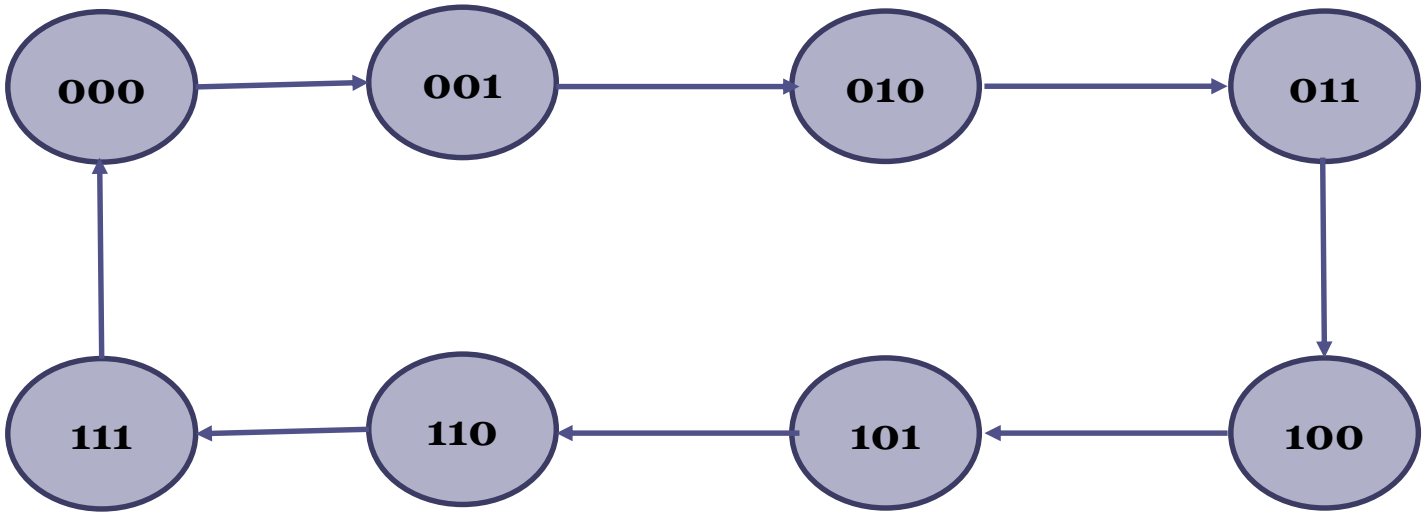


Máquina de Estado

Exercício:
Complete o exercício, elaborando todo o circuito da máquina de estado, montando o circuito no Proteus e avaliando o sinal gerado na saída Vs

Máquina de Estado

Exercício:



1° Passo:

Estado Anterior (Qa)			Estado Final (Qf)		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Máquina de Estado

2°Passo: Vamos montar a tabela de alimentação das entradas dos FF-JK, de acordo com a tabela do Qa e Qf dos estados;

Qa	Qf	J	K
0	0	0	*
0	1	1	*
1	0	*	1
1	1	*	0

Estado Anterior (Qa)			Estado Final (Qf)			FF-JK(2)		FF-JK(1)		FF-JK(0)	
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1						
0	0	1	0	1	0						
0	1	0	0	1	1						
0	1	1	1	0	0						
1	0	0	1	0	1						
1	0	1	1	1	0						
1	1	0	1	1	1						
1	1	1	0	0	0						

Máquina de Estado

3°Passo: Montar o Mapa de Karnaught de cada saída:

Estado Anterior (Qa)			Estado Final (Qf)			FF-JK(2)		FF-JK(1)		FF-JK(0)	
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	*	0	*	1	*
0	0	1	0	1	0	0	*	1	*	*	1
0	1	0	0	1	1	0	*	*	0	1	*
0	1	1	1	0	0	1	*	*	1	*	1
1	0	0	1	0	1	*	0	0	*	1	*
1	0	1	1	1	0	*	0	1	*	*	1
1	1	0	1	1	1	*	0	*	0	1	*
1	1	1	0	0	0	*	1	*	1	*	1

J2

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	0	0	1	0
Q2	*	*	*	*

J2=Q1Q0

K2

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	*	*	*	*
Q2	0	0	1	0

K2=Q1Q0

J1

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	0	1	*	*
Q2	0	1	*	*

J1=Q0

Máquina de Estado

3°Passo: Montar o Mapa de Karnaught de cada saída:

Estado Anterior (Qa)			Estado Final (Qf)			FF-JK(2)		FF-JK(1)		FF-JK(0)	
Q2	Q1	Q0	Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0	0	0	1	0	*	0	*	1	*
0	0	1	0	1	0	0	*	1	*	*	1
0	1	0	0	1	1	0	*	*	0	1	*
0	1	1	1	0	0	1	*	*	1	*	1
1	0	0	1	0	1	*	0	0	*	1	*
1	0	1	1	1	0	*	0	1	*	*	1
1	1	0	1	1	1	*	0	*	0	1	*
1	1	1	0	0	0	*	1	*	1	*	1

K1

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	*	*	1	0
Q2	*	*	1	0

K1=Q0

J0

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	1	*	*	1
Q2	1	*	*	1

J0=1

K0

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	*	1	1	*
Q2	*	1	1	*

K0=1

Máquina de Estado

4°Passo: Montar o circuito

J2=Q1Q0

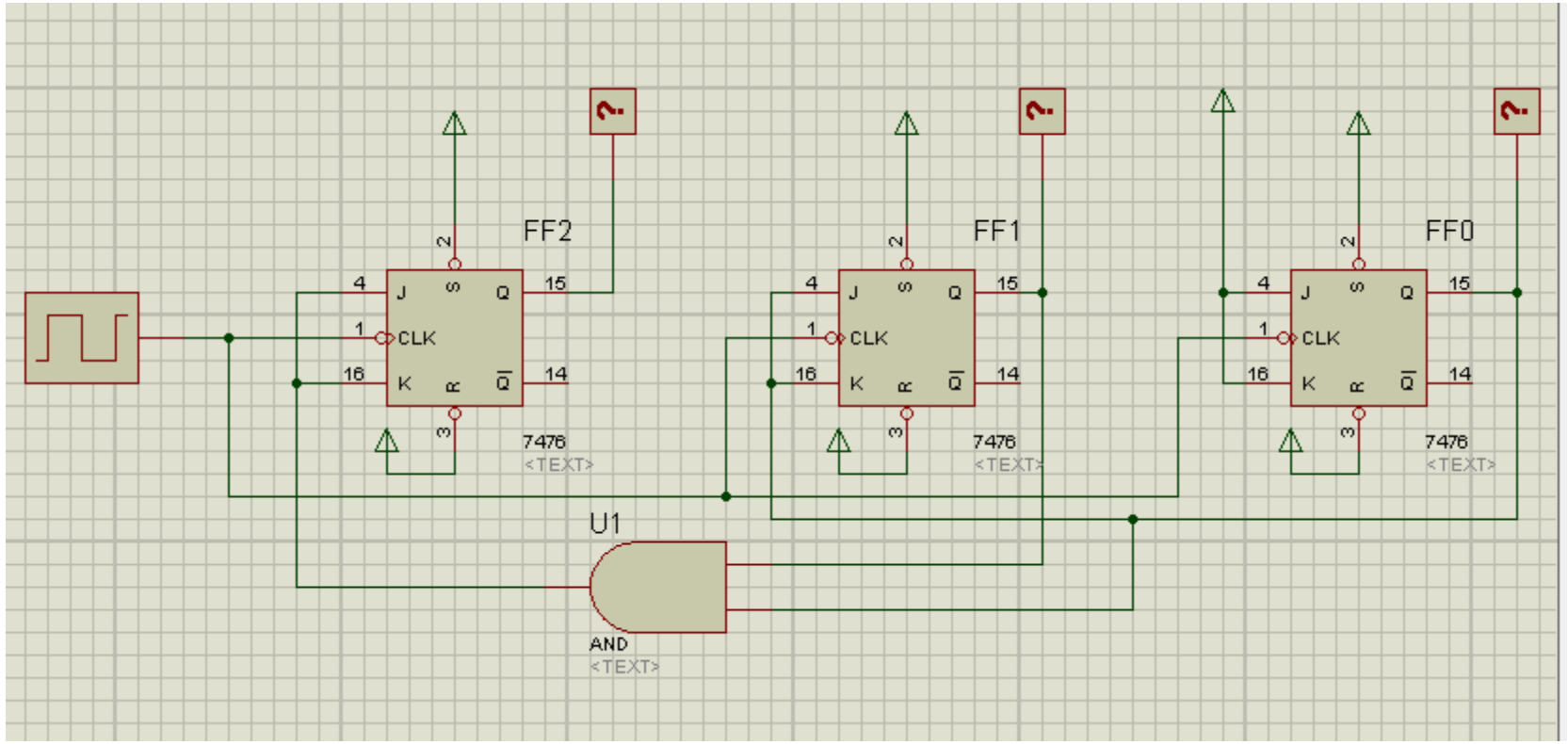
K2=Q1Q0

J1=Q0

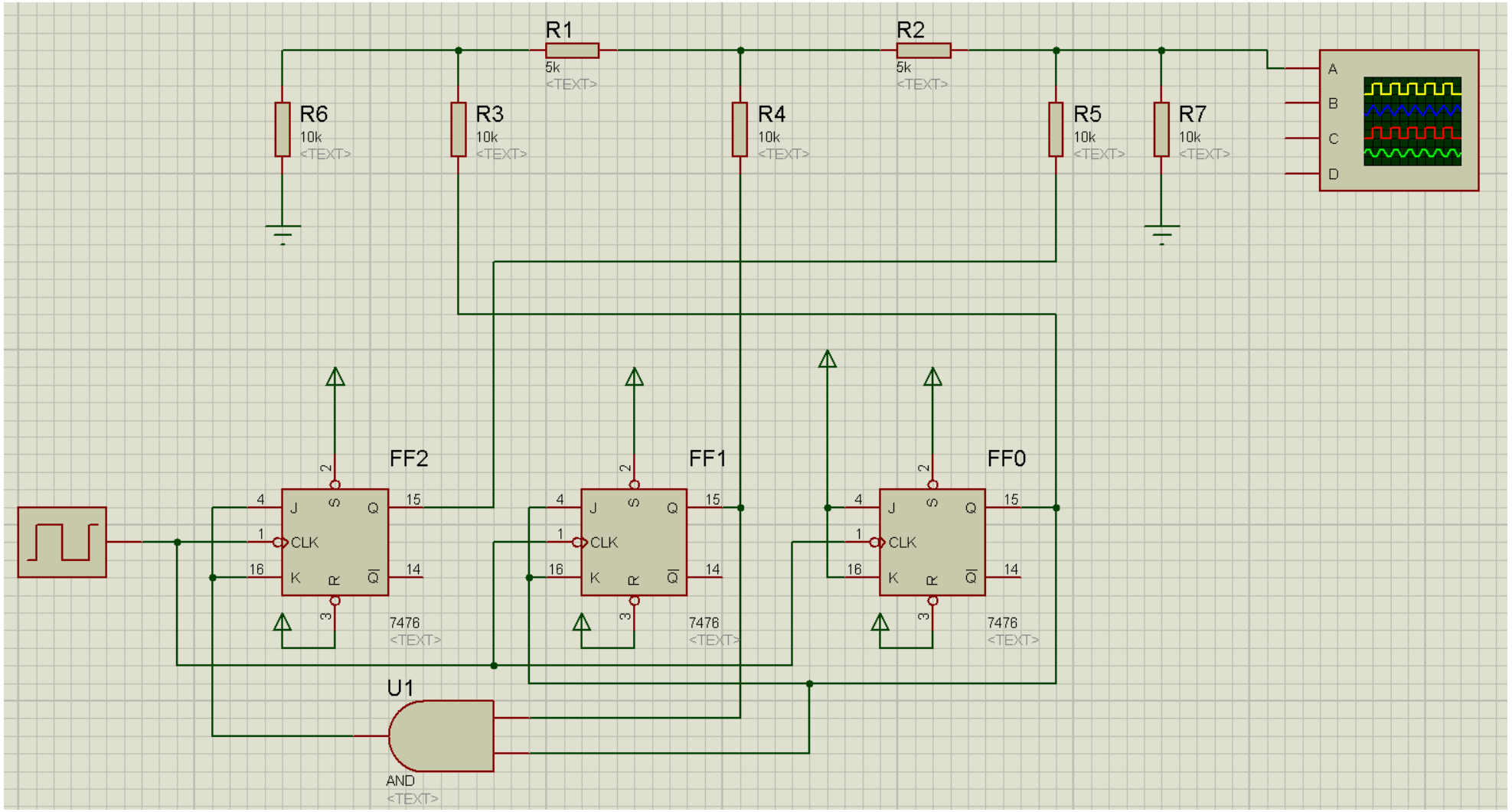
K1=Q0

J0=1

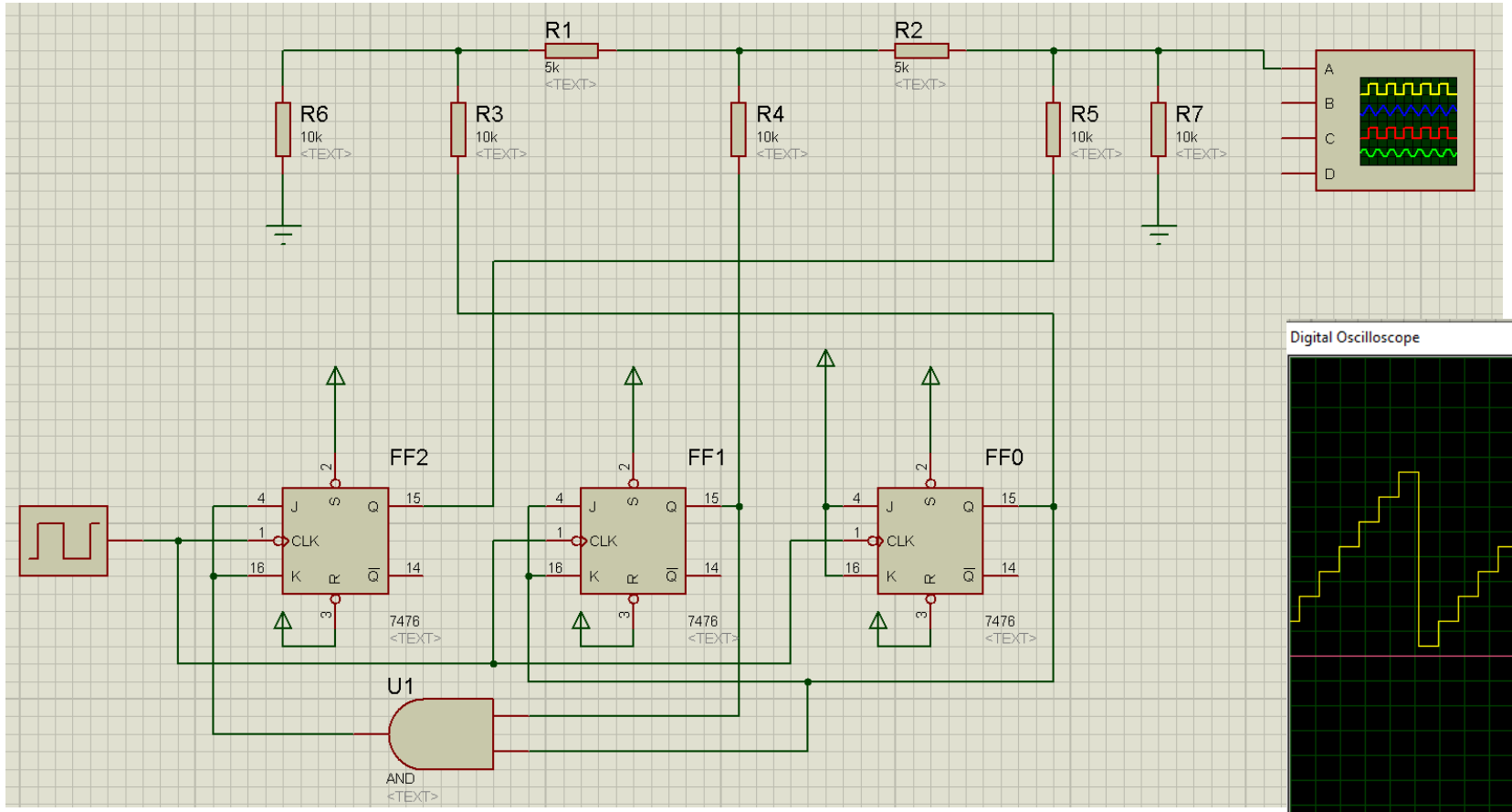
K0=1

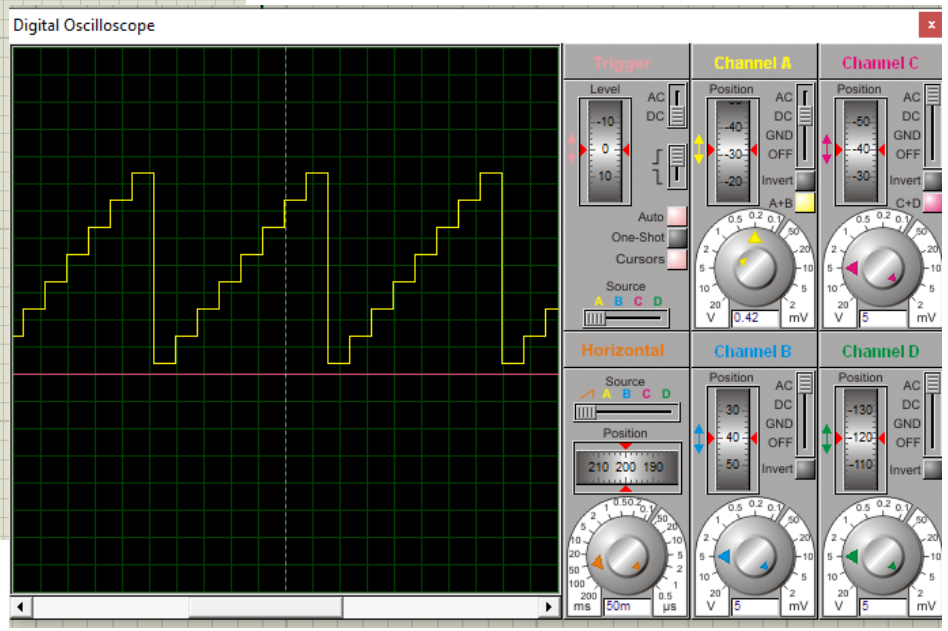


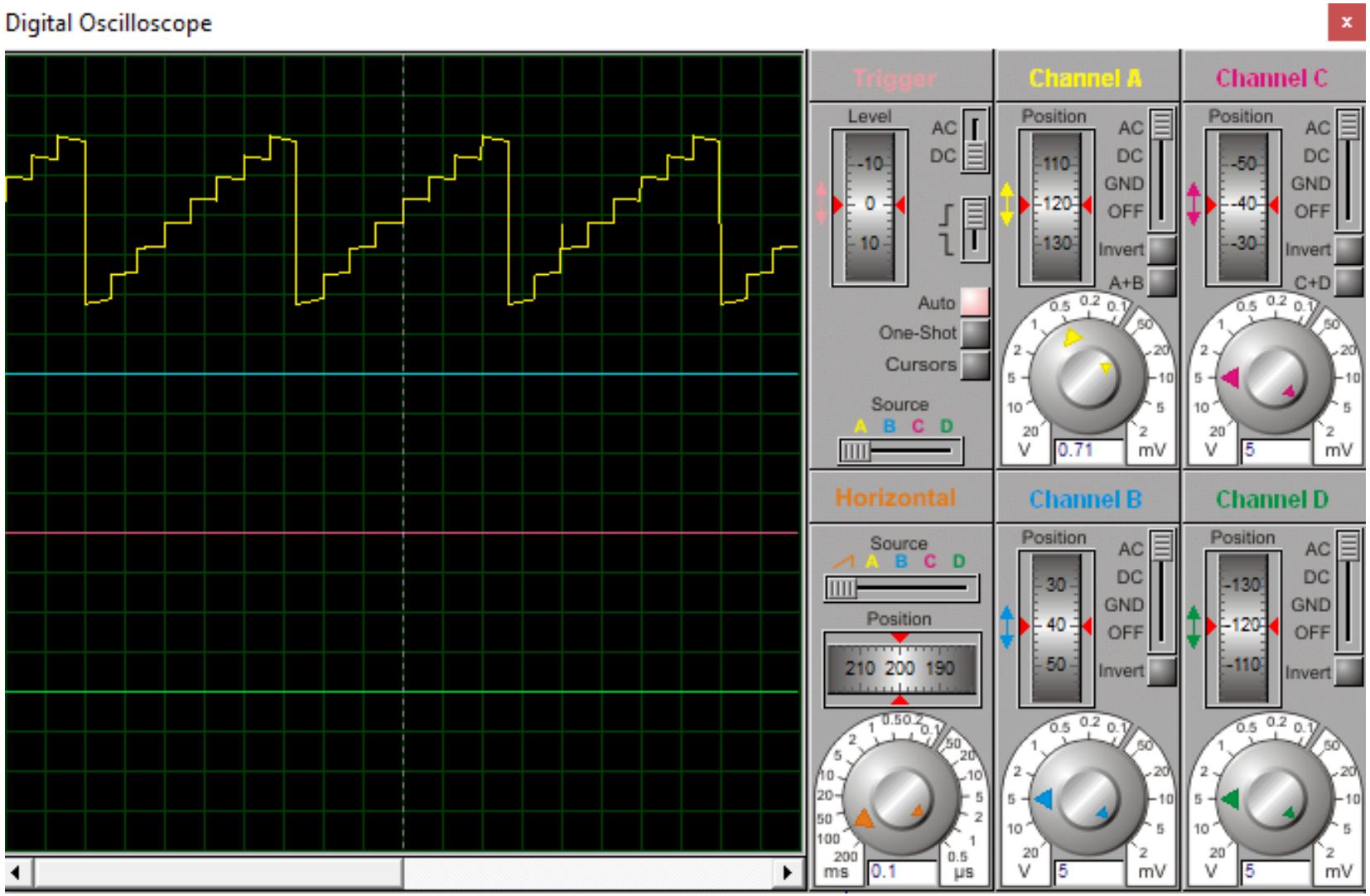
Máquina de Estado + Conversor D/A



Sinal no Osciloscópio

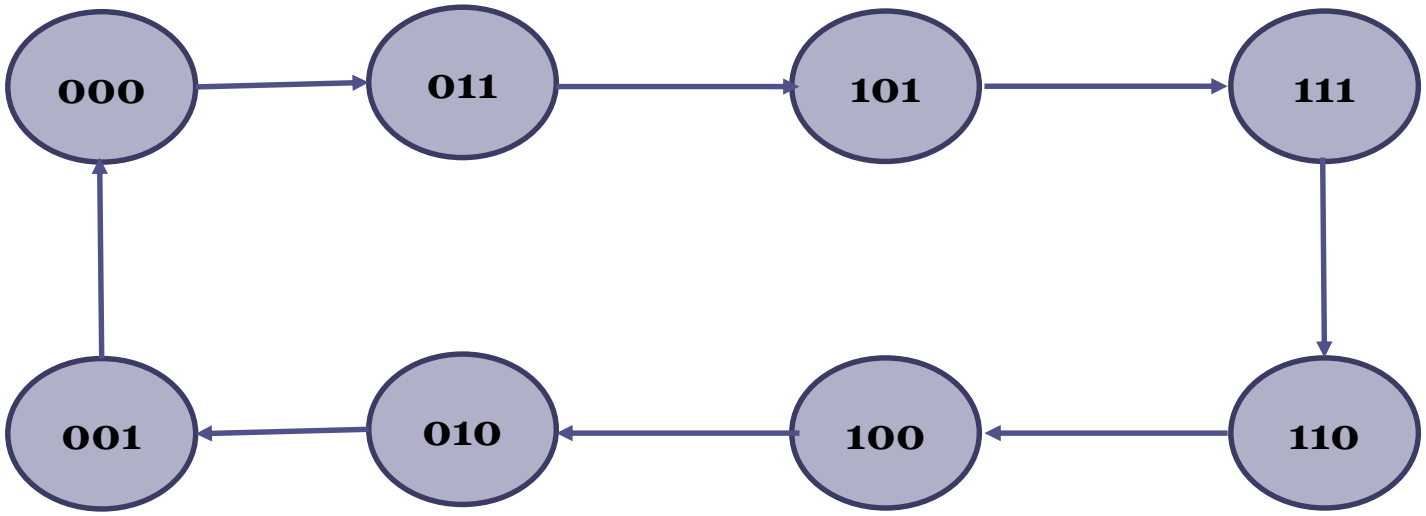





Digital Oscilloscope
Trigger
Level
AC
DC
Auto
One-Shot
Cursors
Source
A B C D
Channel A
Position
AC
DC
GND
OFF
Invert
A+B
0.71
mV
Channel C
Position
AC
DC
GND
OFF
Invert
C+D
5
mV
Horizontal
Source
A B C D
Position
210 200 190
0.1
ms
µs
Channel B
Position
AC
DC
GND
OFF
Invert
5
mV
Channel D
Position
AC
DC
GND
OFF
Invert
5
mV

Máquina de Estado

Exercício 2(fixação) : Utilizar o FF-T



1° Passo:

Estado Anterior (Qa)			Estado Final (Qf)		
Q2	Q1	Q0	Q2	Q1	Q0
0	0	0	0	1	1
0	0	1	0	0	0
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	0

Máquina de Estado

2°Passo: Vamos montar a tabela de alimentação das entradas dos FF-T, de acordo com a tabela do Qa e Qf dos estados;

Qa	Qf	T
0	0	0
0	1	1
1	0	1
1	1	0

Estado Anterior (Qa)			Estado Final (Qf)			FF-T(2)	FF-T(1)	FF-T(0)
Q2	Q1	Q0	Q2	Q1	Q0	T2	T1	T0
0	0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	1	0	1	1	1	0
1	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	1	0
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1

T2

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	0	0	1	0
Q2	1	0	0	0

T2=Q2Q1´Q0´+Q2´Q1Q0

T1

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	1	0	1	1
Q2	1	1	0	1

T1=Q0´+Q2Q1´+Q2´Q1

T0

	Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
Q2´	1	1	0	1
Q2	0	0	1	0

T0= Q2´Q1´+Q2´Q0´+Q2Q1Q0

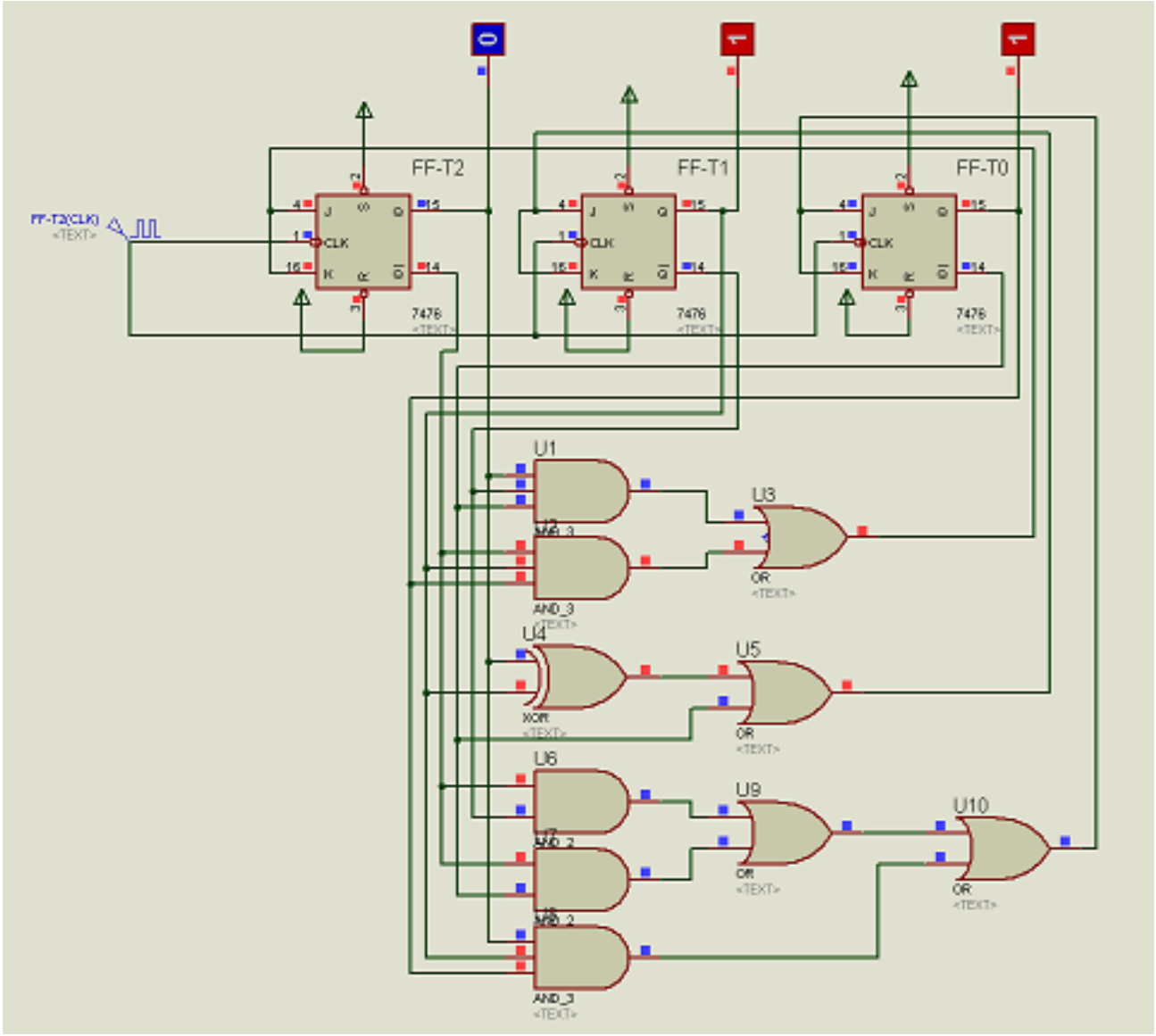
Máquina de Estado

3°Passo: Montar o circuito

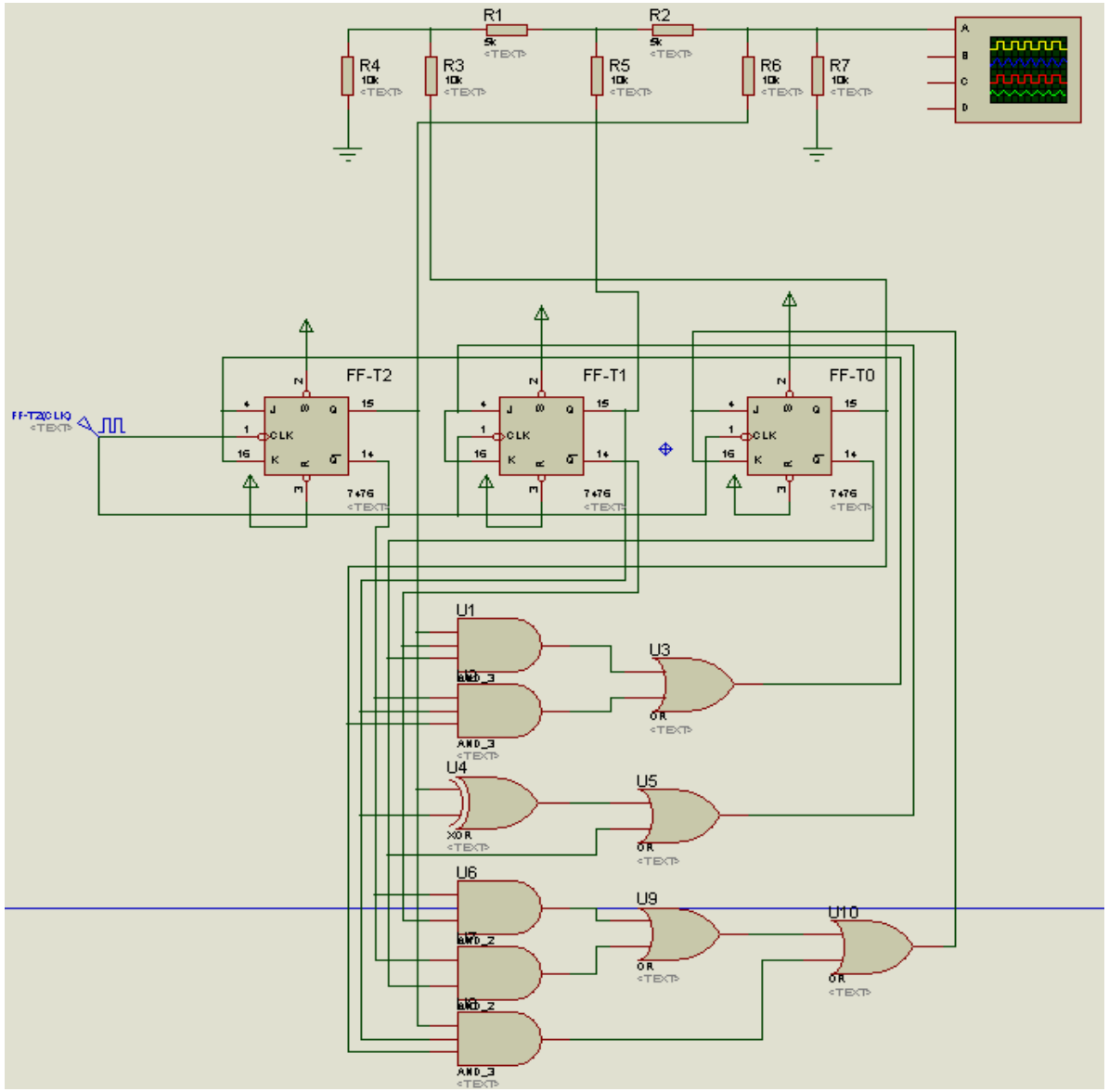
T2=Q2Q1´Q0´+Q2´Q1Q0

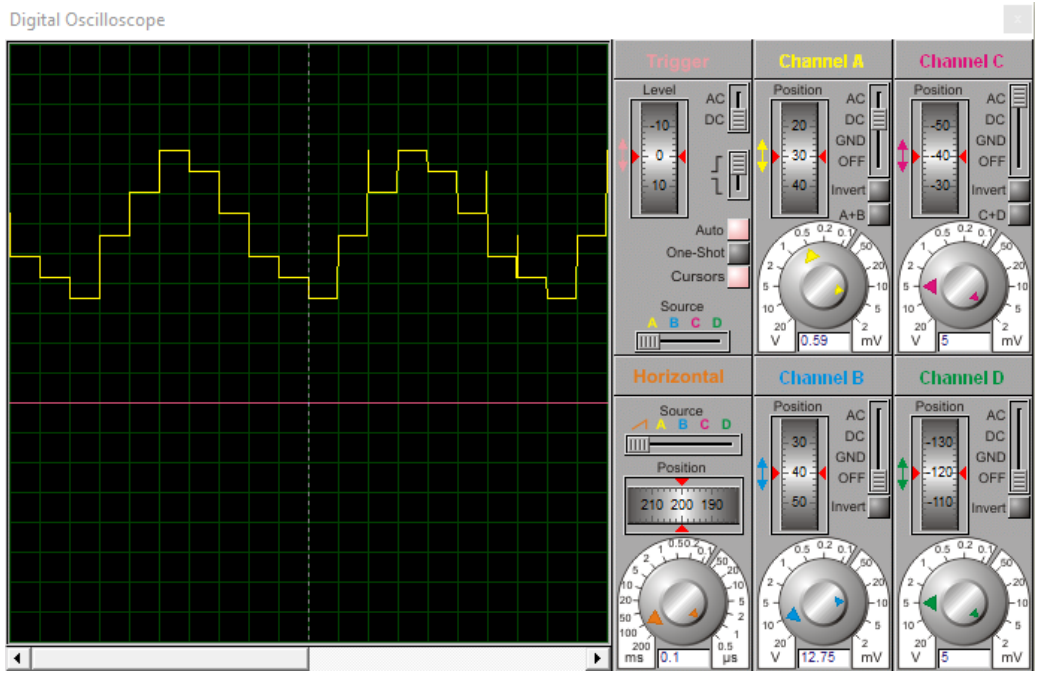
T1=Q0´+Q2Q1´+Q2´Q1

T0= Q2´Q1´+Q2´Q0´+Q2Q1Q0



Máquina de Estado + Conversor D/A



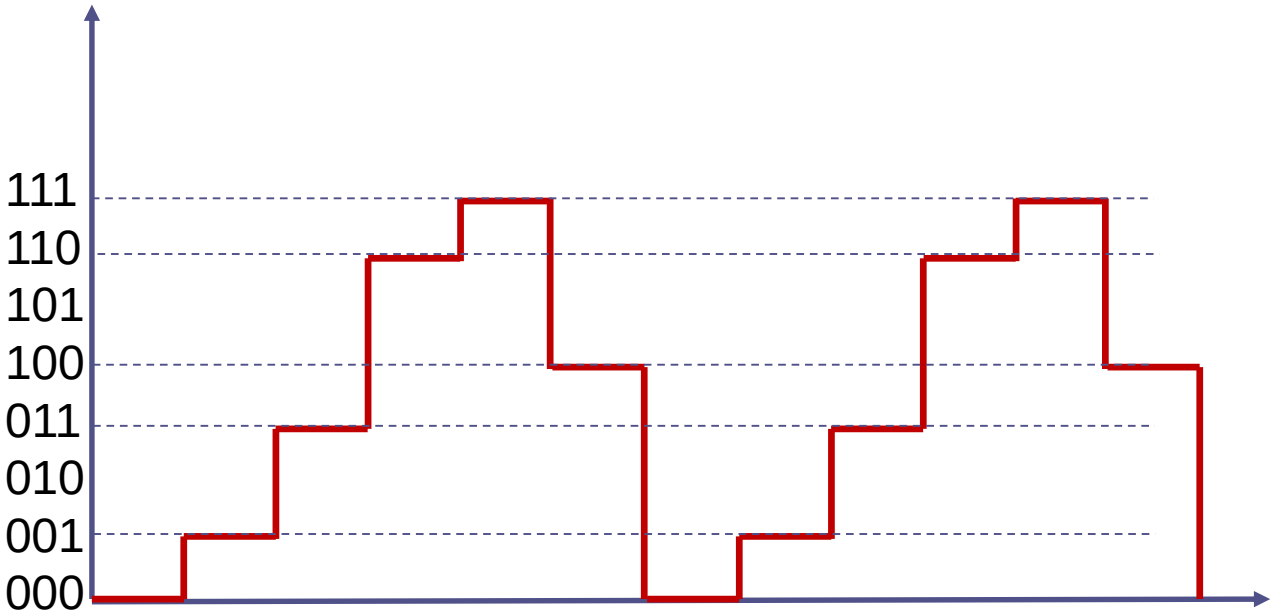


Exercício 3 (desafio):

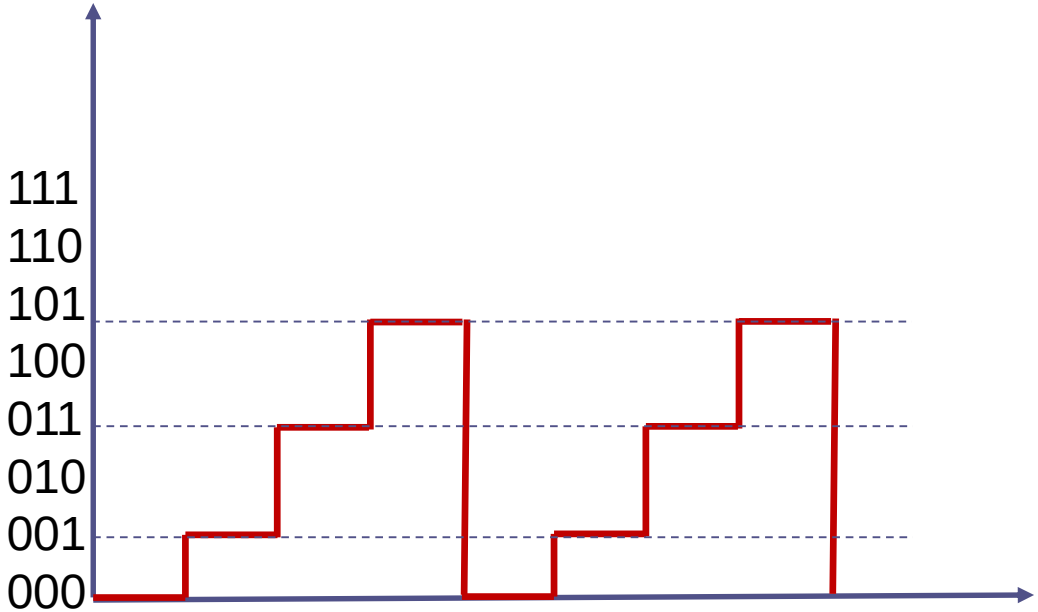
Utilizando um circuito R-2R e um circuito contador binário síncrono.

Elabore uma máquina de estado capaz de gerar duas formas de ondas:

Forma de onda 1, para X=0
Forma de onda 2, para X=1

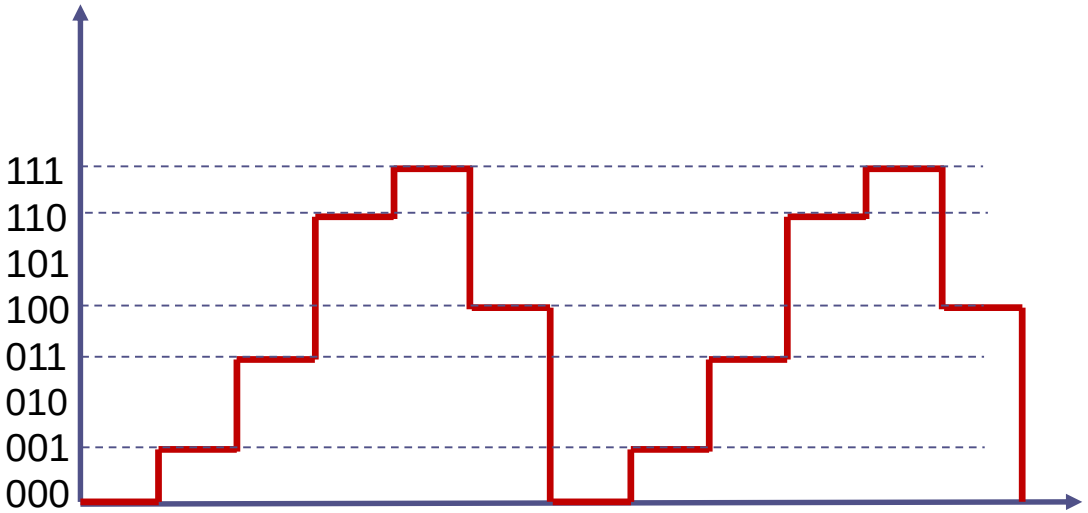


X=0

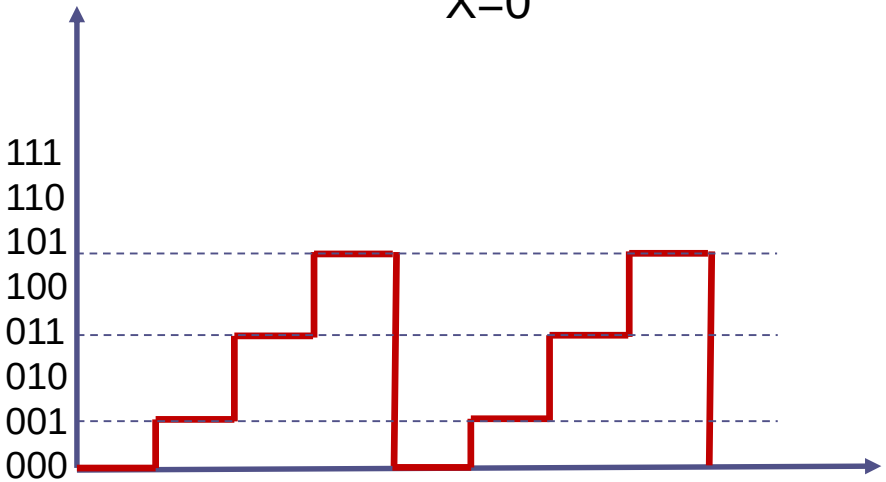


X=1

Resposta do Exercício 2:



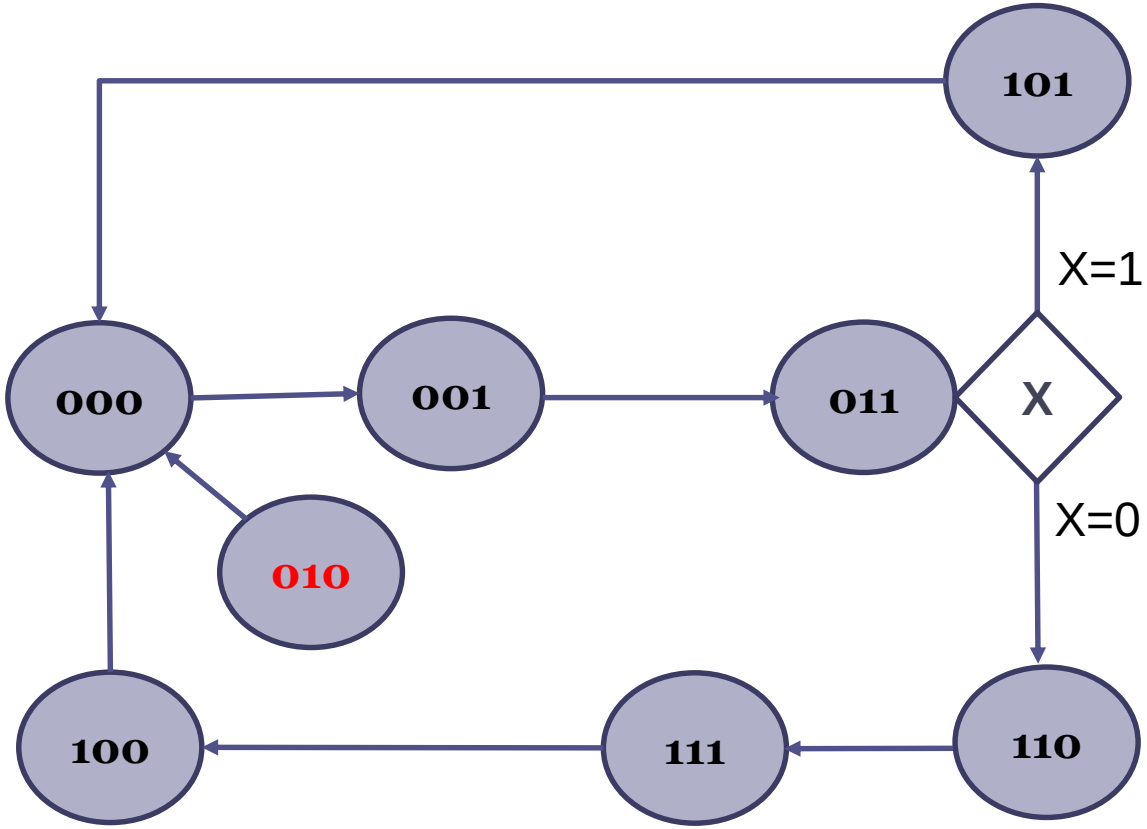
X=0



X=1

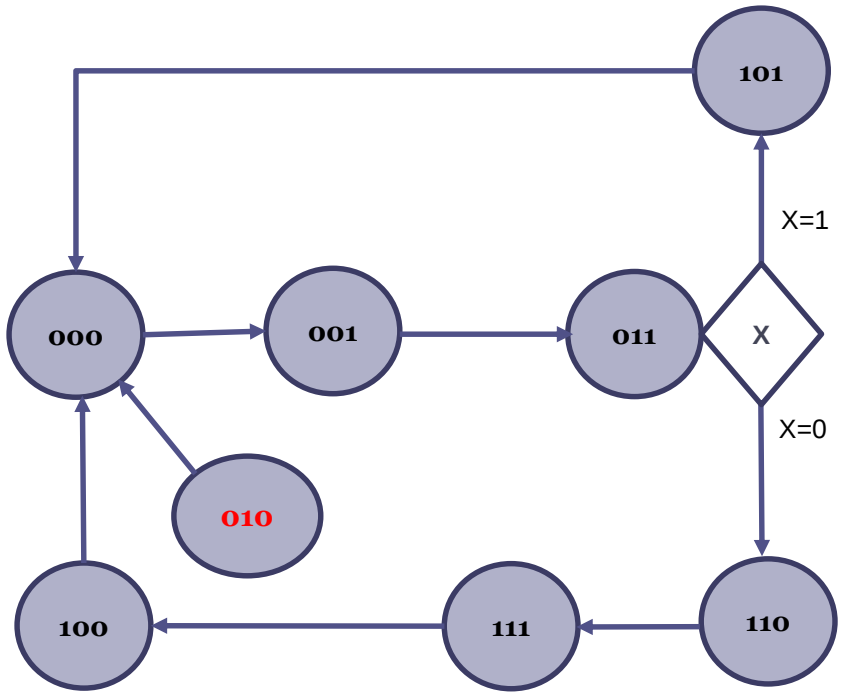
1° Passo: Montar o DE (Diagrama de Estado).

Percebe-se que o estado 010 não está sendo usado, desta forma irei direcionar para o estado inicial 000.



Resposta do Exercício 3:

2° Passo: Montar a tabela com base no DE



Estado Anterior (Qa)			Variável (X)	Estado Final (Qf)		
Q2	Q1	Q0	X	Q2	Q1	Q0
0	0	0	-	0	0	1
0	0	1	-	0	1	1
0	1	0	-	0	0	0
0	1	1	0 1	1 1	1 0	0 1
1	0	0	-	0	0	0
1	0	1	-	0	0	0
1	1	0	-	1	1	1
1	1	1	-	1	0	0

Resposta do Exercício 3:

3° Passo: Definir o FF que iremos trabalhar e montar a tabela.

Faremos o exemplo com um FF-JK, um FF-T e um FF-D, apenas para diferenciar. Para exercitar você pode fazer usando qualquer FF e avaliar qual é mais simples de montar.

Estado Anterior (Qa)			Variável (X)	Estado Final (Qf)			FF-JK		FF-T	FF-D
Q2	Q1	Q0	X	Q2	Q1	Q0	J2	K2	T1	D0
0	0	0	-	0	0	1	0	*	0	1
0	0	1	-	0	1	1	0	*	1	1
0	1	0	-	0	0	0	0	*	1	0
0	1	1	0	1	1	0	1	*	0	0
			1	1	0	1	1	*	1	1
1	0	0	-	0	0	0	*	1	0	0
1	0	1	-	0	0	0	*	1	0	0
1	1	0	-	1	1	1	*	0	0	1
1	1	1	-	1	0	0	*	0	1	0

Qa	Qf	J	K
0	0	0	*
0	1	1	*
1	0	*	1
1	1	*	0

Qa	Qf	D
0	0	0
0	1	1
1	0	0
1	1	1

Resposta do Exercício 3:

4° Passo: Simplificar montando as expressões para as entradas dos FFs.

Estado Anterior (Qa)			Variável (X)	Estado Final (Qf)			FF-JK		FF-T	FF-D
Q2	Q1	Q0	X	Q2	Q1	Q0	J2	K2	T1	D0
0	0	0	-	0	0	1	0	*	0	1
0	0	1	-	0	1	1	0	*	1	1
0	1	0	-	0	0	0	0	*	1	0
0	1	1	0 1	1 1	1 0	0 1	1 1	* *	0 1	0 1
1	0	0	-	0	0	0	*	1	0	0
1	0	1	-	0	0	0	*	1	0	0
1	1	0	-	1	1	1	*	0	0	1
1	1	1	-	1	0	0	*	0	1	0

J2

Q2´ \ Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
0	0	1	0
*	*	*	*

J2=Q1Q0

K2

Q2´ \ Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
*	*	*	*
1	1	0	0

K2=Q1´

Resposta do Exercício 3:

4° Passo: Simplificar montando as expressões para as entradas dos FFs.

Estado Anterior (Qa)			Variável (X)	Estado Final (Qf)			FF-JK		FF-T	FF-D
Q2	Q1	Q0	X	Q2	Q1	Q0	J2	K2	T1	D0
0	0	0	-	0	0	1	0	*	0	1
0	0	1	-	0	1	1	0	*	1	1
0	1	0	-	0	0	0	0	*	1	0
0	1	1	0 1	1 1	1 0	0 1	1 1	* *	0 1	0 1
1	0	0	-	0	0	0	*	1	0	0
1	0	1	-	0	0	0	*	1	0	0
1	1	0	-	1	1	1	*	0	0	1
1	1	1	-	1	0	0	*	0	1	0

T1

Q2´ \ Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
0	1	X	1
Q2 0	0	1	0

T1= Q2´Q1´Q0+Q2´Q1Q0´+X(Q2´Q1Q0) +Q2Q1Q0

D0

Q2´ \ Q1´Q0´	Q1´Q0	Q1Q0	Q1Q0´
1	1	X	0
Q2 0	0	0	1

D0=Q2´Q1´+X(Q2´Q1Q0)+Q2Q1Q0´

Resposta do Exercício 3:

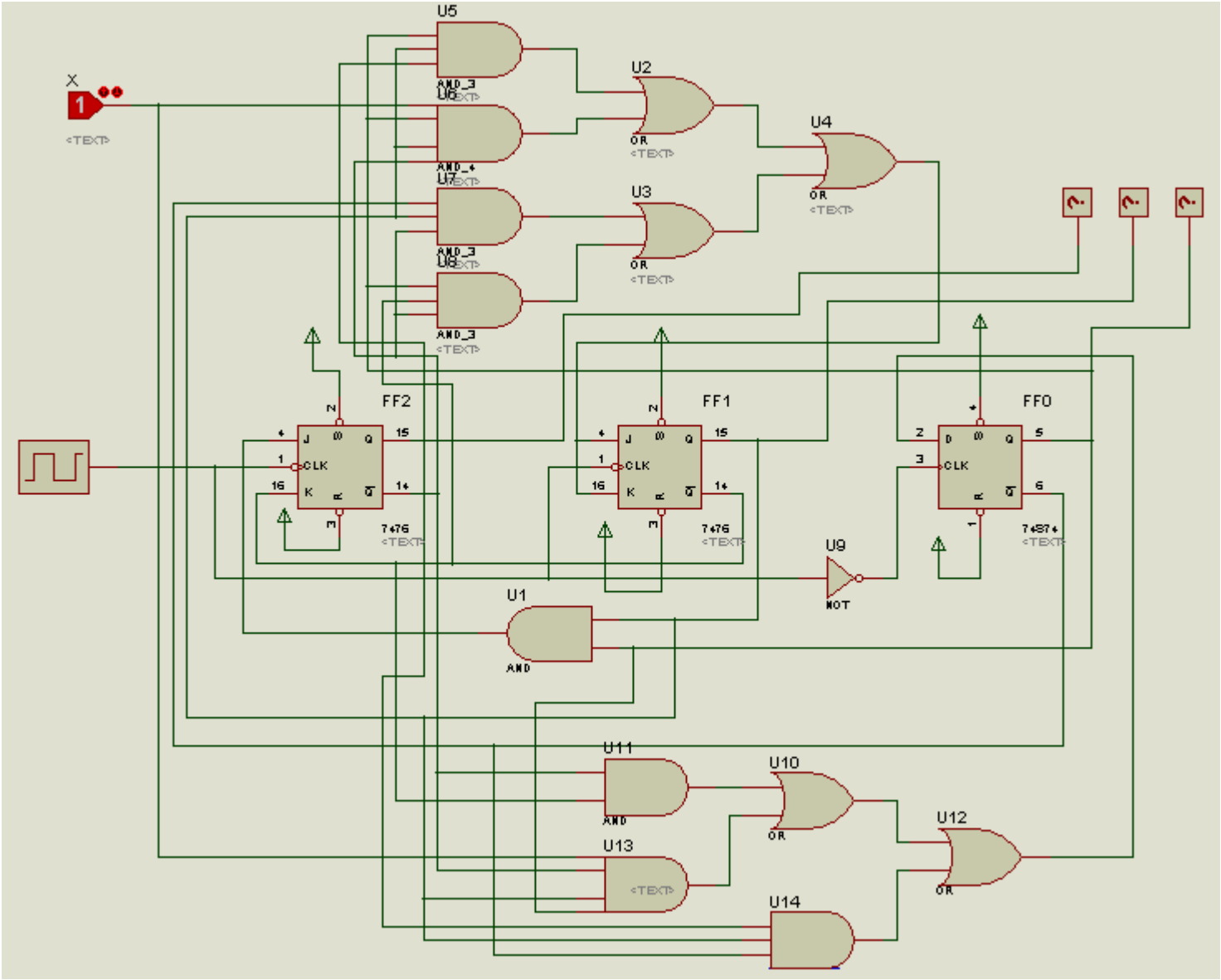
5° Passo: Montar o circuito no Proteus.

J2=Q1Q0

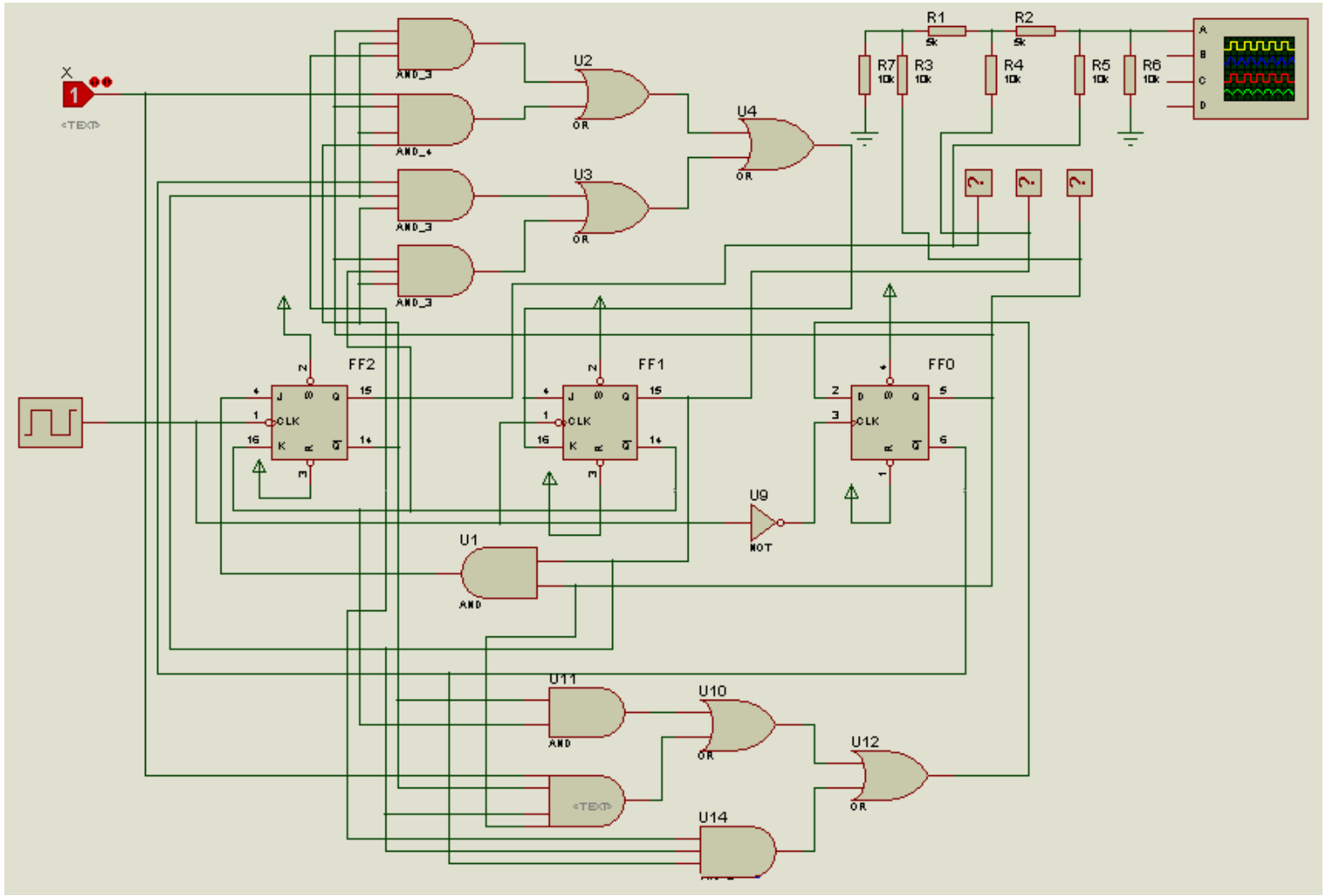
K2=Q1´

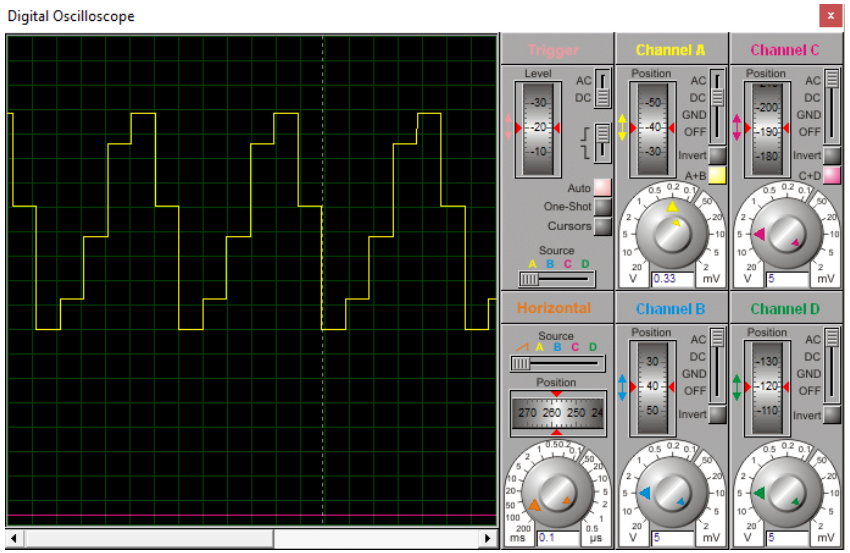
T1= Q2´Q1´Q0+Q2´Q1Q0´+X(Q2´Q1Q0) +Q2Q1Q0

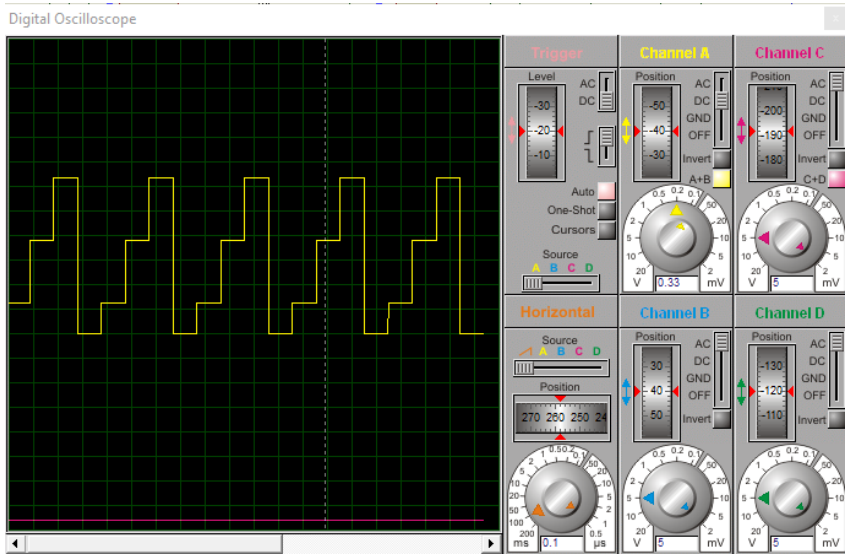
D0=Q2´Q1´+X(Q2´Q1Q0)+Q2Q1Q0´



Resposta do Exercício 3:







Bons Estudos

Prof. MSc. Bruno de Oliveira Monteiro

Inatel