INATEL - Instituto Nacional de Telecomunicações

E207 – Eletrônica Digital I **3º Período / 1º Semestre de 2021**

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Aluno: **Matrícula:** **Período:** **Data:** / /

RELATÓRIO 5 RESOLUÇÃO

EXERCÍCIO

Questão 1.

Módulo

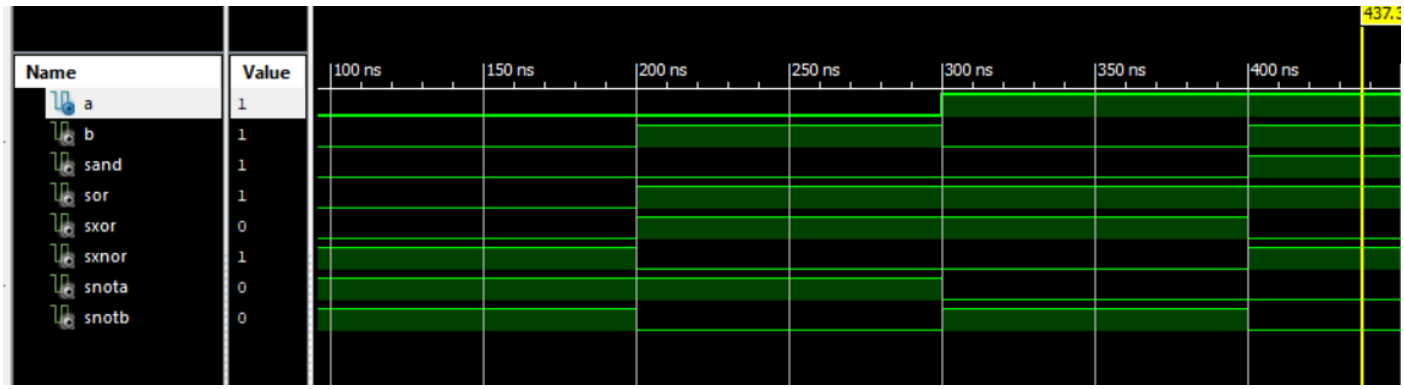
```
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Questaol is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           Sand : out  STD_LOGIC;
           Sor : out  STD_LOGIC;
           Sxor  : out  STD_LOGIC;
           Sxnor : out  STD_LOGIC;
           SnotA : out  STD_LOGIC;
           SnotB : out  STD_LOGIC);
end Questaol;

architecture Behavioral of Questaol is

begin

Sand <= A and B;
Sor <= A or B;
Sxor <= A xor B;
Sxnor <= A xnor B;
SnotA <= not(A);
SnotB <= not(B);

end Behavioral;
```

Teste

```
41
42      COMPONENT Questaol
43      PORT(
44           A : IN  std_logic;
45           B : IN  std_logic;
46           Sand : OUT  std_logic;
47           Sor : OUT  std_logic;
48           Sxor : OUT  std_logic;
49           Sxnor : OUT  std_logic;
50           SnotA : OUT  std_logic;
51           SnotB : OUT  std_logic
52          );
53      END COMPONENT;
54
55
56     --Inputs
57     signal A : std_logic := '0';
58     signal B : std_logic := '0';
59
60     --Outputs
61     signal Sand : std_logic;
62     signal Sor : std_logic;
63     signal Sxor : std_logic;
64     signal Sxnor : std_logic;
65     signal SnotA : std_logic;
66     signal SnotB : std_logic;
67     -- No clocks detected in port list. Replace <clock> below with
68     -- appropriate port name
69
70
71
72  BEGIN
73
74     -- Instantiate the Unit Under Test (UUT)
```

```
71
72  BEGIN
73
74     -- Instantiate the Unit Under Test (UUT)
75     uut: Questaol PORT MAP (
76            A => A,
77            B => B,
78            Sand => Sand,
79            Sor => Sor,
80            Sxor => Sxor,
81            Sxnor => Sxnor,
82            SnotA => SnotA,
83            SnotB => SnotB
84          );
85
86
87
88     -- Stimulus process
89     stim_proc: process
90     begin
91        -- hold reset state for 100 ns.
92        wait for 100 ns;
93        A <= '0';
94        B <= '0';
95        wait for 100 ns;
96        A <= '0';
97        B <= '1';
98        wait for 100 ns;
99        A <= '1';
100       B <= '0';
101       wait for 100 ns;
102       A <= '1';
103       B <= '1';
```

Simulação



Questão 2.

Circuito 1

Módulo

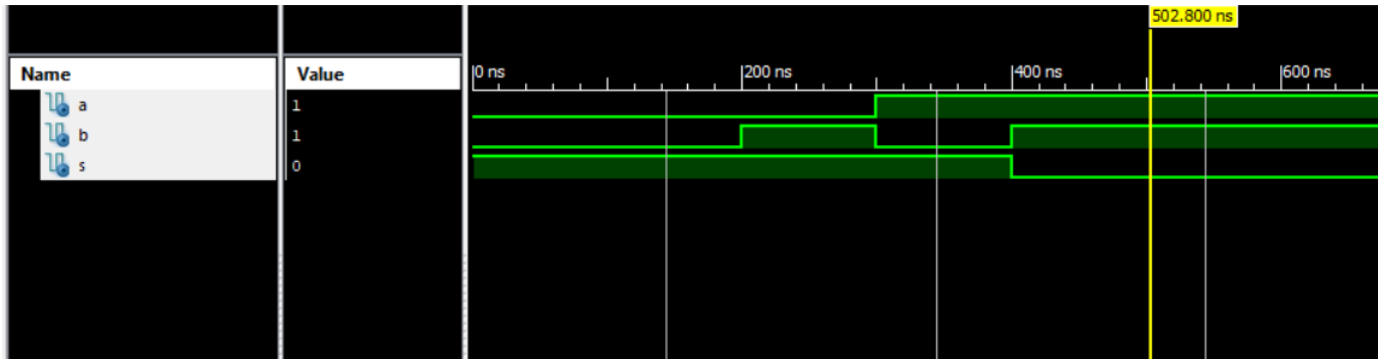
```
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26  
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31  
32  entity Circuitol is
33      Port ( A : in  STD_LOGIC;
34             B : in  STD_LOGIC;
35             S : out  STD_LOGIC);
36  end Circuitol;
37  
38  architecture Behavioral of Circuitol is
39  
40  begin
41  
42  S <= not(A and B);
43  end Behavioral;
44
```

Teste

```
35  ENTITY circuitoltest IS
36  END circuitoltest;
37
38  ARCHITECTURE behavior OF circuitoltest IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT Circuitol
43      PORT(
44           A : IN  std_logic;
45           B : IN  std_logic;
46           S : OUT  std_logic
47          );
48      END COMPONENT;
49
50
51     --Inputs
52     signal A : std_logic := '0';
53     signal B : std_logic := '0';
54
55     --Outputs
56     signal S : std_logic;
57     -- No clocks detected in port list. Replace <clock> below with
58     -- appropriate port name
59
60
61  BEGIN
62
63     -- Instantiate the Unit Under Test (UUT)
64     uut: Circuitol PORT MAP (
```

```
BEGIN

   -- Instantiate the Unit Under Test (UUT)
   uut: Circuito1 PORT MAP (
          A => A,
          B => B,
          S => S
        );


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;
      A <= '0';
      B <= '0';
      wait for 100 ns;
      A <= '0';
      B <= '1';
      wait for 100 ns;
      A <= '1';
      B <= '0';
      wait for 100 ns;
      A <= '1';
      B <= '1';


      -- insert stimulus here

      wait;
   end process;
```

Simulação



Circuito 2

Módulo

```
1
2  entity Circuito2 is
3      Port ( A : in  STD_LOGIC;
4             B : in  STD_LOGIC;
5             C : in  STD_LOGIC;
6             D : in  STD_LOGIC;
7             S : out  STD_LOGIC);
8  end Circuito2;
9
0  architecture Behavioral of Circuito2 is
1
2  begin
3  S <= not((A and B) or ( C and D));
4
5
6  end Behavioral;
7
8
```

Teste

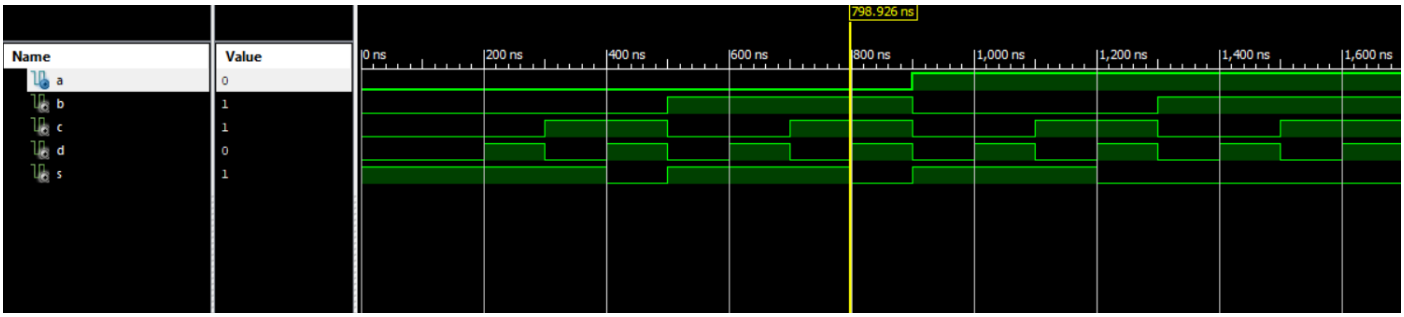
```
34
35  ENTITY Circuito2teste IS
36  END Circuito2teste;
37
38  ARCHITECTURE behavior OF Circuito2teste IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT Circuito2
43      PORT(
44           A : IN  std_logic;
45           B : IN  std_logic;
46           C : IN  std_logic;
47           D : IN  std_logic;
48           S : OUT  std_logic
49          );
50      END COMPONENT;
51
52
53     --Inputs
54     signal A : std_logic := '0';
55     signal B : std_logic := '0';
56     signal C : std_logic := '0';
57     signal D : std_logic := '0';
58
59     --Outputs
60     signal S : std_logic;
61     -- No clocks detected in port list. Replace <clock> below with
62     -- appropriate port name
63
64
65  BEGIN
66
67     -- Instantiate the Unit Under Test (UUT)
```

```
65  BEGIN
66
67     -- Instantiate the Unit Under Test (UUT)
68     uut: Circuito2 PORT MAP (
69            A => A,
70            B => B,
71            C => C,
72            D => D,
73            S => S
74          );
75
76
77     -- Stimulus process
78     stim_proc: process
79     begin
80        -- hold reset state for 100 ns.
81        wait for 100 ns;
82        A <= '0';
83        B <= '0';
84        C <= '0';
85        D <= '0';
86        wait for 100 ns;
87        A <= '0';
88        B <= '0';
89        C <= '0';
90        D <= '1';
91        wait for 100 ns;
92        A <= '0';
93        B <= '0';
94        C <= '1';
95        D <= '0';
96        wait for 100 ns;
97        A <= '0';
```

```
    wait for 100 ns;
    A <= '0';
    B <= '0';
    C <= '1';
    D <= '1';
    wait for 100 ns;
    A <= '0';
    B <= '1';
    C <= '0';
    D <= '0';
    wait for 100 ns;
    A <= '0';
    B <= '1';
    C <= '0';
    D <= '1';
    wait for 100 ns;
    A <= '0';
    B <= '1';
    C <= '1';
    D <= '0';
    wait for 100 ns;
    A <= '0';
    B <= '1';
    C <= '1';
    D <= '1';
    wait for 100 ns;
    A <= '1';
    B <= '0';
    C <= '0';
    D <= '0';
    wait for 100 ns;
    A <= '1';
    B <= '0';
    C <= '0';
```

```
131         wait for 100 ns;
132         A <= '1';
133         B <= '0';
134         C <= '1';
135         D <= '0';
136         wait for 100 ns;
137         A <= '1';
138         B <= '0';
139         C <= '1';
140         D <= '1';
141         wait for 100 ns;
142         A <= '1';
143         B <= '1';
144         C <= '0';
145         D <= '0';
146         wait for 100 ns;
147         A <= '1';
148         B <= '1';
149         C <= '0';
150         D <= '1';
151         wait for 100 ns;
152         A <= '1';
153         B <= '1';
154         C <= '1';
155         D <= '0';
156         wait for 100 ns;
157         A <= '1';
158         B <= '1';
159         C <= '1';
160         D <= '1';
161         wait for 100 ns;
162
163
```

Simulação



Questão 3:

Tabela da verdade

A	B	S
0	0	1
0	1	1
1	0	0
1	1	0

Tirando a expressão

S = A'B' + A'B

Simplificando

S = A'(B' + B)

S = A'

Circuito: