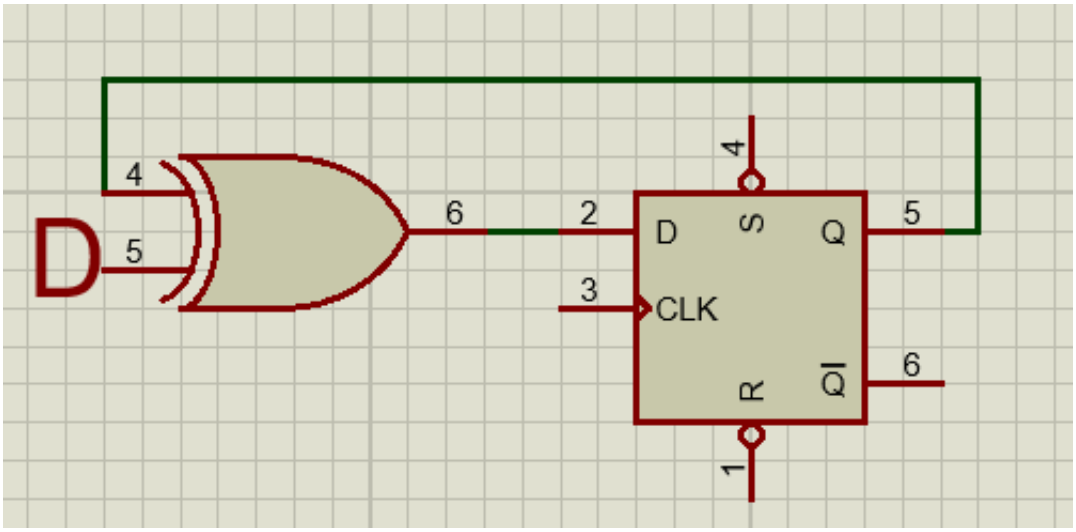
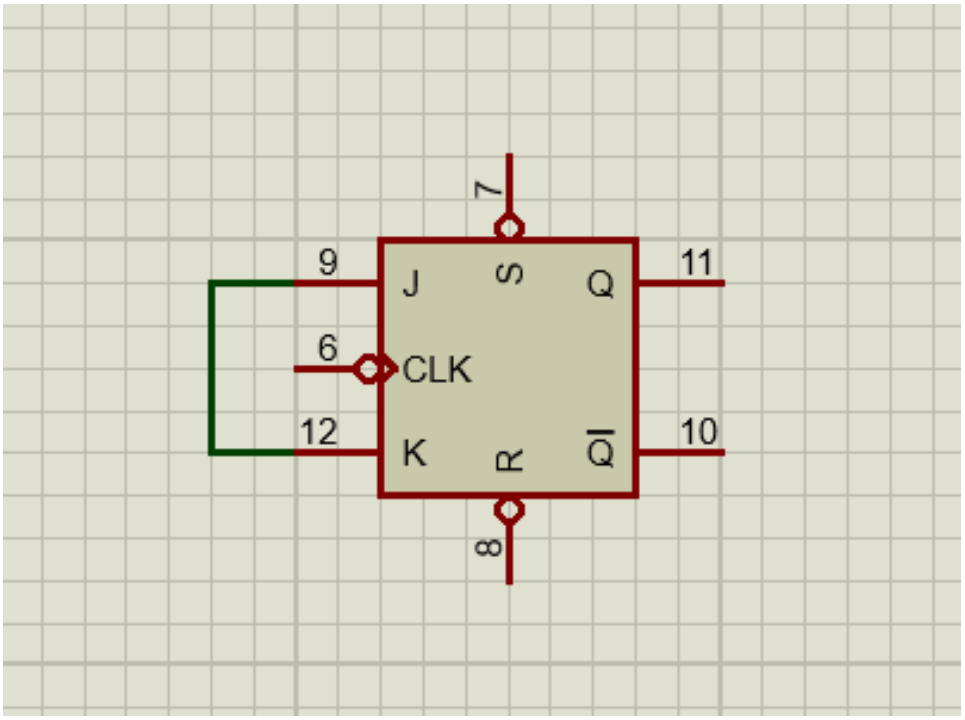
Relatório 3 Resolução

1)

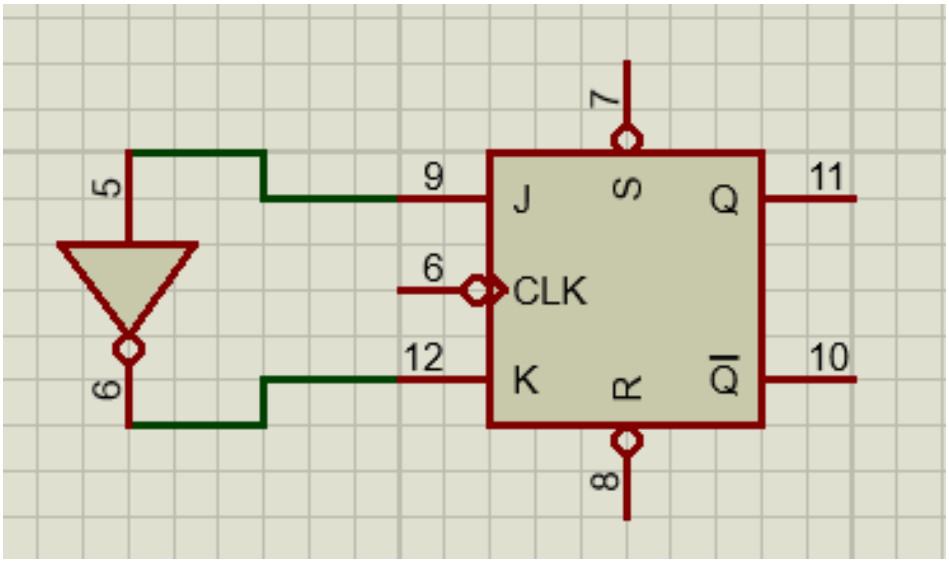
A)



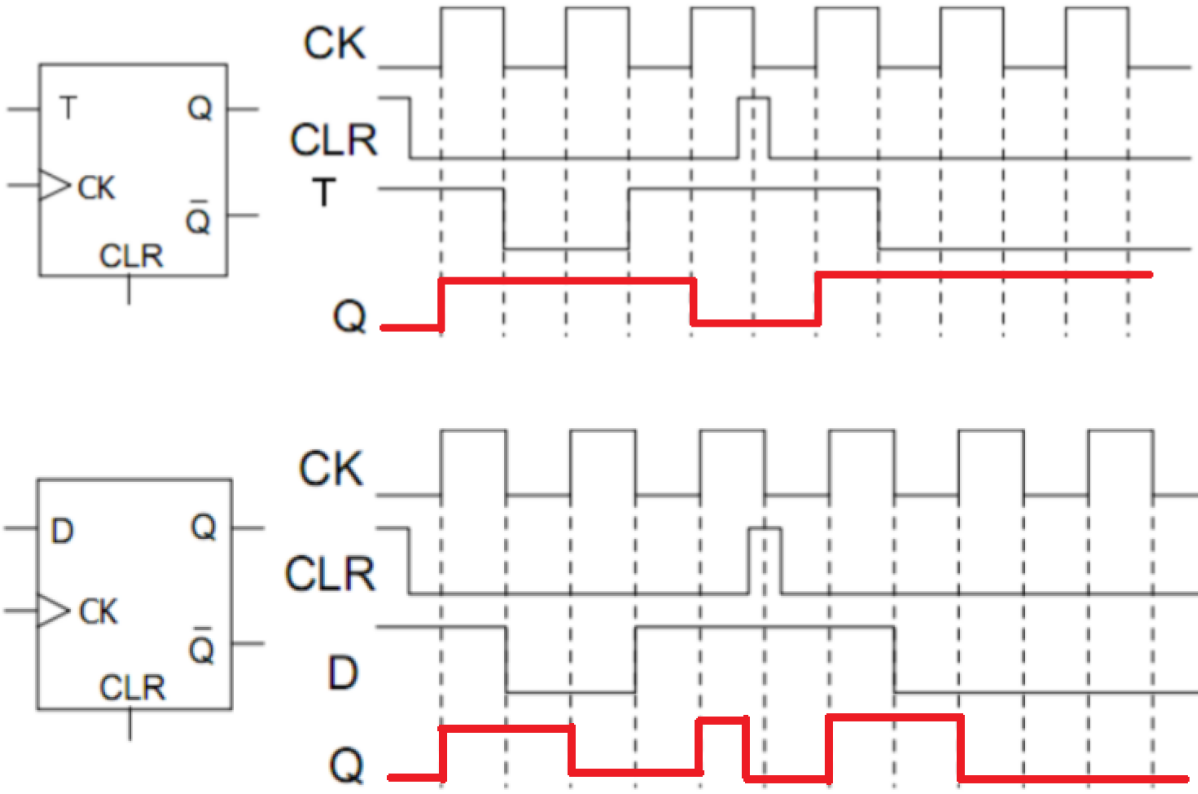
B)



C)


7
5
9
J
S
Q
11
6
CLK
12
K
R
QI
10
6
8

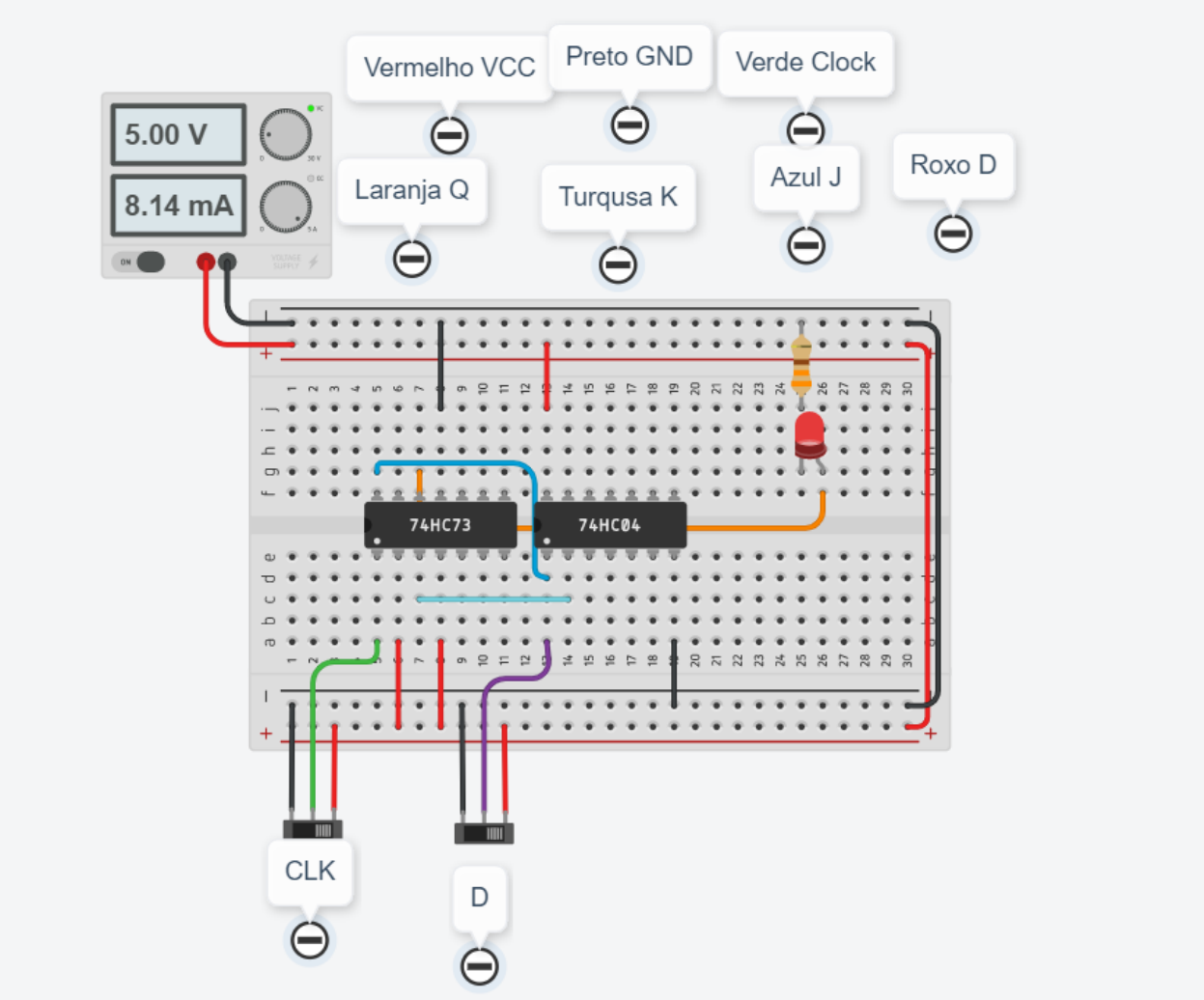
2)

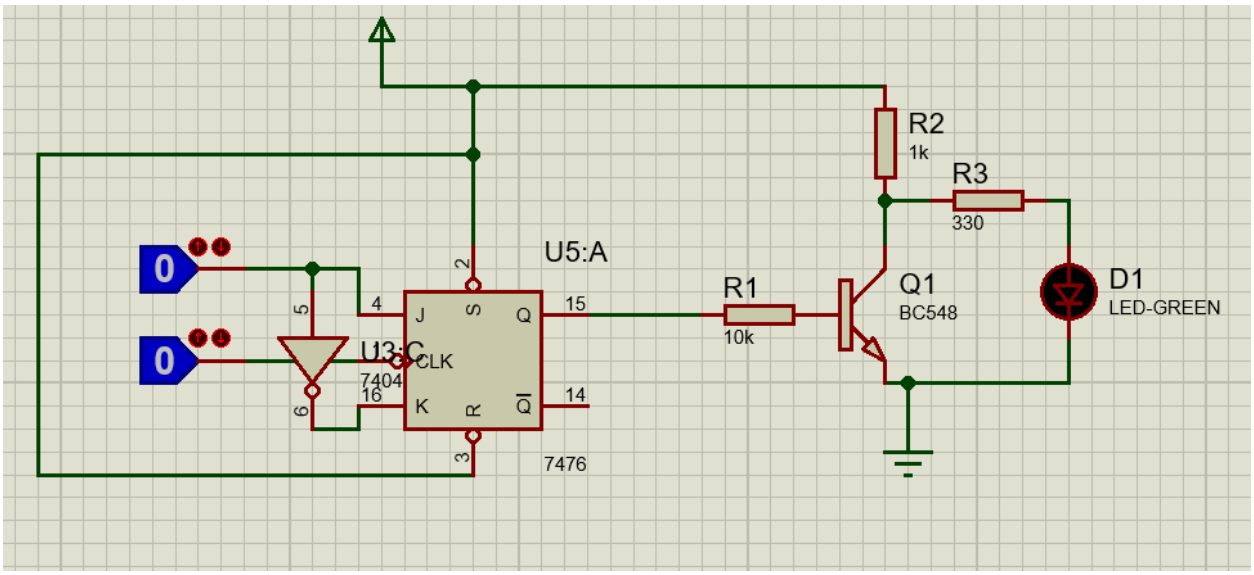

T
Q
CK
Q
CLR
CK
CLR
T
Q
D
Q
CK
Q
CLR
CK
CLR
D
Q

Pratica

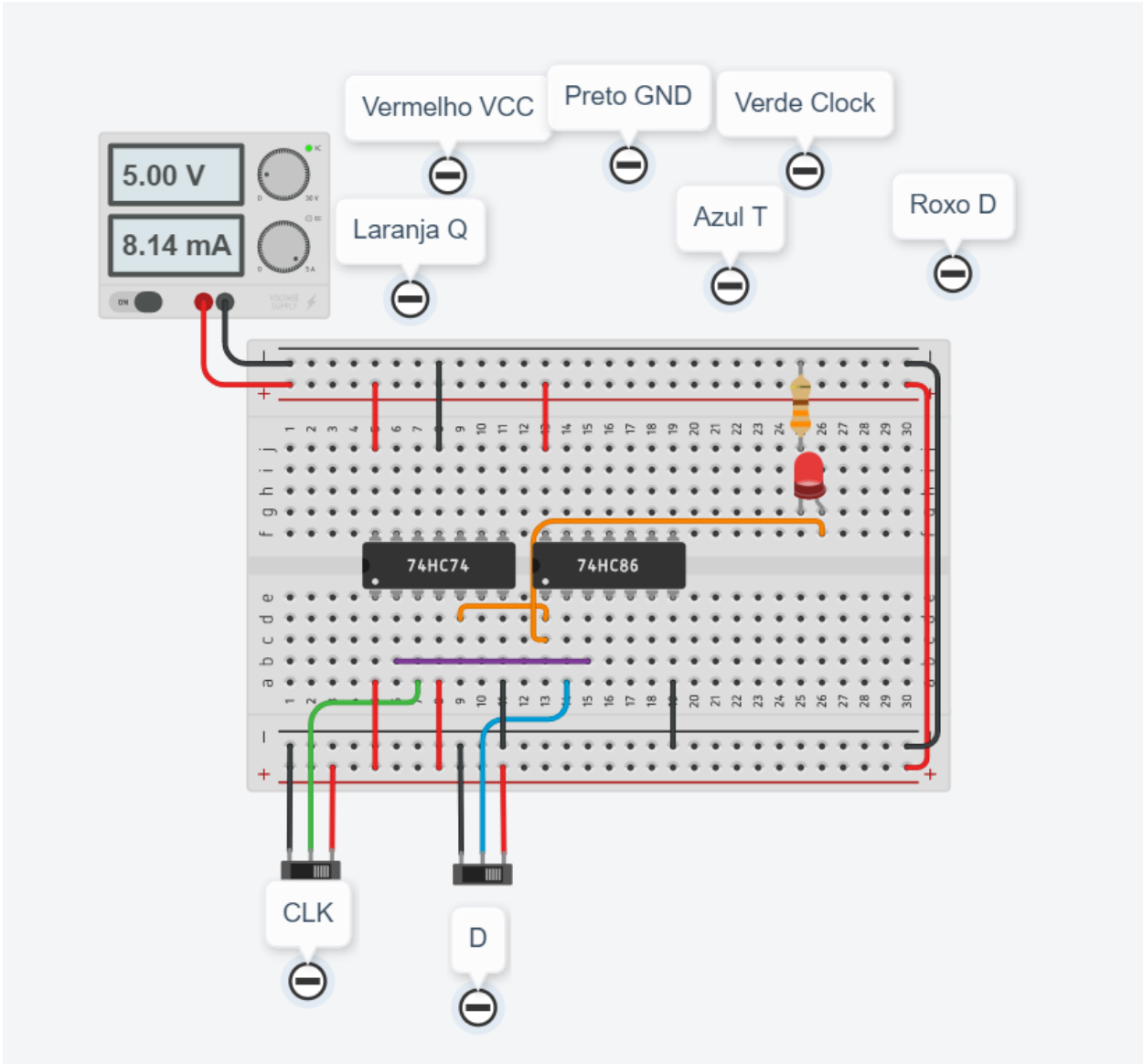
1)

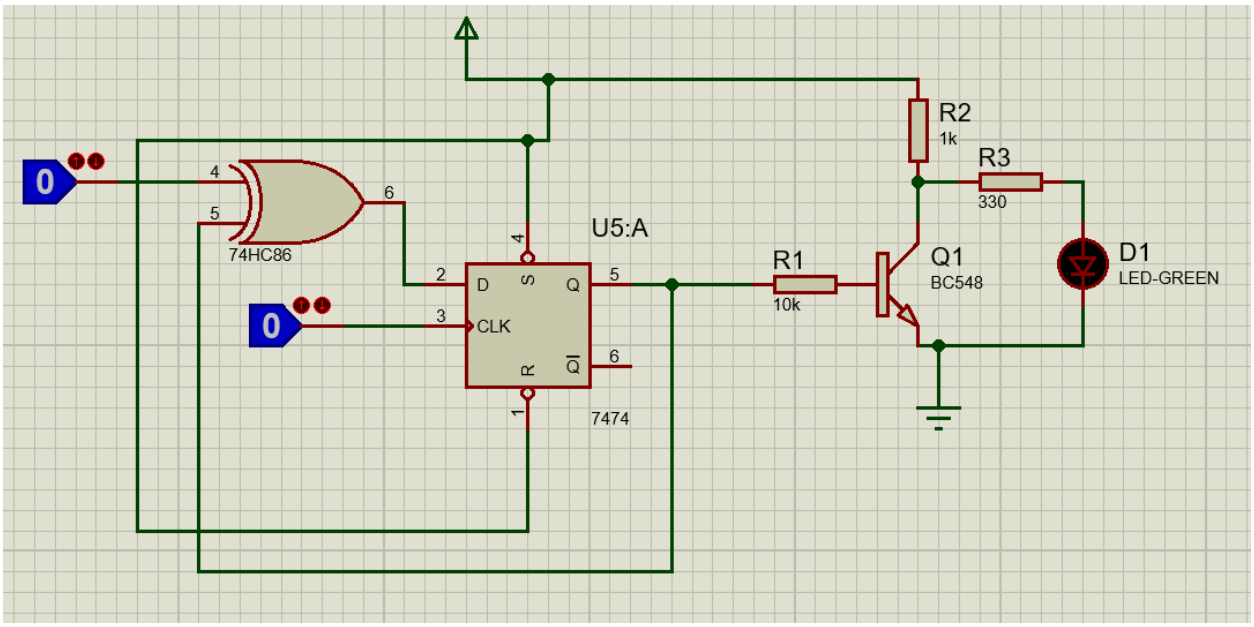
A)


Vermelho VCC
Preto GND
Verde Clock
Laranja Q
Turqusa K
Azul J
Roxo D
5.00 V
8.14 mA
74HC73
74HC04
CLK
D

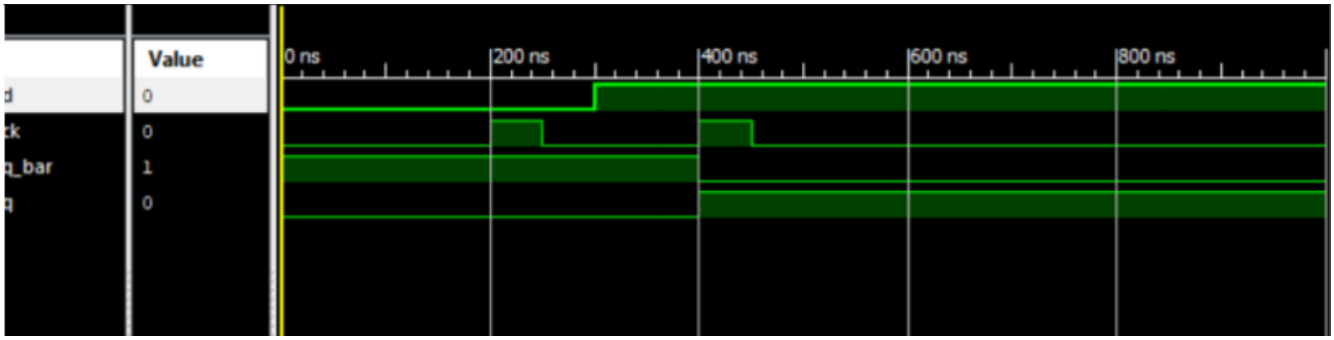

R2
1k
R3
330
U5:A
R1
10k
Q1
BC548
D1
LED-GREEN
0
0
U3:C
7404
J
S
Q
CLK
K
R
Q
7476
2
3
4
5
6
15
14
16

B)


Vermelho VCC
Preto GND
Verde Clock
Laranja Q
Azul T
Roxo D
5.00 V
8.14 mA
74HC74
74HC86
CLK
D


0
4
5
74HC86
6
U5:A
2
D
S
Q
5
3
CLK
R
Q
6
1
7474
0
R2
1k
R3
330
R1
10k
Q1
BC548
D1
LED-GREEN

2)


Value
0
0
1
0
0 ns
200 ns
400 ns
600 ns
800 ns

3)

```
entity FFT is
    Port ( T : in  STD_LOGIC;
           clk : in  STD_LOGIC;
           Q : out  STD_LOGIC;
           Q_bar : out  STD_LOGIC);
end FFT;

architecture Behavioral of FFT is
signal signal_q: STD_LOGIC;

begin
process(clk)
begin
 signal_q<= '0';
 if rising_edge(clk) THEN
    if(T ='1')THEN
      signal_q <= not(signal_q);
    elsif(T ='0')THEN
      signal_q<= Signal_q;
    end if;
  elsif falling_edge(clk) THEN
    signal_q <= Signal_q;
  end if;
  end process;
  Q <= signal_q;
  Q_bar <= not(signal_q);


end Behavioral;
```

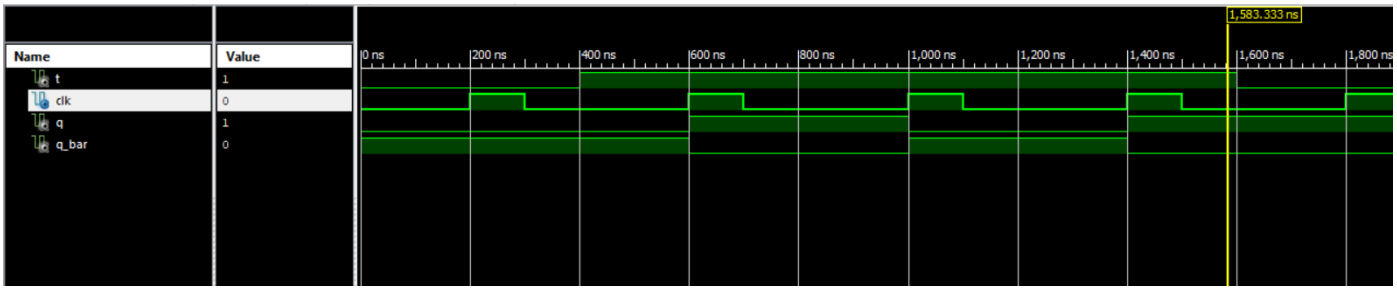
```
-- hold reset state for 100 ns.
T <= '0';
wait for 100 ns;
clk <= '0';
wait for 100 ns;
clk <= '1';
wait for 100 ns;
clk <= '0';
wait for 100 ns;

T <= '1';
wait for 100 ns;
clk <= '0';
wait for 100 ns;
clk <= '1';
wait for 100 ns;
clk <= '0';

wait for 100 ns;
T <= '1';
wait for 100 ns;
clk <= '0';
wait for 100 ns;
clk <= '1';
wait for 100 ns;
clk <= '0';

wait for 100 ns;
T <= '1';
wait for 100 ns;
clk <= '0';
wait for 100 ns;
clk <= '1';
wait for 100 ns;
clk <= '0';

wait for 100 ns;
T <= '0';
wait for 100 ns;
clk <= '0';
wait for 100 ns;
clk <= '1';
wait for 100 ns;
clk <= '0';
```


Name
Value
t
clk
q
q_bar
1
0
1
0
0 ns
200 ns
400 ns
600 ns
800 ns
1,000 ns
1,200 ns
1,400 ns
1,583.333 ns
1,600 ns
1,800 ns