1) A)

A	B	C	S1(Tranca)	S2(Bomba)	S3(Válvula)
0	0	0	0	0	1
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	0	1	0
1	1	1	0	0	0

Variáveis de entrada: A, B, C. Variáveis de saída: S1, S2, S3.

B)

	B'C'	B'C	BC	BC'
A'	0	0	0	0
A	1	1	0	0

S1 = A.B'

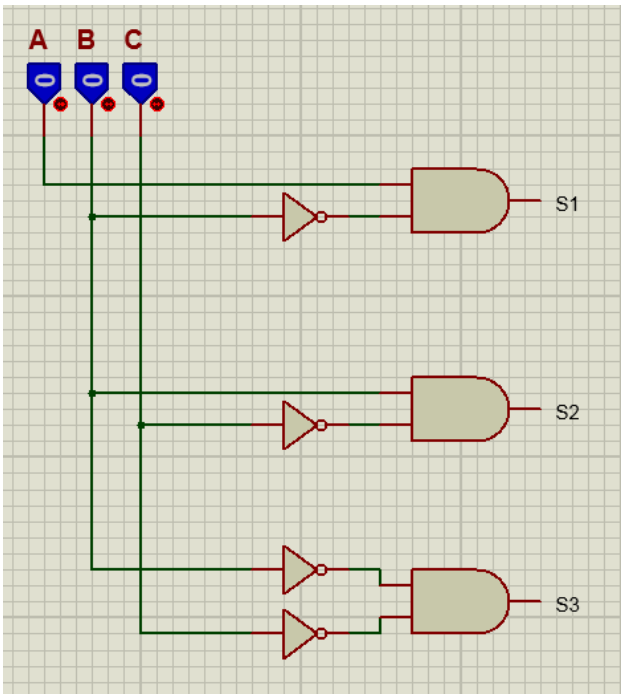
	B'C'	B'C	BC	BC'
A'	0	0	0	1
A	0	0	0	1

S2 = BC'

	B'C'	B'C	BC	BC'
A'	1	0	0	0
A	1	0	0	0

S3 = B'C'

C)



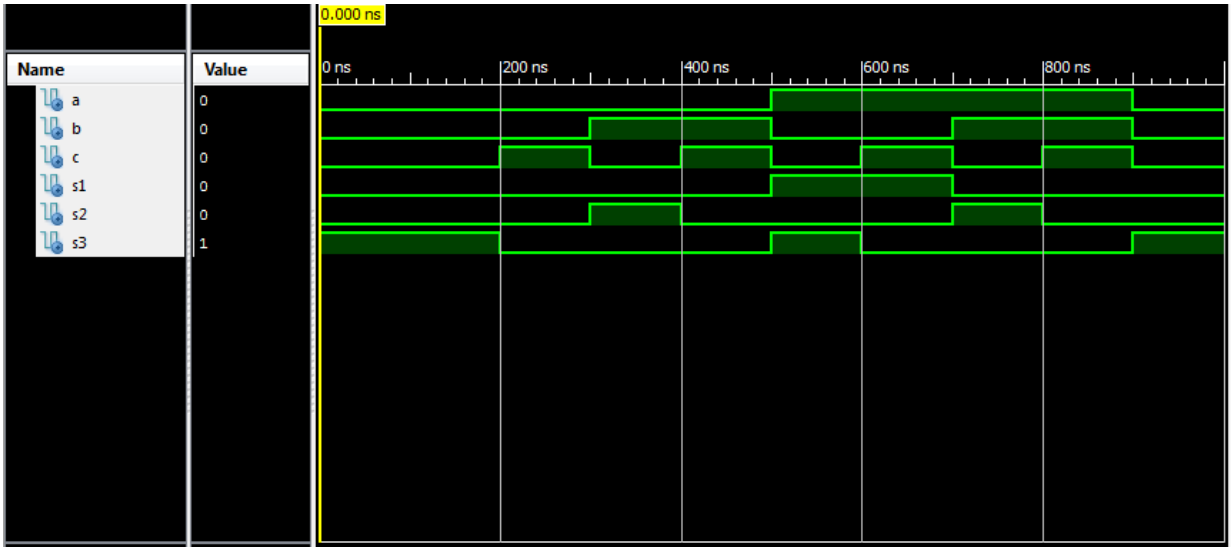
D) Modulo:

```
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity modulo is
33      Port ( A : in  STD_LOGIC;
34             B : in  STD_LOGIC;
35             C : in  STD_LOGIC;
36             S1 : out  STD_LOGIC;
37             S2 : out  STD_LOGIC;
38             S3 : out  STD_LOGIC);
39  end modulo;
40
41  architecture Behavioral of modulo is
42
43  begin
44
45     S1<= (A AND (NOT B));
46     S2<= (B AND (NOT C));
47     S3<= ((NOT B) AND (NOT C));
48
49  end Behavioral;
50
51
```

Teste:

```
81      -- Stimulus process
82      stim_proc: process
83      begin
84
85         wait for 100 ns;
86         A<= '0';
87         B<= '0';
88         C<= '0';
89         -- 001
90         wait for 100 ns;
91         A<= '0';
92         B<= '0';
93         C<= '1';
94         -- 010
95         wait for 100 ns;
96         A<= '0';
97         B<= '1';
98         C<= '0';
99         -- 011
100        wait for 100 ns;
101        A<= '0';
102        B<= '1';
103        C<= '1';
104        -- 100
105        wait for 100 ns;
106        A<= '1';
107        B<= '0';
108        C<= '0';
106        A<= '1';
107        B<= '0';
108        C<= '0';
109        -- 101
110        wait for 100 ns;
111        A<= '1';
112        B<= '0';
113        C<= '1';
114        -- 110
115        wait for 100 ns;
116        A<= '1';
117        B<= '1';
118        C<= '0';
119        -- 111
120        wait for 100 ns;
121        A<= '1';
122        B<= '1';
123        C<= '1';
124        -- 000
125        wait for 100 ns;
126        A<= '0';
127        B<= '0';
128        C<= '0';
129
130        wait;
131     end process;
132
133  END;
```

Gráfico:



2)A) Variáveis de entrada: A, B, C. Variáveis de saída: S

B)

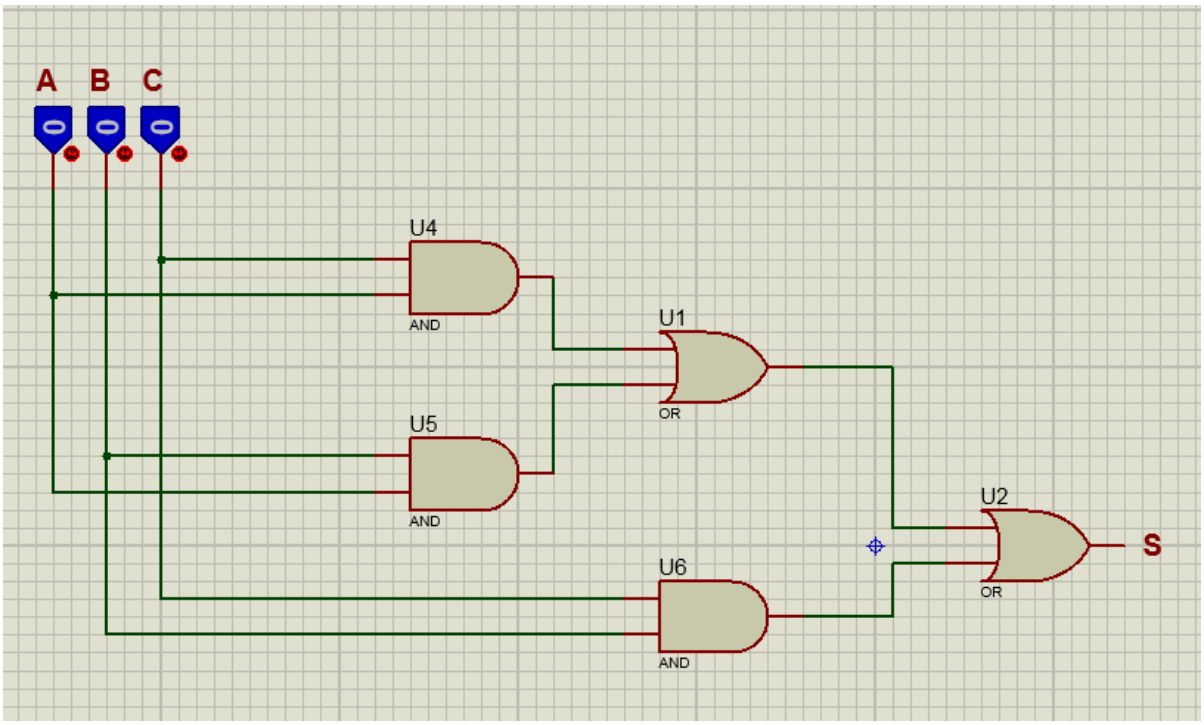
A	B	C	S
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

C)

	B'C'	B'C	BC	BC'
A'	0	0	1	0
A	0	1	1	1

S = AC+AB+BC

D)



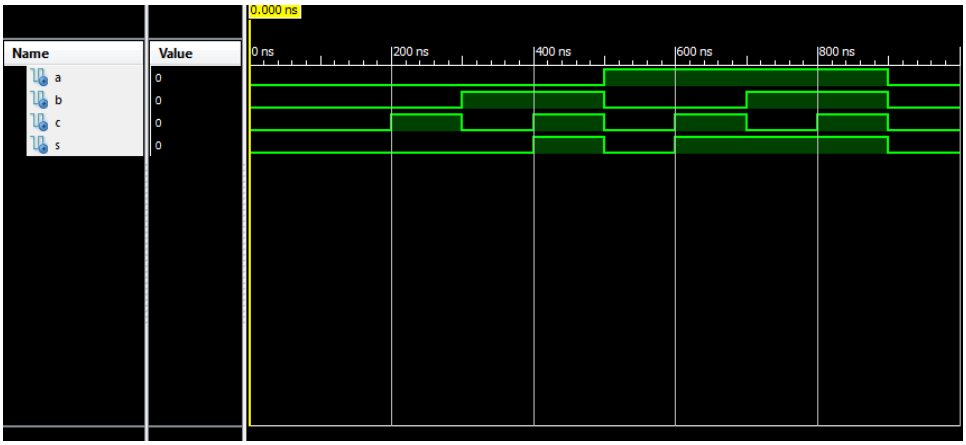
E)Modulo:

```
21  use IEEE.STD_LOGIC_1164.ALL;
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity modulo is
33      Port ( A : in  STD_LOGIC;
34             B : in  STD_LOGIC;
35             C : in  STD_LOGIC;
36             S : out  STD_LOGIC);
37
38  end modulo;
39
40  architecture Behavioral of modulo is
41
42  begin
43
44     S<= (A AND C) OR (A AND B) OR (B AND C);
45
46  end Behavioral;
47
48
```

Teste:

```
77     stim_proc: process
78     begin
79
80        wait for 100 ns;
81        A<= '0';
82        B<= '0';
83        C<= '0';
84        -- 001
85        wait for 100 ns;
86        A<= '0';
87        B<= '0';
88        C<= '1';
89        -- 010
90        wait for 100 ns;
91        A<= '0';
92        B<= '1';
93        C<= '0';
94        -- 011
95        wait for 100 ns;
96        A<= '0';
97        B<= '1';
98        C<= '1';
99        -- 100
100       wait for 100 ns;
101       A<= '1';
102       B<= '0';
103       C<= '0';
104       -- 101
101       A<= '1';
102       B<= '0';
103       C<= '0';
104       -- 101
105       wait for 100 ns;
106       A<= '1';
107       B<= '0';
108       C<= '1';
109       -- 110
110       wait for 100 ns;
111       A<= '1';
112       B<= '1';
113       C<= '0';
114       -- 111
115       wait for 100 ns;
116       A<= '1';
117       B<= '1';
118       C<= '1';
119       -- 000
120       wait for 100 ns;
121       A<= '0';
122       B<= '0';
123       C<= '0';
124
125       wait;
126    end process;
127
128 END;
```

Gráfico:



3) S= [(AB+D)'+(CD)'] + [(B'+(ADBC)'+DD)']

Modulo:

```
22
23  -- Uncomment the following library declaration if using
24  -- arithmetic functions with Signed or Unsigned values
25  --use IEEE.NUMERIC_STD.ALL;
26
27  -- Uncomment the following library declaration if instantiating
28  -- any Xilinx primitives in this code.
29  --library UNISIM;
30  --use UNISIM.VComponents.all;
31
32  entity modulo is
33      Port ( A : in  STD_LOGIC;
34             B : in  STD_LOGIC;
35             C : in  STD_LOGIC;
36             D : in  STD_LOGIC;
37             S : out  STD_LOGIC);
38
39  end modulo;
40
41  architecture Behavioral of modulo is
42
43  begin
44
45     S<= (((NOT((A AND B)OR D)) OR (NOT(C AND D)))  OR (((NOT B) OR (NOT(A AND D AND B AND C))) OR (NOT(D AND D))));
46
47  end Behavioral;
48
49
```

Teste:

```
79    stim_proc: process
80    begin
81
82       wait for 100 ns;
83       A<= '0';
84       B<= '0';
85       C<= '0';
86       D<= '0';
87       -- 0001
88       wait for 100 ns;
89       A<= '0';
90       B<= '0';
91       C<= '0';
92       D<= '1';
93       -- 0010
94       wait for 100 ns;
95       A<= '0';
96       B<= '0';
97       C<= '1';
98       D<= '0';
99       -- 0011
100      wait for 100 ns;
101      A<= '0';
102      B<= '0';
103      C<= '1';
104      D<= '1';
105      -- 0100
106      wait for 100 ns;
```

• • •

```
160      -- 1101
161      wait for 100 ns;
162      A<= '1';
163      B<= '1';
164      C<= '0';
165      D<= '1';
166      -- 1110
167      wait for 100 ns;
168      A<= '1';
169      B<= '1';
170      C<= '1';
171      D<= '0';
172      -- 1111
173      wait for 100 ns;
174      A<= '1';
175      B<= '1';
176      C<= '1';
177      D<= '1';
178      -- 0000
179      wait for 100 ns;
180      A<= '0';
181      B<= '0';
182      C<= '0';
183      D<= '0';
184      wait;
185   end process;
186
187   END;
```

Gráfico: