Eletrônica Digital I

Capítulo V
Multiplex e Demultiplex

Aula O – Circuitos Multiplexadores e Demultiplexadores

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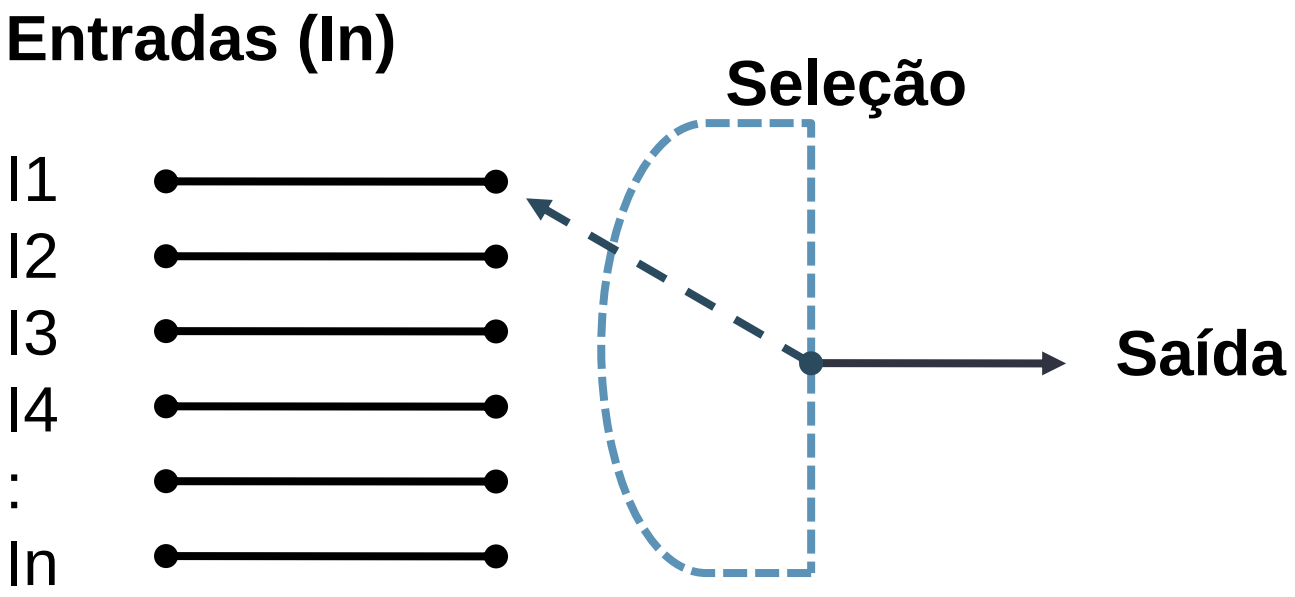
Inatel

Circuitos Multiplex - MUX

- O circuito multiplex é utilizado para enviarmos as informações contidas em vários canais (entradas), a uma única saída. Sendo esse circuito utilizado nos sistemas celulares, transmissão PDH, SDH, e outros.

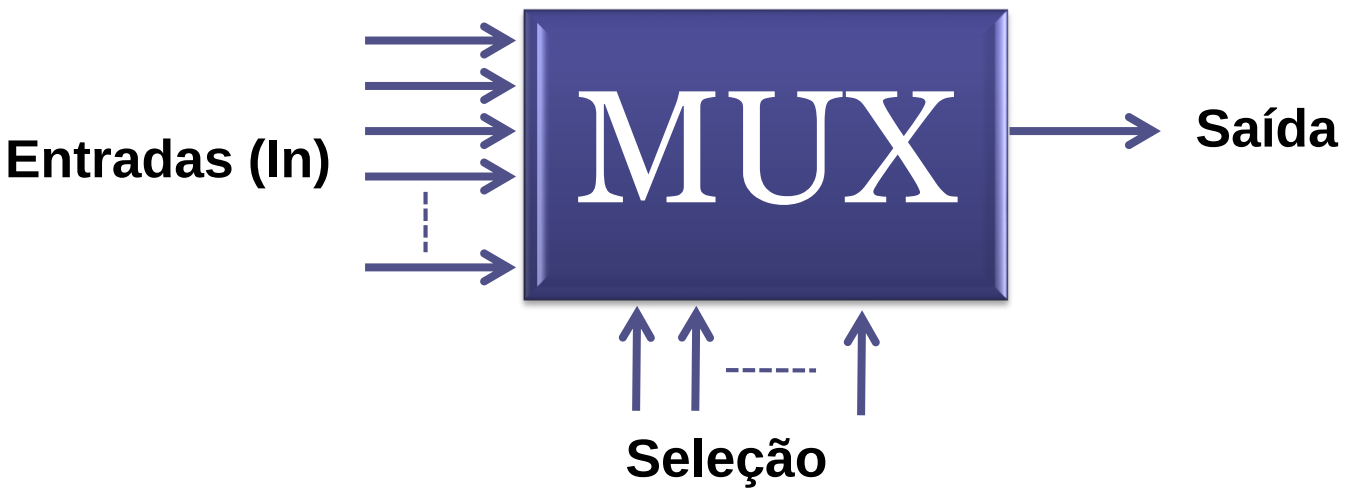
Circuitos Multiplex - MUX

- Diagrama



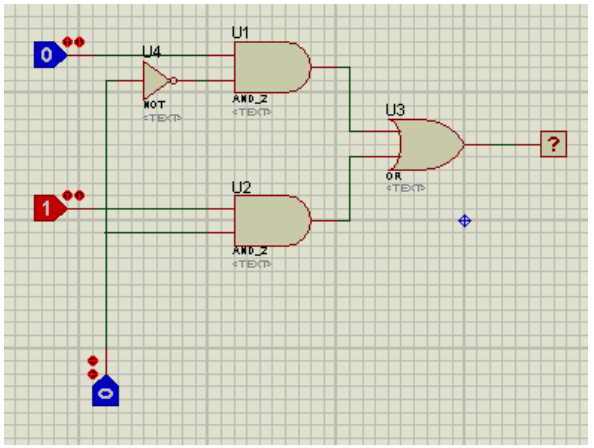
Circuitos Multiplex - MUX

- Diagrama:

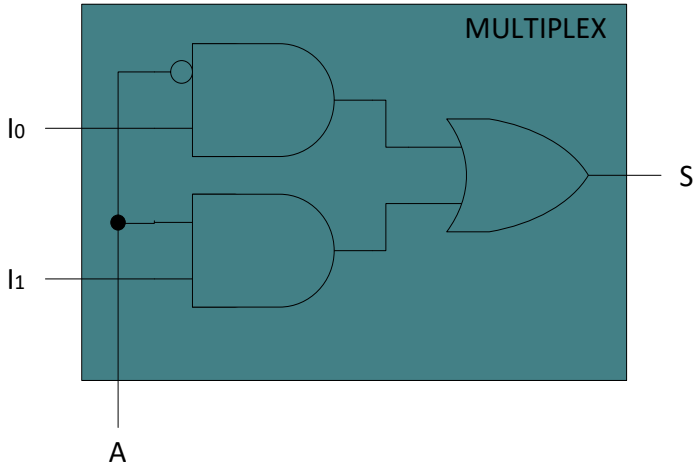


Circuitos Multiplex - MUX

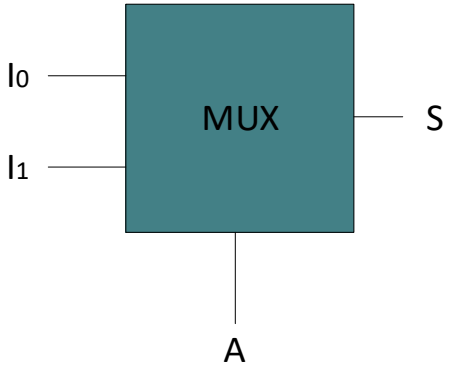
- MUX 2 x 1



Entrada A	Saída S
0	I0
1	I1



Circuito Lógico



Bloco Lógico

Circuitos Multiplex - MUX

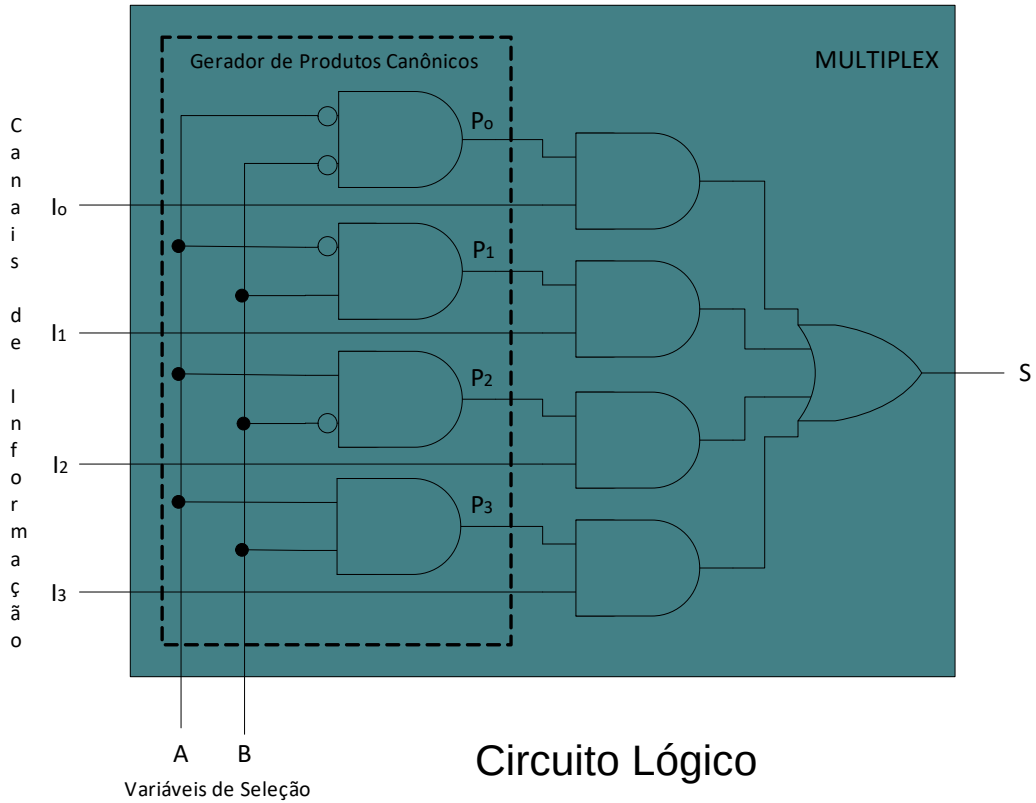
- Tabela da verdade do MUX 4x1

Variáveis de Seleção		Saída
A	B	S
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

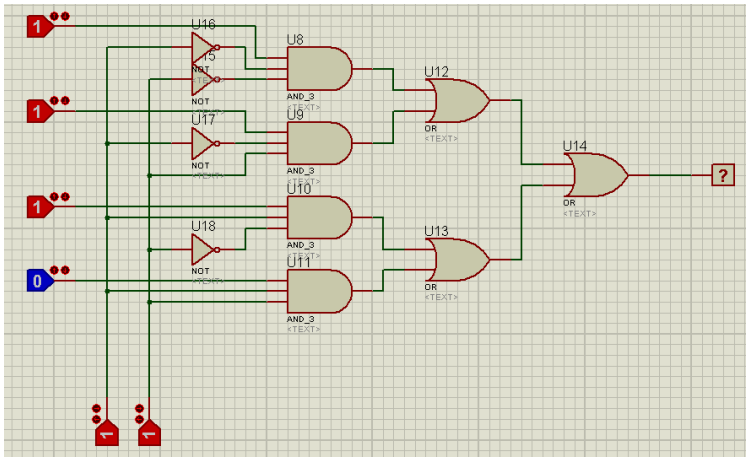
Tabela Verdade

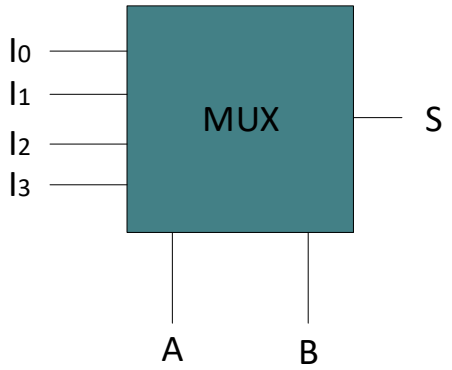
Circuitos Multiplex – 4x1

- Circuito Lógico do Mux 4 x 1



Circuito Lógico





Bloco Lógico

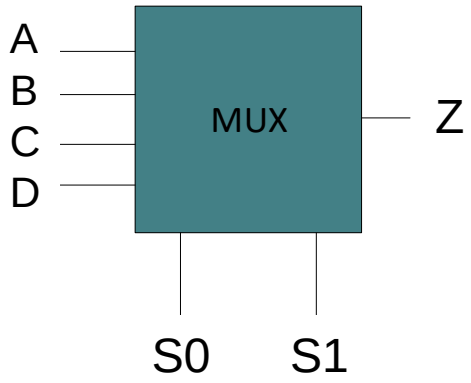
Em VHDL:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity mux_4to1 is
 port(

      A,B,C,D : in STD_LOGIC;
      S0,S1: in STD_LOGIC;
      Z: out STD_LOGIC
  );
end mux_4to1;

architecture bhv of mux_4to1 is
begin
process (A,B,C,D,S0,S1) is
begin
  if (S0 =´0´and S1=´0´) then
  Z<= A;
  elsif (S0 =´1´and S1=´0´) then
  Z<= B;
  elsif (S0 =´0´and S1=´1´) then
  Z<= C;
  elsif (S0 =´1´and S1=´1´) then
  Z<= D;
  end if;
  end process;
  end bhv;
```



Circuitos Multiplex

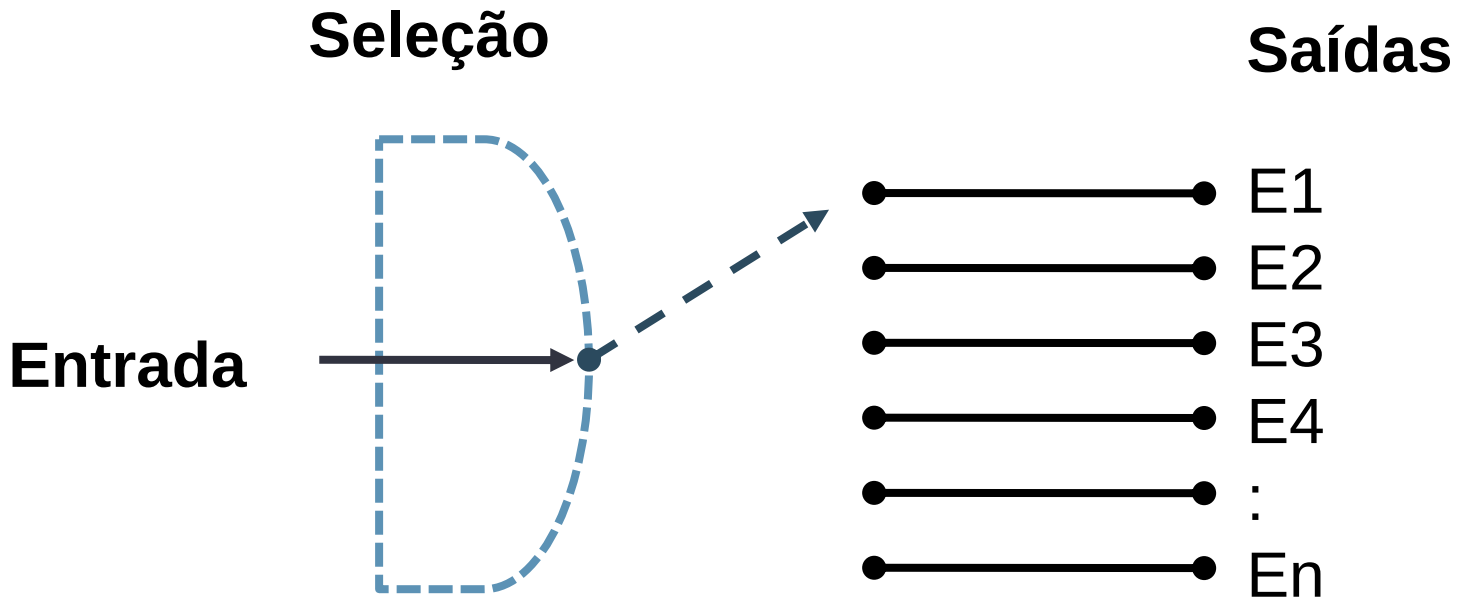
- Exercício:
  - Monte um circuito multiplex 8x1.

?

Circuitos Demultiplex - DEMUX

- Entende -se por demultiplex como sendo o bloco que efetua a função inversa ao multiplex, ou seja, a de enviar informações contidas em um canal a vários canais de saída.

Circuitos Demultiplex - DEMUX



Circuitos Demultiplex - DEMUX

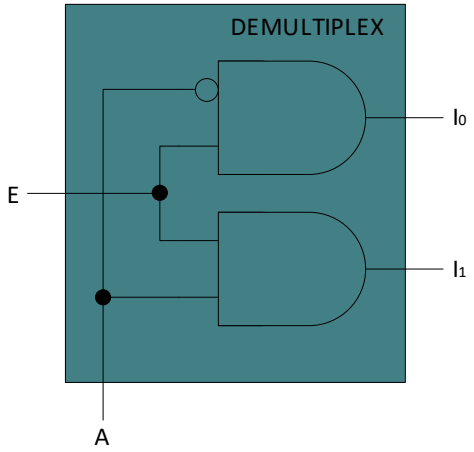
- Diagrama do Demux

Circuitos Demultiplex - DEMUX

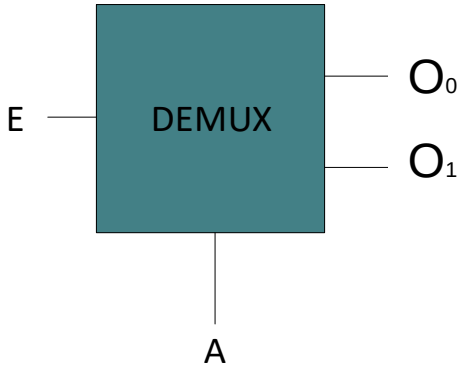
- Circuito Demux 1/2

Variável de Seleção	Canais de Informação (Out)	
A	O^0	O^1
0	E	0
1	0	E

Tabela Verdade

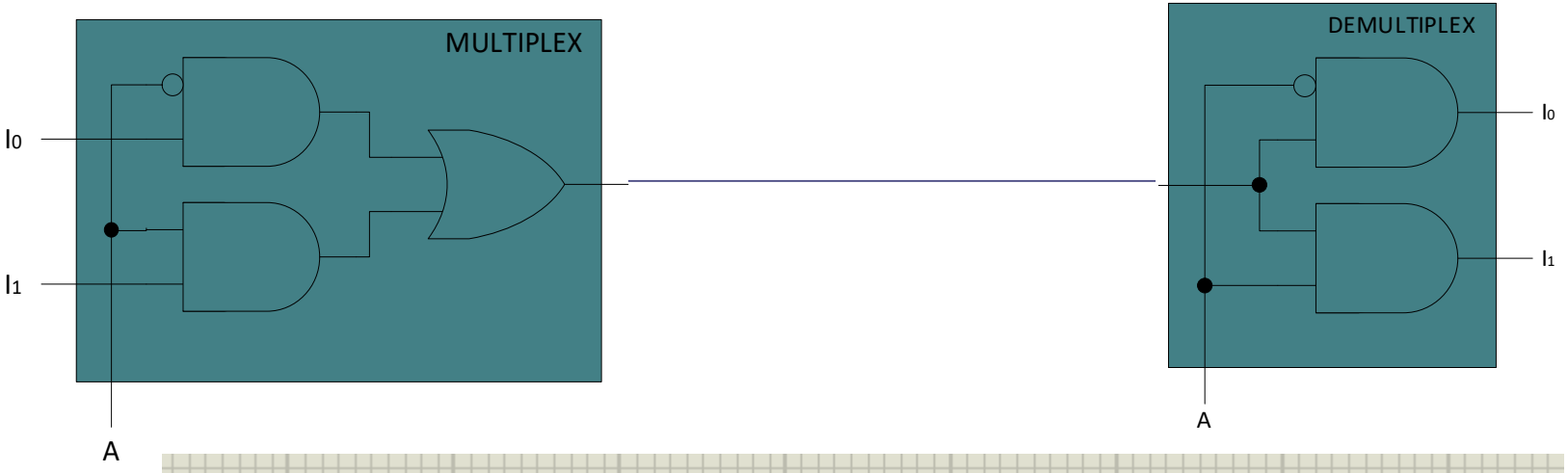


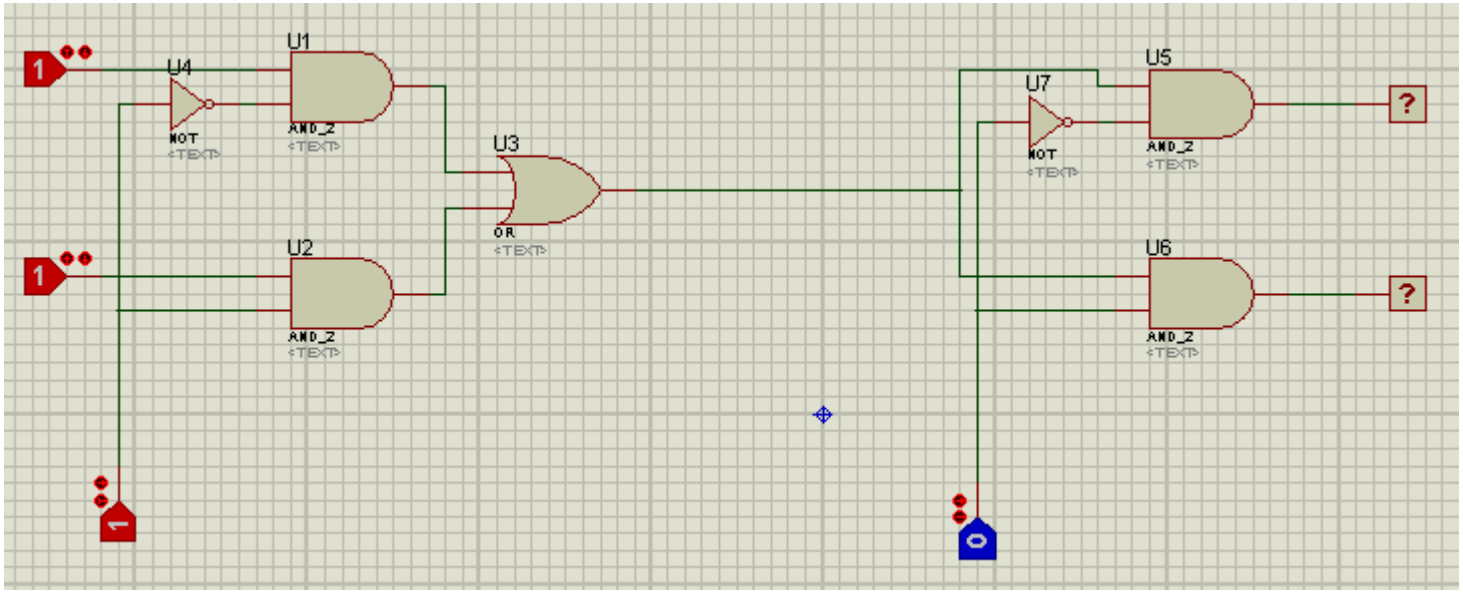
Circuito Lógico



Bloco Lógico

Circuito MUX e DEMUX



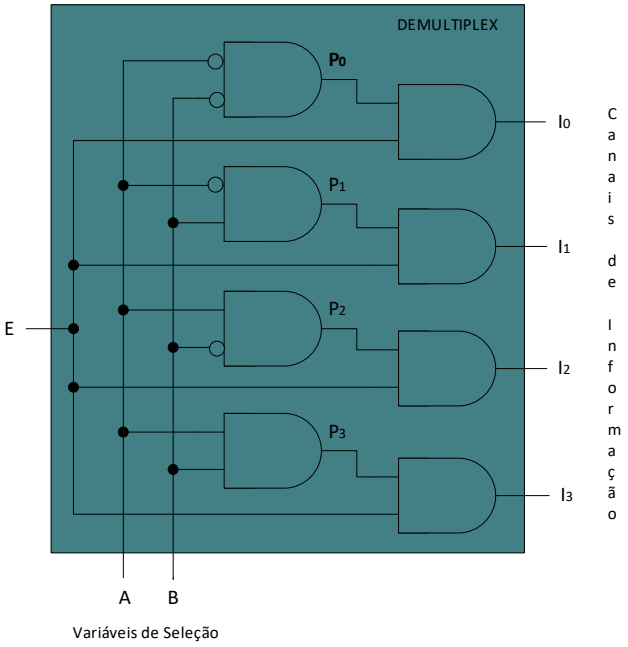


Circuitos Demultiplex - DEMUX

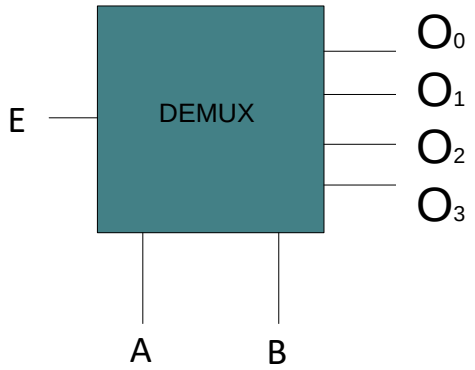
- Circuito do Demux 1/4

Variáveis de Seleção		Canais de Saída (Out)			
A	B	O^0	O^1	O^2	O^3
0	0	E	0	0	0
0	1	0	E	0	0
1	0	0	0	E	0
1	1	0	0	0	E

Tabela Verdade



Circuito Lógico



Bloco Lógico

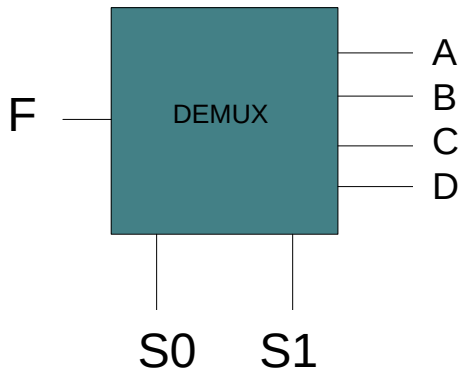
Em VHDL:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity demux_1to4 is
 port(

 F : in STD_LOGIC;
 S0,S1: in STD_LOGIC;
 A,B,C,D: out STD_LOGIC
 );
end demux_1to4;

architecture bhv of demux_1to4 is
begin
process (F,S0,S1) is
begin
if (S0 =´0´and S1=´0´) then
A<= F;
elsif (S0 =´1´and S1=´0´) then
B<= F;
elsif (S0 =´0´and S1=´1´) then
C<= F;
elsif (S0 =´1´and S1=´1´) then
D<= F;
end if;
end process;
end bhv;
```



Circuitos Demultiplex - DEMUX

- Exercício:
  - Monte um circuito demultiplex 1/8.
  - Monte um circuito completo MUX 4x1 e DEMUX 4/1. Teste alterando as chaves de entrada

Bons Estudos

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