RELATÓRIO 1 RESOLUÇÃO

QUESTÃO 1

A)

$$S = \overline{\overline{AB}} + [\overline{AC} \oplus (B + C)]$$

B)

Módulo

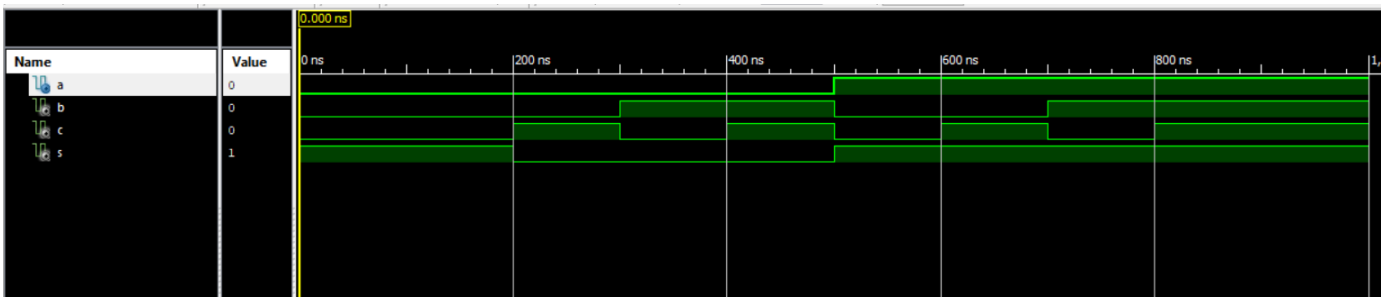
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Questaol is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           C : in  STD_LOGIC;
           S : out  STD_LOGIC);
end Questaol;

architecture Behavioral of Questaol is
Signal S1,S2,S3,S4: STD_LOGIC;

begin
S1 <= not(not(A and B));
S2 <= not(A and C);
S3 <= C or B;
S4 <= S2 xor S3;
S <= S1 or S4;

end Behavioral;
```

Teste

```
41
42      COMPONENT Questaol
43      PORT(
44           A : IN  std_logic;
45           B : IN  std_logic;
46           C : IN  std_logic;
47           S : OUT  std_logic
48          );
49      END COMPONENT;
50
51
52     --Inputs
53     signal A : std_logic := '0';
54     signal B : std_logic := '0';
55     signal C : std_logic := '0';
56
57     --Outputs
58     signal S : std_logic;
59     -- No clocks detected in port list. Replace <clock> below with
60     -- appropriate port name
61
62
63
64  BEGIN
65
66     -- Instantiate the Unit Under Test (UUT)
67     uut: Questaol PORT MAP (
68            A => A,
69            B => B,
70            C => C,
71            S => S
72          );
```

```
        -- hold reset state for 100 ns.
        wait for 100 ns;
        A <= '0';
        B <= '0';
        C <= '0';
        wait for 100 ns;
        A <= '0';
        B <= '0';
        C <= '1';
        wait for 100 ns;
        A <= '0';
        B <= '1';
        C <= '0';
        wait for 100 ns;
        A <= '0';
        B <= '1';
        C <= '1';
        wait for 100 ns;
        A <= '1';
        B <= '0';
        C <= '0';
        wait for 100 ns;
        A <= '1';
        B <= '0';
        C <= '1';
        wait for 100 ns;
        A <= '1';
        B <= '1';
        C <= '0';
        wait for 100 ns;
        A <= '1';
        B <= '1';
        C <= '1';
        wait for 100 ns;
```

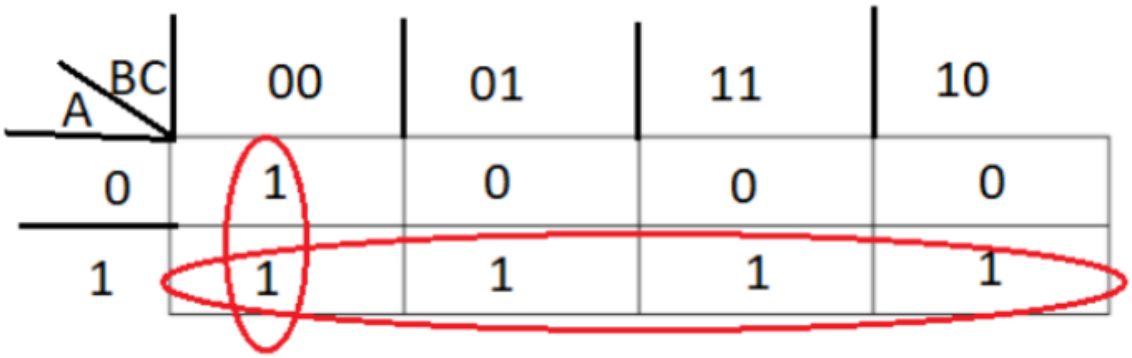
Simulação



C)

A	B	C	S
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

D)



$S = A + \overline{B}\,\overline{C}$

E)

$$S = \overline{\overline{A}\,\overline{B}} + [\overline{A}\,\overline{C} \oplus (B + C)]$$

$$S = AB + [\overline{\overline{A}\,\overline{C}}*(B+C) + \overline{A}\,\overline{C}*\overline{(B + C)}]$$

$$S = AB + [\,ACB + AC + \overline{A}\,\overline{C}*(\overline{B}\,\overline{C})]$$

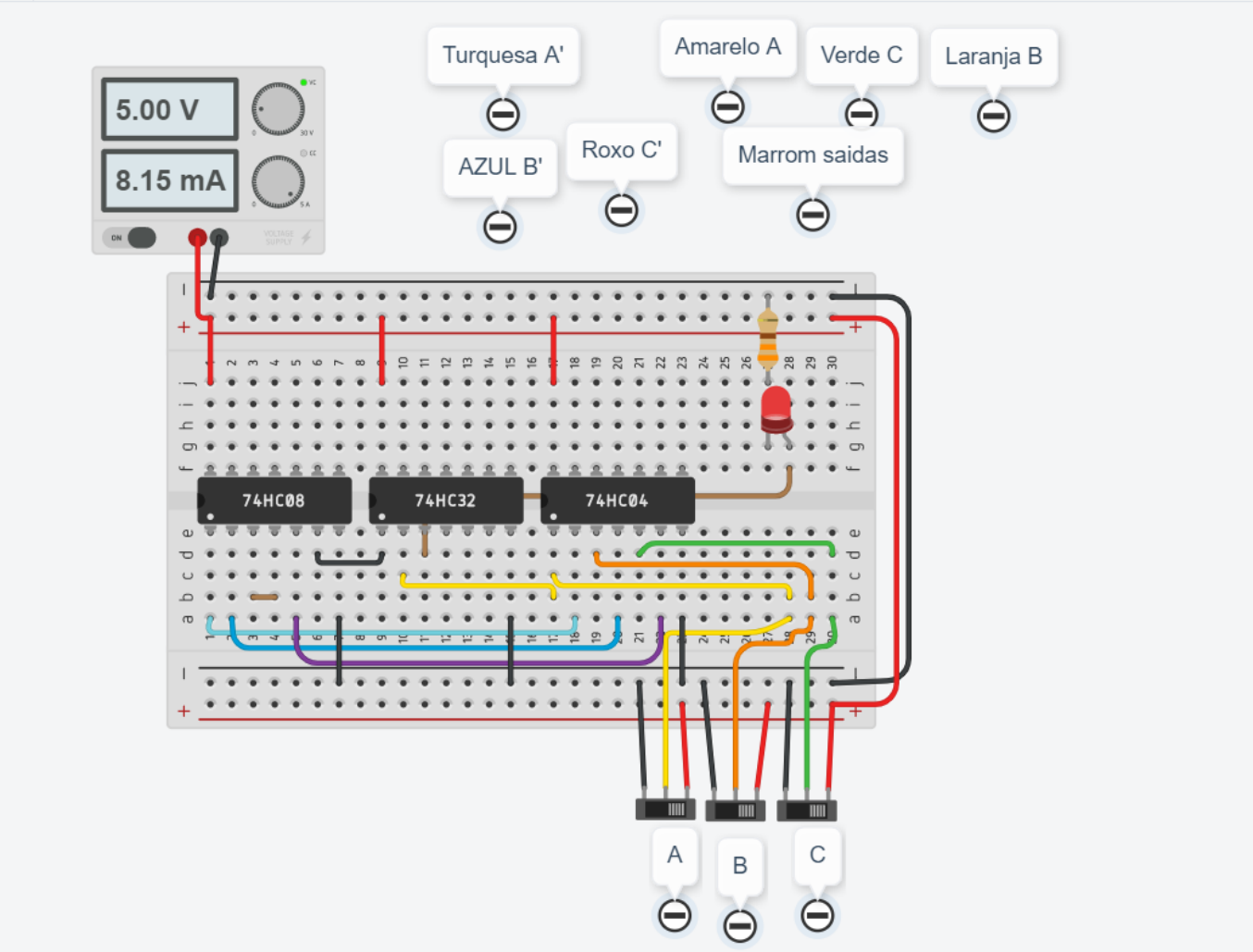
$$S = AB + [ACB + AC + (\overline{A}+\overline{C})(\overline{B}\,\overline{C})$$

$$S = AB + AC + \overline{A}\,\overline{B}\,\overline{C} + \overline{B}\,\overline{C}$$

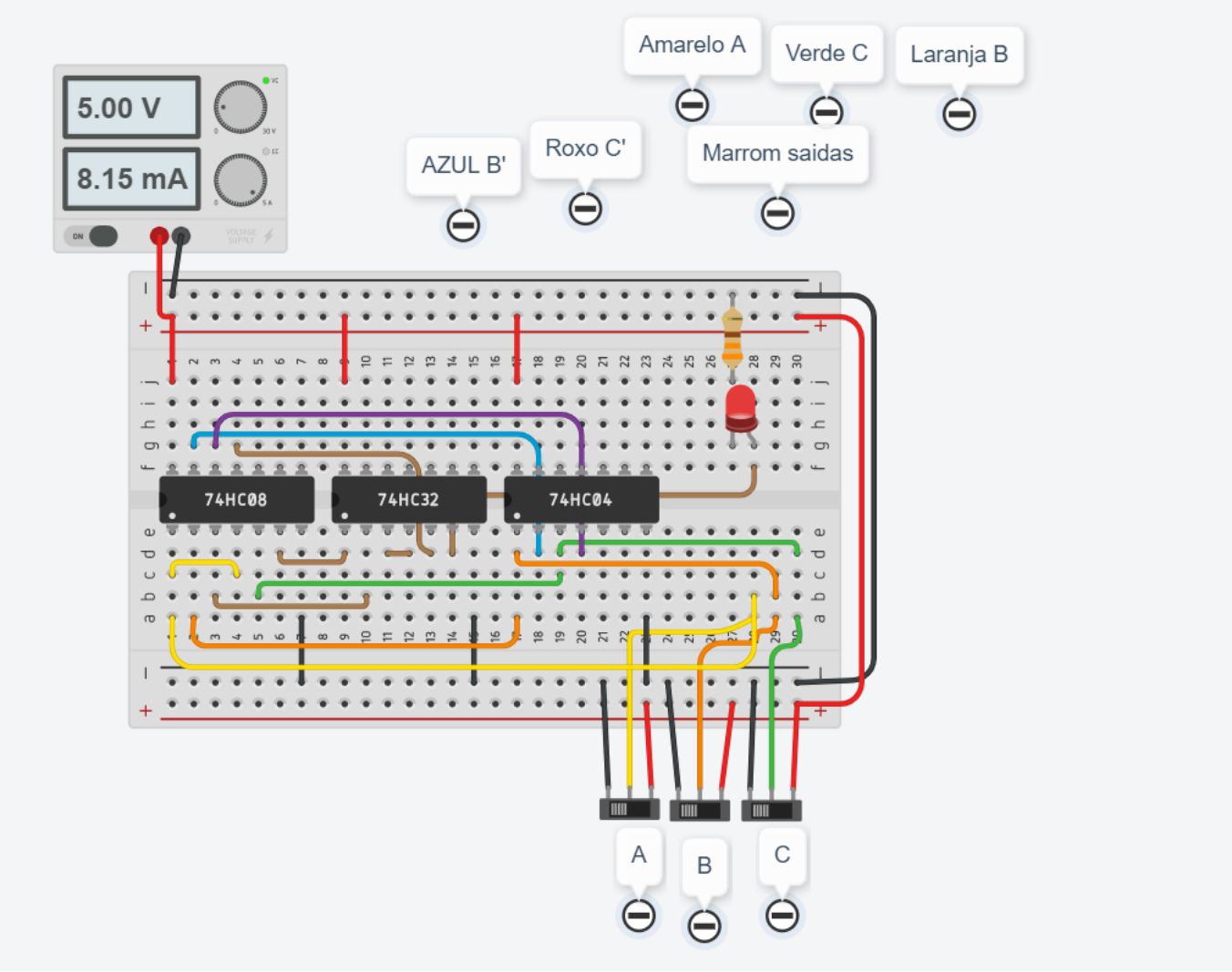
$$\mathbf{S = AB + AC + \overline{B}\,\overline{C}}$$

$$\mathbf{S = A(B + C) + \overline{B}\,\overline{C}} \xrightarrow{\text{Morgan}} \mathbf{S = A + \overline{B}\,\overline{C}}$$

F)Karnaugh


Turquesa A'
Amarelo A
Verde C
Laranja B
AZUL B'
Roxo C'
Marrom saidas
5.00 V
8.15 mA
74HC08
74HC32
74HC04
A
B
C

Boole



2)

A)

Mux 4:1 com Enable

E	A	B	S
0	0	0	X0
0	0	1	X1
0	1	0	X2
0	1	1	X3
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

B)

Modulo

```
30  --use UNISIM.VComponents.all;
31
32  entity Questo2B is
33      Port ( E : in  STD_LOGIC;
34             A : in  STD_LOGIC;
35             X0 : in  STD_LOGIC;
36             X1 : in  STD_LOGIC;
37             S : out  STD_LOGIC);
38  end Questo2B;
39
40  architecture Behavioral of Questo2B is
41  Signal SX0, SX1: STD_Logic;
42
43  begin
44  SX0 <= not(A) and E and X0;
45  SX1 <= A and E and X1;
46  S <= SX0 or SX1;
47
48
49  end Behavioral;
50
```

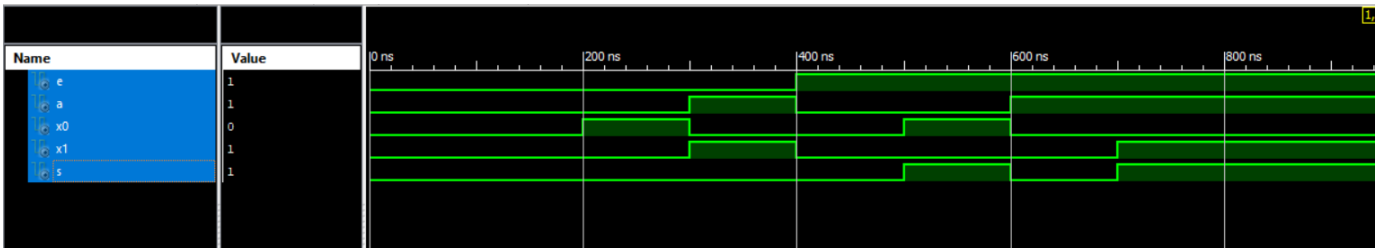
Teste

```
34
35  ENTITY Questao2bteste IS
36  END Questao2bteste;
37
38  ARCHITECTURE behavior OF Questao2bteste IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT Questo2B
43      PORT(
44           E : IN  std_logic;
45           A : IN  std_logic;
46           X0 : IN  std_logic;
47           X1 : IN  std_logic;
48           S : OUT  std_logic
49          );
50      END COMPONENT;
51
52
53     --Inputs
54     signal E : std_logic := '0';
55     signal A : std_logic := '0';
56     signal X0 : std_logic := '0';
57     signal X1 : std_logic := '0';
58
59     --Outputs
60     signal S : std_logic;
61     -- No clocks detected in port list. Replace <clock> below with
62     -- appropriate port name
63
64
65  BEGIN
66
```

```
BEGIN

   -- Instantiate the Unit Under Test (UUT)
   uut: Questo2B PORT MAP (
          E => E,
          A => A,
          X0 => X0,
          X1 => X1,
          S => S
        );



   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;
      E <= '0';
      A <= '0';
      X0 <= '0';
      X1 <= '0';
      wait for 100 ns;
      E <= '0';
      A <= '0';
      X0 <= '1';
      X1 <= '0';
      wait for 100 ns;
      E <= '0';
      A <= '1';
      X0 <= '0';
      X1 <= '1';
      wait for 100 ns;
```

```
 93        wait for 100 ns;
 94        E <= '0';
 95        A <= '1';
 96        X0 <= '0';
 97        X1 <= '1';
 98        wait for 100 ns;
 99        E <= '1';
100        A <= '0';
101        X0 <= '0';
102        X1 <= '0';
103        wait for 100 ns;
104        E <= '1';
105        A <= '0';
106        X0 <= '1';
107        X1 <= '0';
108        wait for 100 ns;
109        E <= '1';
110        A <= '1';
111        X0 <= '0';
112        X1 <= '0';
113        wait for 100 ns;
114        E <= '1';
115        A <= '1';
116        X0 <= '0';
117        X1 <= '1';
118
119
120
121        -- insert stimulus here
122
123        wait;
124     end process;
125
126  END;
```

Simulação



C)

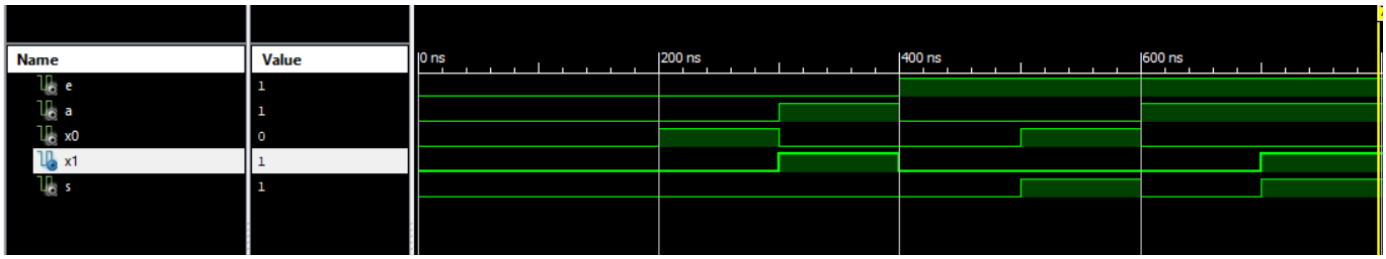
Modulo

```
31
32  entity Questao2C is
33      Port ( E : in  STD_LOGIC;
34             A : in  STD_LOGIC;
35             X0 : in  STD_LOGIC;
36             X1 : in  STD_LOGIC;
37             S : out  STD_LOGIC);
38  end Questao2C;
39
40  architecture Behavioral of Questao2C is
41
42
43  begin
44    process(E,A,X0,X1)
45  begin
46   if(E = '0') THEN
47      S <= '0';
48   else
49      if(A = '0')THEN
50         S <= X0;
51      else
52         S <= X1;
53      end if;
54
55   end if;
56   end process;
57
```

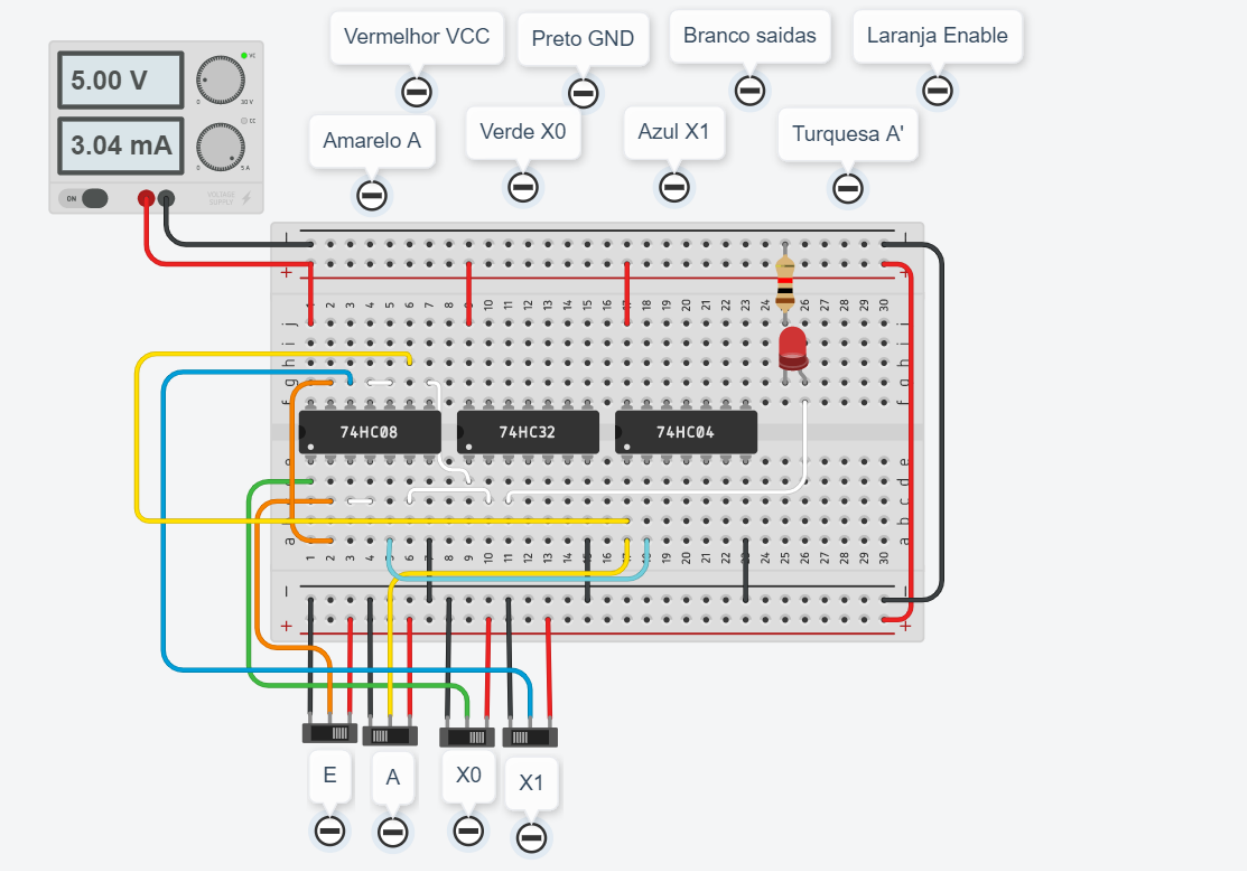
Teste

```
    -- hold reset state for 100 ns.
    wait for 100 ns;
    E <= '0';
    A <= '0';
    X0 <= '0';
    X1 <= '0';
    wait for 100 ns;
    E <= '0';
    A <= '0';
    X0 <= '1';
    X1 <= '0';
    wait for 100 ns;
    E <= '0';
    A <= '1';
    X0 <= '0';
    X1 <= '1';
    wait for 100 ns;
    E <= '1';
    A <= '0';
    X0 <= '0';
    X1 <= '0';
    wait for 100 ns;
    E <= '1';
    A <= '0';
    X0 <= '1';
    X1 <= '0';
    wait for 100 ns;
    E <= '1';
    A <= '1';
    X0 <= '0';
    X1 <= '0';
    wait for 100 ns;
    E <= '1';
    A <= '1';
    X0 <= '0';
    X1 <= '1';
```

Simulação



D)


5.00 V
3.04 mA
Vermelhor VCC
Preto GND
Branco saidas
Laranja Enable
Amarelo A
Verde X0
Azul X1
Turquesa A'
74HC08
74HC32
74HC04
E
A
X0
X1