Eletrônica Digital I

VHDL

Aula L – Software VHDL

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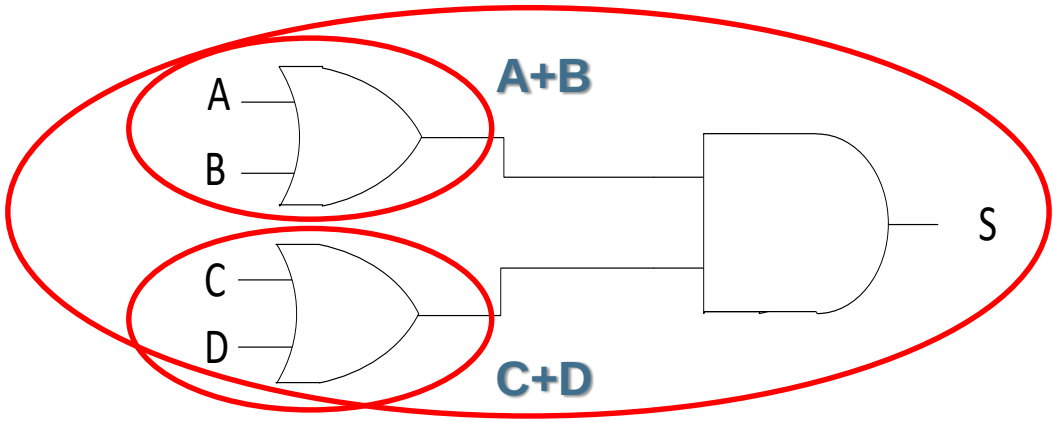
Expressões Booleanas e Circuitos Lógicos

Exemplo:



S= (A+B) . (C+D)

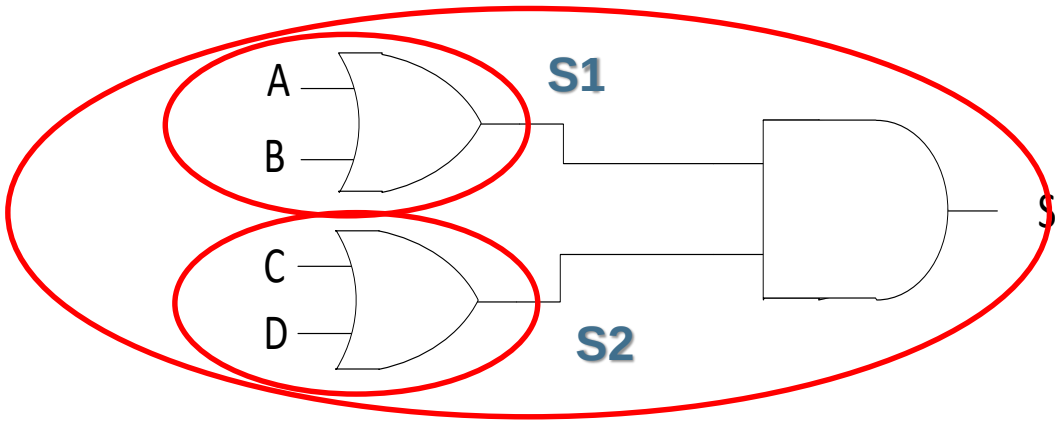
Em VHDL:

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL;
3
4   ENTITY exemplo2 IS
5   PORT (
6             A,B,C,D : IN BIT;
7             S : OUT BIT;
8             );
9   END ENTITY exemplo2;
10
11  ARCHITECTURE logic OF exemplo2 IS
12            SIGNAL S1,S2 : BIT;
13  BEGIN
14            S1 <= A OR B;
15            S2 <= C OR D;
16            S <= S1 AND S2;
17  END ARCHITECTURE logic;
18
19
```

Outra Maneira:

S <= (A OR B) AND (C OR D)

Exemplo2:



Expressões Booleanas e Circuitos Lógicos

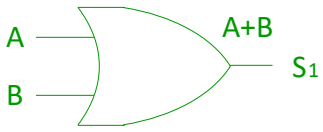
- Circuitos Lógicos obtidos de Expressões Booleanas :

  De maneira análoga ao que utilizamos para obter a expressão booleana que um circuito lógico executa, podemos desenhar um circuito lógico que executa a expressão booleana.

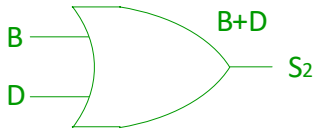
S1 S2

Exemplo: O circuito que representa a expressão booleana **S= (A+B).C.(B+D)**

S

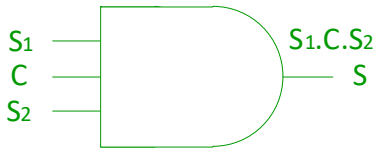


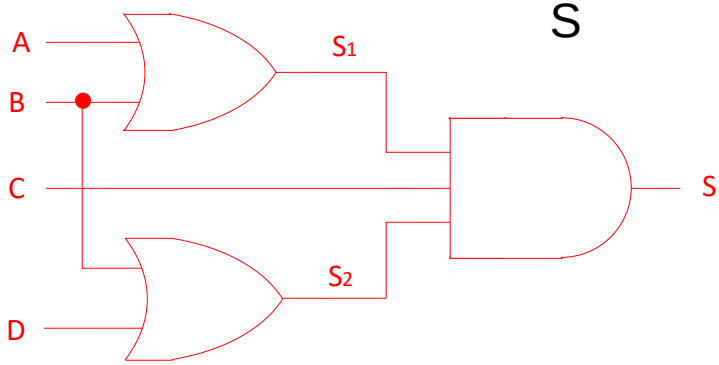
S1=(A+B)



$S_2 = (B+D)$

$S = S_1.C.S_2$

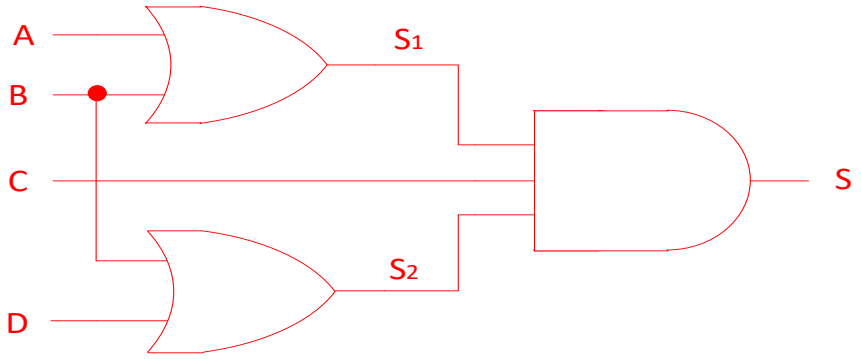




Em VHDL:

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL
3
4   ENTITY exemplo3 IS
5   PORT (
6             A,B,C,D : IN BIT;
7             S : OUT BIT;
8             );
9   END ENTITY exemplo3;
10
11
12  ARCHITECTURE logic OF exemplo3 IS
13            SIGNAL S1,S2 : BIT;
14  BEGIN
15            S1 <= A OR B;
16            S2 <= B OR D;
17            S <= S1 AND C AND S2;
18  END ARCHITECTURE logic;
```

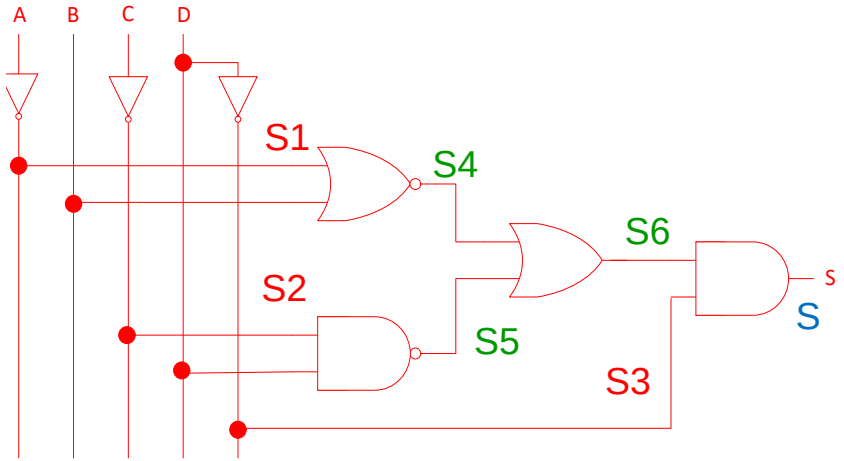
Exemplo3:



Em VHDL:

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL
3
4   ENTITY exemplo4 IS
5   PORT (
6             A,B,C,D : IN BIT;
7             S : OUT BIT;
8             );
9   END ENTITY exemplo4;
10
11  ARCHITECTURE logic OF exemplo4 IS
12            SIGNAL S1,S2,S3,S4,S5,S6 : BIT;
13  BEGIN
14            S1 <= NOT A;
15            S2 <= NOT C;
16            S3 <= NOT D;
17            S4 <= S1 NOR B;
18            S5 <= S2 NAND D;
19            S6 <=  S4  OR S5;
20            S <= S6 AND S3
21  END ARCHITECTURE logic;
```

Exemplo4:



Exercício 1

$$S = A \cdot \overline{B} \cdot C + A \cdot \overline{D} + \overline{A} \cdot B \cdot D$$

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL
3
4   ENTITY exemplo4 IS
5   PORT (
6                   A,B,C,D : IN BIT;
7                     S: OUT BIT;
8             );
9   END ENTITY exemplo4;
10
11  ARCHITECTURE logic OF exemplo4 IS
12          SIGNAL     S1, S2, S3 : BIT;
13  BEGIN
14
15                S1 <= A AND (NOT B) AND C;
16                   S2 <= A AND (NOT D);
17                S3 <= (NOT A) AND B AND D;
18                   S <= S1 OR S2 OR S3;
19
20
21  END ARCHITECTURE logic;
```

Exercício 2

$$S = \overline{[(A + B) . C]} + \overline{[D . (B + C)]}$$

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL
3
4   ENTITY exemplo4 IS
5   PORT (
6                   A,B,C,D : IN BIT;
7                   S: OUT BIT;
8               );
9   END ENTITY exemplo4;
10
11  ARCHITECTURE logic OF exemplo4 IS
12          SIGNAL S1, S2, S3 : BIT;
13  BEGIN
14
15                  S1 <= A OR B;
16                S2 <= S1 NAND C;
17                  S3 <= B OR C;
18                S4 <= S3 NAND D;
19                  S <= S2 OR S4;
20
21  END ARCHITECTURE logic;
```

Simplificação:
S= A´B´+C´+D´

S1 : BIT;

S1 <= (NOT A) AND (NOTB);
S <= S1 OR (NOT C) OR (NOT D);

Exercício 3

$$S = \overline{\overline{[(\overline{A} \cdot B) + (C \cdot \overline{D})]} \cdot E + \overline{A} \cdot (A \cdot \overline{D} \cdot \overline{E} + C \cdot D \cdot E)}$$

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL
3
4   ENTITY exemplo4 IS
5   PORT (      A,B,C,D, E : IN BIT;
6                   S: OUT BIT;
7
8               );
9   END ENTITY exemplo4;
10
11  ARCHITECTURE logic OF exemplo4 IS
12          SIGNAL   S1, S2, S3, S4, S5, S6, S7, S8 : BIT;
13  BEGIN
14                          S1 <=  (NOT A) NAND B;
15                          S2 <= C NAND (NOT D);
16                          S3 <= S1 NOR S2;
17                          S4 <= S3 AND E;
18                  S5 <= A AND (NOT D) AND (NOT E);
19                          S6 <= C AND D AND E;
20                          S7 <= S5 OR S6;
21                          S8 <= (NOT A) AND S7;
                            S <= S4 OR S8;
    END ARCHITECTURE logic;
```

Simplificação:
S= A´BCE + A´CDE

S1 : BIT;

S1 <= (NOT A) AND B AND C AND E;
S2 <= (NOT A) AND C AND D AND E;
S <= S1 OR S2;

Exercício 4

$$S = \overline{(A \oplus B + \overline{B} \,.\, C \,.\, \overline{D})} \,.\, \overline{[\overline{(\overline{A} + B)} \,.\, D + \overline{B} \,.\, C + \overline{D}]} + \overline{A} \,.\, \overline{D}$$

```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL
3
4   ENTITY exemplo4 IS
5   PORT (
6             A,B,C,D, E : IN BIT;
7                 S: OUT BIT;
8              );
9   END ENTITY exemplo4;
10
11  ARCHITECTURE logic OF exemplo4 IS
12          SIGNAL          S1,S2,S3,S4,S5,S6,S7,S8,S9 : BIT;
13  BEGIN
                            S1 <= A XOR B;
14                          S2 <= (NOT B) AND C AND (NOT D);
15                          S3 <= S1 NOR S2;
16                          S4 <=(NOT A) NOR B;
17                          S5 <= S4 AND D;
18                          S6 <= (NOT B) AND C;
19                          S7 <= S5 NOR S6 NOR (NOT D);
20                          S8 <= S3 AND S7;
                            S9 <= (NOT A) AND (NOT D);
21                          S<= S8 OR S9;
    END ARCHITECTURE logic;
```

Bons Estudos

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