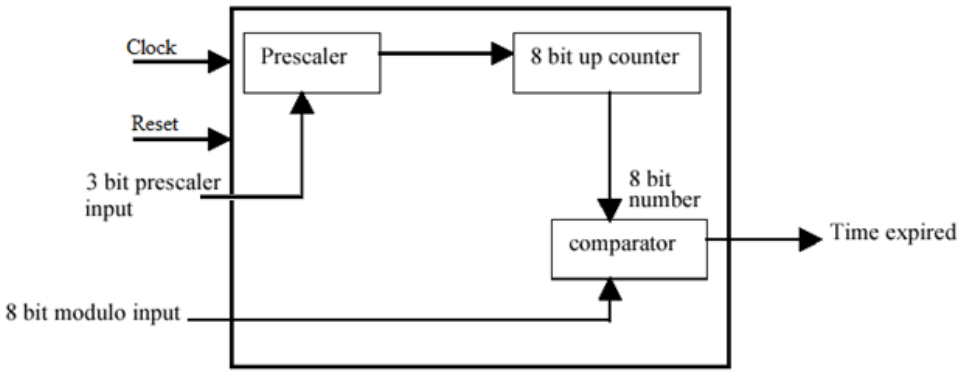
Timer

It is required to design a digital circuit for implementing Timer. The circuit is composed of a Counter, a Prescaler and a Comparator. Their interconnection and the system interface of the circuit to be designed is as follows:



The timer operates simply by setting the Prescaler to a value from 1 to 8, setting the module value to a number from 0 to 255, and simply supplying the circuit with the clock. The Timer expired output is set to 1 for a clock cycle at intervals determined by the Prescaler and module value.
In particular, the Prescaler counts the number of input clock cycles and outputs a pulse, of one clock cycle duration, when the number of clock cycles is a multiple of the Prescaler input value. The counter counts the number of input pulses. The comparator provides a high output when the two input data coincide.

You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions