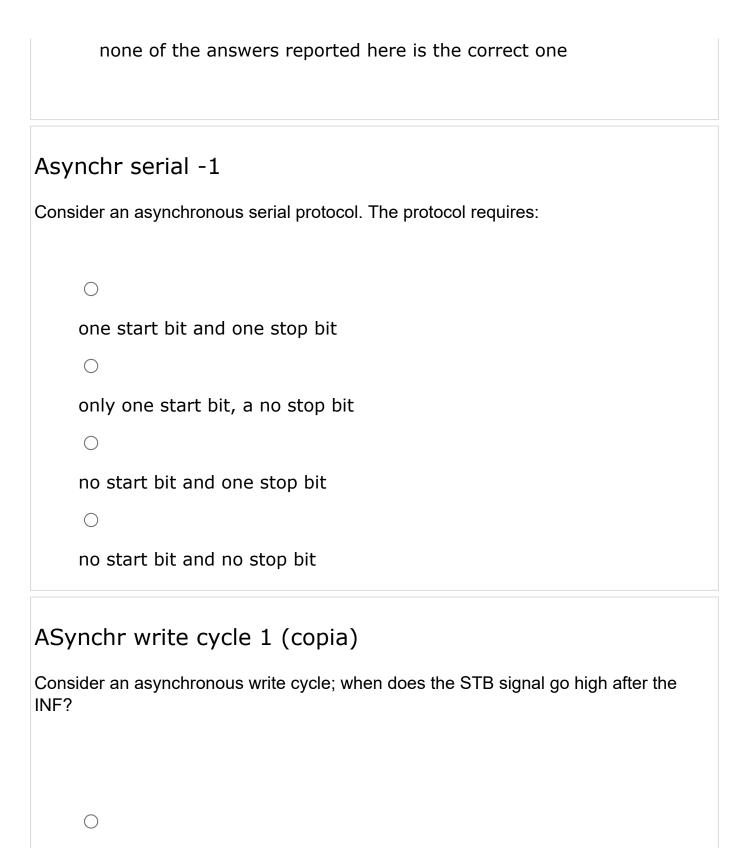
ADC pipeline		
The conversion time of a pipeline ADC with N bits:		
is not determined by the number of bits N		
0		
is proportional to N		
is proportional to 2 <sup>N</sup>		
is proportionalto 1/N		
ADC SAR circuit 1		
The conversion time Tc of a Successive Approximation Converter can be reduced of a actor 2 by:		
actor 2 by:		
actor 2 by:  O doubling the CK frequency of the SAR		
actor 2 by:  O doubling the CK frequency of the SAR		
actor 2 by:  Oubling the CK frequency of the SAR Odoubling the CK period of the SAR		



STB goes high after tk

STB goes high after tk+th

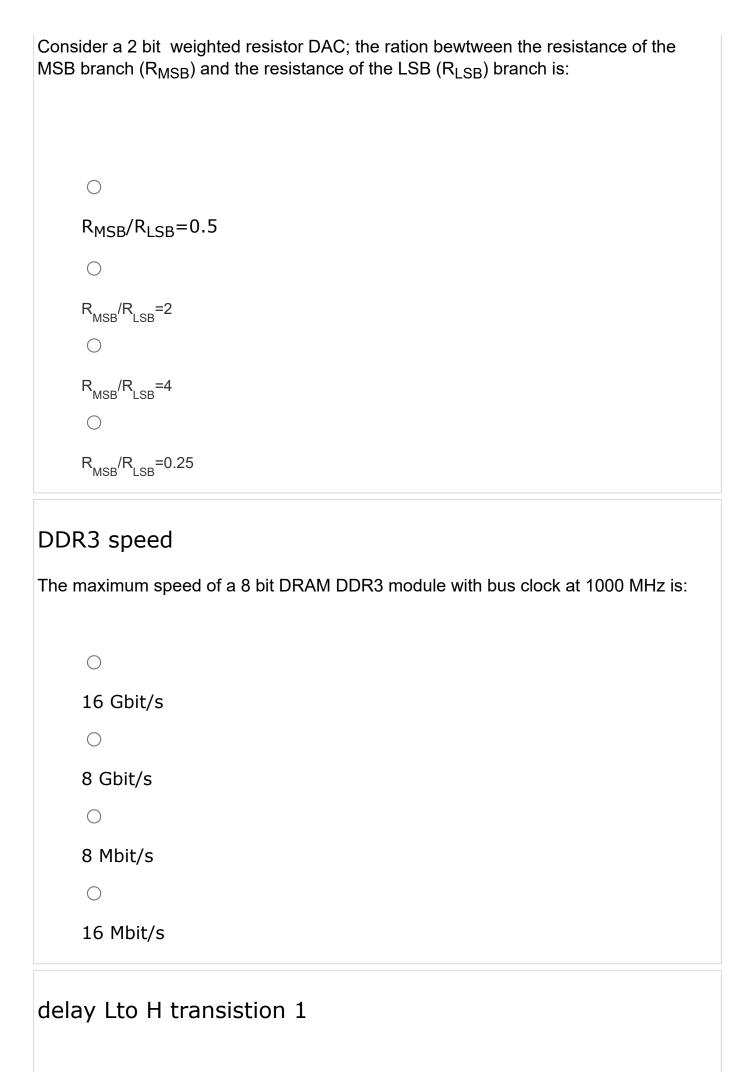
STB goes high after tk+tsu

 $\bigcirc$ 

 $\bigcirc$ 

 $\bigcirc$ 

buck regulator 1	
The output voltage of buck regulators is:	
$\circ$	
Vout <vin< td=""></vin<>	
Vout>Vin	
Vout=Vin	
Vout=2 Vin	
D-FF	
Consider a D-FF. Select the correct sentece:	
During the set-up time D must not change	
D must be always 1 during the set-up time	
D must be always 0 during the set-up time	
During the set-up time D must change no more than 2 times	
DAC resistenze pesate	



One logic gate with output resistance Ro is driving 4 inverters with input capacitance Ci=4pF. The propagation delay of a L→ H transitions is:
2.76·Ro·Ci
0.69·Ro·Ci
Ro·Ci
4·Ro·Ci
DRAM cell
A DRAM memory cell consists in:
one MOS and one capacitor
one FAMOS
6 MOS
one MOS and 2 capacitors
dynamic power vs f
If we divide by 2 the clock frequency of a CMOS digital circuit, the dynamic power consumption will change of a factor equal to:

0.5
2
4
0.25
ENOB 1
The ADC of a data acquisition system provides a SNRq=65.76dB, whereas the total SNR is degraded of other 10dB due to the non-idealities of the other blocks. Calculate the ENOB.
ENOB=9
ENOB=10
ENOB>10
ENOB<8
ENOB2
A data acquisistion system has a total SNR of 49.76dB. Calculate the ENOB.
ENOB=8

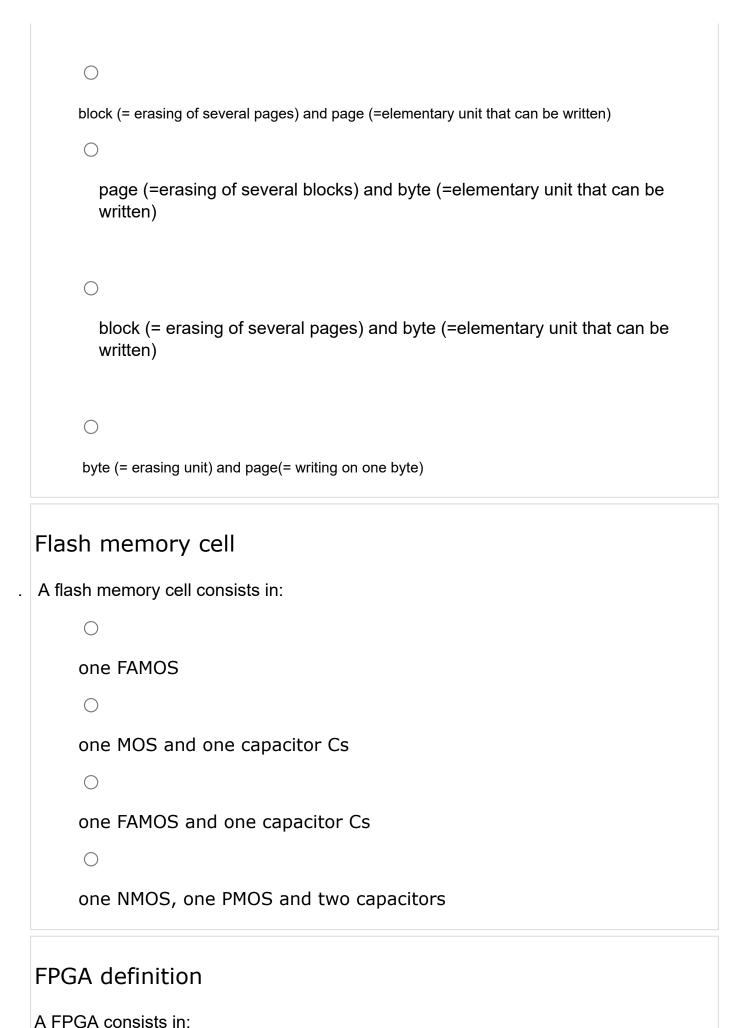
	ENOB=10
	ENOB<7
	ENOB>10
Erro	ore DAC resitenze pesate
	sider a 8 bit weighted resistors DAC. The resistor of the MSB branch has an error %. Which is the error that we find in the DAC characteristic?
	non-monotonicity error
	non linear error
	gain error
	differential error
FAN	10S 1
A FA	MOS when programmed
	has a threshold voltage higher than the threshold voltage of the FAMOS which is not programmed
	has a threshold voltage equal to the threshold voltage of the FAMOS which is not programmed

has a threshold voltage smaller than the threshold voltage of the FAMOS which is not programmed  has I <sub>DS</sub> higher than the not programmed FAMOS, when same V <sub>DS</sub> is applied
Fan out 1
The maximum number of CMOS logic gates that can be connected to a logic gate of same family is limited by:
the maximum acceptable delay for a state transition
the current I <sub>IH</sub>
the current I <sub>IL</sub>
the maximum static power consumption
Fan out 2
The maximum number of CMOS logic gates that can be connected to one CMOS logic gate of the same family is limited by:

 $\bigcirc$ 

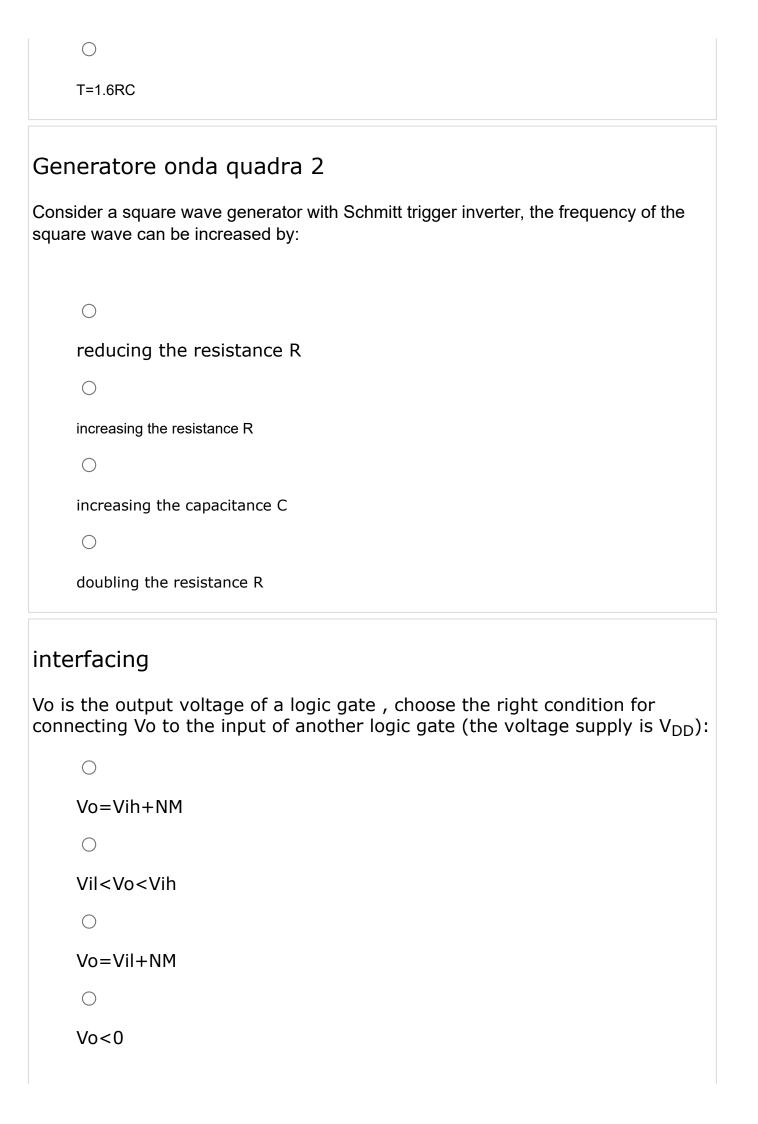
	the maximum acceptable delay for a logic state transition
	$\bigcirc$
	the maximum output current from the logic gate
	the voltage supply Vdd
	the maximum static power consumption
FF.	JK
Con: nave	sider a JK-FF with CK active on the falling edge and J=K=1; in this condition we
	the output toggles on the falling edge of the CK
	the FF is in memory state
	the output toggles on the rising edge of the CK
	the output is always Q=1
	ch mamany
ria:	sh memory

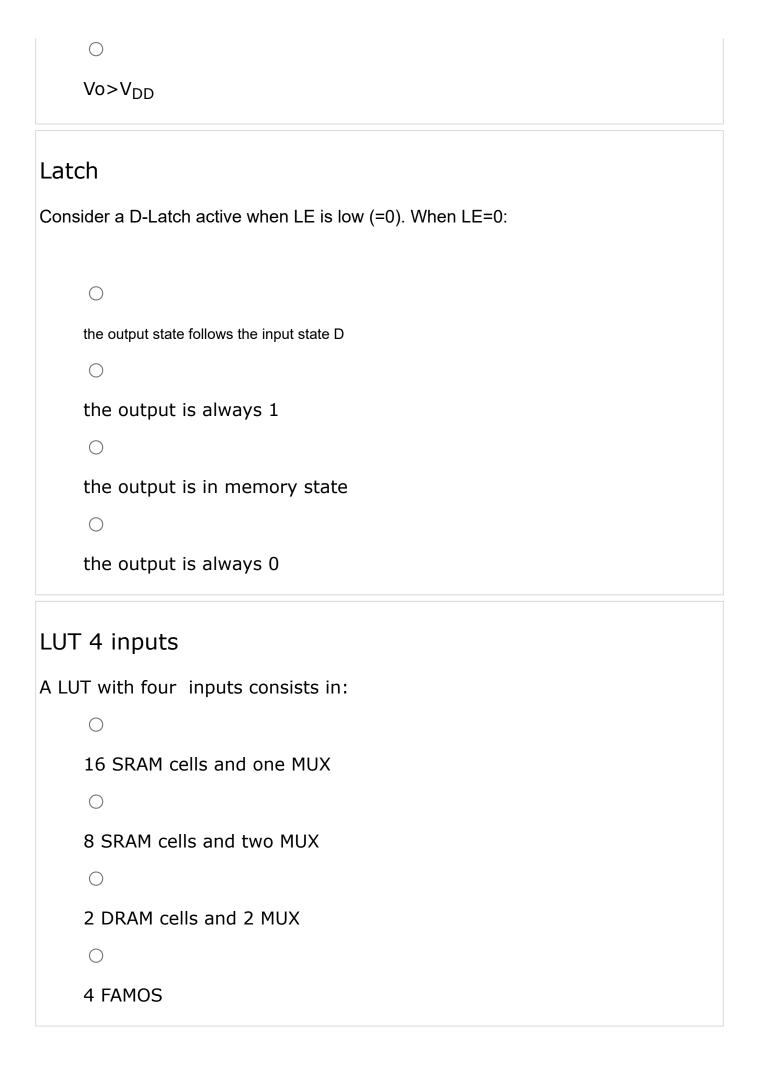
Consider a NAND flash memory; the elementary units for erasing and writing operations are:



LUT, MUX and registers	
Arrays of OR gates	
Arrays of AND gates	
Arrays of SRAM cells	
FPGA LUT 1	
To realize an FPGA-LUT of 2 inputs we need:	
4 SRAM cells and 1 MUX	
a ROM	
8 DRAM cells	
6 SRAM cells and 1 MUX	
FPGA, LUT	
Consider a FPGA; a Look-Up Table (LUT) with 3 inputs needs:	
8 SRAM memory cells	
8 FAMOS	

4 NAND gates and 8 NOR gates
8 NAND gates and 4 NOR gates
Full wave rectifier-1
If we substitute a full-wave rectifier with a half wave rectifier, the power associated to the ripple voltage noise will scale of a factor equal to:
4
2
0.5
0.25
Generatore onda quadra 1
Consider a square wave generator with Schmitt trigger inverter, the period T of the square wave can be approximated with
T=RC
T=0.69RC
T=2RC



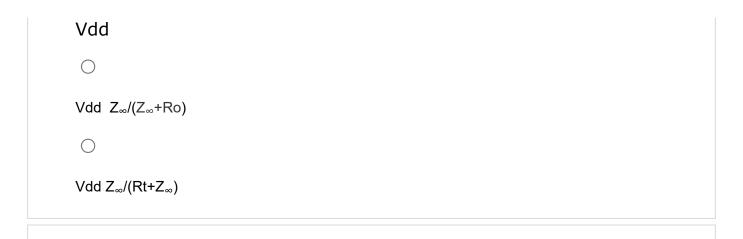


matched termination
The reflection coefficient of a transmission line terminated with a termination resistance $R_{T}$ equal to two times the characteristic impedance of the line, is:
1/3
1/2
1
1/4
A DRAM memory with words of 8 bits and 3 bit row address has:  64 capacitors  128 MOS transistors  8 capacitors
8 MOS transistors
moore law 1

show	raph reporting the number of transistors in microprocessors in the last 40 years s that:
	The number of transistors doubles every two years
	<ul><li>○ The number of transistors increases of a factor 4 every two years</li><li>○</li></ul>
	It is impossible to find a clear trend
	As consequence of the increased number of transistors, the CK speed has been reduced of a factor 2
The t	rend (during the last 40 years) of the number of transistors in microprocessors
show	s that:
show	s that:
show	
show	s that:  The number of transistors doubles every two years
show	<ul><li>○</li><li>The number of transistors doubles every two years</li><li>○</li></ul>
show	
show	The number of transistors doubles every two years  The number of transistors is increased of a factor 4 every two years
show	<ul><li>○</li><li>The number of transistors doubles every two years</li><li>○</li></ul>
show	The number of transistors doubles every two years  The number of transistors is increased of a factor 4 every two years
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NAN	The number of transistors doubles every two years  The number of transistors is increased of a factor 4 every two years  It is impossible to find a clear trend  As consequence of the increased number of transistors, the CK speed has been reduced of a factor 2

FAMOS transistors in series
FAMOS transistors in parallel
NMOS and PMOS transistoes in series
NMOS and PMOS transistors in parallel
onda quadra-condesatore
Consider a square wave generator realized with Schmitt trigger inverter; the voltage on the capacitor varies with time as:
exponential
square wave
linear
is always zero
SDRAM 1
A SDRAM memory is
a synchronous dynamic RAM

a type of static RA	М
$\circ$	
an asynchronous S	SRAM
$\circ$	
a RAM with 6 MOS	S transistor
Synchr write cy	ycle 1
Consider a synchronous write cycle; the STB signal must stay high for a minimum duration equal to:	
Th LTL	
Th+Tk	
TL	
Tk	
Tauri Tle	
Tsu+Tk	
O	
Tk+Ttxmin	
Voltage after tr	ansient
with characteristic im	supply Vdd and output resistance Ro drives a transmission line pedance $Z_{\infty}$ ; the line is terminated with a resistor Rt. After the sition, the line steady state voltage is:
○Vdd ·Rt/(Rt ○	t+Ro)



## voltage regulator

The efficiency (ie: ratio between output and input power) of a series linear volatge regulator, with input Vi and output Vo can be approximated as:

 $\bigcirc$ 

Vo/Vi

 $\bigcirc$ 

Vi/Vo

C

Vo/(Vi+Vo)

 $\bigcirc$ 

\( \sqrt{Vi/Vo} \)

## voltage step 2

Consider a L $\rightarrow$  H transition propagating in a transmission line with characteristic impedance  $Z_{\infty}$  and matched termination. The output resistance of the driver is  $R_0$ =0.5  $Z_{\infty}$  and  $V_{DD}$ =3.3V. The first incident voltage step is:

 $\bigcirc$ 

2.2 V

 $\bigcirc$ 

1.5 V

3.3 V1.65 V

Submit