Politecnico di Torino
Exam 22/01/2020 Applied Electronics (a.y. 19-20)

Surname .....
Name ..... **COMPITO "ENG"**
ID .....

Room .....

Part A – Quiz
(Report with X the correct answer in the table – Do not write in the row "Total points")

Quiz	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	
Answer a											
Answer b											
Answer c											
Answer d											
Total points											

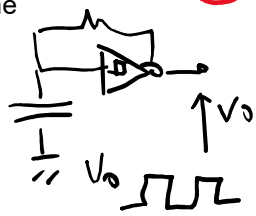
Quiz A1
Consider a 8 bit A/D conversion system. By adding two more bits, the signal to noise ratio due to quantization

a) decreases of 6 dB
b) increases of 6 dB
c) increases of 1.76 dB
d) increases of 12 dB

$SNR_Q = 6N + 1.76\ dB$
$SNR_Q = 6(N+2) + 1.76\ dB$
$6N + 1.76\ dB + 12$

Quiz A.2
Consider a square wave generator realized with Schimtt trigger inverter, one resistor and one capacitor. The voltage out of the Schimtt trigger inverter is:

a) exponential
b) square wave
c) linear
d) sine wave



Quiz A.3
Consider a synchronous write cycle; the delay, at source, between INF and STB signal is:

a) Tsu+Tk
b) Tk
c) Th
d) Tk+Ttxmin

Quiz A.4
Consider a voltage step propagating in a transmission line with open circuit termination, $R_0=Z_\infty$ and V_{DD}=2V. The first incident voltage step is:

a) 1 V
b) 2 V
c) 0.5 V
d) 1.5 V

$V_B^+(\infty) = \frac{Z_0}{R_0+Z_0} V_{DD} = V_{DD}/2$

Quiz A.5
Series voltage regulators: the efficiency is:

a) 1
b) >1
c) <1
d) 100

Quiz A.6
How many voltage comparators are required in a 4 bit FLASH ADC?

a) 1
b) 15
c) 4
d) 8

$\Rightarrow$ comparators: $2^N - 1 = 2^4 - 1$

Quiz A.7
If we reduce of a factor of 2 the voltage supply V_{DD} of a CMOS logic gate, then the dynamic power consumption:

A) increases of factor 2
b) reduces of factor 1/2
c) increases of factor 4
d) reduces of factor 1/4

$P_{DD} = \frac{V_{DD}^2 C_L f}{2}$

Quiz A.8
A flash memory cell consists in:

a) one FAMOS
b) one FAMOS and one capacitor Cs
c) 1 MOS and one capacitor Cs
d) one NMOS, one PMOS and two capacitors

Quiz A.9
A FPGA logic block contains:

a) Look-Up Tables and several AND/OR gates
b) several AND/OR gates and several flip-flops
c) Look-up Table and several flip-flops
d) programmable switch only

Quiz A.10
The output of a CAM memory is:

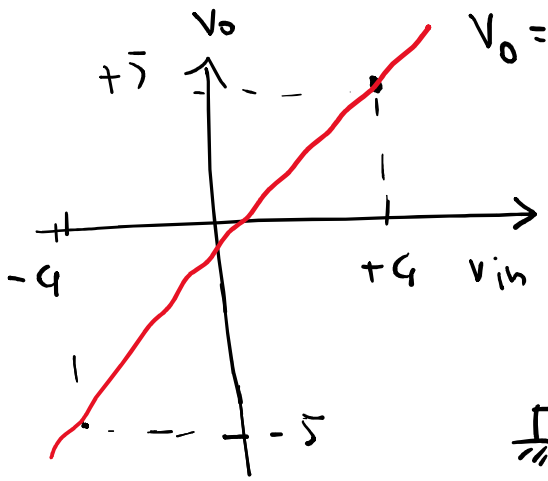
a) a control signal
b) a data
c) a command
d) an address

Parte B – Problem B.1

Consider 4 analog sinusoidal signals with voltage in the range between -4V and +4V. The signals are converted with an A/D conversion system using only one S/H and one ADC. The S/H acquisition time is 800ns. The ADC is a 8 bit successive approximation converter with clock frequency of 60 MHz and input dynamics from -5V to +5V. The signals are sampled with over-sampling factor K=3.5.

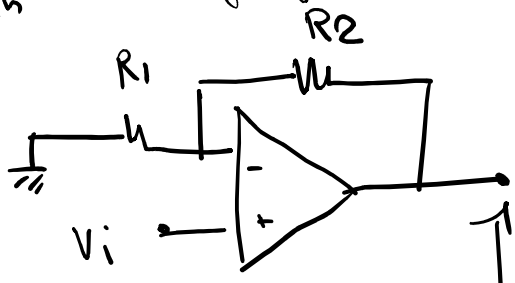
a) Plot the block diagram of the A/D conversion system. Indicate if the conditioning amplifier is required; trace the characteristic (ie: Vout versus Vin) of the conditioning amplifier and plot a circuit of this conditioning amplifier.

Block diagram: see slide of lecture



$V_o = A_V V_{in}$ $A_V = \frac{5}{4}$ $V_{OFF} = 0$

Non inverting voltage amplifier



$V_o = \left(1 + \frac{R_2}{R_1}\right)$

b) Calculate the maximum possible input frequency of each input signal and calculate the signal to noise ratio due to quantization.

$T_{S\,min} = T_c + T_{S/H} + T_{mux} = N T_{CK} + T_{S/H} =$ @S/H

$800\,ns + 8/60\,MHz = 933\,ns$

$f_{S/H\,max} \leq 1\,MHz$

$f_{Signal\,max} = 2B_{max} \cdot K = \frac{1\,MHz}{4}$

$B_{max} = 35.7\,kHz$

Part B – Problem B.2

One driver with voltage supply equal to 3,3 V (Voh=3.3V, Vol=0V) is used for driving a transmission line with Z_∞ = 60 Ω, propagation speed U = 0,6 C, length 25 cm and termination R_T=100 Ω. The receivers are CMOS circuits with Vil = 1V, Vih = 2,2 V. Consider L-H transition and answer to the following questions:

a) Calculate the value of the driver output resistance R0 to have RWS on the first reflected wave.

We must avoid IWS and satisfy RWS:

→ no IWS ⇒ $V_B(0) < V_{IH} \Rightarrow \frac{Z_0}{Z_0+R_0} \cdot V_{DD} < V_{IH}$ ⇒ $R_0 > 30\,\Omega$

$\Gamma_T = \frac{R_T - Z_0}{R_T + Z_0} = 0.25$

→ Switch on RWS ⇒

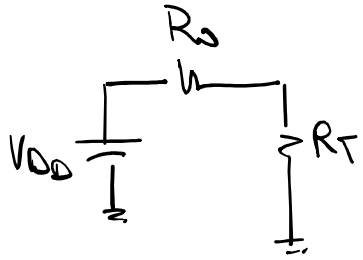
$V_c(t_p) = V_B(0)[1+\Gamma_T] > V_{IH}$

$V_2(>t_p) = V_B(0)[1+\Gamma_T] > V_{IH}$

$1.25\,V_B(0) > V_{IH}$ ⇒ $R_0 < 52.5\,\Omega$

b) Assuming now the far-end is open circuit, calculate:
- the steady state far-end voltage when the transient is concluded
- the maximum and minimum transmission time and the skew for a receiver connected to the far-end.

$V_c(t \to \infty) \Rightarrow$

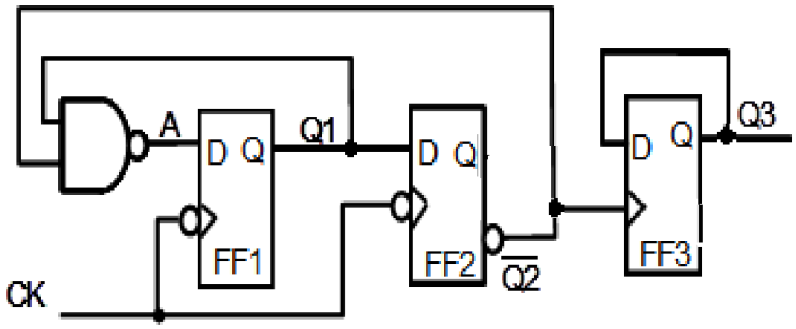


$V_c = \frac{R_T}{R_0 + R_T} V_{DD} = 2V$ with $R_0 = 40\,\Omega$

$T_{Txmin} = t_p = T_{Txmax}$ because $V_c(t_p) = V_{DD} \cdot 0.6 \cdot 2 > V_{IH}$

$t_p = \frac{L}{U} = \frac{25\,cm}{0.6\,c} = 0.13 \cdot 10^{-8}\,s = 1.3\,ns$

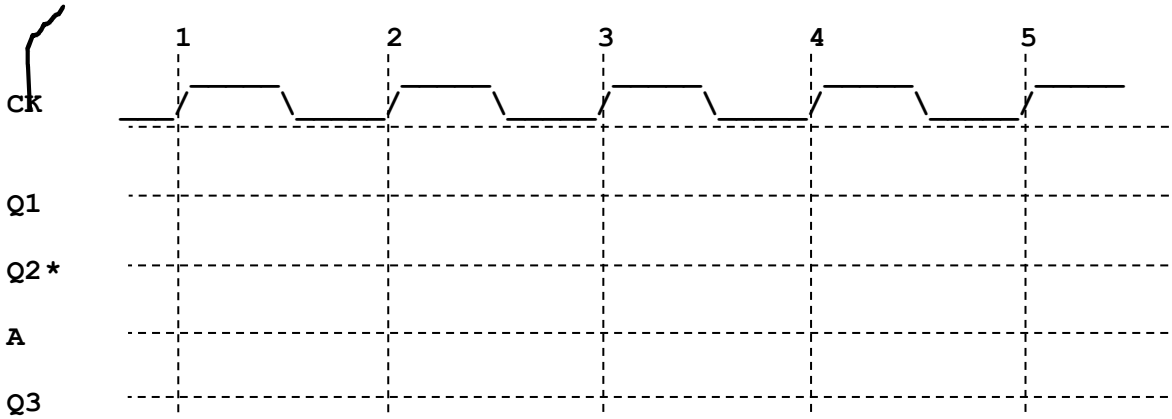
Part B – Problem B.3



Consider the sequential circuit shown in the figure. All outputs Q are initially reset to zero.

a) Plot the timing diagrams of the outputs Q1, Q2*, A and Q3 for 5 CK cycles; **assuming the following delays:**

FF1, FF2 and FF3: $T_{ck=>Q}$ =2 ns; Th=1ns; Tsu=3ns
NAND: Tp=5ns per H-L e 4ns per L-H



b) Calculate the maximum CK frequency when the components have the dynamic parameters of point (1)

$T_{CK\,min} = T_{CK\to Q}^{FF_2} + T_{pd}^{NAND} + T_{su}^{FF_1} = 10\,ns$

$f_{CK\,max} = 100\,MHz$

c) If Tck=10ns specify if any FF will enter in metastable state.

Enters in metastable state

Part-B –Problem B.4

A DRAM memory has:
- 12 bit address,4 bits are for column address and 8 bits are for row address.
- 8 bit words
- pass transistors with Cd=0.5fF

The

a) Calculate the number of Word lines

$2^8 = 256$

b) Calculate the total number of memory cells

$2^8 \times 2^4 \times 8 = 32768$

32 kbit

c) Calculate the capacitance of the bit line C_{BL}

$C_{BL} = \#rows \cdot C_d = 128\,fF$

how much is femto?