POLITECNICO DI TORINO

Applied electronics

Exam of 31 August 2020

This is an example of exam. Solutions are reported in red in the orange rectangle.

Exam consistes in 10 Quiz (max 10 points), 4 open problems (5 point each), 3 optinal questions on lab part (1 point each)

Score is: (quiz points + problem points)*0.9+optinal questions points . Max mark is 30/30

Domanda 1

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a square wave generator with Schmitt trigger inverter, the frequency of the square wave can be increased by:

- (a) reducing the resistance R ✓
- (b) increasing the resistance R
- (c) increasing the capacitance C
- (d) doubling the resistance R

Risposta corretta.

La risposta corretta è: reducing the resistance R

Domanda 2

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider an asynchronous write cycle; when does the STB signal go high after the INF?

- (a) STB goes high after tk ✓
- (b) STB goes high after tk+th
- (c) STB goes high after tk+tsu
- (d) STB goes high after tk+th+tsu

Risposta corretta.

La risposta corretta è: STB goes high after tk

Domanda 3

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a D-FF. Select the correct sentece:

- (a) During the set-up time D must not change ✓
- (b) D must be always 1 during the set-up time
- (c) D must be always 0 during the set-up time
- (d) During the set-up time D must change no more than 2 times

Risposta corretta.

La risposta corretta è: During the set-up time D must not change

Domanda 4

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The efficiency (ie: ratio between output and input power) of a series linear volatge regulator, with input Vi and output Vo can be approximated as:

- (a) Vo/Vi ✓
- (b) Vi/Vo
- (c) Vo/(Vi+Vo)
- (d) $\sqrt{Vi/Vo}$

Risposta corretta.

La risposta corretta è: Vo/Vi

Domanda 5

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

A driver with voltage supply Vdd and output resistance Ro drives a transmission line with characteristic impedance Z_∞; the line is terminated with a resistor Rt. After the transient of L->H transition, the line steady state voltage is:

- (a) Vdd ·Rt/(Rt+Ro) ✓
- (b) Vdd
- (c) Vdd $Z_\infty/(Z_\infty+Ro)$
- (d) Vdd $Z_\infty/(Rt+Z_\infty)$

Risposta corretta.

La risposta corretta è: Vdd ·Rt/(Rt+Ro)

Domanda 6

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

A FPGA consists in:

- (a) LUT, MUX and registers ✓
- (b) Arrays of OR gates
- (c) Arrays of AND gates
- (d) Arrays of SRAM cells

Risposta corretta.

La risposta corretta è: LUT, MUX and registers

Domanda 7

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

A data acquisistion system has a total SNR of 49.76dB. Calculate the ENOB.

- (a) ENOB=8 ✓
- (b) ENOB=10
- (c) ENOB<7
- (d) ENOB>10

Risposta corretta.

La risposta corretta è: ENOB=8

Domanda 8

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The conversion time of a pipeline ADC with N bits:

- (a) is not determined by the number of bits N ✓
- (b) is proportional to N
- (c) is proportional to 2^N
- (d) is proportionalto 1/N

Risposta corretta.

La risposta corretta è: is not determined by the number of bits N

Domanda 9

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

AA NAND Flash memory consists in:

- (a) FAMOS transistors in series ✓
- (b) FAMOS transistors in parallel
- (c) NMOS and PMOS transistoes in series
- (d) NMOS and PMOS transistors in parallel

Risposta corretta.

La risposta corretta è: FAMOS transistors in series

Domanda 10

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

A DRAM memory with words of 8 bits and 3 bit row address has:

- (a) 64 capacitors ✓
- (b) 128 MOS transistors
- (c) 8 capacitors
- (d) 8 MOS transistors

Risposta corretta.

La risposta corretta è: 64 capacitors

Domanda 11

Completo

We have 6 analog input channels with voltage in the range between -2V and +2V. The maximum bandwith of the channels is 30kHz.

The acquisition system uses one S/H and one SAR ADC with input dynamic range [0, +10 V]. The channels are oversampled with oversampling factor of 3.

Request 1:

List the various blocks of the acquisition system and define the role of each block. Indicate the relation V_{out} versus V_{in} of the conditioning amplifier .

Request 2:

Calculate the sampling frequency of the S/H

Request 3:

Calculate the number of bits to convert the signals with precision of 0.5%.

Request 4:

Assuming the S/H has acquisition time of 250ns and the MUX intruduces a delay of 50ns , calculate the CK frequency of the SAR

Request 1:

Conditioning amplifier: Av=10/4, offset +5V. ==> Vo=Av*Vi+offset

Request 2:

Sampling frequency of S/H is: fs=B*2*3*6=30kHz*36=1080kHz ==> Ts=926ns

Request 3:

quantization error is S/(2^N) ==> precision 1/(2^N)<0.5/100 => N>=8, we select N=8

Request 4:

Ts=Tc+Tacq+Tmux<926ns => Tc<(926-50-250)ns=626ns Tc=N*Tck, with N=8 we have Tck=78.25 fck=12.8MHz

Domanda 12

Completo

A track of 30cm on a PCB backplane has characteristic impedance $Z_{¥} = 90\Omega$ (with no load), and wave propagation speed u = 0,6 c. We need to connect to the track N=10 equally spaced receivers. Each device has an input capacitance of 1pF. The line is driven on one side and closed with a matched termination on the other side.

The driver and receivers have the following electrical parameters:

Voh = 4.1 V, Vol = 0,4 V, Vih = 2,5 V, Vil = 1,0 V; Vdd=4.5V.

Request 1)

Calculate the capacitance per unit length of the line without any connected device.

Request 2)

Calculate the characteristic impedance of the line with the connected

receivers

Request 3)

Calculate the output resistance of the driver to drive the line in IWS mode and NM=0.5V. Include in the calculation the effect of the capacitive load.

Request 1:

the capacitance per unit of length is *C=1/(Z∞*u) ==> C=0.62pF/cm*

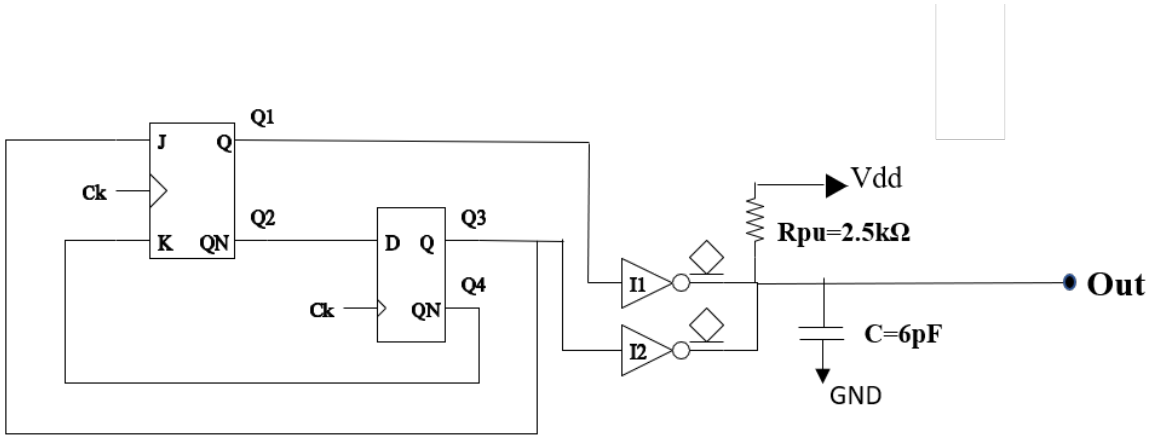
Request 2:

*Z∞'=Z /sqrt(1+NCi/L*C)=72.6 ohm*

Request 3:

Vb(0)=*Z∞'/(Z '+Ro)*Vdd>=Vih+NM=3V ==> Ro<=36.3 ohm*

Consider the sequential circuit shown in the figure. All outputs Q are initially reset to zero.



Request 1:

The inverters I1 and I2 have output resistance R_{OL}=60 Ω. Calculate the maximum and minimum delay for L to H ($T_{LH,max}$ and $T_{LH,min}$) and for H to L transition ($T_{HL,max}$ and $T_{HL,min}$) of the output voltage (Vout) on the capacitor C.

Request 2:

Assuming the following dynamic parameters for the FFs and the delays calculated in Request 1

FF_D: T*ck->Q* =5 ns, Tsu = 4ns;

FF JK : T*ck->Q* = 7ns, Tsu = 6ns;

Answer the following questions assuming the CK period is 60ns:

- which are the inital states of Q1, Q2 and Q4?

- which is the state of the voltage on the capacitor (Vout) if Q1=1 and Q3=1

- how many CK rising edges are necessary to switch Q3 to high state?

- calculate the delay between a transition L->H of Q2 and the correspoding variation of the state of the voltage on the capacitor

Request 2:

Calculate the maximum CK frequency

Request 1

time constant for L to H transition tau_LH=Rpu*C=150ns ==> propagation delay

T_LHmax=T_LHmin=0.69*tau_LH=103.5ns

time constant for H to L transition:

- only one inverter is connected to GND => tau_HLmax=Rol*C ==> T_HLmax=0.69*tau_HLmax=2.4 ns

- both inverted are connected to GND ==> Rol are in parallel ==> tau_HLmin=Rol/2*C T_HLmin=0.69*tau_HLmin=1.2ns

Request 2

a) Q1=0 Q2=1 Q4=1

b) voltage on the capacitor is HIGH state

c) first rising edge of the CK

d) after the CK rising edge Q2 goes high and Q1 and Q3 goes low. The delay between the transition L-H of Q2 respect to the CK edge is 7 ns, whereas it is 5ns for the transition H-L of Q1 and Q3. As consequence of the transition H-L of Q1 and Q3 the voltage on the capacitor goes high with a delay T_LH=103.5 ns. In conclusion: the delay of the variation of the output respect to the transition L-H of Q2 is: 103.5ns-(7-5)ns=101.5ns

Request 3

For FF-JK: Tck,min=Tck,Q D+TsuJK=5ns+6ns=11 ns

For FF-D Tck,min=Tck,Q JK+Tsu,D=7ns+4ns=11 ns

fck,max=1/11ns=90.9MHz

Domanda 14

Consider a DRAM memory with 8 bit address; all bits are used for row decoder. Each word is 8 bit. The pass transistors have drain parassitic capacitance Cd=0,4fF and threshold voltage Vth=0,2V; voltage supply is Vdd=2V. Answer to the following questions:

Request 1:

Calculate

- the number of bit lines

- the number of pass transistors connected to one bit line

- the total number of pass transistors of the memory.

Request 2:

Calculate the minimum value of the storage capacitor Cs, if the sense amplifier can sense a minimum voltage level of 30mV.

Request 1:

- the number of bit lines = number of word =8

- the number of pass transistors connected to one bit line =number of rows=2^8=256

- the total number of pass transistors of the memory = 256*8=2048

Request 2:

ΔV=(Vdd-Vth-Vdd/2)*Cs/(Cs+Cbl)>=30mV Cbl=2^8*0.4fF=102.4fF

Cs>=4fF

Domanda 15

Punteggio max.: 1,0

Considering a DAC circuit analogous to the one implemented with the LTspice software in the virtual LAB, which type of error do you expect to observe on the converted Analog signal if an error affect the MSB branch of the DAC weighted network?

Domanda 16

Punteggio max.: 1,0

- Logic gates and simple sequential logic circuits:

How can you visualise using the Waveform Viewer in the LTspice software the trascharacteristic of a CMOS inverter? Which information can you extract from this plot ?

Domanda 17

Punteggio max.: 1,0

How can you realise and simulate with the LTspice software a Time Domain Reflectometer able to measure the length of a coaxial cable behaving as a transmission line?