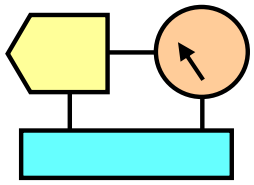
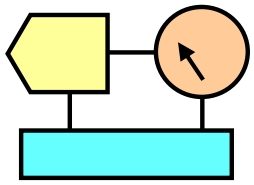


APPLIED ELECTONICS

Part D:

Class exercises 3 with solutions on:

- **Analog-Digital and Digital-Analog conversion systems proprieties**



Problem 1 – Assignment
A/D conversion

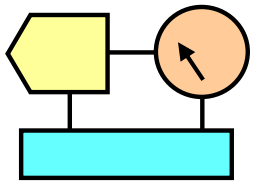
a) Plot the block diagram of a system for A/D conversion of signals from 4 channels. The input signals have dynamics $[1\ \mathrm{V} - 2\ \mathrm{V}]$ and bandwidth $0 - 15\ \mathrm{kHz}$. The system must use one A/D converter (dynamics $[0 - 5\ \mathrm{V}]$ and $\mathrm{T_c} = 500\ \mathrm{ns}$) and one S/H with acquisition time $\mathrm{T_{acq}} = 700\ \mathrm{ns}$.

b) Determine the maximum and minimum sampling frequency.

c) Draw the circuit of the conditioning amplifier (if it is necessary) and calculate the value of the resistors of the circuit.

d) If the input signals are sine waves with dynamics $[1\ \mathrm{V} - 2\ \mathrm{V}]$, calculate the minimum number of bit to guarantee $\mathrm{SNR_q} > 35\ \mathrm{dB}$.

e) If the input sine wave has amplitude $\mathrm{V_P}$ variable in the range between $0.5\ \mathrm{V}$ and $2.5\ \mathrm{V}$ (i.e: $\mathrm{V_{Pmin}} = 0.5\ \mathrm{V}$ and $\mathrm{V_{Pmax}} = 2.5\ \mathrm{V}$) and average value equal to $1.5\ \mathrm{V}$, calculate the minimum number of bits of the A/D to guarantee $\mathrm{SNR_q} > 35\ \mathrm{dB}$.



Problem 1 - Assignment

f) Specify the anti-aliasing filter characteristics to guarantee a signal to noise ratio due to aliasing (SNRa) of minimum $60\mathrm{dB}$.

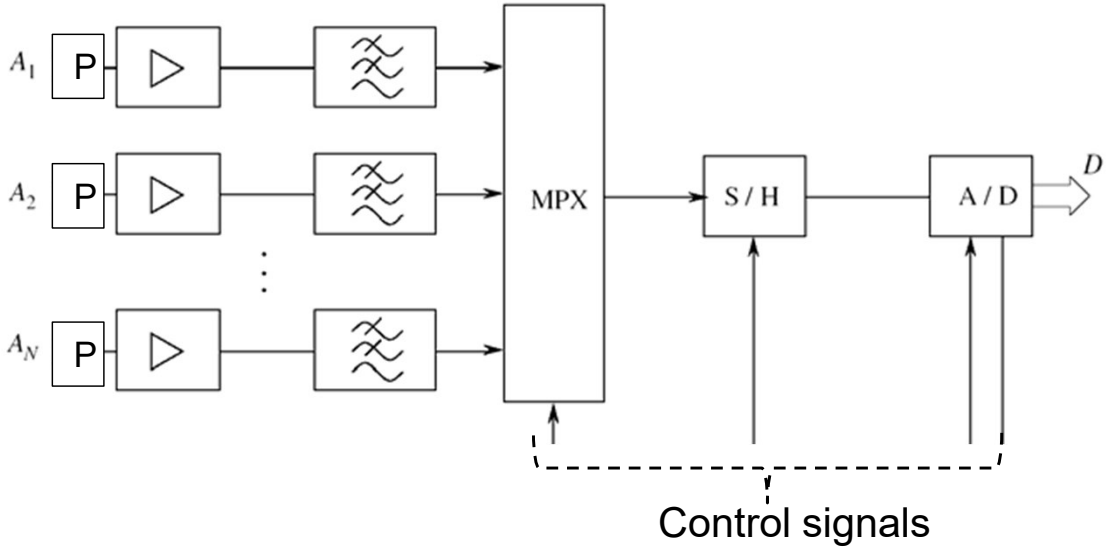
g) Calculate the maximum aperture jitter ($\mathrm{T_{jamax}}$) of the SH to guarantee an error due to jitter of less than 0.1%

h) Calculate the number of bits to have quantization error equal to aliasing error $\mathrm{SNRa} = 60\ \mathrm{dB}$.

i) Calculate from point (h) the total $\mathrm{SNR_t}$ and the ENOB.

Problem 1a - Solution

Block diagram



a) The blocks of the data acquisition system are in the order:

1. Protection circuit to limit the Analog signal voltage in the "safe" input range
2. Conditioning amplifier to adapt the input dynamics to the ADC converter dynamics and thus to reduce the SNR associate to the quantization error
3. Antialiasing filter to limit the Analog signal bandwidth and thus to reduce the aliasing error
4. Multiplexing to use the same S/H and ADC blocks for several channels
5. S/H unit to sample at discrete instant of time the Analog signal
6. ADC converter to convert the discrete Analog values in Digital values

Problem 1b - Solution

b) The **minimum sampling frequency** ($f_{s,min}$) is determined by the Nyquist rule:

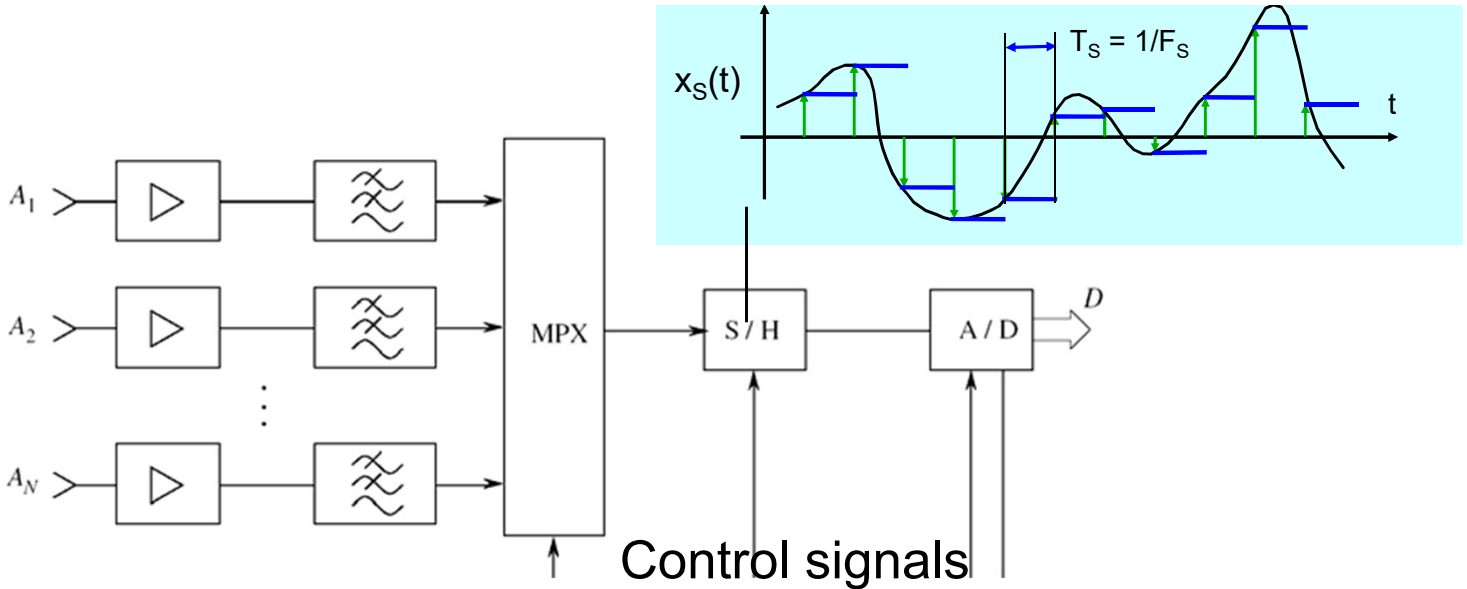
$$f_{s,min\_1channel} = 2 \times 15\ kHz = 30\ KHz$$

$$f_{s,min\_4channel} = 4 \times 2 \times 15\ kHz = 4 \times 30\ kHz = 120\ kHz$$

The **maximum sampling frequency** ($f_{s,max}$) is determined by the inverse of the minimum sampling time $T_{s,min}$:

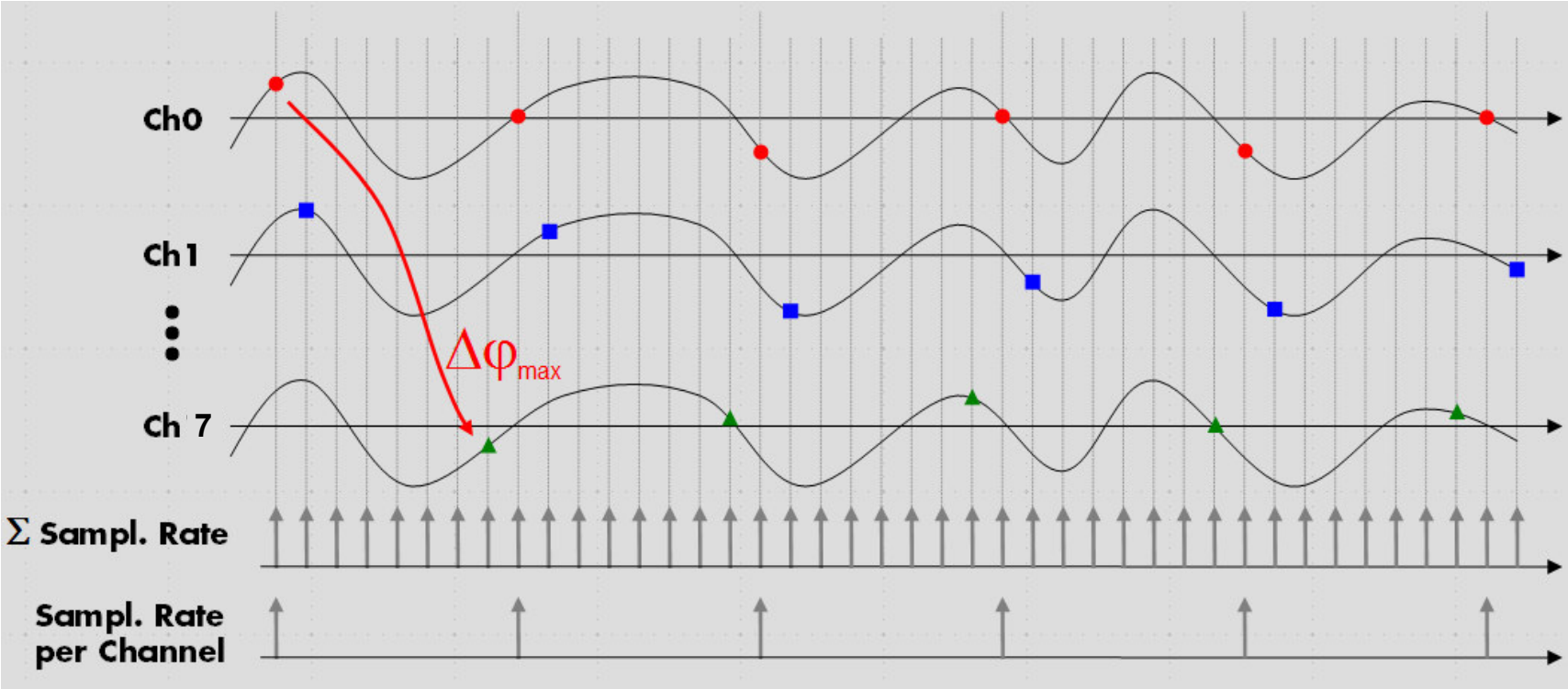
$$T_{s,min} = T_c + T_{acq} = 500\ ns + 700\ ns = 1200\ ns \implies f_{s,max} = 833\ kHz$$

Block diagram



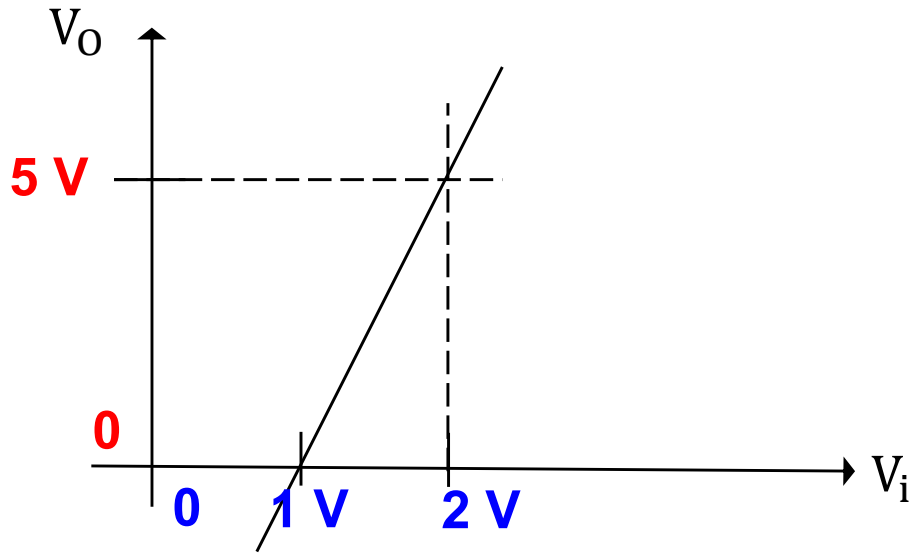
Problem 1
Theoretical remind

In presence of Multiplexing the effective sampling rate of the single channel is given by the A/D converter sampling rate divided by the number of channels



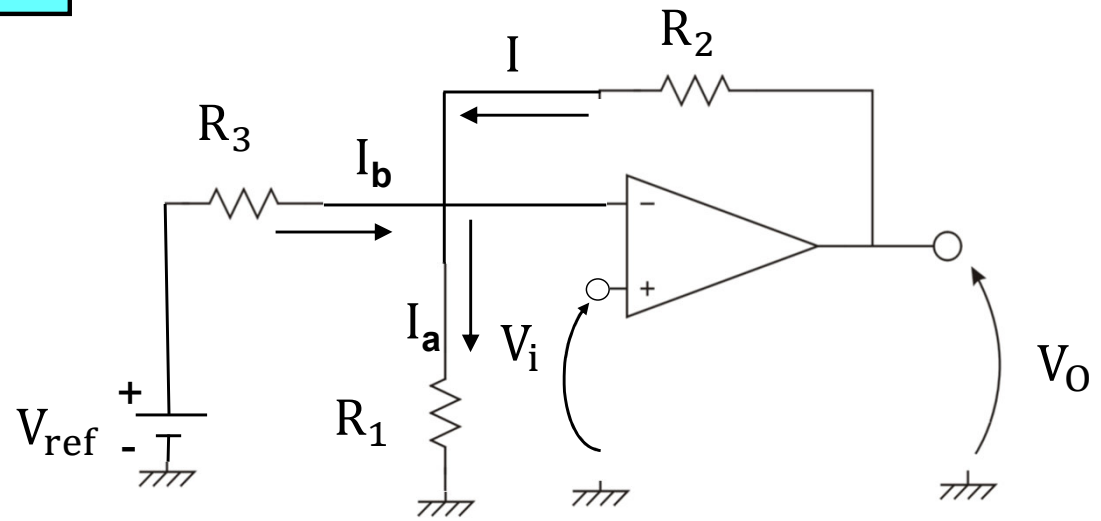
Problem 1c - Solution

c) The **conditioning amplifier** must be used because the signal dynamics is $[1\ \mathrm{V} - 2\ \mathrm{V}]$ while the A/D dynamics is $[0\ -5\ \mathrm{V}]$. So the circuit of the conditioning amplifier must be associated to the following transfer function:



The input signal has to be multiplied by $A_V = 5$ and translated of $V_{off} = -5\ \mathrm{V}$. This can be realized with the following circuit:

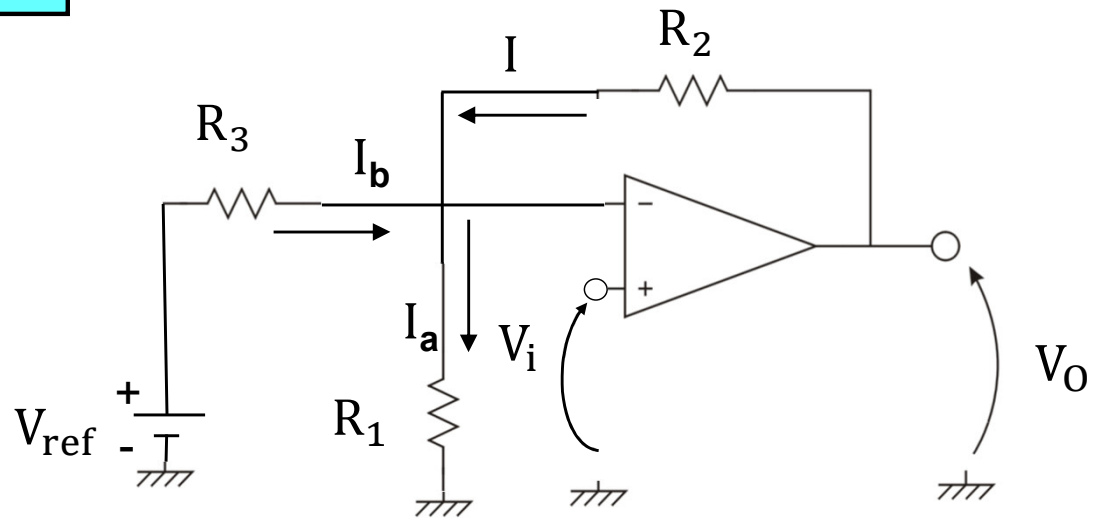
Problem 1 - Solution



In fact for a closed loop Operational Amplifier (OA) the input/output voltage relation is:

from which:

Problem 1 - Solution



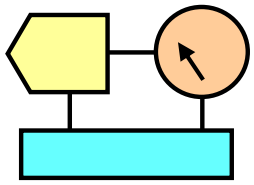
In fact for a closed loop Operational Amplifier (OA) the input/output voltage relation is:

$$V_O = V_i + R_2 I = V_i + R_2(I_a - I_b) = V_i + R_2\left(\frac{V_i - V_{ref}}{R_3} + \frac{V_i}{R_1}\right)$$

from which:

$$V_O = \left(1 + \frac{R_2}{R_1 \parallel R_3}\right) V_i - \frac{R_2}{R_3} V_{ref}$$

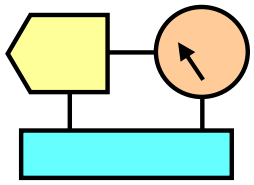
If we now choose $V_{ref} = 5\ V, R_2 = R_3 = 10\ k\Omega, R_1 = \frac{R_3}{3} = 3.3\ k\Omega$ it is easy to verify that $A_V = \left(1 + \frac{R_2}{R_1 \parallel R_3}\right) = 5$ and $V_{off} = -\frac{R_2}{R_3} V_{ref} = -5\ V$



Problem 1d,e - Solution

d) In presence of the amplifier the input signal is amplified in order to cover the whole A/D dynamic range S. Then the signal to noise ratio of the quantification error is for a sine wave of $\mathrm{Vpp} = S$:

$$\mathrm{SNR_q} = 10\log_{10}\left(\frac{S^2/8}{A_D^2/12}\right)$$



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$$\mathrm{SNR_q} = 10\log_{10}\left(\frac{S^2/8}{A_D^2/12}\right) = 10\log_{10}\left[\frac{S^2}{A_D^2}\left(\frac{12}{8}\right)\right] = 10\log_{10}\left(2^{2N}\right) + 10\log_{10}(1.5)$$
$$= (6N + 1.76)\mathrm{dB}$$

From the request $\mathrm{SNR_q} > 35\ \mathrm{dB}$ thus follows:

$$N > \frac{35-1.76}{6} = 5.54 \Longrightarrow N_{min} = 6$$

e) In case the amplitude is variable between $V_{p,\,min} = \frac{Vpp,min}{2} = 0.5\ \mathrm{V}$ and $2.5\ V$ and we consider the worst case associated with the minimum dynamics:

Problem 1d,e - Solution

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$$\mathrm{SNR_q} = 10\log_{10}\left(\frac{1}{A_D^2/12}\frac{Vpp,_{min}^2}{8}\right) = 10\log_{10}\left(\frac{S^2/8}{A_D^2/12}\frac{4V_{Pmin}^2}{S^2}\right) = (6N + 1.76)\mathrm{dB}-$$
$$-\ 20\log_{10}\left(\frac{S}{2V_{Pmin}}\right) = (6N + 1.76)\mathrm{dB} - 14\mathrm{dB}$$

Problem 1e,h - Solution

From the request $\mathrm{SNR_q} > 35\ \mathrm{dB}$ thus follows:

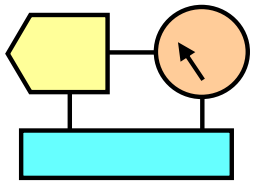
$$\mathrm{N} > \frac{35-1.76+14}{6} = 7.87 \Longrightarrow \mathrm{N_{min}} = 8$$

h) In the hypothesis that $\mathrm{SNR_q} = \mathrm{SNR_a} = 60\ \mathrm{dB}$ i.e. that the error power due to aliasing $\mathrm{P_a}$ is equal to the power error due to quantization $\mathrm{P_q}$ and a sine wave signal covering the whole dynamic range:

$$\mathrm{SNR_q} = (6\mathrm{N} + 1.76)\mathrm{dB} = 60\ \mathrm{dB}$$

From which:

$$\mathrm{N} > \frac{60-1.76}{6} = 9.7 \Longrightarrow \mathrm{N_{min}} = 10$$



Problem 1i - Solution

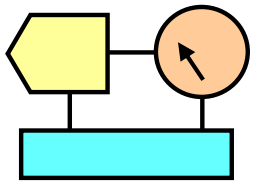
i) Assuming that the only relevant sources of errors are those related to aliasing and quantization:

$$\mathrm{SNR_t} = 10\log_{10}\left(\frac{P_s}{P_a + P_q}\right) = -10\log_{10}\left(\frac{2\mathrm{P_a}}{\mathrm{P_s}}\right) = 10\log_{10}\left(\frac{\mathrm{P_s}}{\mathrm{P_a}}\right) - 3\ \mathrm{dB} = 57\ \mathrm{dB}$$

From which:

$$\mathrm{ENOB} = \frac{\mathrm{SNR_t} - 1.76\ \mathrm{dB}}{6} = 9.21\ (\cong 10)$$

Equivalent number of bits



Problem 2 – Assignment
D/A conversion

Consider a N bit weighted resistor D/A converter. The resistors of the branches have precision equal to ε.

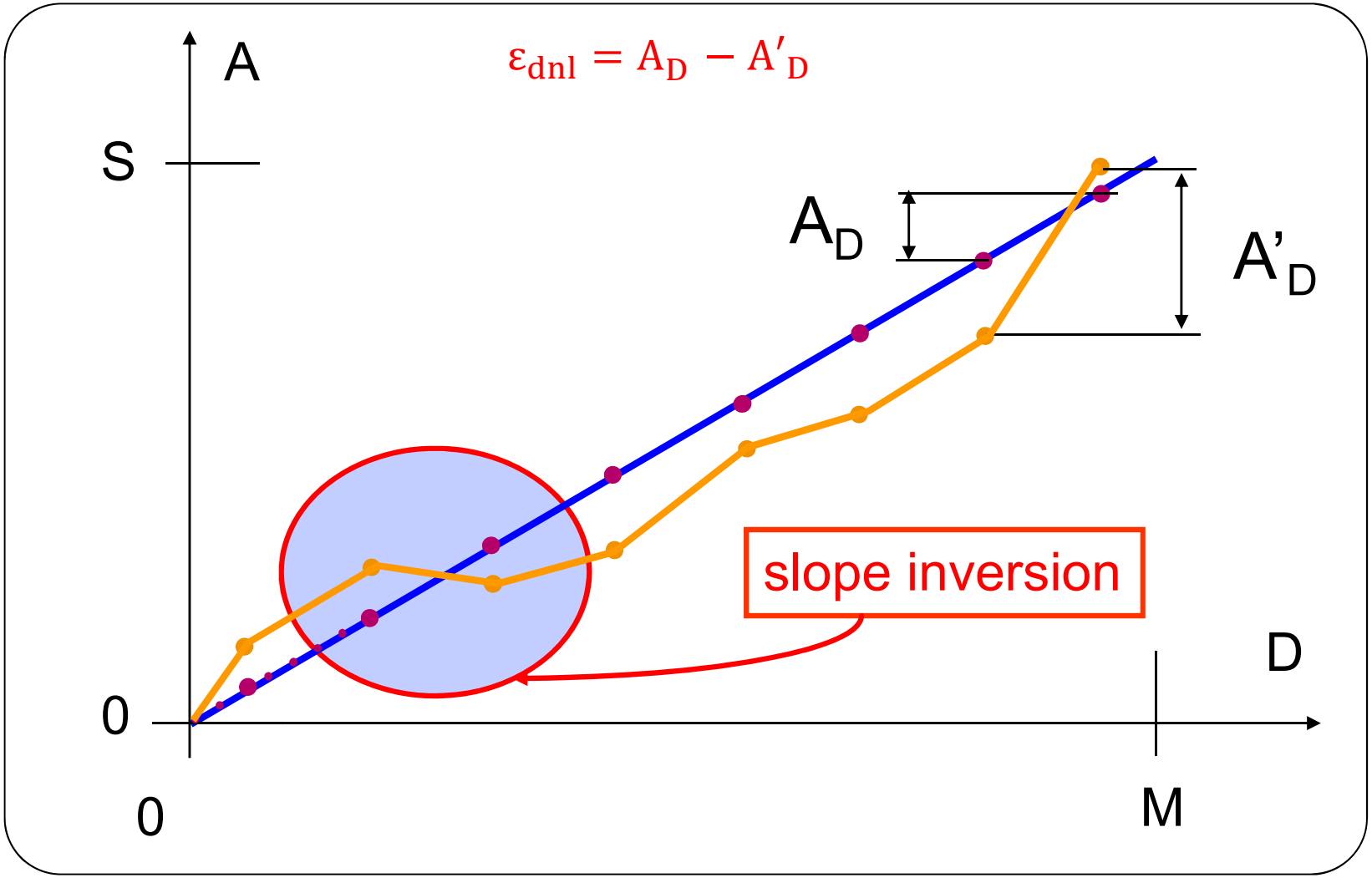
a) Calculate the error on the output voltage due to the MSB branch and the LSB branch.

b) Calculate the precision ε to make the error lower than $\frac{1}{2}$ LSB.

c) Calculate the precision in the case of 4 bits D/A and in the case of 8 bits D/A.

Problem 2
Theoretical remind

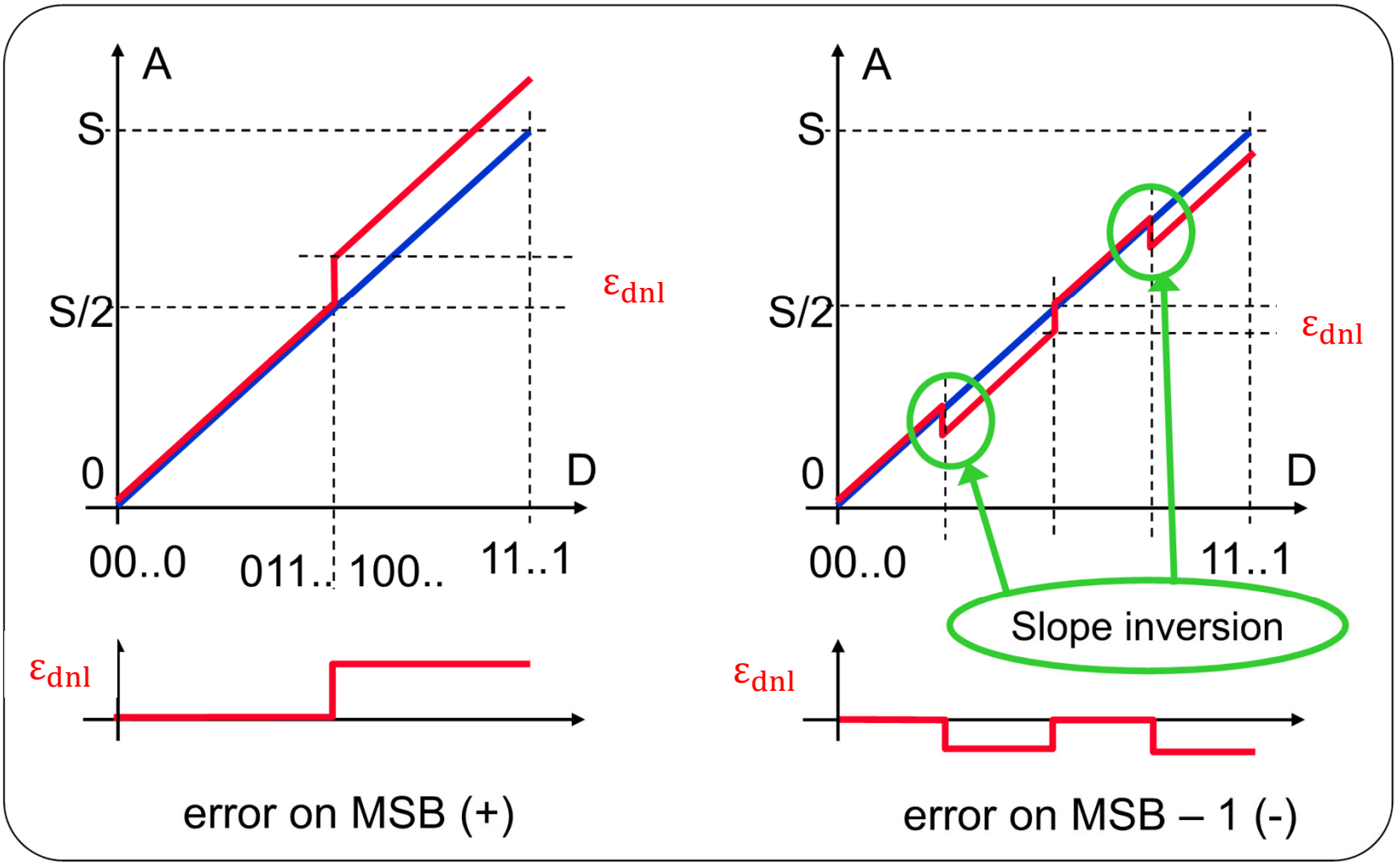
Differential nonlinearity errors

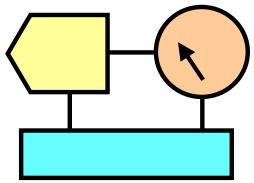


Problem 2
Theoretical remind

Differential nonlinearity errors

Errors in weighted network: MSB, MSB-1. Examples





Problem 2
Theoretical remind

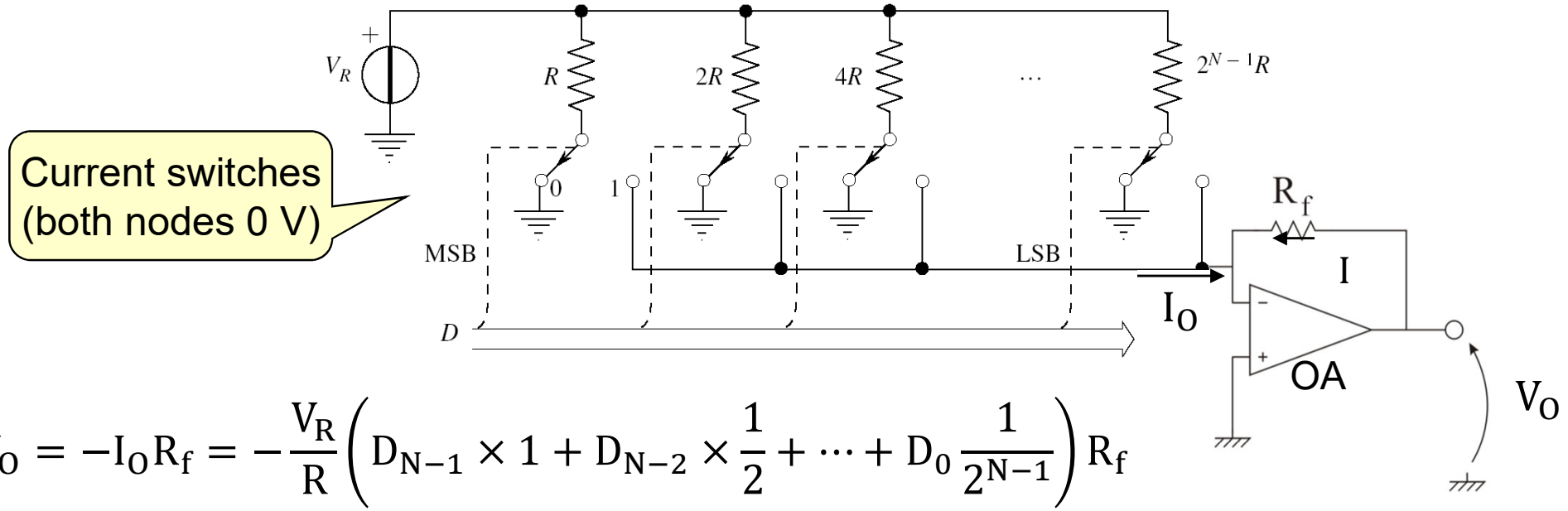
Differential nonlinearity errors

Errors in weighted converters. Examples

- Error on MSB branch
  - actual contribution higher than ideal
  - raised upper half of characteristic
  - branch error 10%: --> output error 5%
- Error on MSB - 1 branch
  - actual contribution lower than ideal
  - lowered even quarters (2,4) of characteristic
  - branch error 10%: --> output error 2.5%
- Error on MSB - 2 branch
  - branch error 10%: --> output error 1.25%
  - ...

Problem 2a,b - Solution

a), b) In case of a **D/A weighted network converter** as the one sketched here:



$$V_O = -I_O R_f = -\frac{V_R}{R}\left(D_{N-1} \times 1 + D_{N-2} \times \frac{1}{2} + \cdots + D_0 \frac{1}{2^{N-1}}\right) R_f$$

Focusing on the MSB branch: $R(1-\varepsilon) < R_{MSB} < R(1+\varepsilon)$.

Then:

$$V_{OMSB} + \Delta V_{MSB} = -\frac{V_R}{R(1 \pm \varepsilon)} R_f = -\frac{V_R}{R} R_f \left(1 \mp \varepsilon + O(\varepsilon^2)\right) \cong -\frac{V_R}{R} R_f (1 \mp \varepsilon)$$

From which: $|\Delta V_{MSB}| = \frac{V_R}{R} R_f(\varepsilon) \cong \frac{S}{2}\varepsilon$. Moreover since 1LSB = $\frac{S}{2^N}$, in order for the condition:

Problem 2a,b - Solution

$$|\Delta V_{MSB}| \cong \frac{S}{2}\,\varepsilon < \frac{1}{2}\mathrm{LSB} = \frac{S}{2\times 2^{N}}$$

to be fulfilled we must require that the uncertainty on the value of R satisfy the relation:

$$\varepsilon < \frac{1}{2^{N}} \begin{cases} 4\ bits \Longrightarrow 0.06 \\ 8\ bits \Longrightarrow 0.004 \end{cases}$$

Focusing on the LSB branch: $2^{N-1}R(1-\varepsilon) < R_{LSB} < 2^{N-1}R(1+\varepsilon)$.

From which:

$$V_{OLSB} + \Delta V_{LSB} = -\frac{V_R}{2^{N-1}R(1\pm\varepsilon)}R_f = -\frac{V_R}{2^{N-1}R}R_f\left(1\mp\varepsilon+O(\varepsilon^2)\right)$$

$$\cong -\frac{V_R}{2^{N-1}R}R_f(1\mp\varepsilon)$$

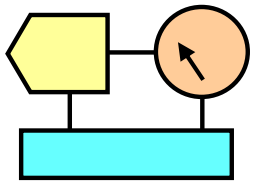
Hence: $|\Delta V_{LSB}| = \frac{V_R}{2^{N-1}R}R_f(\varepsilon) \cong \frac{S}{2^{N}}\varepsilon$. Finally the condition:

$$|\Delta V_{LSB}| \cong \frac{S}{2^{N}}\varepsilon < \frac{1}{2}\mathrm{LSB} = \frac{S}{2\times 2^{N}}$$

is satisfied when:

$$\varepsilon < 0.5$$

It does not depend on N.



Problem 2c - Solution

c) Since the largest error is the one associated with the MSB branch if we want a system with a precision higher than $\frac{1}{2}\mathrm{LSB}$ we must require:

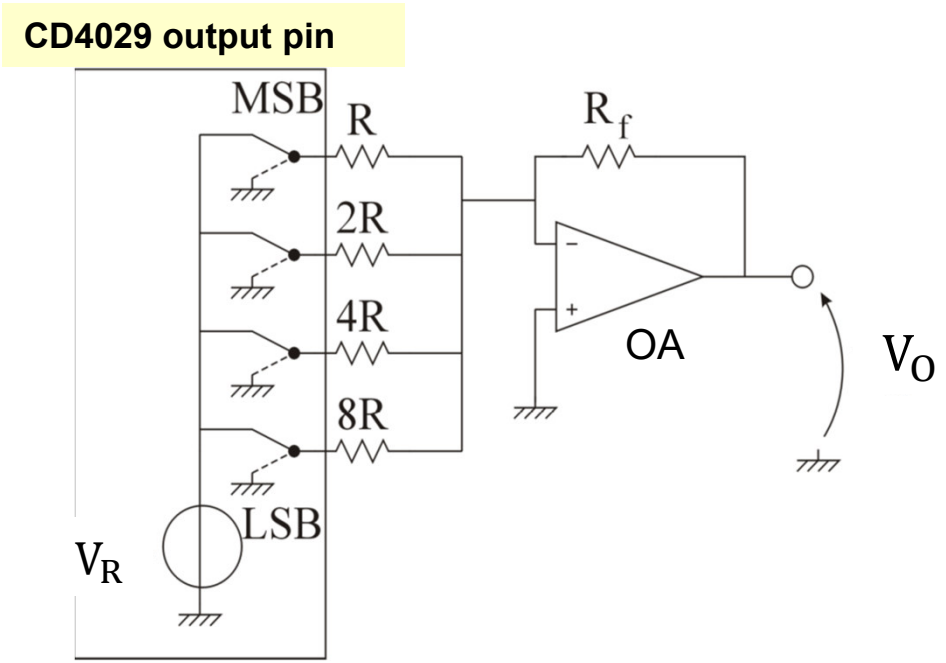
$$\varepsilon < \frac{1}{2^{\mathrm{N}}} \begin{cases} 4\ bits \Longrightarrow \varepsilon < 0.06 \\ 8\ bits \Longrightarrow \varepsilon < 0.004 \end{cases}$$

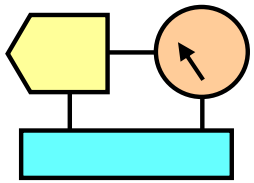
Problem 3 – Assignment
D/A conversion
(NOTE: useful for Lab experiments)

Given the circuit shown in the figure where the CD4029 is a counter with $V_{CC} = 5\ V$ and OA is an operational amplifier with $V_{CC} = \pm 10\ V$, calculate the resistors values to satisfy the following conditions:

a) Full scale output voltage $V_{fs} = -5V$

b) Error in the MSB output voltage due to the "equivalent resistance of the switches" less than ½ LSB.





Problem 3a,b - Solution

a) The full scale V_{fs} voltage is the one that corresponds to $D = D_3D_2D_1D_0 = 1111$. Then:

$$V_{fs} = -\frac{V_R}{R}\left(1+\frac{1}{2}+\frac{1}{4}+\frac{1}{8}\right)R_f = -\frac{15}{8}\frac{R_f V_R}{R}$$

If we suppose that $V_R = V_{OH} \cong V_{cc} = 5V$ (typical "new" datasheets values) is the output voltage of the counter when the clock pin Q_i are in the high state, then we get the following relation for the resistors:

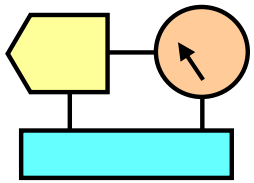
$$\frac{R_f}{R} = \frac{8}{15}$$

b) If we suppose that the presence of a switch introduces a resistance R_{ON} in series with R ($R_{ON} << R$) the equivalent output resistance for the MSB is $R_{ON} + R$. Then:

$$V_{OMSB} + \Delta V_{MSB} = -\frac{V_{CC}}{R_{ON}+R}R_f = -\frac{V_{CC}}{1+\frac{R_{ON}}{R}}\left(\frac{R_f}{R}\right) \cong -V_{CC}\left(\frac{R_f}{R}\right)\left(1-\frac{R_{ON}}{R}\right)$$

From which:

$$|\Delta V_{MSB}| = \left|V_{CC}\frac{R_{ON}}{R}\frac{R_f}{R}\right| = |V_{fs}|\frac{8}{15}\frac{R_{ON}}{R}$$



Problem 3 - Solution

The condition $|\Delta V_{MSB}| < \frac{1}{2}LSB$ thus becomes:

$$|\Delta V_{MSB}| = |V_{fs}|\frac{8}{15}\frac{R_{ON}}{R} < \frac{1}{2}\frac{|V_{fs}|}{2^4} \cong \frac{1}{2}\frac{|V_{fs}|}{15}$$

Finally:

$$16\,R_{ON} < R$$

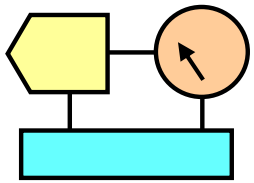
Example: If we use the relation: $R_{ON} = R_{OH} = \frac{V_{CC}}{|I_{OH}|}$ - $\frac{V_{OH}}{|I_{OH}|}$, and the typical "old" datasheets values: $V_{OH} = 4.6\ V, |I_{OH}| = 0.51\ mA$, we get: $R_{ON} = 784\ \Omega$.

Thus

$$R > 12.54\ k\Omega$$

If we use the E12 commercially available value, we might thus chose:

$R_{MSB} = 15\ k\Omega; R_{MSB-1} = 33\ k\Omega; R_{MSB-2} = 56\ k\Omega; R_{LSB} = 120\ k\Omega$ and $R_f = 8\ k\Omega$



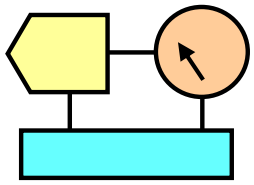
Problem 4 – Assignment
A/D conversion

Consider 4 analog signals in the range between 0 and 4 V and maximum frequency 50 kHz. The signals are analog-to-digital converted in a conversion system with one S/H and one A/D. The A/D converter has input dynamics -5 V to +5 V. Answer the following questions:

a) List in the order from input to the output the blocks of the data acquisition system and specify if a conditioning amplifier is necessary

b) If a conditioning amplifier is necessary, calculate the expression of the output voltage versus the input voltage.

c) 1. Choose the sampling frequency of the S/H to sample the channels with an oversampling factor of 3.
2. Choose a reasonable value for the conversion time of the ADC and for the acquisition time of the S/H to satisfy point 1.

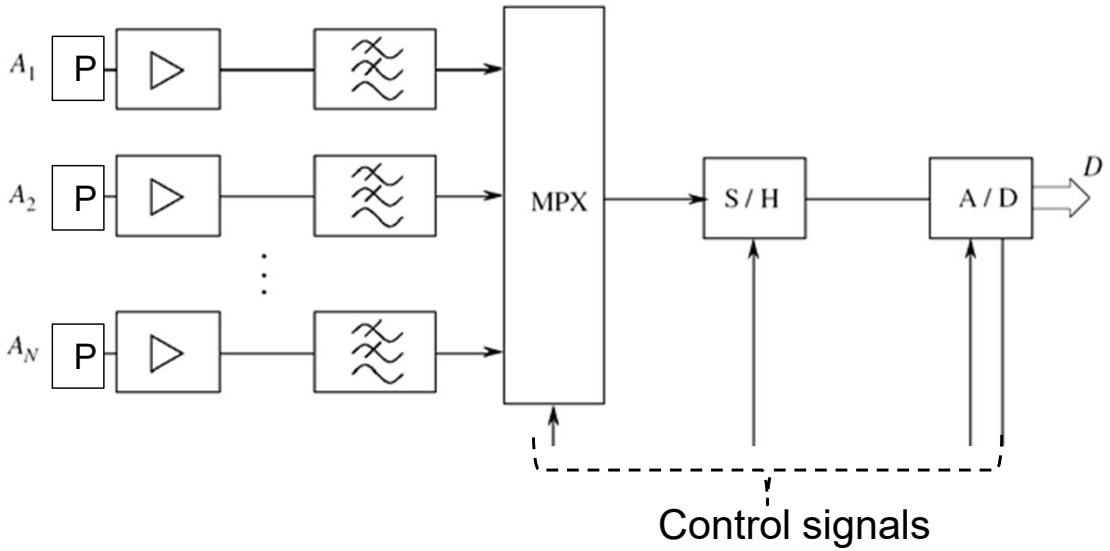


Problem 4 – Assignment
A/D conversion

d) Assuming the A/D is a successive approximation converter with following characteristics: DAC with settling time 80 ns, SAR with $t_{pCK->Q}$ = 10 ns, voltage comparator with negligible delay. Calculate the maximum clock frequency

Solution 1

Block diagram

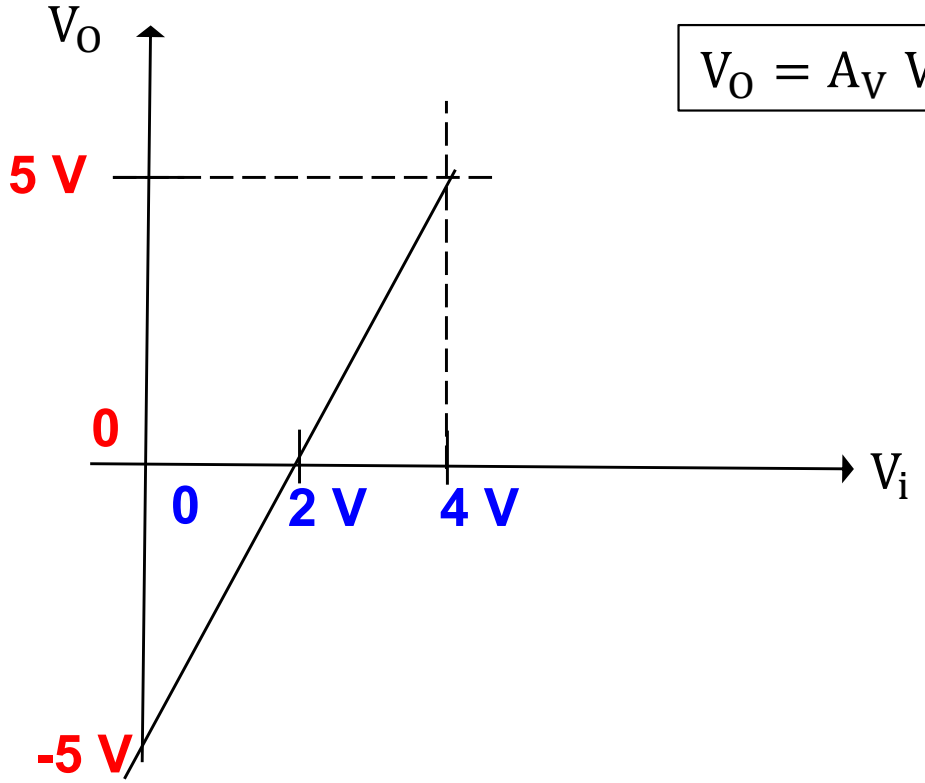


The blocks of the data acquisition system are in the order:

1. Protection circuit to limit the Analog signal voltage in the "safe" input range
2. Conditioning amplifier to adapt the input dynamics to the ADC converter dynamics and thus to reduce the SNR associate to the quantization error
3. Antialiasing filter to limit the Analog signal bandwidth and thus to reduce the aliasing error
4. Multiplexing to use the same S/H and ADC blocks for several channels
5. S/H unit to sample at discrete instant of time the Analog signal
6. ADC converter to convert the discrete Analog values in Digital values

Solution 2

The **conditioning amplifier** must be used because the signal dynamics is in the range from $0\ \mathrm{V}$ to $4\ \mathrm{V}$ while the A/D dynamics is from $-5\ \mathrm{V}$ to $5\ \mathrm{V}$, so the circuit of the conditioning amplifier must be associated to the following transfer function:



The input signal has to be multiplied by A_V = 10/4 = 5/2 and translated of $V_{off} = -\ 5\ \mathrm{V}$. This can be realized with a closed loop operational amplifier and a suitable choice of the resistors.

Solution 3

The **minimum sampling frequency** ($f_{s\,min}$) is determined by the Nyquist rule:

$$f_{s\,min,1channel} = 2 \times 50\ \text{kHz} = 100\ \text{kHz}$$

In case an oversampling factor of 3 is required:

$$f_{s,1channel} = 3\times 100\ \text{kHz} = 300\ \text{kHz}$$

$$f_{s,4channels} = 4 \times 300\ \text{kHz} = 1.2\ \text{MHz}$$

Since this corresponds to a sampling time $T_s = 1/f_{s,4channels} = 1/(1.2\ \text{MHz}) = 833\ \text{ns}$, reasonable values for the acquisition time T_{acq} and the conversion time T_c are respectively $T_{acq} = 400\ \text{ns}$ and $T_c = 400\ \text{ns}$ such that:

$$T_s > T_c + T_{acq}$$

Solution 4

Between two conversions the time is T_{ck} that coincides with the sampling time and it must be greater than the sum of the propagation from the CK to Q at the output of the SAR ($t_{pCK->Q}$), the time it takes for converting D to V_A' at the DAC (the settling time, t_{settl}), the time it takes for the comparison at the threshold comparator and the set-up time of the register. Thus, neglecting in this calculation the set-up time of the register and the comparator delay, we get a **maximum sampling frequency**:

$$f_{s\,max} = \frac{1}{T_{s\,min}} = \frac{1}{T_{ck\,min}} = \frac{1}{t_{settl} + t_{pCK->Q}} = \frac{1}{80\text{ ns} + 10\text{ ns}} = \frac{1}{90\text{ ns}} = 111\text{ MHz}$$