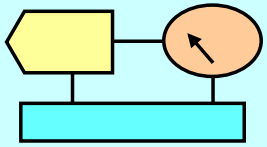


Applied Electronics
a.y 2021-22

Exercises and problems solved in class in preparation for the exam

Part D- Data Acquisition systems- Problem 1

Problem1: Consider a data acquisition system with 5 input channels. The signal in each channel can

be a triangular wave or a sine wave both with amplitude -500mV to 500 mV and maximum frequency 3kHz. The signal must be converted using only one A/D converter with input dynamics [-5V;5V]. Answer the following questions:

1. Draw the trans-characteristics of the conditioning amplifier and design the circuit.

2 Calculate the signal to noise ratio due to quantization error (SNRq) for both signals. The SNRq must be expressed as function of the number of bits *N* and of the A/D dynamics *S*.

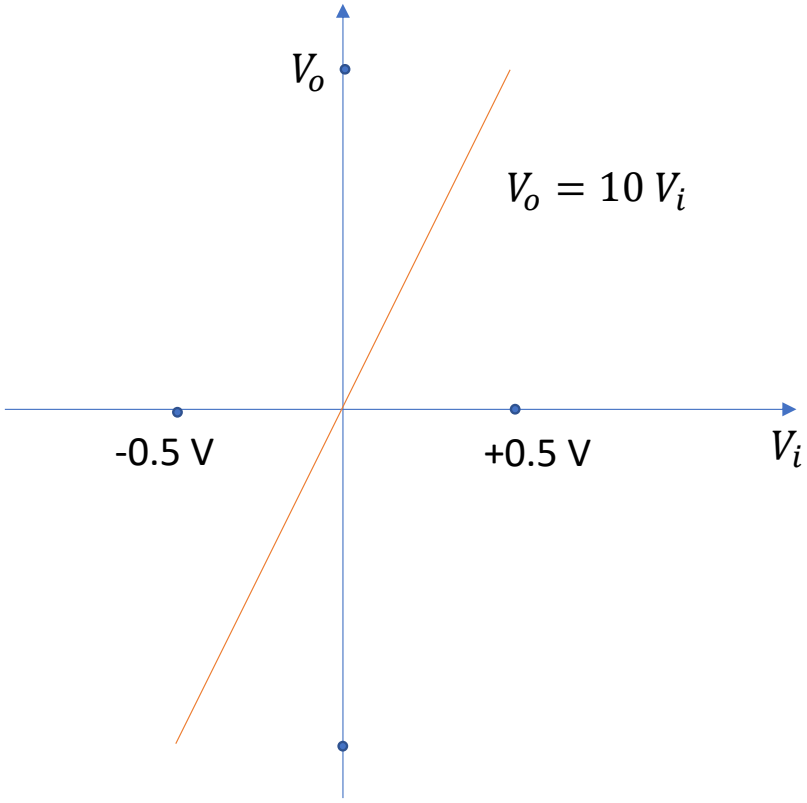
3 Calculate the number of bits N of the A/D converter to guarantee SNRq>28 dB.

4. Assuming that the other sources of errors reduce the SNR of other 8 dB calculate the ENOB.

5. The A/D is a successive approximation converter; calculate the clock frequency necessary to sample the signals with an over-sampling factor of 1.5. Assume that the S/H has an acquisition time of 10 μs.

Problem 1- solutions

1. Draw the trans-characteristics of the conditioning amplifier and design the circuit.



The circuit is a non-inverting voltage amplifier with amplification of 10.

2. Calculate the signal to noise ratio due to quantization error (SNRq) for both signals. The SNRq must be expressed as function of the number of bits *N* and of the A/D dynamics *S*.

For triangular signal: $SNR_{q,dB} = 10\log_{10}\frac{S^2}{12}\cdot\frac{12}{A_D^2}$ with $A_D = \frac{S}{2^N}$ ➔ $SNR_{q,dB} = 6N$ dB

For sinusoidal signal $SNR_{q,dB} = 10\log_{10}\frac{S^2}{8}\cdot\frac{12}{A_D^2}$ with $A_D = \frac{S}{2^N}$ ➔ $SNR_{q,dB} = 6N + 1.76$ dB

3. Calculate the number of bits N of the A/D converter to guarantee SNRq>28 dB.

We must consider the worst case that is the triangular signal.

➔ 6N>28 dB ➔ N=5

4. Assuming that the other sources of errors reduce the SNR of other 8 dB calculate the ENOB.

In the case of the sine wave and N=5 we have: SNRq=31.76 dB. This is reduced of 8dB due to the rest of the blocks of the system. $SNR_{tot} = 31.76dB - 8dB = 23.76dB$

By definition of ENOB: $\mathrm{ENOB} = \frac{SNR_{tot}-1.76}{6} = 3.67$

5. The A/D is a successive approximation converter; calculate the clock frequency necessary to sample the signals with an over-sampling factor of 1.5. Assume that the S/H has an acquisition time of 10 μs.

To sample with oversampling factor K=1.5 we must sample one single channel with sampling frequency

$$f_{s1} = 1.5 \cdot 2 \cdot f_{i,max} = 9kHz$$

The S/H samples at frequency $f_s = N_{\{channels\}} \cdot f_{s1} = 45\ kHz$

During one sampling period we must fit the switching time of the MUX, the acquisition of the signal and the conversion time of the ADC ➔

$$T_s = \frac{1}{f_s} = T_{acq} + T_{MUX} + Tc$$

We assume the delay of the MUX is negligible, we find $Tc = T_s - T_{acq} = 12.23\mu s = \mathrm{N} \cdot T_{ck}$

With N=5 we get: fck= $\frac{5}{12.23\mu s} = 408kHz$

Part D- Data Acquisition systems- Problem 2

A 8bit A/D tracking converter is used to convert a sine wave with amplitude $1V_{PP}$. The CK frequency of the converter is fck=1MHz; the DAC has 1LSB=10mV.

1. Calculate the maximum sine wave frequency to avoid overload condition.

2. Calculate the conversion rate when the converter works in tracking mode.

3. The same input sine wave is converted with 8 bit successive approximation ADC with f_{ck}=1MHz, calculate the maximum frequency of the sine wave that can be converted. Assume the acquisition time of the S/H is 1.5μs.

1. Calculate the maximum sine wave frequency to avoid overload condition.

The ADC operates in tracking mode (ie: no overload) when the maximum voltage variation in one CK period is less than A_D.

$$\max\left\{\frac{dV}{dt}\right\} \cdot T_{CK} < A_D$$

For sinusoidal signal:

$$V_{in}(t) = 0.5\, V_{i,PP} \sin(2\pi f t)$$

$$\max\left\{\frac{dV}{dt}\right\} = 0.5\, V_{i,PP} \cdot 2\pi f \Longrightarrow 0.5\, V_{i,PP} \cdot 2\pi f < \frac{A_D}{T_{CK}}$$

$$f_{max} = \frac{A_D}{V_{i,PP}} \cdot \frac{f_{CK}}{\pi} = 3.2kHz$$

2. Calculate the conversion time when the converter works in tracking mode.

In tracking mode (ie: when we assure that the input signal changes slowly) the ADC can follow the input signal by increasing/decreasing the output of 1 bit during each clock period. The conversion time is equal to the CK period ➔ $T_C = T_{CK} = 1\mu s$.

3. If the same input sine wave is converted with 8 bit successive approximation ADC with f_{ck}=1MHz, calculate the maximum frequency of the sine wave that can be converted.

By employing a SAR ADC, we have $T_c=NT_{ck}=8\mu s$

The minimum sampling period is $T_s=T_c+T_{acq}$ ➔ maximum sampling frequency is therefore $f_s=1/(T_c+T_{acq})$

Nyquist rules requires the maximum frequency of the input signal to be one-half of the sampling frequency

➔ $f_{i,max} = \frac{1}{2} \cdot \frac{1}{T_c+T_{acq}} = 52.6kHz$

Part B- Digital Electronics: Problem 1

Consider the combinational logic function: **Out= not(A or (B and C))** realized in CMOS technology.

1) Plot the circuit and answer the following questions:

a. how many NMOS are needed?

b. how many NMOS must be connected in series?

c. how many PMOS are needed?

d. how many PMOS must be connected in parallel?

2)

Assuming the MOS transistors have Ron=70Ω, calculate the maximum delay for H-L and L-H transition to drive 5 gates with input capacitance Ci=5pF each.

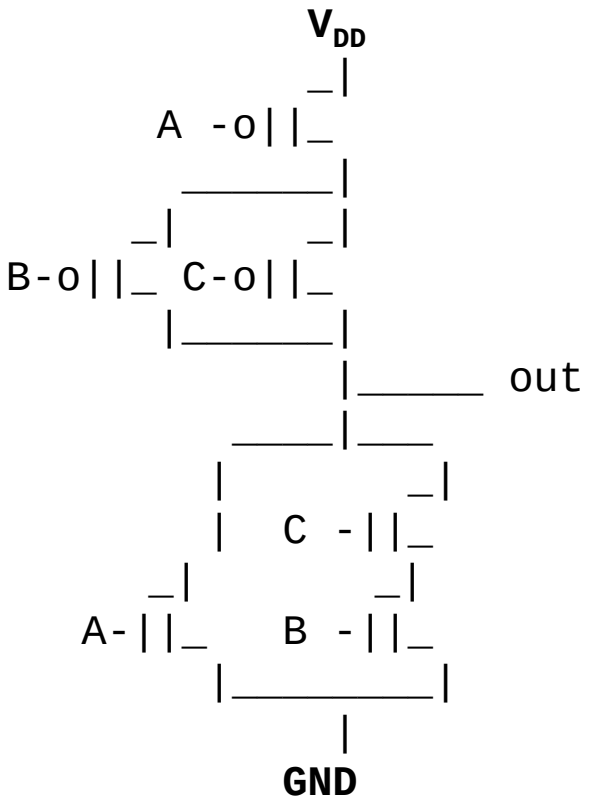
1) Plot the circuit and answer the following questions:

a. how many NMOS are needed? 3NMOS

b. how many NMOS must be connected in series? 2 NMOS

c. how many PMOS are needed? 3 PMOS

d. how many PMOS must be connected in parallel? 2 PMOS



2)

Assuming the MOS transistors have Ron=70Ω, calculate the maximum delay for H-L and L-H transition to drive 5 gates with input capacitance Ci=5pF each.

Total load capacitance connected to the output is $C_L = 5 \cdot 5pF = 25\,pF$

For L➔ H transition we have that some of the PMOS transistors turn ON to guarantee the connection to V_{DD} .

In general, the delay is $t_d = 0.69 \cdot C_L R_{eq}$. The maximum delay $t_{d,LH}$ is when the equivalent resistance (connecting to V_{DD} is the maximum). It is the case when PMOS-A is ON and one of the two PMOS in parallel (PMOS-B or PMOS-C) are ON.

➔ $\max R_{eqH} = 2R_{ON} = 140\Omega$ ➔ $t_{d,LH,max} = 0.69 \cdot 25pF \cdot 140\Omega$=2.42ns

For H➔ L transition we have that some of the NMOS transistors turn ON to guarantee the connection to GND. .

In general, the delay is $t_d = 0.69 \cdot C_L R_{eq}$. In this case the maximum delay $t_{d,HL}$ is when the equivalent resistance (connecting to GND is the maximum): that is when NMOS-A is OFF and the two NMOS in series are both ON

➔ $\max R_{eqL} = 2R_{ON} = 140\Omega$ ➔ $t_{d,HL,max} = 0.69 \cdot 25pF \cdot 140\Omega$=2.42ns

Part B- Digital Electronics: Problem 2

Consider a DRAM memory with 11 bit address: 8 bits are used for row decoder and 3 bits are used for column decoder. Each word is 8 bit. The pass transistors have drain parasitic capacitance Cd=0,2fF and threshold voltage Vth=0,2V; voltage supply is Vdd=2V. Answer the following questions:

1):

Sketch the matrix structure of the memory and calculate

- the number of bit lines
- the number of pass transistors connected to one bit line
- the total number of pass transistors of the memory.

2)

The sense amplifier can sense a minimum voltage level of 50mV, calculate the minimum value of the storage capacitor Cs.

1) Sketch the matrix structure of the memory and calculate:

- the number of bit lines
- the number of pass transistors connected to one bit line
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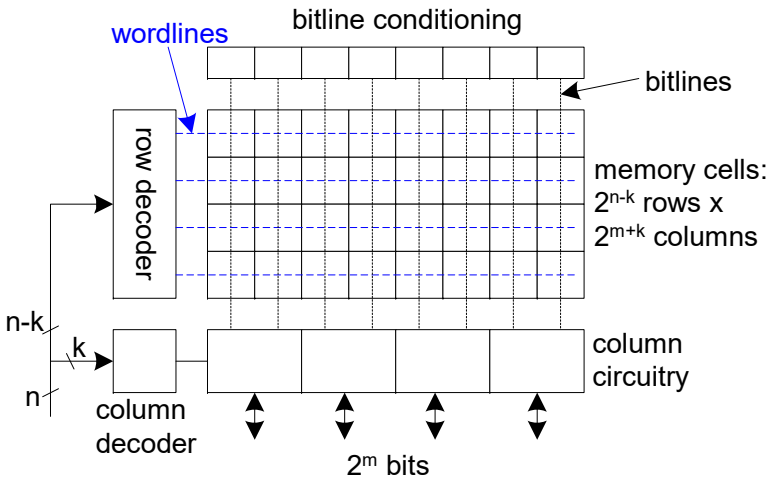


The memory is a matrix of words. Each word is 8 bit, which means each word consists in 8 memory cells.

The rows are addressed by the row address of 8bit ➔ we address in total 2^8 rows.

The columns are address by 3 bit ➔ we address in total 2^3 columns. Note that each column is a word; so the total number of column is 2^3*8 !!!

In conclusion we have a matrix of DRAM cells that is 2^8 x (2^3*8)

Answers:

- number of bit lines= 2^3*8=64
- number of pass transistors connected to one bit line: 2^8=256
- total number of pass transistors is equal to the total number of cells ➔ 2^3*8*2^8=16384

2) The sense amplifier can sense a minimum voltage level of 50mV, calculate the minimum value of the storage capacitor Cs

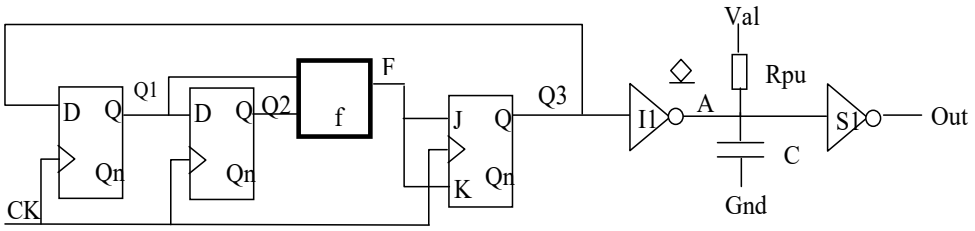
The voltage variation for reading must be higher than the minimum voltage that can be sensed by the sense amplifier

$\Delta V = \frac{(V_{bit} - \frac{V_{DD}}{2} - V_{TH})}{C_S + C_{BL}} \cdot C_S \geq 50mV$

Where C_{BL} is the total capacitance of one bit line ➔ $C_{BL} = number\ of\ rows \cdot C_d = 2^8 \cdot 0.2fF = 51.2fF$

Assuming V_{bit}=V_{DD} ➔ $C_S \geq \frac{50mV}{0.8V} \cdot C_{BL} = 3.4fF$

Part B- Digital Electronics: Problem 3



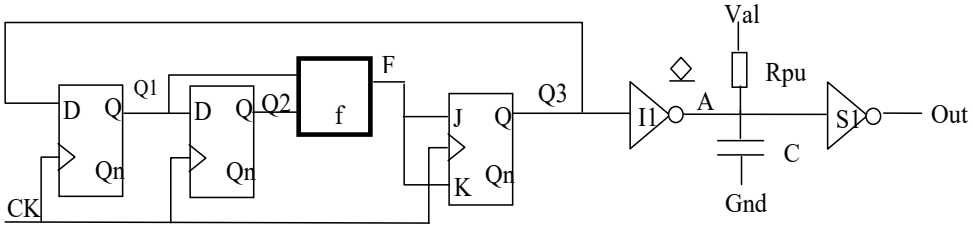
In the sequential circuit shown in the figure, the combinational logic function *f* is: F=NOT(Q1● NOT(Q2)) .

1) Plot the timing diagram of the outputs Q1,Q2,Q3,OUT. Consider the following parameters: CK period of 50 ns, capacitor C=0; time delays of I1 and S1 (equal for both LH and HL transitions) are 2ns; FF -D: T*ck->Q* =5 ns, Tsu = 4ns; FF JK : T*ck->Q* = 7ns, Tsu = 6ns; combinational logic block *f* : $T_{d,LH}$= 4ns , $T_{d,HL}$= 8 ns.

2) Calculate the static power consumption to set voltage levels in A; assume C=10pF and R_{PU}=10kΩ

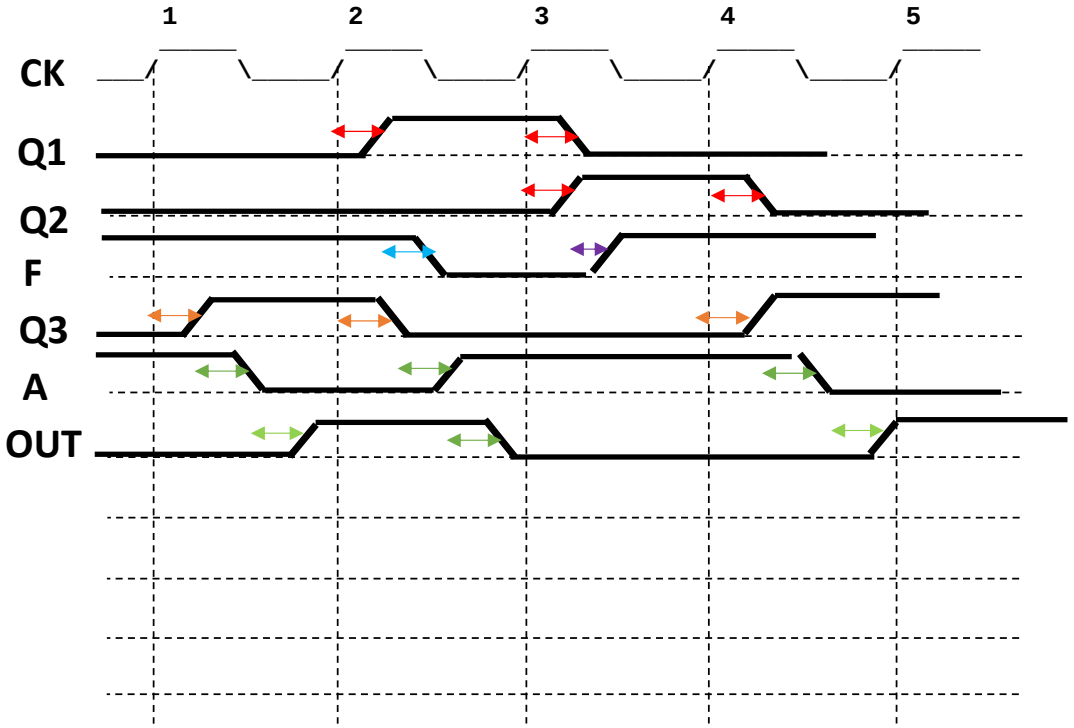
3) Calculate the maximum CK frequency.

1) CK period of 50 ns, capacitor C=0; time delays (equal for both LH and HL transitions): FF -D: T*ck->Q* =5 ns, Tsu = 4ns; FF JK : T*ck->Q* = 7ns, Tsu = 6ns; combinational logic block *f* : $T_{d,LH}$= 4ns , $T_{d,HL}$= 8 ns.



F=NOT(Q1● NOT(Q2)) .

We start assuming all outputs Qi are reset to "0"



FF-JK $T_{CK\rightarrow Q}$ 7ns

Inverter delay 2ns

FF-D $T_{CK\rightarrow Q}$ 5ns

$T_{d,HL}$= 8 ns

$T_{d,LH}$=4ns

2) Calculate the static power consumption to set voltage levels in A; assume C=10pF and R_{PU}=10kΩ

Static power consumption is not null when A is at logic state "0" because we have current flowing in the pull-up resistor. If A stays low for half of the time, we have:

$$P_S = 0.5 \cdot \frac{V_{al}^2}{R_{PU}} = 0.5 \cdot \frac{(5V)^2}{10k\Omega} = 1.25\ mW$$

3) Calculate the maximum CK frequency.

Worst case is for JK-FF ➔

$T_{CKmin} = T_{CK\rightarrow QFF1,2} + \max T_{d,f} + T_{setupJK}$=19 ns ➔ $f_{CK,max}$=52.6MHz

Part C- Interconnections : Problem 1

A track on PCB is 30 cm long and connects a driver to several slots (receivers) distributed along the line. The track (without the connected loads) has characteristic impedance Z_{∞}=65 Ω and the propagation speed is 0.65c. The capacitive load of the receivers increases the capacitance per unit length of the line of a factor of 3.5. The driver voltage supply is Vdd=3.3V. Electrical parameters of the receivers are: Vih=2.2V; Vil=1.4V; Iih,Iil=100nA.

1) Calculate the characteristic impedance and the propagation delay t_p including the effect of the loads.
2) Calculate the output resistance of the driver, to drive the receiver in IWS (incident wave switching) mode and noise margin 0.6V
3) If the transmission line is terminated with a resistance R_T=200 Ω, calculate the voltage at the far-end at t=tp and the voltage at the near-end at t=2tp.

1) Calculate the characteristic impedance and the propagation delay t_p including the effect of the loads.

$Z'_\infty = \frac{65\Omega}{\sqrt{3.5}} = 34.75\ \Omega$ propagation speed reduces of the same factor $u' = \frac{u}{\sqrt{3.5}}$

And propagation delay increases proportionally ➔ $t'_p = \frac{Length}{u'} = 2.88\ ns$

2) Calculate the output resistance of the driver, to drive the receiver in IWS (incident wave switching) mode and noise margin 0.6V

In IWS the first incident step must be high enough t be recognized as a high voltage ➔

$$V_B(0) = \frac{Z_\infty{}'}{Z'_\infty + R_o} \cdot V_{DD} + NM = 2.8\ V \Longrightarrow R_o = 6.2\ \Omega$$

3) If the transmission line is terminated with a resistance R_T=200 Ω, calculate the voltage at the far-end at t=2tp and the voltage at the near-end at t=3tp.

With output resistance of the driver as in point (2) we have at the far-end:

$$V_C(t_p') = V_B(0) \cdot (1 + \Gamma_T) = V_B(0) \cdot \left(1 + \frac{R_T - Z'_\infty}{R_T + Z'_\infty}\right) = 4.76$$

At the near end we have:

$$V_B(2\ t_p') = V_B(0) + V_B(0)\Gamma_T + V_B(0)\Gamma_T \cdot \Gamma_B$$

$$\Gamma_B = \frac{R_o - Z_\infty'}{R_o + Z_\infty} = -0.7 \Longrightarrow V_B(2\ t_p') = 3.39\ \text{V}$$