Applied electronics

Iniziato	lunedì, 20 luglio 2020, 13:20
Stato	Completato
Terminato	lunedì, 20 luglio 2020, 13:26
Tempo impiegato	6 min. 16 secondi
Valutazione	Non ancora valutato

Domanda 1

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a square wave generator realized with Schmitt trigger inverter; the voltage on the capacitor varies with time as:

- (a) exponential ✓
- (b) square wave
- (c) linear
- (d) is always zero

Risposta corretta.

La risposta corretta è: exponential

Domanda 2

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a D-Latch active when LE is low (=0). When LE=0:

- (a) the output state follows the input state D ✓
- (b) the output is always 1
- (c) the output is in memory state
- (d) the output is always 0

Risposta corretta.

La risposta corretta è: the output state follows the input state D

Domanda 3

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a 4 bit weighted resistor DAC; the ration bewtween the resistance of the MSB branch (R_{MSB}) and the resistance of the LSB (R_{LSB}) branch is:

- (a) $R_{MSB}/R_{LSB}=0.125$ ✓
- (b) $R_{MSB}/R_{LSB}=8$
- (c) $R_{MSB}/R_{LSB}=0.5$
- (d) $R_{MSB}/R_{LSB}=4$

Risposta corretta.

La risposta corretta è: $R_{MSB}/R_{LSB}=0.125$

Domanda 4

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The efficiency (ie: ratio between output and input power) of a series linear volatge regulator, with input Vi and output Vo can be approximated as:

- (a) Vo/Vi ✓
- (b) Vi/Vo
- (c) Vo/(Vi+Vo)
- (d) $\sqrt{Vi/Vo}$

Risposta corretta.

La risposta corretta è: Vo/Vi

Domanda 5

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

If we double the clock frequency of a CMOS digital circuit, the dynamic power consumption will increase of a factor equal to:

- (a) 2 ✓
- (b) 4
- (c) 8
- (d) does not change

Risposta corretta.

La risposta corretta è: 2

Domanda 6

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a FPGA; a Look-Up Table (LUT) with 3 inputs needs:

- (a) 8 SRAM memory cells ✓
- (b) 8 FAMOS
- (c) 4 NAND gates and 8 NOR gates
- (d) 8 NAND gates and 4 NOR gates

Risposta corretta.

La risposta corretta è: 8 SRAM memory cells

Domanda 7

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The reflection coefficient of a matched termination of a transmission line is:

- (a) 0 ✓
- (b) 1
- (c) -1
- (d) 0.5

Risposta corretta.

La risposta corretta è: 0

Domanda 8

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Vo is the output voltage of a logic gate , choose the right condition for connecting Vo to the input of another logic gate (the voltage supply is V_{DD}):

- (a) Vo=Vih+NM ✓
- (b) Vil<Vo<Vih
- (c) Vo=Vil+NM
- (d) Vo<0
- (e) Vo>V_{DD}

Risposta corretta.

La risposta corretta è: Vo=Vih+NM

Domanda 9

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a NAND flash memory; the elementary units for erasing and writing operations are:

- (a) block (= erasing of several pages) and page (=elementary unit that can be written) ✓
- (b) page (=erasing of several blocks) and byte (=elementary unit that can be written)
- (c) block (= erasing of several pages) and byte (=elementary unit that can be written)

Risposta corretta.

La risposta corretta è: block (= erasing of several pages) and page (=elementary unit that can be written)

Domanda 10

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

A DRAM memory cell consists in:

- (a) one MOS and one capacitor ✓
- (b) one FAMOS
- (c) 6 MOS
- (d) one MOS and 2 capacitors

Risposta corretta.

La risposta corretta è: one MOS and one capacitor

Domanda 11

Completo

Punteggio max.: 5,0

We have 4 analog input channels with voltage in the range between -0.5V and +0.5V. The maximum frequencies of the channels are $F_{max,1}$ = 3 kHz, $F_{max,2}$ = 2,5 kHz, $F_{max,3}$ = 1 kHz, $F_{max,4}$ = 2 kHz. The acquisition system uses only one S/H and only one tracking ADC with input dynamic range [0, +10 V]. The channels are oversampled with oversampling factor of 2.5.

Request 1:

List the various blocks of the acquisition system and define the role of each block. Indicate the relation V_{out} versus V_{in} of the conditioning amplifier .

Request 2:

Calculate the sampling frequency of the S/H

Request 3:

The ADC operates in overload condition; if the maximum ADC conversion time must be Tc=8.5 μs, calculate the number of bits assuming that the clock frequency 250 MHz.

Request 4:

With the number of bits of previous point, calculate the SNRq for input sinusoidal signals

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Request 1:

Conditioning amplifier: Av=10, offset +5V. ==> Vo=Av*Vi+offset

Request 2:

Sampling freqeuncy of S/H is: fs=max{Fmax,i}*2*2.5*4=3KHz*2*2.5*4=60kHz ==> Ts=16.7us

Request 3:

In overload condition, the conversion time is Tc=2^N*Tck=8.5us => N=log(8.5*250)/log(2)=11

Request 4:

SNRq=(6*N+1.76) dB=67.76dB

Domanda 12

Completo

Punteggio max.: 5,0

One driver with Vdd=3,3 V is connected on one side of a transmission line with Z_∞ = 60 Ω, propagation speed U = 0,7 C, length 15 cm and open circuit termination. The receivers are CMOS circuits with Vil = 1V, Vih = 2,2 V. Answer the following questions for a L->H transition:

Request 1:

Calculate the range of values of the output resistance of the driver (Ro) to drive the line in Reflective Wave Switching (RWS) mode and not in Incident Wave Switching mode, when only one receiver is connected at the near-end of the line.

Request 2:

With Ro = 80 Ω, calculate the maximum and minimum transmission times and the skew for a receiver connected in the near-end and a receiver connected in the far-end.

Request 3:

This interconnection is used for a parallel synchronous write bus protocol. The receiver registers have set-up time Tsu = 5 ns and hold time Th = 2 ns. Calculate the delay between the DATA and STB signals and the duration of the write cycle.

Request 1:

In RWS mode the volatbe at Vb(2tp) is the sum of the incent plus reflected voltage and must be recongnized as high => Vb(2tp)= **$2* Z_\infty / (Z_\infty+R0)*Vdd>Vih$ ==> R0<120ohm**

To avoid the switching on the first incindet voltage step (IWS mode) we must set: Vb(0)<Vih ==> Vb(0)= **$Z_\infty / (Z_\infty+R0)*Vdd<Vih$ ==>R0>30ohm**

This implies:

30Ω< R0<120 Ω

Request 2:

Tp=0.71ns

First incident voltage step: VB(0)=1.4V >Vil =>

For the receiver connected to the near-end:

Ttxmin=0 ns because Vb(0)>Vil

Ttxmax=2tp because we need the back reflected voltage such that >Vih

For the receiver connected to the far-end: Vc(Tp)>Vih always therefore

Ttxmin=Ttxmax=tp

Tk=Ttxmax-Ttxmin=2tp=1.42ns

Request 3:

Delay between DATA and STB for the case of write cycle: ta=tk+tsu=1.42ns+5ns=6.42ns

Duration of the write cycle: 2tk+tsu+th=2*1.42+5+2=9.84ns

Domanda 13

Completo

Punteggio max.: 5,0

Consider the sequential circuit shown in the figure. All outputs Q are initially reset to zero. The block *f* is a combinational logic block with function F = not(Q1· not(Q2)) . Assume C=0;

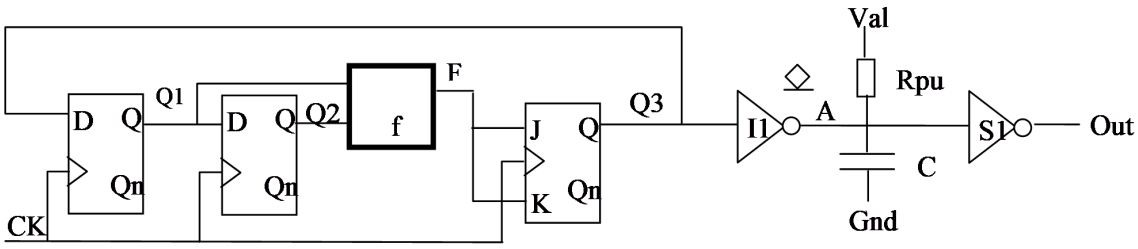
Dynamics parameters are:

FF D: T*ck->Q* =5 ns, Tsu = 4ns;

FF JK : T*ck->Q* = 7ns, Tsu = 6ns;

combinational logic block *f* : TLH*f* = 3ns , THL*f* = 6 ns;

inverters I1 and S1: TLH=4 ns; THL=2ns



Request 1:

Answer the following questions assuming the CK period is 60ns:

- which are the inital states of F, A and Out?

- how many CK rising edges are necessary to switch Q3 to high state?

- calculate the delay between a transition L->H of Q3 and the switch of Q1 to High

- calculate the delay between a transition L->H of Q3 and the switch of F to Low

- calculate the delay between a switch L->H of Q3 and the switch of the state OUT

Request 2:

Calculate the maximum CK frequency

Request 1:

Answer the following questions:

- which are the inital states of F, A and Out? **F=1; A=1; Out=0**

- how many CK rising edges are necessary to switch Q3 to high state? **F=1; J=K=1 therefore the JKFF swithes at the first CK rising edge**

- calculate the delay between a transition L->H of Q3 and the switch of Q1 : Q1 switches on the second rising edge of the CK, the delay between the L to H transition of Q3 and Q1 is : **(60-7)ns + 5 ns=58ns**

- calculate the delay between a transition L->H of Q3 and the switch of F: **F switches to L as consequence of the transition to H of Q1. It is delayed respect to Q1 of 6ns. The delay respect to the transition of Q3 is 58+6ns=64ns.**

- calculate the delay between a switch L->H of Q3 and the switch of the state OUT: **we sum the delay for H->L transition of I1 (THL=2ns) and the delay for L->H transition of S1 (TLH=4ns). The total delay is (2+4)ns=6ns**

Request 2:

Calculate the maximum CK frequency

IThe worst case is for the FF JK :

Tck->Q1,2+Tdmax of *f*+TsuJK=5ns+6ns+6ns=17ns fckmax=58.8MHz

Domanda 14

Completo

Punteggio max.: 5,0

Consider a DRAM memory with 8 bit address (all 8 bits are used for row decoder) and 8 bit word. Pass transistors have drain parassitic capacitance Cd=0,2fF and threshold voltage Vth=0,1V; voltage supply is Vdd=1V. Answer to the following questions:

Request 1:

Calculate

- the number of bit lines
- the number of pass transistors connected to one bit line
- the total number of pass transistors of the memory.

Request 2:

Calculate the minimum value of the storage capacitor Cs, if the sense amplifier can sense a minimum voltage level of 70mV.

Request 1:

number of bitline: 8

number of rows: 2^8=256 => 256 pass transistor connected to one bit line

total number of pass transistor 256*8=2048

Request 2:

The parassitic capacitance of the BL is: CBL=2^8*0.2fF=51.2fF

The bitline variation of the voltage during the read must be sensed by the amplifier therefore must be higher than 70mV =>

ΔVbl = Cs/(Cs+Cbl) * (Vdd/2 – Vth)>70mV => Cs>=10.86fF

Domanda 15

Completo

Punteggio max.: 1,0

OPTIONAL Question on virtual lab:

Analog-to-digital and Digital-to-Analog converters

Which components do you need in the LTspice software to realise and simulate a DAC circuit analogous to the one considered during the virtual LAB?

Domanda 16

Completo

Punteggio max.: 1,0

OPTIONAL Question on Virtual Lab

Logic gates and simple sequential logic circuits:

How could you check using the LTspice software the correct operation of a synchronous counter such as the 4-bit CD4029 used during the virtual LAB?

Domanda 17

Completo

Punteggio max.: 1,0

OPTIONAL QUESTION on Virtual LAB

Transmission lines:

How could you simulate and characterise with the LTspice software the effect of a capacitive load connected at the far end of a transmission line with matched termination? What do you expect to observe at the near end? Consider L to H transition.
