LAB QUESTIONS AND ANSWERS

Analog-to-digital and Digital-to-Analog converters 1

Which components do you need in order to realise a DAC circuit analogous to the one considered during the EXPERIMENTAL LAB?

In order to realise a DAC we need:

1. A synchronous counter like the CD4029;
2. A square wave generator for the clock;
3. An operational amplifier like the OP1177;
4. Some weighted resistors for the network;

Analog-to-digital and Digital-to-Analog converters 2

Which are the main logic blocks that you need in order to realise an A/D tracking converter analogous to the one considered during the EXPERIMENTAL LAB?

4-bit U/D synchronous counter driven by a signal generator

Weighed resistors network made by resistors: $R_4 = R$, $R_3 = 2R$, $R_2 = 2^2R$, $R_1 = 2^3R$ where R_i is the resistor on the branch Qi of the counter where Q4 is the most significativebit output

Operational amplifier OA1 in a closed loop configuration with a feedback resistor R_5 that

converts the output current in the output voltage V_{DAC}
Parts 1, 2, 3 constitute the D/A converter the output of which is the best approximationV_{DAC} of the analog signal

Operational amplifier OA2 used as **comparator** between the analog input signal V_i andits best approximation represented by the signal V_{DAC} at the output of the D/A converter

Diode-resistor network that guarantees that the output of OA2 falls within the acceptedvalue for the U/D command of the counter

A **sine wave generator** was used to generate the analog input signal V_i and the digital signalD result of the conversion was obtained at the output of the counter.

Analog-to-digital and Digital-to-Analog converters 3

When is it possible to observe the phenomenon of "glitches" affecting the performance of a DAC converter similar to the one realised during the EXPERIMENTAL LAB? Explain the origin of the glitch.

The phenomenon of “glitches” occurs when there is a **delay in the switching of one bit** in a DAC converter system. A glitch is an error that consists in a sudden change in the value of the output towards a largely wrong value; this can happen when the switching of the output to the next number leads to a change of multiple bits (e.g. 0111 to 1000). In the LAB a DAC based on a synchronous counter and a weighted resistor network has been implemented and the phenomenon of “glitches” has been induced by connecting to one of the counter output a small capacitor (from 50 pF to 50 nF) to the GND.The polarity of “glitches” reflects the direction of bit switching.

Example of “glitches”

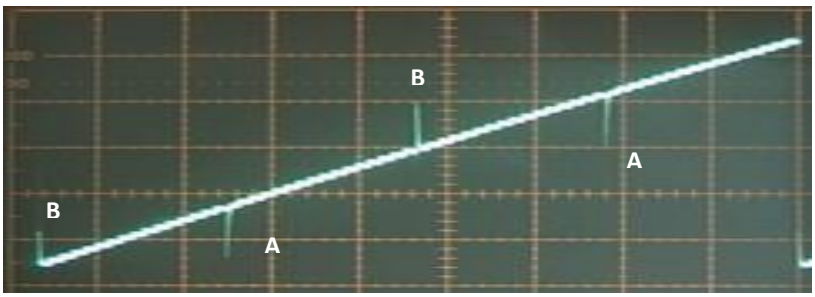

Figure 6 – Experimental waveform associated with the presence of a capacitor on MSB-1

Analog-to-digital and Digital-to-Analog converters 4

Considering a DAC circuit analogous to the one implemented in the EXPERIMENTAL LAB, which type of error do you expect to observe on the converted Analog signal if an error affect the MSB branch of the DAC weighted network?

It is expected to have a non-linearity error affecting the uppermost part of the output signal (the one where MSB=1).

Logic gates and simple sequential logic circuits 1

How can you visualise using the oscilloscope the trascharacteristic of a CMOS inverter? Which information can you extract from this plot about the logic gate performance?

1) Use a **triangular wave** voltage generator with suitable parameters that generates the input signal V_{in}

2) Connect it to the input of the CMOS component under test

3) Set the oscilloscope in (XY) mode

One can extract information about the **static parameters** of the CMOS inverter for a given voltage supply (V_{IL},V_{IH}, V_{OL},V_{OH}) and for e.g. the presence of hysteresis that differentiates a Schmitt trigger for a standard inverter.

Logic gates and simple sequential logic circuits 3

How could you check using the LTspice software the correct operation of a synchronous counter such as the 4-bit CD4029 used during the virtual LAB?

In case of correct counter operation and in presence of square wave clock signal, by comparing the frequency of the different counter output Qi (i=1:4) it must be observed that each **Qi output has a frequency halved with respect to that of the Qi-1 output**, and that the frequency of Q1 is half the clock frequency.

Transmission lines 1

Which behaviour do you expect to observe if you visualise with the oscilloscope the voltages at the near and far end of a coaxial cable described by a transmission line model (with characteristic impedance Zinf=50Ohm) with open termination and connected to a square wave generator characterised by an internal resistance of RG=50Ohm on the driving side?

After the **L->H transition** (t=0) since the reflection coefficient at the driving side is $G_G = 0$ while at the termination is $G_T = 1$ we expect (using for e.g. the lattice diagram) to observe the voltage at the driving end (Vb) starting at the value $V_0=V_1Z_0/(Z_o+R_G)=V_1/2$, were V_1 is the voltage provided by the voltage signal generator and corresponding to the H-level, and reaching the value $2V_0 = V_1$ after a time $2t_p$. At the termination we expect to observe the voltage (Vc) starting from 0V at time t = 0 and reaching a value of $2V_0 = V_1$ after a time t_p.

After a **H->L transition** (t=0) we will expect to observe the voltage at the termination Vc to drop to 0 V after a time t_p, while the voltage at the driving end Vb starting from the value V_1 at t=0 and reaching the value 0 V after $2t_p$

Transmission lines 2

How can you realise in the EXPERIMENTAL LAB a Time Domain Reflectometer able to measure the length of a coaxial cable behaving as a transmission line?

The length of the RG 58 coaxial cable can be measured:

-by connecting the 'near end' of the cable to a **square wave signal generator** (with output impedance of ≅ 50 W) and leaving open its 'far end';

-by measuring with an oscilloscope the **width of the intermediate voltage step** at the near-end that is equal to $2t_p$, where t_p is the propagation time of the coaxial cable;

-by multiplying t_p for the **propagation speed** of the cable that can be read on its datasheet.

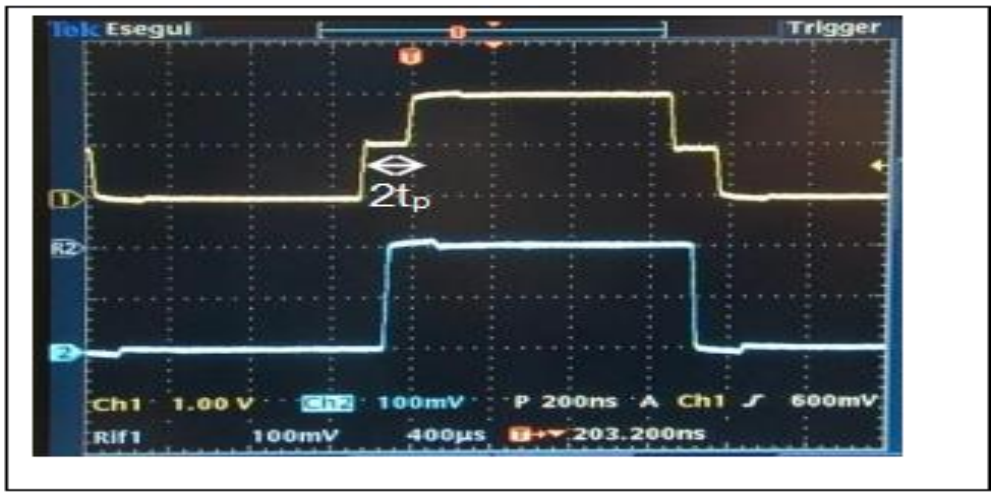

Figure 5. Waveforms at the 'near' (top trace) and 'far' (bottom trace) end of a transmission line matched at the driving end with open termination