Exam 30th June 2020

Solution of Quiz and problems

Quiz

Domanda 1
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

The ADC of a data acquisition system provides a SNRq=65.76dB, whereas the total SNR is degraded of other 10dB due to the non-idealities of the other blocks. Calculate the ENOB.

- (a) ENOB=9 ✓
- (b) ENOB=10
- (c) ENOB>10
- (d) ENOB<8

Risposta corretta.
La risposta corretta è: ENOB=9

Commenta o inserisci punteggio a mano

Storico delle risposte

Passo	Data/Ora	Azione	Stato	Punteggio
1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: ENOB=9	Risposta salvata	
3	**30/06/2020 13:09**	**Tentativo terminato**	**Risposta corretta**	**1,0**

Domanda 2
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

Consider an asynchronous serial protocol. The protocol requires:

- (a) one start bit and one stop bit ✓
- (b) only one start bit, a no stop bit
- (c) no start bit and one stop bit
- (d) no start bit and no stop bit

Risposta corretta.
La risposta corretta è: one start bit and one stop bit

Commenta o inserisci punteggio a mano

Storico delle risposte

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1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: one start bit and one stop bit	Risposta salvata	
3	**30/06/2020 13:09**	**Tentativo terminato**	**Risposta corretta**	**1,0**

Domanda 3
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

Consider a L➔H transition propagating in a transmission line with characteristic impedance Z_0 and matched termination. The output resistance of the driver is R_0=0.5 Z_0 and V_{DD}=3.3V. The first incident voltage step is:

- (a) 2.2 V ✓
- (b) 1.5 V
- (c) 3.3 V
- (d) 1.65 V

Risposta corretta.
La risposta corretta è: 2.2 V

Commenta o inserisci punteggio a mano

Domanda 4
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

The output voltage of buck regulators is:

- (a) Vout<Vin ✓
- (b) Vout>Vin
- (c) Vout=Vin
- (d) Vout=2 Vin

Risposta corretta.
La risposta corretta è: Vout<Vin

Commenta o inserisci punteggio a mano

Storico delle risposte

Passo	Data/Ora	Azione	Stato	Punteggio
1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: Vout<Vin	Risposta salvata	
3	**30/06/2020 13:09**	**Tentativo terminato**	**Risposta corretta**	**1,0**

Domanda 5
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

The conversion time Tc of a Successive Approximation Converter can be reduced of a factor 2 by:

- (a) doubling the CK frequency of the SAR ✓
- (b) doubling the CK period of the SAR
- (c) doubling the number of bit of the SAR
- (d) none of the answers reported here is the correct one

Risposta corretta.
La risposta corretta è: doubling the CK frequency of the SAR

Commenta o inserisci punteggio a mano

Storico delle risposte

Passo	Data/Ora	Azione	Stato	Punteggio
1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: doubling the CK frequency of the SAR	Risposta salvata	
3	**30/06/2020 13:09**	**Tentativo terminato**	**Risposta corretta**	**1,0**

Domanda 6
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

The trend (during the last 40 years) of the number of transistors in microprocessors shows that:

- (a) The number of transistors doubles every two years ✓
- (b) The number of transistors is increased of a factor 4 every two years
- (c) It is impossible to find a clear trend
- (d) As consequence of the increased number of transistors, the CK speed has been reduced of a factor 2

Risposta corretta.
La risposta corretta è: The number of transistors doubles every two years

Commenta o inserisci punteggio a mano

Domanda 7
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

1. A flash memory cell consists in:

- (a) one FAMOS ✓
- (b) one MOS and one capacitor Cs
- (c) one FAMOS and one capacitor Cs
- (d) one NMOS, one PMOS and two capacitors

Risposta corretta.
La risposta corretta è: one FAMOS

Commenta o inserisci punteggio a mano

Storico delle risposte

Passo	Data/Ora	Azione	Stato	Punteggio
1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: one FAMOS	Risposta salvata	
3	30/06/2020 13:09	Tentativo terminato	Risposta corretta	1,0

Domanda 8
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

A LUT with four inputs consists in:

- (a) 16 SRAM cells and one MUX ✓
- (b) 8 SRAM cells and two MUX
- (c) 2 DRAM cells and 2 MUX
- (d) 4 FAMOS

Risposta corretta.
La risposta corretta è: 16 SRAM cells and one MUX

Commenta o inserisci punteggio a mano

Storico delle risposte

Passo	Data/Ora	Azione	Stato	Punteggio
1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: 16 SRAM cells and one MUX	Risposta salvata	
3	30/06/2020 13:09	Tentativo terminato	Risposta corretta	1,0

Domanda 9
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

One logic gate with output resistance Ro is driving 6 inverters with input capacitance Ci=5pF. The propagation delay of a L → H transitions is:

- (a) 4.14·Ro·Ci ✓
- (b) 0.69·Ro·Ci
- (c) Ro·Ci
- (d) 0.41·Ro·Ci

Risposta corretta.
La risposta corretta è: 4.14·Ro·Ci

Commenta o inserisci punteggio a mano

Storico delle risposte

Passo	Data/Ora	Azione	Stato	Punteggio
1	30/06/2020 11:02	Iniziato	Risposta non ancora data	
2	30/06/2020 13:09	Salvato: 4.14·Ro·Ci	Risposta salvata	
3	30/06/2020 13:09	Tentativo terminato	Risposta corretta	1,0

Domanda 10
Risposta corretta
Punteggio ottenuto 1,0 su 1,0
Modifica domanda

The maximum speed of a 8 bit DRAM DDR3 module with bus clock at 1000 MHz is:

- (a) 16 Gbit/s ✓
- (b) 8 Gbit/s
- (c) 8 Mbit/s
- (d) 16 Mbit/s

Risposta corretta.
La risposta corretta è: 16 Gbit/s

Commenta o inserisci punteggio a mano

Problems

Problem 1

Consider 8 input channels with analog signals with bandwidth up to 30kHz. The input voltage of each channel is in the range between -0.5V and +0.5V. The signals are converted with an A/D conversion system using only one S/H and Successive Approximation ADC with dynamics 0-10V. The S/H acquisition time is 500ns and the MUX introduces a delay of 30ns.

Request 1: List the building blocks of the entire acquisition system, describe the role of each block and specify the bandwidth of the anti-aliasing filters.

Request 2: Calculate the minimum number of bits of the ADC to have 1LSB of less than 10mV

Request 3: Each input signal must be sampled at a frequency of 100kHz. Calculate the CK frequency of the SAR.

Solution

a) List the building blocks of the entire acquisition system, describe the role of each block and specify the bandwidth of the anti-aliasing filters. Filter bandwidth is 30kHz.

b) Calculate the minimum number of bits of the ADC to have 1LSB of less than 10mV

10 bit implies 10/(2^10)*1000=9.76 mV è N=10

c) Each input signal must be sampled at a frequency of 100kHz. Calculate the CK frequency of the SAR.

Sampling frequency at SH is 800kHz. è Ts=1/(800kHz)=1250ns.

Ts=Tacq+Tmux+Tc è Tc=1250-500-30=720ns = NTck è Tck=720/10=7.2ns => fck=1/7.2ns=13.89MHz

Problem 2

A track on PCB is 30 cm long and connects a driver to several slots (receivers) distributed along the line. The track (without connected load) has characteristic impedance Z_{∞}=65 Ω and the propagation speed is 0.65c. The capacitive load of the receivers increases the capacitance per unit length of the line of a factor of 3.5. The driver voltage supply is Vdd=3.3V. Electrical parameters of the receivers are: Vih=2.2V; Vil=1.4V; Iih,Iil=100nA.

Request 1: Calculate the characteristic impedance and the propagation delay t_p including the effect of the loads.

Request 2: Calculate the output resistance of the driver, to drive the receiver in IWS (incident wave switching) mode and noise margin 0.6V

Request 3: If the transmission line is terminated with a resistance RT=200 Ω, calculate the voltage at the far-end at t=2tp and the voltage at the near end at t=3tp.

1) Zinf'=65/sqrt(3.5)=34.75 ohm
t'p=L/u u'=u/(sqrt(3.5)) t'p=L/(0.65c)*sqrt(3.5)=2.88ns

2) Vdd*Zinf'/(Zinf'+Ro)=vih+NM=2.8 V ==>> Zinf'*3.3/2.8-Zinf'=Ro ==> Ro=6.2 ohm

3) If Rt=200ohm ==> Far end: GammaT=(Rt-Zinf')/(Rt+Zinf')=0.7 Vc(tp)=2.8*(1+0.7)=4.76
Near end: GammaB=-0.7
Vb(2tp)=2.8+2.8*0.7+2.8*0.7*(-0.7)=3.39 V

Vc(2tp)=Vc(tp) and Vb(3tp)=Vb(2tp)

Problem 3

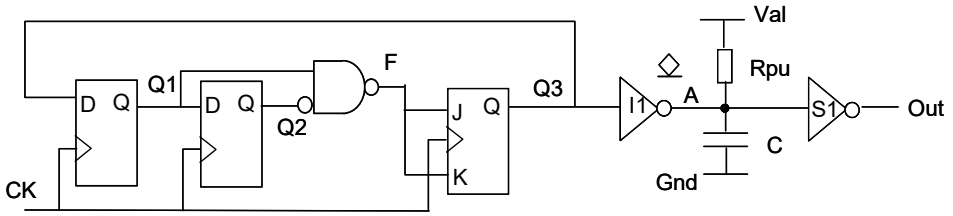
Consider the sequential circuit shown in the figure and assume that the outputs Q1, Q2 and Q3 are initially all reset to 0 logic state. Consider the capacitor C=0.

The delays for all the components are reported below:

Tsu = 3 ns, Th = 2 ns (D-FF and JK FF) ;

T*ck->Q* = 5 ns (D-FF and JK FF)

NAND gate and inverters I1 and S1: T_{LH} = 3ns, T_{HL} = 4 ns,



Answer the following questions:

Request 1:

- How many CK active edges are needed to switch Q1 to logic state 1?

- Which is the initial state of the output A

- How many CK active edges are necessary to switch the output of S1 to state 1 ?

Request 2:

Assuming C=0, calculate the maximum CK frequency.

Request 3:

Calculate the propagation delay for a transition LèH of the state at node A. Assume: C=5pF, the input capacitance of S1 equal to Ci=4pF, Rpu=1kohm and the output resistance of I1 equal to Ro=100 ohm (when output of I1 is in low state);

Problem 3: solutions

1

- How many CK active edges are needed to switch Q1 to logic state 1? **2**
- Which is the initial state of the output A? **high state**
- How many CK active edges are necessary to switch the output of S1 to state 1 ? **first CK edge**

2:

Assuming C=0, calculate the maximum CK frequency.

Tckmin=tck_>Q+tdnand+tsu=12 ns fckmax=83.3MHz

3:

tdLH=0.69*(Ci+C)*1kohm=6.21 ns

Problem 4

A DRAM memory has the following characteristics:

- 16 bit address: 12 bits are for row address and 4 bits are for column address.

- words are of 8 bits

- pass transistors with Cd=0.5fF

1:

Calculate the number of Word lines

2:

Calculate the total number of memory cells

3:

Calculate the capacitance of the bit line C_{BL}

1. #word lines = # of rows=2^12=4096

2. # memory cells= 2^12*2^4*8= 524288

3. CbL=2^12*0.5fF=2.05 pF