Politecnico di Torino
Written exam- 4th July 2023 Applied Electronics (AY 22-23)

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Part -A – Quiz
(report with X the correct answer in the grid below – do not write in the row "total")

QUIZ	1	2	3	4	5	6	7	8	9	10	
Answer a											
Answer b											
Answer c											
Answer d											
Total points											

Quiz A.1
Assuming that the delay of a combination logic block of a sequential circuit is Tcl, choose the correct expression for the minimum CK period of the sequential circuit:

a) (Tck➔Q) +Thold
b) (Tck➔Q)+Tset-up+Thold
c) (Tck➔Q)+Tset-up+max(Tcl)
d) (Tck➔Q)+Tset-up+min(Tcl)

Quiz A.2
An SRAM bit cell is composed of

a) a floating gate transistor
b) six MOS transistors
c) an nMOS and a pMOS
d) a MOS transistor and a capacitor

Quiz A.3
Consider two CMOS digital circuits with, in average per time instant, about 1E6 and 1E8 MOS transistors in OFF state respectively. Choose the correct sentence:

a) The static power consumption is always zero
b) The circuit with 1E6 MOS has a higher static power consumption respect to the one with 1E8 MOS
c) **The static power consumption of the circuit with 1E6 MOS is about one hundred times smaller than the circuit with 1E8 MOS**
d) The static power consumption is the same in both circuits.

Quiz A.4
Consider a JK-FF. Select the correct sentence:

a) Inputs J and K must be always 1 during the set-up time.
b) The output Q toggles at each CK trigger when J=K=1 provided that the set-up constrain is satisfied
e) During the set-up time K can change
f) During the set-up time J and K can change no more than 2 times

Quiz A.5
A Look-Up Table (LUT) with 4 inputs and 1 output:

a) can implement a logic function of 16 variables
b) it contains 4 memory cells
c) can implement a logic function of 4 variables
d) it contains 8 memory cells

Quiz A.6
In Non-Blocking assignment in a Verilog always block

a) the signal is immediately assigned a value when the statement is executed
b) the signal is given a future value, which is assigned later
c) the signal is immediately assigned a value if it is of type wire
d) the signal is immediately assigned a value if it is in the sensitivity list

Quiz A.7
Asynchronous serial protocol: the number of information bits that can be transmitted between the start and stop bit is:

a) Infinite (there is no limit to the number of bits that can be transmitted)
b) One (only one bit can be transmitted)
c) Limited to a few bits depending on how often the CK needs to be resynchronized.
d) Always 8 bits

Quiz A.8
Consider a full-wave rectifier, the ripple voltage is proportional to the wave period T as:

a) T
b) T/4
c) 2T
d) T/2

Quiz A.9
Consider a buck voltage regulator with input voltage varying between 6V and 12V; the output voltage is 3V. Calculate the range of the required regulation of the duty-cycle:
:

a) **between 25% and 50%**
b) between 50% and 75%
c) between 12.5 % and 25%
d) duty cycle must stay at 50% constant

Quiz A.10
Consider a driver that drives a transmission line with N receivers connected to the line. The connected receivers increase the capacitance per unit of length of line of a factor 16 respect to the capacitance per unit of length of the unloaded line. Choose the correct sentence:

a) The propagation time tp is increased of a factor 3
b) The propagation time tp is decreased of a factor 16
c) The characteristic impedance of the line is reduced of a factor 4
d) The propagation speed is increased of a factor 4.

Part -B – Problem B.1

Consider 6 input channels with analog signals with bandwidth up to 15kHz. The input voltage of each channel is in the range between +0.5V and +1.5V. The signals are converted with an A/D conversion system using only one S/H and Successive Approximation ADC with dynamics -5 to +5V. The MUX introduces a delay of 40ns, and the acquisition time of the S/H is 450 ns.

1) List the building blocks of the entire acquisition system, describe the role of each block, specify the bandwidth of the anti-aliasing filters. Design the condition amplifier by reporting the output voltage versus the input voltage and the circuit.

$A_V = 10 \quad V_{OFF} = -10V$

2) Calculate the minimum number of bits of the ADC to have 1LSB of less than 5mV.

$N = 11$

3) Choose the minimum CK frequency of the SAR to sample the input signals with oversampling factor of 5 and calculate the conversion time of the ADC.

$T_{s\,S/H} = T_C + T_{HOLD} + T_{ACQ} = \frac{1}{6 \cdot 30kHz \cdot 5} = 1111ns$

$T_C = 1111ns - 40ns - 450ns = 621ns$

$T_C = N T_{CK} \Rightarrow f_{CK} = \frac{1}{T_{CK}} = \frac{N}{T_C} = 17.7MHz$

Time the ADC is $T_C = 621ns$

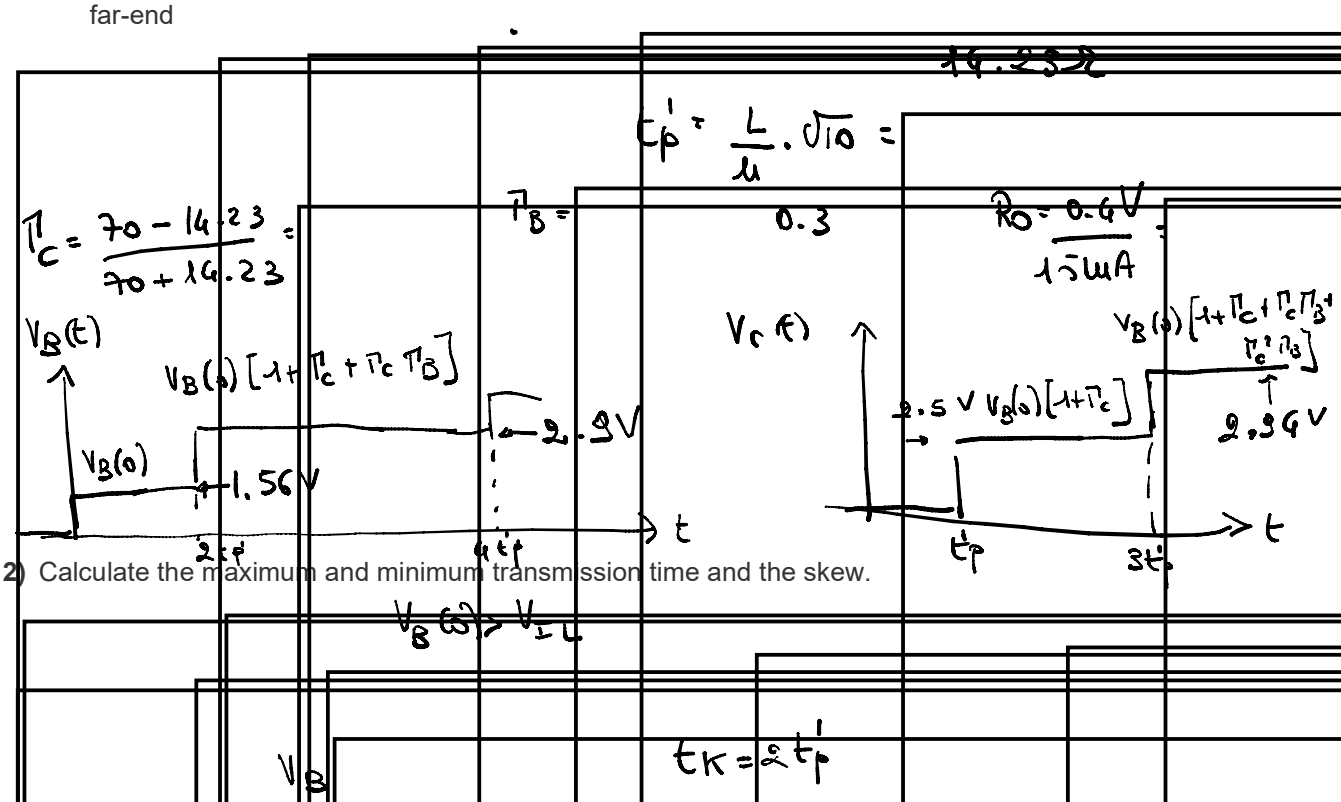
Part-B – Problem B.2

A track of 50cm on a PCB backplane has characteristic impedance Z_∞= 45Ω, and wave propagation speed u = 0,6c. N=15 receivers are equally distributed increasing the capacitance per unit of length of the line of a factor 10. The line is terminated with a termination Rt=70 Ω. The driver and receivers have the following electrical parameters:

Driver: Voh = 4.1 V, Vol = 0.4 V, Ioh=Iol=15mA Vdd=4.5V.

Receivers: Vih = 2.4 V, Vil = 1.2 V;

1) Plot the voltage (indicating the voltage values) versus time for 0≤t≤3tp at the near-end and at the far-end

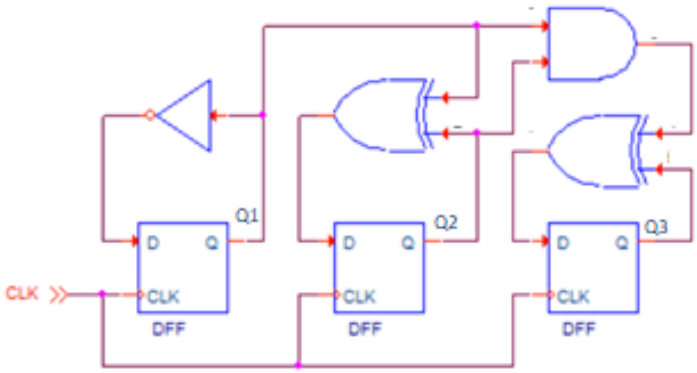


2) Calculate the maximum and minimum transmission time and the skew.

3) Consider an asynchronous write cycle and the parameters of point (2). Answer the following questions assuming that the receiver registers have set-up time of 5 ns and hold time of 1ns.

- Calculate the delay between INF and STB at source
- Calculate the delay between STB and ACK at destination
- Calculate the delay between STB and CK at destination
- Calculate the time duration STB must stay high at source

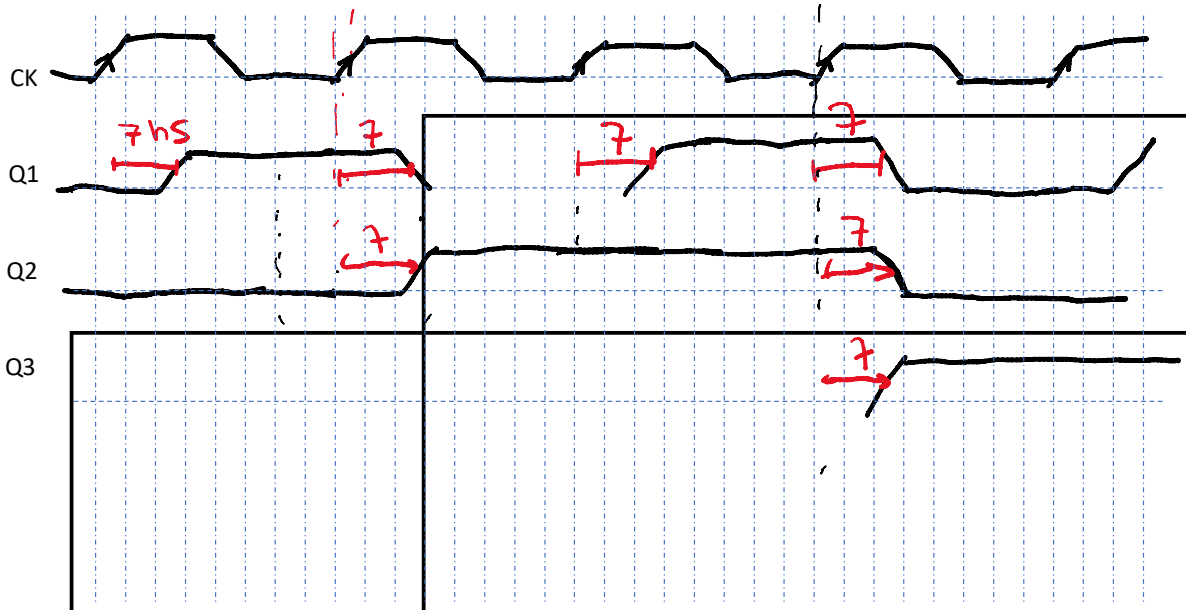
Parte B – Problem B.3



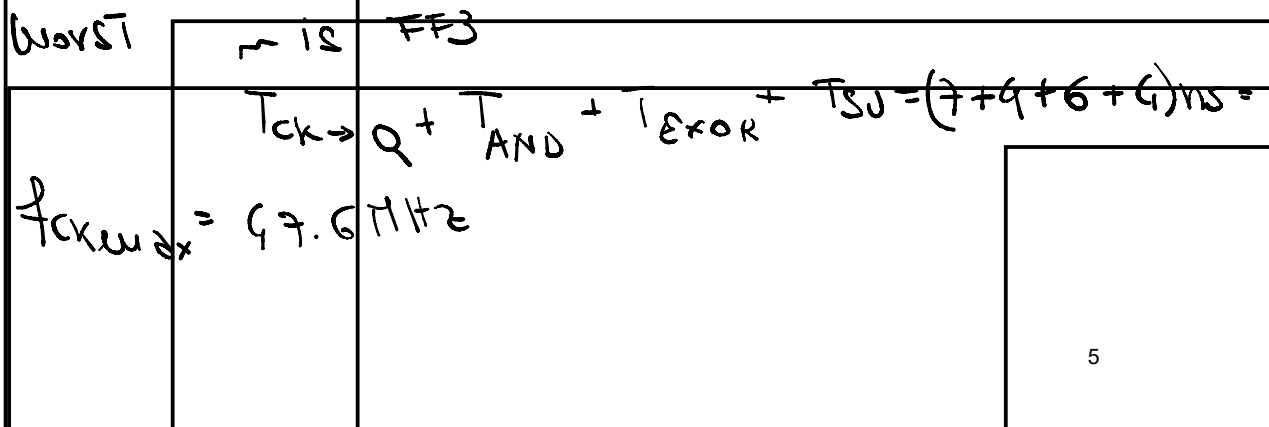
Consider the sequential circuit shown in the figure; all outputs Q are initially set to Q=0.

1) Plot the timing diagram of the outputs Q1, Q2, and Q3 for the number of CK cycles necessary to observe the transition L➔H of Q3. **Consider the delays that follows and report the delays on the timing diagram:**

All FFs: Tck➔Q=7ns Tset-up=4ns Thold=1ns
AND gate: THL=TLH=4 ns
EXOR gate THL=TLH=6ns
NOT gate THL=TLH=2 ns



2) Calculate the maximum CK frequency.



Part-B –Problem B.4

You are given a DRAM memory with 10 bits used for row decoding and 6 bits used for column decoding, with each word of 8 bits. Pass transistors have a drain capacitance of Cd = 0.1fF and the voltage supply is Vdd = 1.2V.

1) Compute the size in bytes of the memory, the number of bitlines, the number of pass transistors connected to each bit line, and the total number of pass transistors in the memory.

2) Compute the minimum storage capacitance Cbit in a bit cell in order to use a sense amplifier with a sensitivity of 100mV.

MemSize = 2^(10+6) = 2^16 = 65536 bytes = 64 Kbytes

*Nbitlines = 8 * 2^6 = 8 * 64 = 512*

Npt/bitline = 2^10 = 1024

*Npt = Npt/bitline * Nbitlines = 1024 * 512 = 524288*

*CL = Npt/bitline * Cd = 1024 * 0.1fF = 102.4fF*

*Qbit = Vbit * Cbit (where Vbit=0 when 0 is stored, Vbit=Vdd=1.2V when 1 is stored)*

*QL = CL * Vdd/2*

Qtot = Qbit + QL = VL(Cbit + CL)

*==> VL = Vbit * Cbit/(Cbit + CL) + Vdd/2 * CL/(Cbit + CL)*

*DeltaV = VL - Vdd/2 = |Vbit - Vdd/2| * Cbit/(Cbit + CL) > 100mV*

*==> Cbit > CL * DeltaV / (|Vbit - Vdd/2| - DeltaV) = 102.4fF * 0.2 = 20.48fF*

(the problem is simmetric, if Vbit=0 or Vbit=Vdd the result is the same. We assume Vth is negligible)

OPTIONAL QUESTIONS on EXPERIMENTAL LAB PART (for students attending a.y. 2022/2022)

Question 1:

Consider the 4 bits asynchronous counter CD4040 tested during the LAB1. Answer the following questions:

- How have you got the CK to provide to the counter?
- What have you observed when comparing the clock frequency with that of the different outputs of the counter (outputs are Qi with Q4 corresponding to the MSB and Q1 to the LSB).
- What have you observed when measuring the delays between the CK trigger and the variation of the logic state at different outputs Qi

Question 2:

Explain how starting from the 4 bit weighted resistor DAC mounted in LAB 3, you can mount a tracking ADC. List what are the components used and why.

Question 3:

Consider the RG58 coaxial cable employed in LAB2. Plot the voltage measured at near end and at the far-end when the cable has been terminated with an open circuit termination. Assume the input signal is a square wave.
Explain and motivate your plots.

OPTIONAL QUESTIONS on VIRTUAL LAB PART (for students attending a.y. 2020/2021 or a.y. 2019/2020)

Question 1: Analog-to-digital and Digital-to-Analog converters

List the components needed in the LTspice software to realise and simulate a DAC circuit analogous to the one considered during the virtual LAB?

Question 2: Logic gates and simple sequential logic circuits:

How could you check in LTspice software the correct operation of a counter such as the 4-bit CD4029 used during the virtual LAB?

Question 3: Transmission lines:

How do you simulate and characterize in LTspice software the effect of a capacitive load connected at the far end of a transmission line with matched termination? What do you expect to observe at the near end? Consider L to H transition.