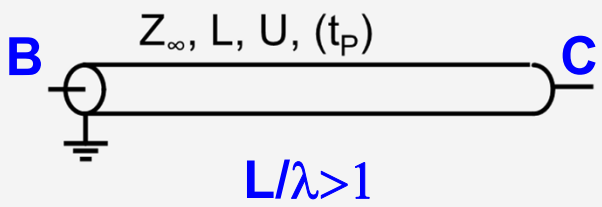
APPLIED ELECTONICS

Part C:

Class exercises 2 with solutions on:

- **Transmission lines**



Parameters

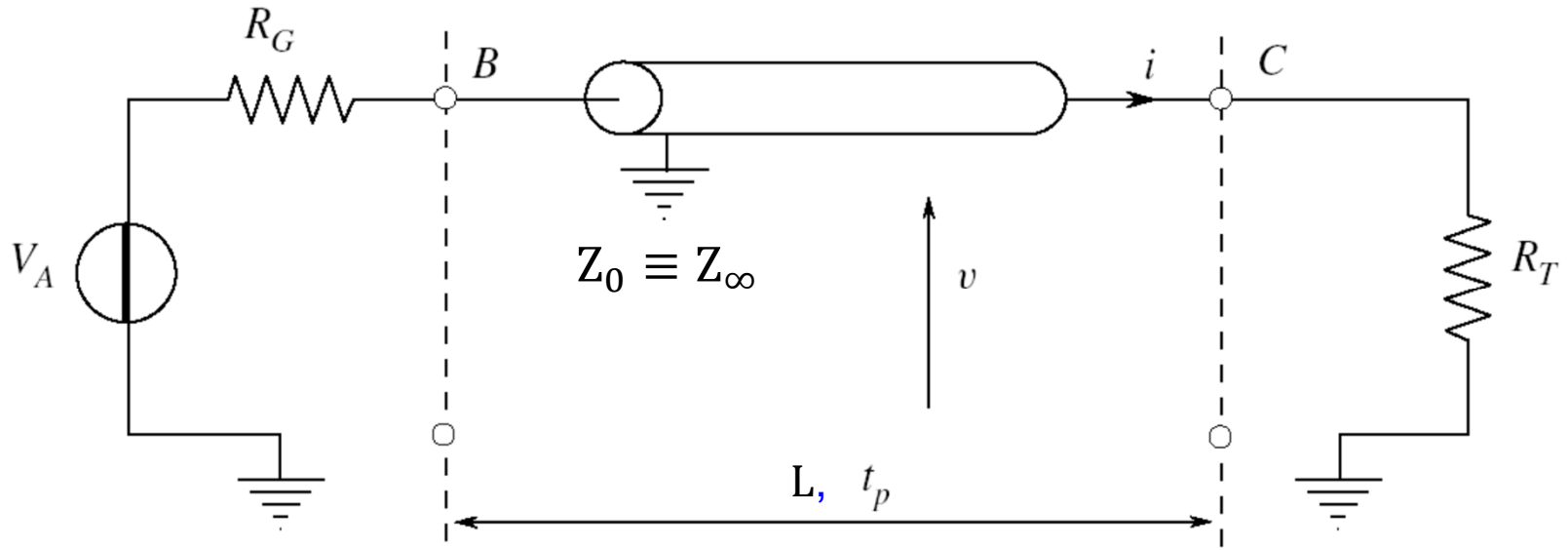
Z_∞: characteristic impedance,
L: length,
U: propagation speed
t_P: propagation time

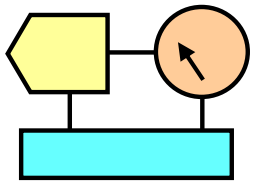
Problem 1 - Assignment
Lattice diagram

a) Use lattice diagram to plot the voltage at the receiver $V_C(t)$ and at the driver $V_B(t)$ in a (0 - 4 t_p) time range for L → H transition with V_A from $0\ V$ to $5\ V$ and:

$$R_G = 50\ \Omega,\ R_T = \infty,\ Z_\infty = 50\ \Omega,\ U = 0.8\ c,\ L = 20\ cm$$

b) Repeat the calculation with $R_G = 270\ \Omega$ and $R_G = 15\ \Omega$





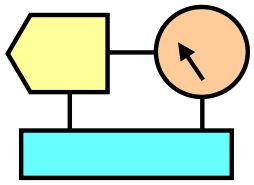
Problem 2 – Assignment
Incident Wave Switching

a) Calculate the driver output resistance (R_O) for IWS driving for a connection with:

   L → H transition with $V_A = 0\,V \rightarrow 4\,V$
   Receiver threshold $V_T = 2.5\,V$
   Z_∞= 70 Ω and open circuit termination

b) Explain why this configuration can give multiple transition for a receiver placed at the far-end. Indicate how multiple transitions can be eliminated

c) Draw qualitatively the voltage $V_C(t)$ in the case a capacitor C_L is connected at the far end.



Problem 3 – Assignment

Transmission times and total skew time

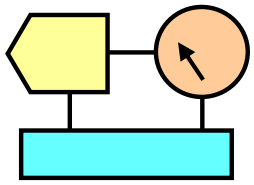
Consider a backplane with $L_U = 8\ nH/cm$, $Z_\infty = 85\ \Omega$ (without capacitive load), length $L = 48\ cm$, open circuit termination, and 24 connectors. Each board that can be inserted in the connectors has an input capacitance of $35\ pF$. The system can have from 2 to 24 connected boards.
Driver/receiver CMOS: $V_{DD} = 3.3\ V;\ R_O = 95\ \Omega;\ V_{IH} = 2\ V, V_{IL} = 1\ V.$

a) Calculate t_p in the cases of 2 and 24 connected boards.

b) Calculate t_{TXmin} and t_{TXmax} for 2 connected boards in the two extremes of the line

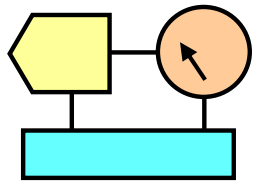
c) Calculate t_{TXmin} and t_{TXmax} with 24 connected boards

d) Calculate the maximum R_{OH} to drive the line in IWS mode in the case of 24 inserted boards



Problem 4 - Assignment

A track on a PCB backplane has characteristic impedance $Z_0 = 95\ \Omega$ (with no load), wave propagation speed $U = 0.65\ c$. The track length is $L = 30\ cm$, without terminations, and 15 equally spaced devices are connected to the track. The total capacitive load of these devices increases the distributed track capacitance (towards GND) by a factor 20 (loaded unity capacitance = unloaded capacitance $x\ 20$).
The interface uses CMOS circuits, with power supply $5\ V$, and the following parameters: $V_{OH} = 4\ V, I_{OH} = -16\ mA, V_{OL} = 0.8\ V, I_{OL} = 16\ mA, V_{IH} = 2.7\ V, V_{IL} = 1.3\ V$.
Further assumptions: the PCB tracks can be considered lossless transmission lines, and linear equivalent circuits can be used for drivers and receivers.

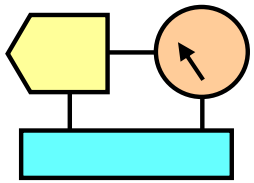


Problem 4 - Assignment

a) Find the characteristic impedance Z_0' and the propagation speed U' of the loaded track, and evaluate the propagation time t_P over the full length of the connection, for a fully loaded track.
(propagation speed $U = 1/\sqrt{L_U C_U}$)

b) Find the equivalent output resistance of drivers, for H and L states (respectively R_{OH} and R_{OL}), and find the minimum and maximum transmission times t_{TXmin} and t_{TXmax} from a driver placed at one end and a receiver placed at any position along the connection, for fully loaded track without termination in case of L→H transition.

c) Evaluate the equivalent driver output resistance R'_{OH} required to operate a receiver connected at any intermediate point of the track in IWS (Incident Wave Switching) for the L → H transition, with $NM = 100\ mV$, and line driven from one end.
Using drivers with equivalent output resistance R'_{OH}, what should be connected at the opposite end to guarantee correct operation?



Problem 4 - Assignment

d) Draw the Information and Control signals (INF, STB) at Driver and at Receiver, and the destination register clock CK for a **synchronous** write cycle and evaluate cycle duration with the following parameters.
- Interconnection: $t_K = 25\ ns, t_{TXmin} = 20\ ns$
- Receiver register: $t_{SU} = 10\ ns, t_H = 5\ ns$

e) Draw the Information and Control signals (INF, STB, ACK) at Driver and at Receiver, and the destination register clock CK for an **asynchronous** transfer cycle and evaluate cycle duration with the following parameters.
- Interconnection: $t_K = 25\ ns, t_{TXmin} = 20\ ns$
- Receiver register: $t_{SU} = 10\ ns, t_H = 5\ ns$