Cominational Logic 1

Consider the combinational logic function: **Out= not(A or (B and C))** which has to be realized with CMOS technology.

Request 1)

Answer the following questions:

1.a: How many NMOS are needed?

1.b how many NMOS must be connected in series?

1.c how many PMOS are needed?

1.d homw many PMOS muct be connected in paraller?

Request 2)

Using MOS with R_{on}=70Ω, calculate the maximum delay for H-L and L-H transition to drive 5 gates with input capacitance Ci=5pF each.

Transmission Lines 1

A track of 20cm on a PCB backplane has characteristic impedance Z_∞ = 120Ω (with no load), and wave propagation speed u = 0,65 c. We need to connect to the track N equally spaced receivers. Each device has an input capacitance of 2pF. The line is driven on one side and closed with a matched termination on the other side.

The driver/receivers have the following electrical parameters:

Voh = 4.1 V, Ioh = -10 mA, Vol = 0,4 V, Iol = 10 mA, Vih = 2,5 V, Vil = 1,0 V; Vcc=4.5V.

Request 1)

Calculate the capacitance per unit length of the line without any connected device.

Request 2)

Calculate the minimum characteristic impedance Z_∞ to drive the line in IWS with noise margin NM=0.4V.

Request 3)

Using the result of Request (2), calculate the maximum number N of receivers that can be connected to the track.

Transmission Lines 2

A track on PCB is 30 cm long and connects a driver to several slots (receivers) distributed along the line. The track (without connected load) has characteristic impedance Z_∞=65 Ω and the propagation speed is 0.65c. The capacitive load of the receivers increases the capacitance per unit length of the line of a factor of 3.5. The driver voltage supply is Vdd=3.3V. Electrical parameters of the receivers are: Vih=2.2V; Vil=1.4V; Iih,Iil=100nA.

Request 1: Calculate the characteristic impedance and the propagation delay t_p including the effect of the loads.

Request 2: Calculate the output resistance of the driver, to drive the receiver in IWS (incident wave switching) mode and noise margin 0.6V

Request 3: If the transmission line is terminated with a resistance RT=200 Ω, calculate the voltage at the far-end at t=2tp and the voltage at the near end at t=3tp.

Transmission Lines 3

A track of 20cm on a PCB backplane has characteristic impedance Z_∞ = 120Ω (with no load), and wave propagation speed u = 0,65 c. We need to connect to the line N=7 equally spaced receivers. The line with the capacitive loads has a characteristic impedance Z'_∞ =72.5 Ω. The line is driven on one side and closed with a matched termination on the other side.

The receivers have the following electrical parameters:

Vih = 2,5 V, Vil = 1,0 V; V_{DD}=4.5V.

Request 1)

Calculate the trasmission time tp' of the line including the effect of the reciever loads

Request 2)

Calculate the output resistance of the driver to drive the line in IWS with noise margin NM=0.2V.

Request 3)

Considering the loaded line, calculate the maximum and minimum trasmission time and the skew tk.

Transmission Lines 4

A track of 30cm on a PCB backplane has characteristic impedance Z_∞ = 90Ω (with no load), and wave propagation speed u = 0,6 c. We need to connect to the track N=10 equally spaced receivers. Each device has an input capacitance of 1pF. The line is driven on one side and closed with a matched termination on the other side.

The driver and receivers have the following electrical parameters:

Voh = 4.1 V, Vol = 0,4 V, Vih = 2,5 V, Vil = 1,0 V; Vdd=4.5V.

Request 1)

Calculate the capacitance per unit length of the line without any connected device.

Request 2)

Calculate the characteristic impedance of the line with the connected receivers

Request 3)

Calculate the output resistance of the driver to drive the line in IWS mode and NM=0.5V. Include in the calculation the effect of the capacitive load.

Memories DRAM-1

A DRAM memory has the following characteristics:

- 16 bit address: 12 bits are for row address and 4 bits are for column address.

- words are of 8 bits

- pass transistors with Cd=0.5fF

Request 1:

Calculate the number of Word lines

Request 2:

Calculate the total number of memory cells

Request 3:

Calculate the capacitance of the bit line C_{BL}

Transmission lines RWS

One driver with Vdd=3,3 V is connected on one side of a transmission line with Z_∞ = 60 Ω, propagation speed U = 0,7 C, length 15 cm and open circuit termination. The receivers are CMOS circuits with Vil = 1V, Vih = 2,2 V. Answer the following questions for a L->H transition:

Request 1:

Calculate the range of values of the output resistance of the driver (Ro) to drive the line in Reflective Wave Switching (RWS) mode and not in Incident Wave Switching mode, when only one receiver is connected at the near-end of the line.

Request 2:

With Ro = 80 Ω, calculate the maximum and minimum transmission times and the skew for a receiver connected in the near-end and a receiver connected in the far-end.

Request 3:

This interconnection is used for a parallel synchronous write bus protocol. The receiver registers have set-up time Tsu = 5 ns and hold time Th = 2 ns. Calculate the delay between the DATA and STB signals and the duration of the write cycle.

Sense amplifiers

Consider a DRAM memory with 11 bit address: 8 bits are used for row decoder and 3 bits are used for column decoder. Each word is 8 bit. The pass transistors have drain parassitic capacitance Cd=0,2fF and threshold voltage Vth=0,2V; voltage supply is Vdd=2V. Answer to the following questions:

Request 1:

Calculate

- the number of bit lines

- the number of pass transistors connected to one bit line

- the total number of pass transistors of the memory.

Request 2:

Calculate the minimum value of the storage capacitor Cs, if the sense amplifier can sense a minimum voltage level of 50mV.

Sense amplifiers 2

Consider a DRAM memory with 8 bit address; all bits are used for row decoder. Each word is 8 bit. The pass transistors have drain parassitic capacitance Cd=0,4fF and threshold voltage Vth=0,2V; voltage supply is Vdd=2V. Answer to the following questions:

Request 1:

Calculate

- the number of bit lines

- the number of pass transistors connected to one bit line

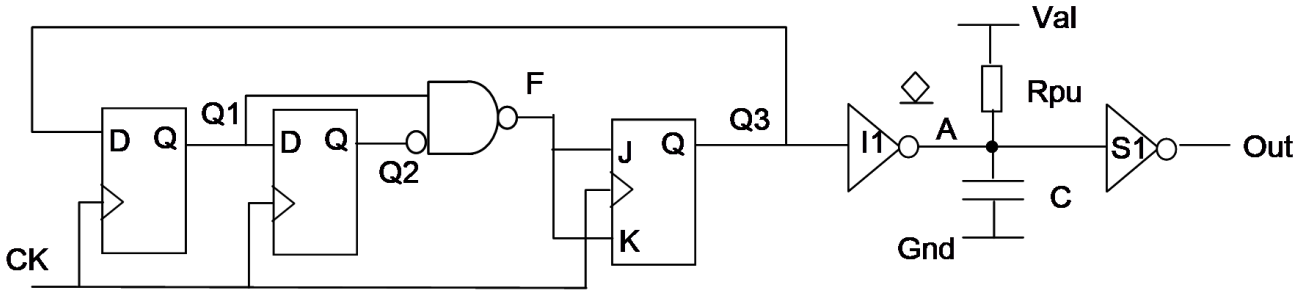
- the total number of pass transistors of the memory.

Request 2:

Calculate the minimum value of the storage capacitor Cs, if the sense amplifier can sense a minimum voltage level of 30mV.

Sequential circuit 2

Consider the sequential circuit shown in the figure and assume that the outputs Q1, Q2 and Q3 are initially all reset to 0 logic state. Consider the capacitor C=0.



The delays for all the components are reported below:

Tsu = 3 ns, Th = 2 ns (D-FF and JK FF) ;

T*ck->Q* = 5 ns (D-FF and JK FF)

NAND gate and inverters I1 and S1: T_{LH} = 3ns, T_{HL} = 4 ns,

Answer the following questions:

Request 1:

- How many CK active edges are needed to switch Q1 to logic state 1?

- Which is the initial state of the output A

- How many CK active edges are necessary to switch the output of S1 to state 1 ?

Request 2:

Assuming C=0, calculate the maximum CK frequency.

Request 3:

Calculate the propagation delay for a transition L➔H of the state at node A. Assume: C=5pF, the input capacitance of S1 equal to Ci=4pF, Rpu=1kohm and the output resistance of I1 equal to Ro=100 ohm (when output of I1 is in low state);

Sequential Circuit 3

Consider the sequential circuit shown in the figure. All outputs Q are initially reset to zero. The block *f* is a combinational logic block with function F = not(Q1· not(Q2)) . Assume C=0;

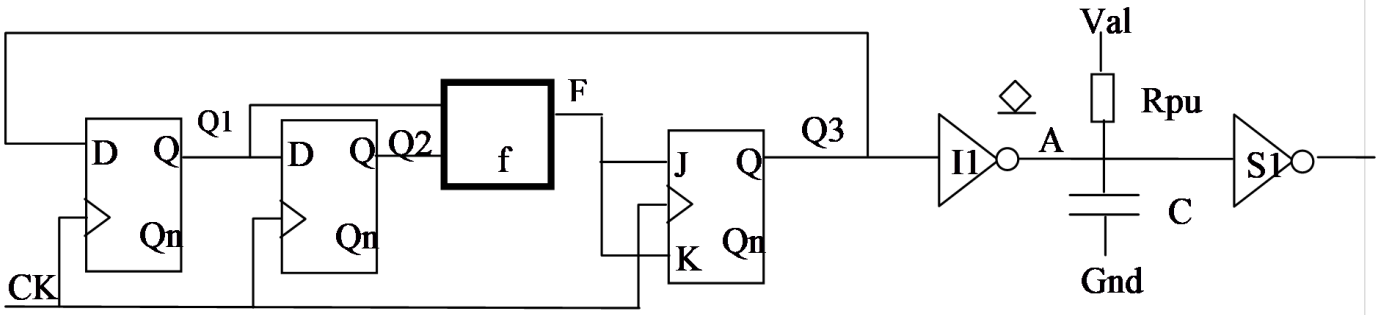
Dynamics parameters are:

FF D: T*ck->Q* =5 ns, Tsu = 4ns;

FF JK : T*ck->Q* = 7ns, Tsu = 6ns;

combinational logic block *f* : TLH*f* = 3ns , THL*f* = 6 ns;

inverters I1 and S1: TLH=4 ns; THL=2ns



Request 1:

Answer the following questions assuming the CK period is 60ns:

- which are the inital states of F, A and Out?

- how many CK rising edges are necessary to switch Q3 to high state?

- calculate the delay between a transition L->H of Q3 and the switch of Q1 to High

- calculate the delay between a transition L->H of Q3 and the switch of F to Low

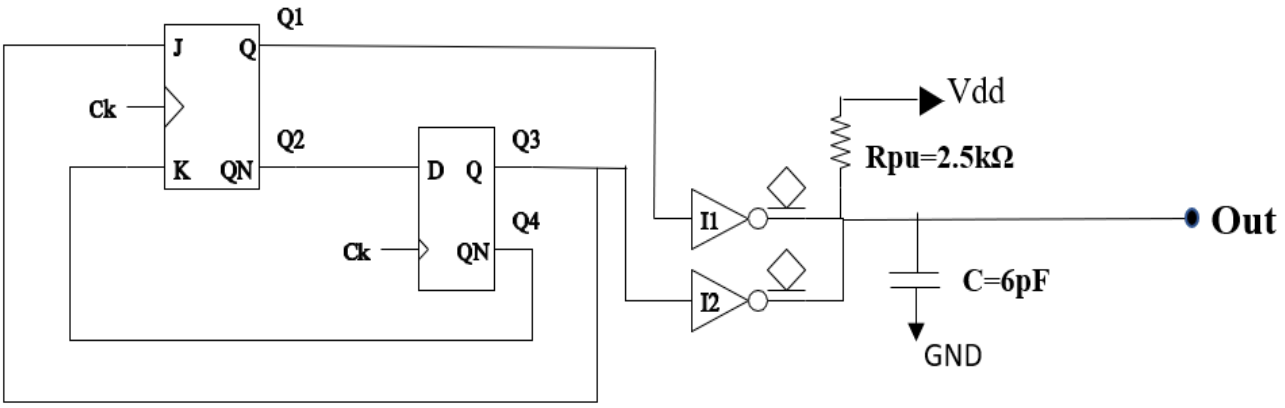
- calculate the delay between a switch L->H of Q3 and the switch of the state OUT

Request 2:

Calculate the maximum CK frequency

Sequential Circuit 4

Consider the sequential circuit shown in the figure. All outputs Q are initially reset to zero.



Request 1:

The inverters I1 and I2 have output resistance R_{OL}=60 Ω. Calculate the maximum and minimum delay for L to H ($T_{LH,max}$ and $T_{LH,min}$) and for H to L transition ($T_{HL,max}$ and $T_{HL,min}$) of the output voltage (Vout) on the capacitor C.

Request 2:

Assuming the following dynamic parameters for the FFs and the delays calculated in Request 1

FF D: T*ck->Q* =5 ns, Tsu = 4ns;

FF JK : T*ck->Q* = 7ns, Tsu = 6ns;

Answer the following questions assuming the CK period is 60ns:

- which are the inital states of Q1, Q2 and Q4?

- which is the state of the voltage on the capacitor (Vout) if Q1=1 and Q3=1

- how many CK rising edges are necessary to switch Q3 to high state?

- calculate the delay between a transition L->H of Q2 and the correspoding variation of the state of the voltage on the capacitor

Request 2:

Calculate the maximum CK frequency

Data Acquisition System 4 Channels

We have 4 analog input channels with voltage in the range between -0.5V and +0.5V. The maximum frequencies of the channels are $F_{max,1}$ = 3 kHz, $F_{max,2}$ = 2,5 kHz, $F_{max,3}$ = 1 kHz, $F_{max,4}$ = 2 kHz. The acquisition system uses only one S/H and only one tracking ADC with input dynamic range [0, +10 V]. The channels are oversampled with oversampling factor of 2.5.

Request 1:

List the various blocks of the acquisition system and define the role of each block. Indicate the relation V_{out} versus V_{in} of the conditioning amplifier .

Request 2:

Calculate the sampling frequency of the S/H

Request 3:

The ADC operates in overload condition; if the maximum ADC conversion time must be Tc=8.5 μs, calculate the number of bits assumin that the clock frequency 250 MHz.

Request 4:

With the number of bits of previous point, calculate the SNRq for input sinusoidal signals

Data Acquisition System 6 channels

We have 6 analog input channels with voltage in the range between -2V and +2V. The maximum bandwith of the channels is 30kHz.

The acquisition system uses one S/H and one SAR ADC with input dynamic range [0, +10 V]. The channels are oversampled with oversampling factor of 3.

Request 1:

List the various blocks of the acquisition system and define the role of each block. Indicate the relation V_{out} versus V_{in} of the conditioning amplifier .

Request 2:

Calculate the sampling frequency of the S/H

Request 3:

Calculate the number of bits to convert the signals with precision of 0.5%.

Request 4:

Assuming the S/H has acquisition time of 250ns and the MUX intruduces a delay of 50ns , calculate the CK frequency o the SAR

Data Acquisition System 1

Consider 4 analog signals in the range between 0 and 4V and maximum frequency 50kHz. The signals are analog-to-digital converted in a conversion system with one S/H and one A/D. The A/D converter has input dynamics -5 to +5V. Answer the following questions:

Request 1)

List in the order from input to the output the blocks of the data acquisition system and specify if a conditioning amplifier is necessary

Request 2)

If a conditioning amplifier is necessary, plot the circuit and calculate the expression (as function og the resistors) of the output voltage versus the input voltage. For the plot use the pen tool (draw a picture tool) and draw with the mouse.

Request 3)

3.a: Choose the sampling frequency of the S/H to sample the channels with an oversampling factor of 3.

3.b: Choose a resonable value for the conversion time of the ADC and for the acquisition time of the S/H to satisfy point 3.a

Request 4)

Assuming the A/D is a successive approximation converter with following characteristics: DAC with settling time 80ns, SAR with $t_{pCK->Q}$ =10ns, voltage comparator with negligible delay. Calculate the maximum clock frequency

Data Acquisition Sytem 2

Consider 8 input channels with analog signals with bandwidth up to 30kHz. The input voltage of each channel is in the range between -0.5V and +0.5V. The signals are converted with an A/D conversion system using only one S/H and Successive Approximation ADC with dynamics 0-10V. The S/H acquisition time is 500ns and the MUX introduces a delay of 30ns.

Request 1: List the building blocks of the entire acquisition system, describe the role of each block and specify the bandwidth of the anti-aliasing filters.

Request 2: Calculate the minimum number of bits of the ADC to have 1LSB of less than 10mV

Request 3: Each input signal must be sampled at a frequency of 100kHz. Calculate the CK frequency of the SAR.

Data Acquisition System 3

Consider 4 input channels with analog signals with the following maximum frequency:

Fmax,1=30kHz Fmax,2=20kHz Fmax,3=15kHz Fmax,3=10kHz

The input voltage of each channel is in the range between -1.5V and +1.5V. The signals are converted with an A/D conversion system using only one S/H and Successive Approximation ADC with dynamics 0-10V. The S/H acquisition time is 500ns and the MUX introduces a delay of 30ns.

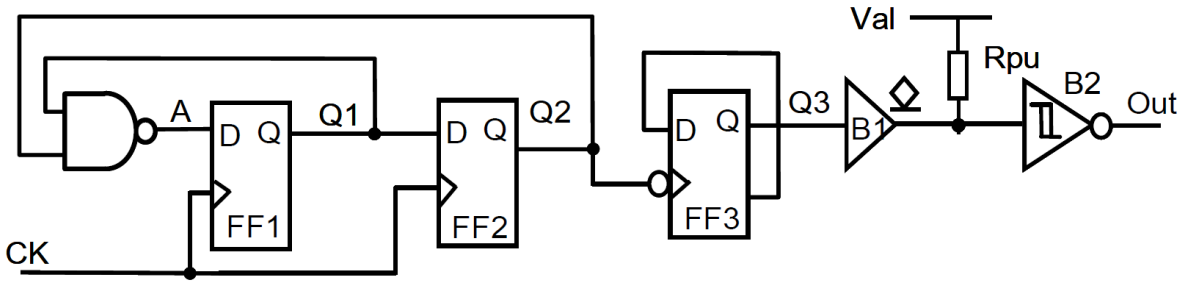
Request 1: List the building blocks of the entire acquisition system, describe the role of each block, specify the bandwidth of the anti-aliasing filters and the characteristic (ie: Vout =Av•Vin + V_{OFF}) of the conditioning amplifier. Av=? V_{OFF}=?

Request 2: Calculate the minimum number of bits of the ADC to have 1LSB of less than 5mV

Request 3: Each input signal must be sampled at a frequency of 100kHz. Calculate the CK frequency of the SAR.

Sequential Cicuit

Consider the circuit shown in the figure below. All outputs Q are initially reset to zero.



Dynamic parameters are:

D FF (FF1 and FF2): $T_{ck=>Q}$ =7 ns; D FF3 : $T_{ck=>Q}$ = 5ns

Hold time for all of the FF: Th=2ns; Set-up time for all FF is Tsu=6ns

Delays of NAND gate 3 ns for H-L and L-H transitions

Delay of B1: TdLH=5 ns TdHL=1ns

Dealy of B2: TdLH=TdHL=3ns

Request 1)

Assuming the CK period is 30 ns, all output Q initially set to low state, and C=0. Answer to the following questions considering the dynamic parameters given above::

- 1.a how many clock cycles are necessary to switch Q3 from L to H state?

- 1.b which is the delay between a transistion L->H of Q3 and the consequent transition of the Out?

- 1.c which is the delay between a transistion L->H of Q1 and the consequent transition of the Q2?

DO NOT PLOT THE TIMING DIAGRAM

Request 2)

With Rpu=10kΩ, gate B1 with R_{on}=200 Ω (when output is low) and input capacitance of B2 equal to Ci=5pF, calculate the delay for L-H transitions of the output of B1.

Request 3)

Calculate the maximum CK frequency when the components have the dynamic parameters specified above.

Submit