POLITECNICO DI TORINO

Applied electronics

Exam of 22 January 2021

This is an example of exam. Solutions are reported in red in the orange rectangle.

Exam consistes in 10 Quiz (max 10 points), 4 open problems (5 point each), 3 optinal questions on lab part (1 point each)

Score is: (quiz points + problem points)*0.9+optinal questions points . Max mark is 30/30

Domanda 1

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a square wave generator realized with Schmitt trigger inverter; the voltage on the capacitor varies with time as:

- (a) square wave
- (b) is always zero
- (c) linear
- (d) exponential ✓

Risposta corretta.

La risposta corretta è: exponential

Domanda 2

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a synchronous write cycle; the STB signal must stay high for a minimum duration equal to:

- (a) Tk+Ttxmin
- (b) Tsu+Tk
- (c) Tk
- (d) Th+Tk ✓

Risposta corretta.

La risposta corretta è: Th+Tk

Domanda 3

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The maximum number of CMOS logic gates that can be connected to one CMOS logic gate of the same family is limited by:

- (a) the maximum output current from the logic gate
- (b) the voltage supply Vdd
- (c) the maximum acceptable delay for a logic state transition ✓
- (d) the maximum static power consumption

Risposta corretta.

La risposta corretta è:
the maximum acceptable delay for a logic state transition

Domanda 4

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

Consider a FPGA; a Look-Up Table (LUT) with 3 inputs needs:

- (a) 8 FAMOS
- (b) 8 NAND gates and 4 NOR gates
- (c) 8 SRAM memory cells ✓
- (d) 4 NAND gates and 8 NOR gates

Risposta corretta.

La risposta corretta è: 8 SRAM memory cells

Domanda 5

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

A FAMOS when programmed

- (a) has a threshold voltage higher than the threshold voltage of the FAMOS which is not programmed ✓
- (b) has I_{DS} higher than the not programmed FAMOS, when same V_{DS} is applied
- (c) has a threshold voltage smaller than the threshold voltage of the FAMOS which is not programmed
- (d) has a threshold voltage equal to the threshold voltage of the FAMOS which is not programmed

Risposta corretta.

La risposta corretta è: has a threshold voltage higher than the threshold voltage of the FAMOS which is not programmed

Domanda 6

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

AA NAND Flash memory consists in:

- (a) NMOS and PMOS transistoes in series
- (b) NMOS and PMOS transistors in parallel
- (c) FAMOS transistors in parallel
- (d) FAMOS transistors in series ✓

Risposta corretta.

La risposta corretta è: FAMOS transistors in series

Domanda 7

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The reflection coefficient of a transmission line terminated with a termination resistance R_T equal to two times the characteristic impedance of the line, is:

- (a) 1
- (b) 1/4
- (c) 1/2
- (d) 1/3 ✓

Risposta corretta.

La risposta corretta è: 1/3

Domanda 8

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The output voltage of buck regulators is:

- (a) Vout<Vin ✓
- (b) Vout=2 Vin
- (c) Vout=Vin
- (d) Vout>Vin

Risposta corretta.

La risposta corretta è: Vout<Vin

Domanda 9

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The conversion time Tc of a Successive Approximation Converter can be reduced of a factor 2 by:

- (a) doubling the number of bit of the SAR
- (b) none of the answers reported here is the correct one
- (c) doubling the CK period of the SAR
- (d) doubling the CK frequency of the SAR ✓

Risposta corretta.

La risposta corretta è: doubling the CK frequency of the SAR

Domanda 10

Risposta corretta

Punteggio ottenuto 1,0 su 1,0

The ADC of a data acquisition system provides a SNRq=65.76dB, whereas the total SNR is degraded of other 10dB due to the non-idealities of the other blocks. Calculate the ENOB.

- (a) ENOB<8
- (b) ENOB>10
- (c) ENOB=10
- (d) ENOB=9 ✓

Risposta corretta.

La risposta corretta è: ENOB=9

Domanda 11

Completo

Punteggio ottenuto 5,0 su 5,0

Consider 8 input channels with analog signals with bandwidth up to 30kHz. The input voltage of each channel is in the range between -0.5V and +0.5V. The signals are converted with an A/D conversion system using only one S/H and Successive Approximation ADC with dynamics 0-10V. The S/H acquisition time is 500ns and the MUX introduces a delay of 30ns.

Request 1: List the building blocks of the entire acquisition system, describe the role of each block and specify the bandwidth of the anti-aliasing filters.

Request 2: Calculate the minimum number of bits of the ADC to have 1LSB of less than 10mV

Request 3: Each input signal must be sampled at a frequency of 100kHz. Calculate the CK frequency of the SAR.

---

write here your answers . Solutions are in the orange rectangle

a) List the building blocks of the entire acquisition system, describe the role of each block and specify the bandwidth of the anti-aliasing filters.

b) Calculate the minimum number of bits of the ADC to have 1LSB of less than 10mV

10 bit implies 10/(2^10)*1000=9.76 mV è N=10

c) Each input signal must be sampled at a frequency of 100kHz. Calculate the CK frequency of the SAR.

Sampling frequency at SH is 800kHz. è Ts=1/(800kHz)=1250ns.

Ts=Tacq+Tmux+Tc è Tc=1250-500-30=720ns = NTck è Tck=720/10=7.2ns => fck=1/7.2ns=13.89MHz

Domanda 12

Completo

Punteggio ottenuto 0,0 su 5,0

A track of 30cm on a PCB backplane has characteristic impedance $Z_{¥}$ = 90Ω (with no load), and wave propagation speed u = 0,6 c. We need to connect to the track N=10 equally spaced receivers. Each device has an input capacitance of 1pF. The line is driven on one side and closed with a matched termination on the other side.

The driver and receivers have the following electrical parameters:

Voh = 4.1 V, Vol = 0,4 V, Vih = 2,5 V, Vil = 1,0 V; Vdd=4.5V.

Request 1)

Calculate the capacitance per unit length of the line without any connected device.

Request 2)

Calculate the characteristic impedance of the line with the connected receivers

Request 3)

Calculate the output resistance of the driver to drive the line in IWS mode and NM=0.5V. Include in the calculation the effect of the capacitive load.

Write here your answers, solutions are in the orange rectangle

Request 1:

the capacitance per unit of length is *C=1/(Z∞*u) ==> C=0.62pF/cm*

Request 2:

*Z∞'=Z /sqrt(1+NCi/L*C)=72.6 ohm*

Request 3:

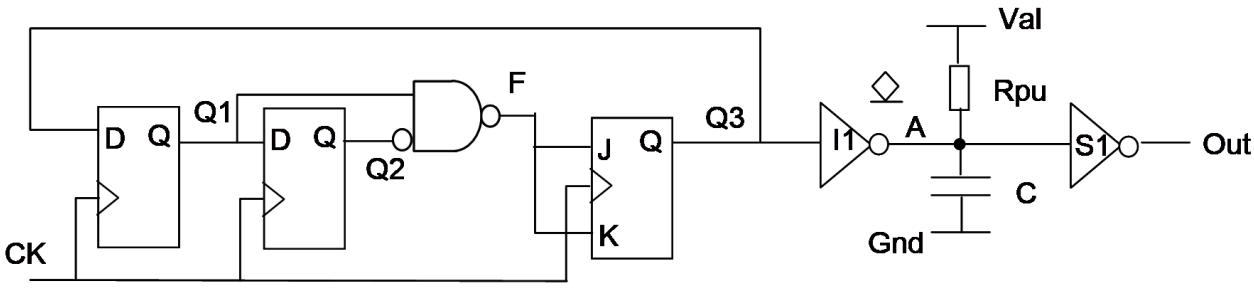
Vb(0)=*Z∞'/(Z '+Ro)*Vdd>=Vih+NM=3V ==> Ro<=36.3 ohm*

Domanda 13

Completo

Punteggio ottenuto 5,0 su 5,0

Consider the sequential circuit shown in the figure and assume that the outputs Q1, Q2 and Q3 are initially all reset to 0 logic state. Consider the capacitor C=0.



The delays for all the components are reported below:

Tsu = 3 ns, Th = 2 ns (D-FF and JK FF) ;

T*ck->Q* = 5 ns (D-FF and JK FF)

NAND gate and inverters I1 and S1: T_{LH} = 3ns, T_{HL} = 4 ns,

Answer the following questions:

Request 1:

- How many CK active edges are needed to switch Q1 to logic state 1?
- Which is the initial state of the output A
- How many CK active edges are necessary to switch the output of S1 to state 1 ?

Request 2:

Assuming C=0, calculate the maximum CK frequency.

Request 3:

Calculate the propagation delay for a transition LèH of the state at node A. Assume: C=5pF, the input capacitance of S1 equal to Ci=4pF, Rpu=1kohm and the output resistance of I1 equal to Ro=100 ohm (when output of I1 is in low state);

Request 1:

- How many CK active edges are needed to switch Q1 to logic state 1? 2
- Which is the initial state of the output A? high state
- How many CK active edges are necessary to switch the output of S1 to state 1 ? first CK edge

Request 2:

Assuming C=0, calculate the maximum CK frequency.

Tckmin=tck_>Q+tdnand+tsu=12 ns fckmax=83.3MHz

Request 3:

tdLH=0.69*(Ci+C)*1kohm=6.21 ns

Domanda 14

Completo

Punteggio ottenuto 5,0 su 5,0

A DRAM memory has the following characteristics:

- 16 bit address: 12 bits are for row address and 4 bits are for column address.

- words are of 8 bits

- pass transistors with Cd=0.5fF

1. #word lines = # of rows=2^12=4096

2. # memory cells= 2^12*2^4*8= 524288

3. CbL=2^12*0.5fF=2.05 pF

Domanda 15- Optional on laboratory part

Analog-to-digital and Digital-to-Analog converters:

When is it possible to observe the phenomenon of "glitches" affecting the performance of a DAC converter similar to the one realised and simulated with the LTspice software during the virtual LAB? Explain the origin of the glitch.

Domanda 16 Optional on laboratory part

Which behaviour do you expect to observe if you visualise with the Waveform Viewer of the LTspice software the voltages at the near and far end of a coaxial cable described by a transmission line model (with characteristic impedance Zinf=50Ohm) with open termination and connected to a square wave generator characterised by an internal resistance of RG=50Ohm on the driving side?

Domanda 17- Optional on laboratory part

How can you realise and simulate with the LTSpice software a square wave signal generator based on a SN74HC14 Schmitt trigger in order to provide the clock signal for a synchronous counter such as the 4-bit CD4029 counter adopted during the virtual LAB?