ADC pipeline

The conversion time of a pipeline ADC with N bits:

- ○ is not determined by the number of bits N
- ○ is proportional to N
- ○ is proportional to 2^N
- ○ is proportionalto 1/N

ADC SAR circuit 1

The conversion time Tc of a Successive Approximation Converter can be reduced of a factor 2 by:

- ○ doubling the CK frequency of the SAR
- ○ doubling the CK period of the SAR
- ○ doubling the number of bit of the SAR
- ○

none of the answers reported here is the correct one

Asynchr serial -1

Consider an asynchronous serial protocol. The protocol requires:

- ○ one start bit and one stop bit
- ○ only one start bit, a no stop bit
- ○ no start bit and one stop bit
- ○ no start bit and no stop bit

ASynchr write cycle 1 (copia)

Consider an asynchronous write cycle; when does the STB signal go high after the INF?

- ○ STB goes high after tk
- ○ STB goes high after tk+th
- ○ STB goes high after tk+tsu
- ○

STB goes high after tk+th+tsu

buck regulator 1

The output voltage of buck regulators is:

- ○ Vout<Vin
- ○ Vout>Vin
- ○ Vout=Vin
- ○ Vout=2 Vin

D-FF

Consider a D-FF. Select the correct sentece:

- ○ During the set-up time D must not change
- ○ D must be always 1 during the set-up time
- ○ D must be always 0 during the set-up time
- ○ During the set-up time D must change no more than 2 times

DAC resistenze pesate

Consider a 2 bit weighted resistor DAC; the ration bewtween the resistance of the MSB branch (R_{MSB}) and the resistance of the LSB (R_{LSB}) branch is:

- ○ $R_{MSB}/R_{LSB}=0.5$
- ○ $R_{MSB}/R_{LSB}=2$
- ○ $R_{MSB}/R_{LSB}=4$
- ○ $R_{MSB}/R_{LSB}=0.25$

DDR3 speed

The maximum speed of a 8 bit DRAM DDR3 module with bus clock at 1000 MHz is:

- ○ 16 Gbit/s
- ○ 8 Gbit/s
- ○ 8 Mbit/s
- ○ 16 Mbit/s

delay Lto H transistion 1

One logic gate with output resistance Ro is driving 4 inverters with input capacitance Ci=4pF. The propagation delay of a L➔ H transitions is:

- 2.76·Ro·Ci
- 0.69·Ro·Ci
- Ro·Ci
- 4·Ro·Ci

DRAM cell

A DRAM memory cell consists in:

- one MOS and one capacitor
- one FAMOS
- 6 MOS
- one MOS and 2 capacitors

dynamic power vs f

If we divide by 2 the clock frequency of a CMOS digital circuit, the dynamic power consumption will change of a factor equal to:

-

0.5

2

4

0.25

ENOB 1

The ADC of a data acquisition system provides a SNRq=65.76dB, whereas the total SNR is degraded of other 10dB due to the non-idealities of the other blocks. Calculate the ENOB.

ENOB=9

ENOB=10

ENOB>10

ENOB<8

ENOB2

A data acquisistion system has a total SNR of 49.76dB. Calculate the ENOB.

ENOB=8

ENOB=10

ENOB<7

ENOB>10

Errore DAC resitenze pesate

Consider a 8 bit weighted resistors DAC. The resistor of the MSB branch has an error of -5%. Which is the error that we find in the DAC characteristic?

non-monotonicity error

non linear error

gain error

differential error

FAMOS 1

A FAMOS when programmed

has a threshold voltage higher than the threshold voltage of the FAMOS which is not programmed

has a threshold voltage equal to the threshold voltage of the FAMOS which is not programmed

○

has a threshold voltage smaller than the threshold voltage of the FAMOS which is not programmed

○

has I_{DS} higher than the not programmed FAMOS, when same V_{DS} is applied

Fan out 1

The maximum number of CMOS logic gates that can be connected to a logic gate of same family is limited by:

○

the maximum acceptable delay for a state transition

○

the current I_{IH}

○

the current I_{IL}

○

the maximum static power consumption

Fan out 2

The maximum number of CMOS logic gates that can be connected to one CMOS logic gate of the same family is limited by:

○

the maximum acceptable delay for a logic state transition

○

the maximum output current from the logic gate

○

the voltage supply Vdd

○

the maximum static power consumption

FF JK

Consider a JK-FF with CK active on the falling edge and J=K=1; in this condition we have:

○

the output toggles on the falling edge of the CK

○

the FF is in memory state

○

the output toggles on the rising edge of the CK

○

the output is always Q=1

Flash memory

Consider a NAND flash memory; the elementary units for erasing and writing operations are:

- block (= erasing of several pages) and page (=elementary unit that can be written)
- page (=erasing of several blocks) and byte (=elementary unit that can be written)
- block (= erasing of several pages) and byte (=elementary unit that can be written)
- byte (= erasing unit) and page(= writing on one byte)

Flash memory cell

. A flash memory cell consists in:

- one FAMOS
- one MOS and one capacitor Cs
- one FAMOS and one capacitor Cs
- one NMOS, one PMOS and two capacitors

FPGA definition

A FPGA consists in:

- LUT, MUX and registers
- Arrays of OR gates
- Arrays of AND gates
- Arrays of SRAM cells

FPGA LUT 1

To realize an FPGA-LUT of 2 inputs we need:

- 4 SRAM cells and 1 MUX
- a ROM
- 8 DRAM cells
- 6 SRAM cells and 1 MUX

FPGA, LUT

Consider a FPGA; a Look-Up Table (LUT) with 3 inputs needs:

- 8 SRAM memory cells
- 8 FAMOS

○

4 NAND gates and 8 NOR gates

○

8 NAND gates and 4 NOR gates

Full wave rectifier-1

If we substitute a full-wave rectifier with a half wave rectifier, the power associated to the ripple voltage noise will scale of a factor equal to:

○

4

○

2

○

0.5

○

0.25

Generatore onda quadra 1

Consider a square wave generator with Schmitt trigger inverter, the period T of the square wave can be approximated with

○

T=RC

○

T=0.69RC

○

T=2RC

○

T=1.6RC

Generatore onda quadra 2

Consider a square wave generator with Schmitt trigger inverter, the frequency of the square wave can be increased by:

○

reducing the resistance R

○

increasing the resistance R

○

increasing the capacitance C

○

doubling the resistance R

interfacing

Vo is the output voltage of a logic gate , choose the right condition for connecting Vo to the input of another logic gate (the voltage supply is V_{DD}):

○

Vo=Vih+NM

○

Vil<Vo<Vih

○

Vo=Vil+NM

○

Vo<0

○

Vo>V_{DD}

Latch

Consider a D-Latch active when LE is low (=0). When LE=0:

○

the output state follows the input state D

○

the output is always 1

○

the output is in memory state

○

the output is always 0

LUT 4 inputs

A LUT with four inputs consists in:

○

16 SRAM cells and one MUX

○

8 SRAM cells and two MUX

○

2 DRAM cells and 2 MUX

○

4 FAMOS

matched termination

The reflection coefficient of a transmission line terminated with a termination resistance R_T equal to two times the characteristic impedance of the line, is:

- ○ 1/3
- ○ 1/2
- ○ 1
- ○ 1/4

memory architecture

A DRAM memory with words of 8 bits and 3 bit row address has:

- ○ 64 capacitors
- ○ 128 MOS transistors
- ○ 8 capacitors
- ○ 8 MOS transistors

moore law 1

The graph reporting the number of transistors in microprocessors in the last 40 years shows that:

- The number of transistors doubles every two years
- The number of transistors increases of a factor 4 every two years
- It is impossible to find a clear trend
- As consequence of the increased number of transistors, the CK speed has been reduced of a factor 2

Moore Law corretta

The trend (during the last 40 years) of the number of transistors in microprocessors shows that:

- The number of transistors doubles every two years
- The number of transistors is increased of a factor 4 every two years
- It is impossible to find a clear trend
- As consequence of the increased number of transistors, the CK speed has been reduced of a factor 2

NAND Flash memory

A NAND Flash memory consists in:

FAMOS transistors in series

FAMOS transistors in parallel

NMOS and PMOS transistoes in series

NMOS and PMOS transistors in parallel

onda quadra-condesatore

Consider a square wave generator realized with Schmitt trigger inverter; the voltage on the capacitor varies with time as:

exponential

square wave

linear

is always zero

SDRAM 1

A SDRAM memory is

a synchronous dynamic RAM

a type of static RAM

an asynchronous SRAM

a RAM with 6 MOS transistor

Synchr write cycle 1

Consider a synchronous write cycle; the STB signal must stay high for a minimum duration equal to:

Th+Tk

Tk

Tsu+Tk

Tk+Ttxmin

Voltage after transient

A driver with voltage supply Vdd and output resistance Ro drives a transmission line with characteristic impedance Z_∞; the line is terminated with a resistor Rt. After the transient of L->H transition, the line steady state voltage is:

Vdd ·Rt/(Rt+Ro)

Vdd

○

Vdd $Z_\infty/(Z_\infty+Ro)$

○

Vdd $Z_\infty/(Rt+Z_\infty)$

voltage regulator

The efficiency (ie: ratio between output and input power) of a series linear volatge regulator, with input Vi and output Vo can be approximated as:

○

Vo/Vi

○

Vi/Vo

○

Vo/(Vi+Vo)

○

\(\sqrt{Vi/Vo} \)

voltage step 2

Consider a L➔ H transition propagating in a transmission line with characteristic impedance Z_∞ and matched termination. The output resistance of the driver is R_0=0.5 Z_∞ and V_{DD}=3.3V. The first incident voltage step is:

○

2.2 V

○

1.5 V

- [ ] 3.3 V
- [ ] 1.65 V

Submit