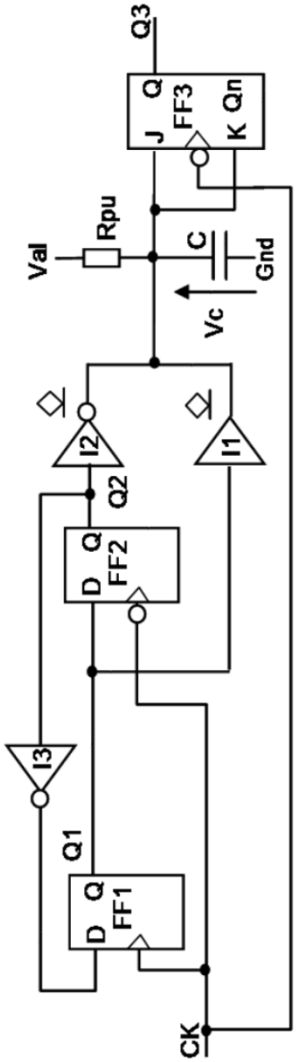
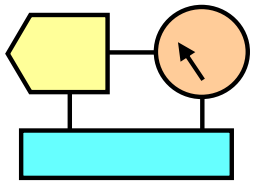


APPLIED ELECTONICS

Class exercises with solutions



APPLIED ELECTONICS

Part B:

- **CMOS logic gate Static and Dynamic parameters**
- **Combinational logic circuits**
- **Sequential logic circuits and timing diagrams**

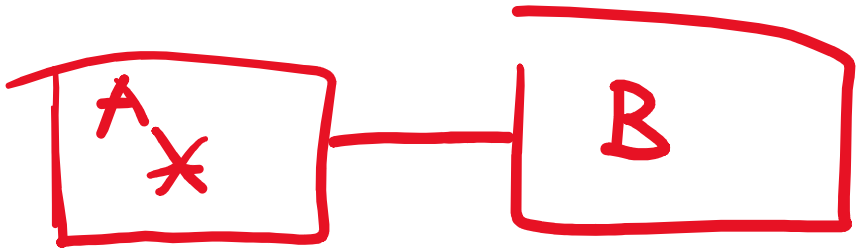
Problem 1- Assignment
Static parameters
Voltage compatibility

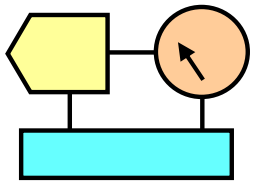
a) Consider a logic gate with the following static electrical parameters:

A
Output electrical parameters
V_{OL} = 0.37 V, V_{OH} = 3.76 V

B
Input electrical parameters
V_{IL} = 0.9 V, V_{IH} = 3.15 V

and check the voltage compatibility





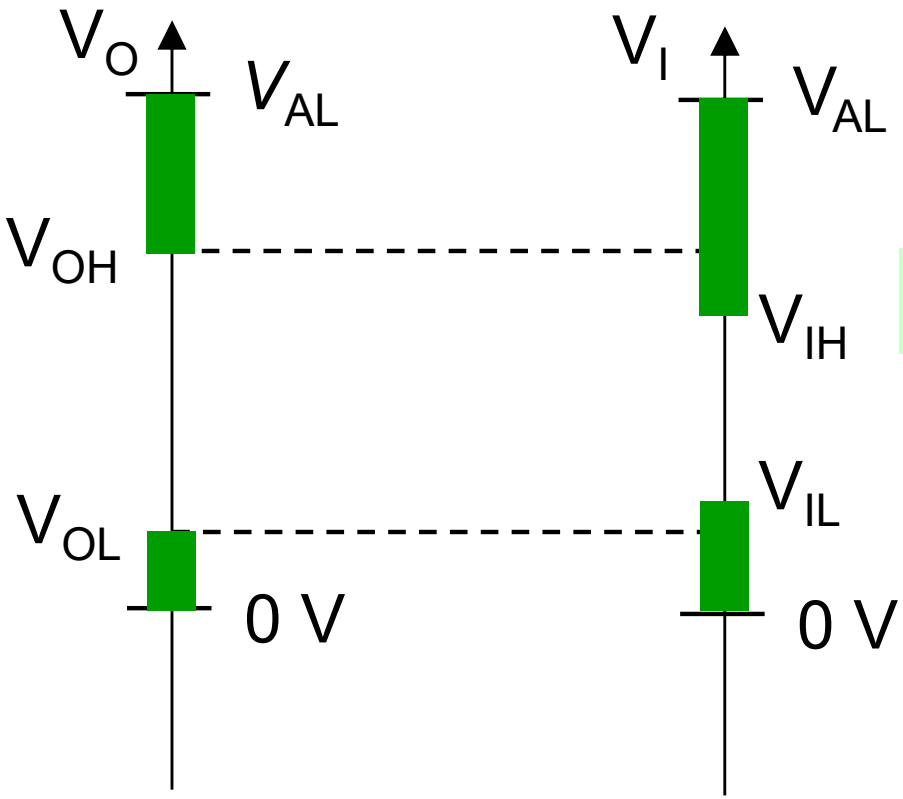
Problem 1
Theoretical remind

Input/output electrical parameters

- V_{IH}: maximum value of the threshold V_T
  - Input voltages $V_I > V_{IH}$ are interpreted as H state
- V_{IL}: minimum value of the threshold V_T
  - Input voltages $V_I < V_{IL}$ are interpreted as L state
- V_{OH}: high state minimum output voltage
  - State H: $V_O > V_{OH}$, **(as long as $|I_O| < |I_{OH}|$)**
- V_{OL}: low state maximum output voltage
  - State L: $V_O < V_{OL}$, **(as long as $|I_O| < |I_{OL}|$)**

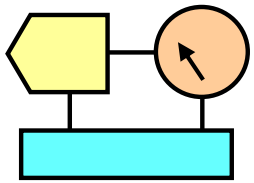
Problem 1 Solution

Since NM_H and NM_L are positive we conclude that the ports **are compatible**



$$NM_H = V_{OH} - V_{IH} = 0.61\,V$$

$$NM_L = V_{IL} - V_{OL} = 0.53\,V$$



Problem 2- Assignment
Dynamic parameters

a) Calculate the maximum delay ($t_{DLH,max}$) in the connection of two gates with the following electrical parameters

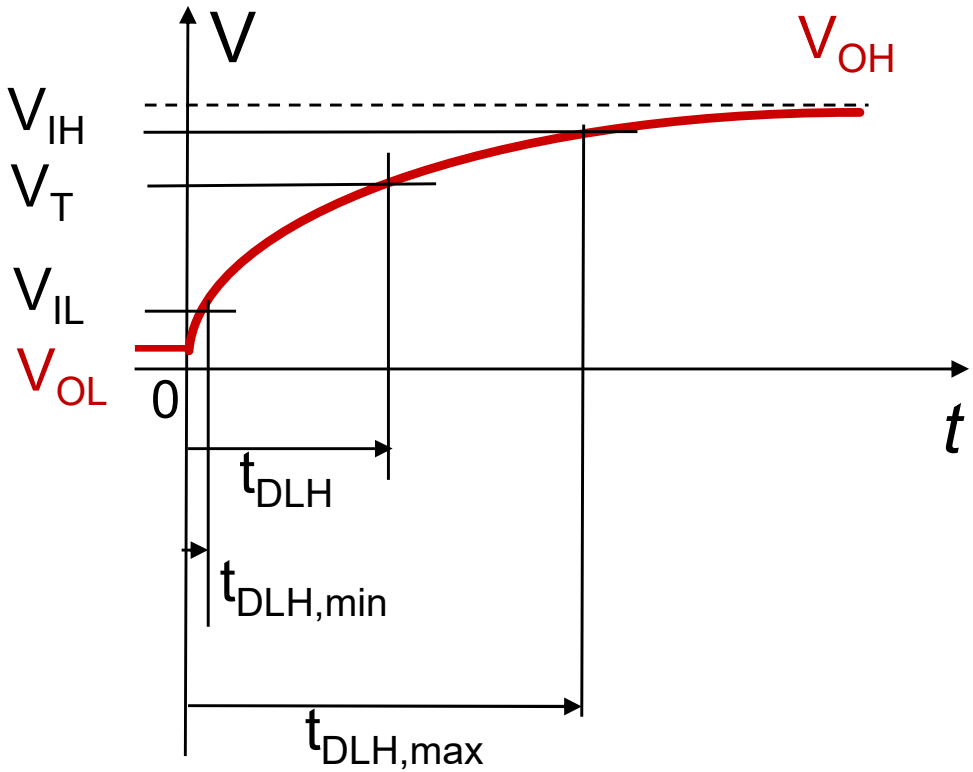
V_{OL} = 0.4 V; V_{OH} = 3 V; V_{IL} = 1 V; V_{IH} = 2 V;
C_I = 50 pF $R_{OH,OL}$ = 130 Ω R_I = 1 MΩ

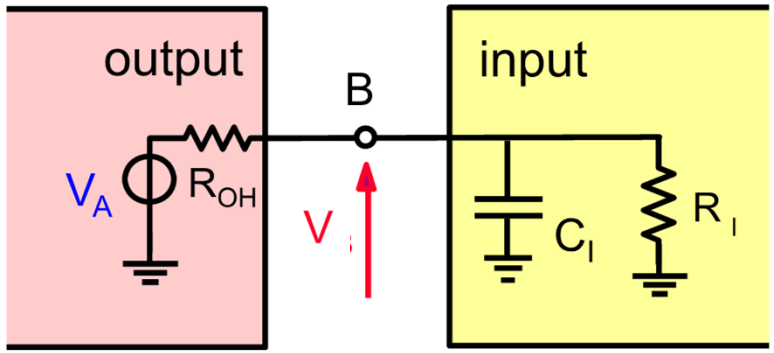
b) Calculate how many gates can be connected to the output to limit the delay to 20 ns

Problem 2
Theoretical remind

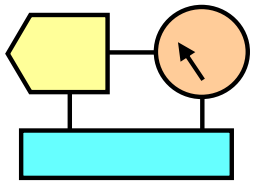
Delay RC model: L→H transition of the output

The time needed for the output voltage V to reach the threshold voltage V_T starting from L level is the delay time t_{DLH}





V_T is generally not known precisely. We only know that it is between V_{IL} and V_{IH}. Therefore, we can calculate a minimum delay for $V_T = V_{IL}$ and a maximum delay for $V_T = V_{IH}$



Problem 2a Solution

The voltage V(t) is (charge of a capacitor with capacitance C_l):

$$V(t) = V_{OH} + (V_{OL} - V_{OH})e^{-t/\tau_{LH}}$$

$$\begin{cases} V(t=0) = 0 \\ V(t \to +\infty) = V_{DD} \end{cases}$$

with $\tau_{LH} = C_l R_{OH\,=\,6.5}$ ns (R_l can be neglected since it is >> R_{OH}).

Since the **maximum delay $t_{DLH,max}$** satisfies the relation $V(t_{DLH,max}) = V_{IH}$:

$$V_{IH} = V_{OH}(1 - e^{-t_{DLH,max}/\tau_{LH}})$$

$$t_{DLH,max} = \tau_{LH} \ln\left[\frac{V_{DD}}{(V_{DD} - V_{IH})}\right]$$

At the exam you could use this simplified formula

NOTE: In the ideal case: $V_{IH} = V_{IL} = V_T = \frac{V_{AL}}{2} \Longrightarrow$

$t_{DLH} = \ln(2)\tau_{LH} = 0.69 \times 6.5$ ns $= 4.485$ ns

Problem 2b Solution

The total delay increases in presence of $\mathbf{n_{gates}}$ **(>1) gates** connected to the output because the total capacitance increases according to the formula:

$$C_{tot} = n_{gates} C_I$$

In fact:

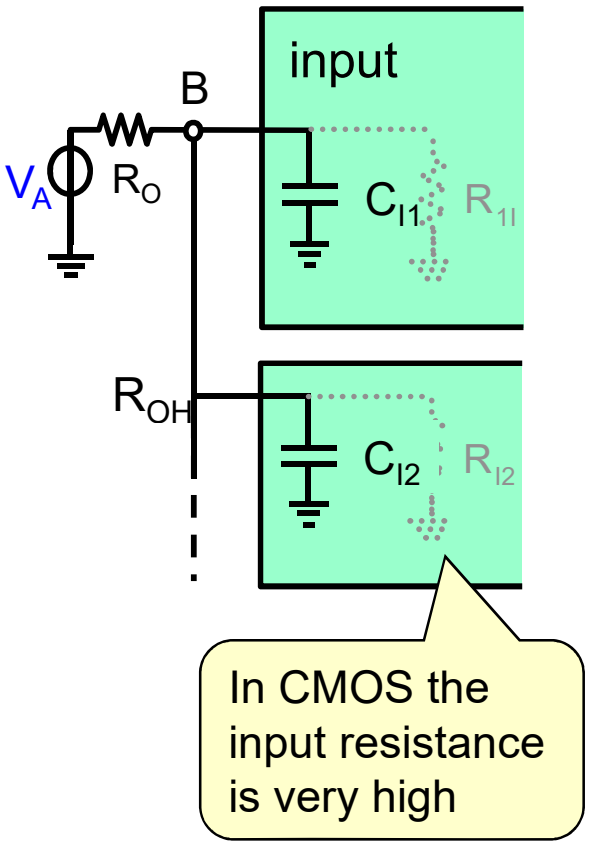
$$\tau_{LH} = R_{OH} C_{tot} = n_{gates} (R_{OH} C_I) = n_{gates} 6.5 \text{ ns}$$

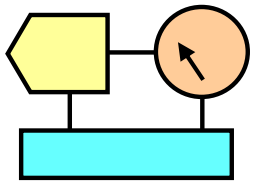
In the ideal case:

$$t_{DLH,ngates} = \ln(2) \tau_{LH} = 0.69\, n_{gates} 6.5 \text{ ns}$$

From which, in order to limit the delay to 20 ns ($t_{DLH,ngates} < 20$ ns), we must require that:

$$n_{gates} < 4$$



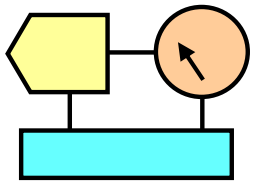


Problem 3- Assignment
Combinational logic circuit

a) Plot the circuit in CMOS technology that implements the logic function:

$$U = (A*B) + C$$

b) If the output is loaded with C_L= 50 pF, calculate the maximum delay for a L-> H and H->L transition. Assume for each MOS R_O= 60 Ω.



Problem 3
Theoretical remind

Boolean identities

AND function	OR function	NOT function
$0 \cdot 0 = 0$	$0 + 0 = 0$	$\overline{0} = 1$
$0 \cdot 1 = 0$	$0 + 1 = 1$	$\overline{1} = 0$
$1 \cdot 0 = 0$	$1 + 0 = 1$	$\overline{\overline{A}} = A$
$1 \cdot 1 = 1$	$1 + 1 = 1$	
$A \cdot 0 = 0$	$A + 0 = A$	
$0 \cdot A = 0$	$0 + A = A$	
$A \cdot 1 = A$	$A + 1 = 1$	
$1 \cdot A = A$	$1 + A = 1$	
$A \cdot A = A$	$A + A = A$	
$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$	

Boolean laws

Commutative law
$AB = BA$
$A + B = B + A$

Distributive law
$A(B + C) = AB + BC$
$A + BC = (A + B)(A + C)$

Associative law
$A(BC) = (AB)C$
$A + (B + C) = (A + B) + C$

Absorption law
$A + AB = A$
$A(A + B) = A$

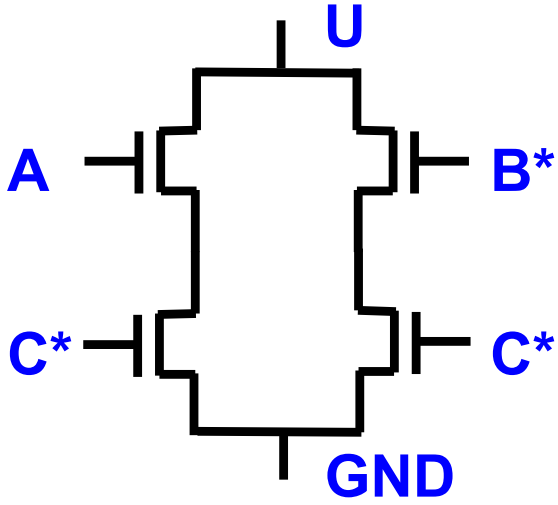
De Morgan's law
$\overline{a \cdot b} = \overline{a} + \overline{b}$
$\overline{a + b} = \overline{a} \cdot \overline{b}$

Note also
$A + \overline{a}\, B = A + B$
$A(\overline{a} + B) = AB$

Problem 3a Solution

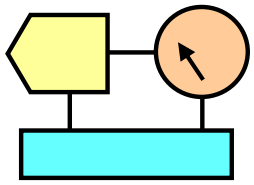
1. We define the **equivalent nSW structure** starting from the **negated output**.

   From the De Morgan's laws and the other properties of the Boolean algebra:



$$U^* = ((A^*B) + C)^*$$

$$U^* = (A^*B)^*\ C^* = (A + B^*)\ C^* = A\ C^* + B^*\ C^*$$



Problem 3a Solution

1. We define the **equivalent nSW structure** starting from the **negated output**.

   From the De Morgan's laws and the other properties of the Boolean algebra:

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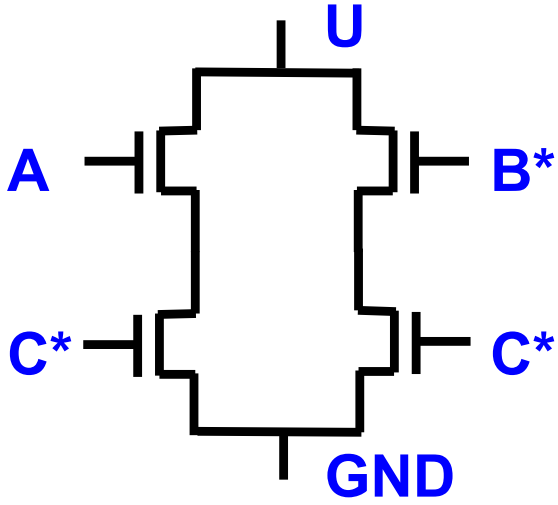
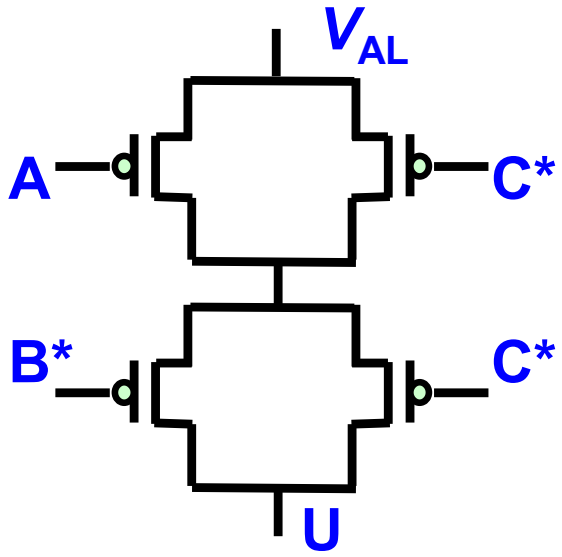
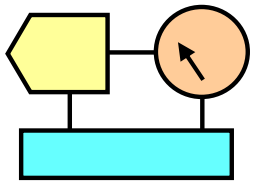
$$U^* = (A^*B)^*\ C^* = (A + B^*)\ C^* = A\ C^* + B^*\ C^*$$



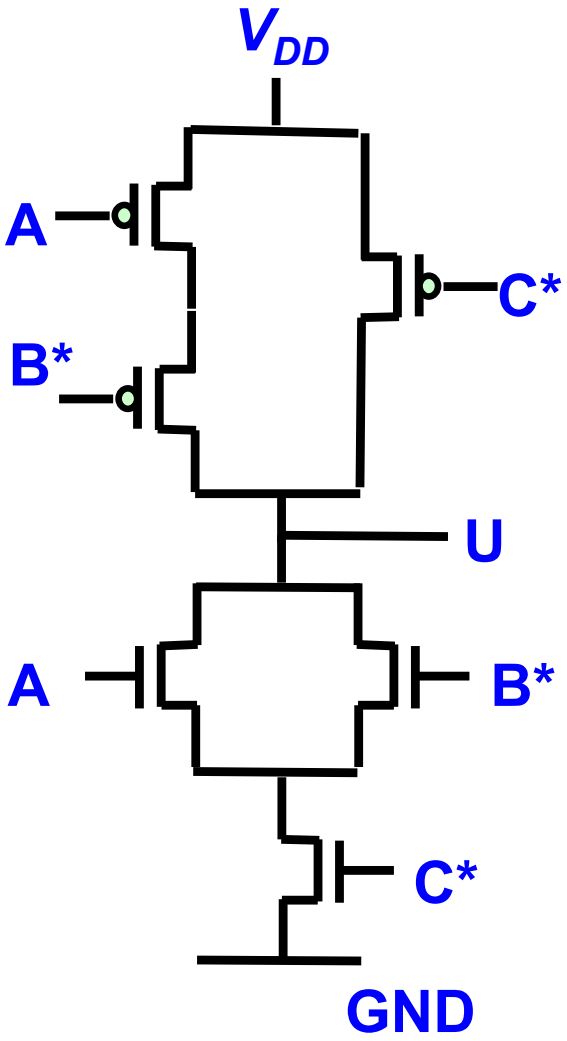
2. We define the **complementary pSW circuit**





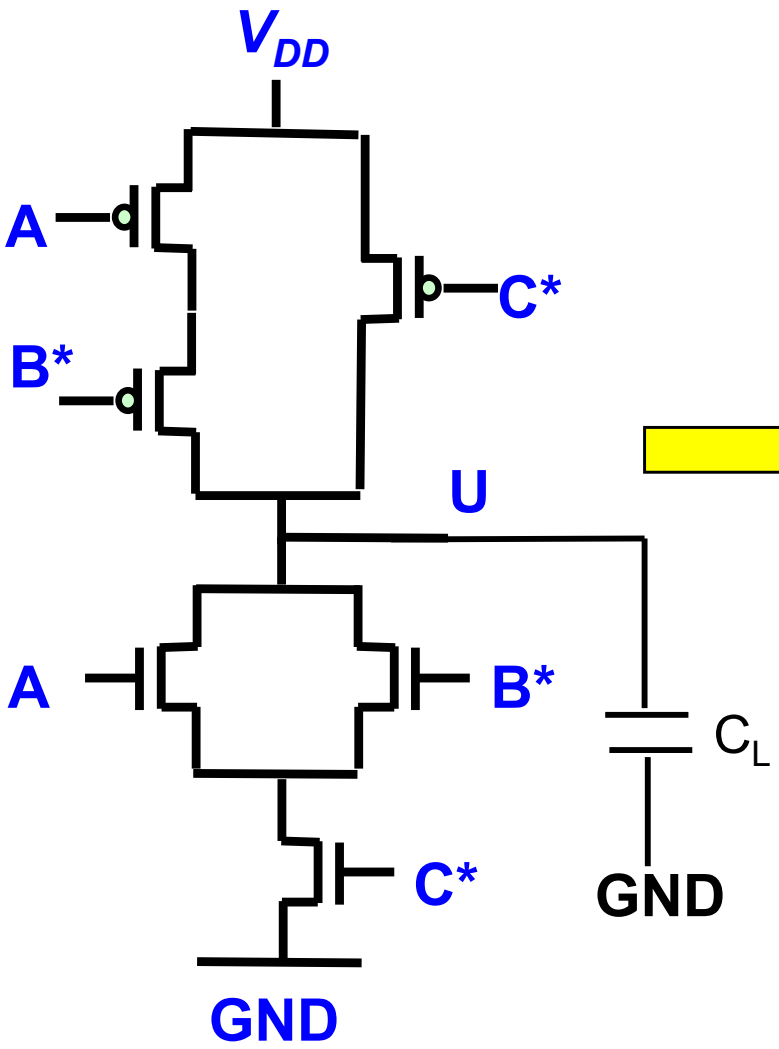
Problem 3a
Solution

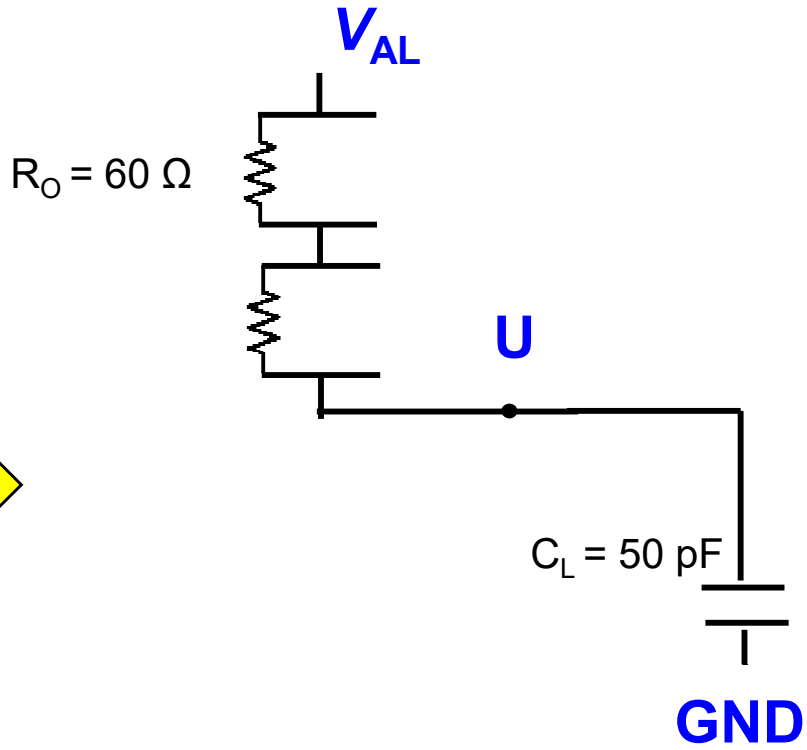
3. We build the **complete circuit**



Problem 3b Solution

Delay for L→H: we use the simplified formula for the delay time: $t_{DLH}=0.69\tau_{LH}$





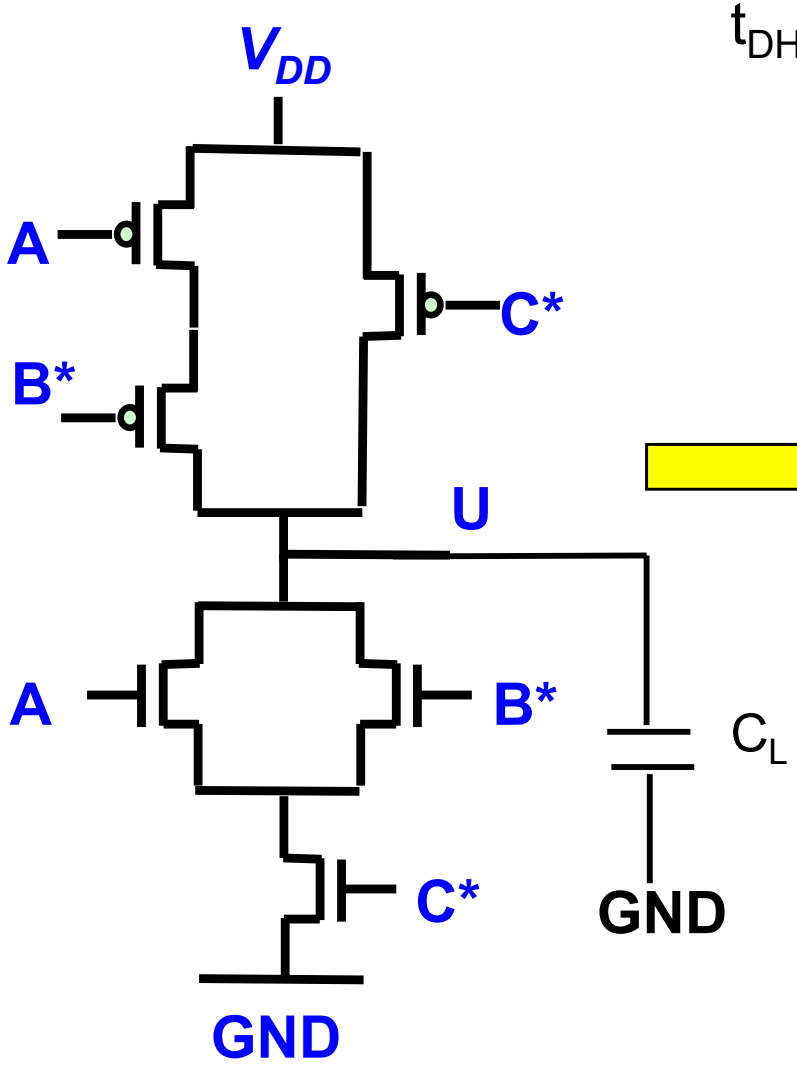
Maxium delay is:

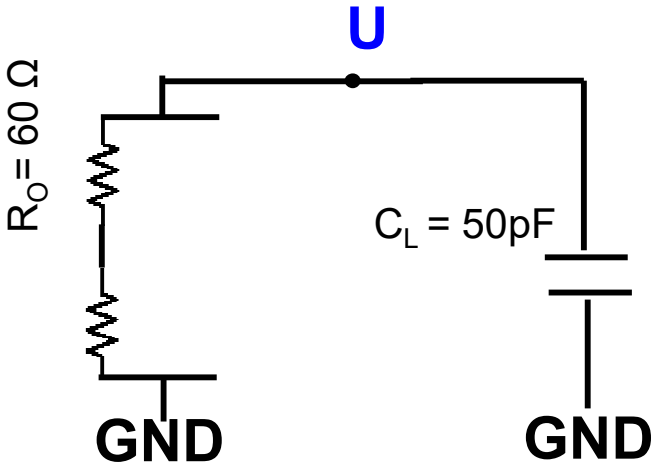
$$t_{DLH,M} = 0.69(2R_O C_L) = 4.1 \text{ ns}$$

Problem 3b Solution

Delay for H→L: we use the simplified formula for the delay time:

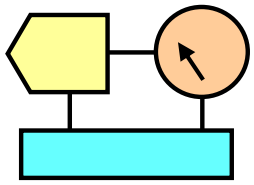
$$t_{DHL} = 0.69\tau_{HL}$$





maximum delay is:

$$t_{DHL,M} = 0.69(2R_O C_L) = 4.1 \text{ ns}$$



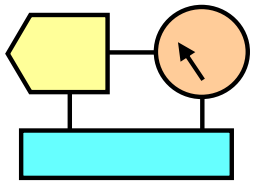
Problem 4 - Assignment
Power consumption

a) Calculate the static and dynamic power consumption of a CMOS circuit with:
   - Voltage supply of 2 V
   - In average per time instant:

     50.000.000 transistors in 'off' state

     100.000.000 inputs with Ci = 1 fF

   Consider the two cases:
   - Switching frequency Fm = 200 MHz and Ioff = 1 nA per MOS
   - Switching frequency Fm = 2 GHz and Ioff = 100 nA per MOS



Problem 4a Solution

The **static power dissipated** due to Ioff of the MOS transistors is:

P_S = Ioff × 2V × Noff where Noff is the number of transistors OFF.

Then: for Ioff = 1 nA and Noff = 50E6: P_S = 0.1 W
for Ioff = 100 nA and Noff = 50E6: P_S = 10 W

The **dynamic power dissipated** due to capacitance charge/discharge is:

$P_D = (C \times Fm \times V^2) \times N$ where N is the number of connected transistors.

Then for a single transistor connected we get:
for Fm = 200 MHz: P_D (1 capacitor, 200 MHz) = 0.8 μW
for Fm = 2 GHz: P_D(1 capacitor, 2 GHz) = 8.0 μW

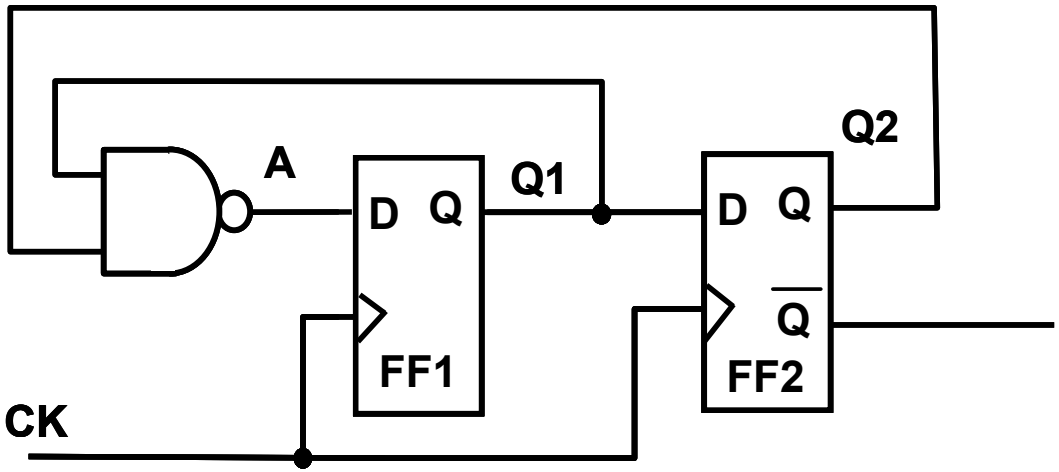
Finally, multiplying by the number of transistors N =100E6 we get:
P_D (total, 200MHz) = 80 W and P_D(total, 2 GHz) = 800 W

!!!!!!! Important thermal issue!!!!!

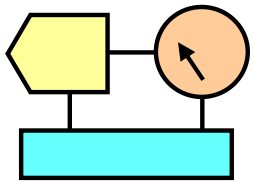
Problem 5 - Assignment
Sequential logic circuits
Timing diagrams

a) Plot in a timing diagram the output signals sequence ($Q_1(t)$; $Q_2(t)$; A(t)) for 4 clock cycles in the digital circuit reported in the picture below. Assume that at the initial state (t = 0): $Q_i = 0$

b) Compute the delays and estimate the maximum clock frequency in the case: $T_{NAND} = 2$ ns ; $T_{CKQ} = 3$ ns; $T_{su} = 1$ ns ; $T_h = 1$ ns



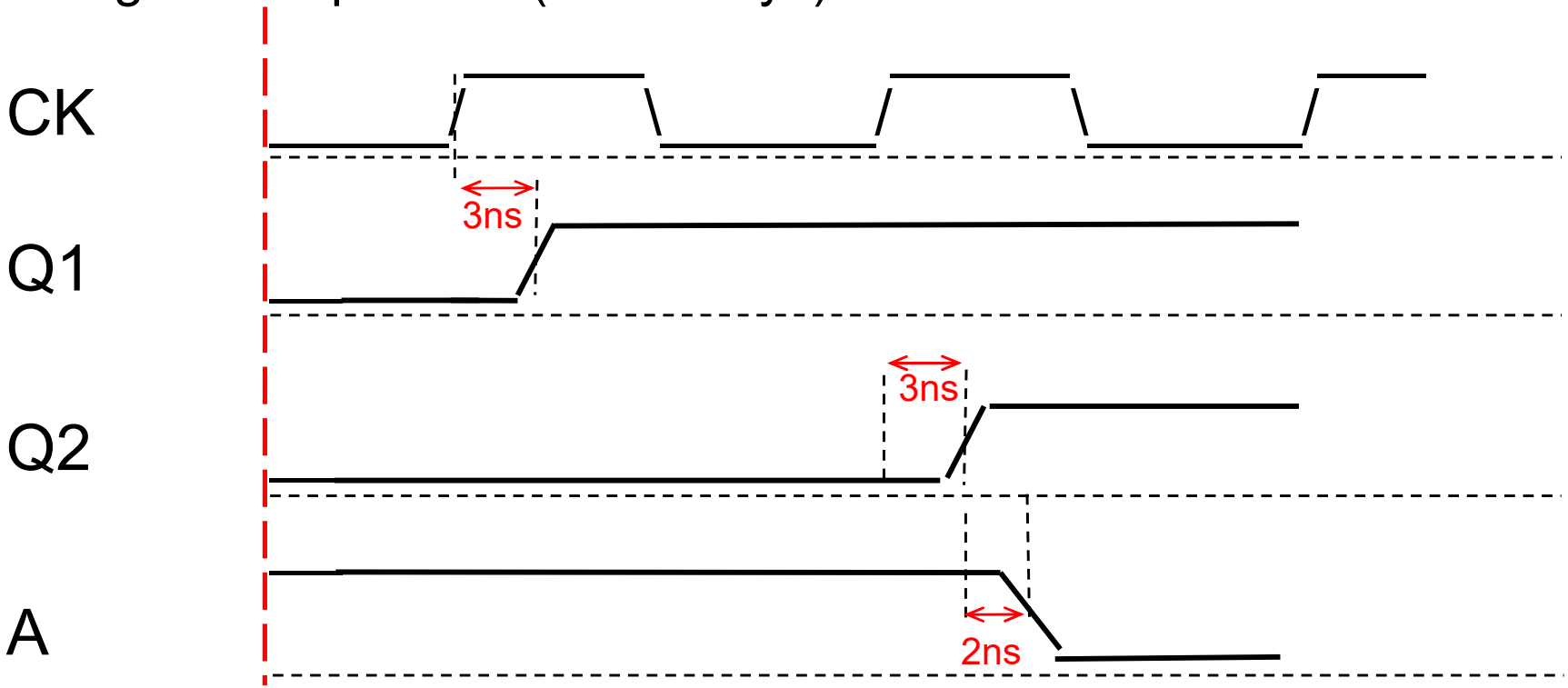

POLITECNICO DI TORINO
1859
1906



Problem 5b Solution

T_{NAND} = 2 ns ; T_{CKQ} = 3 ns; T_{su} = 1 ns ; T_h = 1 ns

- Signals sequences (with delays)



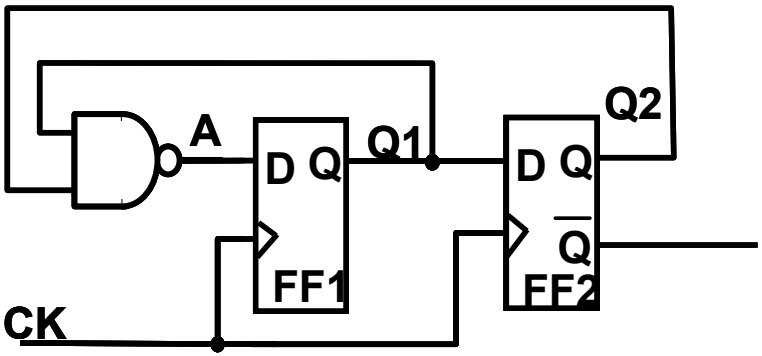
The most stringent time constraint on the clock period T_{CK} is:

$$T_{CK} > T_{CK->Q} + T_{su} + T_{NAND} = 6 \text{ ns}$$

The **maximum clock frequency** F_{CKmax} is thus:

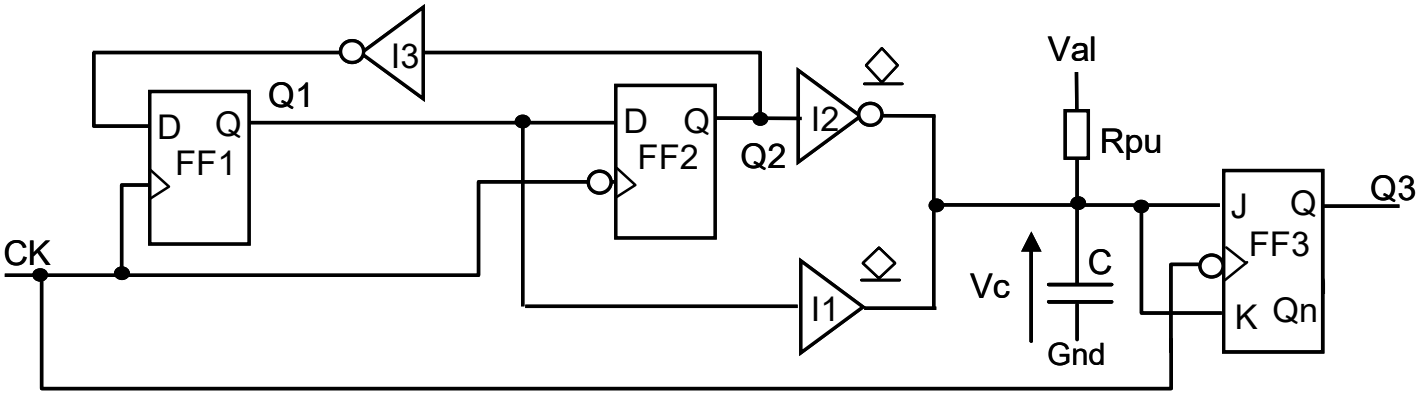
$$F_{CKmax} = 167 \text{ MHz}$$

Digital circuit



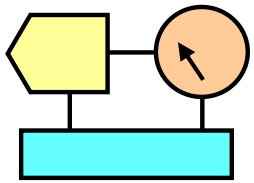
Problem 6 - Assignment
Sequential logic circuits
Timing diagrams

Consider the circuit shown in the figure. The FF outputs are initially set at 0; I1 and I2 have an open drain output.



a) Plot for at least two clock cycles the time diagrams at the nodes Q_1,Q_2, Q_3 and Vc quoting the delays and consider the following parameters:

CK period T_{CK} = 24 ns, C = 0
FF D: T_{CKQ} = 4 ns (both transitions), T_{su} = 2ns, T_h = 3 ns
FF JK :T_{CKQ} = 3ns (both transitions) , T_{su} = 3 ns, T_h = 2 ns
I1 and I2 inverter: $T_{LH1 = 6}$ ns, $T_{HL1 = 1}$ ns
I3 inverter: $T_{LH3 = 3}$ ns, $T_{HL3 = 4}$ ns



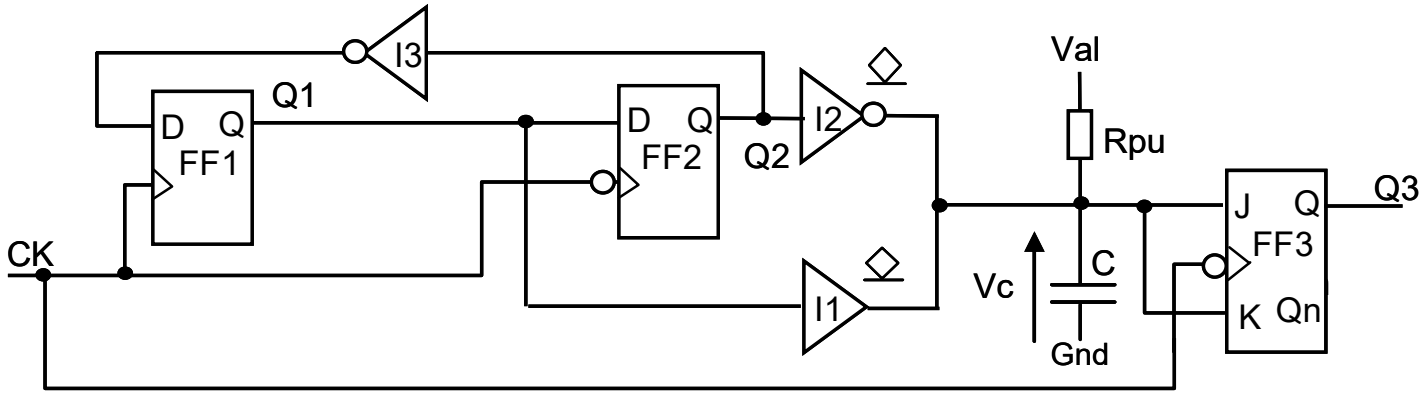
Cont.

c) Given the parameters of b), calculate the maximum clock frequency (consider C = 0).

d) Substitute I3 with a non-inverting buffer and move the input of I3 from Q_2 to Vc. Calculate in this new configuration the maximum clock frequency (with C = 0 and same parameters as in b). Discuss how C ≠ 0 changes the maximum clock frequency.

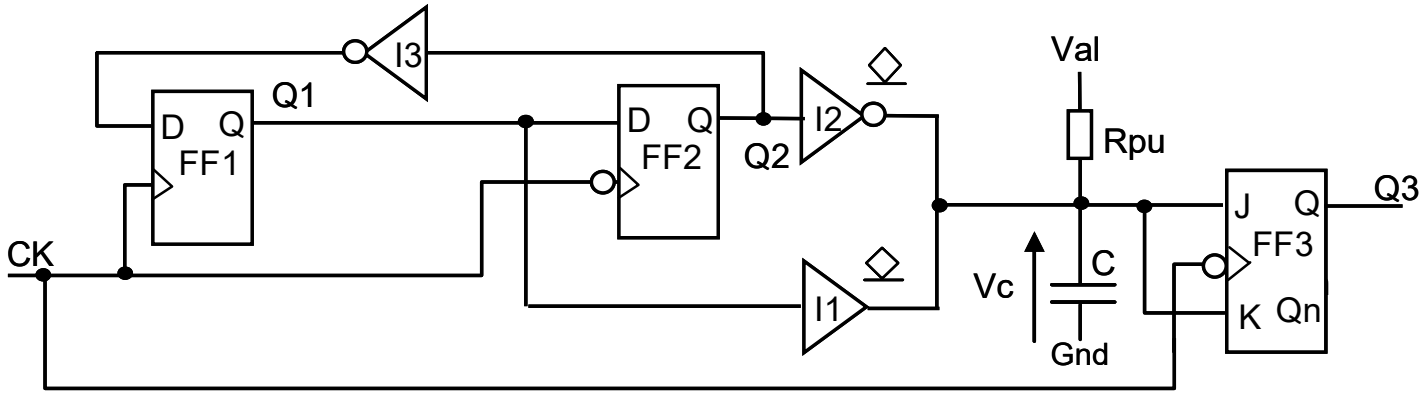
Problem 6a,b
Solution

- The system has a feedback **loop with two FFs**, therefore the system evolves in a cycle with 4 states maximum.



Problem 6a,b
Solution

- The system has a feedback **loop with two FFs**, therefore the system evolves in a cycle with 4 states maximum.
- The clock is active in the **L-H transition in the** FF1 and in **the H-L transition in the FF2**, therefore a cycle with the evolution through all the 4 states is concluded in two CK periods.



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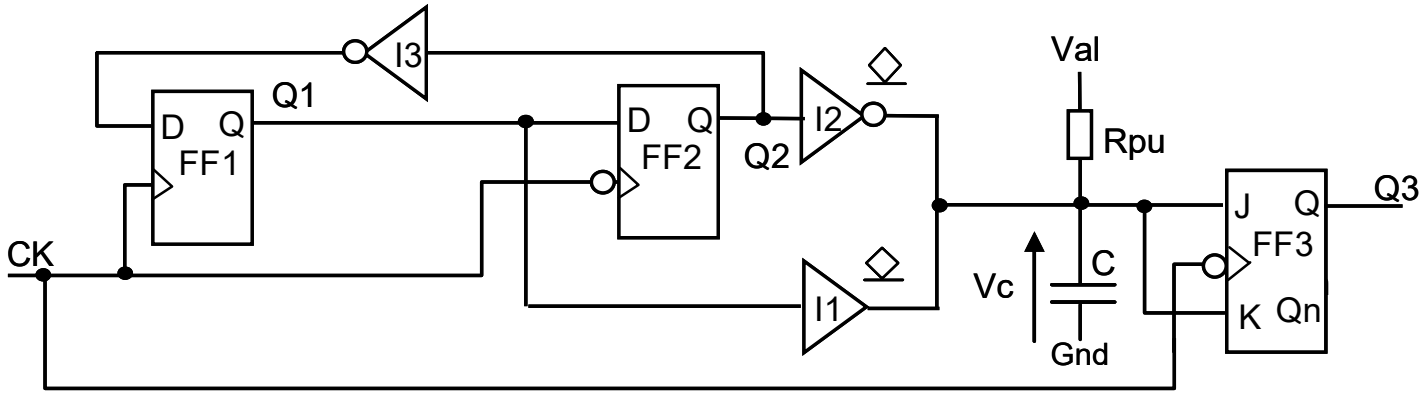
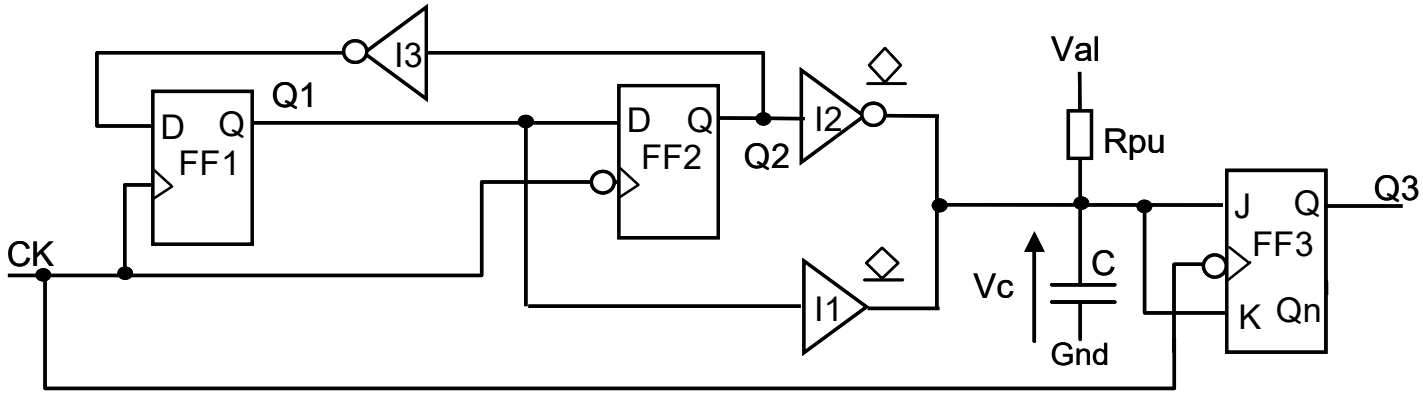
- The clock is active in the **L-H transition in the** FF1 and in **the H-L transition in the FF2**, therefore a cycle with the evolution through all the 4 states is concluded in two CK periods.
- The node Vc is a **wired-AND** of Q_1 and Q_2^*, therefore Vc is High only when we have the state $Q_1 = 1$ and $Q_2 = 0$. In the other 3 states of Q_1,Q_2, we have one of the outputs of I1 or I2 in the high impedance (HZ) state (I1 when $Q_1 = 0$, I2 when $Q_2 = 1$). In these cases the voltage Vc is determined by the connection to GND of the other output (I2 when I1 is HZ, I1 when I2 is HZ).



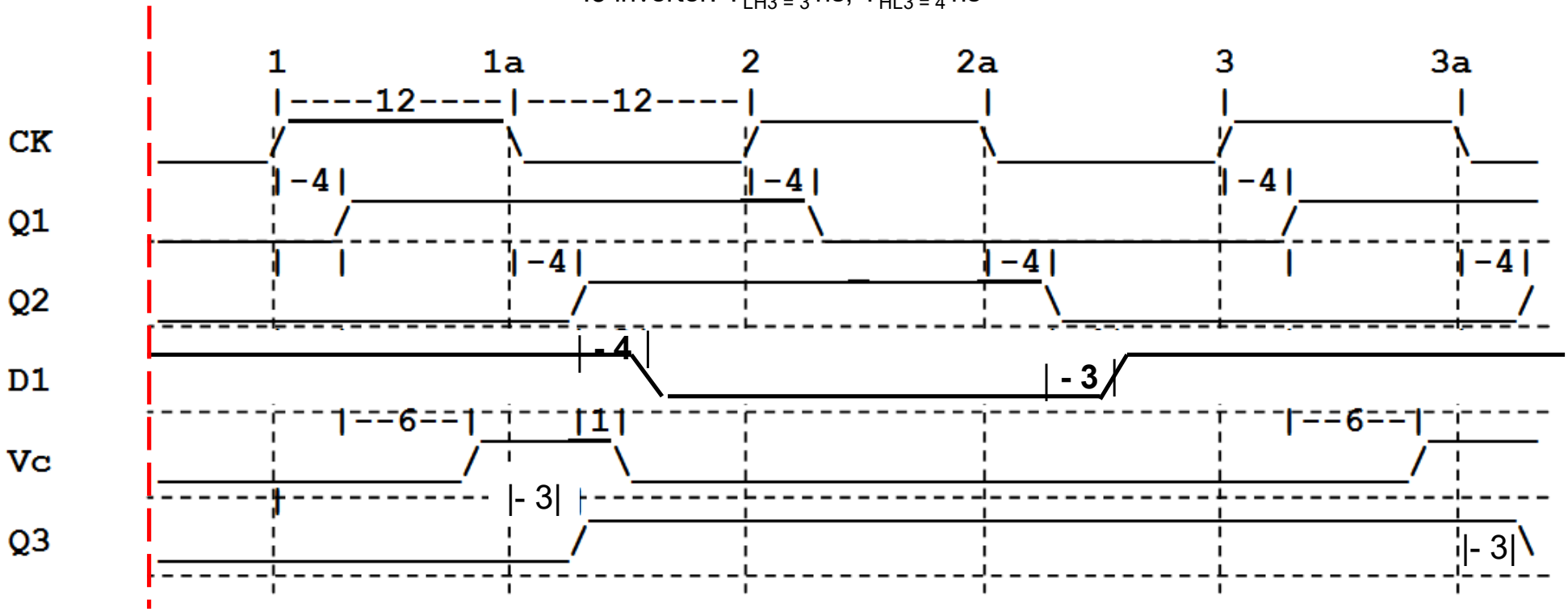
Problem 6a,b Solution

- The system has a feedback **loop with two FFs**, therefore the system evolves in a cycle with 4 states maximum.
- The clock is active in the **L-H transition in the** FF1 and in **the H-L transition in the FF2**, therefore a cycle with the evolution through all the 4 states is concluded in two CK periods.
- The node Vc is a **wired-AND** of Q_1 and Q_2*, therefore Vc is High only when we have the state $Q_1 = 1$ and $Q_2 = 0$ ($Q_2*=1$). In the other 3 states of Q_1,Q_2, we have one of the outputs of I1 or I2 in the high impedance (HZ) state (I1 when $Q_1 = 0$, I2 when $Q_2 = 1$). In these cases the voltage Vc is determined by the connection to GND of the other output (I2 when I1 is HZ, I1 when I2 is HZ).
- **FF3 is not part of the feedback loop**, therefore the output is only dependent on the voltage on Vc. Q3 changes the state (on the CK transition H->L) only when Vc is High.

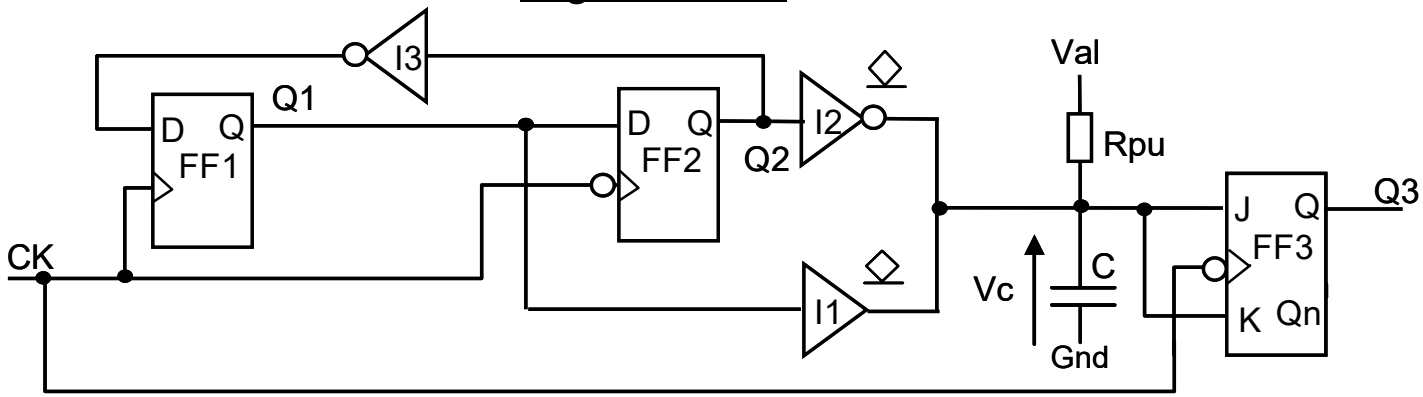


Problem 6a,b Solution

CK period T_{CK} = 24 ns, C=0
FF D: T_{CKQ} = 4 ns (both transitions)
FF JK :T_{CKQ} = 3 ns (both transitions)
I1 and I2 inverter: T_{LH1} = 6 ns, $T_{HL1 = 1}$ ns
I3 inverter: $T_{LH3 = 3}$ ns, $T_{HL3 = 4}$ ns



Digital circuit

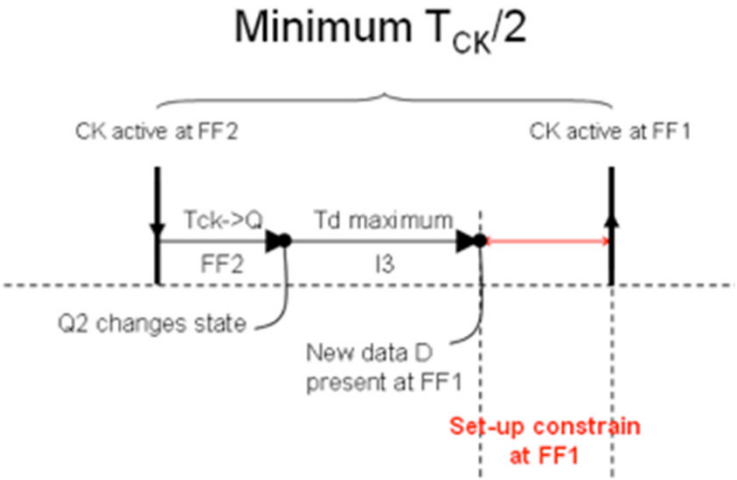


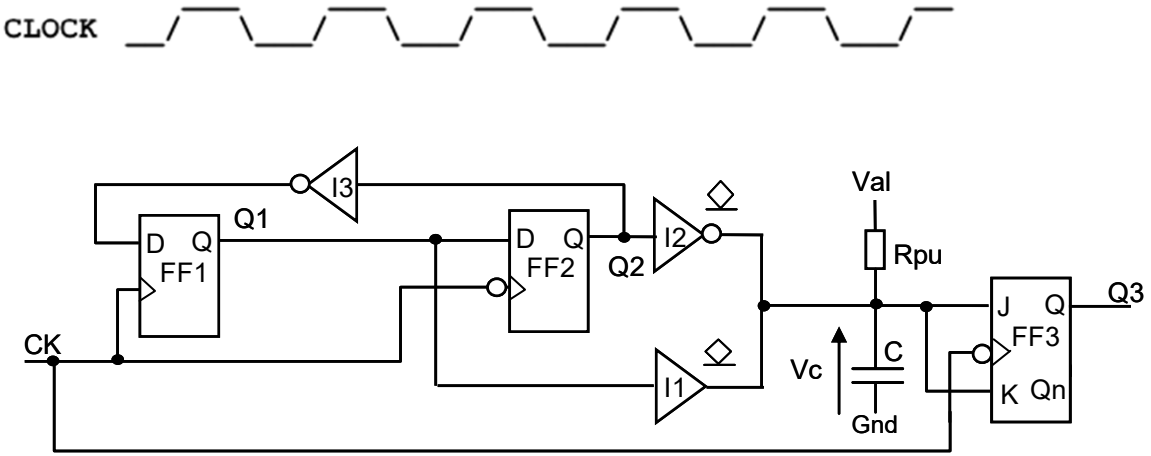
Problem 6c Solution

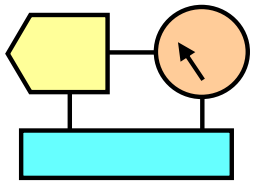
Considering the 3 FFs, we set constrain on T_{CK} or on $T_{CK}/2$ such that the set-up conditions are satisfied at each FF. For this circuit we have therefore **3 constrains** and the **maximum CK frequency is determined by the most stringent one** (i.e: the worst case). The worst case corresponds to the path producing the maximum delay across the combinational logic network.

Set-up constrain at FF1:

The data D is obtained by the output Q_2 (present after the H->L CK transition) and further delayed by I3 as shown in the following scheme:







Problem 6c Solution

As consequence we have that the maximum delay across the FF2 + combinational logic network must be lower than $T_{CK}/2$ minus the set-up time:

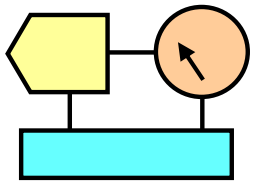
$$T_{CKQFF2} + T_{dmaxl3} < \frac{T_{CK}}{2} - T_{suFF1} \quad \text{(eq. 1)}$$

Then, we get:

$$T_{CK} > 2\,(T_{CKQFF2} + T_{HL3} + T_{suFF1})$$

Note that:
- We use for T_{dmaxl3} the propagation time T_{HL3} because it the longest one
- We have the factor 2 because the FF1 and FF2 are active on different CK edges; if they where active on the same edge, eq. (1) would have applied over a CK period and not over a half-period.

With the given values: $T_{CK} > 2\,(4\text{ ns} + 4\text{ ns} + 2\text{ ns}) = 20\text{ ns}$



Problem 6c Solution

Set-up constrain at FF2:

In a similar way we write in eq. (2) the set-up condition for FF2. This is less stringent than eq. (1), because we do not have any additional delay over any combinational network (i.e: the input D of FF2 is directly Q_1 of FF1). Q_1 switches at the CK transition L->H after a delay T_{CKQFF1}, therefore:

$$T_{CKQFF1} < \frac{T_{CK}}{2} - T_{suFF2} \Rightarrow T_{CK} > 2\,(4\text{ ns} + 2\text{ ns}) = 12\text{ ns} \quad \text{(eq. 2)}$$

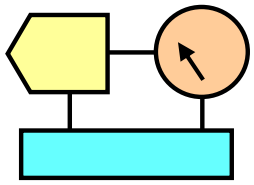
Set-up constrain at FF3:

In this case the delays to consider are the one through FF1 and the inverter I1 or through FF2 and the inverter I2.

We get as the most stringent constraint:

$$T_{CKQFF1} + T_{dmaxI1} < \frac{T_{CK}}{2} - T_{suFF3} \Rightarrow T_{CK} > 2\,(4\text{ ns} + 6\text{ ns} + 3\text{ ns}) = 26\text{ ns} \quad \text{(eq. 3)}$$

In conclusion the most stringent constrain on T_{CK} is given by eq. (3) with $T_{CK} > 26$ ns and then the **maximum CK frequency** is: $F_{CKmax} = 38.5$ MHz



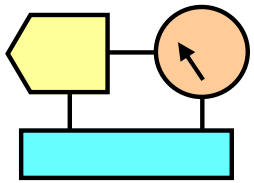
Problem 6d Solution

Moving the input of I3 to the node Vc, we add an additional delay due to I2. The set-up condition for FF1 becomes:

$$T_{CKQFF2} + T_{dmaxI3} + T_{dmaxI2} < \frac{T_{CK}}{2} - T_{suFF1} \quad \text{(eq. 1)}$$

Therefore we obtain: $T_{CK} > 2\ (4\ ns + 4\ ns + 6\ ns + 2\ ns) = 32\ ns$ and then the maximum frequency becomes: $\boxed{F_{CKmax} = 31.25\ MHz}$

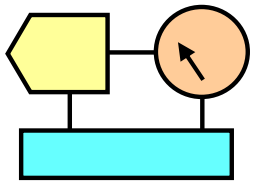
The capacitor C (neglected in the previous points of this exercise) causes an increased delay due to the increase of both T_{HL1} and T_{LH1} and reduces the F_{CKmax}.



Problem 7 – Assignment
Finite State Machine

a) Design a FSM (Finite State Machine) that acts as 2 bit counter triggered by an input signal T (i.e: the counter advances of 1 (base 10) every time T =1; the counter does not advance if T=0)

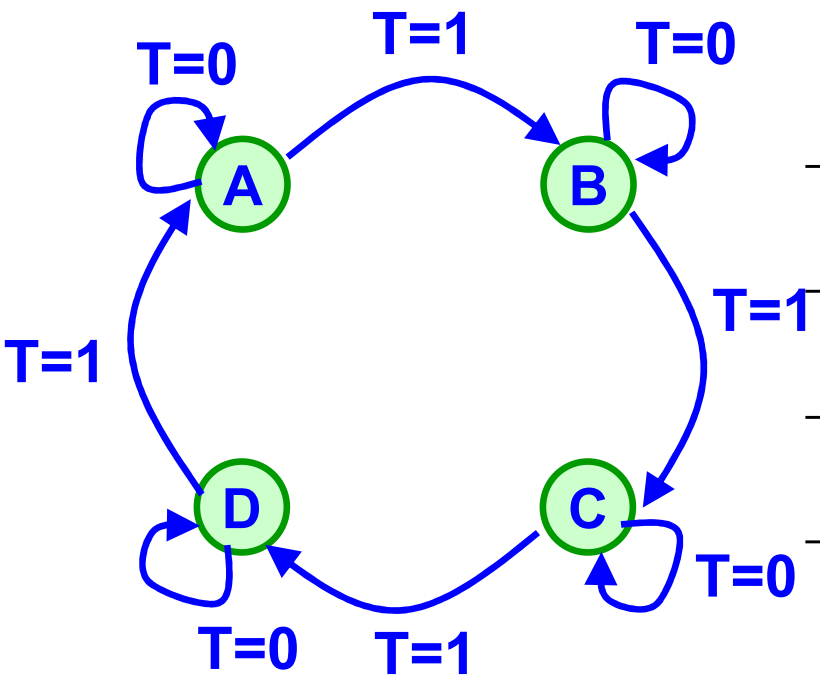
b) Calculate the maximum CK frequency



Problem 7a Solution

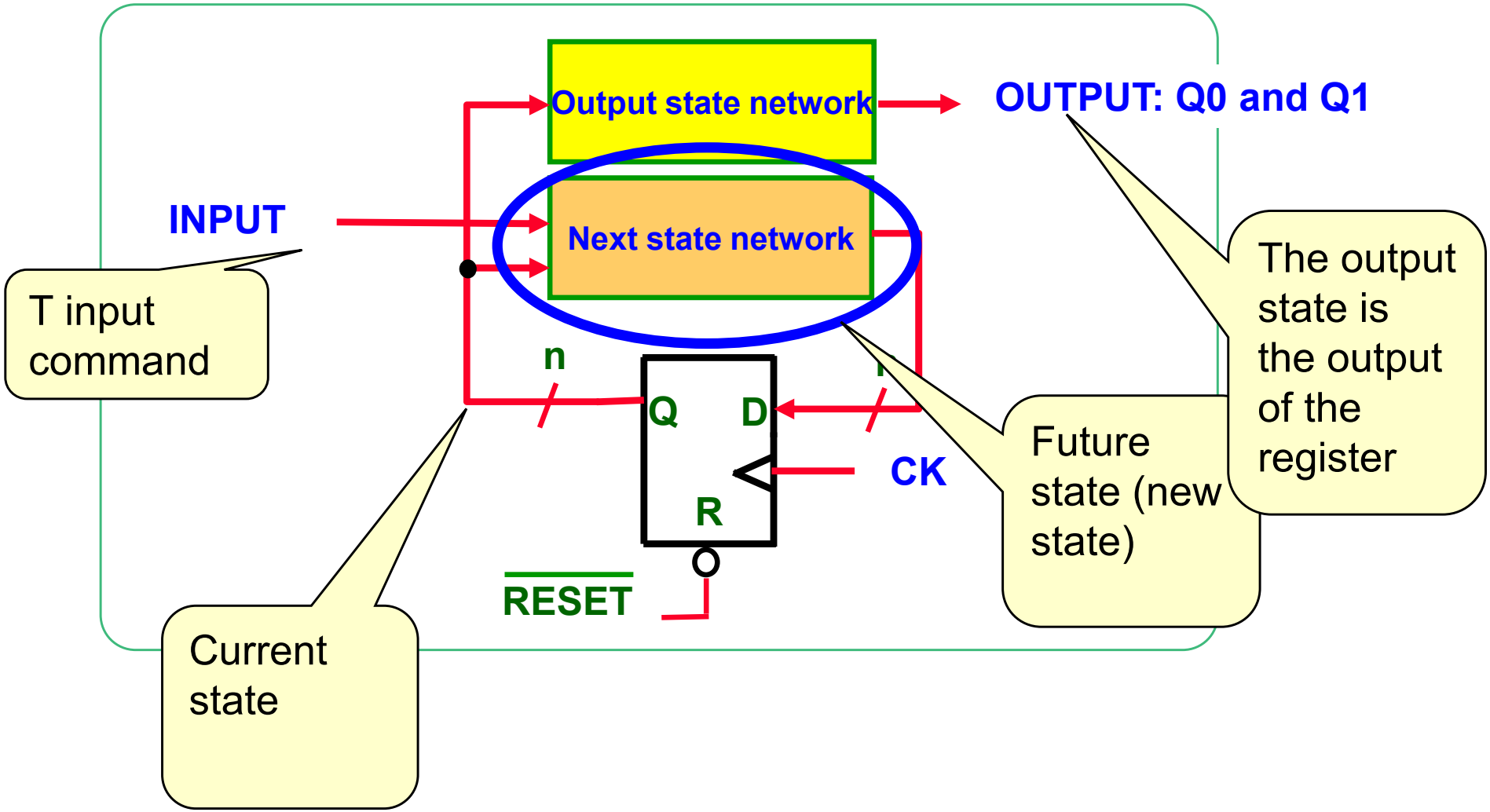
2 bit counter $\Longrightarrow$ number of different states: $2^2 = 4$

FSM states:



STATE	Q_1	Q_0	
A	0	0	Out = 0
B	0	1	Out = 1
C	1	0	Out = 2
D	1	1	Out = 3

Problem 7a
Solution
FSM machine bocks

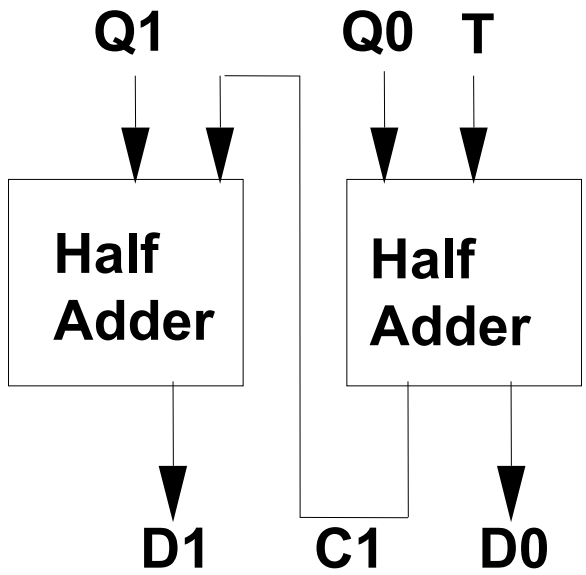


Problem 7a
Solution
Next state (Future state) circuit

The circuit generates the future state (represented by D_0,D_1) given the current state (represented by Q_0 and Q_1)

- If T=0 ➔ the circuit remains in the current state
- If T=1 ➔ current state +1 (the circuit moves to next state)
- Circuit: Adder controlled by T

$D_0 = Q_0$ XOR T
$C_1 = Q_0$ AND T
$D_1 = Q_1$ XOR C_1



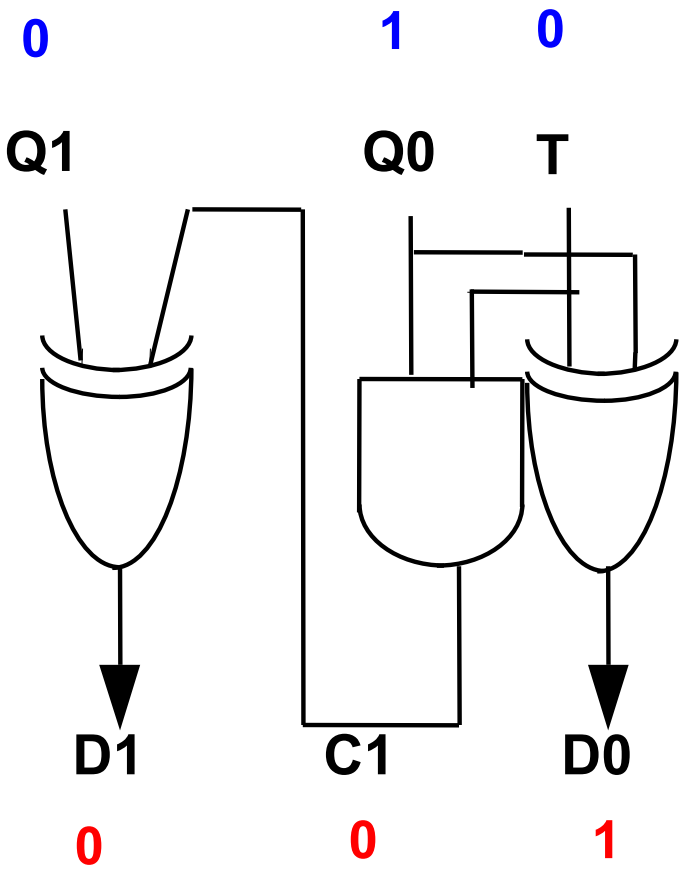
Problem 7a
Solution
Adder circuit

$OUT = Q_1 2^1 + Q_0 2^0 = 0*2^1 + 1*2^0 = 1 = B$

$OUT = D_1 2^1 + D_0 2^0 = 0*2^1 + 1*2^0 = 1 = B$

XOR truth table

Input		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	0



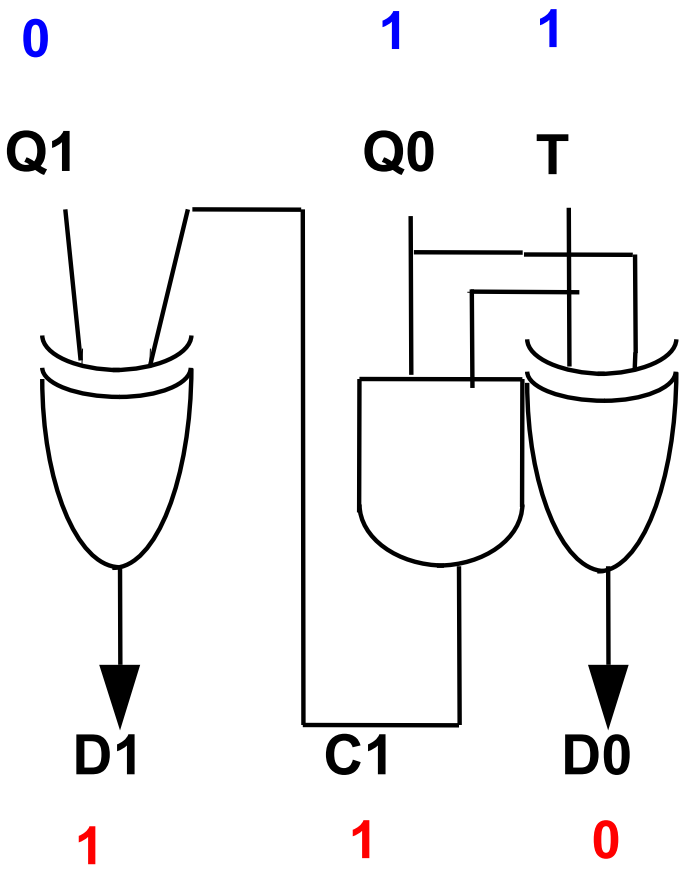
Problem 7a
Solution
Adder circuit

$OUT = Q_1 2^1 + Q_0 2^0 = 0*2^1 + 1*2^0 = 1 = B$

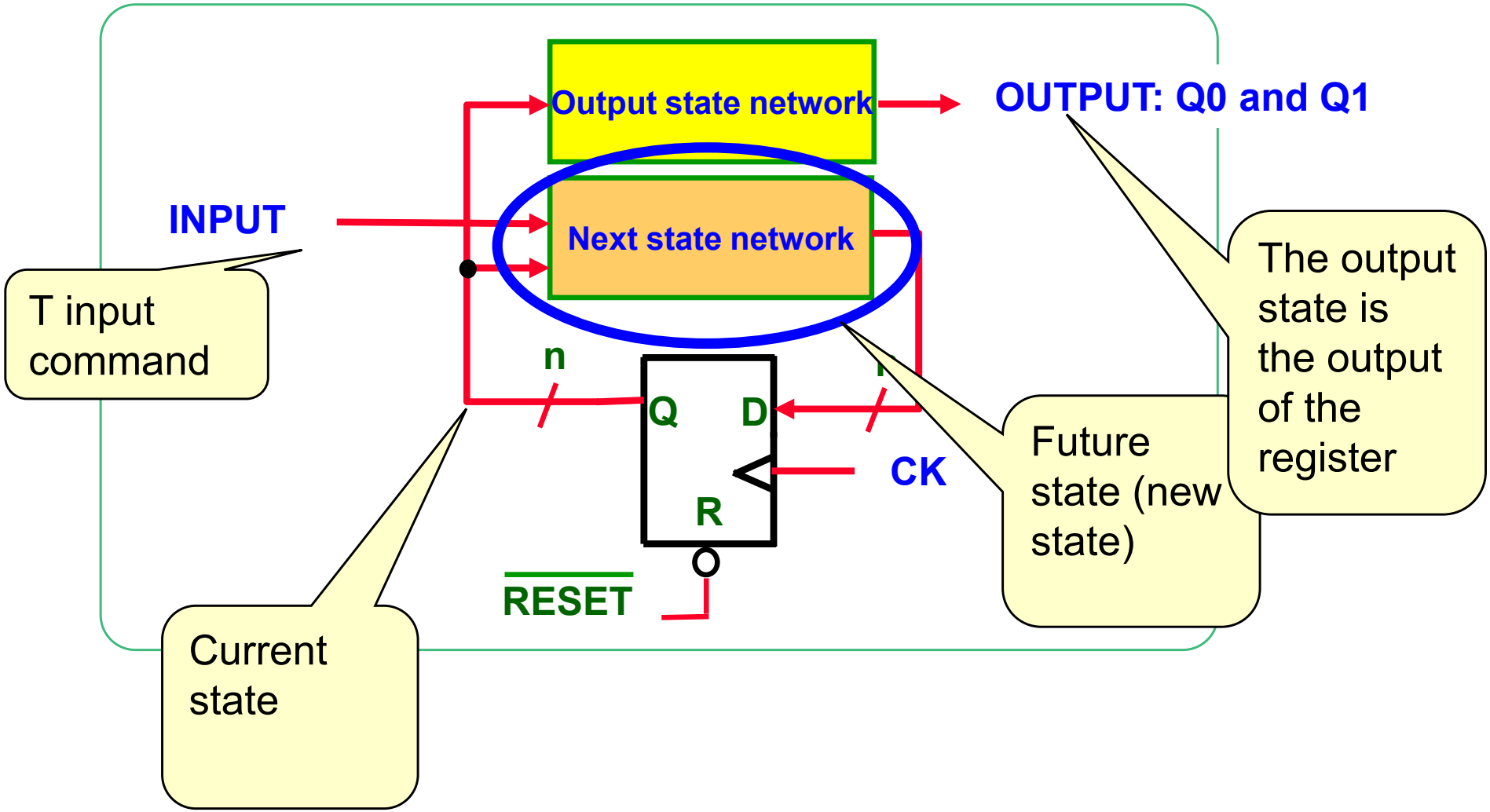
$OUT = D_1 2^1 + D_0 2^0 = 1*2^1 + 0*2^0 = 2 = C$

XOR truth table

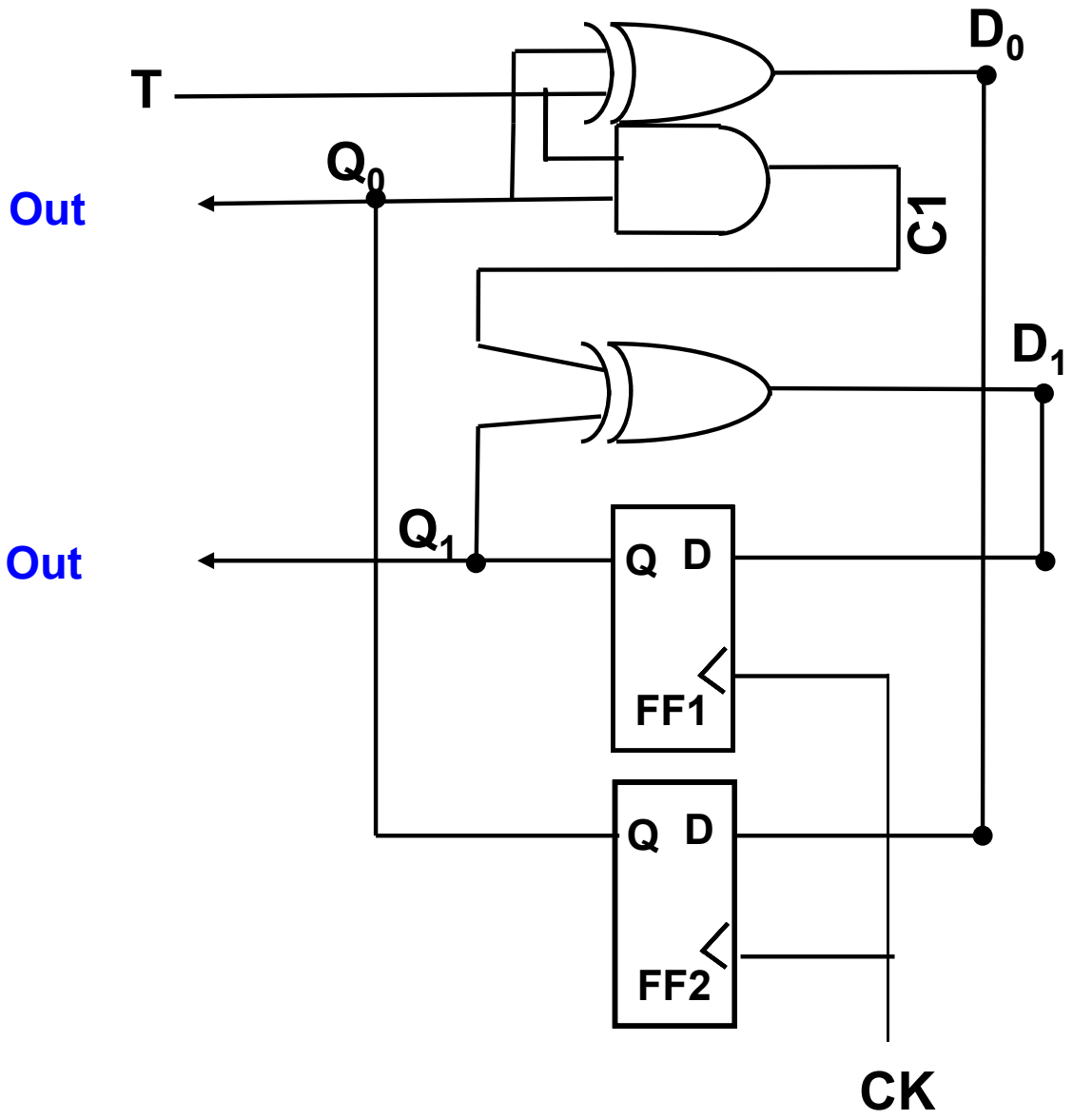
Input		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	0



Problem 7a
Solution
FSM machine bocks



Problem 7a
Solution
FSM machine: final circuit



Problem 7b Solution
Maximum operation frequency

The maximum operation frequency $F_{CKmax} = 1/T_{CKmin}$ is linked to:

- FF Delay CK → Q: T_{CKQ}
- Combinational circuit delay: T_{CL}
- FF set up time: T_{su}

Than:

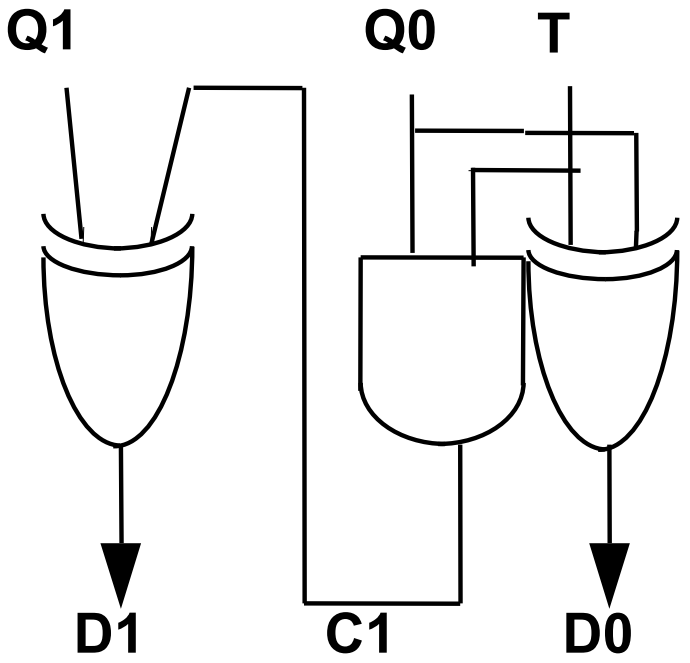
$$T_{CKQ} + T_{CLmax} + T_{su} = T_{CKmin}$$

Since the next state logic is:

$D_0 = Q_0$ XOR T
$C_1 = Q_0$ AND T
$D_1 = Q_1$ XOR C_1

we get:

$$T_{CLmax} = T_{AND} + TXOR$$



Problem - Assignement
Square wave generator

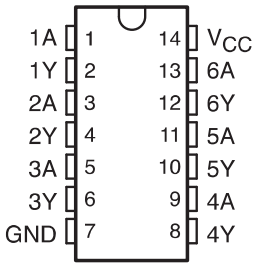
Design a square wave generator with frequency 50 KHz using a Schimtt trigger inverter 74HC14

SN54HC14, SN74HC14
HEX SCHMITT-TRIGGER INVERTERS

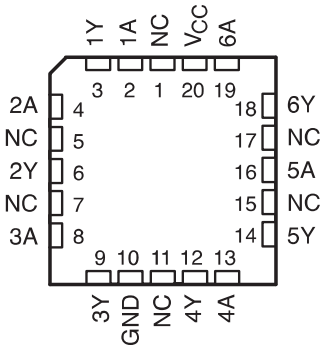
SCLS085E – DECEMBER 1982 – REVISED NOVEMBER 2004

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 11 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC14 . . . J OR W PACKAGE
SN74HC14 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



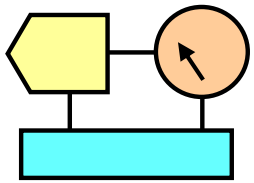
SN54HC14 . . . FK PACKAGE
(TOP VIEW)



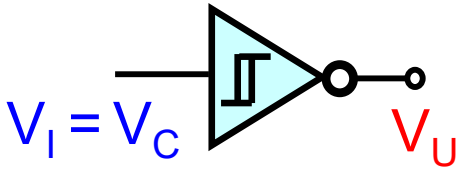
NC – No internal connection

description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

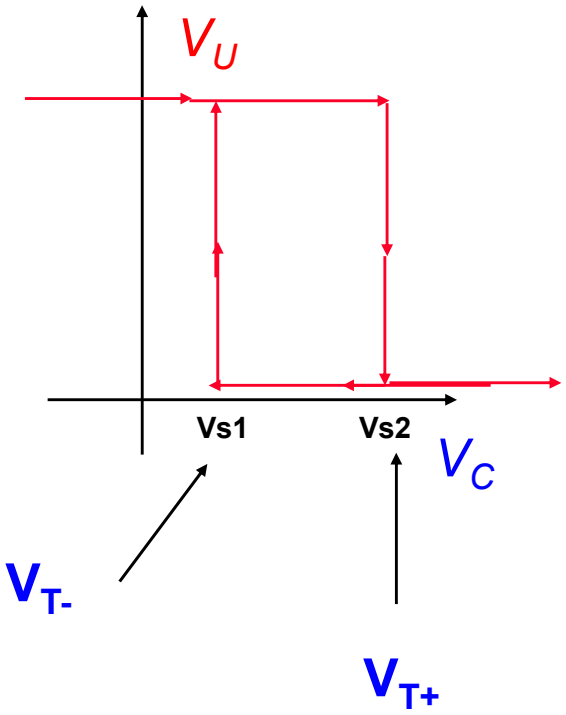


Transcharacteristic of the Schmitt trigger



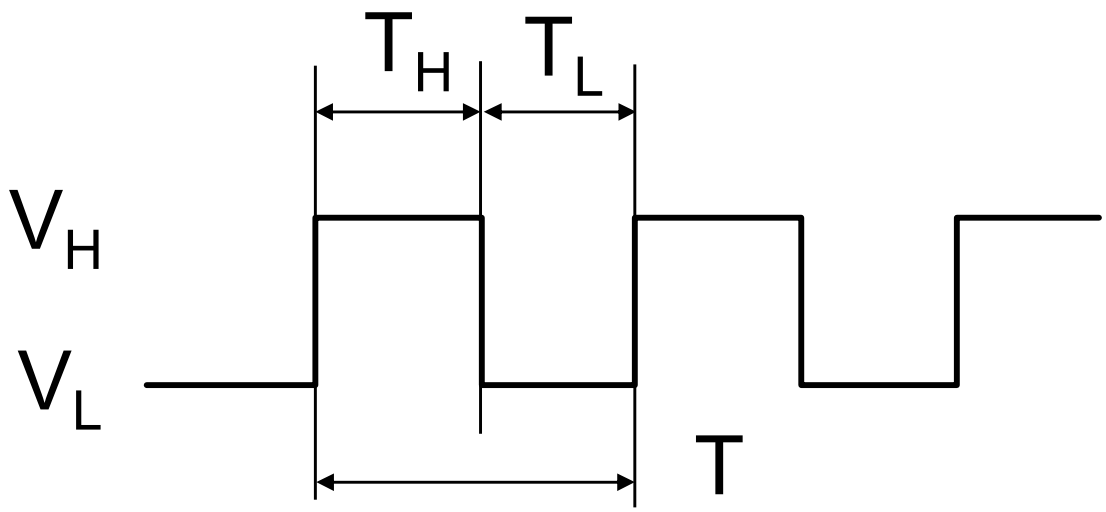
- 74HC14
  - Thresholds $V_{T\pm}$ is dependent on supply voltage V_{CC}
  - Values spred in a wide range

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST
		74HCT								
		+25			–40 to +85		–40 to +125			V_{CC} (V)
		min.	typ.	max.	min.	max.	min.	max.		
V_{T+}	positive-going threshold	1.2 1.4	1.41 1.59	1.9 2.1	1.2 1.4	1.9 2.1	1.2 1.4	1.9 2.1	V	4.5 5.5
V_{T-}	negative-going threshold	0.5 0.6	0.85 0.99	1.2 1.4	0.5 0.6	1.2 1.4	0.5 0.6	1.2 1.4	V	4.5 5.5
V_H	hysteresis ($V_{T+} - V_{T-}$)	0.4 0.4	0.56 0.60	– –	0.4 0.4	– –	0.4 0.4	– –	V	4.5 5.5

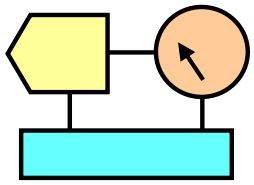


Problem
Theoretical remind

Binary signal: periodic repetition of high and low levels



Parameters:		
	Voltage levels:	V_H, V_L
	Period:	T
	Frequency:	$f = 1/T$
	Duty Cycle:	$DC = T_H/T$

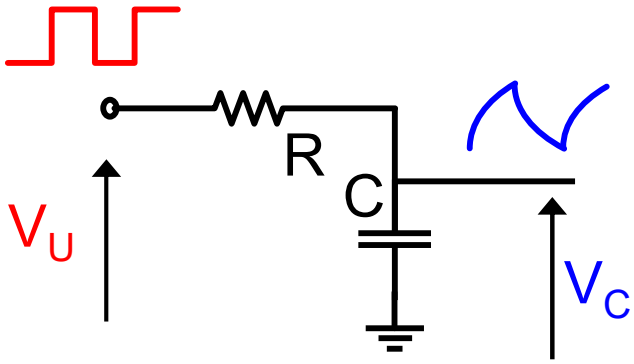


Digital Circuit for the generation of square wave signal:

- ANALYSIS
- DESIGN

Example: it can be used to generate the **clock signal (CK)** for digital counters

1 ingredient: RC filter



- The low pass RC filter is driven by a digital signal (input to V_H or V_L)

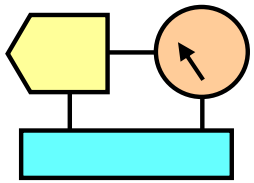
  The capacitor is charged/discharged with exponetial law

1. Capacitor discharge (t=0, $V_C = V_H$)

   $V(t) = V_H e^{-t/RC}$ (V_L=0)

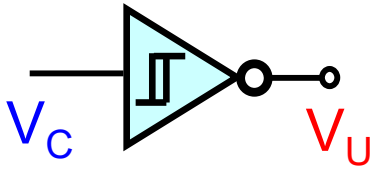
2. Capacitor charge (t=0, $V_C = V_L = 0$)

   $V(t) = V_H \left(1 - e^{-t/RC}\right)$

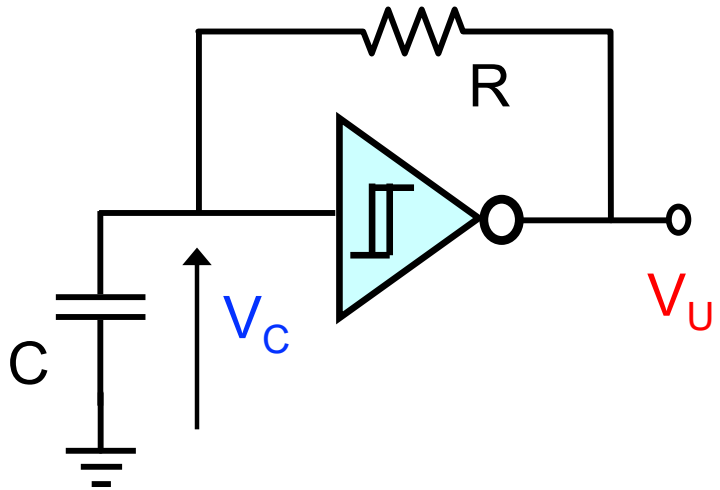


2 ingredient: Comparator circuit

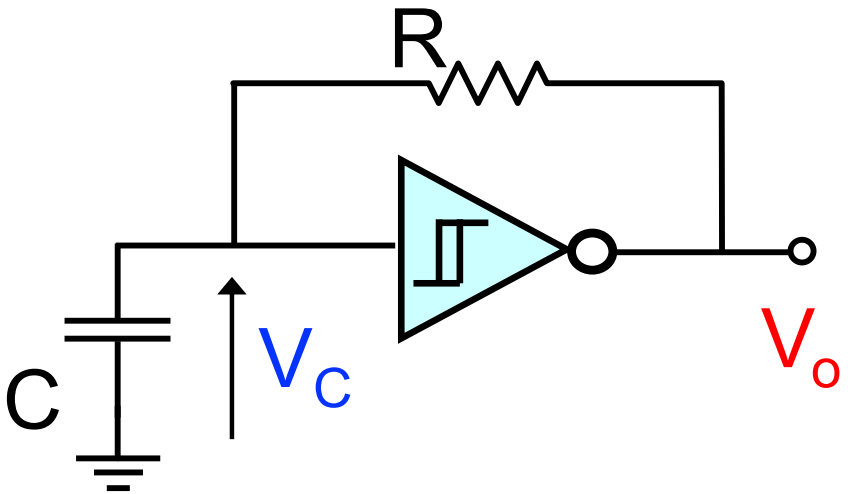
- The voltage V_C is compared with the **comparator** thresholds
  - The **comparator**, i.e. **Schmitt trigger inverter,** has hysteresis



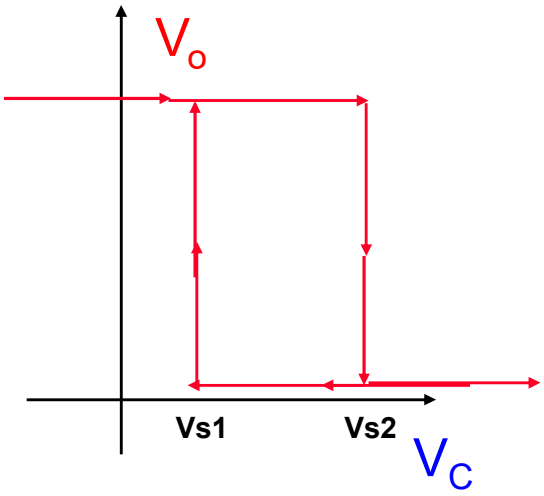
- The output of the comparator drives the RC circuit



Square wave oscillator

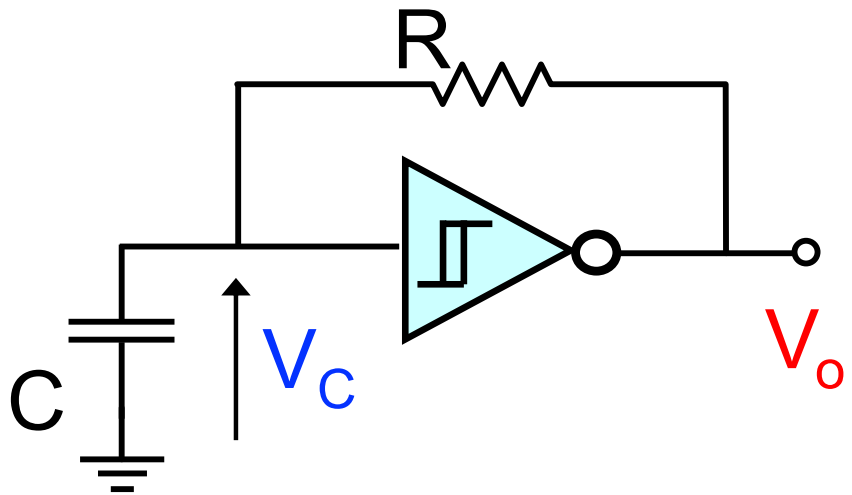


The capacitor is **charged** or **discharged** by the output current of the trigger comparator. The capacitor voltage varies between V_{s1} and V_{s2}

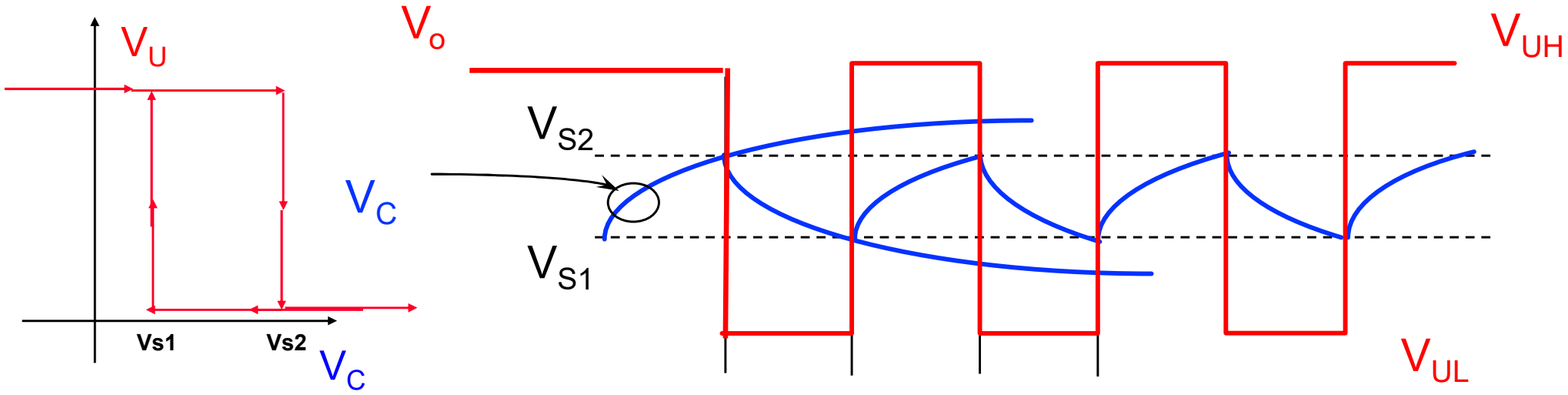


Assume that at t=0: $V_C = 0 \Longrightarrow$ no charge on the capacitance $\Rightarrow V_U = V_{UH}$

Square wave oscillator



The capacitor is **charged** or **discharged** by the output current of the trigger comparator. The capacitor voltage varies between V_{s1} and V_{s2}



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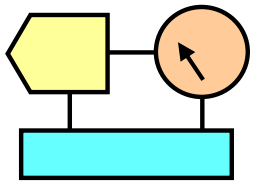
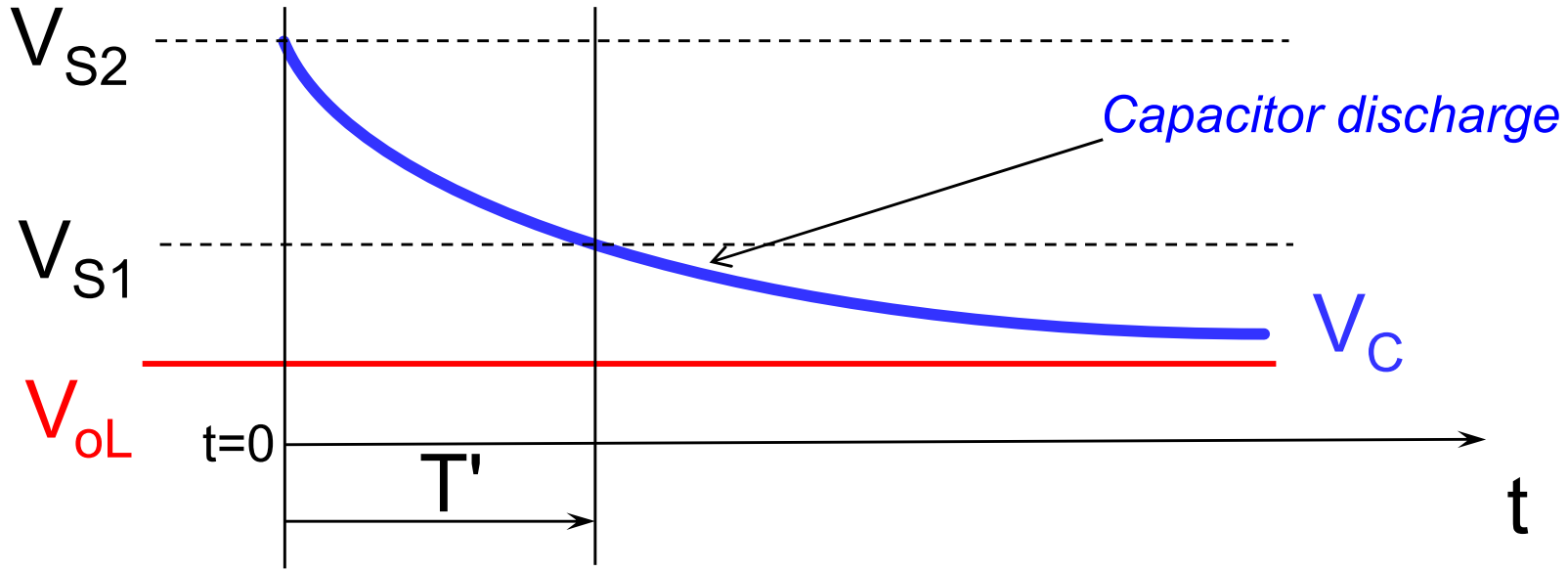
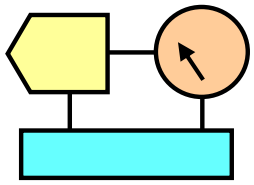


Problem Solution

Calculation of the square wave period

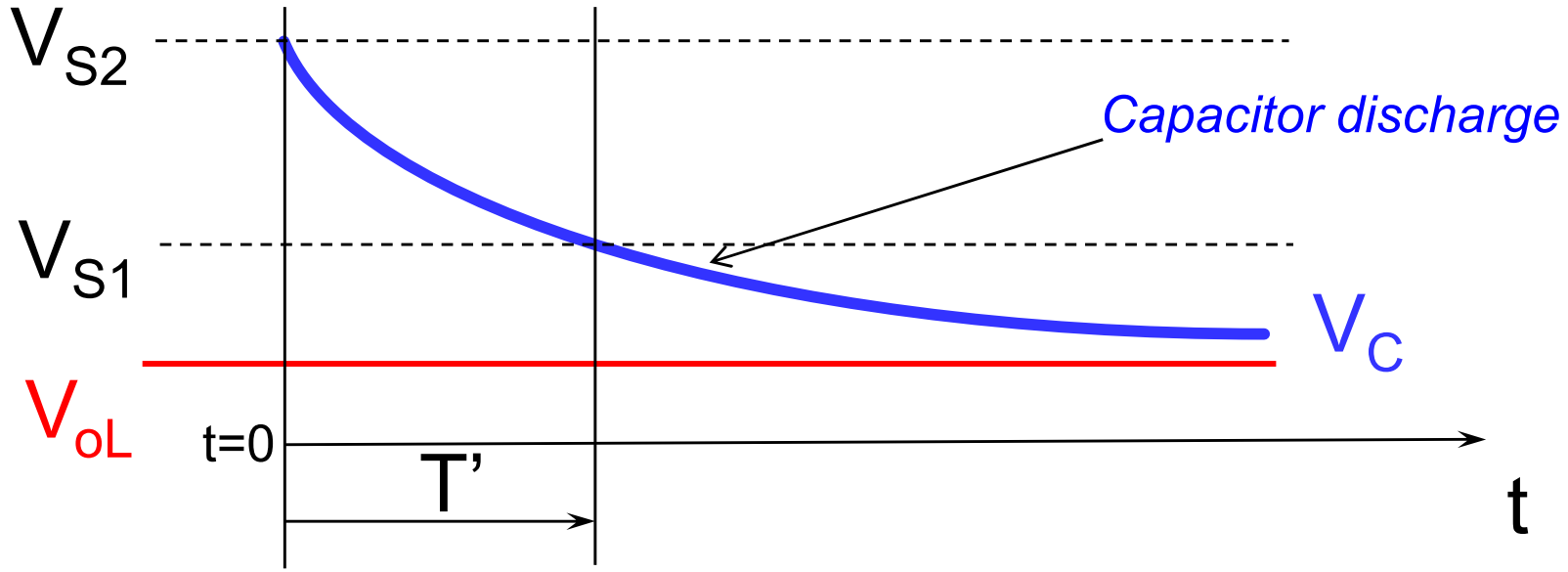


Since the voltage across the capacitor is: $V_C(t) = V_{UL} - (V_{UL} - V_{S2})e^{-t/RC}$



Problem Solution

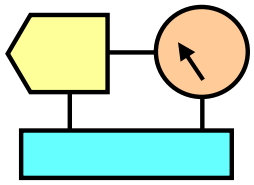
Calculation of the square wave period



$$V_C(t) = V_{oL} - (V_{oL} - V_{S2})e^{-t/RC}$$

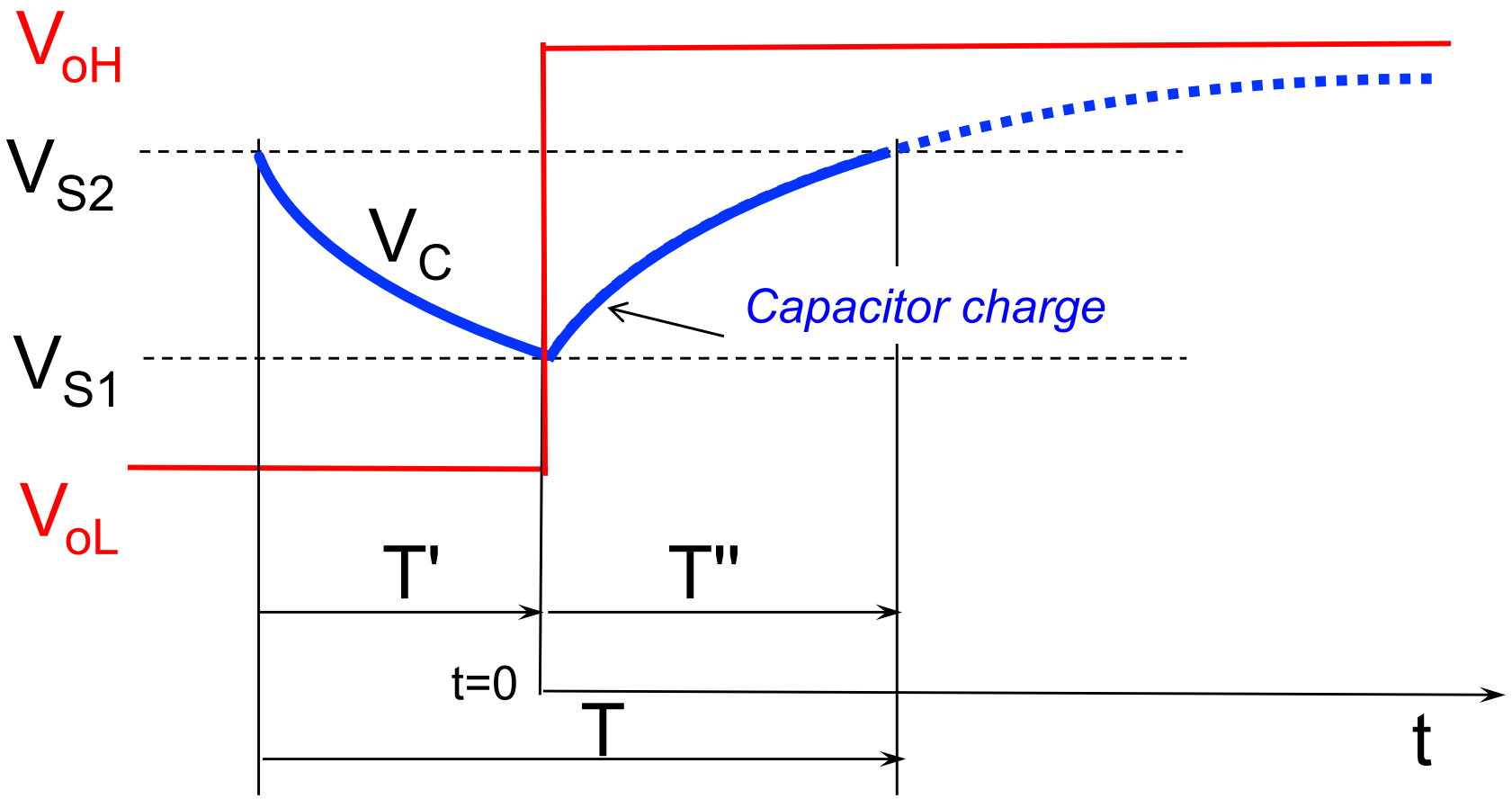
Then the T' interval is given by:

$$V_{S1} = V_{oL} - (V_{oL} - V_{S2})e^{-T'/RC} \Rightarrow T' = RC\ln\left[\frac{(V_{oL} - V_{S2})}{(V_{oL} - V_{S1})}\right]$$



Problem Solution

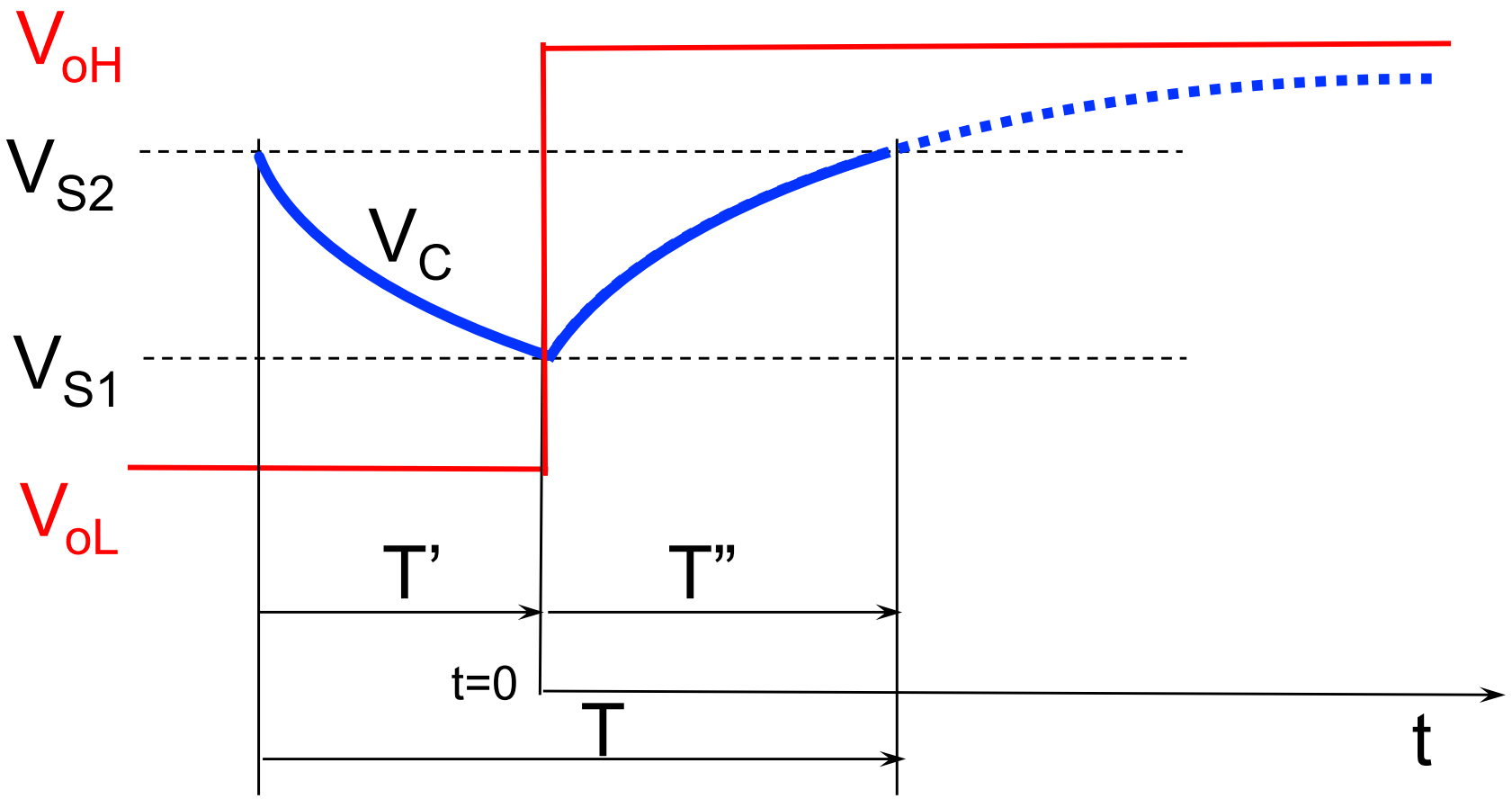
Calculation of the square wave period



Since the voltage across the capacitor is:

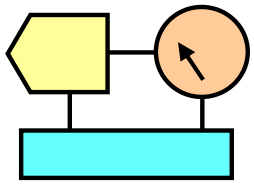
$$V_C(t) = V_{oH} - (V_{oH} - V_{S1})e^{-t/RC}$$

Calculation of the square wave period



$V_C(t)=V_{oH}-(V_{oH}-V_{S1})e^{-t/RC}$ Then the T" interval is given by:

$$V_{S2} = V_{oH}-(V_{oH}-V_{S1})e^{-T''/RC} \Rightarrow T'' = RC\ln\left[\frac{(V_{oH}-V_{S1})}{(V_{oH}-V_{S2})}\right]$$



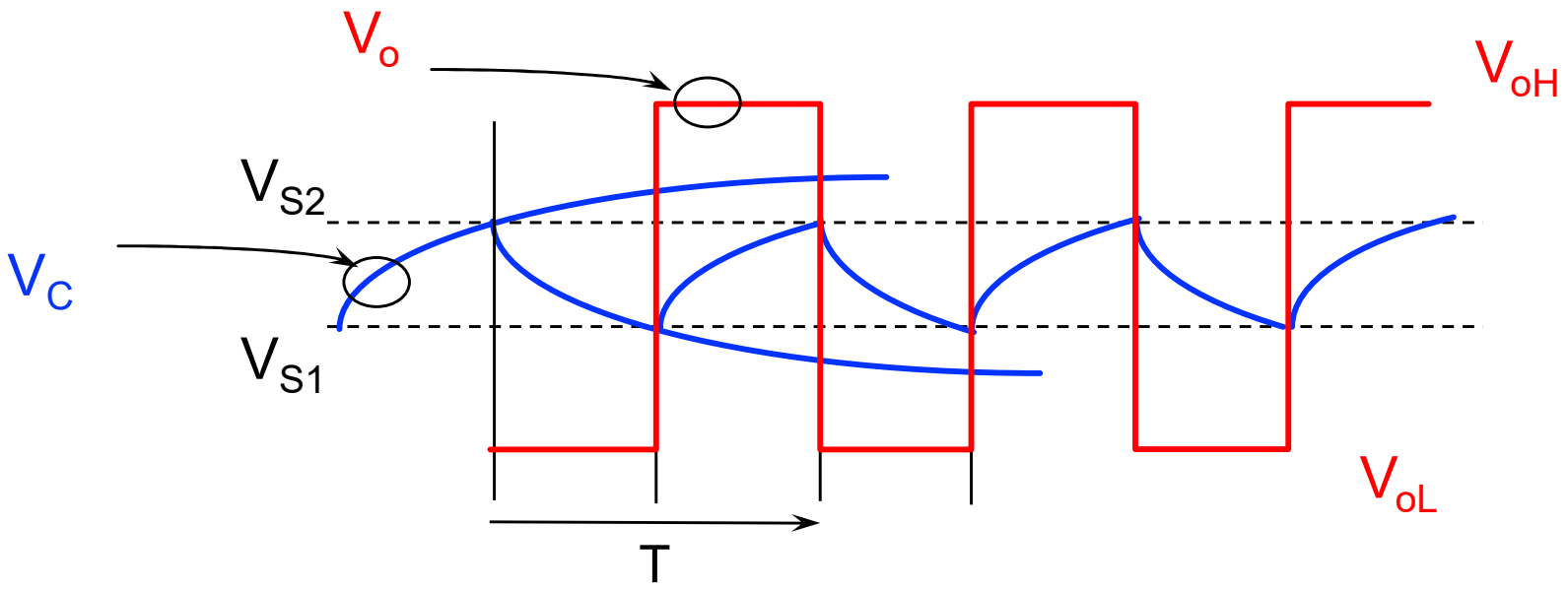
Problem Solution

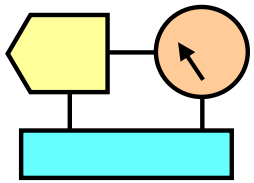
Calculation of the square wave period

Finally we get:

$$T=T'+T'' = RC\ln\left[\frac{(V_{oL}-V_{S2})}{(V_{oL}-V_{S1})}\right]+RC\ln\left[\frac{(V_{oH}-V_{S1})}{(V_{oH}-V_{S2})}\right]$$

$$T= RC\ln\left[\frac{(V_{oL}-V_{S2})(V_{oH}-V_{S1})}{(V_{oL}-V_{S1})(V_{oH}-V_{S2})}\right]$$





Problem Solution

Calculation of the square wave period

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			2		40		20	µA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		32		26	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

From the Datasheet for V_{CC}= 4.5 V:

$$V_{T-} = V_{S1} = 1.6V$$
$$V_{T+} = V_{S2} = 2.5V$$
$$V_{OH} = 4.3V$$
$$V_{OL} = 0.17V$$

In order to have a square wave frequency of 50 kHz that corresponds to T = 1/50 ms = 20 µs we then must require that:

$$RC \cong 22\ \mu s \overset{\text{e.g.}}{\Longrightarrow} \begin{cases} R = 10\ k\Omega \\ C = 2.22\ nF \end{cases}$$