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文档编号:(芯片型号) –ASR6501(英文、数字)

# ASR6501 Datasheet

| | | |
|---|---|---|
| 文件状态：<br>[√] 正在修改<br>[　] 正式发布 | 当前版本： | V0.8 |
| | 作者： | ASR6501 Design Team |
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| | 审核： | |
| | 完成日期： | 2018-11-27 |



翱捷科技（上海）有限公司

ASR Microelectronics Co., Ltd

# 版本历史

| 版本号 | 修改日期 | 作 者 | 修 改 说 明 |
|---|---|---|---|
| V0.1 | 2018.05.16 | ASR6501 Design Team | Created |
| V0.2 | 2018.05.22 | ASR6501 Design Team | 1. Change the package size to 6mm x 6mm x0.9mm<br>2. Add current in Tx 17dBm output Spec. |
| V0.3 | 2018.05.23 | ASR6501 Design Team | 1. Remove module information.<br>2. Change the SRAM from 4kBytes to 16kBytes. |
| V0.4 | 2018.05.31 | ASR6501 Design Team | 1. Change 1.2 Block diagram DIO direction. |
| V0.5 | 2018.07.05 | ASR6501 Design Team | 1. Change XRES pin function description. |
| V0.6 | 2018.08.03 | ASR6501 Design Team | 1. Change RX current from 15mA to 11mA. |
| V0.7 | 2018.09.13 | ASR6501 Design Team | 1. Add deepsleep current without RF Config Retention and without RTC mode current.<br>2. Update RX mode current to 10mA.<br>3. Update TX mode current at TX OPT mode results. |
| V0.8 | 2018.11.27 | ASR6501 Design Team | 1. Add some pin usage forbiddens. |

# Table of Contents

# 1 General Description

The ASR6501 is a general LoRa Wireless Communication Chipset, with integrated LoRa Radio Transceiver, LoRa Modem and a 32-Bit RISC MCU. The MCU uses ARM Cortex M0+, with 48MHz operation frequency. The LoRa Radio Transceiver has continuous frequency coverage from 150MHz to 960MHz. The LoRa Modem supports LoRa modulation for LPWAN use cases and (G)FSK modulation for legacy use cases. The LoRa Wireless Communication module designed by ASR6501 provides ultra long range, ultra low power communication for LPWAN application.

The ASR6501 can achieve a high sensitivity of over -140dBm and the maximum transmit power is higher than +21dBm. This makes it suitable to be used in long range LPWAN and have high efficiency. The total chip package is of very small size, 6mm x 6mm.

## 1.1 Key Feature

- Small footprint: 6mm x 6mm x 0.9mm.
- LoRa Radio and LoRa Modem.
- Frequency Range: 150MHz ~ 960MHz.
- Maximum Power +21dBm constant RF output.
- High sensitivity: down to -140dBm.
- Programmable bit rate up to 62.5kbps in LoRa modulation mode.
- Programmable bit rate up to 300kbps in (G)FSK modulation mode.
- Preamble detection.
- Embedded memories (up to 128kbytes of Flash memory and 16Kbytes of SRAM).
- 6x configurable GPIOs, 1xI2C, 1xUART, 1xSWD.
- 48-MHz ARM Cortex-M0+ CPU.
- 8-Channel DMA engine.
- Embedded 12-bit 1Msps SAR ADC.
- 32.768kHz External Watch Crystal Oscillator.
- 4-33MHz External Crystal Oscillator for MCU (Optional).
- 32MHz External Crystal Oscillator for LoRa Radio.
- Embedded internal High frequency (48MHz) RC oscillator.
- Embedded internal Low frequency (40kHz) RC oscillator.
- Embedded internal PLL to generate 48MHz clock.

## 1.2 Block Diagram

Fig. 1.1 shows the block diagram of ASR6501 and the ASR LoRa Communication Module.

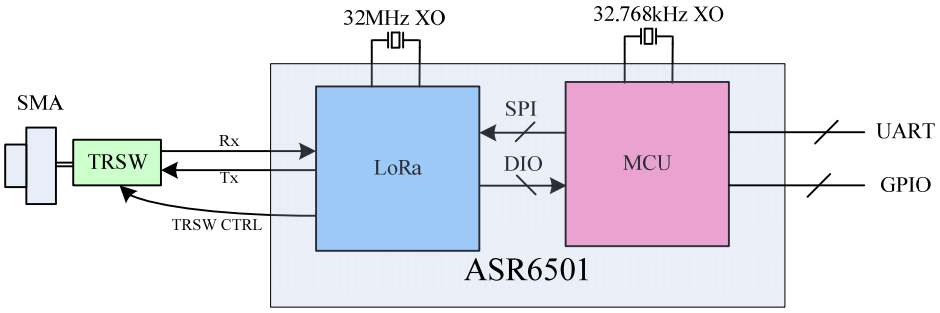



Fig. 1.1: The block diagram of ASR6501 and the ASR LoRa Communication Module

The module of LoRa Communication is designed by ASR6501 and also a reference design for customers. Customers could communicate with ASR6501 by UART and GPIO interfaces.

## 1.3 General Specification

Following Table 1.1 shows the general specifications of ASR6501 chipset and module.

Table 1.1 General specifications of ASR6501 chipset and module

| | |
|---|---|
| Chipset Name | ASR6501 |
| Module Name | ASR6501 LoRa Wireless Communication Module |
| Host Interface | UART, GPIO |
| Operation Conditions | |
| Temperature | ● Storage: -55C ~ +125C<br>● Operating: -40C ~ +85C |
| Humidity | ● Storage: 5 ~ 95% (Non-Condensing)<br>● Operating: 10 ~ 95% (Non-Condensing) |
| Dimension | 6mm x 6mm x 0.9mm |
| Package | QFN Type |

# 2 Electrical Characteristics

Electrical Characteristics include Absolute Maximum Ratings for the Chipset and Module, Recommended Operating Range and Power Consumption Characteristics. All the data are tested under demo board with fully matching and harmonic filtering networks.

## 2.1 Absolute Maximum Rating

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDD | Supply Voltage | -0.3 | | 3.9 | V |
| Vin | Digital Input Voltage Level | -0.3 | | 3.9 | V |
| Pin | RF Input Power | | | +10 | dBm |

## 2.2 Power Consumption Characteristics

| Symbol | Parameter | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| IDD_SL | Supply current in Sleep mode | Without RF Config Retention, without RTC | 2 | | uA |
| | | Without RF Config Retention, with RTC | 2.7 | | |
| | | With RF Config Retention and RTC | 3.1 | | uA |
| IDD_RX | Supply current in Receiver mode | | 10 | | mA |
| IDD_TX | Supply current in Transmitter mode | Pout=+22dBm | 108 | | mA |
| | | Pout=+22dBm(TX OPT) | 85 | | mA |
| | | Pout=+21dBm | 106 | | mA |
| | | Pout=+20dBm | 98 | | mA |
| | | Pout=+17dBm | 90 | | mA |

| | | | | | |
|---|---|---|---|---|---|
| | | Pout=+17dBm(TX OPT) | 52 | | mA |
| | | Pout=+14dBm | 78 | | mA |
| | | Pout=+10dBm | 59 | | mA |
| | | Pout=+5dBm | 47 | | mA |

## 2.3 Recommended Operating Range

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDD | Supply Voltage | 1.8 | 3.3 | 3.7 | V |
| Pin | RF Input Power | | | +10 | dBm |

## 2.4 RF Characteristics

The table 2.1 gives the electrical specifications for the LoRa RF transceiver operating with LoRa modulation. Following conditions apply unless otherwise specified:

- Supply Voltage = 3.3V.
- Temperature = 25C.
- Frequency bands: 470MHz.
- Bandwidth (BW) = 125kHz.
- Spreading Factor (SF) = 12.
- Coding Rate (CR) = 4/6.
- Package Error Rate (PER) = 1%.
- CRC on payload enabled.
- Payload length = 10bytes.
- Preamble Length = 12 symbols.
- With matched impedances.

Table 2.1: LoRa RF Transceiver Characteristics

| LoRa Transmitter RF Characteristics | | | | | |
|---|---|---|---|---|---|
| Items | Condition | Min. | Typ. | Max. | Unit |
| Frequency Range | | 150 | 470 | 960 | MHz |
| Tx Power | RFO Pin | 18 | 20 | 22 | dBm |
| LoRa Receiver RF Characteristics | | | | | |
| Items | Condition | Min. | Typ. | Max. | Unit |
| Frequency Range | | 150 | 470 | 960 | MHz |
| Sensitivity | 125kHz Bandwidth, SF=7 | | -126 | | dBm |
| | 125kHz Bandwidth, SF=10 | | -135 | | dBm |
| | 125kHz Bandwidth, SF=12 | | -140 | | dBm |
| 2nd order harmonic | Tx Power = 20dBm | | -41 | | dBm |

## 2.5 Digital Characteristics

### 2.5.1 DC Characteristics

| Symbol | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| VIH | I/O input high level | | 0.7xVDD | | | V |
| VIL | I/O input low level | | | | 0.3xVDD | V |
| RPU | Weak pull up resistor | Vin=GND | 30 | 45 | 60 | KΩ |
| RPD | Weak pull down resistor | Vin=VDD | 30 | 45 | 60 | KΩ |

### 2.5.2 RST Characteristics

Fig. 2.1 shows the recommended XRES pin connection. An external RESET button is used to generate reset pulse of the whole chip. The 0.1uF capacitor is to filter out the parasitic reset glitch.

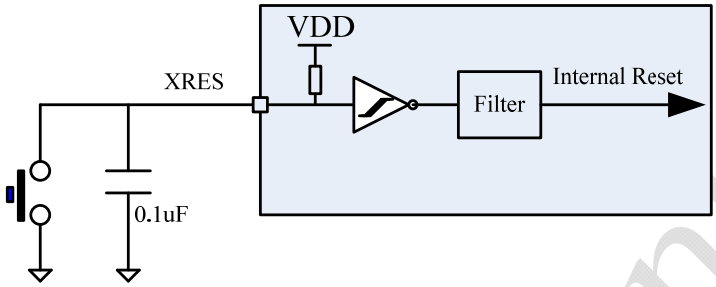



Fig. 2.1: XRES Pin Connection

# 3 Pin Definition

| Pin NO. | Pin Name | P/G/I/O | Description |
|---|---|---|---|
| 1 | VDD_IN | P | Input voltage for power amplifier, VR_PA |
| 2 | ADC_IN | I | ADC input pin. |
| 3 | GND | G | Ground |
| 4 | XTA | I | XO32M for LoRa input |
| 5 | XTB | I | XO32M for LoRa output |
| 6 | GPIO | I/O | MCU GPIO |
| 7 | AUX | I/O | MCU GPIO |
| 8 | SETA | I/O | MCU GPIO |
| 9 | DIO3 | I/O | Multipurpose digital I/O-external TCXO32M supply voltage, cannot be external GPIO |
| 10 | VREG | O | Regulated output voltage from the internal LDO/DC-DC |
| 11 | GND | G | Ground |
| 12 | DCC_SW | O | DC-DC Switcher Output |
| 13 | VBAT_RF | P | Supply for the LoRa Radio |
| 14 | UART_RX | I/O | UART RX pin |
| 15 | UART_TX | I/O | UART TX pin |
| 16 | SWD_DATA | I/O | SWD Data pin |
| 17 | SWD_CLK | I/O | SWD Clock pin |
| 18 | VDDD | P | Power supply for MCU digital section |
| 19 | P4.0 | I/O | MCU GPIO for SPI, cannot be external SPI |
| 20 | P4.1 | I/O | MCU GPIO for SPI, cannot be external SPI |
| 21 | P4.2 | I/O | MCU GPIO for SPI, cannot be external SPI |
| 22 | P4.3 | I/O | MCU GPIO for SPI, cannot be external SPI |

| | | | |
|---|---|---|---|
| 23 | VBAT_DIO | P | Digital I/O supply voltage |
| 24 | DIO2 | I/O | Multipurpose digital I/O-RF switch control, cannot be external GPIO |
| 25 | DIO1 | I/O | Multipurpose digital I/O, cannot be external GPIO |
| 26 | SPI_BUSY | I/O | SPI busy indicator, cannot be external GPIO |
| 27 | SPI_NRESET | I/O | Reset signal, active low, cannot be external GPIO |
| 28 | I2C_SCL | I/O | I2C SCL pin |
| 29 | I2C_SDA | I/O | I2C SDA pin |
| 30 | SETB | I/O | MCU GPIO |
| 31 | WCO_IN | I | XO32K for MCU input |
| 32 | WCO_OUT | I | XO32K for MCU output |
| 33 | UART_CTS | I/O | UART CTS pin |
| 34 | UART_RTS | I/O | UART RTS pin |
| 35 | SPI_MISO | I/O | SPI slave output, cannot be external SPI |
| 36 | SPI_MOSI | I/O | SPI slave input, cannot be external SPI |
| 37 | SPI_SCK | I/O | SPI clock, cannot be external SPI |
| 38 | XRES | I | External reset pin |
| 39 | SPI_NSS | I/O | SPI slave select, cannot be external SPI |
| 40 | SCAN | I | LoRa Scan pin |
| 41 | VCCD | P | Regulated digital supply (1.8V±5%) |
| 42 | VDDD | P | Power supply for MCU digital section |
| 43 | VDDA | P | Power supply for MCU analog section |
| 44 | VSSA | G | Ground |
| 45 | RFI_P | I | RF receiver input |
| 46 | RFI_N | I | RF receiver input |
| 47 | FRO | O | RF transmitter output |
| 48 | VR_PA | O | Regulated power amplifier supply |

## 3.1 Pin Assignment

Fig. 3.1 shows the pin assignment of ASR6501, QFN 6mmx6mm package is used and the total footprint is 48 pins.

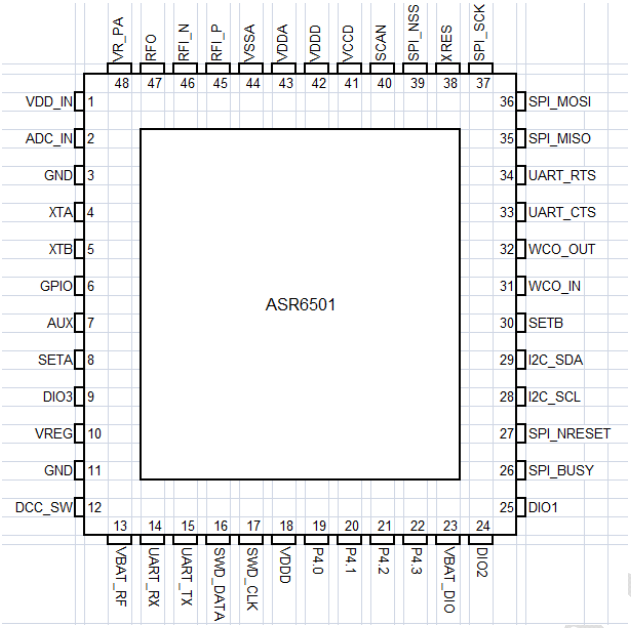
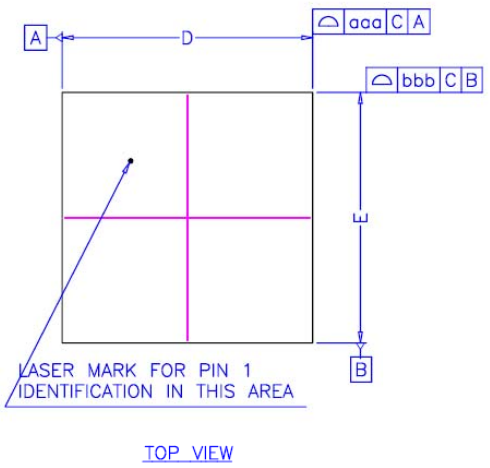
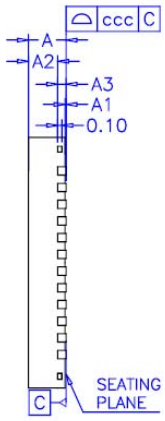



Fig. 3.1 Pin assignment of ASR6501

# 4 Mechanical Dimension



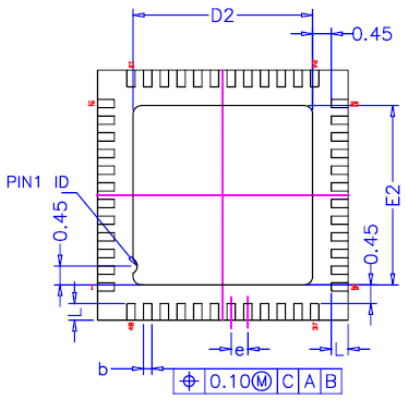

TOP VIEW




SIDE VIEW

* CONTROLLING DIMENSION : MM

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.035 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | --- | 0.65 | 0.70 | --- | 0.026 | 0.028 |
| A3 | | 0.203 REF. | | | 0.008 REF. | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | | 6.00 bsc | | | 0.236 bsc | |
| D2 | 4.20 | 4.30 | 4.40 | 0.165 | 0.169 | 0.173 |
| E | | 6.00 bsc | | | 0.236 bsc | |
| E2 | 4.20 | 4.30 | 4.40 | 0.165 | 0.169 | 0.173 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | | 0.40 bsc | | | 0.016 bsc | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | | 0.10 | | | 0.004 | |
| bbb | | 0.10 | | | 0.004 | |
| ccc | | 0.08 | | | 0.003 | |




BOTTOM VIEW

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. –1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

| ASR MICROELECTRONICS | SCALE | PROJ. |
|---|---|---|
| TITLE: PACKAGE OUTLINE 48L SAWN QFN 6.0x6.0x0.9 mm | DWG. NO.: AAA07182 | REV.: A |
| | SHEET: 1 OF 2 | SIZE: A4 |
| UNIT: INCH / MM | TOLERANCE: DIMENSION ±0.05, ANGLE | REFERENCE DOCUMENT |

# 5 Package Information

## 5.1 Product Marking

Fig. 5.1 shows the product marking of ASR6501.

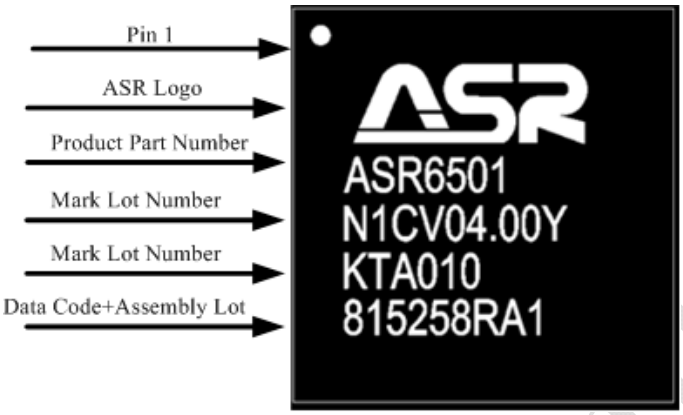



Fig. 5.1 The product marking of ASR6501