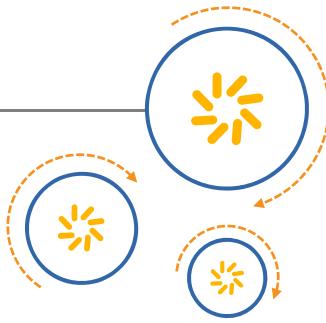




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Cambridge Business Park  
Cambridge, CB4 0WZ  
United Kingdom

## Features

- Bluetooth® v4.2 specification compliant
- 80 MHz RISC MCU Qualcomm® Kalimba™ DSP technology
- High-performance stereo codec with 1 or 2 microphones (analogue or digital)
- Mono or stereo line-in
- Radio includes integrated balun with RF performance of 9 dBm (typ) transmit power and -89 dBm (typ) basic rate receiver sensitivity
- AVRCP v1.6
- User and manufacturer configurable EQs
- Wideband speech supported by HFP v1.6 and mSBC codec
- 8<sup>th</sup> generation Qualcomm® cVc™ noise cancellation technology for narrowband and wideband voice connections including wind noise reduction
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- TrueWireless Stereo (TWS), which enables stereo sound via 2 mono devices
- Simple Speech Recognition
- Secure simple pairing, QTIL's proximity pairing and QTIL's proximity connections
- Serial interfaces: USB 2.0, UART, I<sup>2</sup>C and SPI
- Audio interfaces: Analogue/digital microphone and stereo line input
- SBC and AAC decoder support
- Wired audio support
- Integrated dual switch-mode regulators, linear regulators and battery charger
- External crystal load capacitors not required for typical crystals
- 3 LED outputs (RGB)
- 52-lead QFN 6 x 6 x 0.6 mm 0.4 mm pitch
- Green (RoHS compliant and no antimony or halogenated flame retardants)

## General Description

The CSRA63120 A11 QFN is a single-chip Bluetooth ROM audio solution for rapid evaluation and development of Bluetooth ROM applications.

The CSRA63120 A11 QFN consumer audio platform for wired and wireless applications using the QFN package integrates an ultra-low power DSP and application processor, high-performance stereo codec, a power management subsystem and LED drivers.

The configuration tools and the development kit provide a flexible and powerful development platform to design advanced and high-quality Bluetooth products using the CSRA63120 A11 QFN single-chip Bluetooth audio solution.

## BlueCore™ CSRA63120 A11 QFN

### CSRA63120 Mono ROM Solution

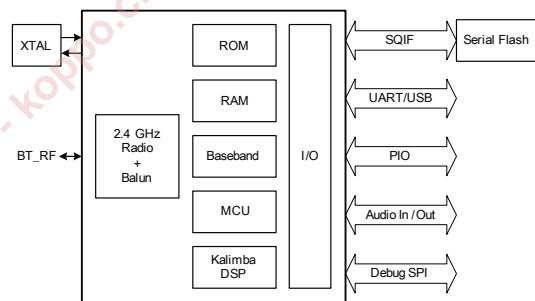
### 1 or 2-mic Qualcomm® cVc™ Headset Noise Cancellation Technology

### Fully Qualified Single-chip Bluetooth® v4.2 System

### Production Information

CSRA63120A11

Issue 1



## Applications

- Mono headsets
- Wired mono headsets and headphones
- TrueWireless Stereo-enabled headphones

The 80 MHz Kalimba DSP coprocessor supports enhanced audio and DSP applications.

The integrated audio codec supports stereo input and mono output with 1 or 2 microphones (analogue or digital), as well as a variety of audio standards.



## Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSRA63120 Mono ROM Solution	QFN-52-lead (Pb free)	6 x 6 x 0.6 mm 0.4 mm pitch	Tape and reel	CSRA63120A11-IQQW-R

**Note:**

CSRA63120 A11 QFN is a ROM-based device where the product code has the form CSRA63120Axx. Axx is the specific ROM-variant, A11 is the ROM-variant for CSRA63120 Mono ROM Solution.

Minimum order quantity is 2kpcs taped and reeled.

**Supply chain:** CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

## Contacts

General information

[www.csr.com](http://www.csr.com)

Information on this product

[sales@csr.com](mailto:sales@csr.com)

Customer support for this product

[www.csrsupport.com](http://www.csrsupport.com)

Details of compliance and standards

[product.compliance@csr.com](mailto:product.compliance@csr.com)

Help with this document

[comments@csr.com](mailto:comments@csr.com)

## CSRA63120 Mono ROM Solution Development Kit Ordering Information

Description	Order Number
CSRA63120 Mono ROM Solution Development Kit	DK-CSRA63120-10273-1A

## Device Details

### Bluetooth Radio

- On-chip balun (50 Ω impedance)
- No production trimming of external components
- Bluetooth v4.2 specification compliant

### Bluetooth Transmitter

- 9 dBm (typ) RF transmit power with level control
- Class 1, Class 2 and Class 3 support, no external PA or TX/RX switch required

### Bluetooth Receiver

- -91.0 dBm (typ) π/4 DQPSK receiver sensitivity and -81.0 dBm (typ) 8DPSK receiver sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available to application
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

### Bluetooth Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16 MHz to 32 MHz

### Kalimba DSP

- Kalimba DSP coprocessor, 80 MHz, 24-bit fixed point core
- 2 single-cycle MACs: 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 6K x 32-bit program RAM including 1K instruction cache for executing out of internal ROM
- 16K x 24-bit + 16K x 24-bit 2-bank data RAM

### Audio Interfaces

- Stereo audio ADC with line input
- Mono audio DAC
- Supported sample rates of 8, 11.025, 16, 22.05, 32, 44.1, 48 and 96 kHz (DAC only)

### Auxiliary Features

- Crystal oscillator with built-in digital trimming

### Package Option

- 52-lead QFN 6 x 6 x 0.6 mm 0.4 mm pitch

### Physical Interfaces

- UART interface for debug
- USB 2.0 (full-speed) interface, including USB BC1.2 charger detection
- 4-bit SPI flash memory interface
- SPI interface for debug and programming
- I<sup>2</sup>C master for amp control
- Up to 10 general purpose PIOs
- 3 LED drivers (includes RGB) with PWM flasher independent of MCU

### Integrated Power Control and Regulation

- Automatic power switching to charger when present
- 2 high-efficiency switch-mode regulators with 1.8 V and 1.35 V outputs direct from battery supply
- 3.3 V linear regulator for USB supply
- Low-voltage linear regulator for internal digital circuits
- Low-voltage linear regulator for internal analogue circuits
- Power-on-reset detects low supply voltage
- Power management includes digital shutdown and wake-up commands for ultra-low power modes

### Battery Charger

- Lithium ion / Lithium polymer battery charger
- Instant-on function automatically selects the power supply between battery and USB, which enables operation even if the battery is fully discharged
- Fast charging support up to 200 mA with no external components.
- Supports USB charger detection
- Support for thermistor protection of battery pack
- Support to enable end product design to PSE law:
  - Design to JIS-C 8712/8714 (batteries)
  - Testing based on IEEE 1725

### Baseband and Software

- Internal ROM
- 56 KB internal RAM, enables full-speed data transfer, and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping

## CSRA63120 Mono ROM Solution Details

### Bluetooth Profiles

- Bluetooth v4.2 specification support
- A2DP v1.3
- AVRCP v1.6
- HFP v1.6
- HSP v1.2
- DI v1.3

### Music Enhancements

- SBC and AAC
- TrueWireless Stereo (TWS)
- Configurable Signal Detection to trigger events
- Up to 10 stages of Speaker Parametric EQ
- Up to 6 banks of 5 stages of User Parametric EQ for music playback (user, rock, pop, classical, jazz, etc)
- Volume Control
- Compander to compress or expand the dynamic range of the audio
- Post Mastering to improve DAC fidelity
- Volume Boost

### Additional Functionality

- Support for multi-language programmable audio prompts
- QTIL's proximity pairing and QTIL's proximity connection
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Talk-time extension, which automatically reduces processor functions to extend use when a low battery condition is detected

### CSRA63xxx ROM Series Configuration Tool

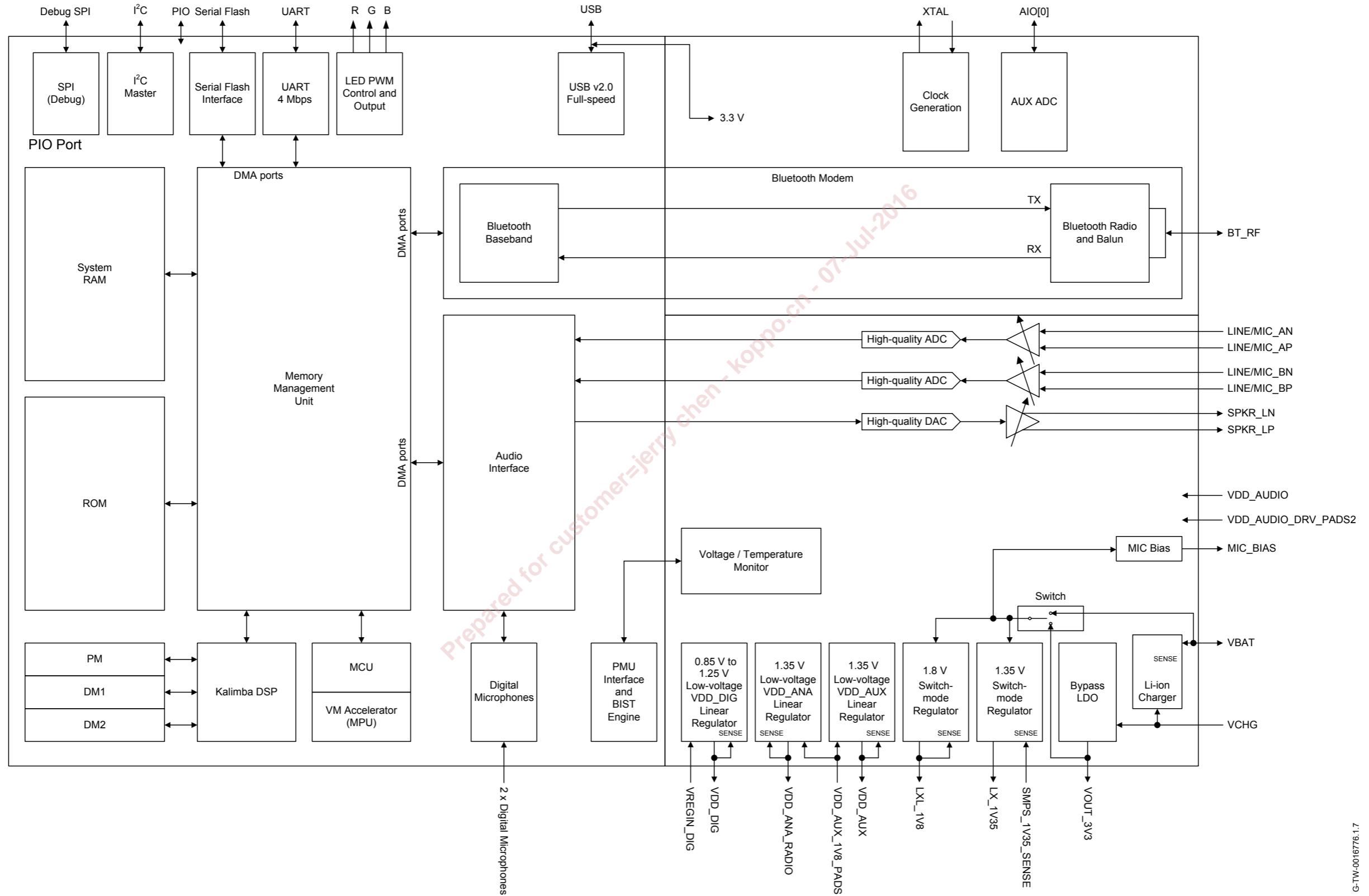
Configures the CSRA63120 mono ROM solution software features:

- Bluetooth v4.2 specification features
- Reconnection policies, e.g. reconnect on power-on
- Audio features, including default volumes
- Button events: configuring button presses and durations for certain events, e.g. double press on PIO for last number redial
- LED indications for states, e.g. headset connected, and events, e.g. power on
- Indication tones for events and ringtones
- Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
- Advanced Multipoint settings

### CSRA63120 Mono ROM Solution Development Kit

- Example CSRA63120 A11 QFN module design
- Carrier board
- Output stage: headphone amplifier
- Interface adapters and cables

## Functional Block Diagram



G-TW001676-1.7

## Document History

Revision	Date	Change Reason
Issue 1	09 MAR 16	Original publication of this document.

Prepared for customer=jerry chen - koppo.cn - 07-Jul-2016

## Status Information

The status of this Data Sheet is **Production Information**. CSR Product Data Sheets progress according to the following format:

- **Advance Information:**
  - Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
- **Engineering Sample:**
  - Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
  - All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.
- **Pre-production Information:**
  - Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
  - All electrical specifications may be changed by CSR without notice.
- **Production Information:**
  - Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.
  - Production Data Sheets supersede all previous document versions.

### Device Implementation

#### Important Note:

As the feature-set of the CSRA63120 A11 QFN is firmware build-specific, see the relevant software release note for the exact implementation of features on the CSRA63120 A11 QFN.

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### CSR Green Semiconductor Products and RoHS Compliance

CSRA63120 A11 QFN devices meet the requirements of Directive 2011/65/EU of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). CSRA63120 A11 QFN devices are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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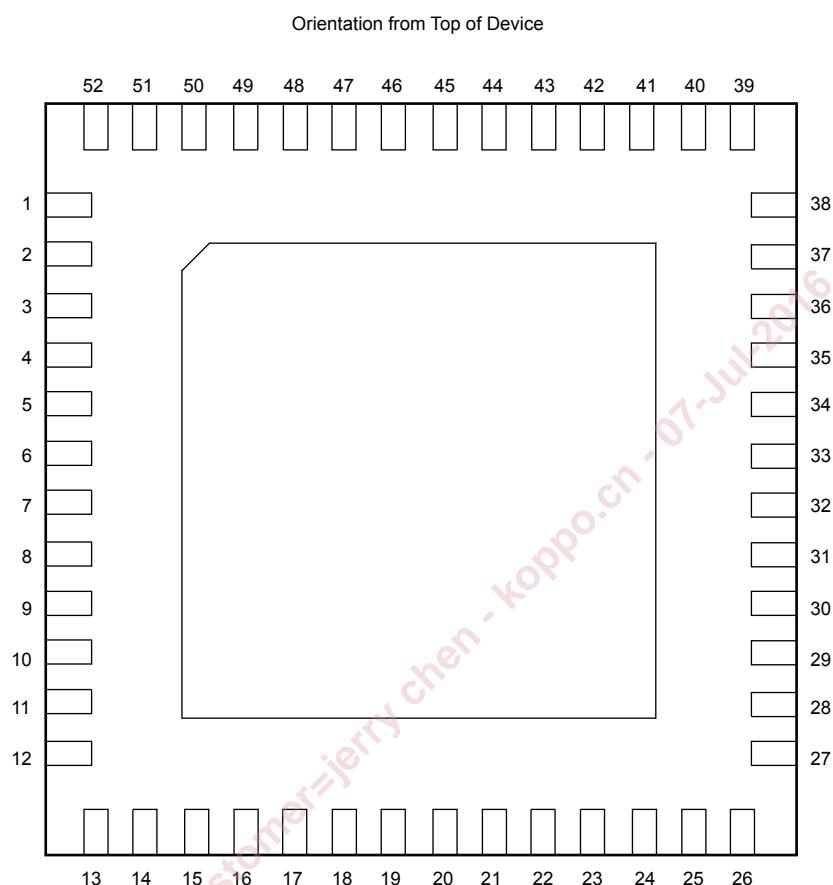
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## 1 Package Information

### 1.1 Pinout Diagram



G-TW-0015988.1.3

**Figure 1.1: Device Pinout**

## 1.2 Device Terminal Functions

Radio	Lead	Pad Type	Supply Domain	Description
BT_RF	9	RF	VDD_ANA_RADIO	Bluetooth 50 Ω transmitter output / receiver input

Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	14	Analogue	VDD_AUX	Crystal input
XTAL_OUT	13	Analogue	VDD_AUX	Drive for crystal

USB	Lead	Pad Type	Supply Domain	Description
USB_DP	41	Bidirectional	VOUT_3V3	USB data plus with selectable internal 1.5 kΩ pull-up resistor
USB_DN	40	Bidirectional	VOUT_3V3	USB data minus

SPI/PIO Interface	Lead	Pad Type	Supply Domain	Description
SPI_PCM#	23	Input with weak pull-down	VDD_AUX_1V8_PADS1	SPI/PIO select input: ■ 0 = PIO interface ■ 1 = SPI

**Note:**

The Debug SPI interface is mapped as an alternative function on the PIO port.

SQIF	Lead	Pad Type	Supply Domain	Description
QSPI_FLASH_CLK	20	Bidirectional with strong pull-down	VDD_AUX_1V8_PADS1	SPI flash clock
QSPI_FLASH_CS#	17	Bidirectional with strong pull-up	VDD_AUX_1V8_PADS1	SPI flash chip select
QSPI_IO[3]	16	Bidirectional with strong pull-up	VDD_AUX_1V8_PADS1	SPI flash data bit 3
QSPI_IO[2]	18	Bidirectional with strong pull-up	VDD_AUX_1V8_PADS1	SPI flash data bit 2
QSPI_IO[1]	25	Bidirectional with strong pull-down	VDD_AUX_1V8_PADS1	SPI flash data bit 1
QSPI_IO[0]	21	Bidirectional with strong pull-down	VDD_AUX_1V8_PADS1	SPI flash data bit 0

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[9]	43	Bidirectional with strong pull-down	VDD_AUDIO_DRV_PADS2	Programmable input / output line 9. Alternative function: ■ UART_CTS: UART clear to send, active low
PIO[8]	46	Bidirectional with strong pull-up	VDD_AUDIO_DRV_PADS2	Programmable input / output line 8. Alternative function: ■ UART_RTS: UART request to send, active low
PIO[7]	42	Bidirectional with strong pull-down	VDD_AUDIO_DRV_PADS2	Programmable input / output line 7.
PIO[6]	47	Bidirectional with strong pull-down	VDD_AUDIO_DRV_PADS2	Programmable input / output line 6.
PIO[5]	26	Bidirectional with weak pull-down	VDD_AUX_1V8_PADS1	Programmable input / output line 5. Alternative function: ■ SPI_CLK: Debug SPI clock
PIO[4]	19	Bidirectional with weak pull-down	VDD_AUX_1V8_PADS1	Programmable input / output line 4. Alternative function: ■ SPI_CS#: chip select for debug SPI, active low
PIO[3]	22	Bidirectional with weak pull-down	VDD_AUX_1V8_PADS1	Programmable input / output line 3. Alternative function: ■ SPI_MISO: debug SPI data output
PIO[2]	24	Bidirectional with weak pull-down	VDD_AUX_1V8_PADS1	Programmable input / output line 2. Alternative function: ■ SPI_MOSI: debug SPI data input
PIO[1]	45	Bidirectional with strong pull-up	VDD_AUDIO_DRV_PADS2	Programmable input / output line 1. Alternative function: ■ UART_TX: UART data output ■ AMP_I2C_SDA: I <sup>2</sup> C serial data line for external amplifier control
PIO[0]	44	Bidirectional with strong pull-up	VDD_AUDIO_DRV_PADS2	Programmable input / output line 0. Alternative function: ■ UART_RX: UART data input ■ AMP_I2C_SCL: I <sup>2</sup> C serial clock line for external amplifier control

AIO Port	Lead	Pad Type	Supply Domain	Description
AIO[0]	15	Bidirectional	VDD_AUX	Analogue programmable input / output line 0.

Codec	Lead	Pad Type	Supply Domain	Description
MIC_BIAS	52	Analogue out	VBAT, VOUT_3V3	Microphone bias
AU_REF	51	Analogue in	VDD_AUDIO	Decoupling of audio reference (for high-quality audio)
SPKR_LN	7	Analogue out	VDD_AUDIO_DRV_PADS2	Speaker output negative
SPKR_LP	8	Analogue out	VDD_AUDIO_DRV_PADS2	Speaker output positive
LINE/MIC_AN	50	Analogue in	VDD_AUDIO	Line or microphone input negative, channel A
LINE/MIC_AP	49	Analogue in	VDD_AUDIO	Line or microphone input positive, channel A
LINE/MIC_BN	2	Analogue in	VDD_AUDIO	Line or microphone input negative, channel B
LINE/MIC_BP	3	Analogue in	VDD_AUDIO	Line or microphone input positive, channel B

LED Drivers	Lead	Pad Type	Supply Domain	Description
LED[2]	48	Bidirectional	VDD_AUDIO_DRV_PADS2	LED driver
LED[1]	27	Bidirectional	VDD_AUX_1V8_PADS1	LED driver
LED[0]	28	Bidirectional	VDD_AUX_1V8_PADS1	LED driver

Power Supplies and Control	Lead	Description
VOUT_3V3	36	Positive supply for USB port and 3.3 V bypass linear regulator output. Connect external minimum 2.2 µF ceramic decoupling capacitor.
LX_1V35	37	1.35 V switch-mode power regulator inductor connection.
LX_1V8	34	1.8 V switch-mode power regulator inductor connection.
SMPS_1V35_SENSE	39	1.35 V switch-mode power regulator sense input.
VBAT	35	Battery positive terminal.
VCHG	32	Charger input. Typically connected to VBUS (USB supply) as Section 11 shows.
VDD_ANA_RADIO	10	Bluetooth radio supply. Connect to 1.35 V supply, see Section 11 for connections.
VDD_AUDIO	1	Positive supply for audio. Connect to 1.35 V supply, see Section 11 for connections.
VDD_AUDIO_DRV_PADS2	6	1.8 V positive supply input for audio output amplifiers and positive supply for input/output ports. Connect to 1.8 V supply, see Section 11 for connections.

Power Supplies and Control	Lead	Description
VDD_AUX	11	Auxiliary supply. Connect to 1.35 V supply, see Section 11 for connections.
VDD_AUX_1V8_PADS1	12	Auxiliary LDO regulator input and 1.8 V positive supply input for input/output ports. Connect to 1.8 V supply, see Section 11 for connections.
VDD_DIG	29	Digital LDO regulator output, see Section 11 for connections.
VREGENABLE	31	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
VREGIN_DIG	30	Digital LDO regulator input, see Section 11 for connections. Typically connected to a 1.35 V supply.
VSS_SMPS_1V35	38	1.35 V switch-mode regulator ground.
VSS_SMPS_1V8	33	1.8 V switch-mode regulator ground.
VSS	Exposed pad	Ground connections.

Unconnected Terminals	Lead	Description
NC	4, 5	Leave unconnected

### 1.3 Package Dimensions

Top View

Side View

Bottom View

Notes

- Dimensions and tolerances conform to ASME Y14.5M - 1994
- Pin 1 identifier is placed on top surface of the package by using identification mark or other feature of package body.
- Exact shape and size of this feature is optional.
- Package warpage 0.08 mm maximum.

Description

52-lead Quad-Flat No-lead (QFN) package

Size

6 x 6 x 0.6 mm QFN

JEDEC

Non-JEDEC

Pitch

0.4 mm pitch

Units

mm

G-TW-00159519

## 1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 6 x 6 x 0.6 mm QFN 52-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- QTIL recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

## 1.5 Typical Solder Reflow Profile

For information, see *Typical Solder Reflow Profile for Lead-free Devices Information Note*.

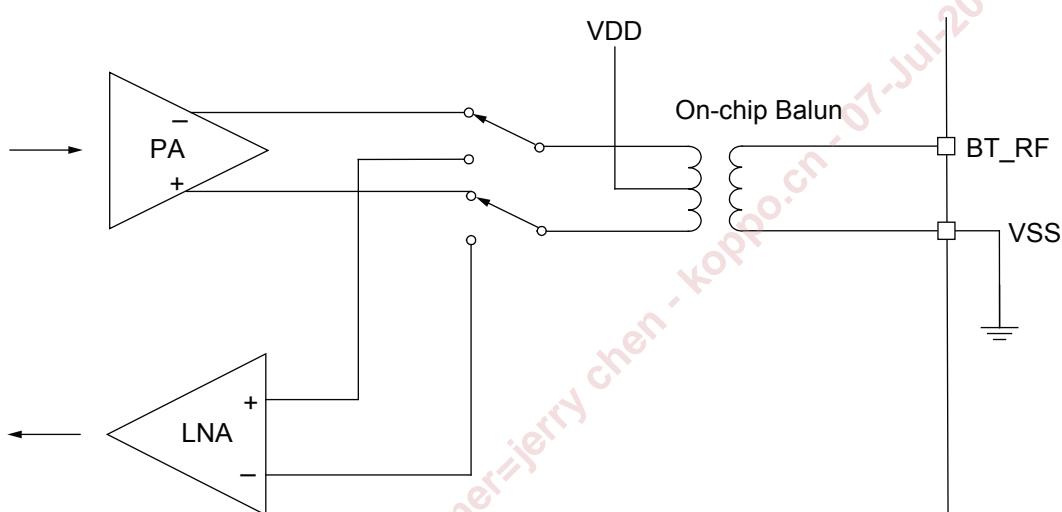
## 2 Bluetooth Modem

The Bluetooth modem includes:

- RF ports
- RF receiver
- RF transmitter
- Bluetooth radio synthesiser
- Baseband

### 2.1 RF Ports (BT\_RF)

CSRA63120 A11 QFN contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is  $50\ \Omega$  and the transmitter has been optimised to deliver power into a  $50\ \Omega$  load.



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Figure 2.1: Simplified Circuit BT\_RF

### 2.2 RF Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. A digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise enables CSRA63120 A11 QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

#### 2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

#### 2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

### 2.3 RF Transmitter

#### 2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

### 2.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the CSRA63120 A11 QFN has a maximum output power that enables it to operate as a Class 1, Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

### 2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.2 specification.

### 2.5 Baseband

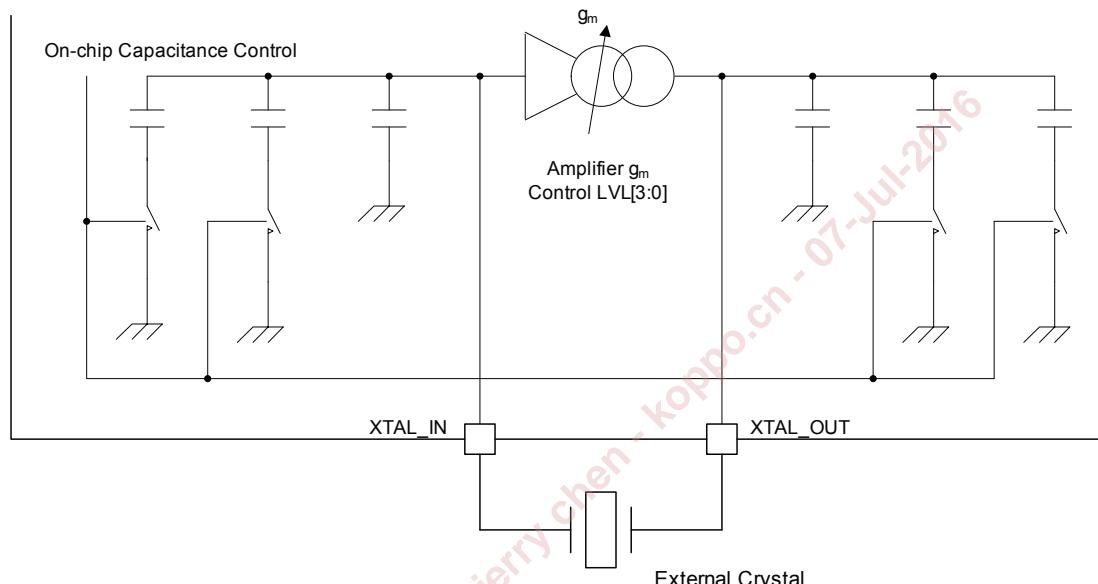
The baseband handles the digital functions of the Bluetooth modem, for example the Burst Mode Controller and Physical Layer Hardware Engine.

### 3 Clock Generation

CSRA63120 A11 QFN accepts a reference clock input from a crystal.

#### 3.1 Crystal

Figure 3.1 shows the CSRA63120 A11 QFN contains a crystal driver circuit that acts as a transconductance amplifier that drives an external crystal connected between XTAL\_IN and XTAL\_OUT. The crystal driver circuit forms a Pierce oscillator with the external crystal. External capacitors are not required for standard crystals that require a load capacitance of around 9pF. QTIL recommends this option.



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**Figure 3.1: Crystal Oscillator Overview**

The on-chip capacitance is adjusted using PSKEY\_XTAL\_OSC\_CONFIG, see Table 3.1. The default values suit a typical crystal requiring a 9 pF load capacitance. In deep sleep mode, the crystal oscillation is maintained, but at a lower drive strength to reduce power consumption. The drive strength and load capacitance are configured with a PS Key.

	Normal Mode PSKEY_XTAL_OSC_CONFIG [3:2]				Low Power Mode PSKEY_XTAL_OSC_CONFIG [1:0]			
	00	01	10	11	00	01	10	11
XTAL_IN (Typical)	15.6 pF	10.8 pF	6.0 pF	1.1 pF	15.6 pF	10.8 pF	6.0 pF	1.1 pF
XTAL_OUT (Typical)	20.8 pF	16.0 pF	11.2 pF	6.4 pF	16.0 pF	11.2 pF	6.4 pF	1.5 pF

**Table 3.1: Typical On-chip Capacitance Values**

The drive strength is configured with PSKEY\_XTAL\_LVL. The default level for this PS Key is sufficient for typical crystals. The level control is set in the range 0 to 15, where 15 is the maximum drive level.

Increasing the crystal amplifier drive level increases the transconductance of the crystal amplifier, which creates an increase in the oscillator margin (ratio of oscillator amplifiers is equivalent to the negative resistance of the crystal ESR).

**Note:**

Excessive amplifier transconductance can lead to an increase in the oscillator phase noise if the oscillator amplifier is excessively overdriven. Set the transconductance to the minimum level to give the desired oscillation ratio. Higher values can increase power consumption. Also, insufficient drive strength can prevent the the crystal from starting to oscillate.

### 3.1.1 Negative Resistance Model

The crystal and its load capacitor can be modelled as a frequency dependant resistive element. Consider the driver amplifier as a circuit that provides negative resistance. For oscillation, the value of the negative resistance should be greater than that of the crystal circuit equivalence resistance. Equation 3.1 shows how to calculate the equivalent negative resistance.

$$R_{\text{neg}} = -\frac{g_m C_{\text{in}} C_{\text{out}}}{2\pi f^2 (C_{\text{out}} C_{\text{in}} + (C_0 + C_{\text{int}})(C_{\text{out}} + C_{\text{in}}))^2}$$

**Equation 3.1: Negative Resistance**

Where:

- $g_m$  = Transconductance of the crystal oscillator amplifier
- $C_0$  = Static capacitance of the crystal, which is sometimes referred to as the shunt or case capacitance
- $C_{\text{int}}$  = On-chip parasitic capacitance between input and output of XTAL amplifier.
- $C_{\text{in}}$  = Internal capacitance on XTAL\_IN, see Table 3.1
- $C_{\text{out}}$  = Internal capacitance on XTAL\_OUT, see Table 3.1

Parameter	Min	Typ	Max	Unit
Transconductance	2	-	-	mS
$C_{\text{int}}$	-	1.5	-	pF

**Table 3.2: Transconductance and On-chip Parasitic Capacitance**

### 3.1.2 Crystal Specification

Table 3.3 shows the specification for an external crystal.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	32	MHz
Initial Frequency error from nominal frequency which can be compensated for	-	-	$\pm 285$	ppm
Frequency Stability	-	-	$\pm 20$	ppm
Crystal ESR	-	-	60	$\Omega$

**Table 3.3: Crystal Specification**

### 3.1.3 Crystal Calibration

The actual crystal frequency depends on the capacitance of XTAL\_IN and XTAL\_OUT on the PCB and the CSRA63120 A11 QFN, as well as the capacitance of the crystal.

The Bluetooth specification requires  $\pm 20$  ppm clock accuracy. The actual frequency at which a crystal oscillates contains two error terms, which are typically mentioned in the crystal device datasheets:

- Initial Frequency Error: The difference between the desired frequency and the actual oscillating frequency caused by the crystal itself and its PCB connections. It is also called as Calibration Tolerance or Frequency Tolerance.
- Frequency Stability: The total of how far the crystal can move off frequency with temperature, aging or other effects. It is also called as Temperature Stability, Frequency Stability or Aging.

CSRA63120 A11 QFN has the capability to compensate for Initial Frequency errors by a simple per-device basis on the production line, with the trim value stored in the non-volatile memory (PS Key). However, it is not possible to compensate for frequency stability, therefore a crystal must be chosen with a Frequency Stability that is better than  $\pm 20$  ppm clock accuracy.

Some crystal datasheets combine both these terms into one tolerance value. This causes a problem because only the initial frequency error can be compensated for and CSRA63120 A11 QFN cannot compensate for the temperature or aging performance. If frequency stability is not explicitly stated, QTIL cannot guarantee remaining within the Bluetooth's  $\pm 20$  ppm frequency accuracy specification.

Crystal calibration uses a single measurement of RF output frequency and can be performed quickly as part of the product final test. Typically, a TXSTART radio command is sent and then a measurement of the output RF frequency is read. From this, the calibration factor to correct actual offset from the desired frequency can be calculated. This offset value is stored in PSKEY\_ANA\_FTRIM\_OFFSET. CSRA63120 A11 QFN then compensates for the initial frequency offset of the crystal.

The value in PSKEY\_ANA\_FTRIM\_OFFSET is a 16-bit 2's complement signed integer which specifies the fractional part of the ratio between the true crystal frequency,  $f_{actual}$ , and the value set in PSKEY\_ANA\_FREQ,  $f_{nominal}$ . Equation 3.2 shows the value of PSKEY\_ANA\_FTRIM\_OFFSET in parts per  $2^{20}$  rounded to the nearest integer.

$$\text{PSKEY\_ANA\_FTRIM\_OFFSET} = \left( \frac{f_{actual}}{f_{nominal}} - 1 \right) \times 2^{20}$$

**Equation 3.2: Crystal Calibration Using PSKEY\_ANA\_FTRIM\_OFFSET**

For more information on TXSTART radio test see *BlueTest User Guide*.

## 4 Processors

### 4.1 Bluetooth Stack Microcontroller

The CSRA63120 A11 QFN uses a 16-bit RISC 80 MHz MCU for low power consumption and efficient use of memory. It contains a single-cycle multiplier and a memory protection unit.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

### 4.2 Kalimba DSP

The Kalimba DSP performs signal processing functions on over-air data or codec data to enhance audio applications.

The key features of the DSP include:

- 80 MHz performance, 24-bit fixed point DSP core
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulate includes 2 rMAC registers and new instructions for improved performance over previous architecture
- 32-bit instruction word
- Separate program memory and dual data memory, enabling an ALU operation and up to 2 memory accesses in a single cycle
- Zero overhead looping, including a very low-power 32-instruction cache
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 56-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

## 5 Memory Interface and Management

### 5.1 Memory Management Unit

The MMU provides buffers that hold the data in transit between the host, the air or the Kalimba DSP. The use of DMA ports also helps with efficient transfer of data to other peripherals.

### 5.2 System RAM

56 KB of integrated RAM supports the RISC MCU.

### 5.3 Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 16K x 24-bit for data memory 1 (DM1)
- 16K x 24-bit for data memory 2 (DM2)
- 6K x 32-bit for program memory (PM)

### 5.4 Internal ROM

Internal ROM is provided for system firmware implementation.

### 5.5 Serial Quad I/O Flash Interface (SQIF)

The CSRA63120 A11 QFN uses external serial flash ICs for storage of device-specific data. The CSRA63120 A11 QFN supports a 4-bit I/O flash-memory interface. Figure 5.1 shows a typical connection between the CSRA63120 A11 QFN and a serial flash IC.

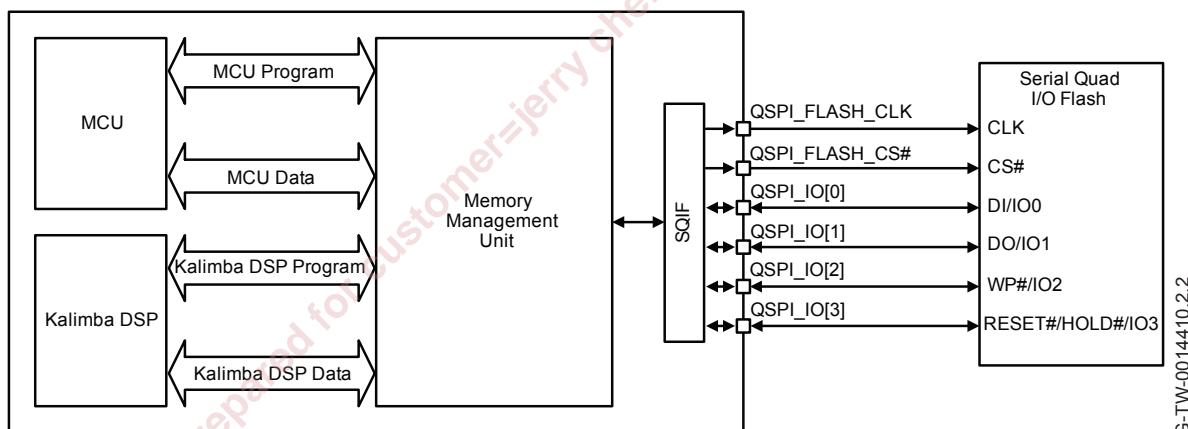


Figure 5.1: Serial Quad I/O Flash Interface

The SQIF interface on the CSRA63120 A11 QFN requires use of a suitable Quad SPI Flash chip of minimum size 4 Mb, connected as Figure 5.1 shows. For a list of supported Quad SPI Flash devices, see the *CSRA63xxx/CSRA64xxx A11 Firmware Release Note*.

## 6 Serial Interfaces

### 6.1 USB Interface

CSRA63120 A11 QFN has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on CSRA63120 A11 QFN acts as a USB peripheral, responding to requests from a master host controller.

CSRA63120 A11 QFN contains internal USB termination resistors and requires no external resistor matching.

CSRA63120 A11 QFN supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, supports USB standard charger detection and fully supports the *USB Battery Charging Specification*, available from <http://www.usb.org>. For more information on how to integrate the USB interface on CSRA63120 A11 QFN, see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

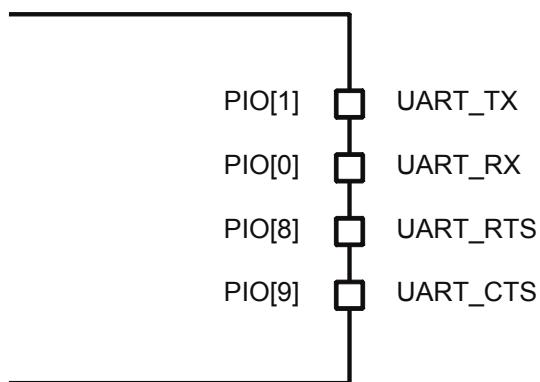
### 6.2 UART Interface

CSRA63120 A11 QFN has an optional UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug. The UART interface is multiplexed with PIOs and other functions, and hardware flow control is optional. Table 6.1 shows the PS Keys for configuring this multiplexing.

PS Key	PIO Location
PSKEY_UART_RX_PIO	PIO[0]
PSKEY_UART_TX_PIO	PIO[1]
PSKEY_UART_RTS_PIO	PIO[8]
PSKEY_UART_CTS_PIO	PIO[9]

Table 6.1: PS Keys for UART/PIO Multiplexing

Figure 6.1 shows the 4 signals that implement the UART function.



**Figure 6.1: Universal Asynchronous Receiver**

When CSRA63120 A11 QFN is connected to another digital device, UART\_RX and UART\_TX transfer data between the 2 devices. The remaining 2 signals, UART\_CTS and UART\_RTS, implement optional RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using CSRA63120 A11 QFN firmware.

**Note:**

To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 6.2 shows the possible UART settings.

Parameter	Possible Values	
Baud rate	Minimum	1200 baud ( $\leq 2\%$ Error)
		9600 baud ( $\leq 1\%$ Error)
	Maximum	4 Mbaud ( $\leq 1\%$ Error)
Flow control	RTS/CTS or None	
Parity	None, Odd or Even	
Number of stop bits	1 or 2	
Bits per byte	8	

**Table 6.2: Possible UART Settings**

Table 6.3 lists common baud rates and their associated error values for PSKEY\_UART\_BITRATE. To set the UART baud rate, load PSKEY\_UART\_BITRATE with the number of bits per second.

Baud Rate	PS Key Value (Bits Per Second)	Error
1200	1200	1.73%
2400	2400	1.73%
4800	4800	1.73%

Baud Rate	PS Key Value (Bits Per Second)	Error
9600	9600	-0.82%
19200	19200	0.45%
38400	38400	-0.18%
57600	57600	0.03%
76800	76800	0.14%
115200	115200	0.03%
230400	230400	0.03%
460800	460800	-0.02%
921600	921600	0.00%
1382400	1382400	-0.01%
1843200	1843200	0.00%
2764800	2764800	0.00%
3686400	3686400	0.00%

Table 6.3: Standard Baud Rates

## 6.3 Programming and Debug Interface

CSRA63120 A11 QFN provides a debug SPI interface for programming, configuring (PS Keys) and debugging the CSRA63120 A11 QFN. Access to this interface is required in production. Ensure the 4 SPI signals and the SPI\_PCM# line are brought out to either test points or a header. To use the SPI interface, the SPI\_PCM# line requires the option of being pulled high externally.

QTIL provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from QTIL.

### 6.3.1 Multi-slave Operation

Avoid connecting CSRA63120 A11 QFN in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSRA63120 A11 QFN is deselected (SPI\_CS# = 1), the SPI\_MISO line does not float. Instead, CSRA63120 A11 QFN outputs 0 if the processor is running or 1 if it is stopped.

## 6.4 I<sup>2</sup>C Interface

The CSRA63120 A11 QFN supports an I<sup>2</sup>C interface for I/O port expansion. Its primary function is to control an external audio power amplifier. The default assignment of the I<sup>2</sup>C interface onto the PIOs on the CSRA63120 A11 QFN is:

- PIO[0] is the I<sup>2</sup>C interface SCL line (AMP\_I2C\_SCL)
- PIO[1] is the I<sup>2</sup>C interface SDA line (AMP\_I2C\_SDA)

Alternatively, the I<sup>2</sup>C interface can be assigned to two PIOs from PIO[9:0] using PSKEY\_I2C\_SCL\_PIO and PSKEY\_I2C\_SDA\_PIO.

**Note:**

The I<sup>2</sup>C interface requires external pull-up resistors. Ensure that external pull-up resistors are suitably sized for the I<sup>2</sup>C interface speed and PCB track capacitance.

## 7 Interfaces

### 7.1 Programmable I/O Ports, PIO

CSRA63120 A11 QFN provides up to 10 lines of programmable bidirectional I/O, PIO[9:0]. Table 7.1 lists the PIOs on the CSRA63120 A11 QFN that have alternative functions.

PIO	Function		
	Debug SPI	UART	I <sup>2</sup> C
PIO[0]	-	UART_RX	AMP_I2C_SCL (default)
PIO[1]	-	UART_TX	AMP_I2C_SDA (default)
PIO[2]	SPI_MOSI	-	Alternate I <sup>2</sup> C function
PIO[3]	SPI_MISO	-	Alternate I <sup>2</sup> C function
PIO[4]	SPI_CS#	-	Alternate I <sup>2</sup> C function
PIO[5]	SPI_CLK	-	Alternate I <sup>2</sup> C function
PIO[6]	-	-	Alternate I <sup>2</sup> C function
PIO[7]	-	-	Alternate I <sup>2</sup> C function
PIO[8]	-	UART_RTS	Alternate I <sup>2</sup> C function
PIO[9]	-	UART_CTS	Alternate I <sup>2</sup> C function

Table 7.1: Alternative PIO Functions

**Note:**

See the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

To change the default assignment shown for some alternative functions, use PS Keys. For UART, see Section 6.2. For I<sup>2</sup>C, see Section 6.4.

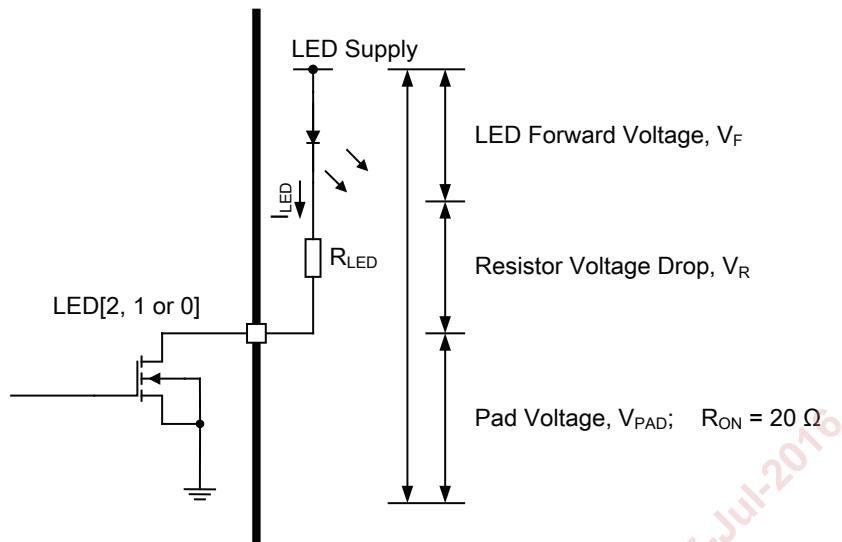
### 7.2 Analogue I/O Ports, AIO

CSRA63120 A11 QFN has 1 general-purpose analogue interface pin, AIO[0]. Typically, this connects to a thermistor for battery pack temperature measurements during charge control. See Section 11 for typical connections.

### 7.3 LED Drivers

The CSRA63120 A11 QFN includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.



**Figure 7.1: LED Equivalent Circuit**

From Figure 7.1 it is possible to derive Equation 7.1 to calculate  $I_{LED}$ . If a known value of current is required through the LED to give a specific luminous intensity, then the value of  $R_{LED}$  is calculated.

$$I_{LED} = \frac{V_{DD} - V_F}{R_{LED} + R_{ON}}$$

**Equation 7.1: LED Current**

For the LED pads to act as resistance, the external series resistor,  $R_{LED}$ , needs to be such that the voltage drop across it,  $V_R$ , keeps  $V_{PAD}$  below 0.5 V. Equation 7.2 also applies.

$$V_{DD} = V_F + V_R + V_{PAD}$$

**Equation 7.2: LED PAD Voltage**

**Note:**

The supply domain for LED[2:0] must remain powered for LED functions to operate.

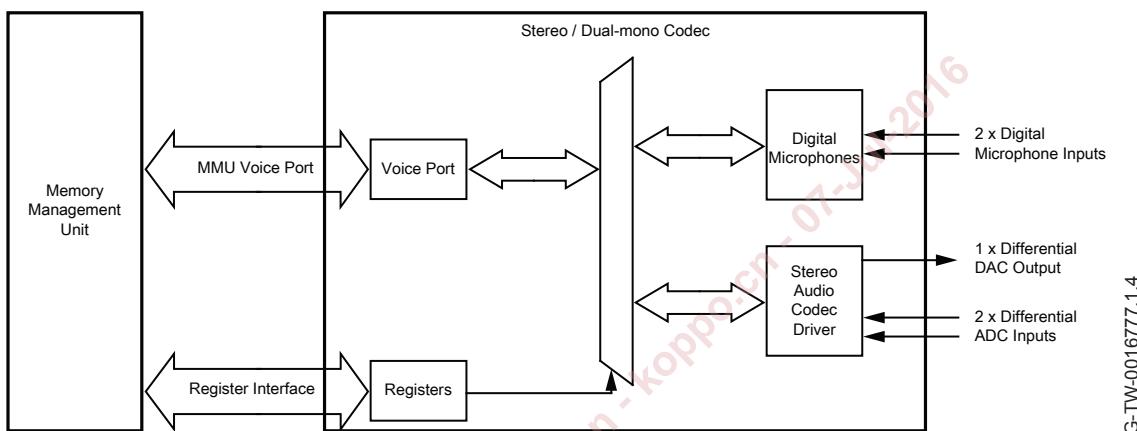
The LED current adds to the overall current. Conservative LED selection extends battery life.

## 8 Audio Interface

The audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analogue audio inputs
- Dual digital microphone inputs
- Mono analogue audio output

Figure 8.1 shows the functional blocks of the interface. The codec supports mono playback and recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC of the codec contains 2 independent high-quality channels, and the DAC contains 1. Any ADC and DAC channels run at their own independent sample rate.



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Figure 8.1: Audio Interface

### 8.1 Audio Input and Output

The audio input circuitry consists of 2 independent 16-bit high-quality ADC channels:

- Programmable as either stereo or dual-mono inputs
- Programmable as either microphone or line input
- Each channel is independently configurable to be either single-ended or fully differential
- Each channel has an analogue and digital programmable gain stage, this also aids optimisation of different microphones

The audio output circuitry consists of a dual differential class A-B output stage.

**Note:**

CSRA63120 A11 QFN is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

### 8.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Mono analogue output for voice band and audio band

**Important Note:**

With respect to audio input, software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

## 8.2.1 Audio Codec Block Diagram

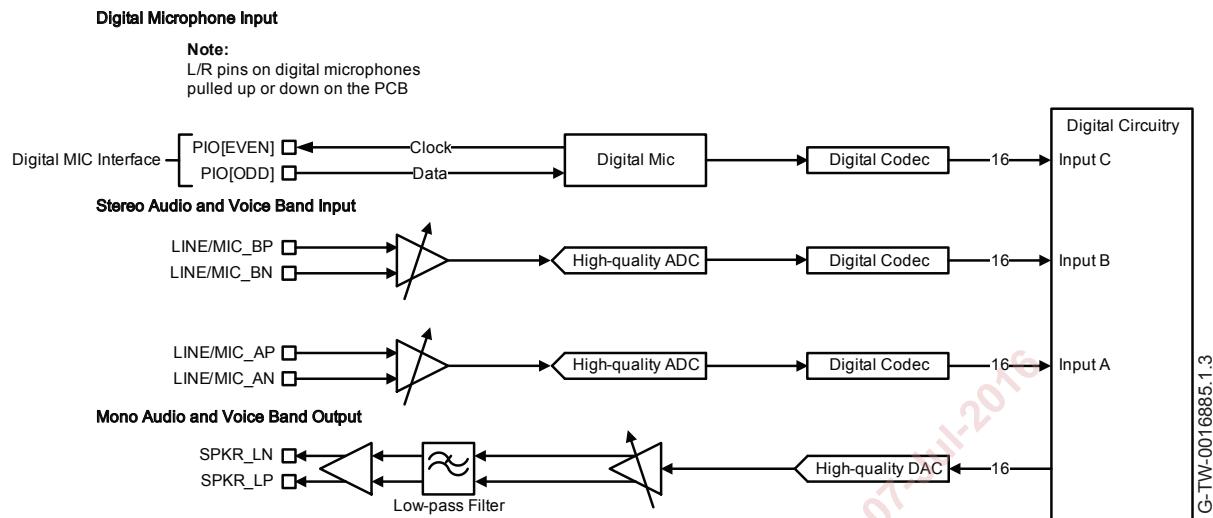


Figure 8.2: Audio Codec Input and Output Stages

The CSRA63120 A11 QFN audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD\_AUDIO for the audio circuits and VDD\_AUDIO\_DRV\_PADS2 for the audio driver circuits.

## 8.2.2 ADC

The CSRA63120 A11 QFN consists of 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter
- Each ADC is a separate channel with identical functionality
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage

## 8.2.3 ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40 kHz:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz

## 8.2.4 ADC Audio Input Gain

Figure 8.3 shows that the CSRA63120 A11 QFN audio input gain consists of:

- An analogue gain stage based on a pre-amplifier and an analogue gain amplifier
- A digital gain stage

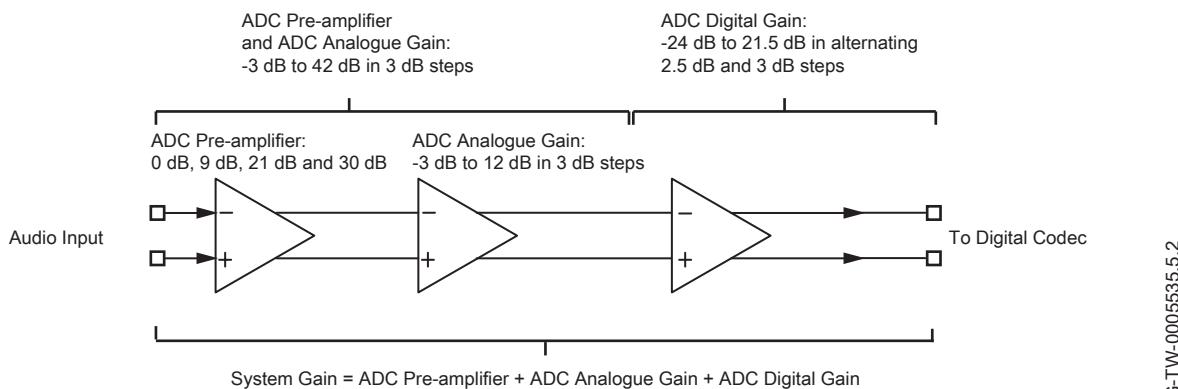


Figure 8.3: Audio Input Gain

### 8.2.5 ADC Pre-amplifier and ADC Analogue Gain

CSRA63120 A11 QFN has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0 dB, 9 dB, 21 dB and 30 dB
- The ADC analogue amplifier gain is -3 dB to 12 dB in 3 dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3 dB to 42 dB in 3 dB steps
- At mid to high gain levels it acts as a microphone pre-amplifier
- At low gain levels it acts as an audio line level amplifier

### 8.2.6 ADC Digital Gain

Table 8.1 shows that a digital gain stage inside the ADC varies between -24 dB to 21.5 dB. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps. For more information, contact QTIL.

Digital Gain Selection Value	ADC Digital Gain Setting (dB)	Digital Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 8.1: ADC Audio Input Gain Rate

The firmware controls the audio input gain.

### 8.2.7 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A *long* IIR filter suitable for music (>44.1 kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8 kHz / 16 kHz / voice)

For more information, contact QTIL.

## 8.2.8 DAC

The DAC consists of:

- 1 fourth-order Sigma-Delta converter
- 2 gain stages, 1 of which is an analogue gain stage and the other is a digital gain stage

## 8.2.9 DAC Sample Rate Selection

The DAC supports the following sample rates:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz
- 32 kHz
- 40 kHz
- 44.1 kHz
- 48 kHz
- 96 kHz

## 8.2.10 DAC Digital Gain

Table 8.2 shows that a digital gain stage inside the DAC varies between -24 dB to 21.5 dB. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact QTIL.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

**Table 8.2: DAC Digital Gain Rate Selection**

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

## 8.2.11 DAC Analogue Gain

Table 8.3 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3 dB steps.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

**Table 8.3: DAC Analogue Gain Rate Selection**

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

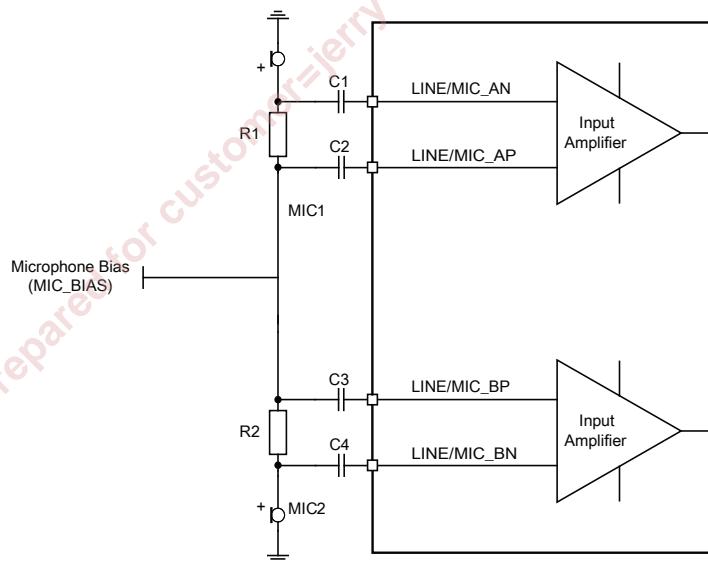
### 8.2.12 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default *long* FIR filter for best performance at  $\geq 44.1$  kHz.
- A *short* FIR to reduce latency.
- A *narrow* FIR (a very sharp roll-off at Nyquist) for G.722 compliance. Best for 8 kHz / 16 kHz.

### 8.2.13 Analogue Microphone Input

CSRA63120 A11 QFN contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condenser microphones. Figure 8.4 shows a biasing circuit for microphones with a sensitivity between about -40 to -60 dB (0 dB = 1 V/Pa).



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**Figure 8.4: Microphone Biasing**

**Where:**

- The microphone bias generator derives its power from VBAT or VOUT\_3V3 and requires no capacitor on its output.
- The microphone bias generator maintains regulation within the limits 70  $\mu$ A to 2.8 mA, supporting a 2 mA source typically required by 2 electret condenser microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
- Biasing resistors R1 and R2 are 2.2 k $\Omega$ .

- The input impedance at LINE/MIC\_AN and LINE/MIC\_AP is typically 6 kΩ.
- C1 and C2 are 100/150 nF if bass roll-off is required to limit wind noise on the microphone.
- R1 and R2 set the microphone load impedance and are normally around 2.2 kΩ.

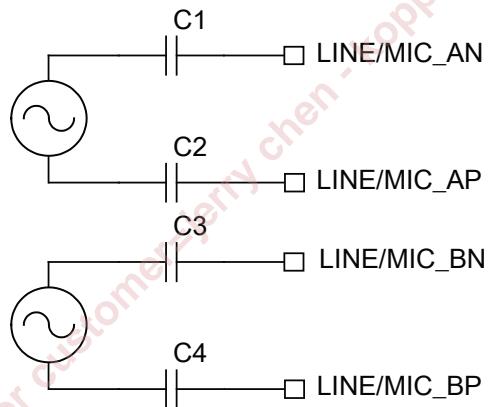
The microphone bias characteristics include:

- Power supply:
  - CSRA63120 A11 QFN microphone supply is VBAT or VOUT\_3V3
  - Minimum input voltage = Output voltage + drop-out voltage
  - Maximum input voltage is 4.3 V
- Drop-out voltage:
  - 300 mV maximum
- Output voltage:
  - 1.8 V or 2.6 V
  - Tolerance 90% to 110%
- Output current:
  - 70 µA to 2.8 mA
- No load capacitor required

## 8.2.14 Line Input

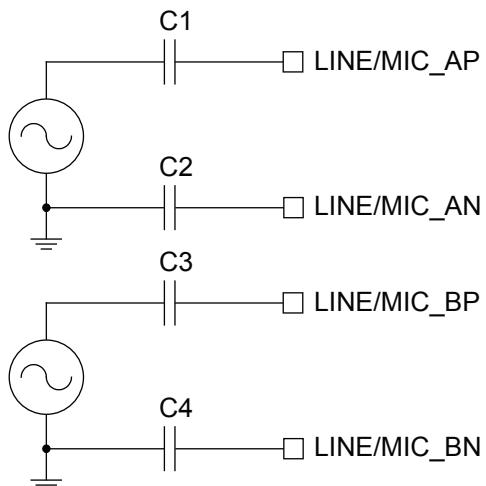
Figure 8.5 and Figure 8.6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

In line input mode, the input impedance of the pins to ground varies from 6 kΩ to 34 kΩ depending on input gain setting.



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Figure 8.5: Differential Input



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Figure 8.6: Single-ended Input

### 8.2.15 Digital Microphone Inputs

The CSRA63120 A11 QFN interfaces to 2 digital microphone inputs. Figure 8.2 shows the interface between the codec and the digital microphone interface, and that the digital microphone interface on the CSRA63120 A11 QFN has:

- Clock lines linked to any even-numbered PIO as determined by the firmware.
- Data lines linked to any odd-numbered PIO as determined by the firmware.

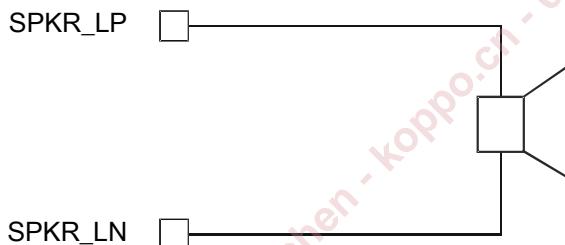
**Note:**

- For the digital microphone interface to work in this configuration, ensure the microphone uses a tristate between edges.
- The left and right selection for the digital microphones are appropriately pulled up or down for selection on the PCB.

### 8.2.16 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 8.7 shows that the output is available as a differential signal between SPKR\_LP and SPKR\_LN.

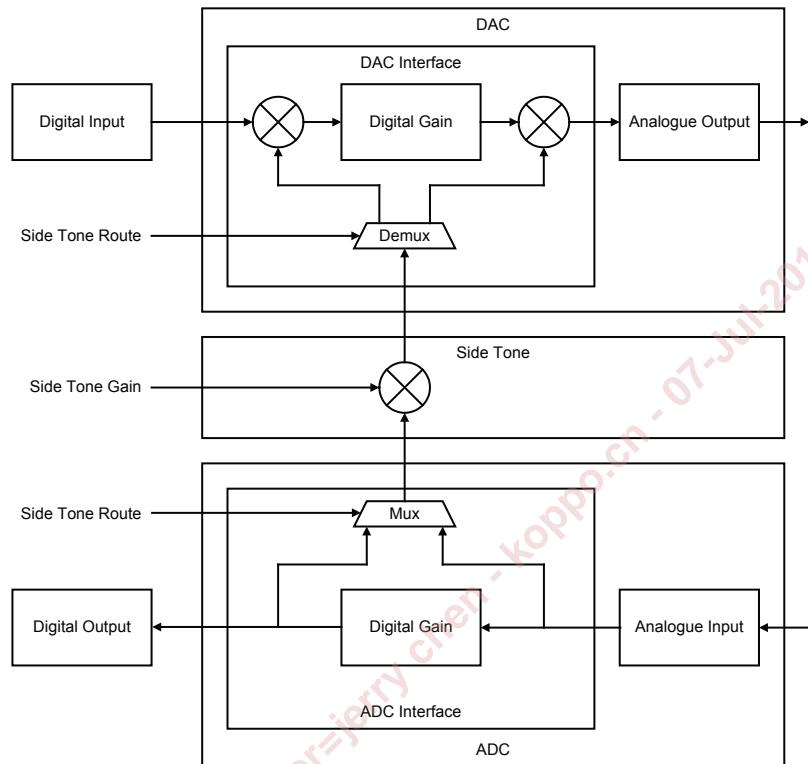


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Figure 8.7: Speaker Output

### 8.2.17 Side Tone

In some applications it is necessary to implement side tone. This side tone function involves feeding a properly gained microphone signal in to the DAC stream, e.g. earpiece. The side tone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface, see Figure 8.8.



**Figure 8.8: Side Tone**

The ADC provides simple gain to the side tone data. The gain values range from -32.6 dB to 12.0 dB in alternating steps of 2.5 dB and 3.5 dB, see Table 8.4.

Value	Side Tone Gain	Value	Side Tone Gain
0	-32.6 dB	8	-8.5 dB
1	-30.1 dB	9	-6.0 dB
2	-26.6 dB	10	-2.5 dB
3	-24.1 dB	11	0 dB
4	-20.6 dB	12	3.5 dB
5	-18.1 dB	13	6.0 dB
6	-14.5 dB	14	9.5 dB
7	-12.0 dB	15	12.0 dB

**Table 8.4: Side Tone Gain**



**Note:**

The values of side tone are shown for information only. During standard operation, the application software controls the side tone gain.

The following PS Keys configure the side tone hardware:

- PSKEY\_SIDE\_TONE\_ENABLE
- PSKEY\_SIDE\_TONE\_GAIN
- PSKEY\_SIDE\_TONE\_AFTER\_ADC
- PSKEY\_SIDE\_TONE\_AFTER\_DAC

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## 9 Power Control and Regulation

For greater power efficiency the CSRA63120 A11 QFN contains 2 switch-mode regulators:

- 1 generates a 1.80 V supply rail with an output current of 185 mA, see Section 9.1.
- 1 generates a 1.35 V supply rail with an output current of 160 mA, see Section 9.2.

CSRA63120 A11 QFN contains 4 LDO linear regulators:

- 3.30 V bypass regulator, see Section 9.4.
- 0.85 V to 1.25 V VDD\_DIG linear regulator, see Section 9.5.
- 1.35 V VDD\_AUX linear regulator, see Section 9.6.
- 1.35 V VDD\_ANA linear regulator, see Section 9.7.

The recommended configurations for power control and regulation on the CSRA63120 A11 QFN are:

- A 1.80 V and 1.35 V dual-supply rail system using the 1.80 V and 1.35 V switch-mode regulators, see Figure 9.1. This is the recommended power control and regulation configuration for CSRA63120 A11 QFN.
- A linear configuration using an external 1.8 V rail not using the switch-mode regulators

Other combinations of switch-mode and LDO are possible, but with limitations. For more information, contact QTIL.

Table 9.1 shows settings for the recommended configurations for power control and regulation on the CSRA63120 A11 QFN.

Supply Configuration	Regulators				Supply Rail	
	Switch-mode		VDD_AUX Linear Regulator	VDD_ANA Linear Regulator		
	1.8 V	1.35 V			1.8 V	1.35 V
Dual-supply SMPS	ON	ON	OFF	OFF	SMPS	SMPS
Linear supply	OFF	OFF	ON	ON	External	LDO

Table 9.1: Recommended Configurations for Power Control and Regulation

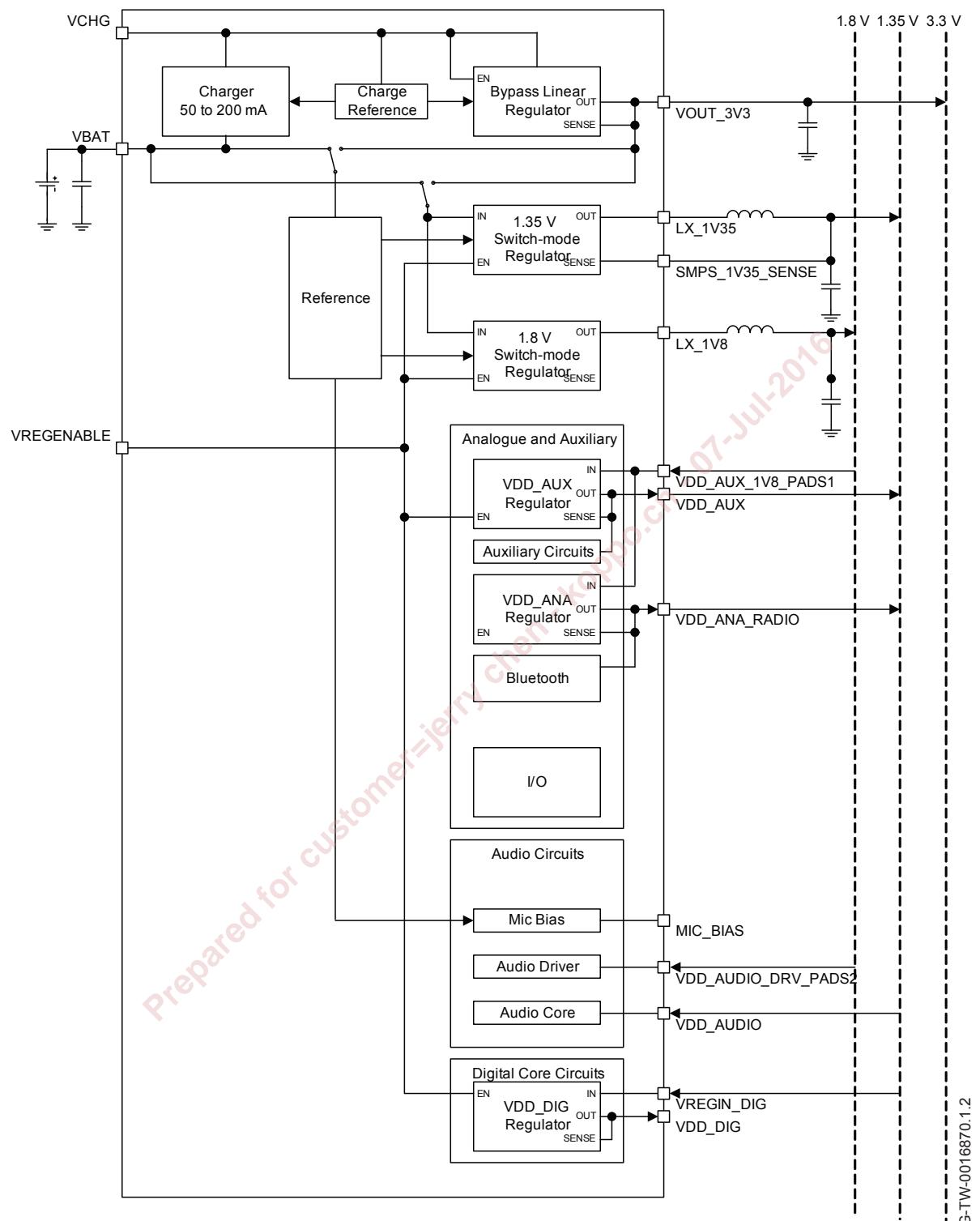
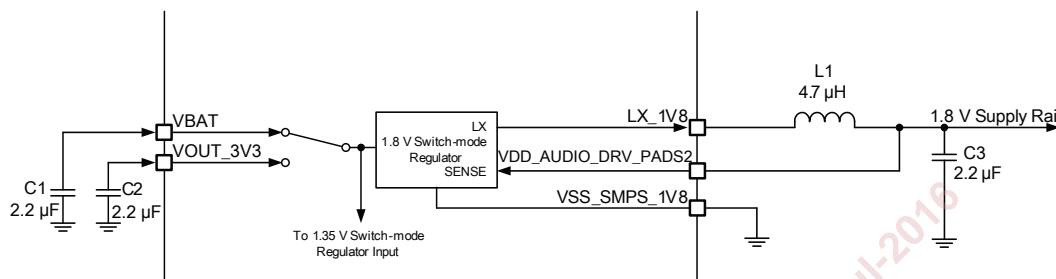


Figure 9.1: 1.80 V and 1.35 V Dual-supply Switch-mode System Configuration

## 9.1 1.8 V Switch-mode Regulator

QTIL recommends using the integrated switch-mode regulator to power the 1.80 V supply rail.

Figure 9.2 shows that an external LC filter circuit of a low-resistance series inductor, L1 (4.7  $\mu$ H), followed by a low ESR shunt capacitor, C3 (2.2  $\mu$ F), is required between the LX\_1V8 terminal and the 1.80 V supply rail. Connect the 1.80 V supply rail and the VDD\_AUDIO\_DRV\_PADS2 pin.



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**Figure 9.2: 1.8 V Switch-mode Regulator Output Configuration**

Minimise the series resistance of the tracks between the regulator input, VBAT and VOUT\_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS\_SMPS\_1V8.

Also minimise the collective parasitic capacitance on the track between LX\_1V8 and the inductor L1, to maximise efficiency.

For the regulator to meet its specifications it requires a total resistance of <1.0  $\Omega$  (<0.5  $\Omega$  recommended) for the following:

- The track between the battery and VBAT.
- The track between LX\_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80 V supply rail.

The following enable the 1.80 V switch-mode regulator:

- VREGENABLE pin
- The CSRA63120 A11 QFN firmware with reference to PSKEY\_PSU\_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00 MHz using PSKEY\_SMPS\_FREQ\_OFFSET, which also affects the 1.35 V switch-mode regulator.

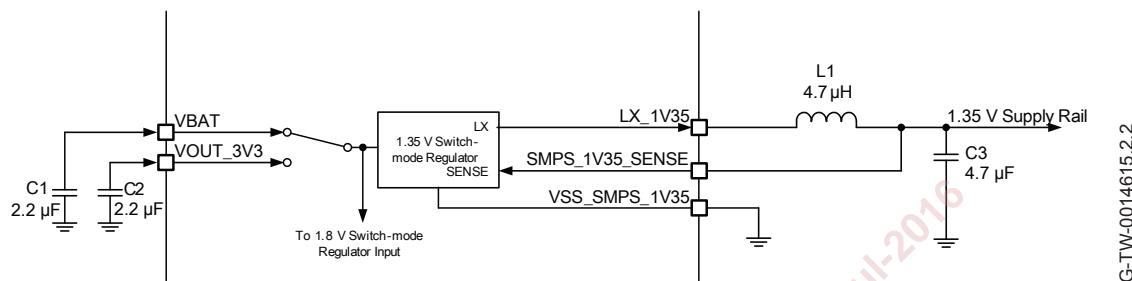
When the 1.80 V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and VOUT\_3V3
- The regulator output LX\_1V8

## 9.2 1.35 V Switch-mode Regulator

QTIL recommends using the integrated switch-mode regulator to power the 1.35 V supply rail.

Figure 9.3 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7  $\mu$ H), followed by a low ESR shunt capacitor, C3 (4.7  $\mu$ F), is required between the LX\_1V35 terminal and the 1.35 V supply rail. Connect the 1.35 V supply rail and the SMPS\_1V35\_SENSE pin.



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**Figure 9.3: 1.35 V Switch-mode Regulator Output Configuration**

Minimise the series resistance of the tracks between the regulator input, VBAT and VOUT\_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS\_SMPS\_1V35.

Also minimise the collective parasitic capacitance on the track between LX\_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet its specifications it requires a total resistance of <1.0  $\Omega$  (<0.5  $\Omega$  recommended) for the following:

- The track between the battery and VBAT.
- The track between LX\_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.35 V supply rail.

The following enable the 1.35 V switch-mode regulator:

- VREGENABLE pin
- The CSRA63120 A11 QFN firmware with reference to PSKEY\_PSU\_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00 MHz using PSKEY\_SMPS\_FREQ\_OFFSET, which also affects the 1.80 V switch-mode regulator.

When the 1.35 V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and VOUT\_3V3
- The regulator output LX\_1V35

### 9.3 Inductor Choice

Correct switch-mode power supply performance depends on inductor choice. A key parameter is the saturation current of the inductor. As an inductor saturates, its effective inductance decreases significantly, leading to the switching currents increasing further. This can eventually lead to:

- Poor regulator performance
- RF interference
- Possible instability

QTIL recommends inductor selection ensures that the inductance reduction at 250 mA is less than 30% of nominal inductance. This is often stated as the inductor parameter *Rated Current (L change) Max* and the value is the current at which the rated inductance has fallen by a specified percentage.

**Note:**

Some inductor manufacturers state the inductor's rated current as the temperature rise (DC current at which the inductor temperature increases by a specified temperature). This is not the same as saturation current.

The saturation performance can be particularly poor with small package inductors.

Another key inductor parameter is the DC resistance, because high DC resistance in the inductor decreases switch-mode power supply efficiency.

**Note:**

Pay attention to the frequency for the inductor specified parameters. The switch-mode power supply operates at 4 MHz, so inductor parameters should be stated at 4 MHz or higher.

Within QTIL, all testing and characterisation is carried out on boards using Taiyo-Yuden CB2012T4R7M parts in a 0805 (2012 metric) package.

Table 9.2 lists the required inductor specifications.

Parameter	Min	Typ	Max	Unit
Nominal inductance value ( $\pm 20\%$ tolerance)	3.84	4.7	5.64	$\mu\text{H}$
Inductor $R_{dc}$ for SMPS stability	0.1	0.25	1	$\Omega$
Inductor $R_{dc}$ for SMPS efficiency	0.1	0.25	0.4	$\Omega$
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor self-resonant frequency	10	-	-	MHz
Direct capacitance on SMPS output (including tolerance and de-rating)	1.5	2.2 / 4.7	10	$\mu\text{F}$

Table 9.2: Inductor Choice, QTIL's Testing and Characterisation

### 9.4 Bypass LDO Linear Regulator

The integrated bypass LDO linear regulator is available as a 3.30 V supply rail and is an alternative supply rail to the battery supply. This is especially useful when the battery has no charge and the CSRA63120 A11 QFN needs to power up. The input voltage should be between 4.25 V to 6.50 V.

**Note:**

The integrated bypass LDO linear regulator can operate down to 3.1 V with a reduced performance.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 2.2  $\mu\text{F}$  to the VOUT\_3V pin.

The output voltage is switched on when VCHG gets above 3.0 V.

This regulator starts in a low power mode, and is not designed to power external circuitry other than that shown in the application schematics in Section 11.

## 9.5 Low-voltage VDD\_DIG Linear Regulator

The integrated low-voltage VDD\_DIG linear regulator powers the digital circuits on CSRA63120 A11 QFN. Externally decouple the output of this regulator using a low ESR MLC capacitor of 470 nF.

## 9.6 Low-voltage VDD\_AUX Linear Regulator

The integrated low-voltage VDD\_AUX linear regulator is optionally available to provide a 1.35 V auxiliary supply rail when the 1.35 V switch-mode regulator is not used. When using the integrated low-voltage VDD\_AUX linear regulator, externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 470 nF to the VDD\_AUX pin.

## 9.7 Low-voltage VDD\_ANA Linear Regulator

The integrated low-voltage VDD\_ANA linear regulator is optionally available to power the 1.35 V analogue supply rail when the 1.35 V switch-mode regulator is not used. When using the integrated low-voltage VDD\_ANA linear regulator, externally decouple the output of this regulator using a 2.2  $\mu$ F low ESR MLC capacitor to the VDD\_ANA pin.

## 9.8 Voltage Regulator Enable

When using the integrated regulators the voltage regulator enable pin, VREGENABLE, enables the CSRA63120 A11 QFN and the following regulators:

- 1.8 V switch-mode regulator
- 1.35 V switch-mode regulator
- Low-voltage VDD\_DIG linear regulator
- Low-voltage VDD\_AUX linear regulator

The VREGENABLE pin is active high, with a pull-down, typical 100 k $\Omega$ , which is disabled by PSKEY\_VREG\_ENABLE\_STRONG\_PULL.

CSRA63120 A11 QFN boots-up when the voltage regulator enable pin is pulled high typically for 10 to 15 ms, enabling the regulators. The firmware then latches the regulators on. The voltage regulator enable pin can then be released.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

**Note:**

VREGENABLE should be asserted after the VBAT supply when VREGENABLE is not used as a power-on button.

## 9.9 External Regulators and Power Sequencing

QTIL recommends that the integrated regulators supply the CSRA63120 A11 QFN and it is configured based on the information in this data sheet.

If any of the supply rails for the CSRA63120 A11 QFN are supplied from an external regulator, then it should match or be better than the internal regulator available on CSRA63120 A11 QFN. For more information see regulator characteristics in Section 12.

**Note:**

The internal regulators described in Section 9.1 to Section 9.7 are not recommended for external circuitry other than that shown in Section 11.

For information about power sequencing of external regulators to supply the CSRA63120 A11 QFN, contact QTIL.

## 9.10 Reset

CSRA63120 A11 QFN is reset from several sources:

- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

**Note:**

Reset can also be triggered by a UART break symbol if:

- Host interface is any UART transport and
- PSKEY\_HOSTIO\_UART\_RESET\_TIMEOUT is set to a non-zero value (>1000)

A warm reset function is also available under software control. After a warm reset RAM data remains available.

### 9.10.1 Digital Pin States on Reset

Table 9.3 shows the pin states of CSRA63120 A11 QFN on reset.

Pin Name	I/O Type	Full Chip Reset	Pin Name	I/O Type	Full Chip Reset
USB_DP	Digital bidirectional	N/A	PIO[4]	Digital bidirectional	PDW
USB_DN	Digital bidirectional	N/A	PIO[5]	Digital bidirectional	PDW
PIO[0]	Digital bidirectional	PUS	PIO[6]	Digital bidirectional	PDS
PIO[1]	Digital bidirectional	PUS	PIO[7]	Digital bidirectional	PDS
PIO[2]	Digital bidirectional	PDW	PIO[8]	Digital bidirectional	PUS
PIO[3]	Digital bidirectional	PDW	PIO[9]	Digital bidirectional	PDS

Table 9.3: Pin States on Reset

**Note:**

PUS = Strong pull-up

PDS = Strong pull-down

PUW = Weak pull-up

PDW = Weak pull-down

### 9.10.2 Status After Reset

The status of CSRA63120 A11 QFN after a reset is:

- Warm reset: baud rate and RAM data remain available
- Cold reset: baud rate and RAM data not available

## 9.11 Automatic Reset Protection

CSRA63120 A11 QFN includes an automatic reset protection circuit which restarts/resets CSRA63120 A11 QFN when an unexpected reset occurs, e.g. ESD strike. The automatic reset protection circuit enables resets from the on-chip application without the requirement for external circuitry.

**Note:**

The reset protection is cleared after typically 2 s (1.6 s min to 2.4 s max).

## 10 Battery Charger

### 10.1 Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the on-chip application. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see Table 10.1 and Figure 10.1.

Mode	Battery Charger Enabled	VBAT
Disabled	No	X
Trickle charge	Yes	$>V_{fast}$ and $<V_{float}$
Fast charge	Yes	$>V_{fast}$ and $<V_{float}$
Standby	Yes	$I_{term}^{(a)}$ and $>(V_{float} - V_{hyst})$
Error	Yes	$>(V_{CHG} - 50mV)$

Table 10.1: Battery Charger Operating Modes Determined by Battery Voltage and Current

(a)  $I_{term}$  is approximately 10% of  $I_{fast}$  for a given  $I_{fast}$  setting

Figure 10.1 shows the mode-to-mode transition voltages. These voltages are fixed and calibrated by QTIL. The transition between modes can occur at any time.

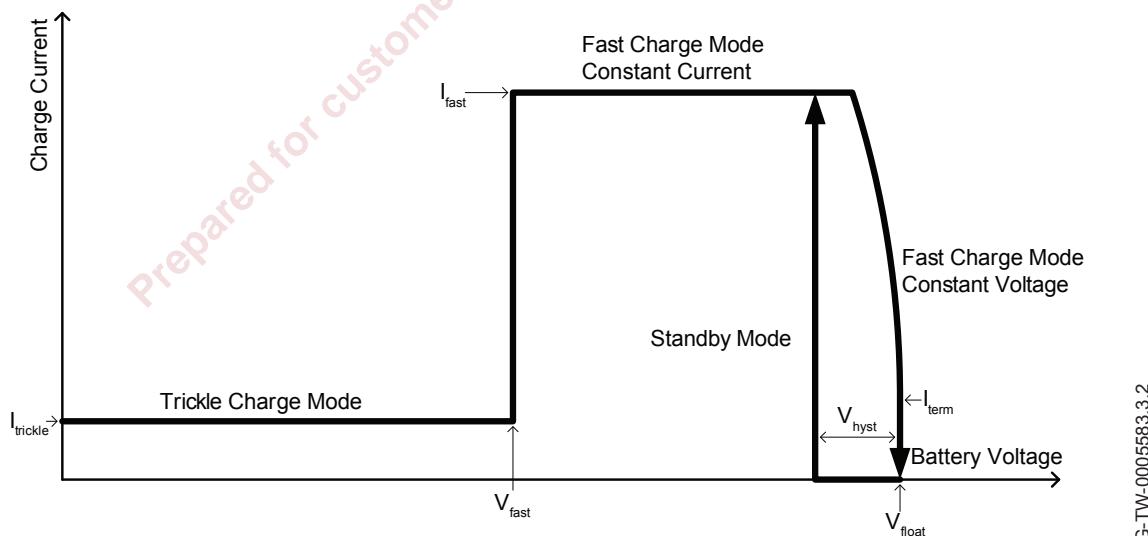


Figure 10.1: Battery Charger Mode-to-Mode Transition Diagram

**Note:**

The battery voltage remains constant in Fast Charge Constant Voltage Mode, the curved line on Figure 10.1 is for clarity only.

### 10.1.1 Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

### 10.1.2 Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT is lower than the  $V_{fast}$  threshold, a current of approximately 10% of the fast charge current,  $I_{fast}$ , is sourced from the VBAT pin.

The  $V_{fast}$  threshold detection has hysteresis to prevent the charger from oscillating between modes.

### 10.1.3 Fast Charge Mode

When the voltage on VBAT is greater than  $V_{fast}$ , the current sourced from the VBAT pin increases to  $I_{fast}$ .  $I_{fast}$  is between 10 mA and 200 mA set by PS Key or a on-chip application. In addition,  $I_{fast}$  is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at  $I_{fast}$  until the voltage at VBAT reaches  $V_{float}$ , then the charger reduces the current sourced to maintain a constant voltage on the VBAT pin.

When the current sourced is below the termination current,  $I_{term}$ , the charging stops and the charger enters standby mode.  $I_{term}$  is typically 10% of the fast charge current.

### 10.1.4 Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT pin is monitored, and when it drops below a threshold set at  $V_{hyst}$  below the final charging voltage,  $V_{float}$ , the charger re-enters fast charge mode.

### 10.1.5 Error Mode

The charger enters the error mode if the voltage on the VCHG pin is too low to operate the charger correctly (VBAT is greater than VCHG - 50 mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

## 10.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written by QTIL into non-volatile memory when each IC is characterised. QTIL provides various PS Keys for overriding the default trims.

## 10.3 On-chip Application Battery Charger Control

The on-chip application charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information
- Driving the user visible charger status LED(s)

## 10.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and A called from the on-chip application charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

For more information on the CSRA63120 A11 QFN, including details on setting up, calibrating, trimming and the PS Keys, see *Lithium Polymer Battery Charger Calibration and Operation for CSR8670* application note.

## 11 Example Application Schematic

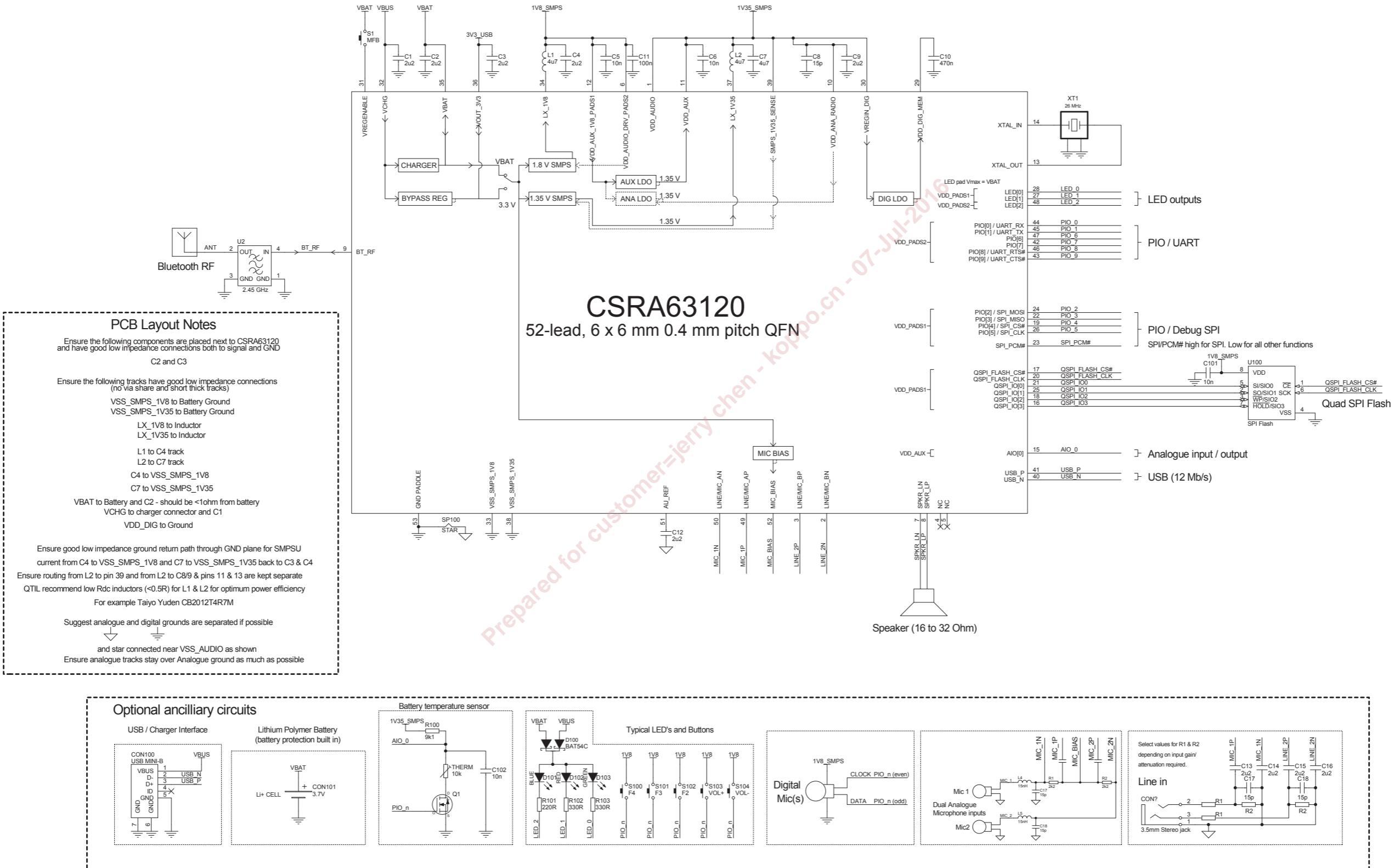


Figure 11.1: Example Application Schematic

## Single 1.8 V only supply. No USB, No switchmodes

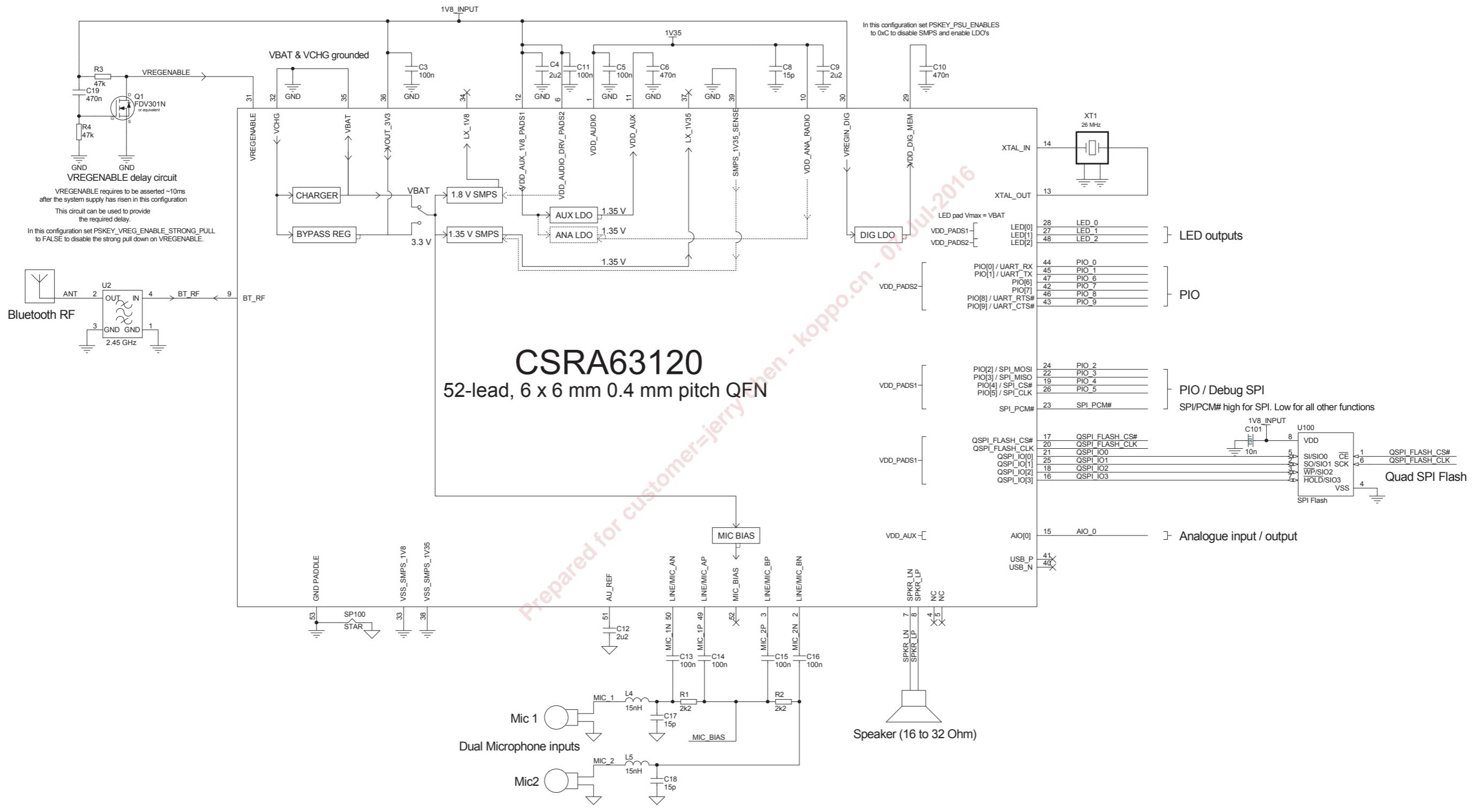


Figure 11.2: Single 1.8 V-only Supply, with no USB or SMPSs

## Single 3.3 V only supply. USB, Dual switchmodes

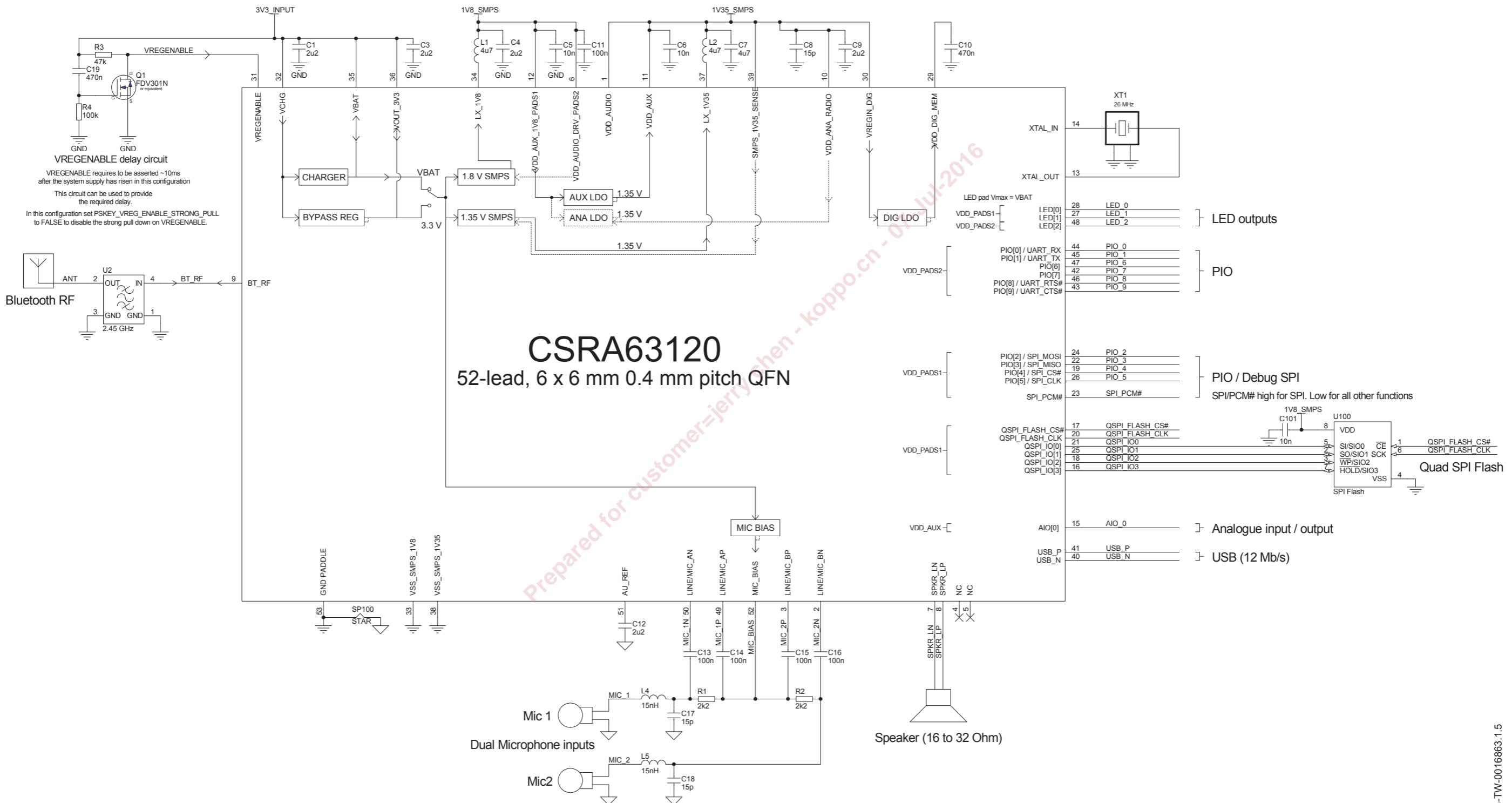


Figure 11.3: Single 3.3 V-only Supply, with USB and Dual SMPSS

## 12 Electrical Characteristics

### 12.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	°C
<b>Supply Voltage</b>				
Charger	VCHG	-0.4	6.50	V
LEDs	LED[2:0]	-0.4	4.40	V
3.3 V	VOUT_3V3	-0.4	3.60	V
Battery	VBAT	-0.4	4.40	V
	VREGENABLE	-0.4	4.40	V
PIO	VDD_AUX_1V8_PADS1	-0.4	1.95	V
	VDD_AUDIO_DRV_PADS2	-0.4	1.95	V
1.35 V	SMPS_1V35_SENSE	-0.4	1.45	V
	VDD_AUDIO	-0.4	1.45	V
	VREGIN_DIG	-0.4	1.95	V
	VDD_ANA_RADIO	-0.4	1.45	V
Other terminal voltages		VSS - 0.4	VDD + 0.4 ≤ 3.60 <sup>(a)</sup>	V

<sup>(a)</sup> VDD is the VDD\_\*\_PADS supply domain for this I/O. For more information, see Section 1.2. Voltage should not exceed 3.6 V on any I/O.

## 12.2 Recommended Operating Conditions

Rating		Min	Typ	Max	Unit
Operating temperature range		-40	20	85	°C
<b>Supply Voltage</b>					
Charger	VCHG	4.75 / 3.10 <sup>(a)</sup>	5.00	6.50	V
LEDs	LED[2:0]	1.10	3.70	4.30	V
3.3 V	VOUT_3V3	3.10	3.30	3.60	V
Battery	VBAT	0	3.70	4.25	V
	VREGENABLE	0	3.70	4.25	V
PIO	VDD_AUX_1V8_PADS1	1.70	1.80	1.95	V
	VDD_AUDIO_DRV_PADS2	1.70	1.80	1.95	V
1.35 V	SMPS_1V35_SENSE	1.30	1.35	1.45	V
	VDD_AUDIO	1.30	1.35	1.45	V
	VREGIN_DIG	1.30	1.35 or 1.80 <sup>(b)</sup>	1.95	V
	VDD_ANA_RADIO	1.30	1.35	1.40	V

<sup>(a)</sup> Minimum input voltage of 4.75 V is required for full specification. Regulator operates at reduced load current from 3.1 V.

<sup>(b)</sup> Typical value depends on output required by the low-voltage VDD\_DIG linear regulator, see Section 12.3.2.2.

## 12.3 Input/Output Terminal Characteristics

### Note:

For all I/O terminal characteristics:

- Current drawn into a pin is defined as positive. Current supplied out of a pin is defined as negative.

### 12.3.1 Regulators: Available For External Use

#### 12.3.1.1 1.8 V Switch-mode Regulator

1.8 V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.70	4.25	V
Output voltage	1.70	1.80	1.90	V
<b>Normal Operation</b>				
Transient settling time	-	30	-	μs
Load current	-	-	185	mA
Current available for external use, audio with 16 Ω load <sup>(a)</sup>	-	-	25	mA
Peak conversion efficiency <sup>(b)</sup>	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
<b>Low-power Mode, Automatically Entered in Deep Sleep</b>				
Transient settling time	-	200	-	μs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

<sup>(a)</sup> More current available for audio loads above 16 Ω.

<sup>(b)</sup> Conversion efficiency depends on inductor selection.

### 12.3.1.2 Bypass LDO Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	4.25 / 3.10 <sup>(a)</sup>	5.00	6.50	V
Output voltage ( $V_{in} > 4.75$ V)	3.00	3.30	3.60	V
Output current ( $V_{in} > 4.75$ V) <sup>(b)</sup>	-	-	250	mA

(a) Minimum input voltage of 4.25 V is required for full specification, regulator operates at reduced load current from 3.1 V.

(b) This regulator starts in a low power mode, and is not designed to power external circuitry other than that shown in the application schematics in Section 11.

### 12.3.2 Regulators: For Internal Use Only

#### 12.3.2.1 1.35 V Switch-mode Regulator

1.35 V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.60	4.25	V
Output voltage	1.30	1.35	1.40	V
Normal Operation				
Transient settling time	-	30	-	μs
Load current	-	-	160	mA
Current available for external use	-	-	0	mA
Peak conversion efficiency <sup>(a)</sup>	-	88	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	μs
Load current	0.005	-	5	mA
Current available for external use	-	-	0	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

(a) Conversion efficiency depends on inductor selection.

### 12.3.2.2 Low-voltage VDD\_DIG Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.30	1.35 or 1.80	1.95	V
Output voltage <sup>(a)</sup>	0.80	0.90 / 1.20	1.25	V
Internal load current	-	-	80	mA

(a) Output voltage level is software controlled.

### 12.3.2.3 Low-voltage VDD\_AUX Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage	1.30	1.35	1.45	V
Internal load current	-	-	5	mA

### 12.3.2.4 Low-voltage VDD\_ANA Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage	1.30	1.35	1.45	V
Load current	-	-	60	mA

### 12.3.3 Regulator Enable

VREGENABLE, Switching Threshold	Min	Typ	Max	Unit
Rising threshold	-	-	1.0	V

### 12.3.4 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage, VCHG	4.75 / 3.10 <sup>(a)</sup>	5.00	6.50	V

(a) Reduced specification from 3.1 V to 4.75 V. Full specification >4.75 V.

Trickle Charge Mode	Min	Typ	Max	Unit
Charge current $I_{\text{trickle}}$ , as percentage of fast charge current	8	10	12	%
$V_{\text{fast}}$ rising threshold	-	2.9	-	V
$V_{\text{fast}}$ rising threshold trim step size	-	0.1	-	V
$V_{\text{fast}}$ falling threshold	-	2.8	-	V

Fast Charge Mode	Min	Typ	Max	Unit
Charge current during constant current mode, $I_{\text{fast}}$	Maximum charge setting ( $V_{\text{CHG}}-V_{\text{BAT}} > 0.55 \text{ V}$ )	194	200	206 mA
	Minimum charge setting ( $V_{\text{CHG}}-V_{\text{BAT}} > 0.55 \text{ V}$ )	-	10	- mA
Reduced headroom charge current, as a percentage of $I_{\text{fast}}$	( $V_{\text{CHG}}-V_{\text{BAT}} < 0.55 \text{ V}$ )	50	-	100 %
Charge current step size	-	10	-	mA
$V_{\text{float}}$ threshold, calibrated	4.16	4.20	4.24	V
Charge termination current $I_{\text{term}}$ , as percentage of $I_{\text{fast}}$	7	10	20	%

Standby Mode	Min	Typ	Max	Unit
Voltage hysteresis on $V_{\text{BAT}}$ , $V_{\text{hyst}}$	100	-	150	mV

Error Charge Mode	Min	Typ	Max	Unit
Headroom <sup>(a)</sup> error falling threshold	-	50	-	mV

<sup>(a)</sup> Headroom =  $V_{\text{CHG}} - V_{\text{BAT}}$

### 12.3.5 USB

USB	Min	Typ	Max	Unit
VOUT_3V3 for correct USB operation	3.1	3.3	3.6	V
<b>Input Threshold</b>				
V <sub>IL</sub> input logic level low	-	-	0.3 x VOUT_3V3	V
V <sub>IH</sub> input logic level high	0.7 x VOUT_3V3	-	-	V
<b>Output Voltage Levels to Correctly Terminated USB Cable</b>				
V <sub>OL</sub> output logic level low	0	-	0.2	V
V <sub>OH</sub> output logic level high	2.8	-	VOUT_3V3	V

### 12.3.6 Stereo Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	Conditions	Min	Typ	Max	Unit	
Resolution	-		-	16	Bits	
Input Sample Rate, $F_{\text{sample}}$	-		8	-	48	kHz
Maximum ADC Input Signal Amplitude	0 dB = 1600 mV <sub>pk-pk</sub>		13	-	2260	mV <sub>pk-pk</sub>
SNR	$f_{\text{in}} = 1 \text{ kHz}$ B/W = 20 Hz → $F_{\text{sample}}/2$ (20 kHz max) A-Weighted THD+N < 0.1% 1.6 V <sub>pk-pk</sub> input	$F_{\text{sample}}$				
		8 kHz	-	94.0	-	dB
		16 kHz	-	93.3	-	dB
		32 kHz	-	93.1	-	dB
		44.1 kHz	-	93.3	-	dB
		48 kHz	-	92.8	-	dB
THD+N	$f_{\text{in}} = 1 \text{ kHz}$ B/W = 20 Hz → $F_{\text{sample}}/2$ (20 kHz max) 1.6 V <sub>pk-pk</sub> input	$F_{\text{sample}}$				
		8 kHz	-	0.0041	-	%
		48 kHz	-	0.0080	-	%
Digital gain	Digital gain resolution = 1/32	-24	-	21.5	dB	
Analogue gain	Pre-amplifier setting = 0 dB, 9 dB, 21 dB or 30 dB Analogue setting = -3 dB to 12 dB in 3 dB steps	-3	-	42	dB	
Stereo separation (crosstalk)		-	-87.3	-	dB	

### 12.3.7 Stereo Codec: Digital to Analogue Converter

Digital to Analogue Converter						
Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Output Sample Rate, $F_{\text{sample}}$	-		8	-	96	kHz
SNR	$f_{\text{in}} = 1 \text{ kHz}$ B/W = 20 Hz → 20 kHz A-Weighted THD+N < 0.1% 0 dBFS input	$F_{\text{sample}}$	Load			
		48 kHz	100 kΩ	-	96.4	-
		48 kHz	32 Ω	-	96.3	-
		48 kHz	16 Ω	-	96.2	-
THD+N	$f_{\text{in}} = 1 \text{ kHz}$ B/W = 20 Hz → 20 kHz 0 dBFS input	$F_{\text{sample}}$	Load			
		8 kHz	100 kΩ	-	0.0022	-
		8 kHz	32 Ω	-	0.0022	-
		8 kHz	16 Ω	-	0.0023	-
		48 kHz	100 kΩ	-	0.0030	-
		48 kHz	32 Ω	-	0.0031	-
		48 kHz	16 Ω	-	0.0033	-
Digital Gain	Digital Gain Resolution = 1/32		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3 dB		-21	-	0	dB
Output voltage	Full-scale swing (differential)		-	-	778	mV rms
Stereo separation (crosstalk)			-	-90.0	-	dB

### 12.3.8 Digital

Digital Terminals	Min	Typ	Max	Unit
<b>Input Voltage</b>				
V <sub>IL</sub> input logic level low	-0.4	-	0.4	V
V <sub>IH</sub> input logic level high	0.7 x VDD	-	VDD + 0.4	V
Tr/Tf	-	-	25	ns
<b>Output Voltage</b>				
V <sub>OL</sub> output logic level low, I <sub>OL</sub> = 4.0 mA	-	-	0.4	V
V <sub>OH</sub> output logic level high, I <sub>OH</sub> = -4.0 mA	0.75 X VDD	-	-	V
Tr/Tf	-	-	5	ns
<b>Input and Tristate Currents</b>				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	1.0	5.0	µA
C <sub>I</sub> Input Capacitance	1.0	-	5.0	pF

### 12.3.9 LED Driver Pads

LED Driver Pads	Min	Typ	Max	Unit
Current, I <sub>PAD</sub>	High impedance state	-	-	5 µA
	Current sink state	-	-	10 mA
LED pad voltage, V <sub>PAD</sub>	I <sub>PAD</sub> = 10 mA	-	0.55	V
LED pad resistance	V <sub>PAD</sub> < 0.5 V	-	40	Ω
V <sub>OL</sub> output logic level low <sup>(a)</sup>	-	0	-	V
V <sub>OH</sub> output logic level high <sup>(a)</sup>	-	0.8	-	V
V <sub>IL</sub> input logic level low	-	0	-	V
V <sub>IH</sub> input logic level high	-	0.8	-	V

(a) LED output port is open-drain and requires a pull-up

### 12.3.10 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range <sup>(a)</sup>		0	-	VDD_AUX	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		1.38	1.69	2.75	μs
Sample rate <sup>(b)</sup>		-	-	700	Samples/s

(a) LSB size = VDD\_AUX/1023

(b) The auxiliary ADC is accessed through an on-chip application function. The sample rate given is achieved as part of this function.

### 12.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 12.1 shows the ESD handling maximum ratings.

Condition	Class	Max Rating
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2 kV (all pins)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500 V (all pins)

Table 12.1: ESD Handling Ratings

## 13 Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
N/A	Deep sleep	With UART host connection	-	-	54	µA
N/A	Page scan	Page = 1280 ms interval Window = 11.25 ms	-	-	230	µA
N/A	Inquiry and page scan	Inquiry = 1280 ms interval Page = 1280 ms interval Window = 11.25 ms	-	-	396	µA

**Note:**

These values exclude SPI Flash device current.

Mono Output						
Slave	SCO	Sniff = 100 ms	HV3	30	11.4	mA
Slave	eSCO	Sniff = 100 ms	EV3	30	12.4	mA
Slave	eSCO	Sniff = 100 ms	2EV3	60	9.7	mA
Slave	SCO	1-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	HV3	30	12.4	mA
Slave	eSCO	1-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	2EV3	60	10.7	mA
Slave	eSCO	1-mic cVc headset: ■ 16 kHz sampling ■ Wideband	2EV3	60	12.2	mA
Slave	SCO	2-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	HV3	30	13.9	mA
Slave	eSCO	2-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	2EV3	60	12.1	mA
Slave	eSCO	2-mic cVc headset: ■ 16 kHz sampling ■ Wideband	2EV3	60	14.0	mA
Master	SCO	Sniff = 100 ms	HV3	30	11.6	mA
Master	eSCO	Sniff = 100 ms	EV3	30	11.9	mA
Master	eSCO	Sniff = 100 ms	2EV3	60	9.5	mA

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Master	SCO	1-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	HV3	30	12.5	mA
Master	eSCO	1-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	2EV3	60	10.4	mA
Master	eSCO	1-mic cVc headset: ■ 16 kHz sampling ■ Wideband	2EV3	60	10.9	mA
Master	SCO	2-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	HV3	30	13.9	mA
Master	eSCO	2-mic cVc headset: ■ 8 kHz sampling ■ Narrowband	2EV3	60	11.8	mA
Master	eSCO	2-mic cVc headset: ■ 16 kHz sampling ■ Wideband	2EV3	60	12.6	mA

**Note:**

Current consumption values are taken with:

- VBAT pin = 3.7 V
- RF TX power set to 0 dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH classification master disabled

## 14 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction of Hazardous Substances directive guidelines in the EU RoHS Directive 2011/65/EU<sup>1</sup>.
- EU REACH, Regulation (EC) No 1907/2006<sup>1</sup>:
  - List of substances subject to authorisation (Annex XIV)
  - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
  - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)<sup>1</sup>.
- POP regulation (EC) No 850/2004<sup>1</sup>
- EU Packaging and Packaging Waste, Directive 94/62/EC<sup>1</sup>
- Montreal Protocol on substances that deplete the ozone layer.
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. CSR is a fabless semiconductor company: all manufacturing is performed by key suppliers. CSR have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. CSR shall provide a complete EICC / GeSI template upon request.

CSR has defined the "CSR Green" standard based on current regulatory and customer requirements including free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions CSR specify. For more information on the full "CSR Green" standard, contact [product.compliance@csr.com](mailto:product.compliance@csr.com).

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<sup>1</sup> Including applicable amendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

## 15 Software

CSRA63120 A11 QFN:

- Includes integrated Bluetooth v4.2 specification qualified HCI stack firmware
- Includes integrated CSRA63120 Mono ROM Solution, with 8<sup>th</sup> generation 1 and 2-mic cVc headset audio enhancements and a configurable EQ
- Can be shipped with QTIL's CSRA63120 mono ROM solution development kit for CSRA63120 A11 QFN, order code DK-CSRA63120-10273-1A

The CSRA63120 A11 QFN software architecture enables Bluetooth processing and the application program to run on the internal RISC MCU and the audio enhancements on the Kalimba DSP.

### 15.1 CSRA63120 Mono ROM Solution

The CSRA63120 mono ROM solution software supports:

- 8<sup>th</sup> generation 1 and 2-mic cVc hands-free audio enhancements
- WNR
- PLC / BEC
- mSBC wideband speech codec
- A2DP v1.3
- HFP v1.6 and HSP v1.2
- SCMS-T
- Bluetooth v4.2 specification is supported in the ROM software
- Secure simple pairing
- Proximity pairing (headset-initiated pairing) for greatly simplifying the out-of-box pairing process
- For connection to more than 1 mobile phone, Advanced Multipoint is supported. This enables a user to take calls from a work and personal phone or a work phone and a VoIP dongle for Skype users. This has minimal impact on power consumption and is easy to configure.
- Most of the CSRA63120 mono ROM solution ROM software features are configured on the CSRA63120 A11 QFN using the 63xxx ROM Series Configuration Tool. The tool reads and writes headset configurations directly to the serial flash or alternatively to a PSR file. Configurable headset features include:
  - Bluetooth v4.2 specification features
  - Reconnection policies, e.g. reconnect on power-on
  - Audio features, including default volumes
  - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for last number redial
  - LED indications for states, e.g. headset connected, and events, e.g. power on
  - Indication tones for events and ringtones
  - HFP v1.6 supported features
  - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
  - Advanced Multipoint settings
- User configurable EQ for music playback (rock, pop, classical, jazz, dance etc)
- Manufacturer configurable Speaker EQ with 10 stages
- AAC and SBC
- TrueWireless Stereo (TWS)
- Stereo widening (S3D)
- MeloD Expansion 3D stereo widening and phase shifting effect
- Volume Boost
- USB audio mode for streaming high-quality music from a PC whilst charging, enables the headset to:
  - Play back high-quality stereo music, e.g. iTunes
  - Use bidirectional audio in conversation mode, e.g. for Skype
- Wired audio mode for pendant-style headsets supports music playback using a line-in jack. Enables non Bluetooth operation in low battery modes or when using the headset in an airplane-mode.
- Support for smartphone applications (apps)
- The CSRA63120 mono ROM solution has undergone extensive interoperability testing to ensure it works with the majority of phones on the market

### 15.1.1 Advanced Multipoint Support

Advanced Multipoint enables the connection of 2 devices to a CSRA63120 A11 QFN headset at the same time, examples include:

- 2 phones connected to a CSRA63120 A11 QFN headset
- Phone and a VoIP dongle connected to a CSRA63120 A11 QFN headset
- Phone and tablet

The CSRA63120 mono ROM solution:

- Supports up to 2 simultaneous connections (either HFP or HSP)
- Enables multiple-call handling from both devices at the same time
- Treats all headset buttons:
  - During a call from one device, as if there is 1 device connected
  - During multiple calls (1 on each device), as if there is a single AG with multiple calls in progress (three-way calling)
  - During multiple calls (more than 1 on each device), as if there are multiple calls on a single device enabling the user to switch between the active and held calls

### 15.1.2 A2DP Multipoint Support

A2DP Multipoint support enables the connection of 2 A2DP source devices to CSRA63120 A11 QFN at the same time, examples include:

- 2 A2DP-capable phones connected to a CSRA63120 A11 QFN headset
- A2DP-capable phone and an A2DP-only source device, e.g. a PC or an iPod touch

The CSRA63120 mono ROM solution enables:

- Music streaming from either of the connected A2DP source devices where the music player is controlled on the source device
- Advanced HFP Multipoint functions to interrupt music streaming for calls, and resume music streaming on the completion of the calls
- AVRCP v1.6 connections to both connected devices, enabling the headset to remotely control the primary device, i.e. the device currently streaming audio

### 15.1.3 Wired Audio Mode

CSRA63120 A11 QFN supports a wired audio mode for playing music over a wired connection.

If CSRA63120 A11 QFN is powered, the audio path is routed through CSRA63120 A11 QFN, including via the DSP, this enables the CSRA63120 A11 QFN to:

- Mix audio sources, e.g. tones and programmable audio prompts
- Control the volume of the audio, i.e. volume up and volume down
- Utilise the 10-band Speaker EQ

In wired audio mode, if required, the CSRA63120 A11 QFN is still available for Bluetooth audio. This enables seamless transition from wired audio mode to Bluetooth audio mode and back again. This transition is configurable to occur automatically as the battery voltage of the headset reduces to a point at which Bluetooth audio is no longer possible.

The carrier board features a stereo line-in with detect.

### 15.1.4 USB Modes Including USB Audio Mode

CSRA63120 A11 QFN supports a variety of USB modes which enables the USB interface to extend the functionality of a CSRA63120 A11 QFN based stereo headset.

CSRA63120 A11 QFN supports:

- USB charger enumeration
- USB soundcard enumeration (USB audio mode)
- USB mass storage enumeration

USB audio mode enables the headset to enumerate as a soundcard while charging from a USB master device, e.g. a PC. In this mode, the headset enumerates as either a stereo music soundcard (for high quality music playback) or a bidirectional voice quality soundcard. This enables the headset for either listening to music streaming from the USB host device or for voice applications, e.g. Skype.

The USB audio mode operates at the same time as the wired audio mode and the USB audio interrupts the wired audio mode if USB audio is attached. This enables a headset to have both wired audio and USB modes connected at the same time.

In USB audio mode, if required, the headset is still available for Bluetooth audio.

### 15.1.5 Smartphone Applications (Apps)

CSRA63120 A11 QFN includes QTIL's proprietary mechanism for communicating with smartphone apps, it enables full UI control of the headset from within the application running on a smartphone, e.g. Google Android OS-based handset. For more information on this feature contact QTIL.

### 15.1.6 Programmable Audio Prompts

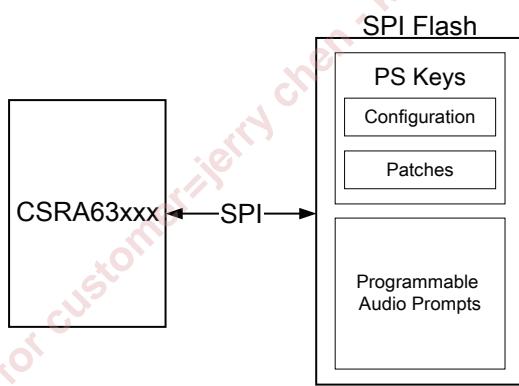
The CSRA63120 A11 QFN enables a user to configure and load pre-programmed audio prompts from an external SPI flash.

The programmable audio prompts provide a mechanism for higher-quality audio indications to replace standard tone indications. A programmable audio prompt is assigned to any user event in place of a standard tone.

Programmable audio prompts contain either voice prompts to indicate that events have occurred or provide user-defined higher quality ring tones/indications, e.g. custom power on/off tones. The CSRA63120 A11 QFN supports multiple languages for audio prompts.

The 63xxx ROM Series Configuration Tool can generate the content for the programmable audio prompts from standard WAV audio files. The tool also enables the user to configure which prompts are assigned to which user events.

Figure 15.1 shows the SPI flash interface.



G-TW-001678.12

Figure 15.1: Programmable Audio Prompts in External SPI Flash

### 15.1.7 QTIL's Intelligent Power Management

IPM extends the available talk time of a CSRA63120 A11 QFN-based headset, by automatically reducing the audio processing performed by cVc at a series of low battery capacity thresholds.

Configurable IPM features include:

- IPM enable/disable
- The battery capacity that engages IPM
- A user-action to enable or disable the IPM

If engaged, cVc processing reduces automatically on reaching the preset battery capacity. Once the audio is terminated, the DSP shuts down to achieve maximum power savings before the next call.

IPM resets when recharging the headset. The talk time extension depends on:

- The battery size
- The battery condition
- The threshold capacity configured for the IPM to engage

### 15.1.8 Proximity Pairing

Proximity pairing is headset-initiated pairing and it simplifies the out-of-box pairing process. Proximity pairing enables the headset to find the closest discoverable phone. The headset then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus to pair with the new headset.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the headset pairing is with a PIN code
- For a Bluetooth v2.1 (or above) phone the headset pairing is without a PIN code

Proximity pairing is based on finding and pairing with the closest phone. To do this, the headset finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and it is defined as the closest device. The headset then attempts to pair with and connect to this device.

Proximity pairing is configurable using the 63xxx ROM Series Configuration Tool available from [www.csrsupport.com](http://www.csrsupport.com).

### 15.1.9 Proximity Connection

Proximity connection is an extension to proximity pairing. It enables the headset-user to take advantage of the proximity of devices each time the headset powers up and not just during a first time pairing event.

Proximity connection enables a user with multiple handsets to easily connect to the closest discoverable phone by comparing the proximity of devices to the headset at power-on to the list of previously paired devices.

Proximity connection speeds up the headset connection process. It requires the headset to initiate a SLC connection to the nearest device first and combines this with the headset's storage of the last 8 paired/connected devices. Using proximity connection means functions operate equally well for the most or least recently paired or connected device.

## 15.2 8<sup>th</sup> Generation 2-mic cVc Audio Enhancements

#### Important Note:

It is important to follow the industrial design considerations in *cVc Two Microphone Headset Design Guidelines* when designing products using 2-mic cVc, even for non-headset products.

2-mic cVc headset full-duplex voice processing software is a fully integrated and highly optimised set of DSP algorithms developed to ensure easy design and build of echo and noise-cancelling products.

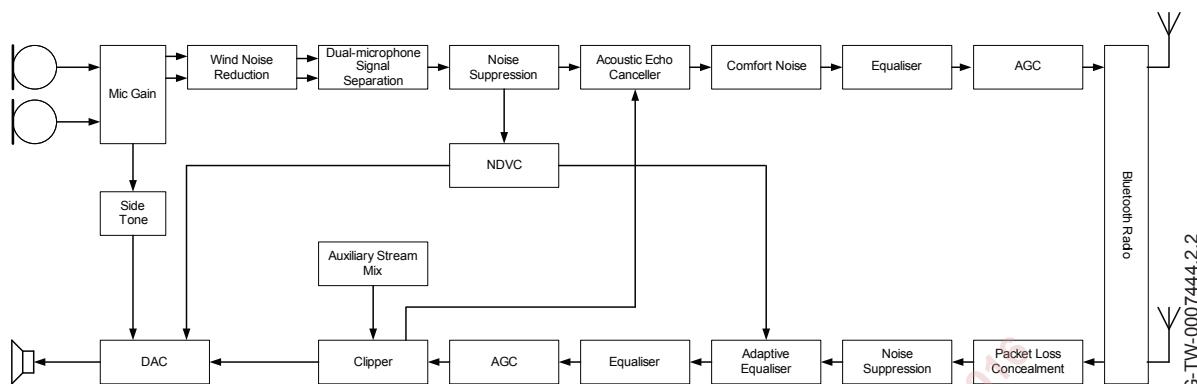
cVc headset enables greater acoustic design flexibility by incorporating software to compensate for cost-optimised microphone-to-speaker coupling and placement. cVc-enabled products operate in a wide variety of acoustic environments. Sophisticated noise suppression technology reduces the impact of noise in the transmission channel. Using intelligent volume control and intelligibility improvements, the receive channel is also enhanced based on the acoustic noise in the listener's environment.

The 8<sup>th</sup> generation cVc headset features include:

- Full-duplex AEC
- Bit error and packet loss concealment
- Transmit and receive noise suppression including WNR
- Transmit and receive AGC
- Noise dependent volume control
- Receive frequency enhanced speech intelligibility using adaptive equaliser
- Narrowband, wideband and frequency expansion operations

2-mic cVc headset includes a tuning tool that enables the developer to easily adapt cVc with different audio configurations and tuning parameters. The tool provides real-time system statistics with immediate feedback that enables designers to quickly investigate the effect of changes.

Figure 15.2 shows the functional block diagram of QTIL's proprietary 2-mic cVc headset DSP solution for a dual-microphone product.



**Figure 15.2: 2-mic cVc Block Diagram**

Section 15.2.1 to Section 15.2.13 describe the audio processing functions provided within cVc headset.

### 15.2.1 Acoustic Echo Cancellation

The AEC includes:

- A referenced sub-band adaptive linear filter that models the acoustic path from the receive reference point to the microphone input
- A non-linear processing function that applies narrowband and wideband attenuation adaptively as a result of residual echo present after the linear filter.

### 15.2.2 Noise Suppression with Wind Noise Reduction

The signal-channel noise suppression block is implemented in both signal paths. They are completely independent and individually tuned. Noise suppression is a sub-band stationary / quasi-stationary noise suppression algorithm that uses the temporal characteristics of speech and noise to remove the noise from the composite signal while maximising speech quality. The current implementation can improve the SNR by up to 20 dB.

In the transmit path, noise suppression aggressiveness is typically 95% improving SNR by 15 to 19 dB to compensate for the upstream processing and to maintain superior voice quality, while the Rx is typically tuned down to 80% improving SNR by 8 to 12 dB because of the cellular network processing. The user can parametrically adjust these default settings.

The noise suppression block contains a WNR feature (send path only). The WNR removes unwanted noise during a hands-free conversation, cleaning the audio for the far-end listener. It detects and tackle winds of various intensities and durations. Once the wind is detected, a good balance between voice quality and WNR is achieved.

### 15.2.3 Non-linear Processing

The non-linear processing module detects the presence of echo after the primary sub-band linear filter and adaptively applies attenuation at frequencies where echo is identified. It is used to minimise echo due to non-linearity caused by the system, for example, from the loudspeaker, microphone, amplifiers or electronics. QTIL recommends minimal use of non-linear processing due to the inherent distortion that it introduces.

### 15.2.4 Howling Control

The Howling Control is a programmable coupling threshold that when triggered applies attenuation to the send path. This control enables cVc to operate in car-to-car calls without experiencing echo events during very high volume situations.

### 15.2.5 Comfort Noise Generator

The CNG:

- Creates a spectrally and temporally consistent noise floor for the far-end listener.
- Adaptively inserts noise modelled from the noise present at the microphone into gaps introduced when the non-linear processing of the AEC applies attenuation. The noise level applied is user-controllable.
- Allows selectable coloured noise.

### 15.2.6 Equalisation

The equalisation filters:

- Are independent in the send and receive signal channels
- Are independently enabled
- Are configurable to achieve the required frequency response
- Each channel comprises of 5 stages of cascaded 2<sup>nd</sup> order IIR filters
- Compensate for the frequency response of transducers in the system, i.e. the microphone and loud speaker

### 15.2.7 Automatic Gain Control

The AGC block attempts to:

- Normalise the amplitude of the incoming audio signal to a desired range to increase perceived loudness
- Reduce distortion due to clipping
- Reduce amplitude variance observed from different users, phones and networks

Maintaining a consistent long-term loudness for the speech ensures it is more easily heard by the listener and it also provides the subsequent processing block a larger amplitude signal to process. The behaviour of the AGC differs from a dynamic range audio compressor. The convergence time for the AGC is much slower to reduce the non-linear distortion.

### 15.2.8 Packet Loss Concealment

Bit errors and packet loss can occur in the Bluetooth transmission due to a variety of reasons, e.g. Wi-Fi interference or RF signal degradation due to distance or physical objects. As a result of these errors, the user hears glitches referred to as *pops* and *clicks* in the audio stream. The PLC block improves the receive path audio quality in the presence of bit and packet errors within the Bluetooth link by using a variety of techniques such as pitch-based waveform substitution.

The PLC tries to re-synthesise the lost packet from the history buffer with the same pitch period. The PLC uses a highly efficient 3-phase pitch estimator and performs cross-fading at the concatenation boundaries, i.e. the PLC attempts to clean up the audio signal by removing the *pops* and *clicks* and smoothing out gaps. This improves the audio quality for the user and the improved signal enables proceeding processing blocks to perform better.

The PLC significantly improves dealing with bit errors, using the BFI output from the firmware. The DSP calculates an average BER and selectively applies the PLC to the incoming data. This optimises audio quality for a variety of bit errors and packet loss conditions. The PLC is enabled in all modes.

**Note:**

The PLC is enabled in all modes, HFK (full processing), pass-through and loopback by default.

### 15.2.9 Adaptive Equalisation

The adaptive equalisation block improves the intelligibility of the receive path voice signal in the presence of near end noise by altering the spectral shape of the receive path signal while maintaining the overall power level. It has been empirically observed that consonants, which are dominantly high-frequency based and much lower in amplitude than vowels, significantly contribute to the intelligibility of the voice signal. In the presence of noise, the lower amplitude consonants are masked by this noise. Therefore, by increasing the frequency of components that contribute to the consonants while in the presence of noise, the intelligibility can be improved. To maintain a consistent amplitude level, the adaptive equalisation block adaptively increases the high frequencies relative to the middle frequencies and also reduces the low frequencies accordingly. The adaptive equaliser also has the capability to compensate for variations in voice transmission channels, which include far-end devices and telecommunication channels.

The Frequency Emphasis feature can be used with any standard narrow band call, when the DAC is operating at a sample rate of 8 kHz. To complement the AEQ, High Frequency Emphasis can be added to improve the intelligibility of the far-end caller. The emphasis feature repairs frequencies (3469 Hz to 4000 Hz) that were lost due to the filters of the cellular network and Bluetooth link. Information contained in the original speech from 281 Hz to 3469 Hz is used to reconstruct the lost high frequency content.

The Frequency Expansion feature can be used with any standard narrow band call, but a special mode is invoked when the DAC operates at a sample rate of 16 kHz. The frequency expansion allows users to add in frequencies far beyond the band limits caused by the cellular network and Bluetooth link. These expansion frequencies are added between 3469 Hz and 6156 Hz. As in frequency emphasis, it uses the information contained in the original speech from 281 Hz to 3469 Hz to reconstruct the lost high frequency content.

### 15.2.10 Auxiliary Stream Mix

The auxiliary stream mixer enables the system to seamlessly mix audio signals such as tones, beeps and voice prompts with the incoming SCO stream. This avoids any interruption to the SCO stream and as a result prevents any speech from being lost.

### 15.2.11 Clipper

The clipper block intentionally distorts or *clips* the receive signal prior to the reference input of the AEC to more accurately model the behaviour of the post reference input blocks such as the DAC, power amplifier and the loudspeaker. The AEC attempts to correlate the signal received at the reference input and the microphone input. Any non-linearities introduced that are not accounted for after the reference input significantly degrade the AEC performance. This processing block can significantly improve the echo performance in cheap non-linear system designs.

### 15.2.12 Noise Dependent Volume Control

The NDVC block improves the intelligibility of the receive path signal by increasing the analogue DAC gain value based on the send noise estimate from the send path noise suppression block. As the send noise estimate increases, the NDVC algorithm increases the analogue DAC gain value. The NDVC uses hysteresis to minimise the artefacts generated by rapidly adjusting the DAC gain due to the fluctuation in the environmental noise.

### 15.2.13 Input Output Gains

Fixed gain controls are provided at the input to the cVc system. The mic gain is used set the ADC level so that proper levels can be set according to hardware constraints, industry standards and the digital resolution of the DSP fixed point processor. The speaker gain represents the output DAC which drive the speaker. The DAC level varies under software control for events such as the Bluetooth volume, NDVC, tone mixing and other volume based activities.

## 15.3 Music Enhancements

### 15.3.1 Audio Decoders

CSRA63120 A11 QFN supports:

- SBC
- AAC
- Jitter handling and high quality sample rate matching
- Low power consumption

### 15.3.2 Configurable EQ

CSRA63120 A11 QFN has 2 forms of EQ:

- User configurable EQ: Made up of up to 6 banks of 5 stages. Contains tiering for multiple customer presets, e.g. user, rock, pop, classical, jazz, etc. This enables the device user to select between the EQ bank presets through button presses.
- Manufacturer configurable speaker EQ: Made up of 1 bank of 0 to 10 stages. Contains an easy to use GUI, with drag points, see Figure 15.3.

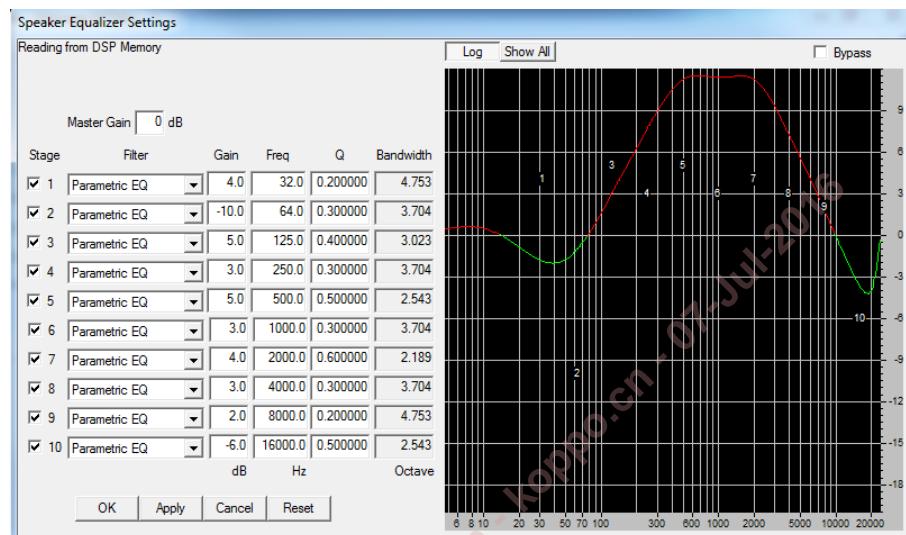


Figure 15.3: Configurable EQ GUI with Drag Points

### 15.3.3 Stereo Widening (S3D)

The stereo widening feature on CSRA63120 A11 QFN:

- Simulates loudspeaker listening to provide 3D listening experience
- Is highly optimised at <1 MIPS of the Kalimba DSP
- Reduces listener fatigue for headphone listening

### 15.3.4 Volume Boost

The volume boost feature on the CSRA63120 A11 QFN is a dynamic range compander and provides:

- Additional loudness without clipping
- Multi-stage compression and expansion
- Processing modules for dynamic bass boost
- Includes new optional volume control hard limiter
- Louder audio output without distortion
- Easy to use GUI, with drag points, see Figure 15.4

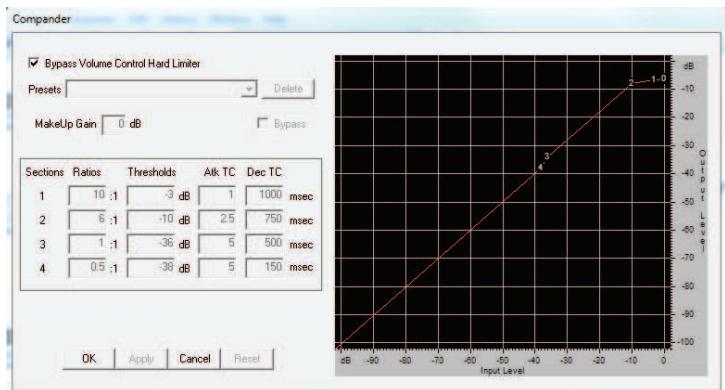


Figure 15.4: Volume Boost GUI with Drag Points

## 15.4 CSRA63120 Mono ROM Solution Development Kit

QTIL's audio development kit for the CSRA63120 A11 QFN, order code DK-CSRA63120-10273-1A, includes a CSRA63120 mono ROM solution demonstrator board and necessary interface adapters and cables are available. In conjunction with the CSRA63xxx ROM Series Configuration Tool and other supporting utilities the development kit provides the best environment for designing audio solutions with the CSRA63120 A11 QFN.

### Important Note:

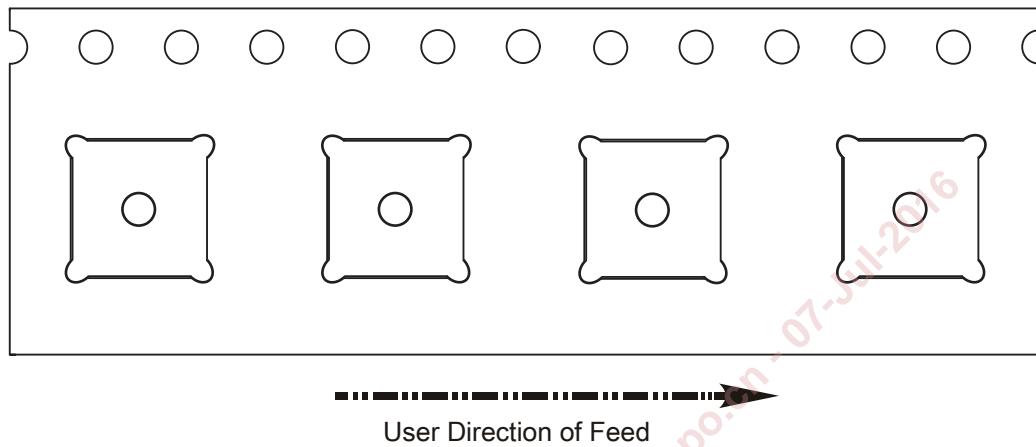
The CSRA63120 Mono ROM Solution audio development kit is subject to change and updates, for up-to-date information see [www.csrsupport.com](http://www.csrsupport.com).

## 16 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

### 16.1 Tape Orientation

Figure 16.1 shows the CSRA63120 A11 QFN packing tape orientation.



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Figure 16.1: CSRA63120 A11 QFN Tape Orientation

## 16.2 Tape Dimensions

Figure 16.2 shows the CSRA63120 A11 QFN tape dimensions.

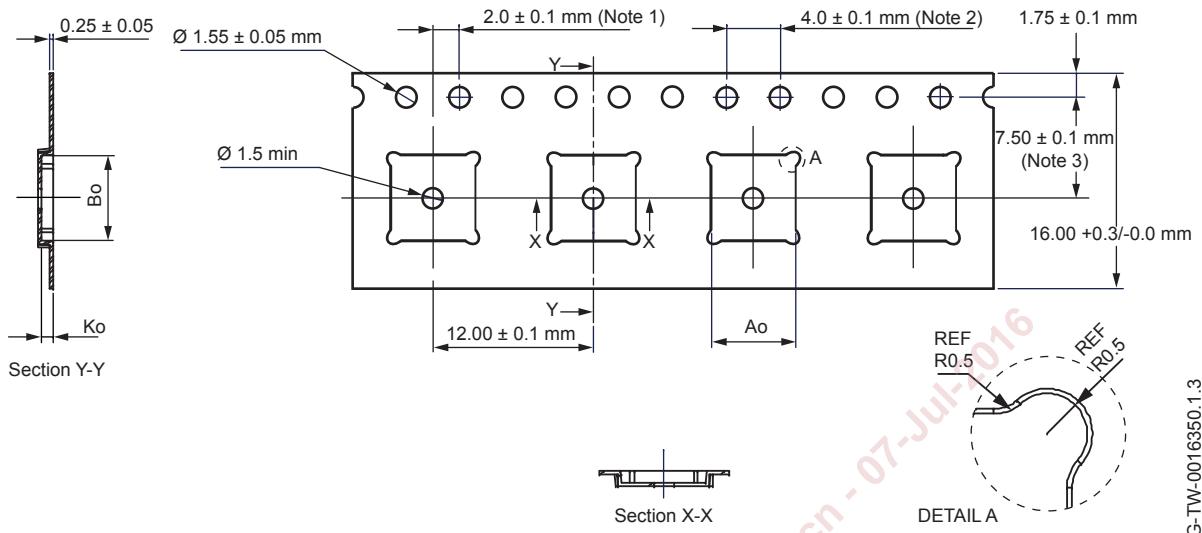


Figure 16.2: Tape Dimensions

$A_0$	$B_0$	$K_0$	Unit	Notes
6.30	6.30	0.90	mm	<ol style="list-style-type: none"> <li>Measured from centreline of sprocket hole to centreline of pocket.</li> <li>Cumulative tolerance of 10 sprocket holes is <math>\pm 0.2</math>.</li> <li>Measured from centreline of sprocket hole to centreline of pocket.</li> <li>Other material available.</li> </ol>

## 16.3 Reel Information

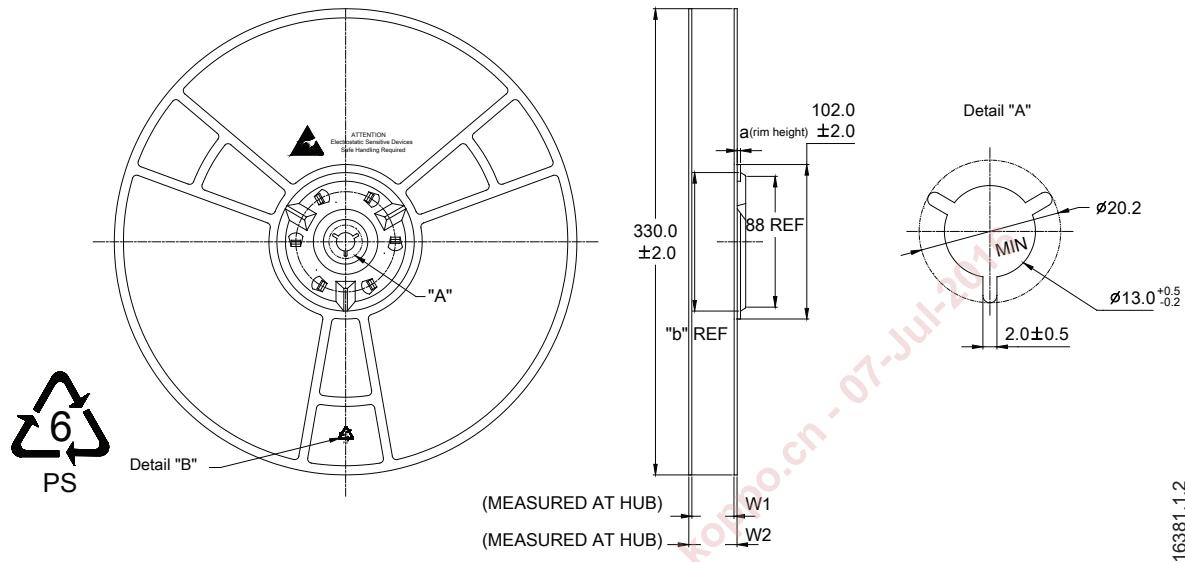


Figure 16.3: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
6 x 6 x 0.6 mm QFN	16	4.5	98.0	16.8 (+1.6/-0.4)	22.4	mm

## 16.4 Moisture Sensitivity Level

CSRA63120 A11 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

## 17 Document References

Document	Reference, Date
<i>BlueCore Audio API Specification</i>	CS-209064-SP
<i>BlueTest User Guide</i>	CS-102736-UG
<i>Bluetooth and USB Design Considerations</i>	CS-101412-AN
<i>Core Specification of the Bluetooth System</i>	Bluetooth Specification Version 4.2, 02 December 2014
<i>CSRA63210 A11 QFN Performance Specification</i>	CS-339621-SP
<i>CSRA63xxx/CSRA64xxx A11 Firmware Release Note</i>	CS-329926-RN
<i>cVc Two Microphone Headset Design Guidelines</i>	CS-218321-DC
<i>ESDA/JEDEC Joint Standard For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level</i>	ANSI/ESDA/JEDEC JS-001-201
<i>Field-Induced Charged-Device Model Test Method for Electrostatic- Discharge-Withstand Thresholds of Microelectronic Components</i>	JESD22-C101E
<i>IC Packing and Labelling Specification</i>	CS-112584-SP
<i>IEC 61000-4-2 Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test</i>	IEC 61000-4-2, Edition 2.0, 2008-12
<i>Kalimba Architecture 3 DSP User Guide</i>	CS-202067-UG
<i>Lithium Polymer Battery Charger Calibration and Operation for CSR8670</i>	CS-204572-AN
<i>Moisture / Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices</i>	IPC / JEDEC J-STD-020
<i>Optimising BlueCore5-Multimedia ADC Performance Application Note</i>	CS-120059-AN
<i>Typical Solder Reflow Profile for Lead-free Device</i>	CS-116434-AN
<i>Universal Serial Bus Specification</i>	v2.0, 27 April 2000
<i>USB Battery Charging Specification</i>	v1.2 December 7 <sup>th</sup> 2010, also errata and ECNs through March 15 <sup>th</sup> 2012

## Terms and Definitions

Term	Definition
3G	3 <sup>rd</sup> Generation of mobile communications technology
8DPSK	8-phase Differential Phase Shift Keying
$\pi/4$ DQPSK	$\pi/4$ rotated Differential Quaternary Phase Shift Keying
A2DP	Advanced Audio Distribution Profile
AAC	Advanced Audio Coding
AC	Alternating Current
ADC	Analogue to Digital Converter
AEC	Acoustic Echo Cancellation
AEQ	Adaptive Equaliser
AG	Audio Gateway
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ALU	Arithmetic Logic Unit
AUX	Auxiliary
AVRCP	Audio/Video Remote Control Profile
BEC	Bit Error Concealment
BER	Bit Error Rate
BFI	Bad Frame Indicator
BlueCore™	Group term for QTIL's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
CNG	Comfort Noise Generation
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear To Send
cVc	Clear Voice Capture
DAC	Digital to Analogue Converter
DC	Direct Current
DI	Device Id profile
DMA	Direct Memory Access
DNL	Differential Non Linearity (ADC accuracy parameter)

Term	Definition
DSP	Digital Signal Processor (or Processing)
DUT	Device Under Test
e.g.	<i>exempli gratia</i> , for example
EIA	Electronic Industries Alliance
EMC	ElectroMagnetic Compatibility
EQ	EQualiser
eSCO	extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
etc	<i>et cetera</i> , and the rest, and so forth
FIR	Finite Impulse Response (filter)
FSK	Frequency Shift Keying
G.722	An ITU-T standard wideband speech codec operating at 48, 56 and 64 kbps
GSM	Global System for Mobile communications
GUI	Graphical User Interface
HBM	Human Body Model
HCI	Host Controller Interface
HFP	Hands-Free Profile
HSP	HeadSet Profile
I <sup>2</sup> C	Inter-Integrated Circuit Interface
i.e.	<i>Id est</i> , that is
I/O	Input/Output
IC	Integrated Circuit
IEEE	Institute of Electronic and Electrical Engineers
IF	Intermediate Frequency
IIR	Infinite Impulse Response (filter)
INL	Integral Non-Linearity (ADC accuracy parameter)
IPC	See <a href="http://www.ipc.org">www.ipc.org</a>
IPM	Intelligent Power Management
IQ	In-Phase and Quadrature
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression and file compression / decompression
LC	An inductor (L) and capacitor (C) network

Term	Definition
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LNA	Low Noise Amplifier
LSB	Least Significant Bit (or Byte)
MAC	Multiplier and ACcumulator
Mb	Megabit
MCU	MicroController Unit
MISO	Master In Slave Out
MLC	MultiLayer Ceramic
MMU	Memory Management Unit
mSBC	modified Sub-Band Coding
N/A	Not Applicable
NDVC	Noise Dependent Volume Control
NSMD	Non-Solder Mask Defined
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIN	Personal Identification Number
PIO	Programmable Input/Output, also known as general purpose I/O
PLC	Packet Loss Concealment
plc	public limited company
PM	Physical Memory
ppm	parts per million
PS Key	Persistent Store Key
PWM	Pulse Width Modulation
QFN	Quad-Flat No-lead
QTIL	Qualcomm Technologies International, Ltd.
RAM	Random Access Memory
RF	Radio Frequency
RGB	Red Green Blue
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)

Term	Definition
ROM	Read Only Memory
RS-232	Recommended Standard-232, a TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.)
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SBC	Sub-Band Coding
SCL	Serial Clock Line
SCMS	Serial Copy Management System (SCMS-T). A content protection scheme for secure transport and use of compressed digital music
SCO	Synchronous Connection-Oriented
SDA	Serial DAta (line)
SIG	(Bluetooth) Special Interest Group
SLC	Service Level Connection
SMPS	Switch-Mode Power Supply
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SQIF	Serial Quad I/O Flash (interface)
THD+N	Total Harmonic Distortion and Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VoIP	Voice over Internet Protocol
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi®	Wireless Fidelity (IEEE 802.11 wireless networking)
WNR	Wind Noise Reduction
XTAL	Crystal