ESP8266 Phy Init Bin

Parameter Configuration Guide

Version 1.0
Espressif Systems
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About This Guide

This guide provides the parameter configuration for *ESP8266 phy init bin*.

Release Notes

Date	Version	Release notes
2018.12	V1.0	Initial release

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1.   Structure of *ESP8266 Phy Init Bin*

ESP8266 phy init bin is comprised of a 128-byte *phy init data* as shown in Table 1-1:

Table 1-1. Structure of ESP8266 Phy Init Bin

Name	Size
phy init data	128 bytes

2. Check Bits for *ESP8266 Phy Init Bin*

The check bits for **ESP8266 phy init bin** are stored in byte zero of **phy init data**, and the relevant parameter is **Init_bin_magic** with default value of 0x5. The check bits are used for verifying the data location in **ESP8266 phy init bin**. If the parameter value is the same as the default value when reading data, it is assumed that data are stored correctly in **ESP8266 phy init bin**.

Table 2-1. Check Bits for ESP8266 Phy Init Bin

Location in *phy init data*	Parameter Name	Default Value	Description
0	*Init_bin_magic*	5	For check

3. Version of *ESP8266 Phy Init Bin*

The version information of **ESP8266 phy init bin** is stored in byte 1 of **phy init data**.

For example, **ESP8266_esp_data_bin_v08.bin** represents Version 08, which is stored in byte 1 as 0x8.

Table 3-1. Version of ESP8266 Phy Init Bin

Location in *phy init data*	Parameter Name	Default Value	Description
1	*Init_bin_version*	8	*phy init bin* version

4.   Selection of Crystal Oscillator

The parameter *crystal_sel* allows you to select a crystal oscillator. The available options are given in Table 4-1. Currently, ESP8266 mainly supports 26 MHz and 40 MHz crystal oscillators.

Table 4-1. Selection of Crystal Oscillator

Location in *phy init data*	Parameter Name	Default Value	Description
48	*crystal_sel*	1	0: 40 MHz crystal oscillator 1: 26 MHz crystal oscillator 2: 24 MHz crystal oscillator

5.   Six Levels of TX Power

TX power can be switched between six levels. The indexes for the six levels are the numbers from 0 to 5 at the end of the parameter names. For example, the index for *txpwr_qdb_0* is 0, representing the maximum TX power. From *txpwr_qdb_0* to *txpwr_qdb_5,* the TX power decreases progressively.

Default *TX power* settings can be found in Table 5-1.

Table 5-1. Six Levels of TX Power

Location in *phy init data*	Parameter Name	Default Value	Unit	Actual TX Power
34	*txpwr_qdb_0*	78	0.25 dB	19.5 dBm
35	*txpwr_qdb_1*	74	0.25 dB	18.5 dBm
36	*txpwr_qdb_2*	70	0.25 dB	17.5 dBm
37	*txpwr_qdb_3*	64	0.25 dB	16 dBm
38	*txpwr_qdb_4*	60	0.25 dB	15 dBm
39	*txpwr_qdb_5*	56	0.25 dB	14 dBm

6.   TX Power for Various Data Rates

You can choose from any of the six TX power levels for different data rates. The column *Default value* in Table 6-1 contains the TX power index.

Table 6-1. TX Power for Various Date Rates

Location in *phy init data*	Parameter Name	Data rate/mode	Default Value	Description
40	*txpwr_index_0*	MCS0, 1 Mbit/s, 2 Mbit/s, 5.5 Mbit/s, 11 Mbit/s, 6 Mbit/s, 9 Mbit/s	0	Select *txpwr_qdb_0*
41	*txpwr_index_1*	MCS1, 12 Mbit/s	0	Select *txpwr_qdb_0*
42	*txpwr_index_2*	MCS2, 18 Mbit/s	1	Select *txpwr_qdb_1*
43	*txpwr_index_3*	MCS3, 24 Mbit/s	1	Select *txpwr_qdb_1*
44	*txpwr_index_4*	MCS4, 36 Mbit/s	2	Select *txpwr_qdb_2*
45	*txpwr_index_5*	MCS5, 48 Mbit/s	3	Select *txpwr_qdb_3*
46	*txpwr_index_6*	MCS6, 54 Mbit/s	4	Select *txpwr_qdb_4*
47	*txpwr_index_7*	MCS7	5	Select *txpwr_qdb_5*
96	*txpwr_index_11b _en*	802.11b	0	0: use *txpwr_index_0* to set TX Power for 802.11b 1: use bytes 97 and 98 to set TX Power for 802.11b
97	*txpwr_index_11b _0*	1 Mbit/s, 2 Mbit/s	0	Select *txpwr_qdb_0*
98	*txpwr_index_11b _1*	5.5 Mbit/s, 11 Mbit/s	0	Select *txpwr_qdb_0*

7. TX Power Limits

The TX power limits have been set mainly to limit the maximum powers for channels 1, 11, 13 and 14 in order to conform to the certification test results.

7.1. Value Range of the TX Power Limits

The TX power limits are set against the six levels. The value range of the limits is [0:5], which includes the values presented in Table 7-1.

Table 7-1. Values of the TX Power Limits

Value	TX Power Limit (Unit: 0.25 dB)
0	*txpwr_qdb_0*
1	*txpwr_qdb_1*
2	*txpwr_qdb_2*
3	*txpwr_qdb_3*
4	*txpwr_qdb_4*
5	*txpwr_qdb_5*

7.2. Parameters for the TX Power Limits

The parameters for the TX power limits are specified in Table 7-2. For example, if the value of byte 78 is set to 2, the bytes 30-33 are enabled to configure the maximum TX powers for channels 1, 11, 13 and 14.

Table 7-2. Parameters for the TX Power Limits

Location in *phy init data*	Parameter name	Default value	Description
78	*fcc_enable*	0	0: disable bytes 30-33 1: reserved 2: enable bytes 30-33 to set maximum TX power
30	*mpwr_chan1*	0	Set the maximum TX power for 802.11 b/g/n mode at channel 1, range [0:5]. 0xf8 is an invalid parameter.
31	*mpwr_chan11*	0	Set the maximum TX power for 802.11 b/g/n mode at channel 11, range [0:5]. 0xf8 is an invalid parameter.

| 32 | *mpwr_chan13* | 0 | Set the maximum TX power for 802.11 b/g/n mode at channel 13, range [0:5]. 0xf8 is an invalid parameter. |
| 33 | *mpwr_chan14* | 0 | Set the maximum TX power for 802.11 b/g/n mode at channel 14, range [0:5]. 0xf8 is an invalid parameter. |

8. RF Calibration

The values of the parameter **RF_calibration** are shown in Table 8-1. To ensure better RF performance, it is recommend to set **RF_calibration** to 3, otherwise the RF performance may become poor.

Table 8-1. Parameter of RF Calibration

Location in *phy init data*	Parameter name	Default value	Description
114	*RF_calibration*	3	0 & 1: only used for setting TX power 2: No RF calibration 3: Conduct all RF calibration

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