Li+ Charger Protection IC

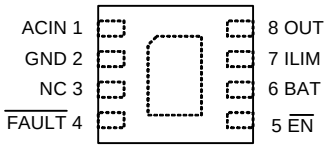
Features

- **Provide Input Over-Voltage Protection**
- **Programmable Input Over-Current Protection**
- **Battery Over-Voltage 4.35V Protection**
- **Over-Temperature Protection**
- **High Immunity of False Triggering**
- **High Accuracy Protection Thresholds**
- **Fault Status Indication**
- **Enable Input**
- **Available in TDFN2x2-8 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Smart Phones and PDAs**
- **Digital Still Cameras**
- **Portable Devices**

Pin Configuration



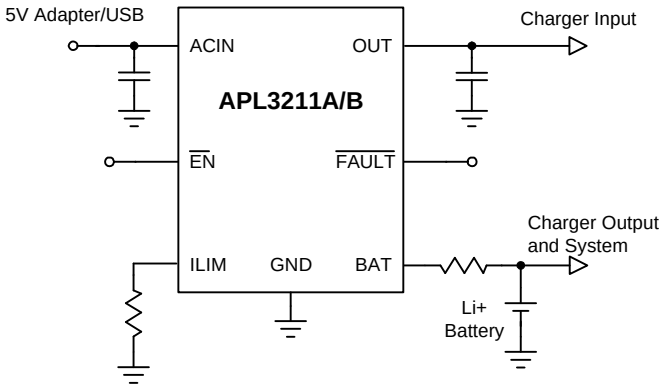
TDFN2x2-8 (Top View)

= Exposed Pad (connected to ground plane for better heat dissipation)

General Description

The APL3211A/B provide complete Li+ charger protections against over-voltage, over-current, and battery over-voltage. The IC is designed to monitor input voltage, input current, and battery voltage. When any of the monitored parameters are over the threshold, the IC removes the power from the charging system by turning off an internal switch. All protections also have deglitch time against false triggering due to voltage spikes or current transients. The APL3211A/B also provide over-temperature protection, a $\overline{\text{FAULT}}$ output pin to indicate the fault conditions, and the $\overline{\text{EN}}$ pin to allow the system to disable the IC.

Simplified Application Circuit



Ordering and Marking Information

APL3211A/B □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN2x2-8 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APL3211A QB: L11A X	X - Date Code
APL3211B QB: L11B X	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{ACIN}	IN Input Voltage (ACIN in to GND)	-0.3 to 30	V
V_{OUT}, V_{BAT}	OUT, BAT Pins to GND Voltage	-0.3 to 7	V
V_{LIM}, $V_{\overline{FAULT}}$, $V_{\overline{EN}}$,	ILIM, $\overline{FAULT}$, $\overline{EN}$ to GND Voltage	-0.3 to 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature,10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction to Ambient Thermal Resistance in Free Air (Note 2) TDFN2x2-8	75	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{ACIN}	ACIN Input Voltage	4.5 to 5.5	V
I_{OUT}	OUT Output Current	0 to 2	A
T_J	Junction Temperature	-40 to 125	°C
T_A	Ambient Temperature	-40 to 85	°C

Note 2 : Refer th the typical application circuit.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, T_A= -40~85°C, unless otherwise specified. Typical values are at T_J=25°C.

Symbol	Parameter	Test Conditions	APL3211A/B			Unit
			Min.	Typ.	Max.	
ACIN INPUT CURRENT AND POWER-ON-RESET(POR)						
I_{ACIN}	ACIN Supply Current	$\overline{EN}$ = Low	-	250	350	µA
		$\overline{EN}$ = High	-	100	150	
V_{ACIN}	ACIN POR Threshold	V_{IN} rising	2.4	2.6	2.8	V
	ACIN POR Hysteresis		200	250	300	
$T_{B(ACIN)}$	ACIN Power-On Blanking Time	V_{IN} rising to V_{OUT} rising	-	8	-	ms
INTERNAL SWITCH ON RESISTANCE						
R_{ON}	Power Switch On Resistance	I_{OUT} = 0.8A	-	130	-	mΩ
	OUT Discharge Resistance	V_{OUT} = 3V	-	500	-	Ω
INPUT OVER-VOLTAGE PROTECTION (OVP)						
V_{OVP}	Input OVP Threshold	APL3211A, T_J=-40~125°C	5.7	5.85	6.0	V
		APL3211B, T_J=-40~125°C	6.6	6.8	7.0	
	Input OVP Hysteresis		-	250	-	mV
	Input OVP Propagation Delay	VACIN=5 to 12V, I_{UT}=10mA	-	1	-	µs
$T_{ON(OVP)}$	Input OVP Recovery Time		-	8	-	ms
OVER-CURRENT PROTECTION (OCP)						
I_{OCP}	OCP Threshold	R_{OCSET}=25kΩ, T_J=25°C	900	1000	1100	mA
	OCP Accuracy	I_{OCP}=800mA~2500mA(or 1A~1.5A), T_J=25°C	-10	-	+10	%
$I_{OCP(MAX)}$	Maximum OCP Threshold	R_{OCSET}=0Ω, T_J=25°C	-	3	-	A
$T_{B(OCP)}$	OCP Blanking Time		-	176	-	µs
$T_{ON(OCP)}$	OCP Recovery Time		-	64	-	ms

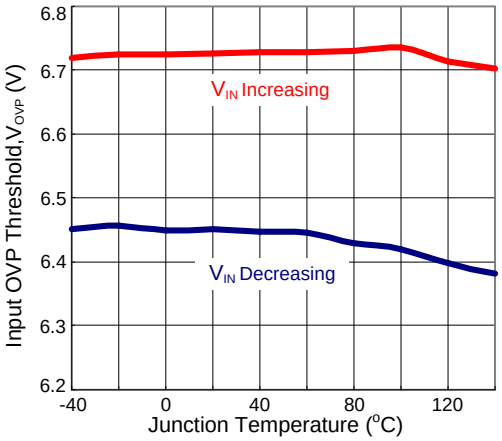
Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{IN}=5V, T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

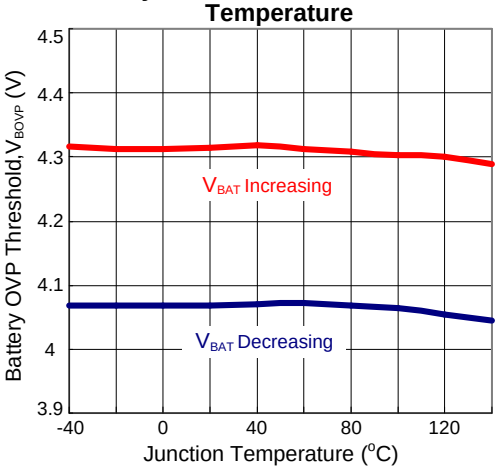
Symbol	Parameter	Test Conditions	APL3211A/B			Unit
			Min.	Typ.	Max.	
BATTERY OVER-VOLTAGE PROTECTION						
V_{BOVP}	Battery OVP Threshold	T_J = -40 ~ 125°C	4.30	4.35	4.40	V
	Battery OVP Hysteresis		200	250	300	mV
I_{BAT}	BAT Pin Leakage Current	V_{BAT} = 4.4V	-	-	20	nA
$T_{B(BOVP)}$	Battery OVP Blanking Time		-	176	-	µs
$\overline{EN}$ LOGIC LEVELS						
$V_{\overline{EN}}$	$\overline{EN}$ Input Logic High		1.4	-	-	V
	$\overline{EN}$ Input Logic Low		-	-	0.4	V
	$\overline{EN}$ Internal Pull-Low Resistor		-	500	-	kΩ
$\overline{FAULT}$ LOGIC LEVELS AND DELAY TIME						
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Output Low Voltage	Sink 5mA current	-	-	0.4	V
	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 5V	-	-	1	µA
Thermal Shutdown Protection						
T_{OTP}	Thermal Shutdown Threshold		-	140	-	°C
	Thermal Shutdown Hysteresis		-	20	-	°C

Typical Operating Characteristics

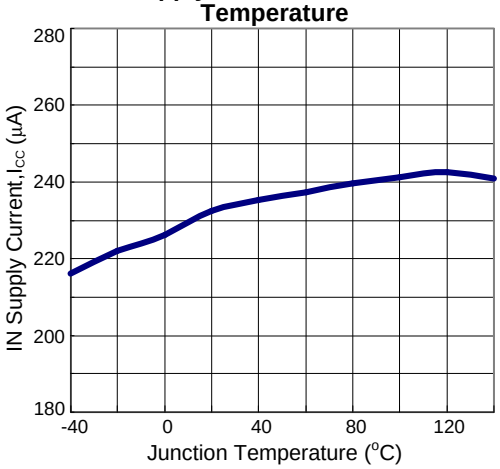
Input OVP Threshold vs. Junction Temperature



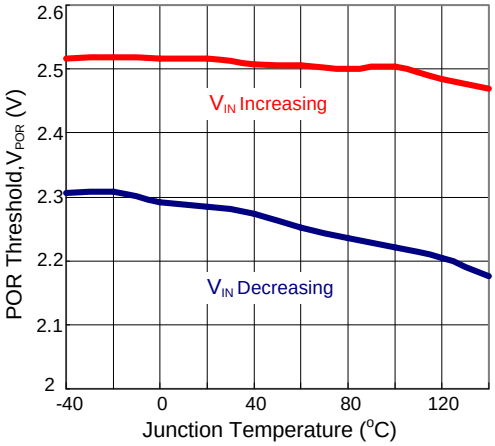
Battery OVP Threshold vs. Junction Temperature



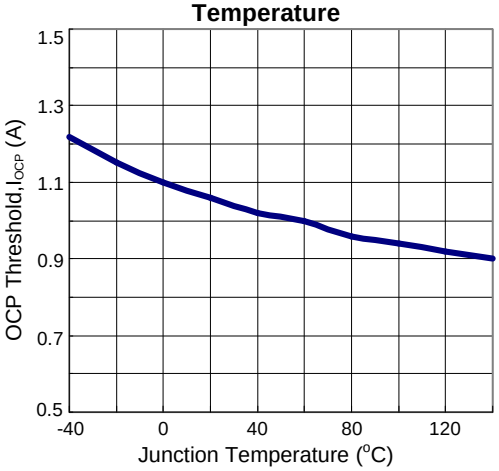
IN Supply Current vs. Junction Temperature



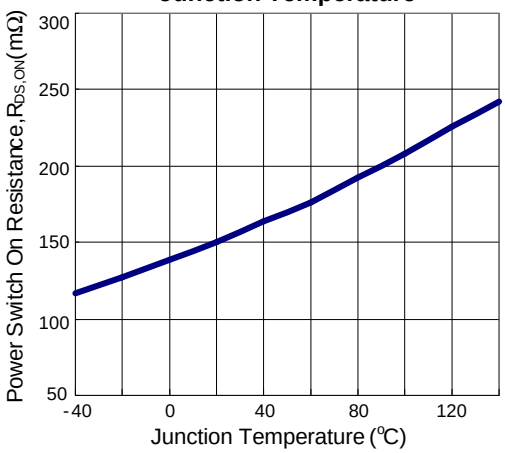
POR Threshold vs. Junction Temperature



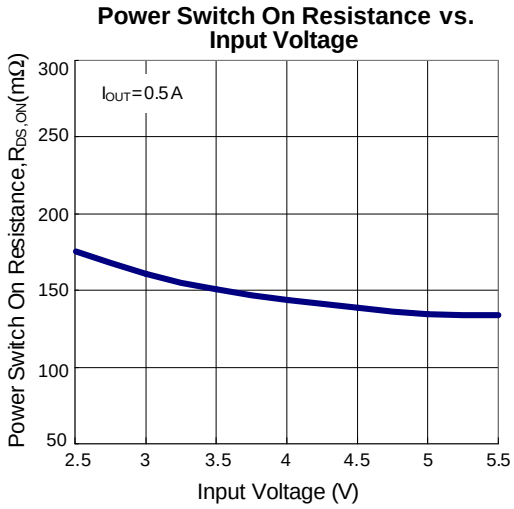
OCP Threshold vs. Junction Temperature



Power Switch On Resistance vs. Junction Temperature

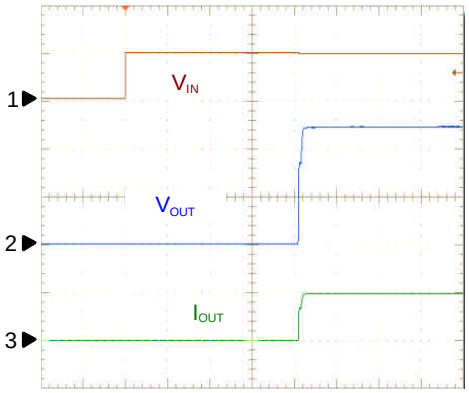


Typical Operating Characteristics



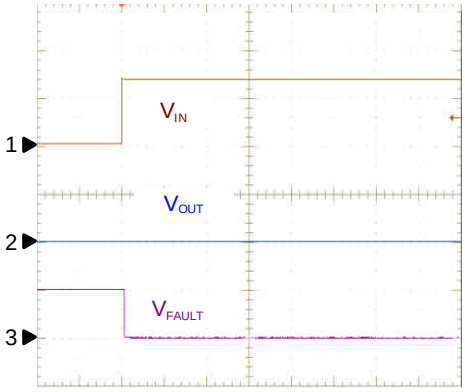
Operating Waveforms

Normal Power On



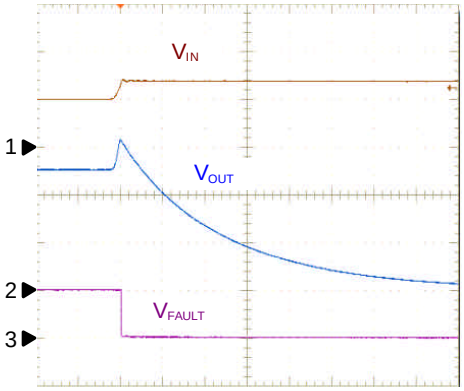
V_{IN}=0 to 5V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=10Ω
CH1:V_{IN},5V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:I_{OUT},0.5A/Div, DC
TIME:2ms/Div

OVP at Power On



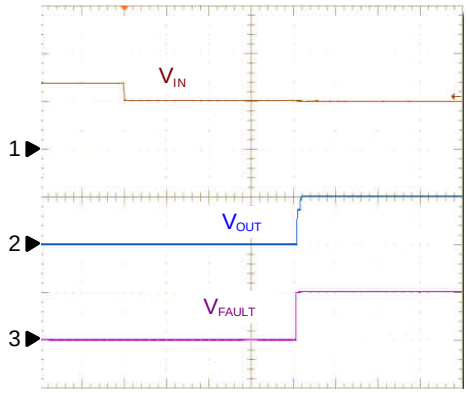
V_{IN}=0 to 7V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=10Ω
CH1:V_{IN},5V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:2ms/Div

Input Over-Voltage Protection



V_{IN}=5 to 7V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=50Ω
CH1:V_{IN},5V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:20µs/Div

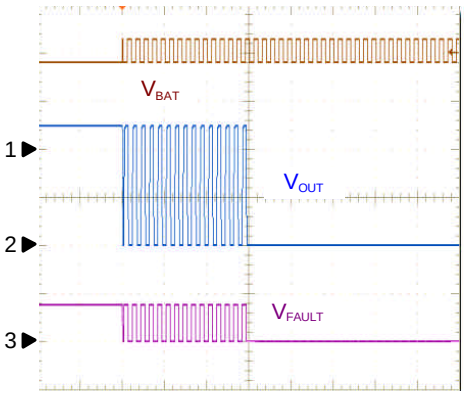
Recovery from Input OVP



V_{IN}=7V to 5V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=50Ω
CH1:V_{IN},5V/Div, DC
CH2:V_{OUT},5V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:2ms/Div

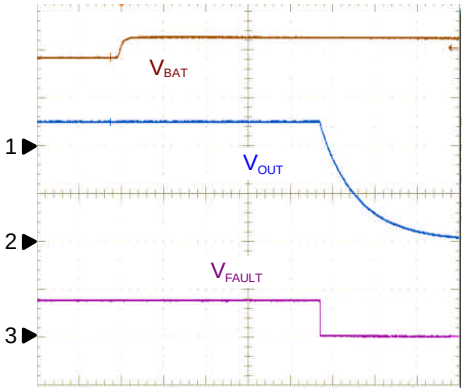
Operating Waveforms

Battery Over-Voltage Protection



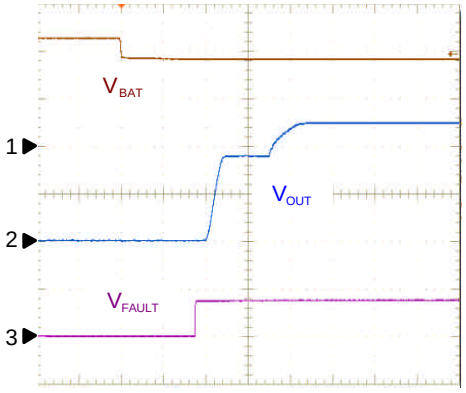
V_{BAT}=3.6V to 4.4V to 3.6V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=33Ω
CH1:V_{BAT},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:10ms/Div

Battery Over-Voltage Protection



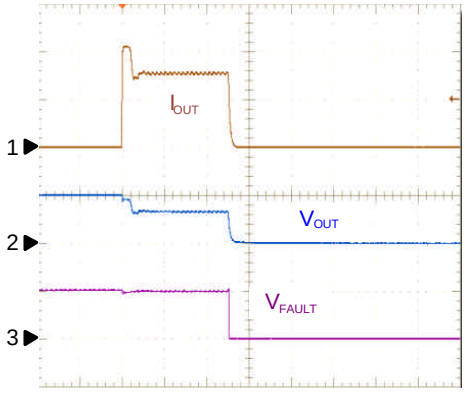
V_{BAT}=3.6V to 4.4V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=33Ω
CH1:V_{BAT},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:40µs/Div

Recovery from Battery OVP



V_{BAT}=4.4V to 3.6V
C_{OUT}=1µF,C_{IN}=1µF,R_{OUT}=33Ω
CH1:V_{BAT},2V/Div, DC
CH2:V_{OUT},2V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:100µs/Div

Over-Current Protection

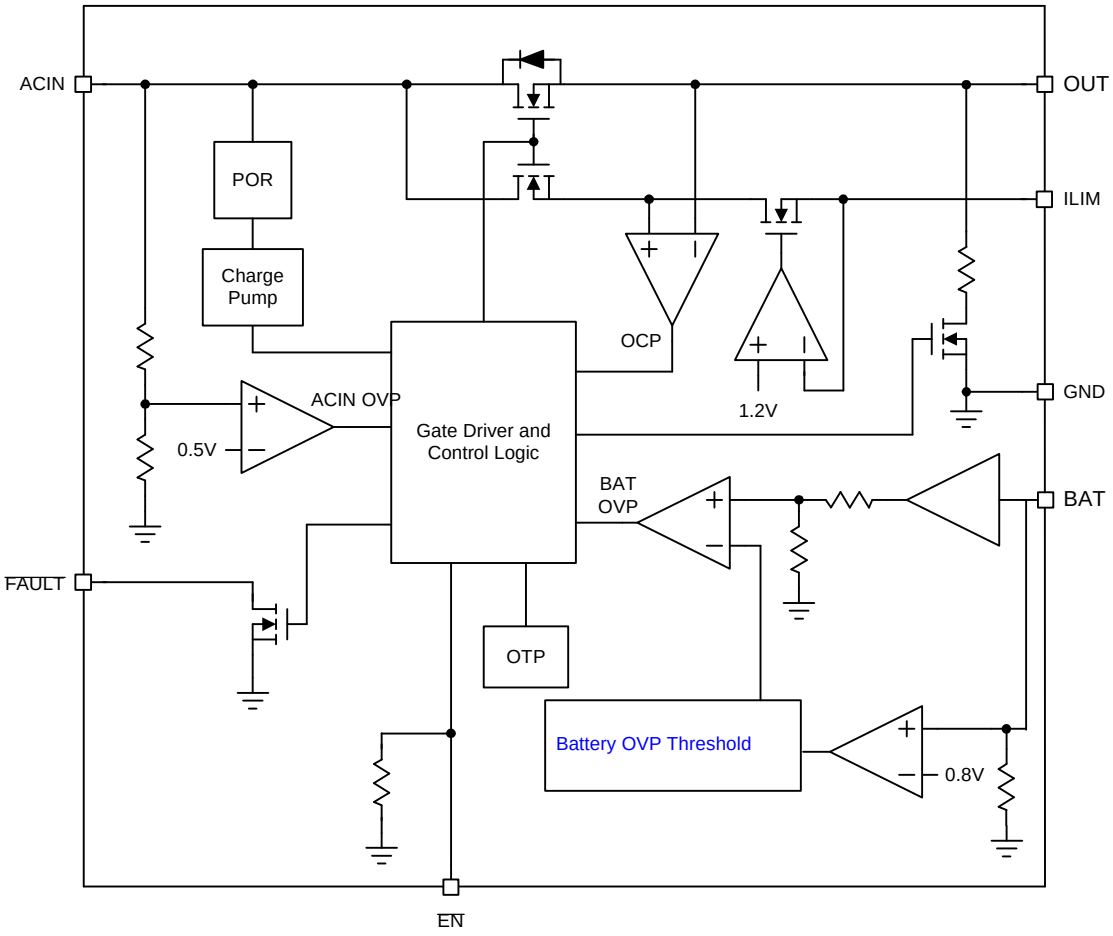


C_{OUT}=1µF,C_{IN}=1µF
CH1:I_{OUT},0.5A/Div, DC
CH2:V_{OUT},5V/Div, DC
CH3:V_{FAULT},5V/Div, DC
TIME:100µs/Div

Pin Description

PIN		FUNCTION
NO.	NAME	
1	ACIN	Power Supply Input, connect to external DC supply. Connect external 1μF ceramic capacitor (minimum) to GND.
2	GND	Ground pin of the circuitry. All voltage levels are measured with respect to this pin.
3	NC	Not connected
4	$\overline{\text{FAULT}}$	Fault Indication Pin. This pin goes low when input OVP, OCP or battery OVP is detected.
5	$\overline{\text{EN}}$	Enable Input. Pull this pin to high to disable the device and pull this pin to low to enable device.
6	BAT	Battery OVP Sense Pin. Connect to positive terminal of battery through a resistor.
7	ILIM	Over-current Protection Setting Pin. Connect a resistor (R_{OCSET}) to GND to set the over-current threshold. When left open, the internal power FET will be turned off.
8	OUT	Output Pins. Output Voltage Pin. The output voltage follows the input voltage when no fault is detected
Exposed Pad	-	Exposed Thermal Pad. Connect this pad to system ground plane for good thermal conductivity.

Block Diagram



Typical Application Circuit

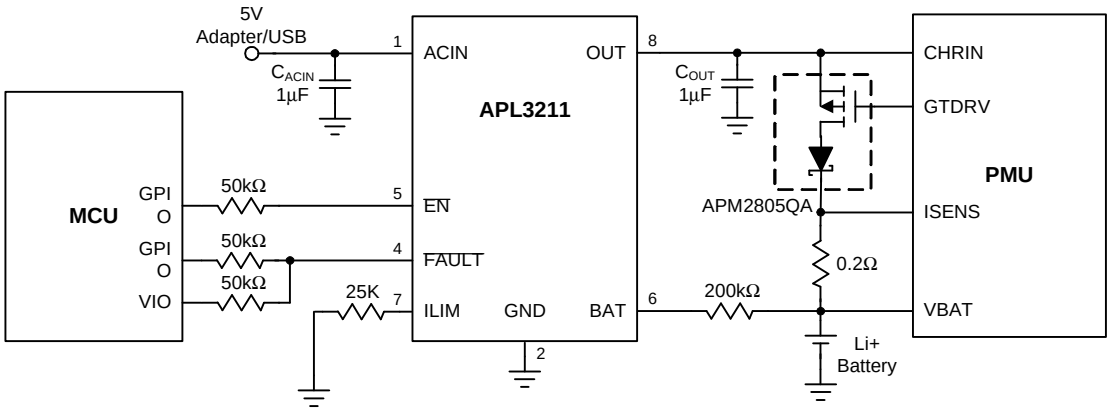


Figure 1. The Typical Protection Circuit for Charger Systems.

Designation	
C_{ACIN}	1µF, 25V, X5R, 0603 Murata GRM188R61E105K
C_{OUT}	1µF, 10V, X5R, 0603 Murata GRM188R61A105K

Murata website: www.murata.com

Function Description

ACIN Power-On-Reset (POR)

The APL3211A/B have a built-in power-on-reset circuit to keep the output shutting off until internal circuitry is operating properly. The POR circuit has hysteresis and a deglitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the POR threshold and after 8ms blanking time, the output voltage starts a soft-start to reduce the inrush current.

Input Over-Voltage Protection (OVP)

The input voltage is monitored by the internal OVP circuit. When the input voltage rises above the input OVP threshold, the internal FET will be turned off within 1µs to protect connected system on OUT pin. When the input voltage returns below the input OVP threshold minus the hysteresis, the FET is turned on again after 8ms recovery time. The input OVP circuit has a 250mV hysteresis and a recovery time of $T_{ON(OVP)}$ to provide noise immunity against transient conditions.(see Figure 2.)

Over-Current Protection (OCP)

The output current is monitored by the internal OCP circuit. When the output current reaches the OCP threshold, the device limits the output current at OCP threshold level. If the OCP condition continues for a blanking time of $T_{B(OCP)}$, the internal power FET is turned off. After the recovery time of $T_{ON(OCP)}$, the FET will be turned on again and the output current is monitored again. The OCP threshold is programmed by a resistor R_{ILIM} connected from ILIM pin to GND. The OCP threshold is calculated by the following equation:

$$I_{OCP} = \frac{K_{ILIM}}{R_{ILIM}}$$

where

K_{ILIM}=25000AΩ

Battery Over-Voltage Protection

The APL3211A/B monitor the BAT pin voltage for battery over-voltage protection. The battery OVP threshold is internally set to 4.35V. When the BAT pin voltage exceeds the battery OVP threshold for a blanking time of $T_{B(BOVP)}$, the internal power FET is turned off. When the BP voltage returns below the battery OVP threshold minus the hysteresis, the FET is turned on again. The APL3211A/B have a built-in counter. When the total count of battery OVP fault reaches 16, the FET is turned off permanently, requiring either a V_{IN} POR or $\overline{EN}$ re-enable again to restart.

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125 °C.

$\overline{FAULT}$ Output

The APL3211A/B provide an open-drain output to indicate that a fault has occurred. When any of input OVP, OCP, battery OVP, is detected, the FAULT goes low to indicate that a fault has occurred. Since the FAULT pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Enable/Shutdown

Pull the $\overline{EN}$ pin voltage above 1.4V to disable the device and pull $\overline{EN}$ pin voltage below 0.4V to enable the device. The $\overline{EN}$ pin has an internal pull-down resistor and can be left floating. When the IC is latched off due to the total count of OCP or battery OVP reaches 16, disable and re-enable the device with the $\overline{EN}$ pin can clear the counter.

ESD Tests

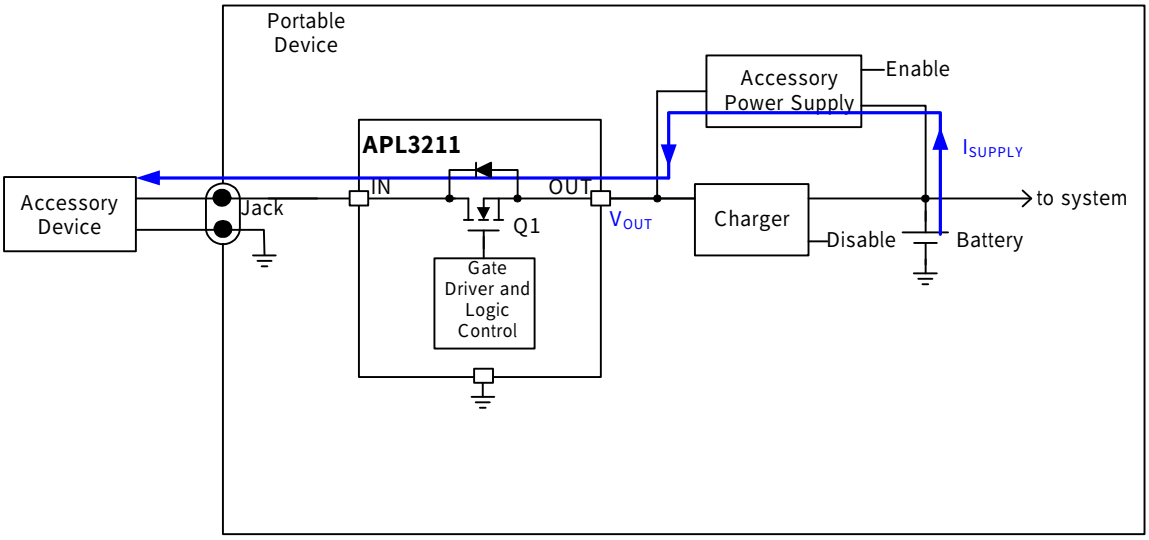
The APL3211A/B VIN input pin fully supports the IEC61000-4-2. That means the VIN pin has immunity of ±15kV ESD discharge in Air condition, and immunity of ±8kV ESD discharge in Contact condition.

Function Description (Cont.)

Powering an Accessory Device

In some applications, such as USB On-The-Go, users need to power an accessory device by using the portable device's battery through the jack holes of AC adapter. The APL3211A/B provide reverse current flow path from OUT to IN.

If $V_{OUT} > V_{POR} + 0.7V$, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 will then remain ON as long as $V_{OUT} > V_{POR}-V_{POR\_HYS} + R_{DS\_ON}*ISUPPLY$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.5A. It should be noted that there is no overcurrent protection in this direction.



Function Description (Cont.)

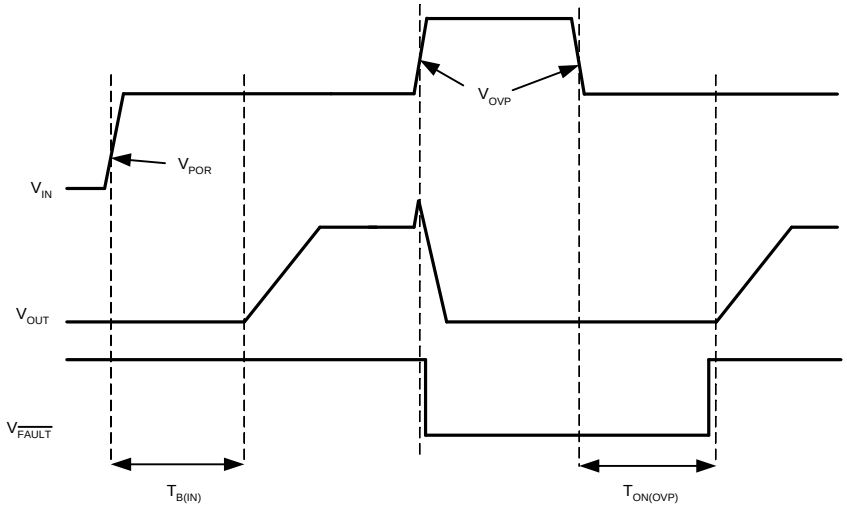


Figure 2. OVP Timing Chart

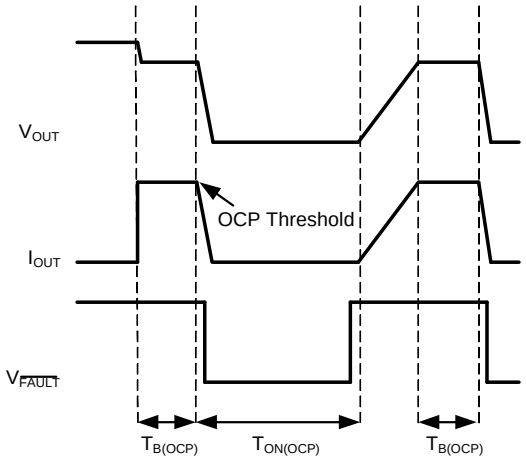


Figure 3. OCP Timing Chart

Function Description (Cont.)

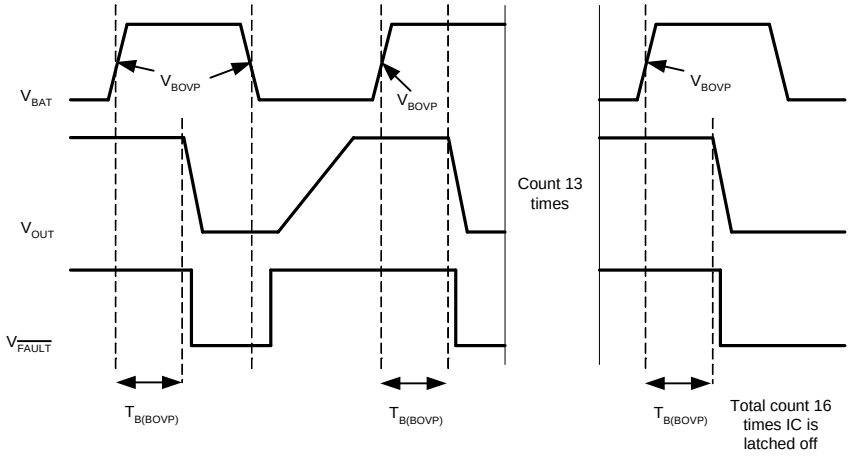


Figure 4. Battery OVP Timing Chart

Application Information

R_{BAT} Selection

Connect the BAT pin to the positive terminal of battery through a resistor R_{BAT} for battery OVP function. The R_{BAT} limits the current flowing from BAT to battery in case of BAT pin is shortened to VIN pin under a failure mode. The recommended value of R_{BAT} is 100kΩ. In the worse case of an IC failure, the current flowing from the BAT pin to the battery is:

(30V-3V)/ 100kΩ =270μA

where the 30V is the maximum IN voltage and the 3V is the minimum battery voltage. The current is so small and can be absorbed by the charger system.

The disadvantage with the large R_{BAT} is that the error of the battery OVP threshold will be increased. The additional error is the voltage drop across the R_{BAT} because of the BAT bias current. When R_{BAT} is 100kΩ, the worse-case additional error is 100kΩx20nA=2mV, which is acceptable in most applications.

R_{EN} Selection

For the same reason as the BAT pin case, the EN pin should be connected to the MCU GPIO pin through a resistor. The value of the R_{EN} is dependent on the IO voltage of the MCU.

Since the IO voltage is divided by R_{EN} and $\overline{EN}$ internal pull low resistor for $\overline{EN}$ voltage. It has to be ensured that the $\overline{EN}$ voltage is above the $\overline{EN}$ logic high voltage when the GPIO output of the MCU is high.

$\overline{FAULT}$ Output

Since the FAULT pin is an open-drain output, connecting a resistor R_{UP} to a pull high voltage is necessary. It is also recommended that connect the $\overline{FAULT}$ to the MCU GPIO through a resistor R_{FAULT}. The R_{FAULT} prevents damage to the MCU under a failure mode. The recommended value of the resistors should be between 10kΩ to 100kΩ.

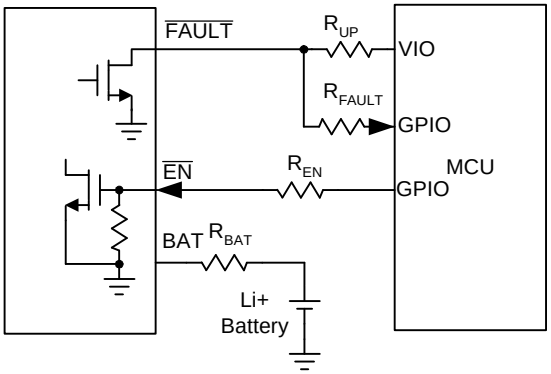


Figure 5. R_{UP}, R_{FAULT}, R_{EN} and R_{BAT}

Capacitor Selection

The input capacitor is for decoupling and prevents the input voltage from overshooting to dangerous levels. In the AC adapter hot plug-in applications or load current step-down transient, the input voltage has a transient spike due to the parasitic inductance of the input cable. A 25V, X5R, dielectric ceramic capacitor with a value between 1μF and 4.7μF placed close to the IN pin is recommended.

The output capacitor is for output voltage decoupling, and also can be as the input capacitor of the charging circuit. At least, a 1μF, 10V, X5R capacitor is recommended.

Layout Consideration

In some failure modes, a high voltage may be applied to the device. Make sure the clearance constraint of the PCB layout must satisfy the design rule for high voltage.

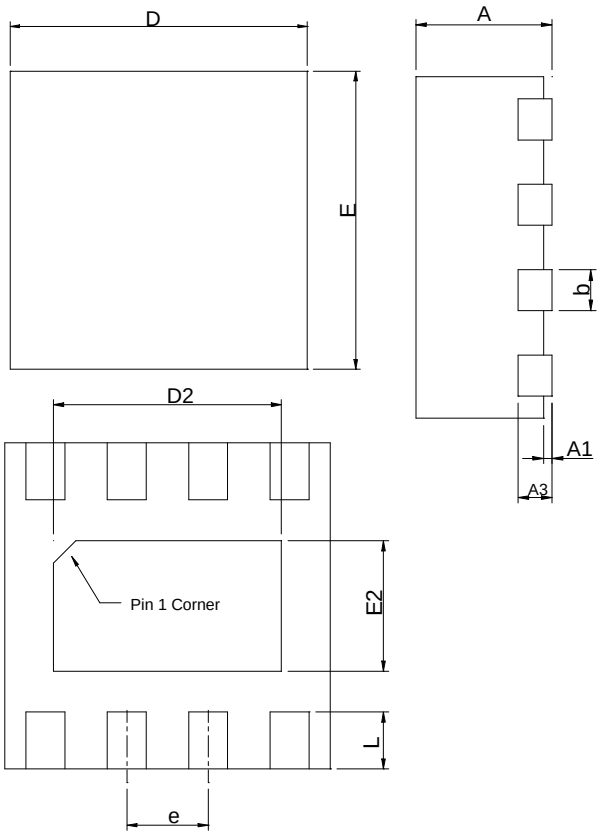
The exposed pad of the TDFN2x2-8 performs the function of channeling heat away. It is recommended that connect the exposed pad to a large copper ground plane on the backside of the circuit board through several thermal vias to improve heat dissipation.

The input and output capacitors should be placed close to the IC. R_{ILIM} also should be placed close to the IC.

The high current traces like input trace and output trace must be wide and short.

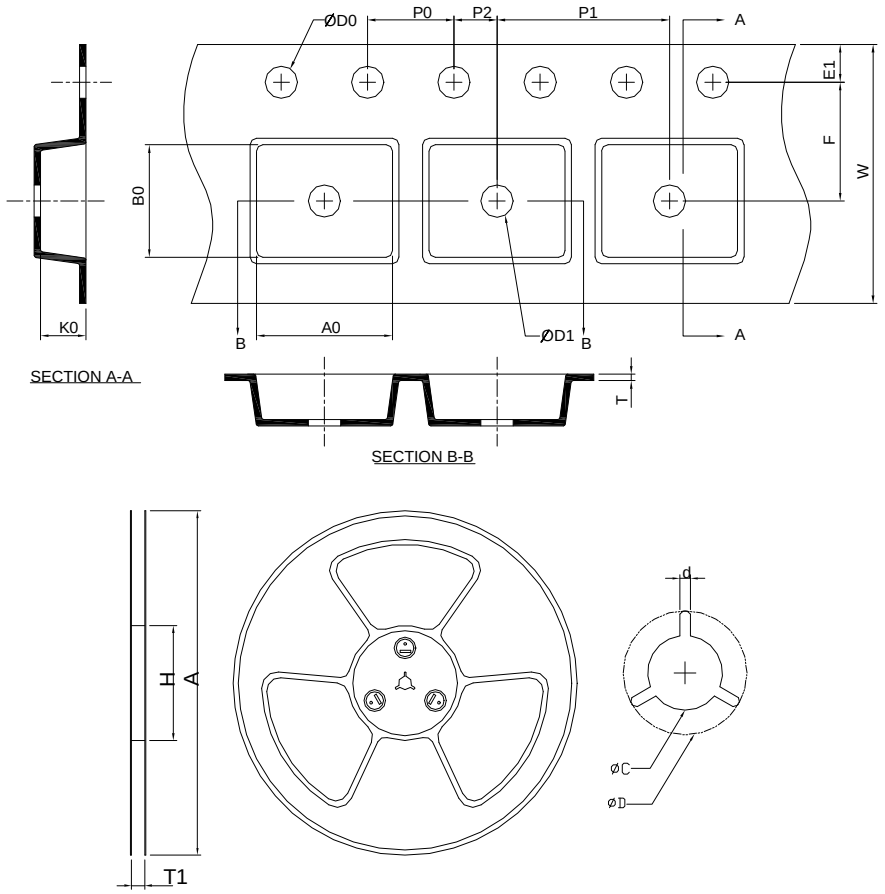
Package Information

TDFN2x2-8



SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20

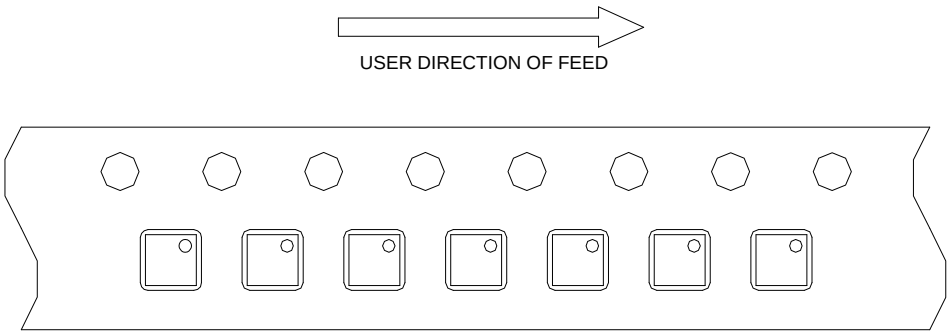
(mm)

Devices Per Unit

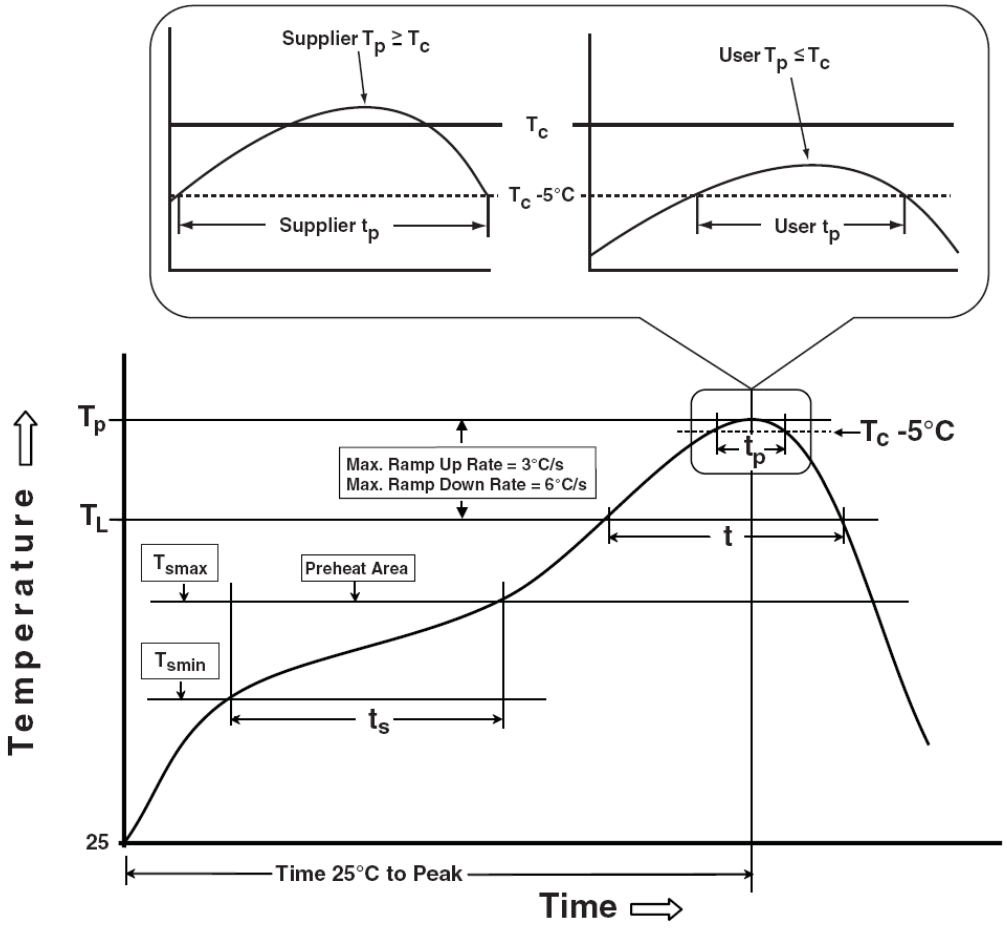
Package Type	Unit	Quantity
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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