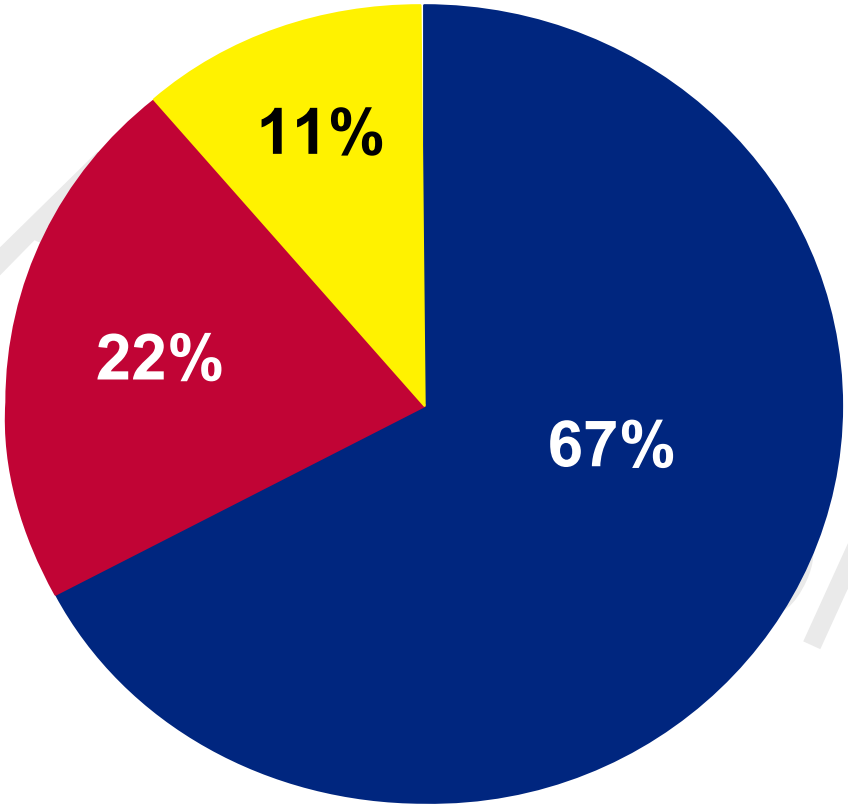
Power Reduction Techniques

Altera Asia Pacific Regional Support Center

Agenda

- Introduction
- Power-Driven Synthesis
- Power-Driven Fitting
- Clock Power Management
- Low-Power Design
- Conclusion

Introduction

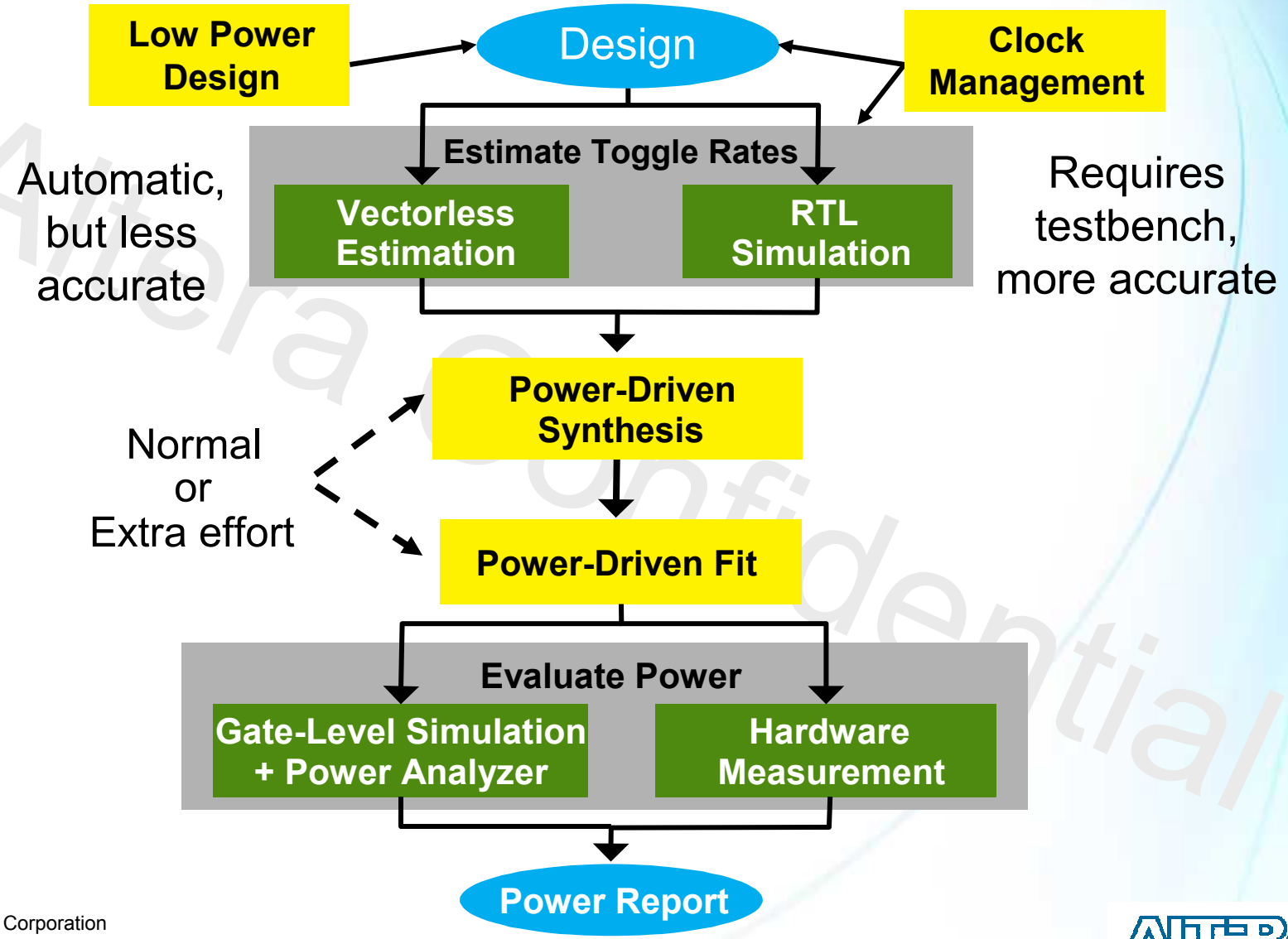


99 Customer Designs on Stratix II Devices

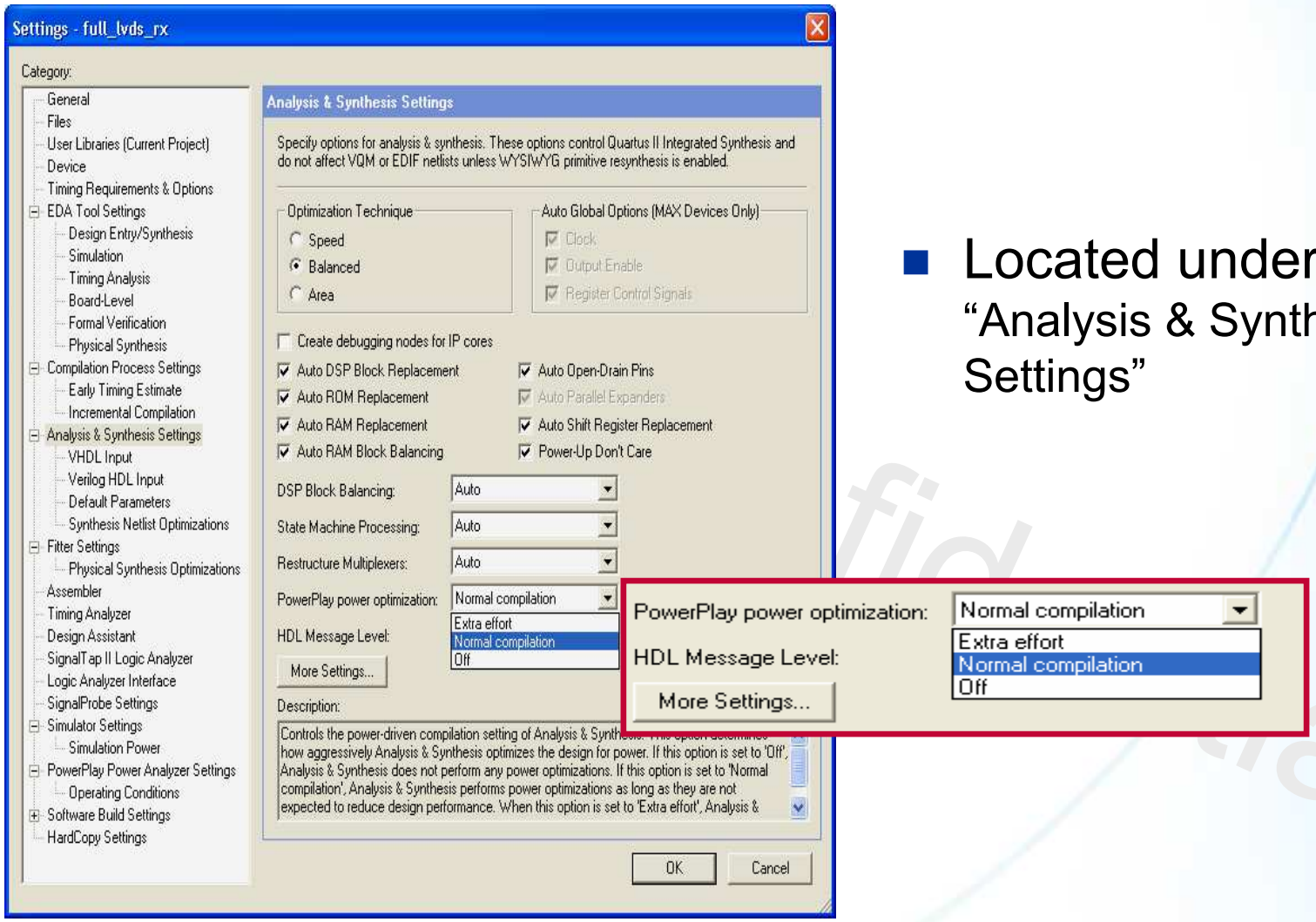
- Core Dynamic
- Core Static
- I/O

Dynamic Power Dominant Focus of Power Optimization

Dynamic Power Optimization Flow



Power-Driven Synthesis



- Located under:
  "Analysis & Synthesis Settings"

Power-Driven Synthesis Options

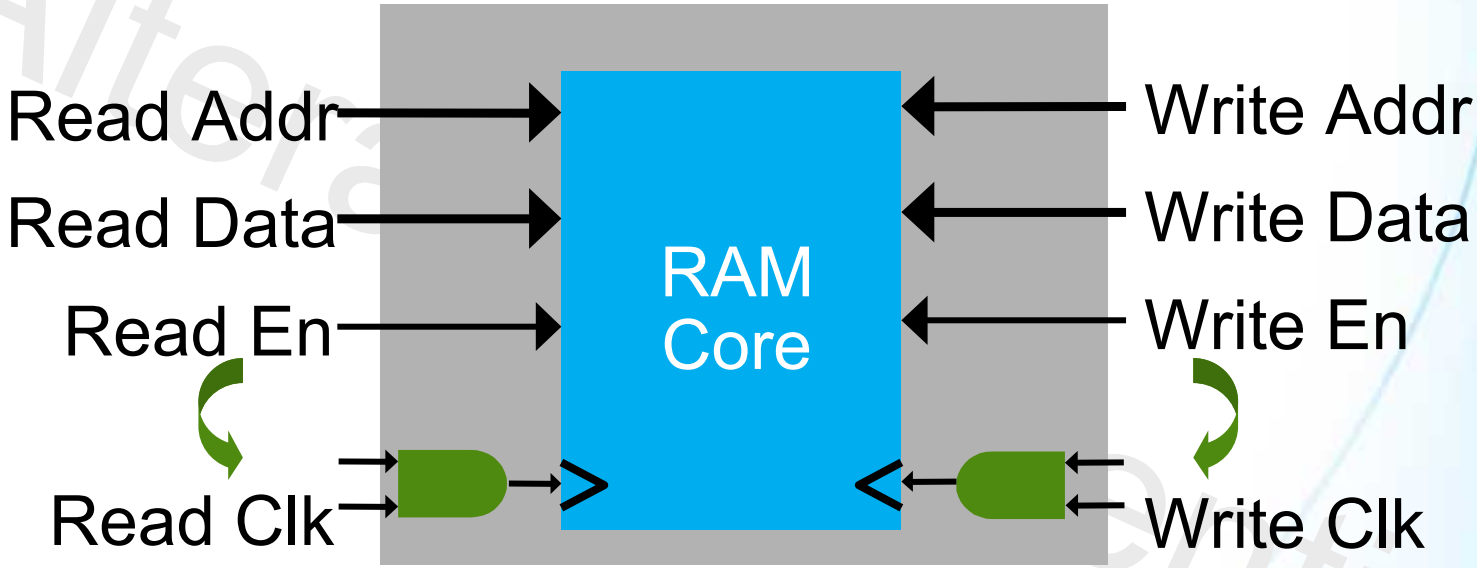
- Extra effort
  - More power reduction
  - May increase compile time
- Normal compilation (Default)
  - Standard power reduction
  - No effect on compile time or design performance
- Off
  - No optimization

Power-Driven Synthesis for RAM

- Memory Optimization
  - Normal compilation Setting
    - Promote Read/Write Enable Signals to Clock Read/Write Enable Signals
  - Extra effort Setting
    - Promote Read/Write Enable Signals to Clock Read/Write Enable Signals
    - **AND** Power-Aware Memory Balancing
- Memory Balancing configures RAM for optimal need
  - Default setting selects narrow/deeper memory configurations
    - e.g. 4 1k x4 blocks (x4=narrow; 1kwords=deeper)
  - MW “Maximum Depth” option selects wider/shallow RAMs for power
    - e.g. 4 256 x16 blocks (x16=wider; 256words=shallow)
    - Access only valid memory slice, disable the rest
    - Does require additional decoder and mux logic however

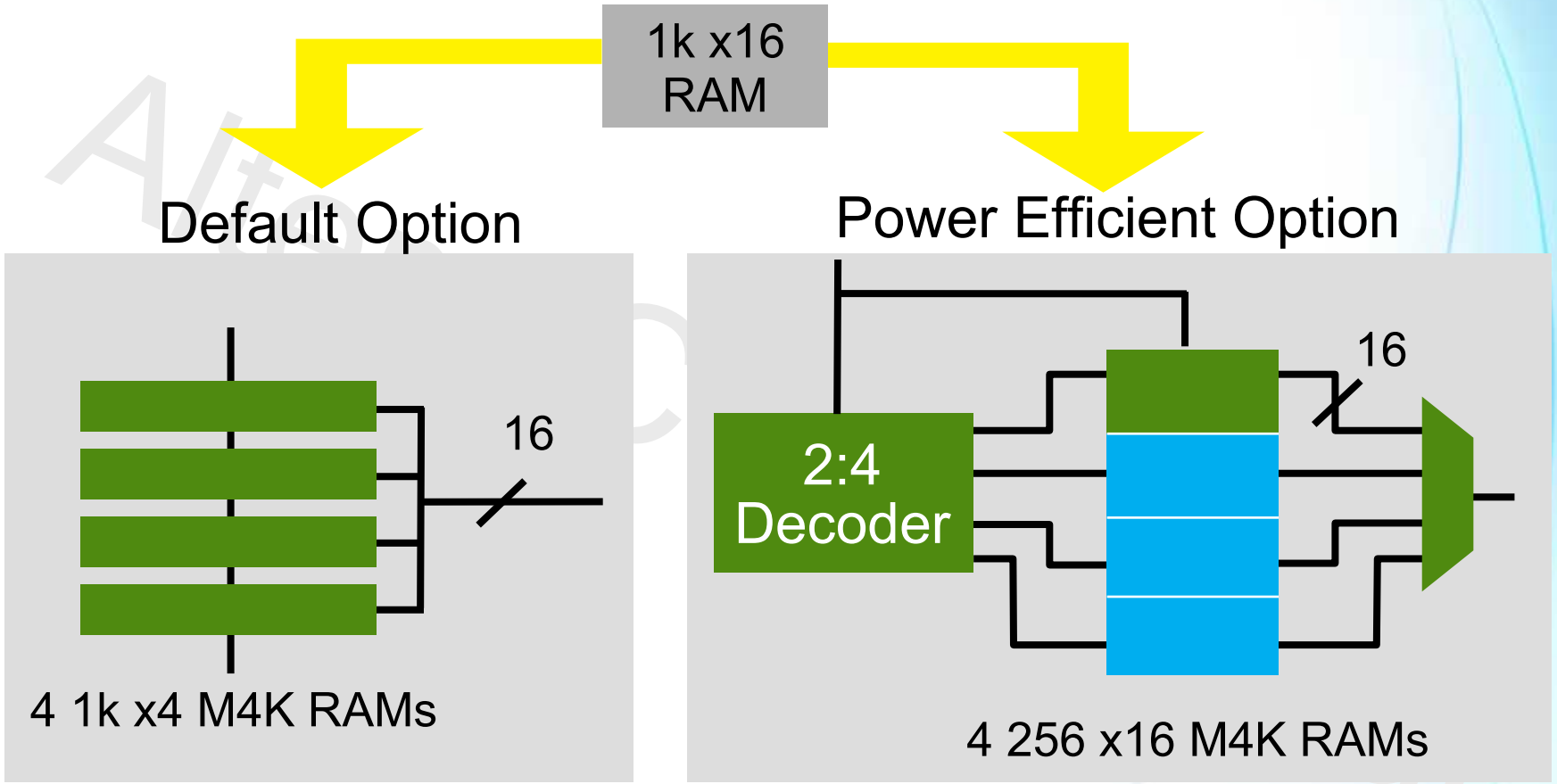
RAM Enable Optimization

- Convert read/write enables to clock read/write enables
  - Shuts RAM down when unused, using less power



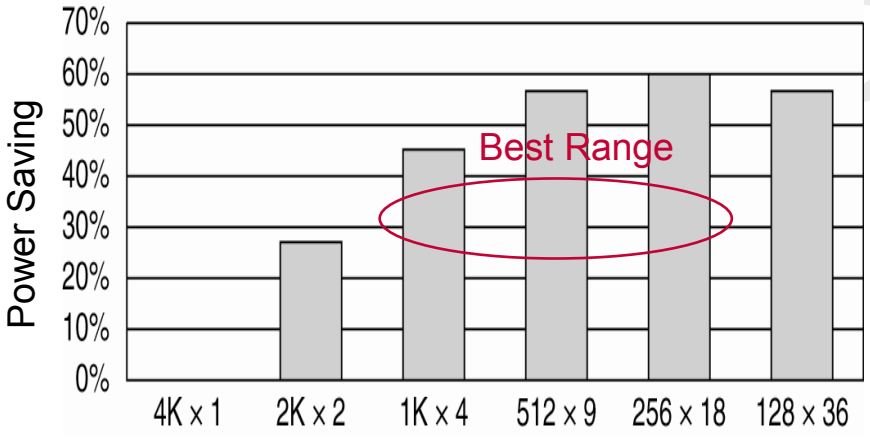
- Set RAM Block Type = “Auto”
  - Quartus II Power Optimizer chooses best RAM block configuration

Memory Balancing



Maximum Depth Parameter

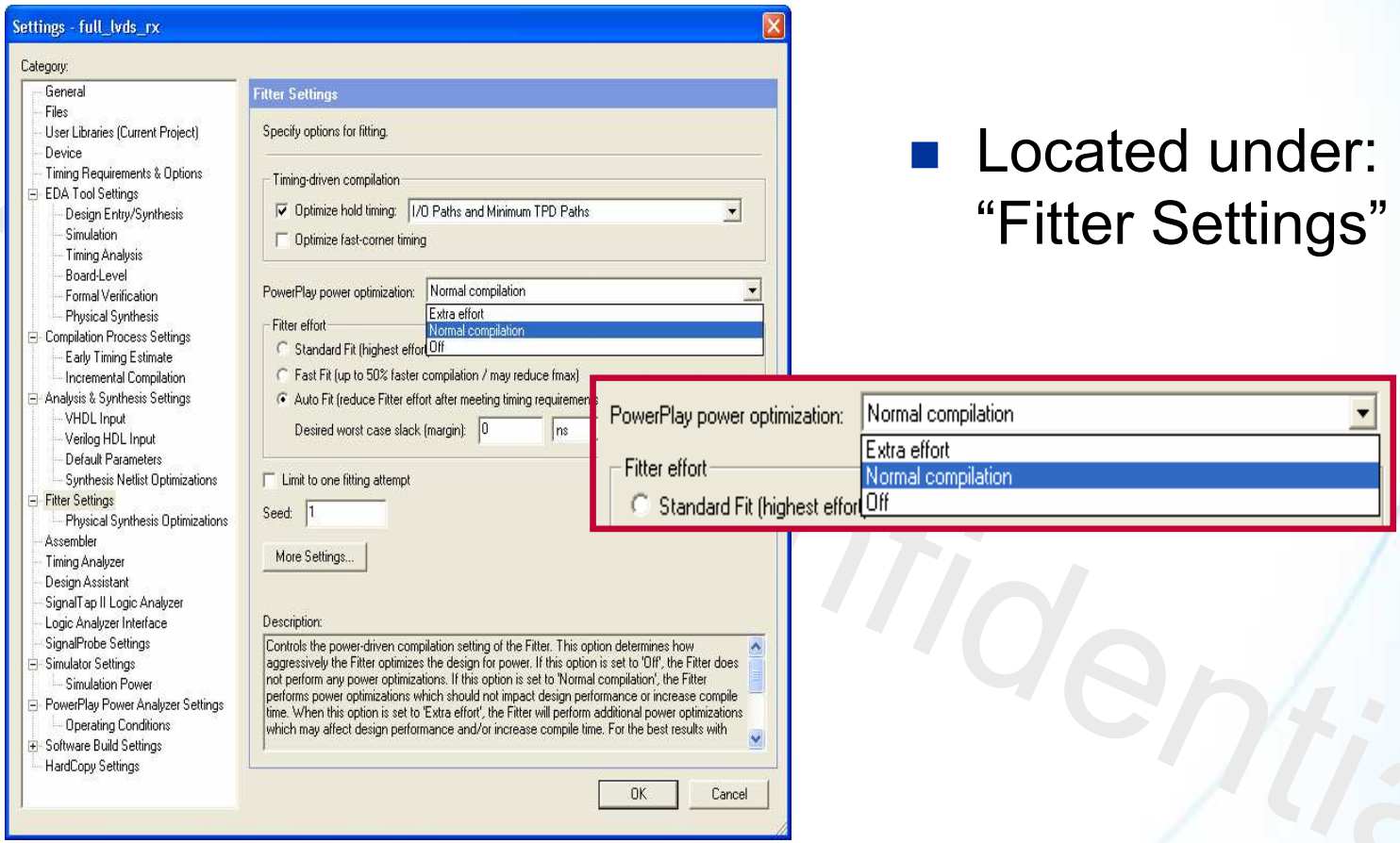
M4K Configuration	Number of M4K Blocks	ALUTs
4K x 1 (default setting)	36	0
2K x 2	36	40
1K x 4	36	62
512 x 9	32	143
256 x 18	32	302
128 x 36	32	633



M4K Blocks Configuration with Different Memory Depth and Width

- 4k x36 Simple Dual-Port memory implementation using M4K blocks
- For 128-deep M4K memory block depth, extra logic power outweighs lower memory power
- Average Dynamic Power saving up to 50%
- PowerPlay Power Analyzer results based on simulation

Power-Driven Fitting



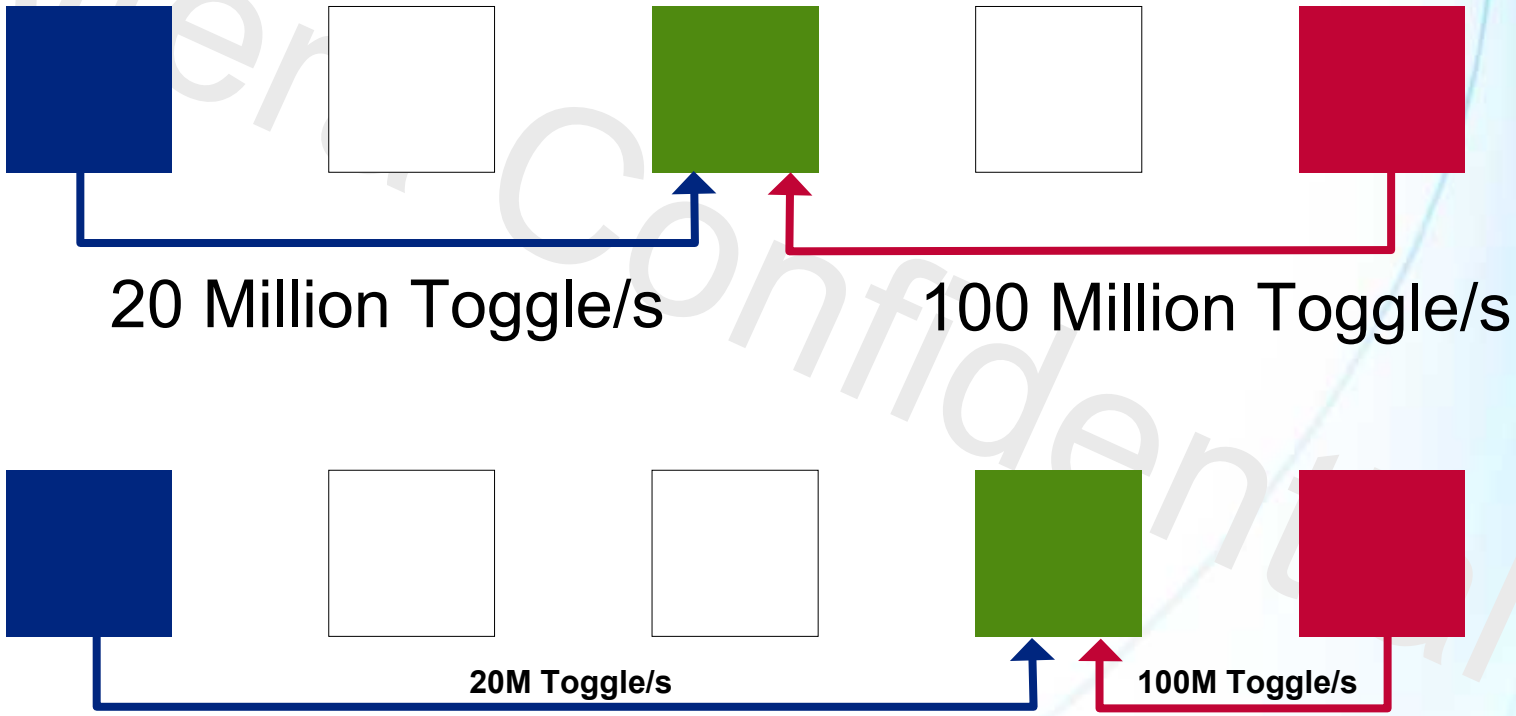
- Located under: “Fitter Settings”

Power-Driven Fitting Options

- Extra effort
  - Optimizes at the expense of speed and compile time
    - Group high-toggling logic together to minimize routing loads
    - Group logic from same clock domains to minimize clock routing
  - Runs PowerPlay Power Analyzer
    - Best with Value Charge Dump (.VCD) or Signal Activity (.SAF)
- Normal compilation
  - Optimizes without affecting speed or compile time
    - Uses power efficient DSP block configurations by swapping input operand order (transparent to designer)

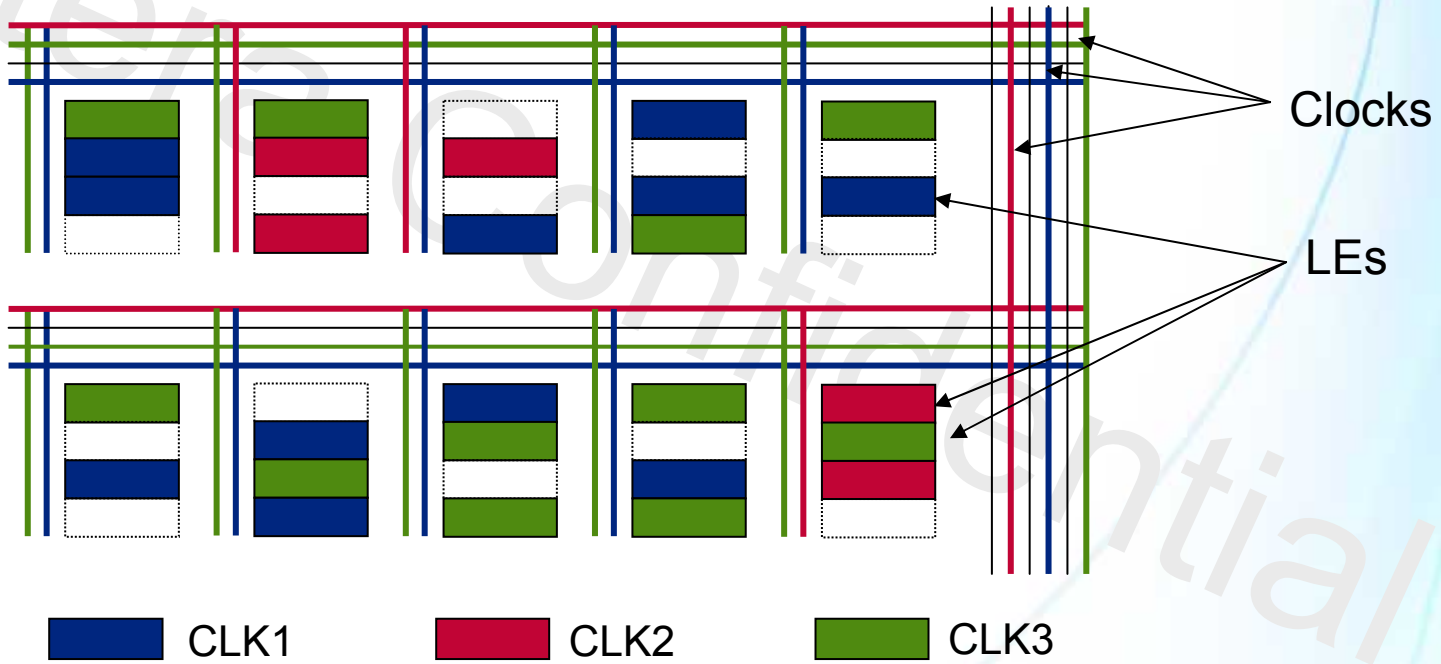
Minimize Routing Loads

- Minimize capacitance of high-toggling signals
- Timing constraints maintained



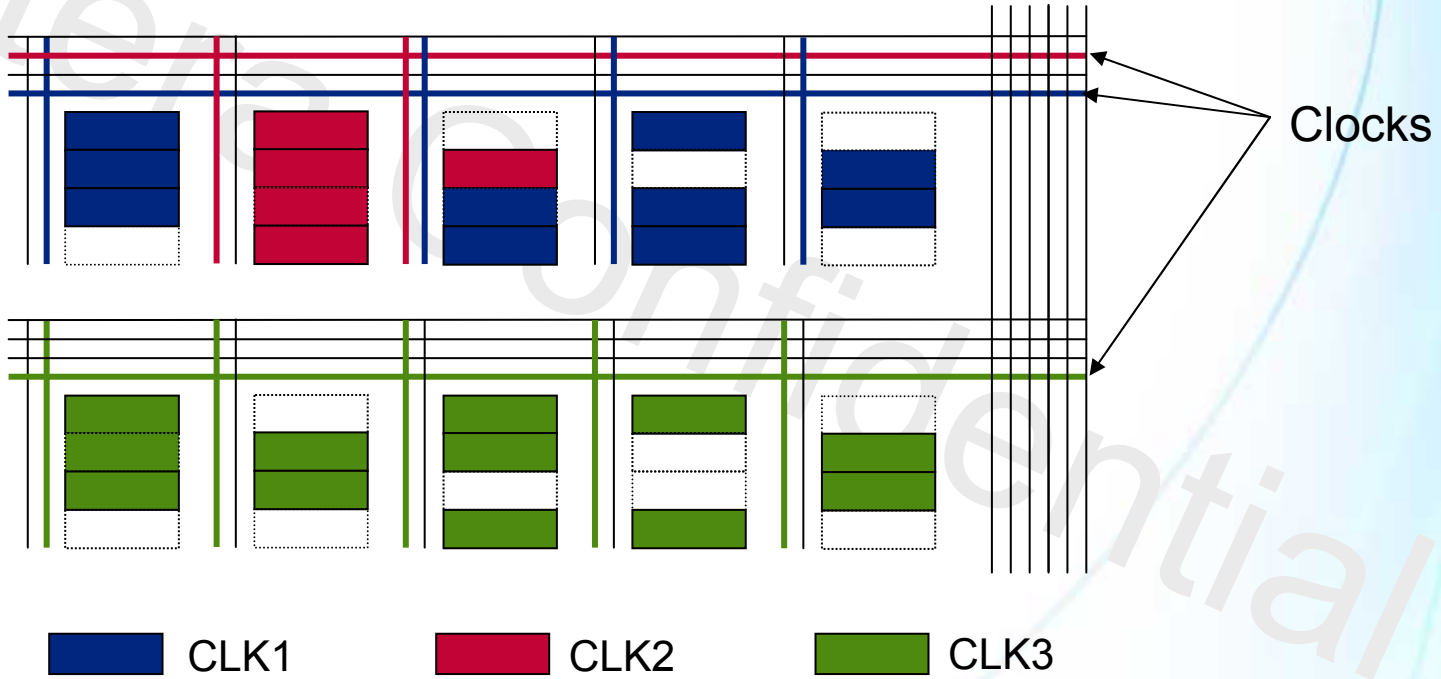
Minimize Clock Routing

- Standard Place & Route
  - Places logic for optimal timing and routing usage
  - Minimizing clock power not high priority



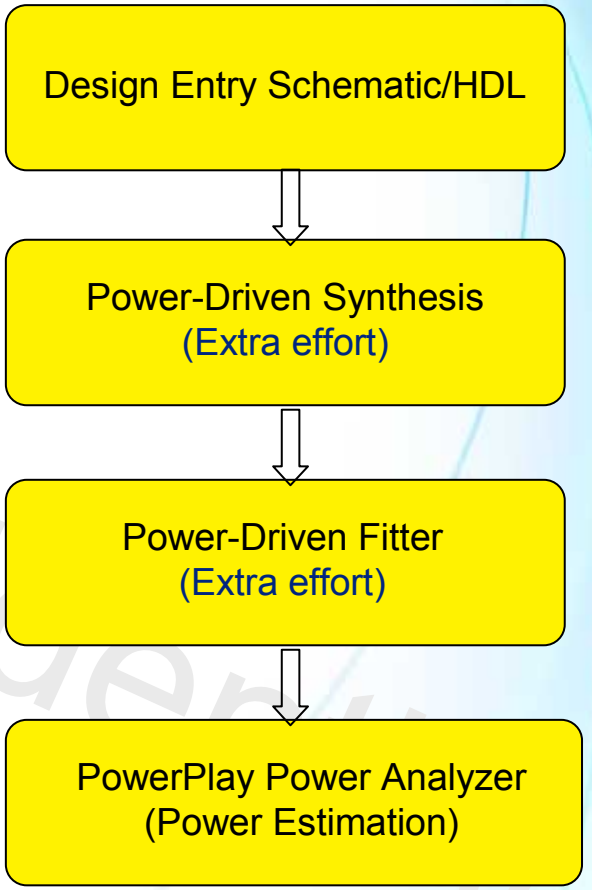
Minimize Clock Routing (ctd)

- Extra effort Place & Route
  - Groups logic from same clock domain with each other
  - Reduces utilized clock routing (and therefore switching power)



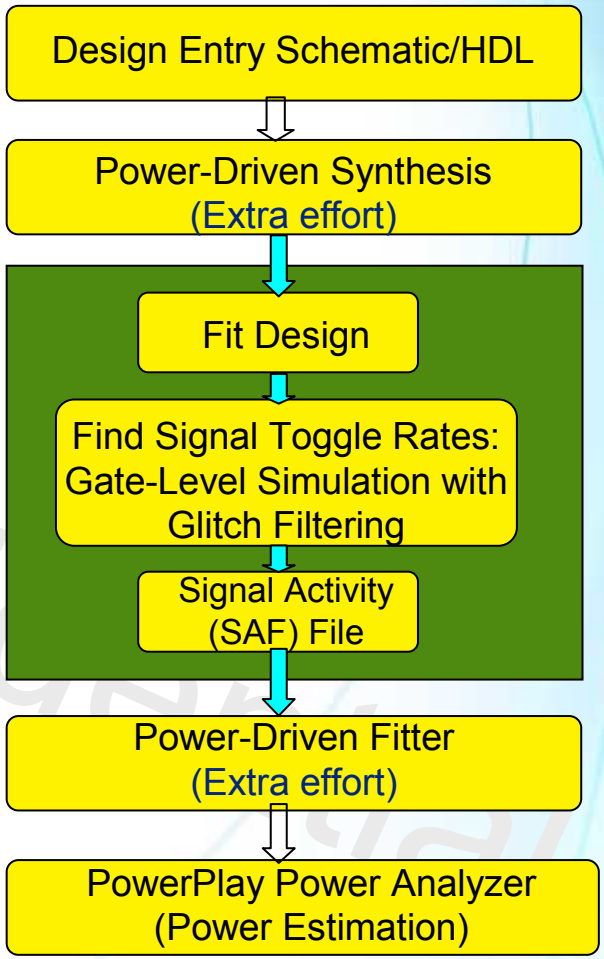
Power Optimization Flow (Default)

- Straight-forward
- Longer compile times
- Not fully optimized for Power



Power Optimization Flow (for Power)

- Accurate toggle rates from simulation
  - SAF provides design signal activity information
  - Processes Power Analyzer input constraints
- Even longer compile times
- **But fully optimized for Power**

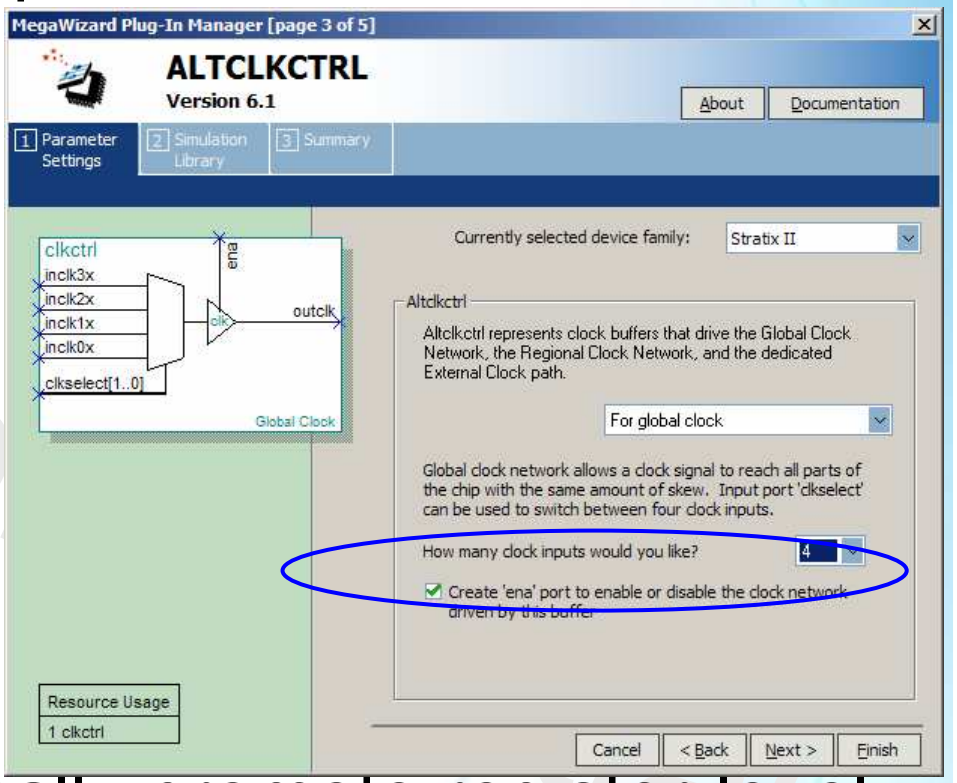


Clock Power Management

- Clocks represent a significant portion of Core Dynamic Power consumption
- Clock routing power is automatically optimized by the Quartus II software where possible
  - Clock domains (under Power-Driven Fitting)
- Dynamic clock-enables driven by internal logic provides further clock routing power reduction

Dynamic Clock Enable

- Use Enable to shut down entire clock domains
  - Entire clock domain unused in some cycles at times
  - Use MegaWizard manager to generate these blocks
    - **altclkctrl** MegaFunction
  - Consumes less power than routing a clock enable to all registers
  - Available on global & regional clock network



- Quartus II can automatically promote register-level clock enables to LAB-block level Enables

Coding Dynamic Clock Enables

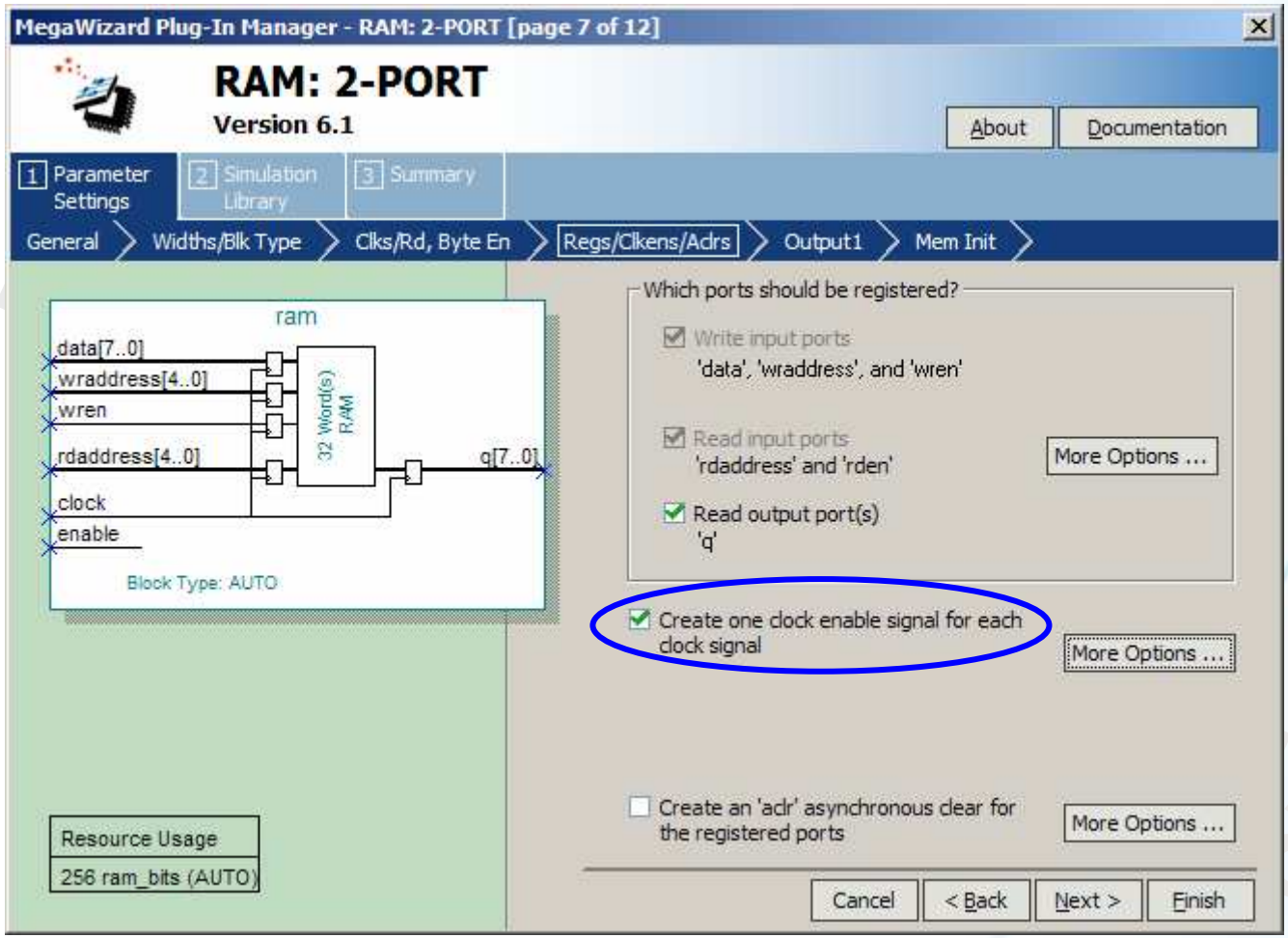
- LAB-wide clock enables allow clock gating at LAB level
- Shutting off LAB-wide clock enable lowers switching power
  - Global clock network remains unaffected
- Clock enables automatically promoted to LAB-wide enables
  - Must be coded correctly

```
always @ (posedge clk)
begin
   if (enable)
      reg <= new_value;
   else
      reg <= reg;
end;
```

Dynamic Clock Enable for RAMs

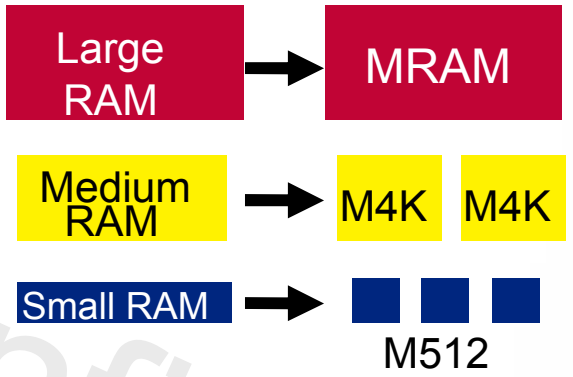
- RAM power primarily from dynamic clocking
  - Pre-charge, discharge of RAM array
  - Reducing number of clock events reduces dynamic power
- Address/data inputs have minimal effect on power
  - Internal memory circuitry active whether address or data has changed
- Use memory clock enable control in MegaWizard
  - Can obtain near zero dynamic power on cycles when RAM not accessed

Dynamic Clock Enable in MegaWizard

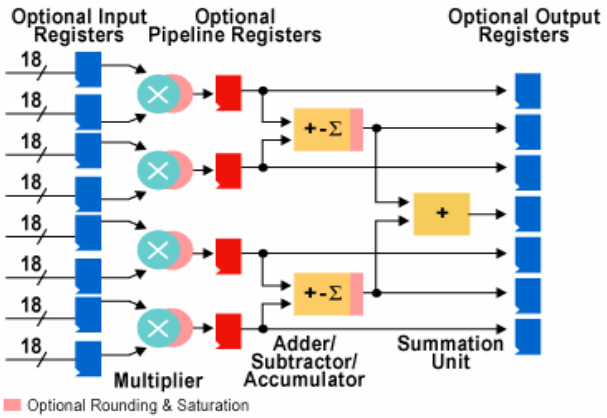


Low-Power Design

- Design techniques utilize specific architecture features, focusing on low power
- TriMatrix memory optimized for different RAM functions
  - Quartus II can select best size and configuration
  - Use **altsyncram** MegaFunction

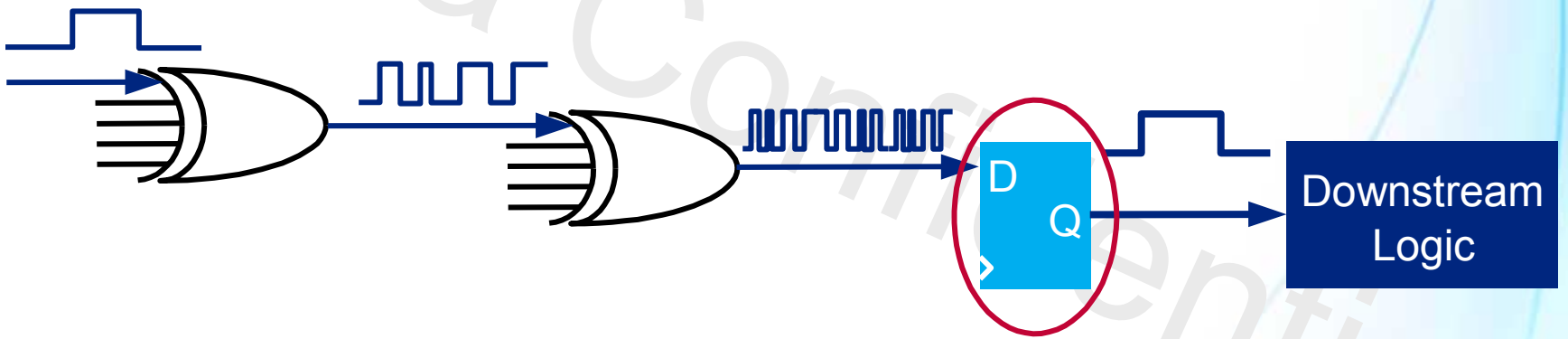


- DSP Implementation
  - Mode Multiplication
  - Multiply-Accumulation
  - Multiply-Addition
  - Less power than using ALM



Low-Power Design – Glitch Reduction

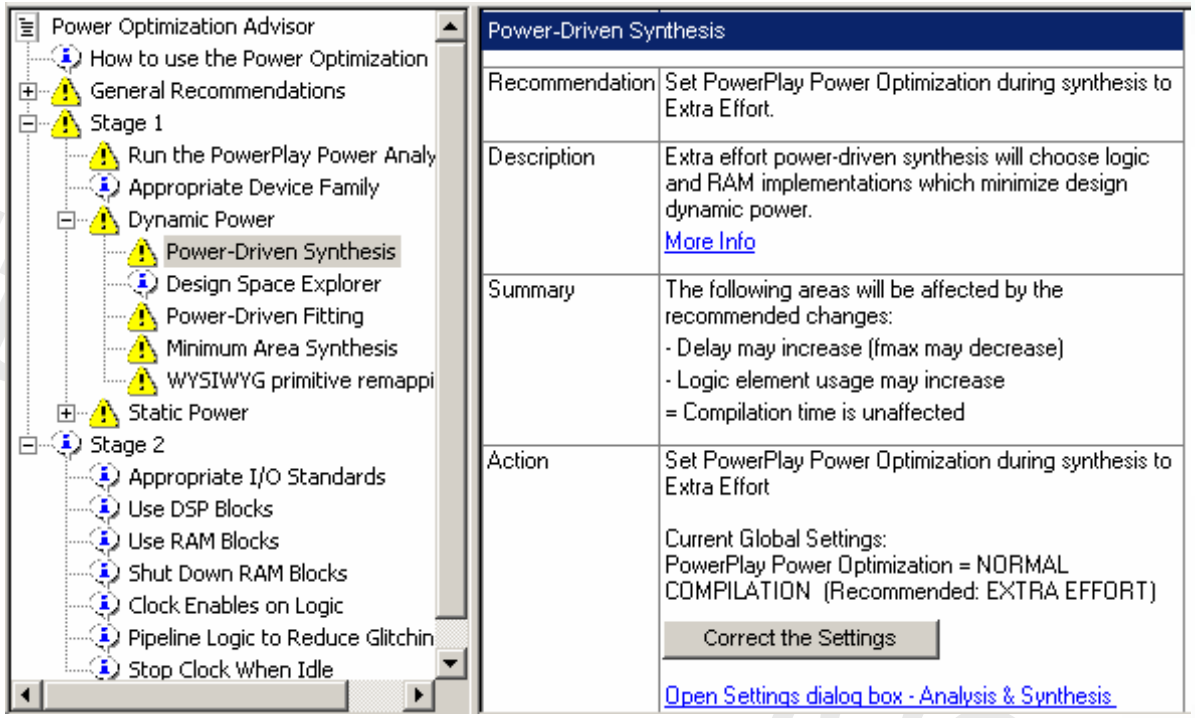
- Some logic produces many edges/transitions per cycle
  - E.g. CRC/parity, combinational multipliers
  - Each transition, or glitch, results in unnecessary power consumption
  - Register inputs & outputs of to filter out “glitchy” behavior
  - Insert pipeline registers if possible



Low-Power Design – Pipelining

- Effective for glitch prone arithmetic systems
- Advantages
  - Increased speed
  - Short logic depth
  - Reduced switching (less dynamic power)
- Disadvantages
  - Increased logic and register utilization
  - May increase power for designs with minimal glitches
  - Latency and throughput changed

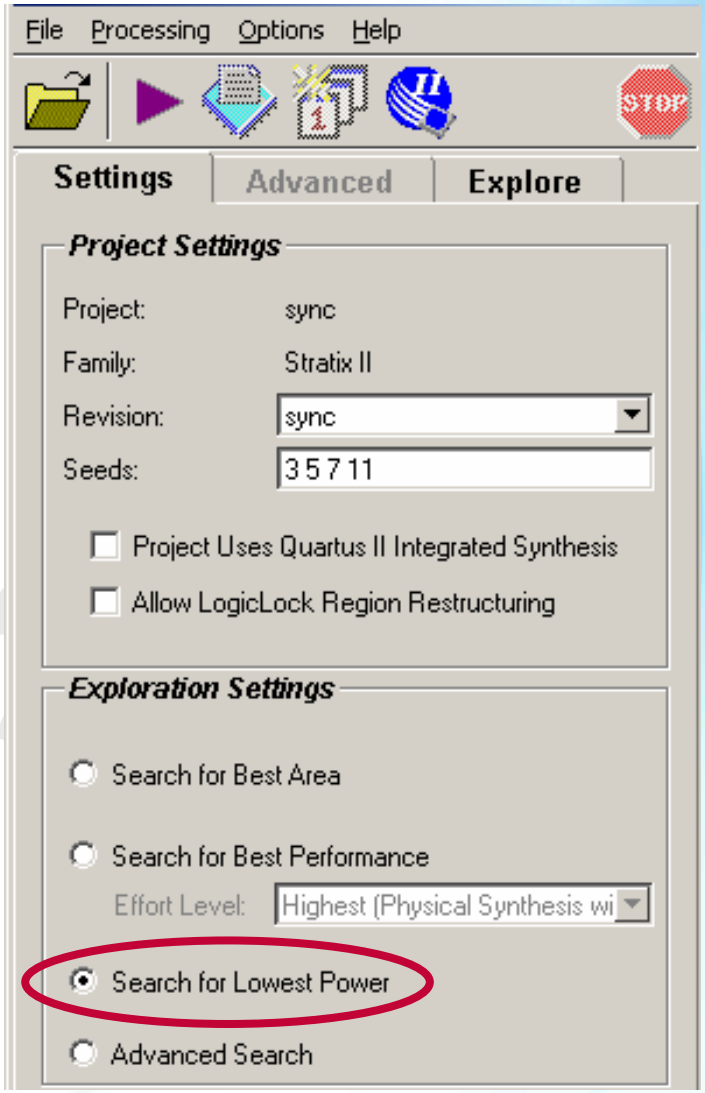
Power Optimization Advisor



- Explains power analysis best practices
- Provides Optimization suggestions
- Highlights recommended settings not enabled in design

Design Space Explorer

- Searches Quartus options to find best implementation
  - "Search for Lowest Power"
  - Finds settings that minimize power while meeting timing constraints
  - "quartus_sh –dse", or Tools Menu



Conclusion

- Power reduction is a major part of successful FPGA design
- Quartus II software provides options to reduce power
  - Power-Driven Synthesis
  - Power-Driven Fitting
- Low-Power Design techniques reduce power further
  - Adding Clock Enables can reduce switching power
  - Glitch-Removal, Pipelining also reduces power
- Power Optimization Advisor
- Design Space Explorer settings for lowest power