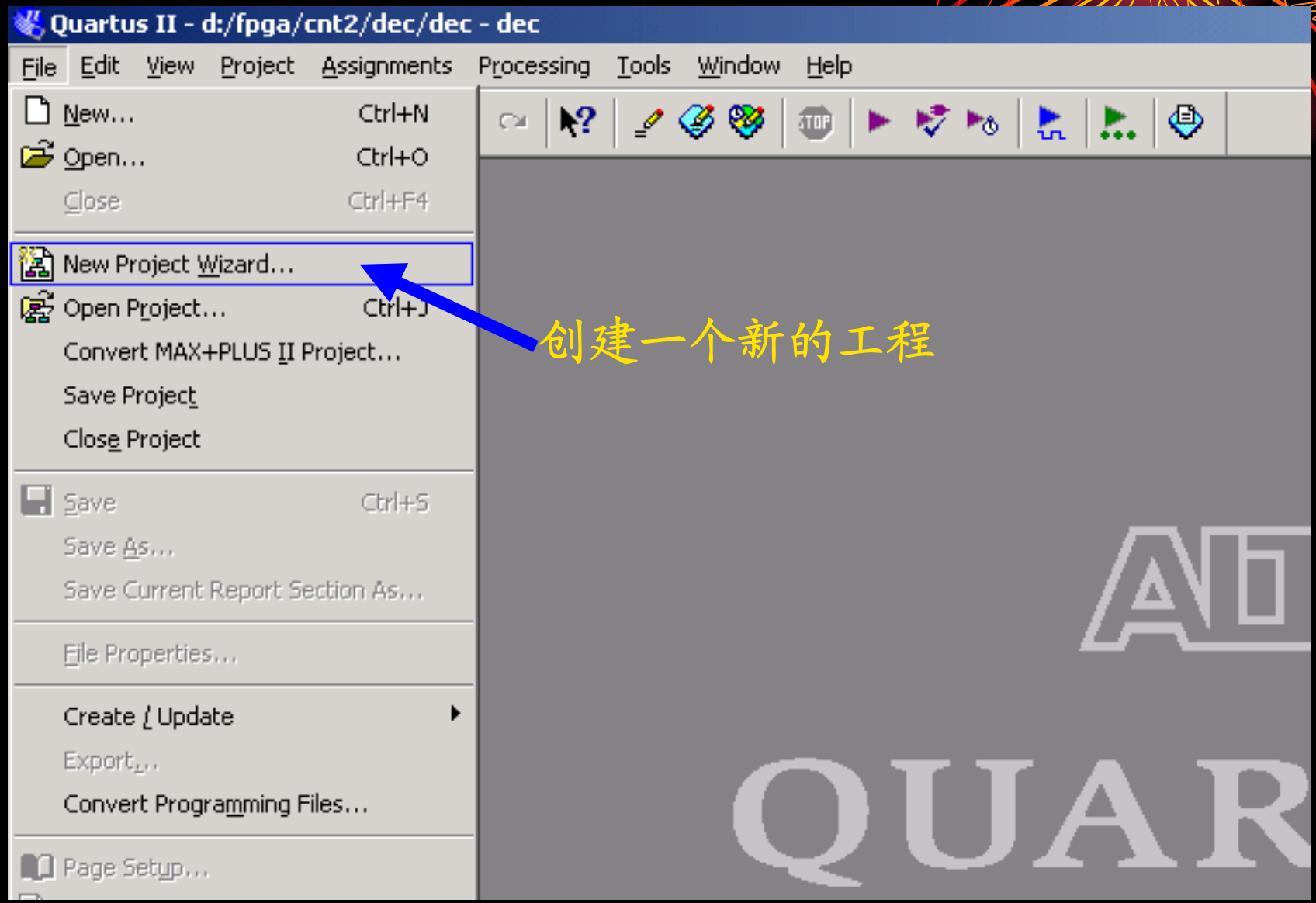
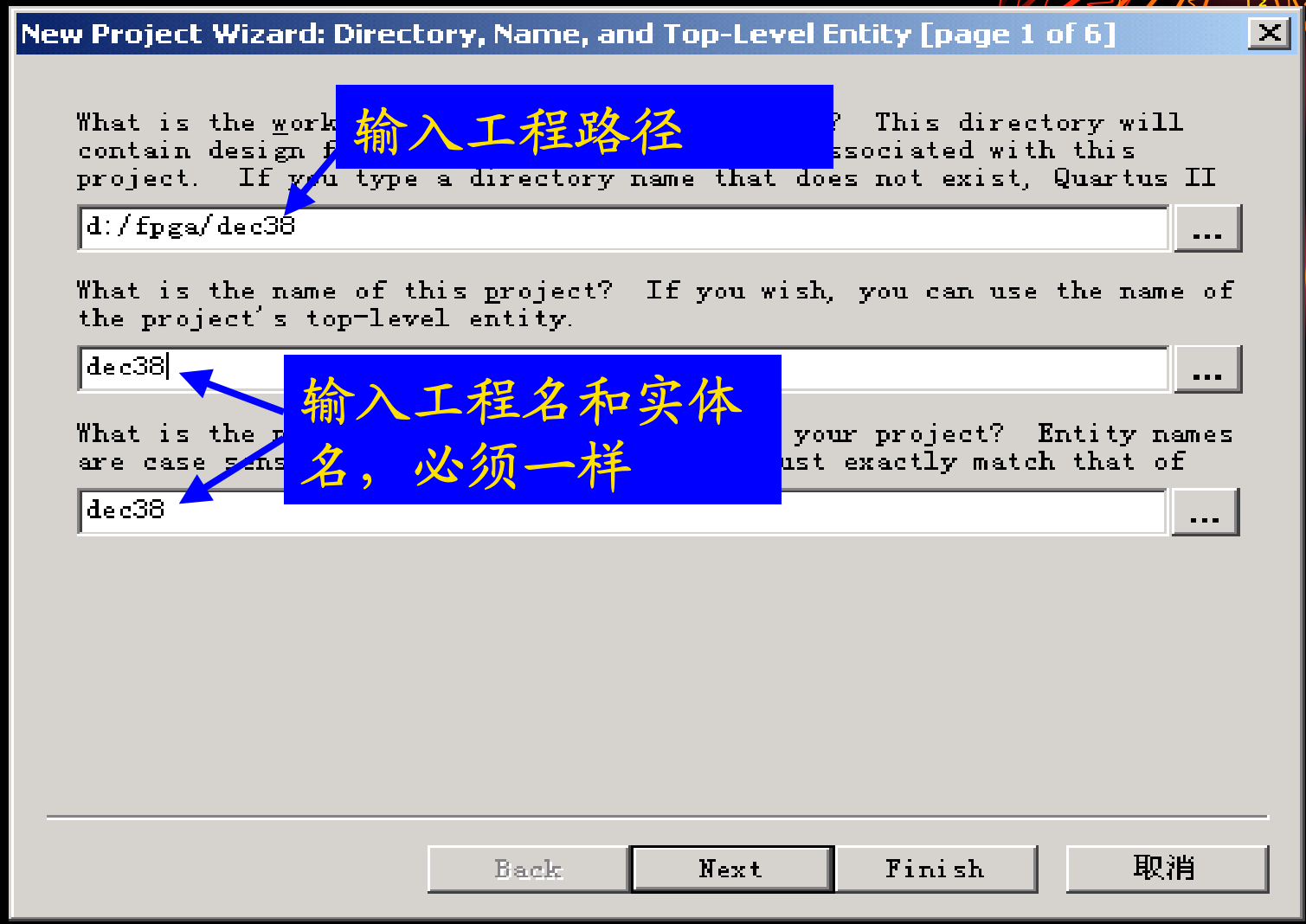
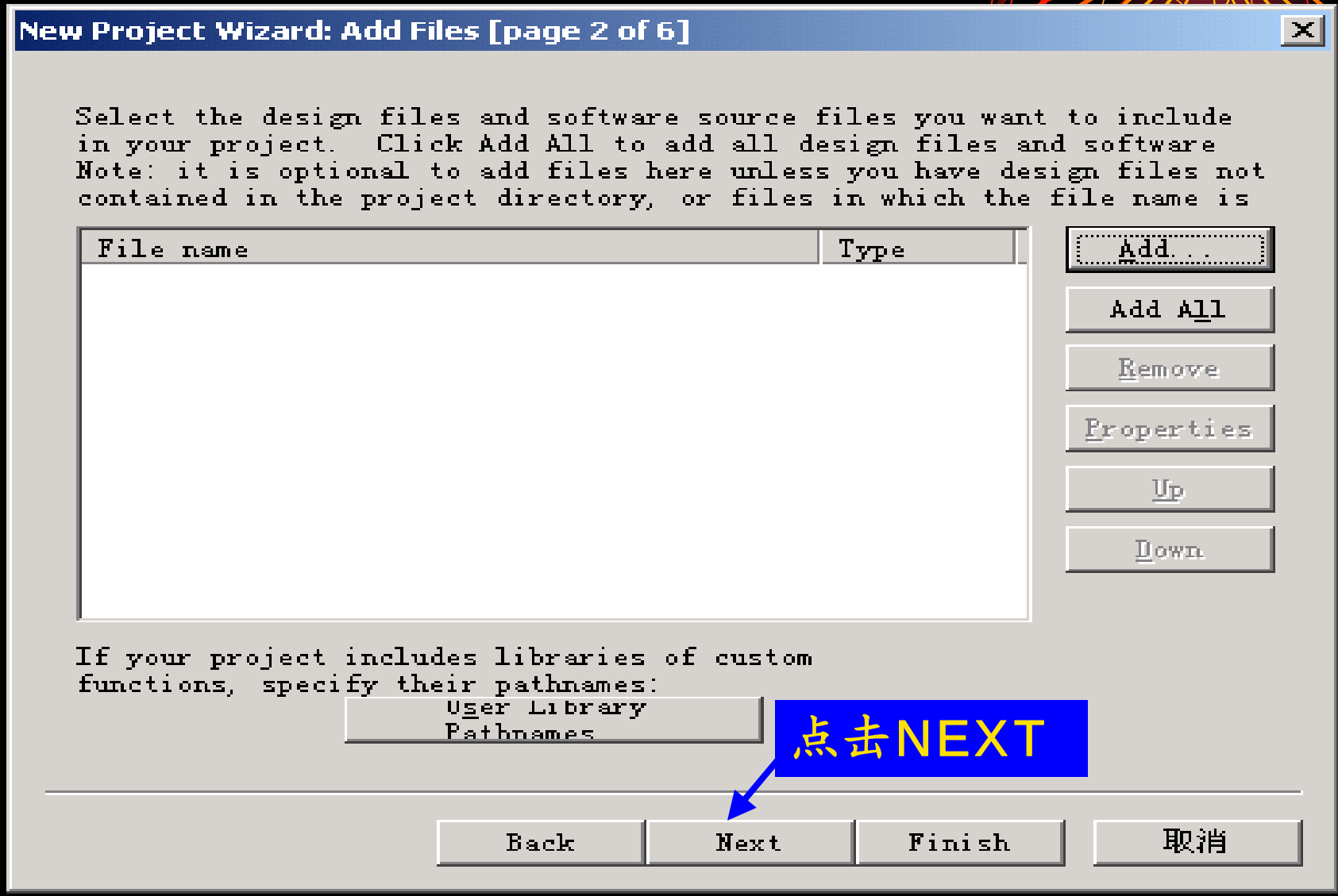
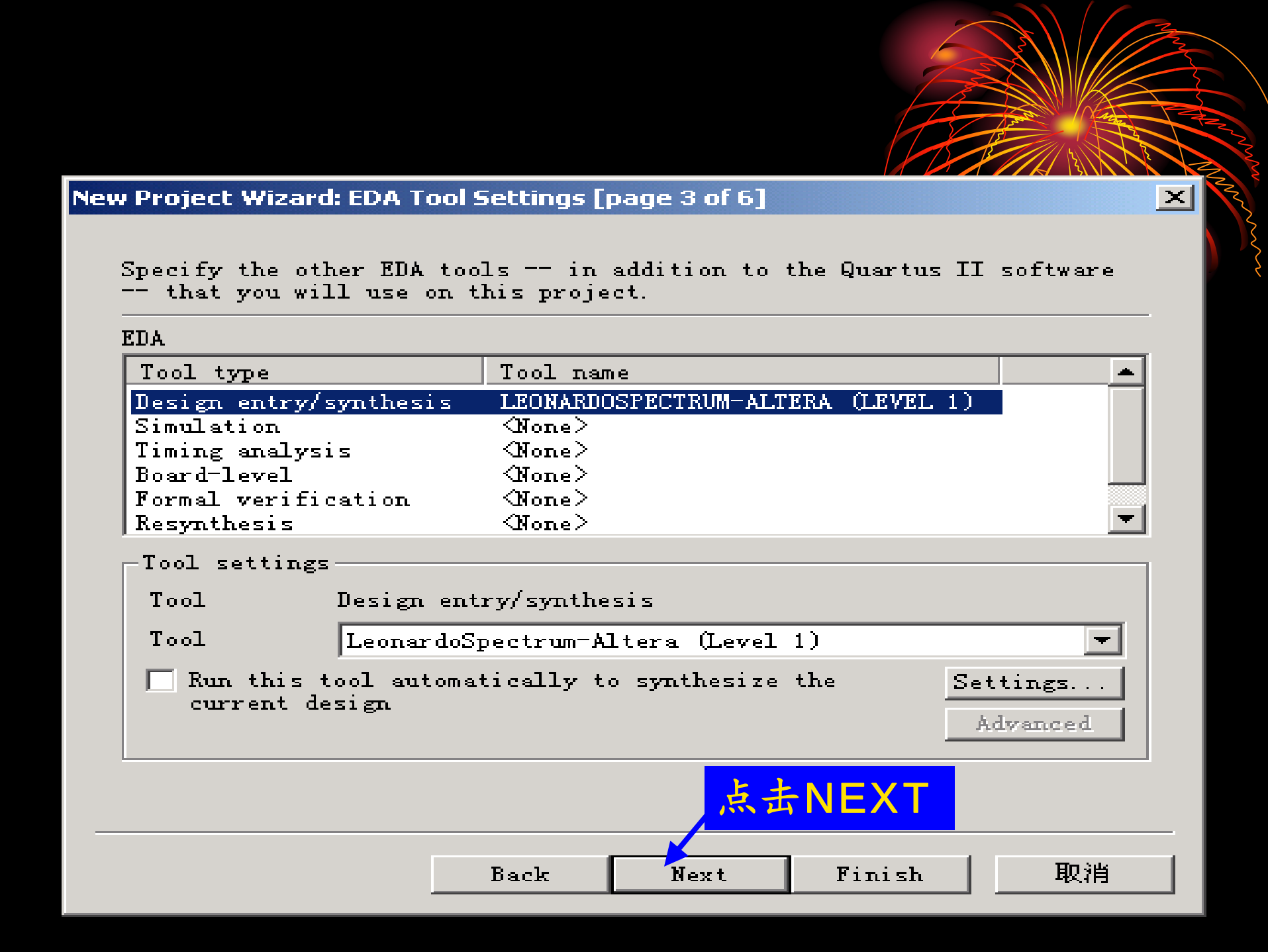
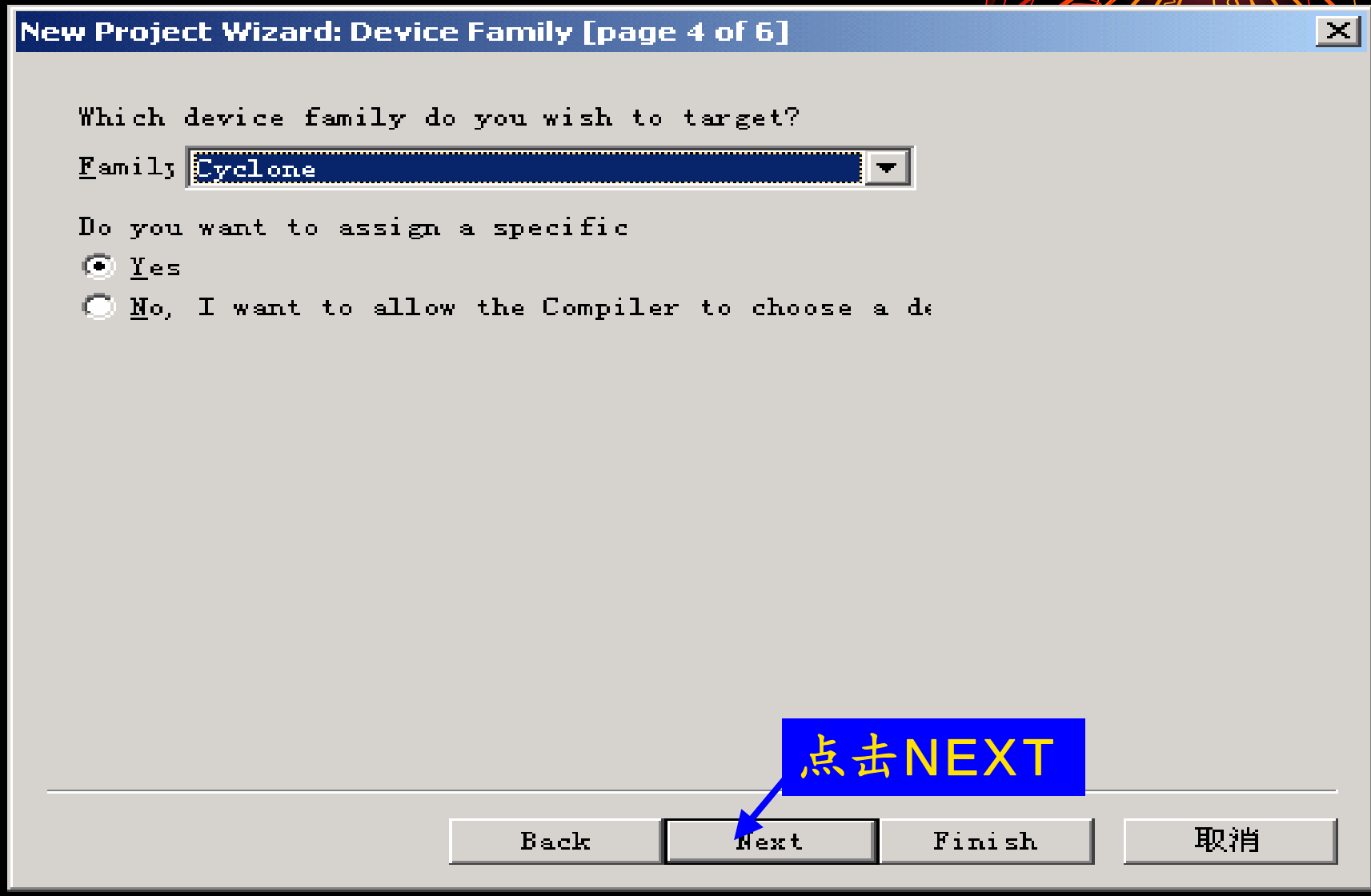
QUARTUS II使用说明

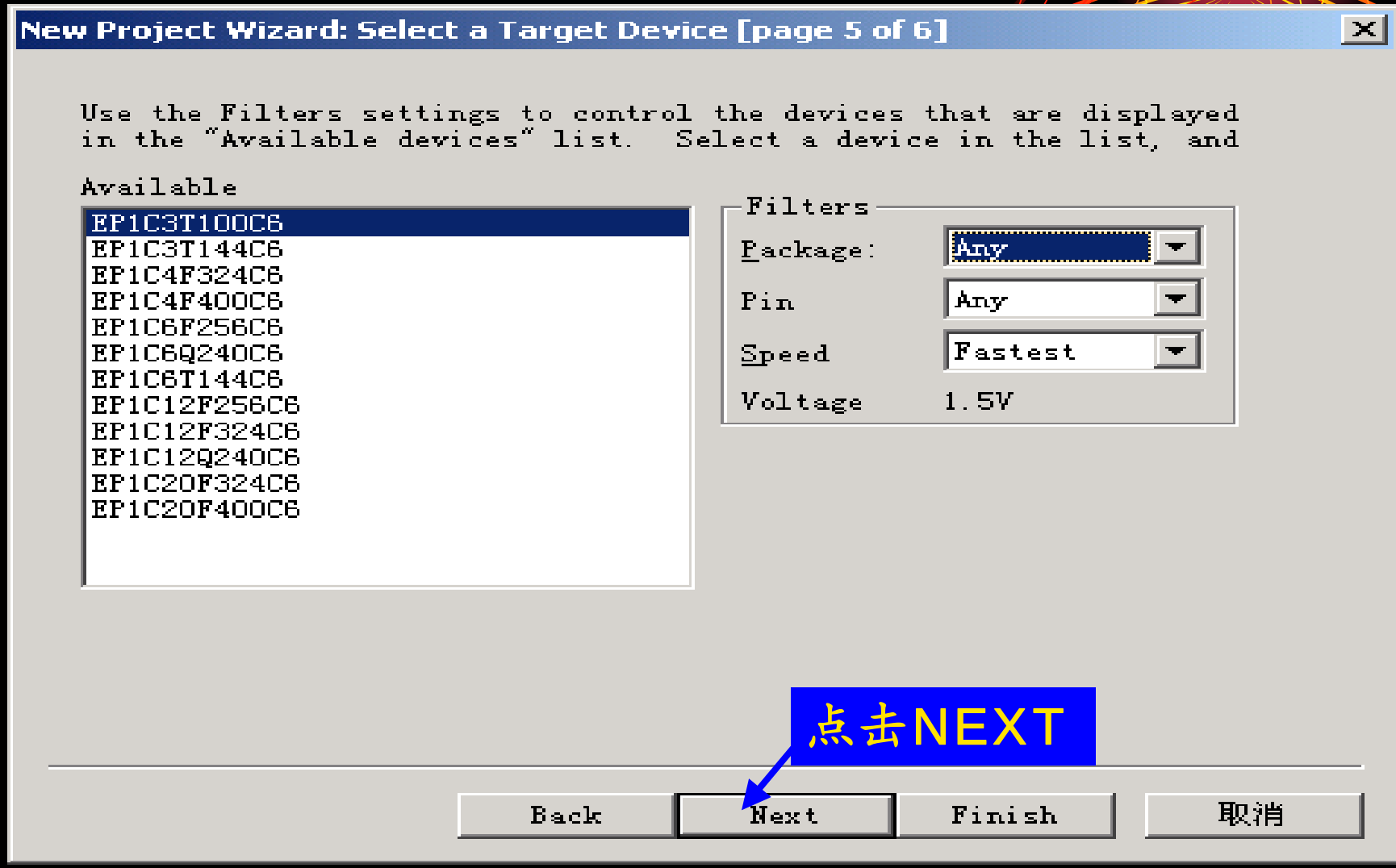

Quartus II - d:/fpga/cnt2/dec/dec - dec
File Edit View Project Assignments Processing Tools Window Help
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Convert MAX+PLUS II Project...
Save Project
Close Project
Save Ctrl+S
Save As...
Save Current Report Section As...
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
创建一个新的工程

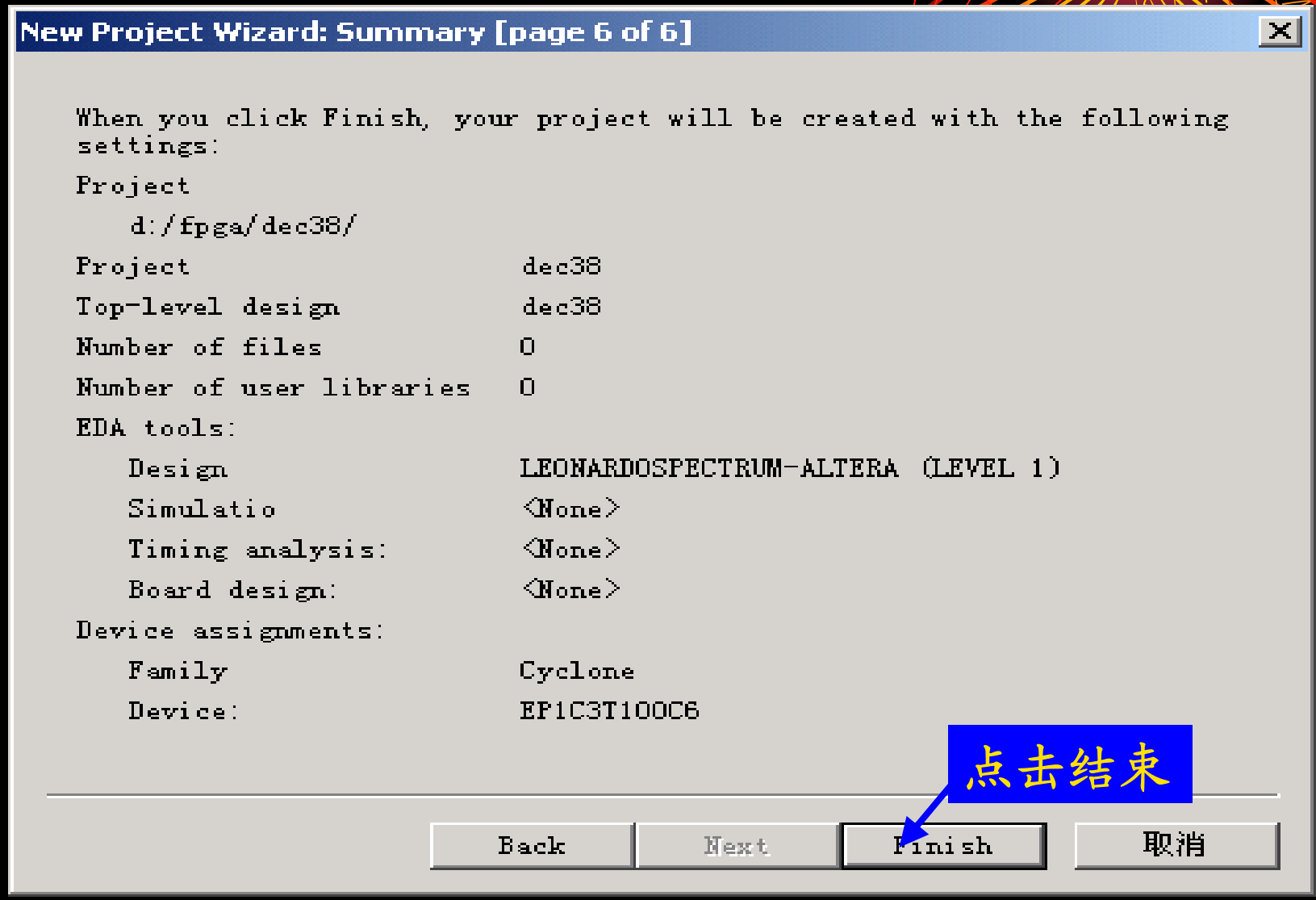

New Project Wizard: Directory, Name, and Top-Level Entity [page 1 of 6]
输入工程路径
What is the work
? This directory will
contain design f
ssociated with this
project. If you type a directory name that does not exist, Quartus II
d:/fpga/dec38
...
What is the name of this project? If you wish, you can use the name of
the project's top-level entity.
dec38
...
输入工程名和实体名，必须一样
What is the
your project? Entity names
are case sens
ust exactly match that of
dec38
...
Back
Next
Finish
取消

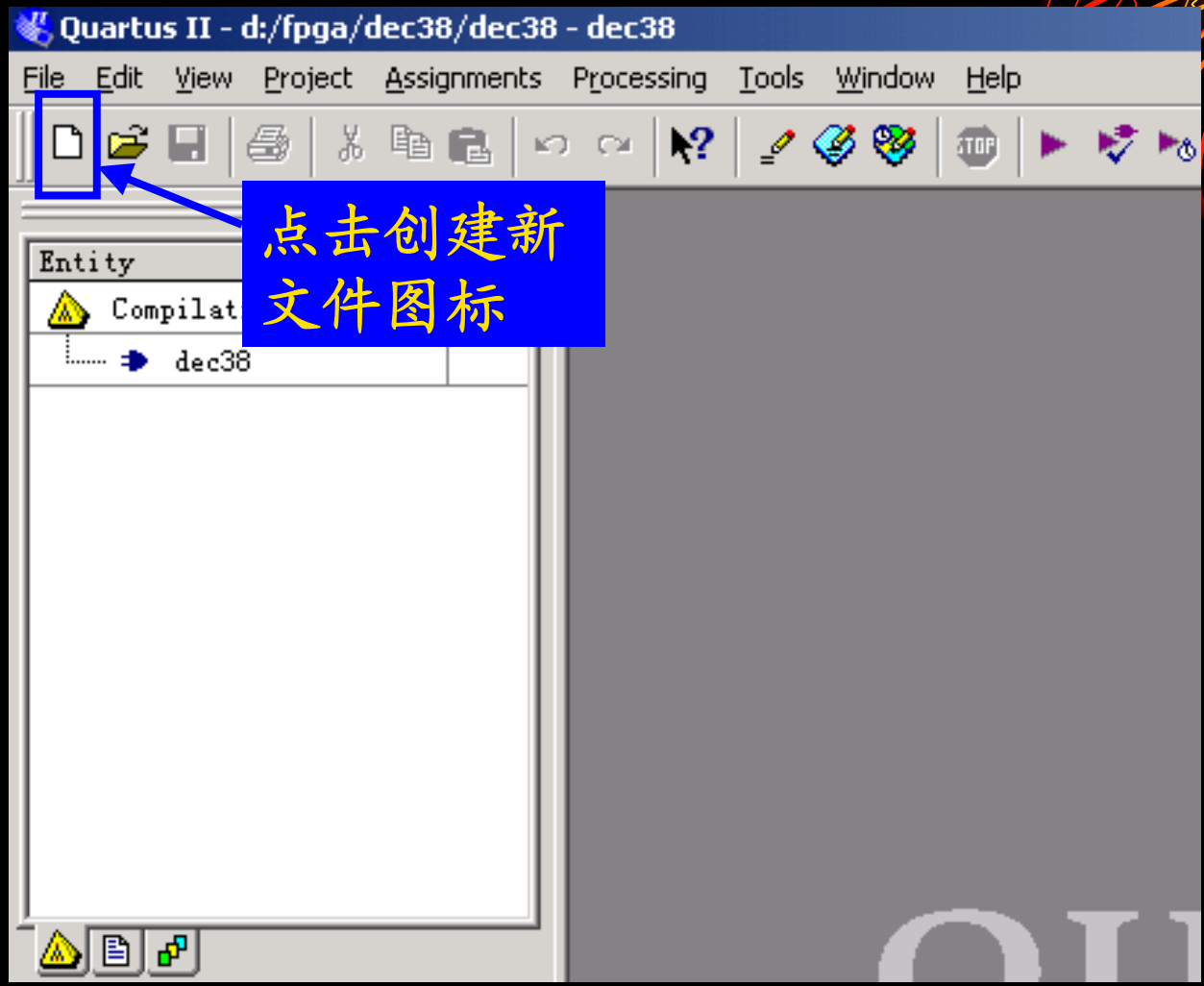

New Project Wizard: Add Files [page 2 of 6]
Select the design files and software source files you want to include in your project. Click Add All to add all design files and software Note: it is optional to add files here unless you have design files not contained in the project directory, or files in which the file name is
File name
Type
Add...
Add All
Remove
Properties
Up
Down
If your project includes libraries of custom functions, specify their pathnames:
User Library Pathnames
点击NEXT
Back
Next
Finish
取消

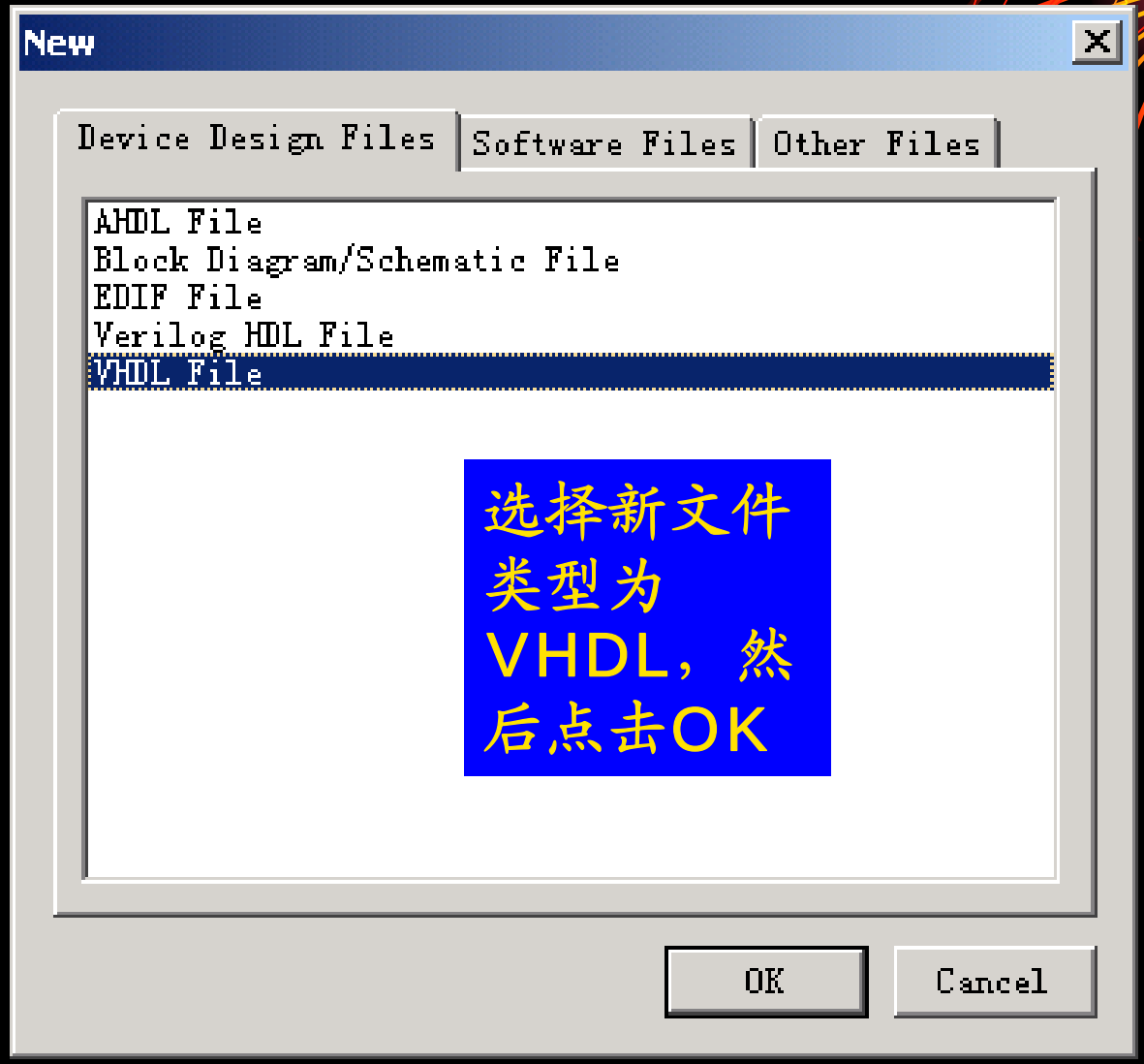

New Project Wizard: EDA Tool Settings [page 3 of 6]
Specify the other EDA tools -- in addition to the Quartus II software -- that you will use on this project.
EDA
Tool type
Tool name
Design entry/synthesis
LEONARDOSPECTRUM-ALTERA (LEVEL 1)
Simulation
<None>
Timing analysis
<None>
Board-level
<None>
Formal verification
<None>
Resynthesis
<None>
Tool settings
Tool
Design entry/synthesis
Tool
LeonardoSpectrum-Altera (Level 1)
Run this tool automatically to synthesize the current design
Settings...
Advanced
点击NEXT
Back
Next
Finish
取消

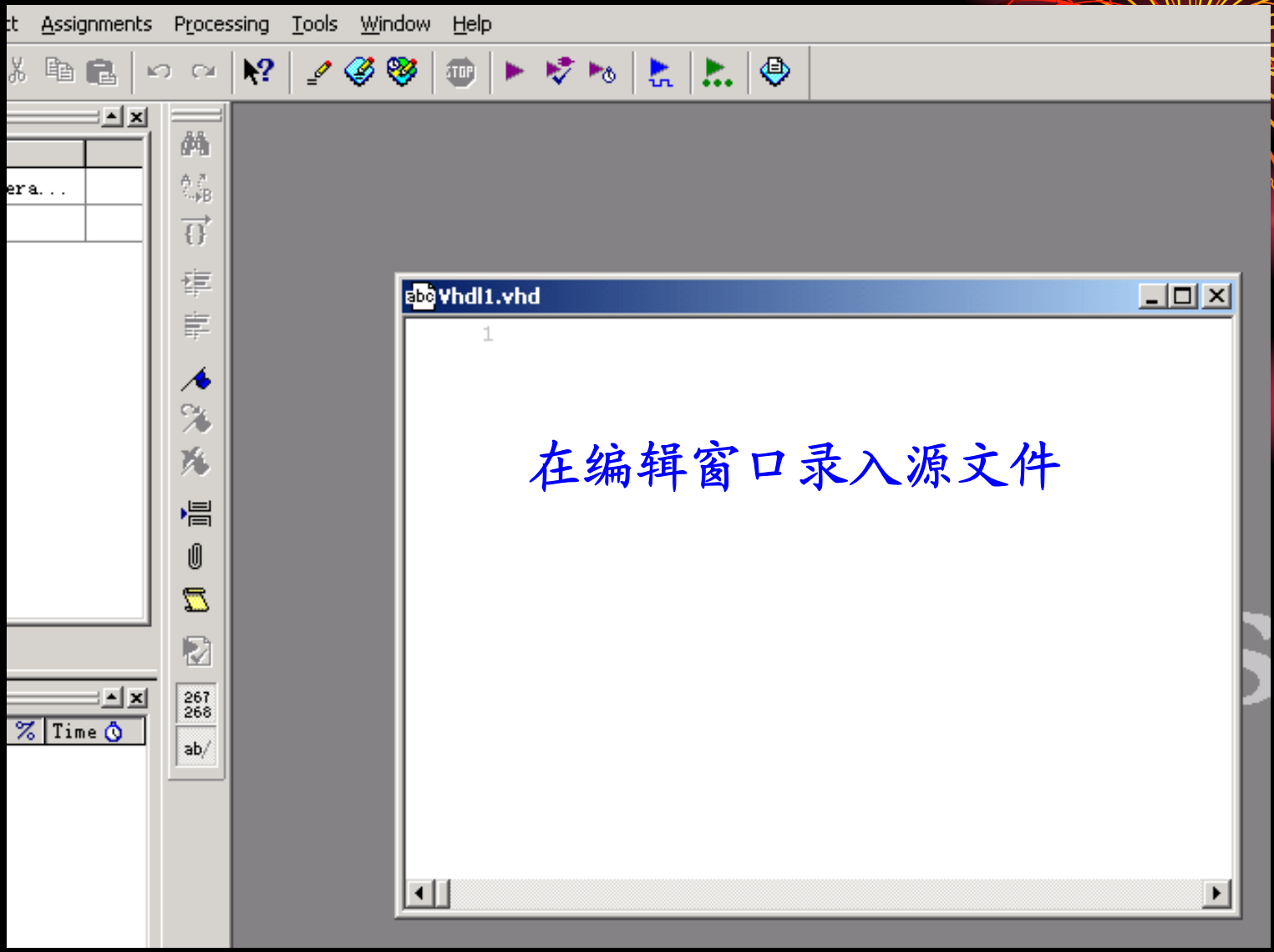

New Project Wizard: Device Family [page 4 of 6]
Which device family do you wish to target?
Family
Cyclone
Do you want to assign a specific
Yes
No, I want to allow the Compiler to choose a d
点击NEXT
Back
Next
Finish
取消

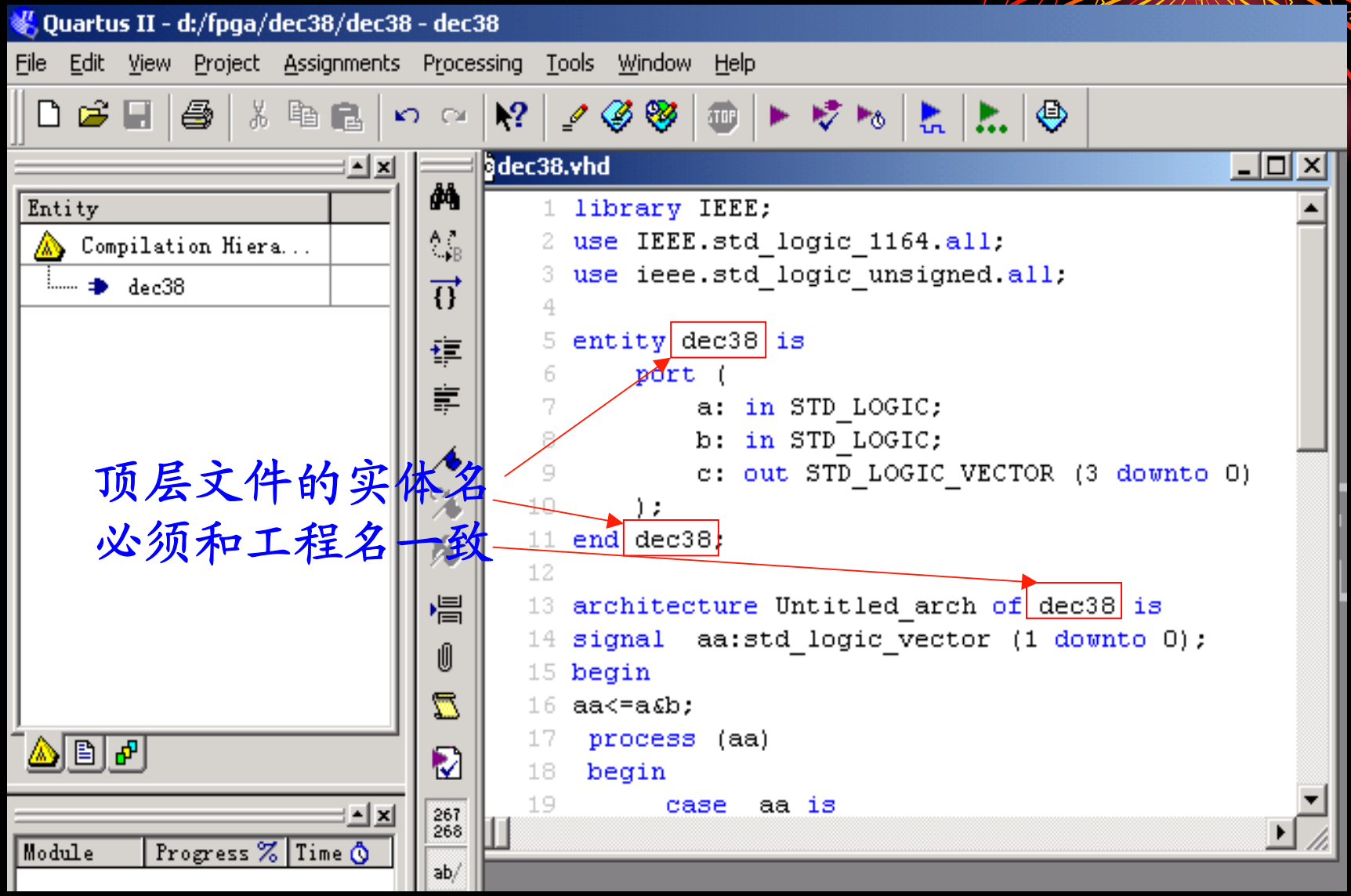

New Project Wizard: Select a Target Device [page 5 of 6]
Use the Filters settings to control the devices that are displayed in the "Available devices" list. Select a device in the list, and
Available
EP1C3T100C6
EP1C3T144C6
EP1C4F324C6
EP1C4F400C6
EP1C6F256C6
EP1C6Q240C6
EP1C6T144C6
EP1C12F256C6
EP1C12F324C6
EP1C12Q240C6
EP1C20F324C6
EP1C20F400C6
Filters
Package:
Any
Pin
Any
Speed
Fastest
Voltage
1.5V
点击NEXT
Back
Next
Finish
取消

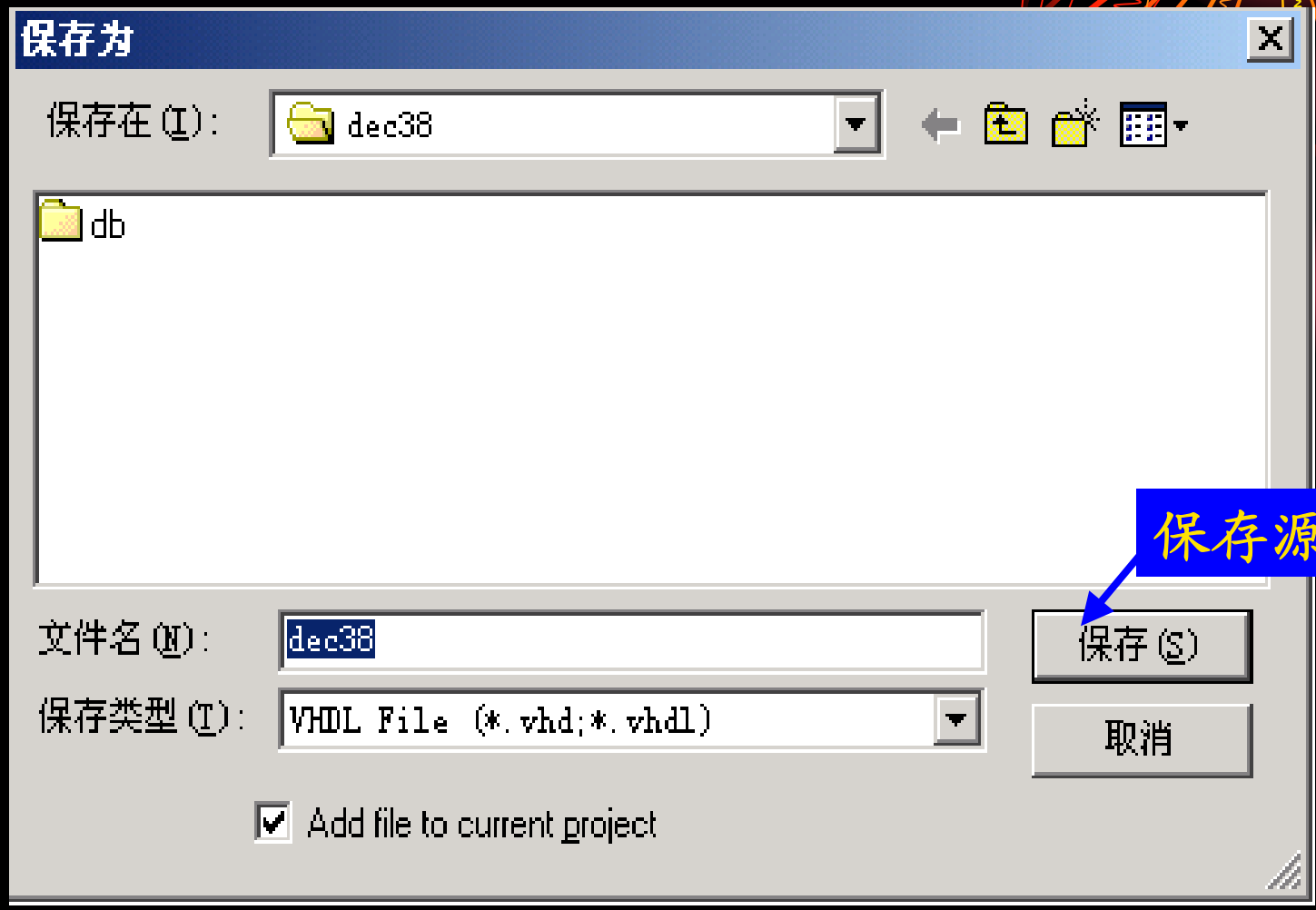

New Project Wizard: Summary [page 6 of 6]
When you click Finish, your project will be created with the following settings:
Project
d:/fpga/dec38/
Project dec38
Top-level design dec38
Number of files 0
Number of user libraries 0
EDA tools:
Design LEONARDOSPECTRUM-ALTERA (LEVEL 1)
Simulatio <None>
Timing analysis: <None>
Board design: <None>
Device assignments:
Family Cyclone
Device: EP1C3T100C6
点击结束
Back
Next
Finish
取消

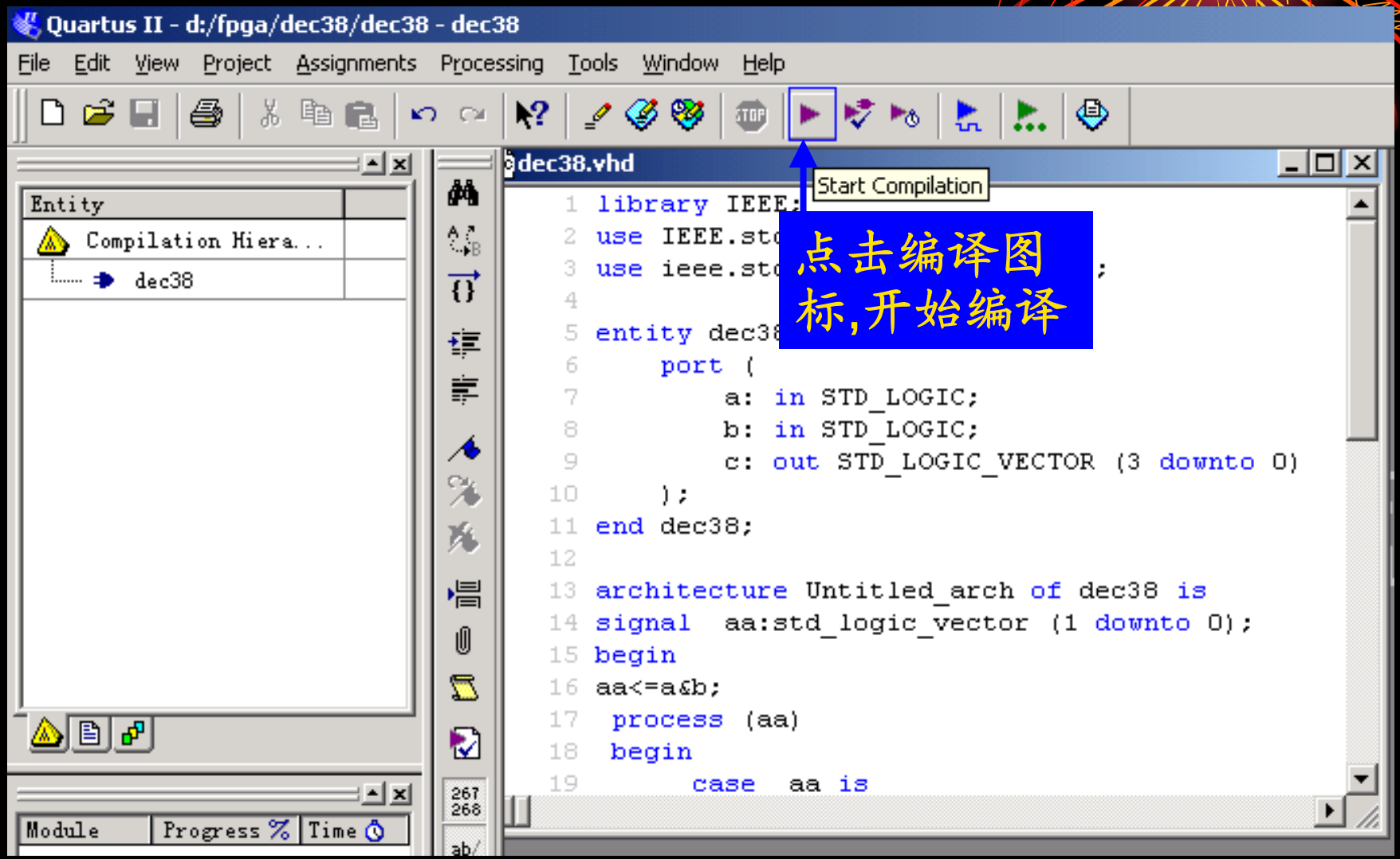

Quartus II - d:/fpga/dec38/dec38 - dec38
File Edit View Project Assignments Processing Tools Window Help
点击创建新文件图标
Entity
Compilat
dec38


New
Device Design Files
Software Files
Other Files
AHDL File
Block Diagram/Schematic File
EDIF File
Verilog HDL File
VHDL File
选择新文件类型为VHDL，然后点击OK
OK
Cancel

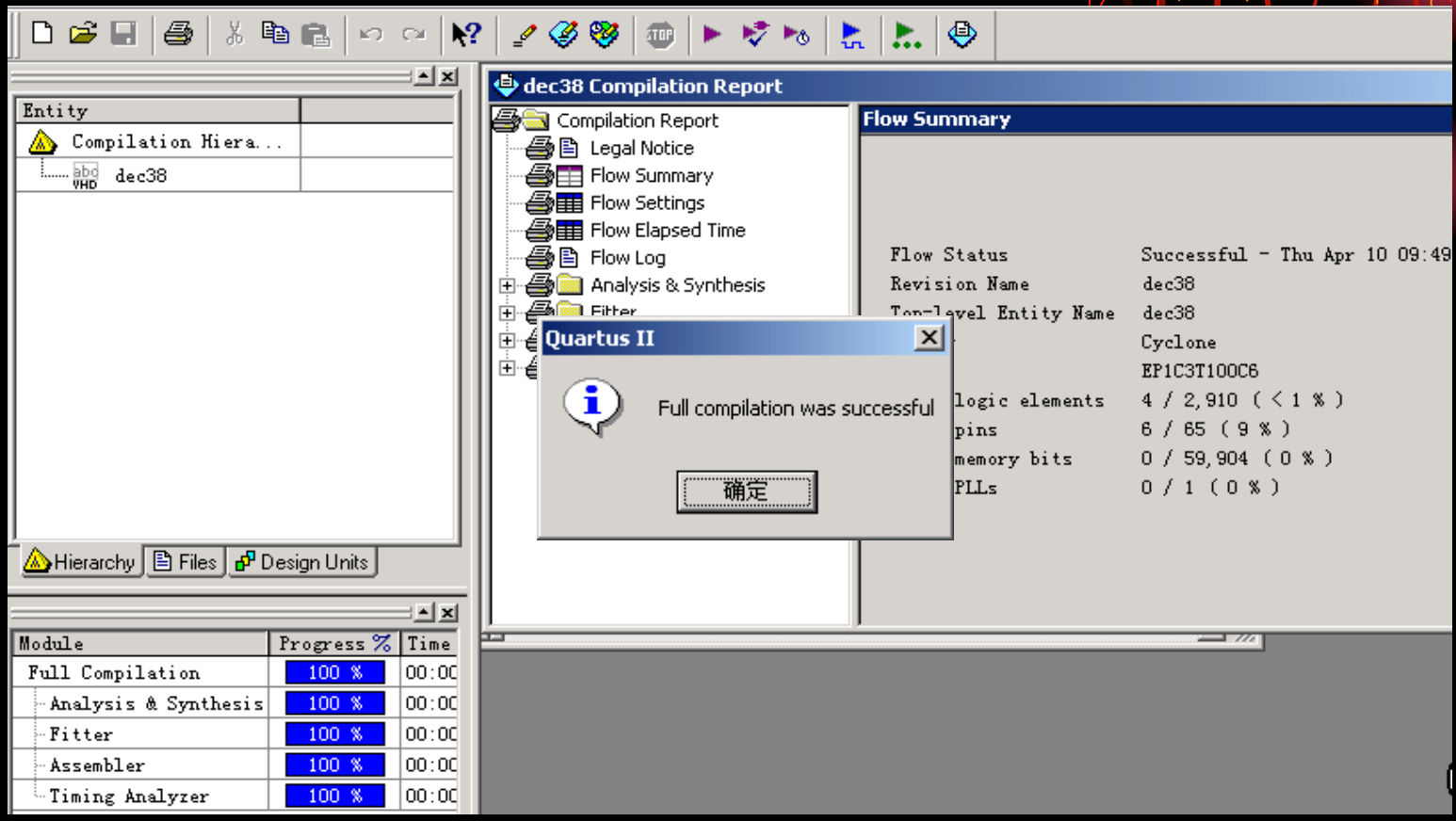

Assignments
Processing
Tools
Window
Help
Vhdl1.vhd
1
在编辑窗口录入源文件
Time


Quartus II - d:/fpga/dec38/dec38 - dec38
File Edit View Project Assignments Processing Tools Window Help
Entity
Compilation Hiera...
dec38
Module Progress % Time
dec38.vhd
1 library IEEE;
2 use IEEE.std_logic_1164.all;
3 use ieee.std_logic_unsigned.all;
4
5 entity dec38 is
6 port (
7 a: in STD_LOGIC;
8 b: in STD_LOGIC;
9 c: out STD_LOGIC_VECTOR (3 downto 0)
10);
11 end dec38;
12
13 architecture Untitled_arch of dec38 is
14 signal aa:std_logic_vector (1 downto 0);
15 begin
16 aa<=a&b;
17 process (aa)
18 begin
19 case aa is
顶层文件的实体名
必须和工程名一致

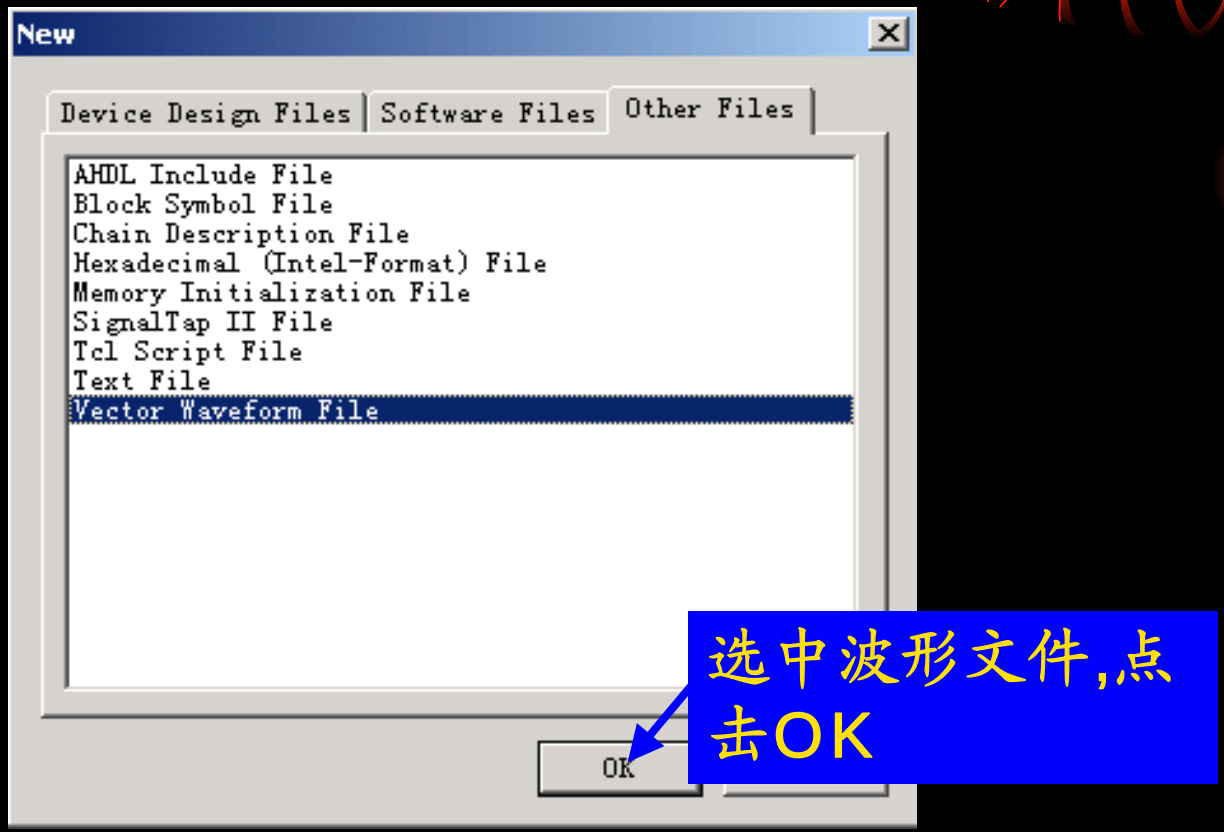

保存为
保存在(I):
dec38
db
文件名(N):
dec38
保存类型(T):
VHDL File (*.vhd;*.vhdl)
保存(S)
取消
Add file to current project
保存源文件


Quartus II - d:/fpga/dec38/dec38 - dec38
File Edit View Project Assignments Processing Tools Window Help
Start Compilation
点击编译图标,开始编译
dec38.vhd
Entity
Compilation Hiera...
dec38
Module
Progress
Time
1 library IEEE;
2 use IEEE.st
3 use ieee.st ;
4
5 entity dec3
6 port (
7 a: in STD_LOGIC;
8 b: in STD_LOGIC;
9 c: out STD_LOGIC_VECTOR (3 downto 0)
10);
11 end dec38;
12
13 architecture Untitled_arch of dec38 is
14 signal aa:std_logic_vector (1 downto 0);
15 begin
16 aa<=a&b;
17 process (aa)
18 begin
19 case aa is

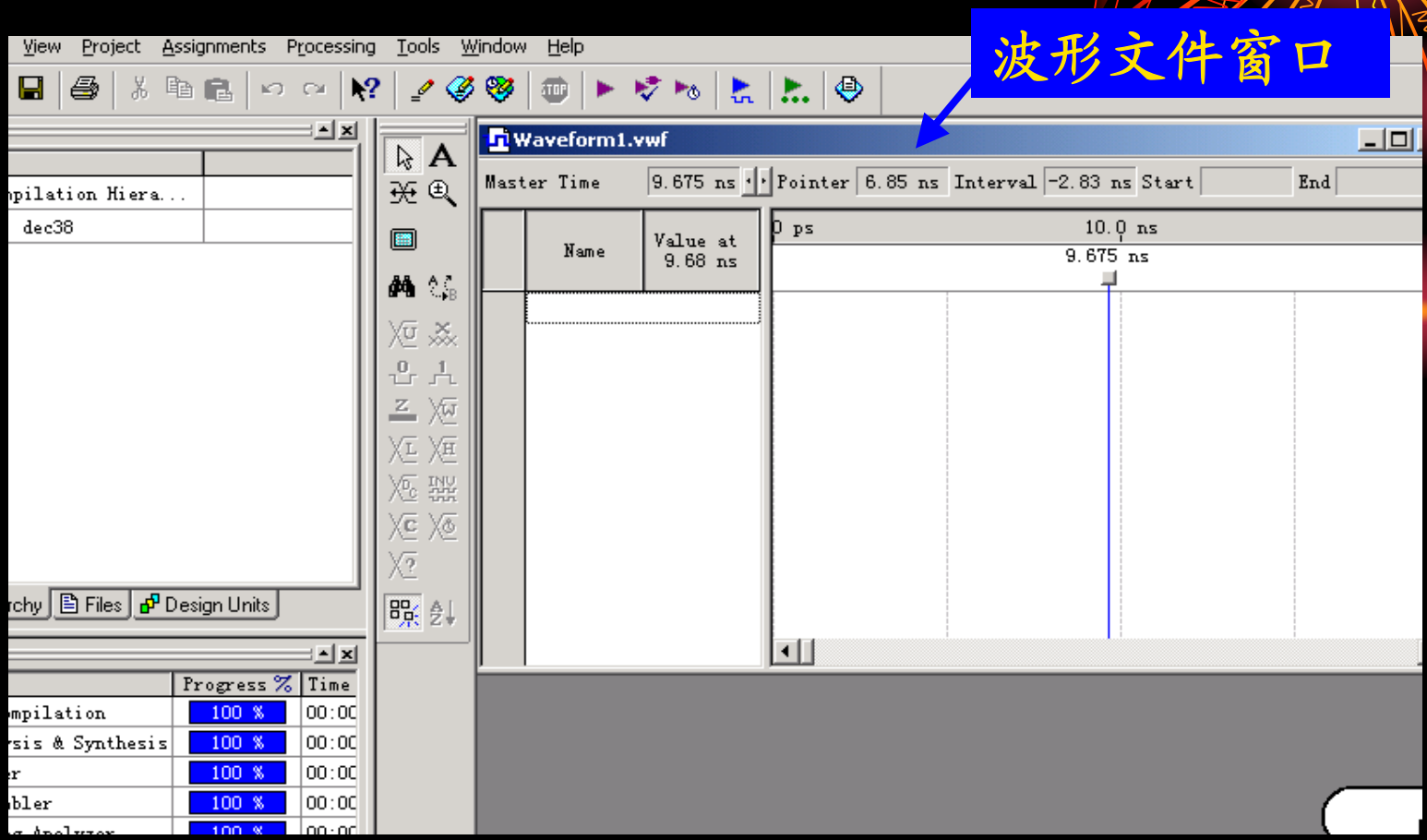
在编译过程中如果有错会给出错误提示,否则显示编译成功



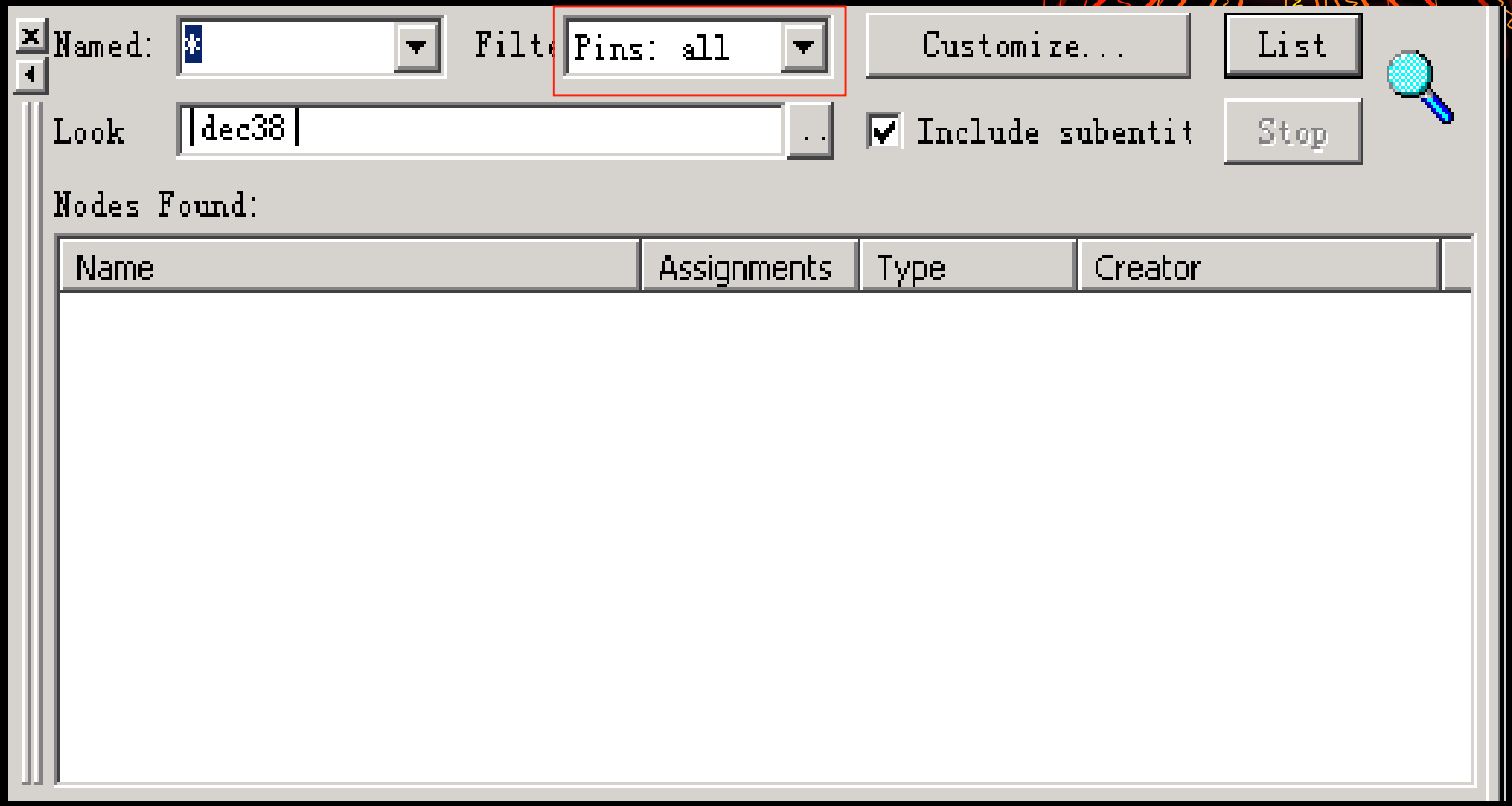
创建波形文件(还是创建一个新文件,并选择类型)



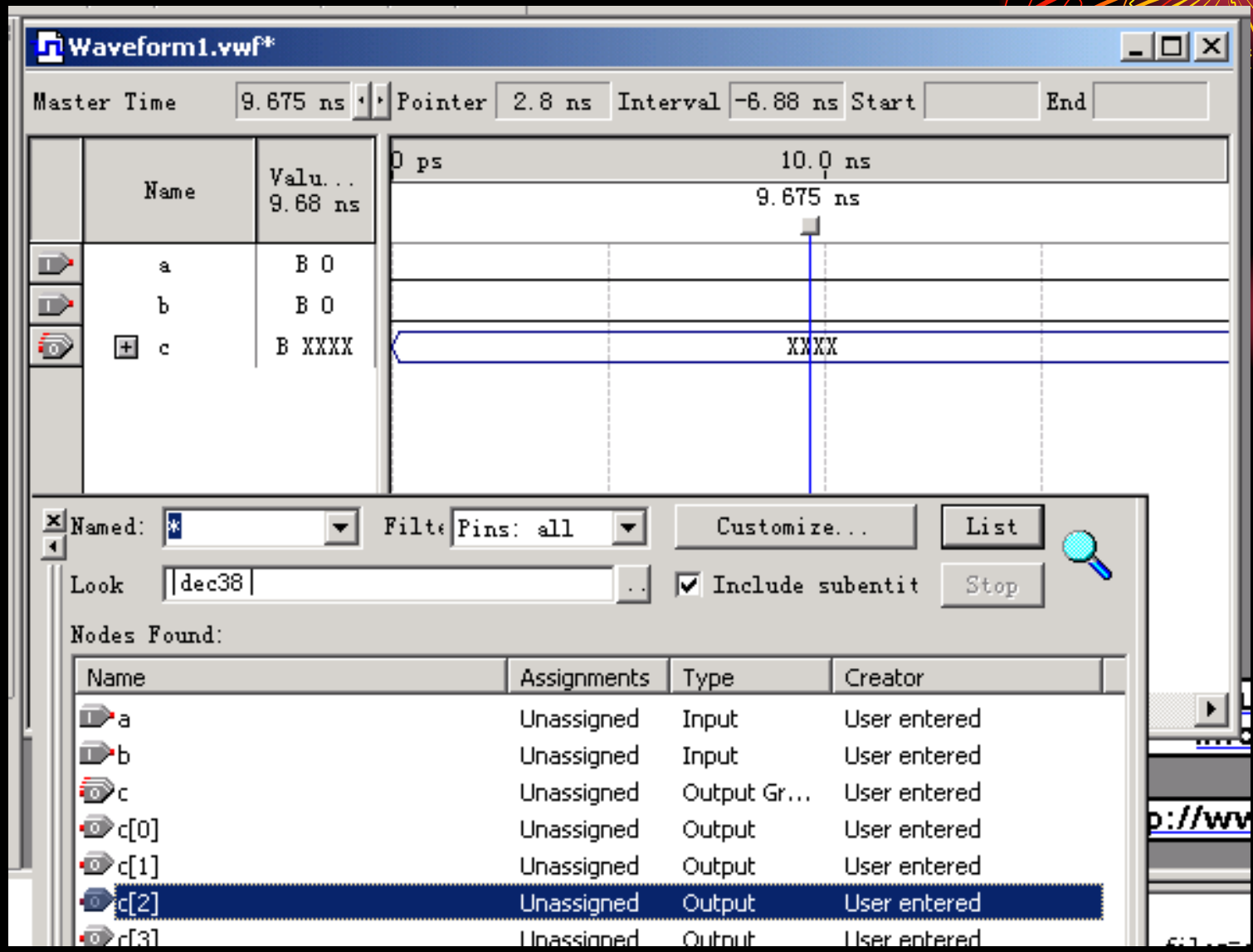
一个空的波形文件被建立

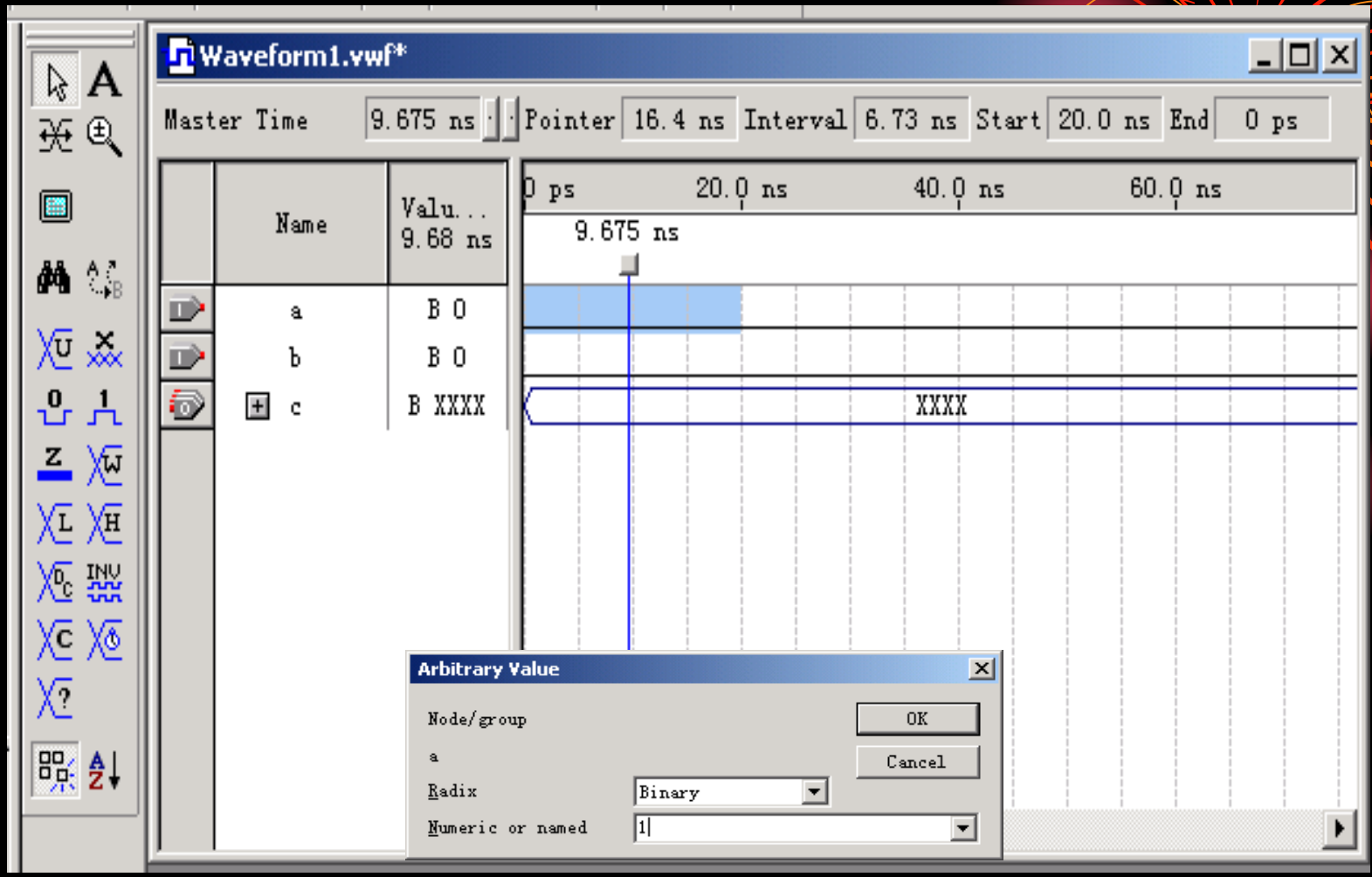


按快捷键Alt+1,弹出如下窗口,按图中所示设置好后,点击List.所有端口信号会被列出来.

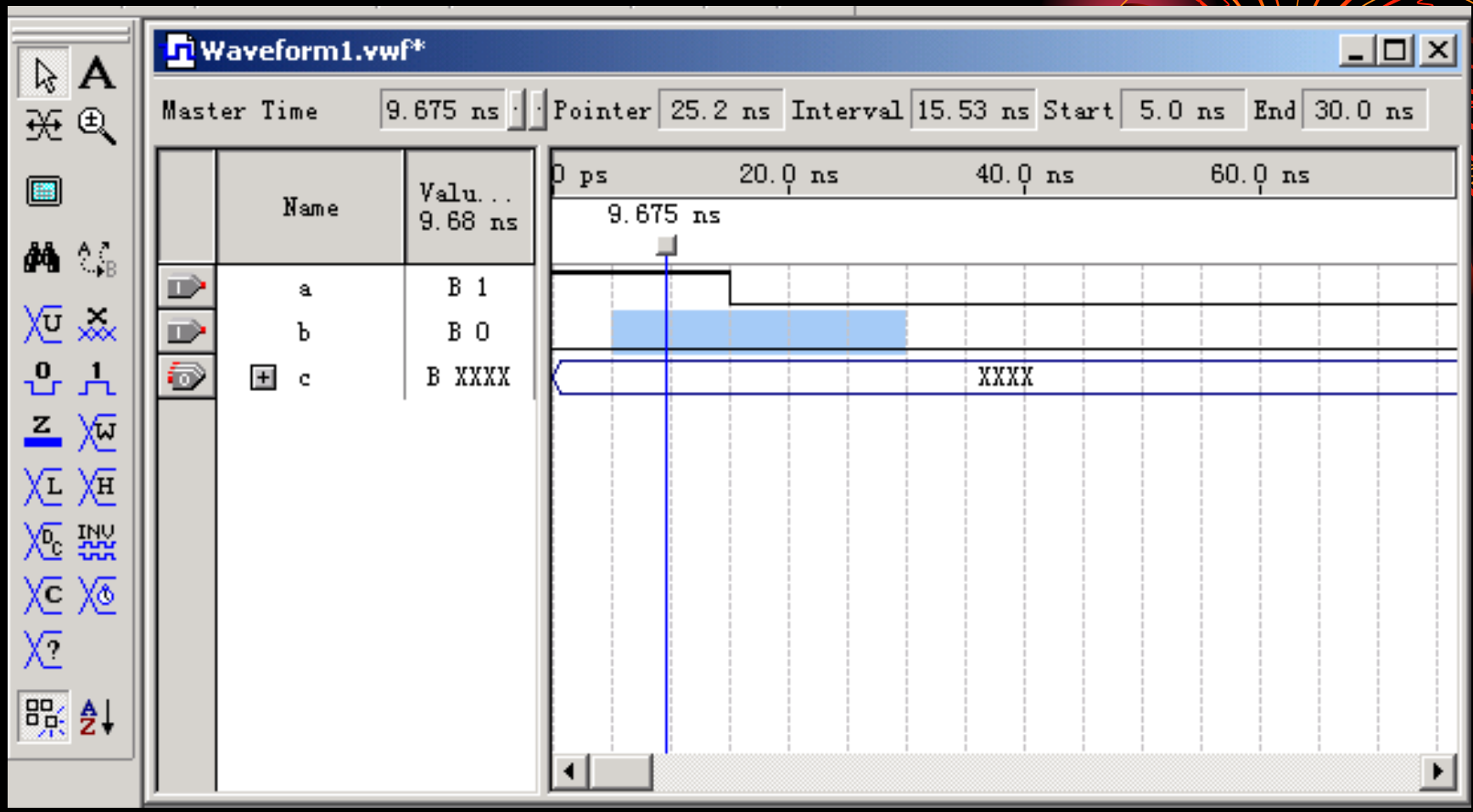


如图，将输入输出信号拖动到波形文件窗口

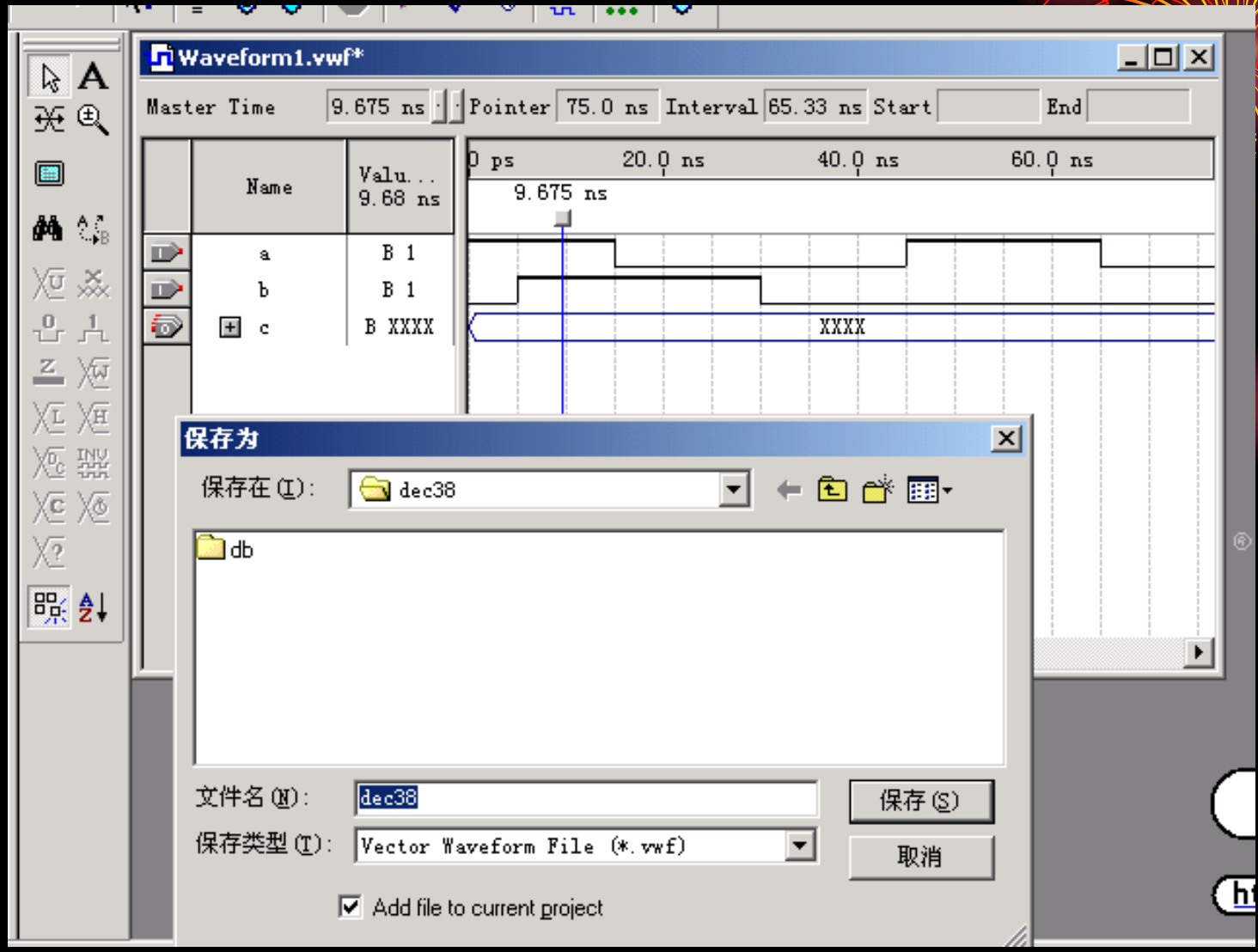




给输入信号添加激励。如图按住鼠标左键不放，拖动一定距离，再将鼠标放在图中的浅兰色区域双击左键，这时会弹出一个窗口，在该窗口中输入波形值（位数据输入0或1，位矢量输二进制序列）并点击ok。

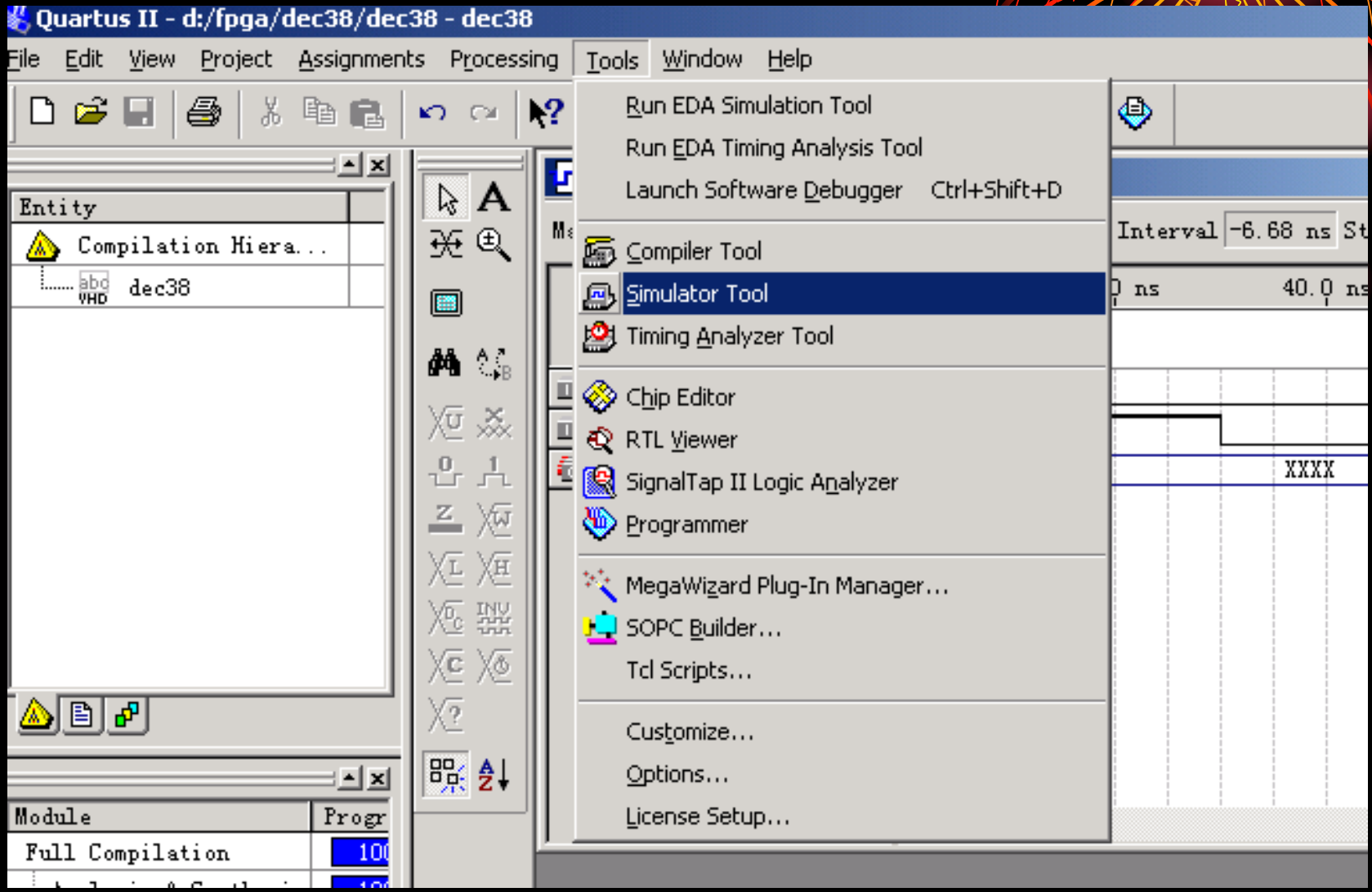


这时就给A端口加上了一段高电平，依此方法给所有的输入都加上指定激励。



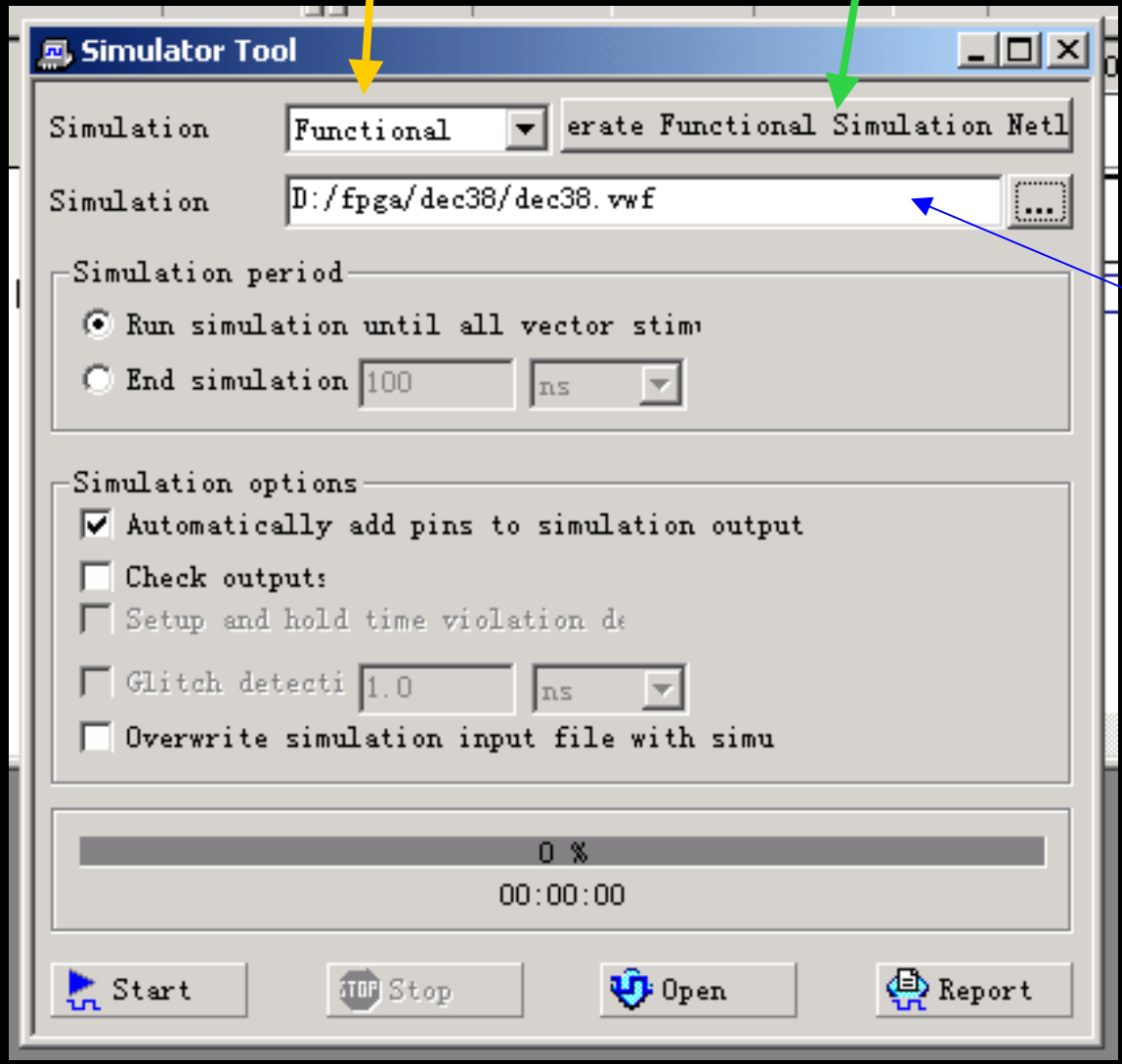
将输入的激励都加上以后，保存该波形文件

在菜单中选择Tools->Simulator Tool



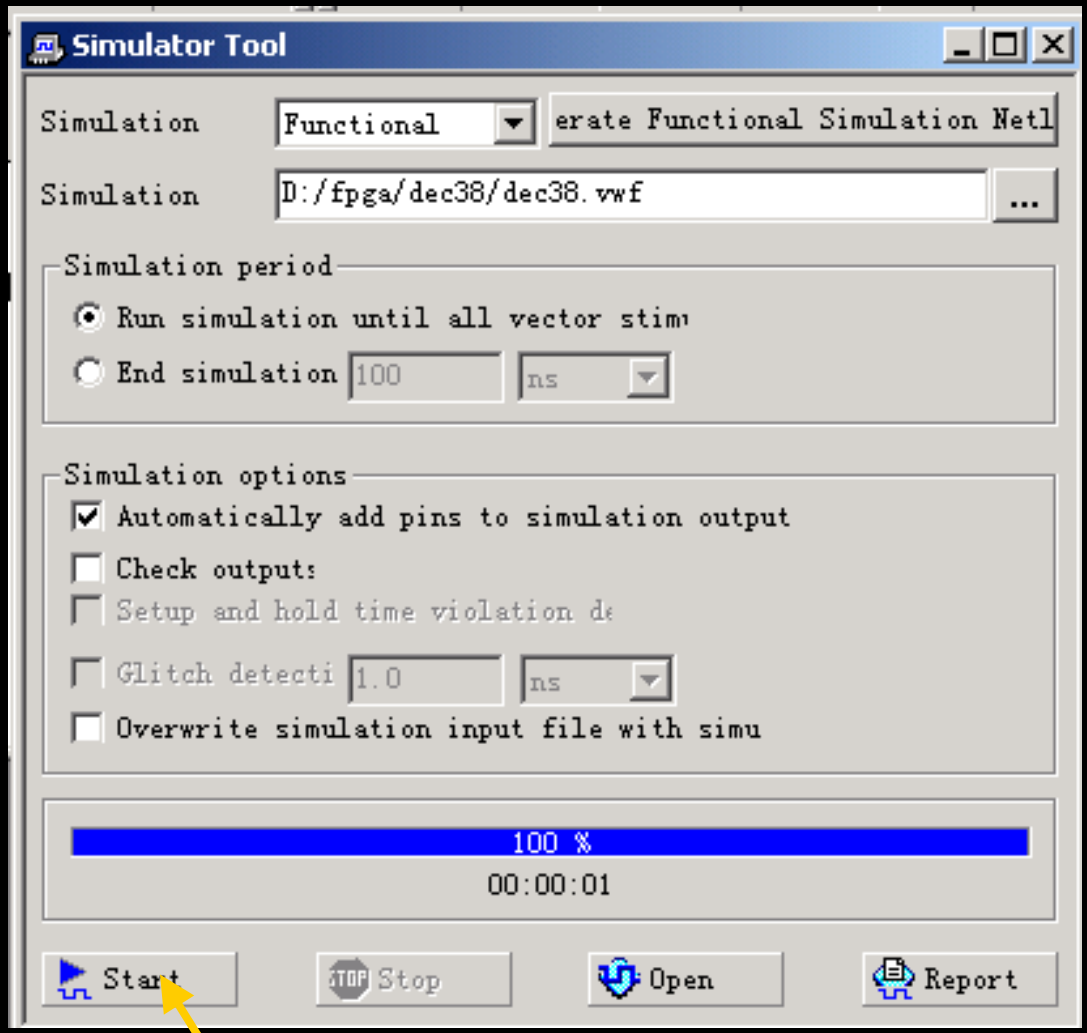
选择仿真类型(Functional),并创建功能仿真网表(点击绿色荐头所指按钮)

功能仿真



此处应为刚才保存的波形文件

功能仿真

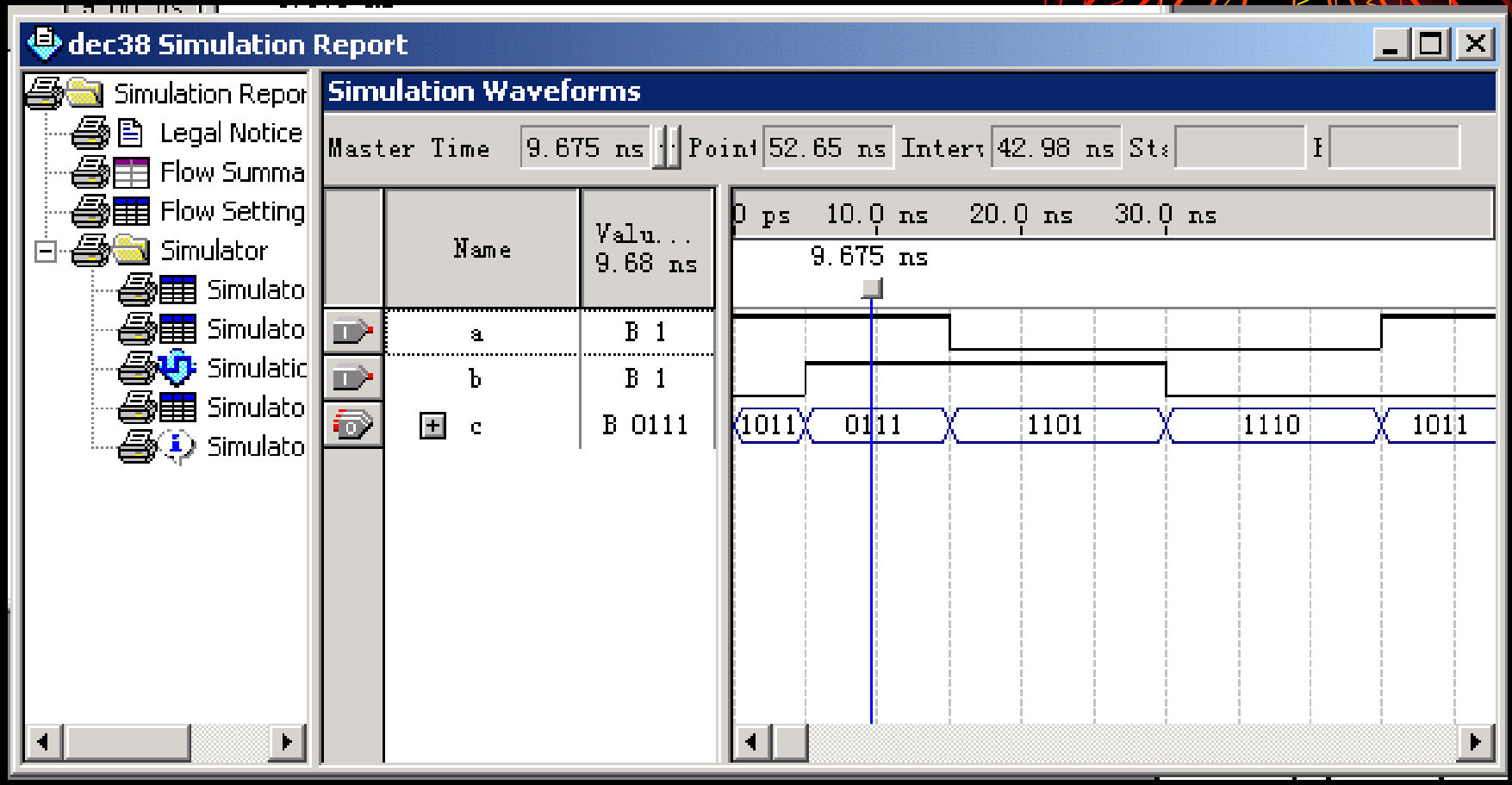


网表创建完后点击Start运行,运行完成后关闭此窗口.

功能仿真

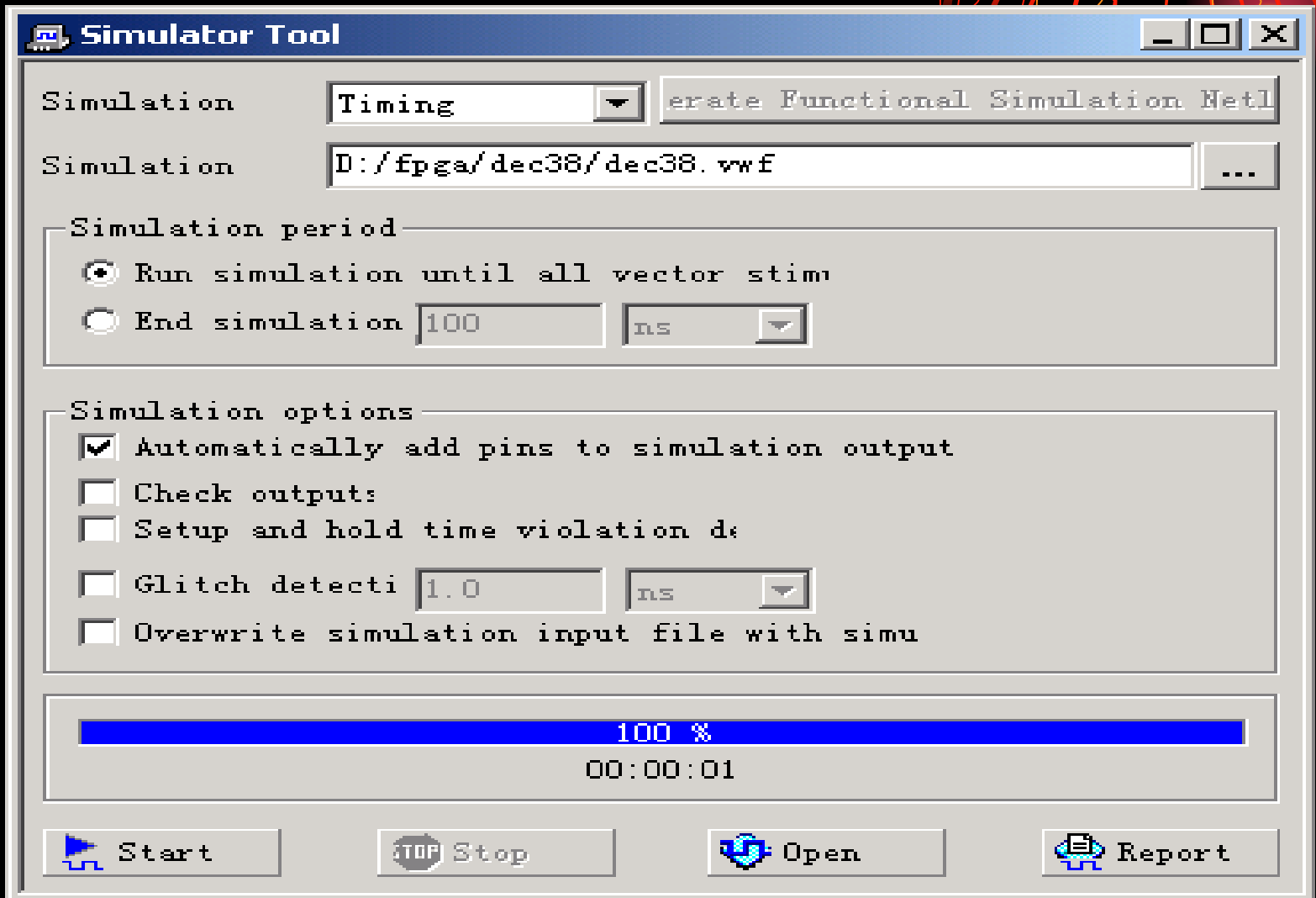
点击此处，开始仿真

运行结束后会弹出功能仿真的波形报告,观察仿真波形并验证



在菜单中选择Tools->Simulator Tool弹出下面的窗口，改变仿真类型(选Timing)，点击Start运行.运行结束后，关闭该窗口.

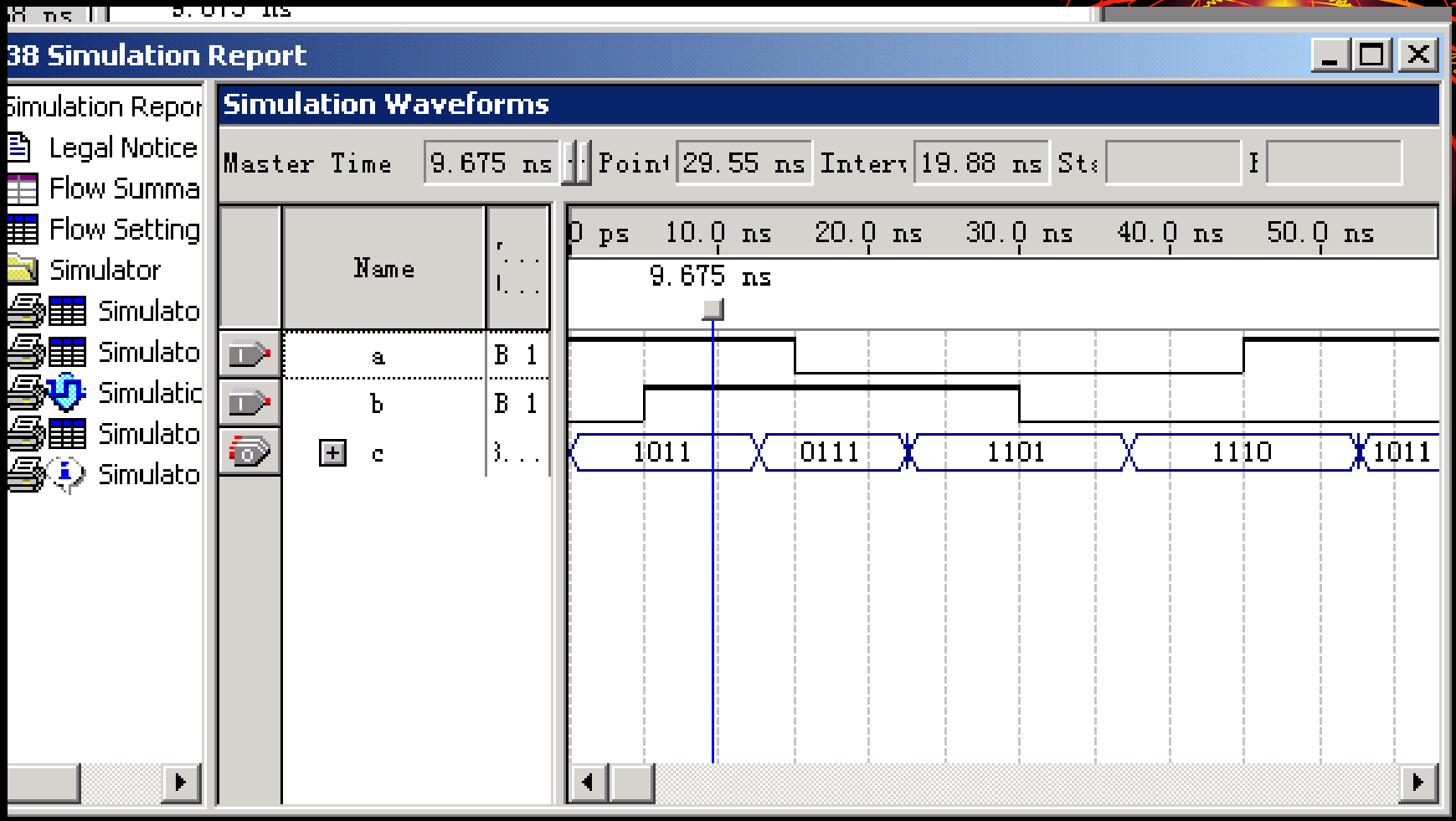
时序仿真



时序仿真

点击此处，开始时序仿真

得到时序仿真波形.



比较时序仿真的波形和功能仿真波形有什么不同