Early Power Estimator

Altera Asia Pacific Regional Support Center

Agenda

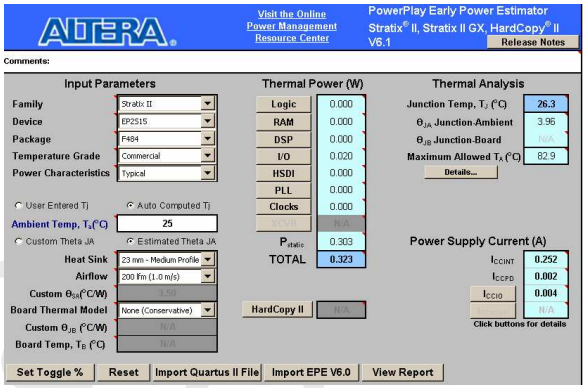
- Overview
- Setup
- Using the EPE
- Lab

Overview

Inputs

User Entry
Or Import Data
from Quartus II

Early Power Estimator



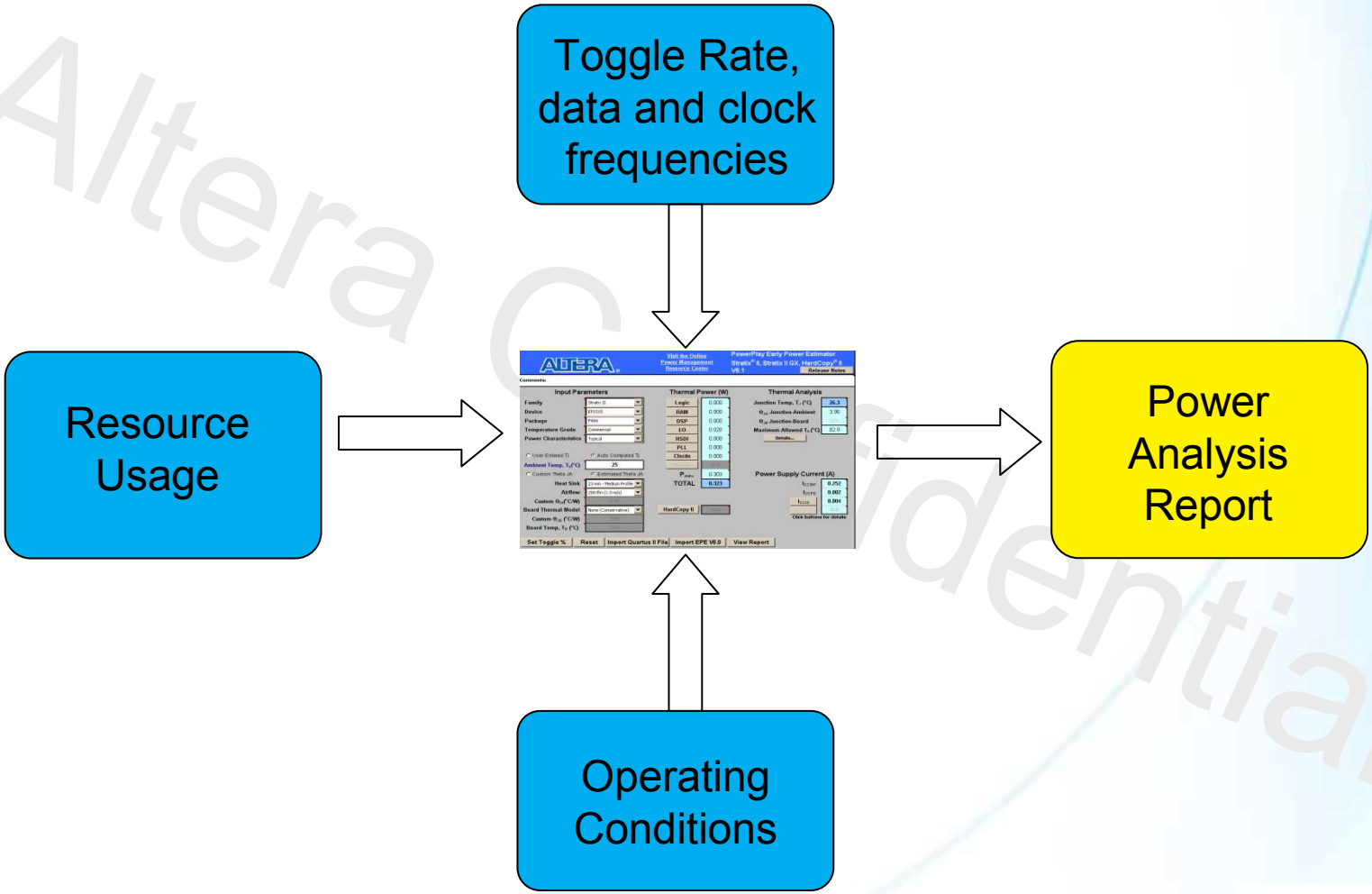
Reports

- Block Power
- Supply Power
- Thermal Analysis

- Accounts for device complexities, including temperature
- Allows quick, efficient “What-If” analysis
- Functional vectors not required
  - Accuracy will be affected, however
- Easily distributed as a spreadsheet

EPE Components

- Accurate FPGA power estimation require 3 components:



EPE Setup

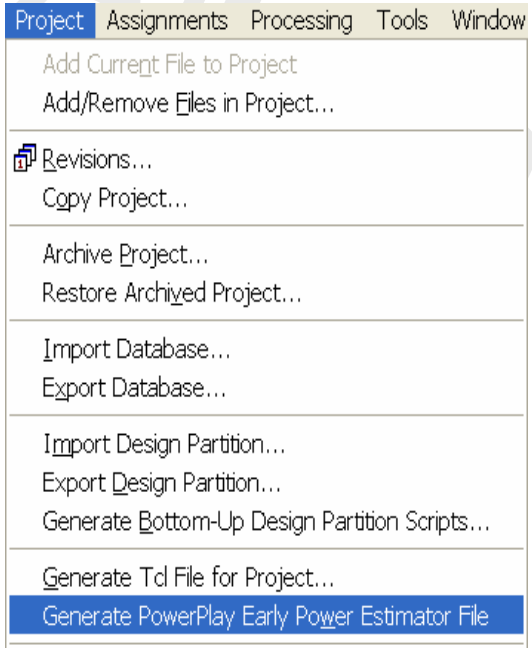
- System Requirements
  - Windows NT/2000/XP Operating System
  - Microsoft Excel 2002 or higher
- Download and Installation
  - Available from Altera web site www.altera.com

Entering Information Into EPE

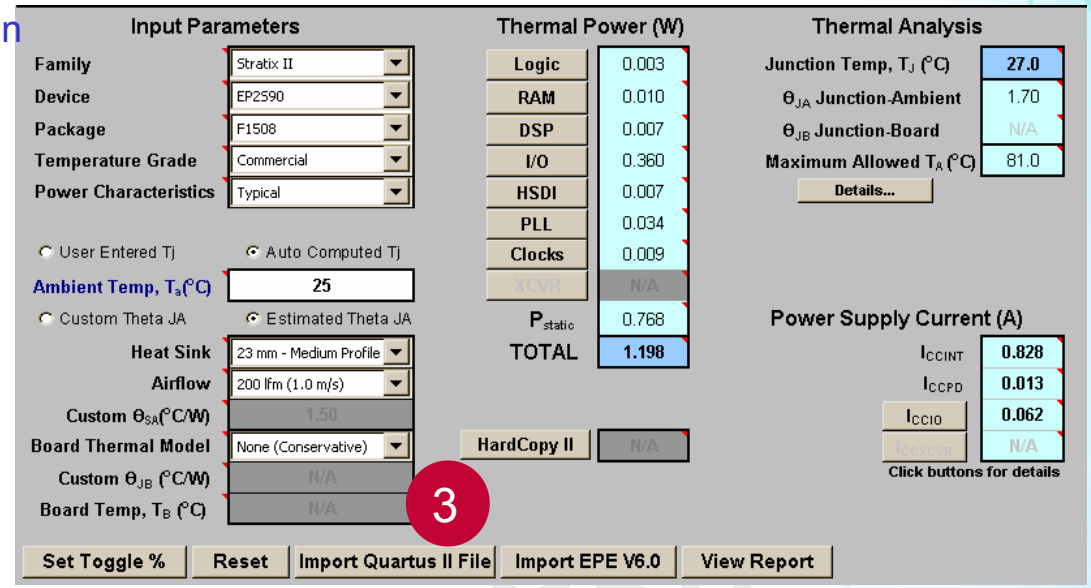
- Clearing All Values
  - Reset all EPE fields/values by clicking **Reset**
- Manually Entering Information
  - Enter values into input-designated cells (white, unshaded)
    - Other cells cannot be edited
  - Can specify module names per resource row
- Importing a Quartus II output .csv file
  - Generate .csv file from Quartus II
  - Launch the EPE Excel spreadsheet
  - Click “Import Quartus II File” button; follow directions

Importing Quartus II Output .csv File

1 Generate .CSV file for your design
design-name_early_pwr.csv



2 Launch the excel spreadsheet
Import design-name_early_pwr.csv

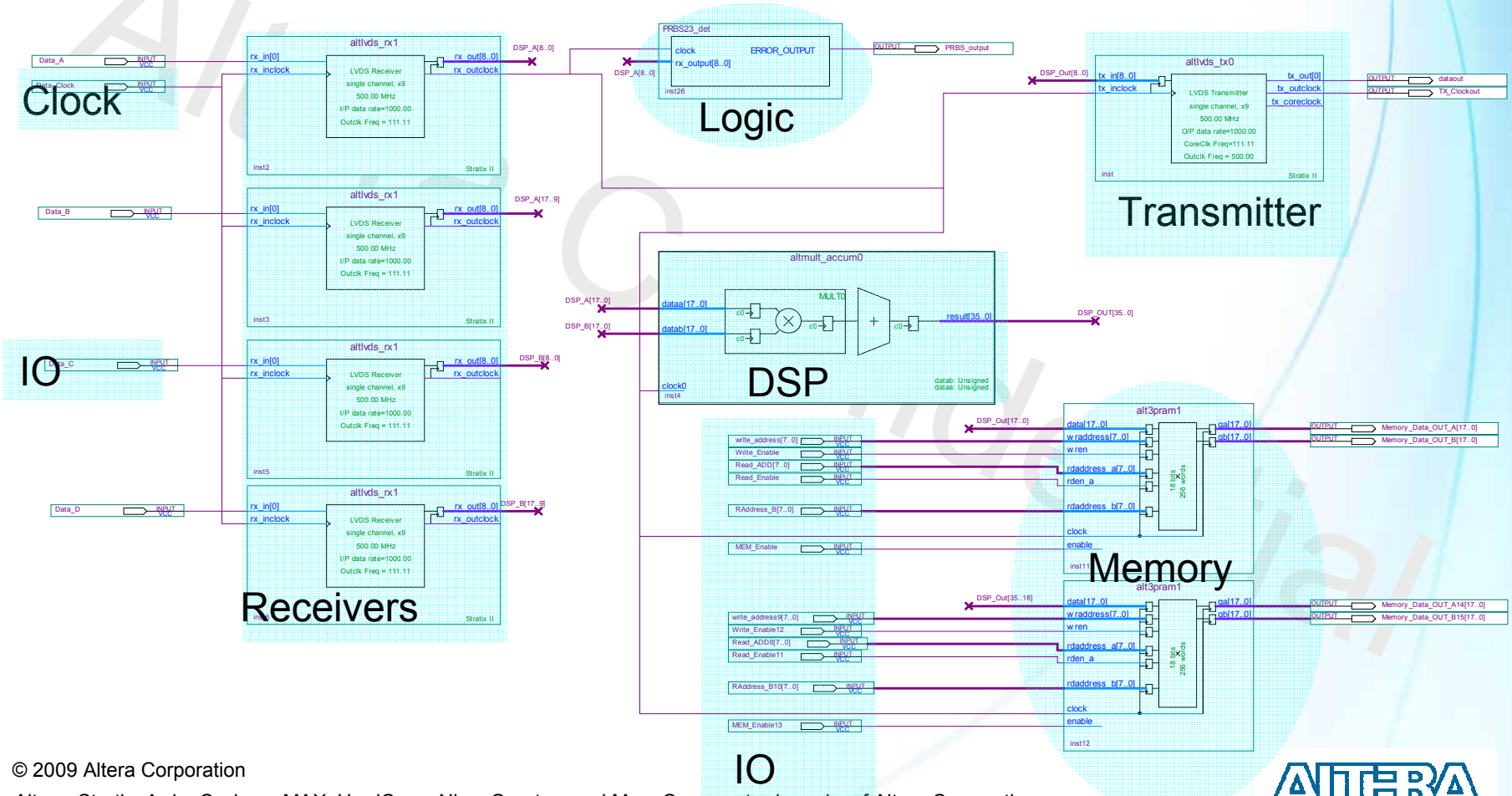


Using the EPE

- Device-related Input Parameters
  - Family
  - Device
  - Package
  - Temperature grade
  - Power Characteristics
- Thermal Input Parameters
  - Ambient (or junction) temperature
  - Heat sink used?
  - Airflow
  - Board thermal model
  - Board temperature

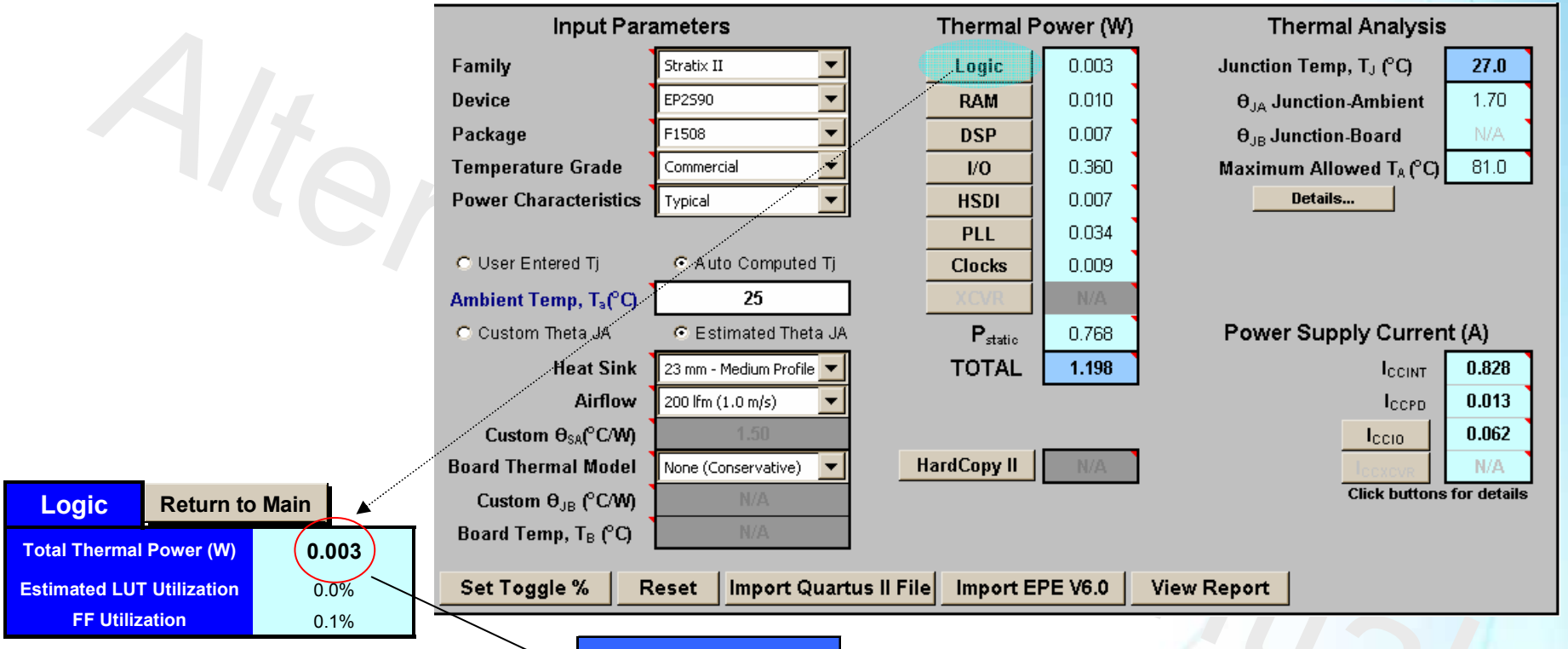
Generic Design

- Lab Design – Top Level Overview
  - What are the resource usage estimates for the design?
  - What are the clock frequencies, data rates, and toggle rates?



Using the Logic Resource Page

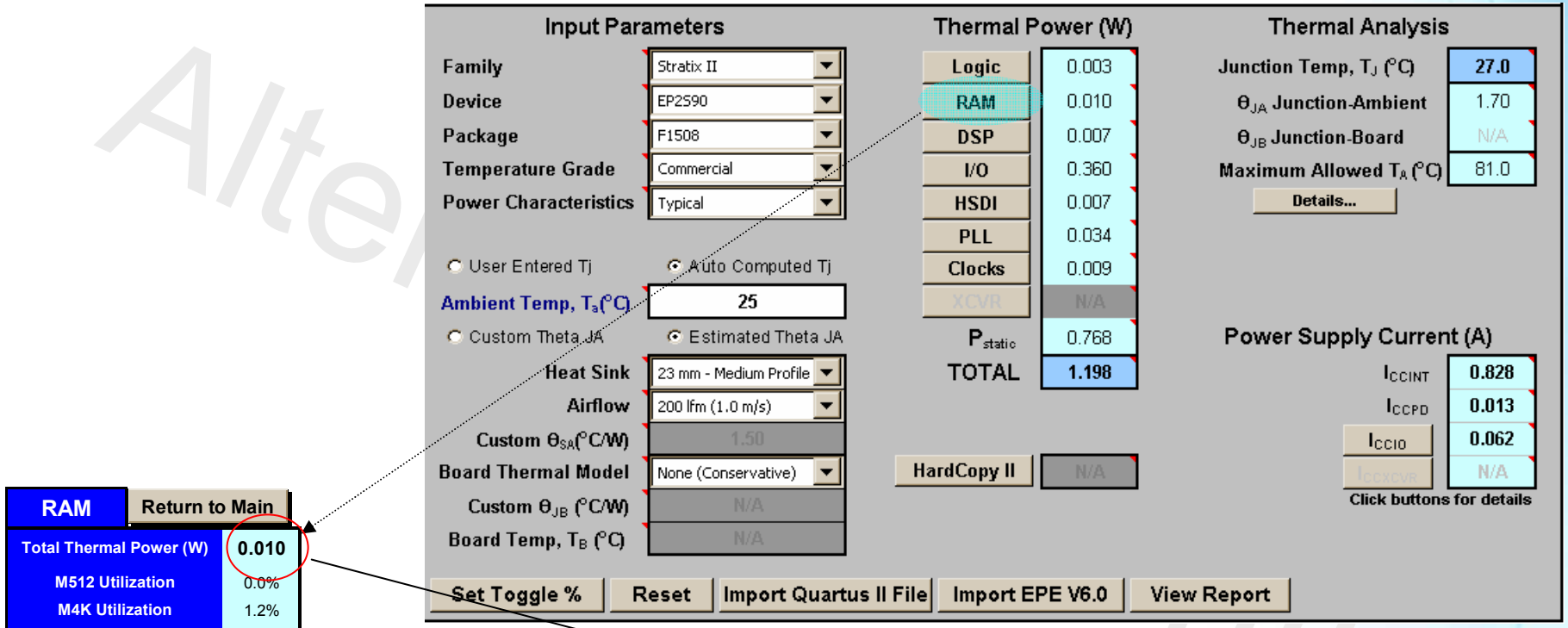
- Click “Logic” button to enter view Resource Page



Module	Clock Frequency (MHz)	# Combinational ALUTs	# FFs	Toggle %	Thermal Power (W) Routing	Block	Total	User Comments
1	111.1	12	0	42.7%	0.000	0.001	0.001	
2	111.1	0	72	18.8%	0.001	0.000	0.002	
	0.0	0	0	12.5%	0.000	0.000	0.000	

Using the RAM Resource Page

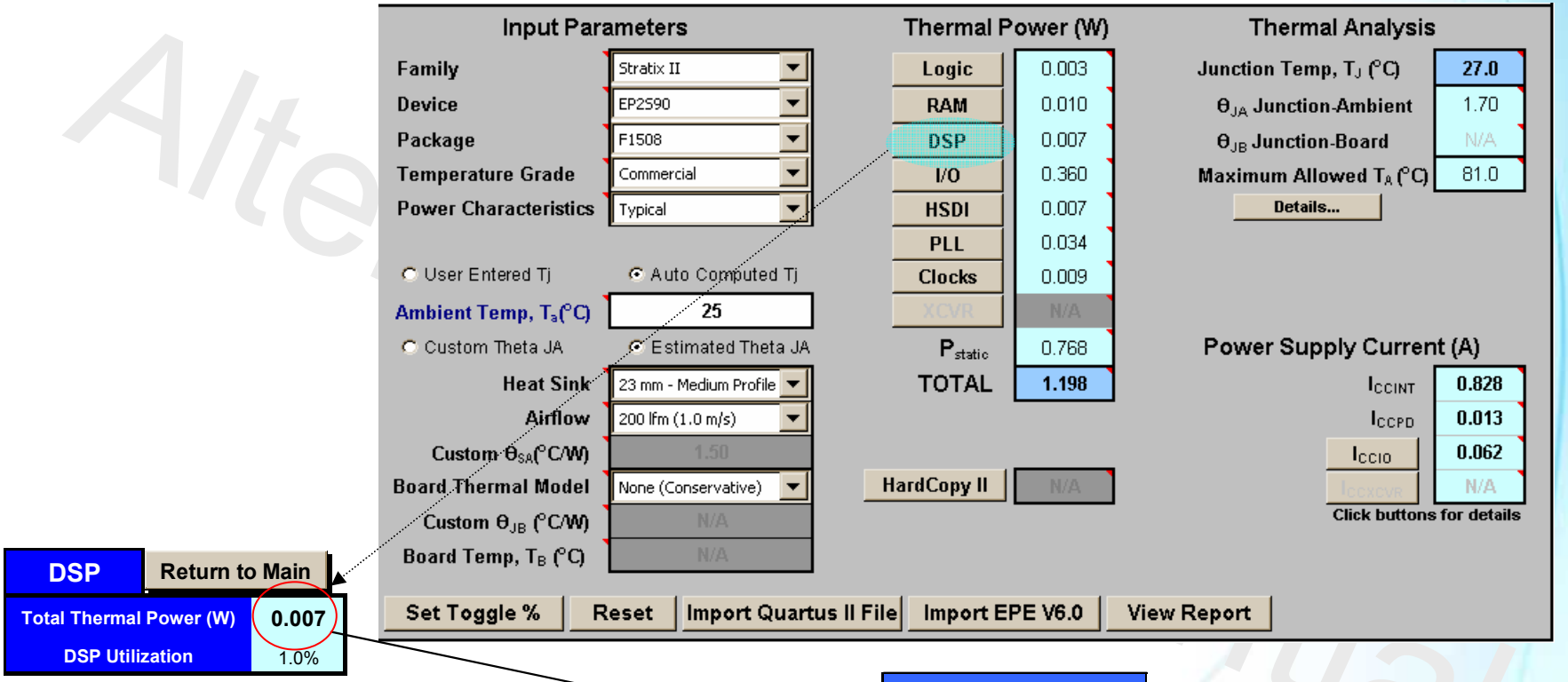
- Click “RAM” button to enter view Resource Page



					Port A			Port B					Thermal Power (W)			
Module	RAM Type	# RAM Blocks	Data Width	RAM Mode	Clock Freq (MHz)	Enable %	Write %	Clock Freq (MHz)	Enable %	R/W %	Toggle %	Valid Width/ Mode	Routing	Block	Total	User Comments
1	M4K	2	18	Simple Dual-Port	111.1	50%	50%	111.1	50%	100%	25.0%	Yes	0.001	0.003	0.003	
2	M4K	2	18	Simple Dual-Port	111.1	50%	50%	111.1	50%	50%	25.0%	Yes	0.000	0.002	0.002	
3	M4K	1	32	Simple Dual-Port	111.1	100%	100%	111.1	100%	100%	50.0%	Yes	0.002	0.003	0.005	

Using the DSP Resource Page

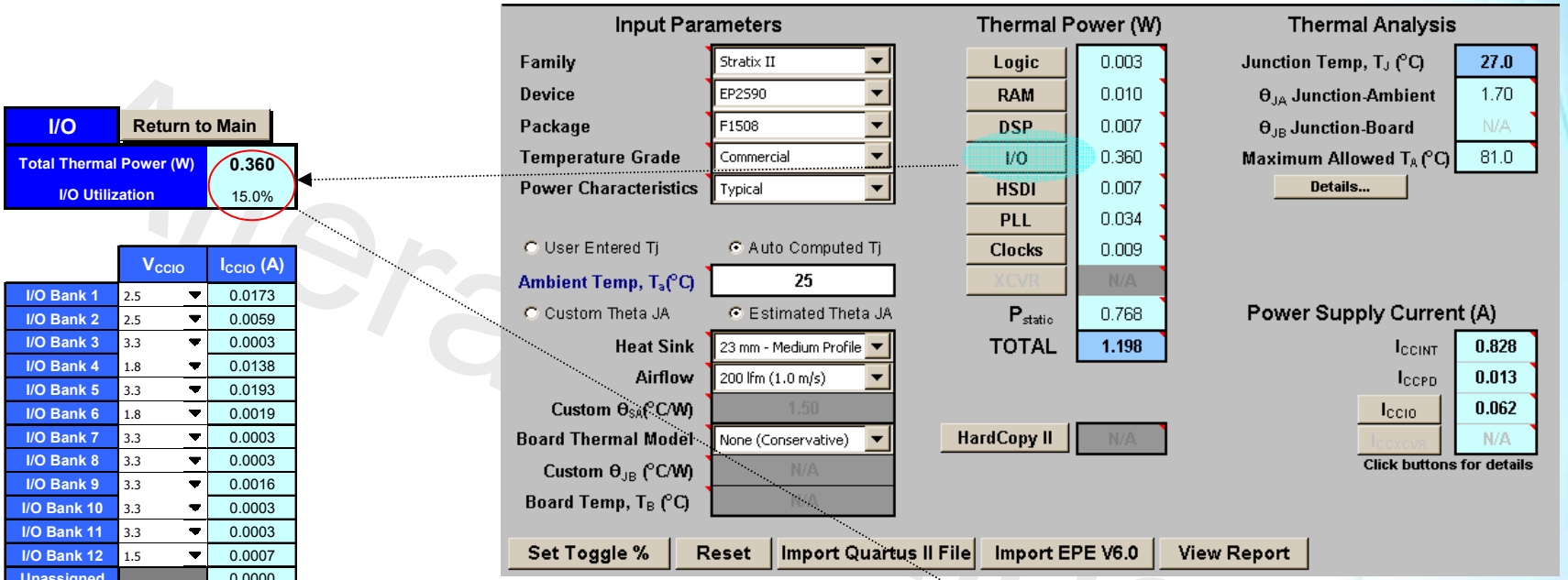
- Click “DSP” button to enter view Resource Page



Module	Configuration	Clock Freq (MHz)	# of Instances	Toggle %	Reg Inputs?	Reg Outputs?	Pipe-lined?	Thermal Power (W) Routing	Block	Total	User Comments
1	18x18 Mult-Accum	111.1	1	50.0%	Yes	No	Yes	0.003	0.004	0.007	
	9x9 Simple Mult	0.0	0	12.5%	Yes	Yes	No	0.000	0.000	0.000	

Using the I/O Resource Page

- Click “I/O” button to enter view Resource Page

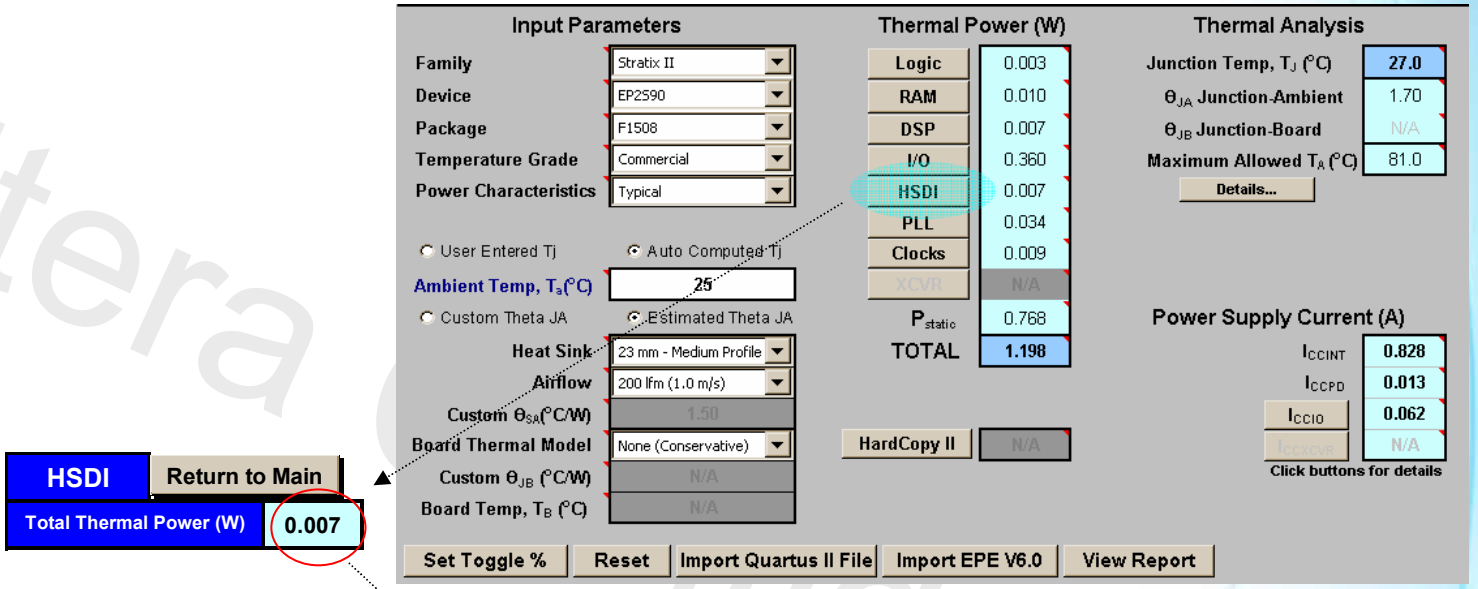


	V_{CCIO}	I_{CCIO} (A)
I/O Bank 1	2.5	0.0173
I/O Bank 2	2.5	0.0059
I/O Bank 3	3.3	0.0003
I/O Bank 4	1.8	0.0138
I/O Bank 5	3.3	0.0193
I/O Bank 6	1.8	0.0019
I/O Bank 7	3.3	0.0003
I/O Bank 8	3.3	0.0003
I/O Bank 9	3.3	0.0016
I/O Bank 10	3.3	0.0003
I/O Bank 11	3.3	0.0003
I/O Bank 12	1.5	0.0007
Unassigned		0.0000

Module	I/O Standard	Drive Strength / On-Chip Termination	Clock Freq (MHz)	# Output Pins	# Input Pins	# Bidir Pins	I/O Bank	Toggle %	OE %	Load (pF)	Data Rate	Bank I/O Std Check	Bank Voltage Check	Thermal Power (W) Routing	Thermal Power (W) Block	Thermal Power (W) Total	Supply Current (A) I_{CCINT}	Supply Current (A) I_{CCPD}	Supply Current (A) I_{CCIO}
1	LVTTL 3.3-V	24 mA	111.1	6	0	0	9	25.0%	100.0%	0	SDR	PASS	PASS	0.000	0.008	0.008	0.000	0.001	0.001
2	LVTTL 3.3-V	24 mA	111.1	1	0	0	3	0.8%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
3	SSTL Class I 1.8-V	12 mA	111.1	0	43	0	4	12.5%	100.0%	0	SDR	PASS	PASS	0.001	0.133	0.134	0.090	0.000	0.013
4	LVTTL 3.3-V	24 mA	111.1	0	5	0	5	12.5%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000	0.000
5	Differential HSTL Class I 1.5-V	12 mA	111.1	0	1	0	12	12.5%	100.0%	0	SDR	PASS	PASS	0.000	0.003	0.003	0.002	0.000	0.000
6	LVDS	Default	222.2	2	0	0	1	50.0%	100.0%	0	SDR	PASS	PASS	0.000	0.041	0.041	0.001	0.000	0.017
7	LVDS	Default	500.0	0	1	0	2	200.0%	100.0%	0	SDR	PASS	PASS	0.002	0.009	0.011	0.007	0.000	0.001
8	SSTL Class I 1.8-V	12 mA	111.1	0	5	0	6	12.5%	100.0%	0	SDR	PASS	PASS	0.000	0.015	0.015	0.010	0.000	0.002
9	LVTTL 3.3-V	12 mA	111.1	66	0	0	5	25.0%	100.0%	0	SDR	PASS	PASS	0.000	0.094	0.094	0.005	0.008	0.019
10	LVTTL 3.3-V	24 mA	0.0	0	1	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
11	LVDS	Default	1000.0	0	4	0	2	12.5%	100.0%	0	SDR	PASS	PASS	0.001	0.027	0.028	0.014	0.000	0.004

Using the HSDI Resource Page

- Click “HSDI” button to enter view Resource Page



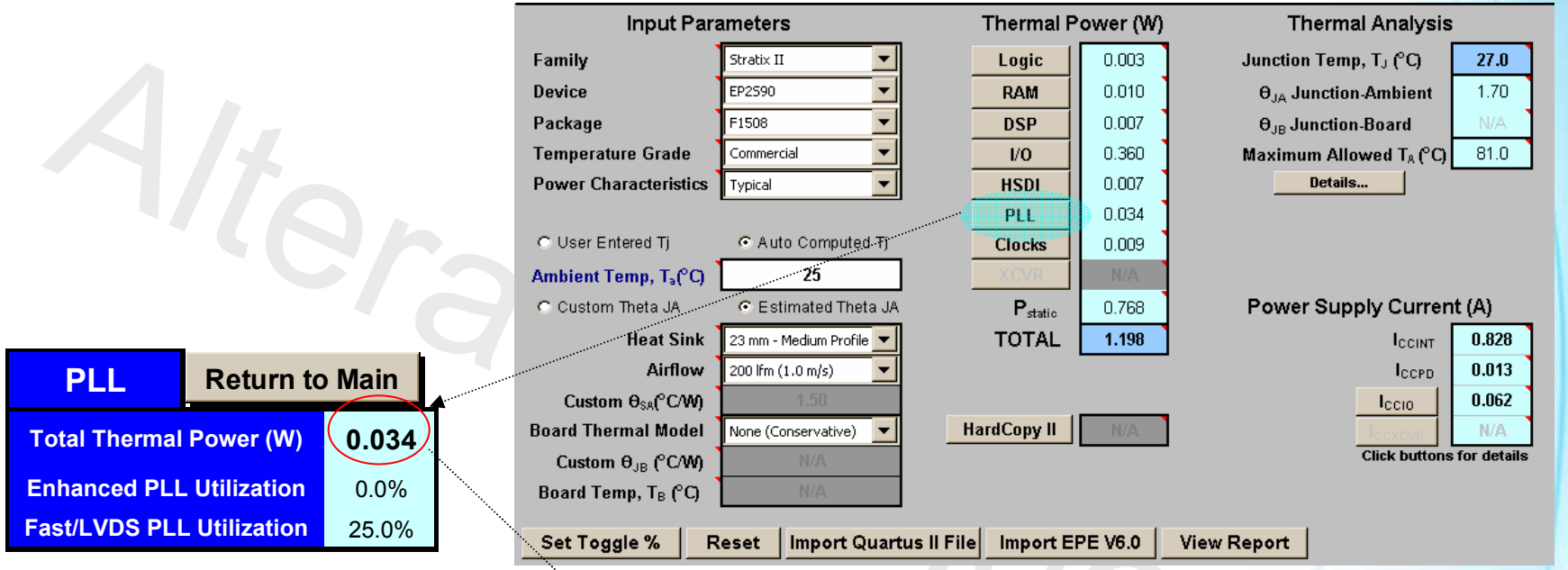
This section only estimates power within the SERDES blocks and does not include the I/O power nor PLL power. Please enter the appropriate parameters in the "IO" section for I/O power, and "PLL" section for PLL power.

Tx Module	Data Rate (Mbps)	# of Channels	Toggle %	Total Power (W)	User Comments
1	1000	2	50.0%	0.002	
	0	0	50.0%	0.000	
	0	0	50.0%	0.000	
	0	0	50.0%	0.000	

Rx Module	Data Rate (Mbps)	# of Channels	Toggle %	Total Power (W)	User Comments
1	1000	4	50.0%	0.005	
	0	0	50.0%	0.000	

Using the PLL Resource Page

- Click “PLL” button to enter view Resource Page

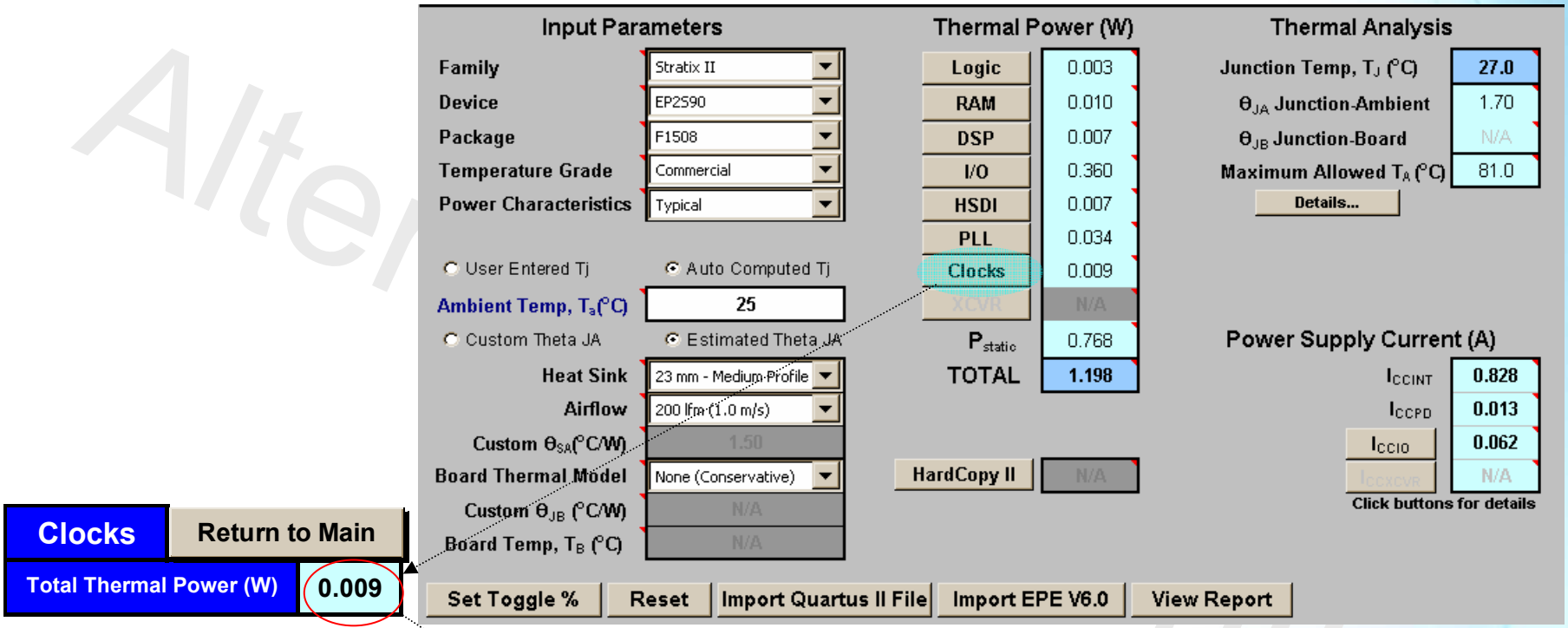


This section only estimates power from the PLL control blocks and does not include the power from the PLL clock output networks. Please enter additional parameters in the "Clocks" section.

Module	PLL Type	# PLL Blocks	# DPA Buses	Output Freq (MHz)	VCO Freq (MHz)	Total Power (W)	User Comments
1	Fast	2	0	111.1	1000.0	0.034	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	

Using the Clock Resource Page

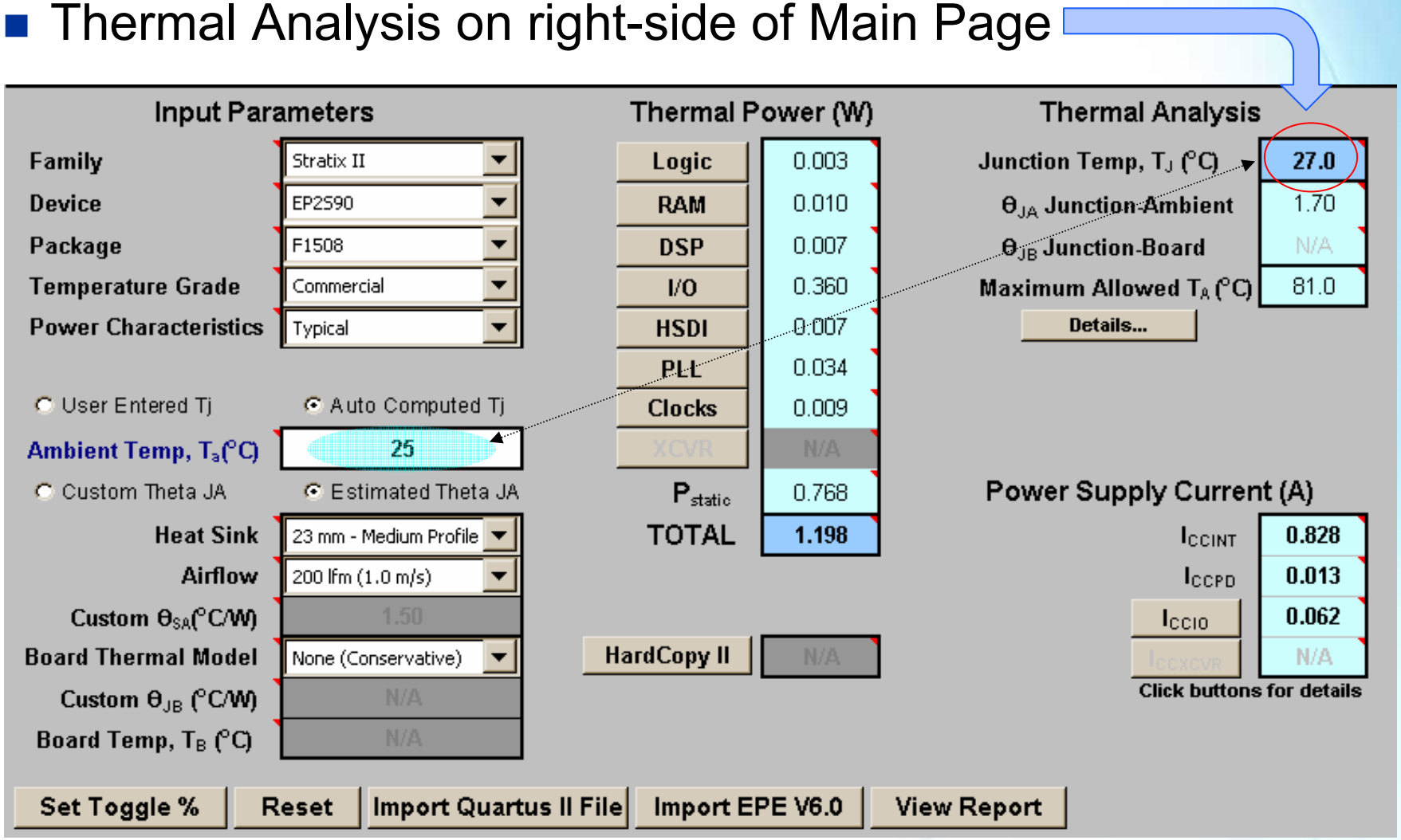
- Click “Clocks” button to enter view Resource Page



Domain	Clock Freq (MHz)	Total Fanout	Global Enable %	Local Enable %	Total Power (W)	User Comments
1	111.1	84	100%	100%	0.009	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	

Using the Thermal Analysis Section

- Thermal Analysis on right-side of Main Page

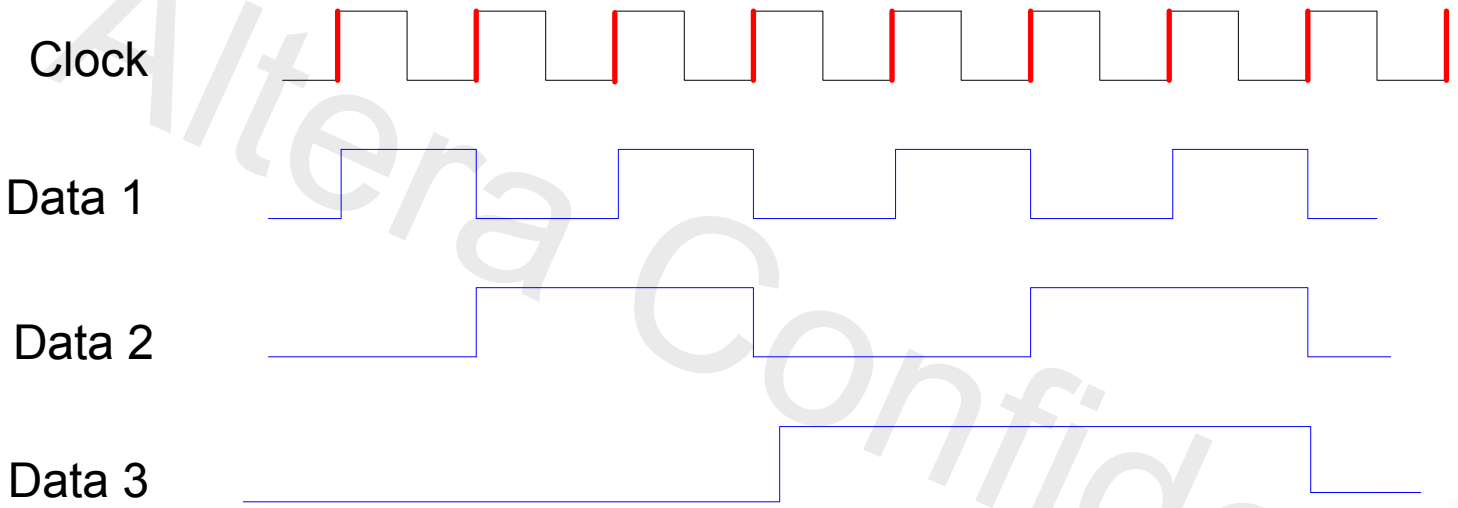


Thermal Analysis

- Thermal Analysis provides the following:
  - Junction Temp (T_J)
  - Junction-to-ambient thermal resistance (T_{JA})
  - Junction-to-board thermal resistance (T_{JB})
  - Maximum allowed ambient temperature (T_A)
- To automatically compute T_J, the following is required:
  - System ambient temperature – 25 C
  - Airflow – 200 lfm (1.0 m/s)
  - Heat sink solution (optional) – 23mm Medium Profile
  - Board thermal model – None (Conservative)

Calculating Toggle Rates

- Toggle Rate Calculations
  - Data 1,2,3 output



Average Toggle Rate for Data 1,2 and 3 = (100% + 50%+25%)/3 = 58.33%

EPE Standard Default Toggle Rate = 12.5%

Conclusion

- Early Power Estimator provides components necessary for system power planning:
  - Thermal Power
  - Thermal Analysis
  - Power Supply Information
- Accuracy of power estimation depends on info provided:
  - Accurate resource usage
  - Correct toggling rate
  - Operating conditions

Appendix

- EPE Block Resource Page – Detailed Descriptions
  - Logic
  - RAM
  - DSP
  - I/O
  - HSDI
  - PLL
  - Clocks

Logic Block

- Most accurate power estimation, partition the design into different design modules
- The following information must be entered by you.
  - Clock frequency (fmax) in MHz
  - Number of combinational adaptive look-up tables (ALUTs)
  - Number of registers
  - Toggle percentage

    The toggle rate describes how often the output changes with respect to the input clock which is usually between 6% and 12% for typical module for estimation purposes. This is a very critical piece of information for estimating your system dynamic power consumption. - Default toggle rate 12.5% for EPE

- Generic Design: Logic
  - ✓ Clock frequency = 111.1 MHz
  - ✓ Number of combinational adaptive look-up tables = 12
  - ✓ Number of registers = 72
  - ✓ Toggle percentage: ALUT = 42.7% & FFS= 18.8%

RAM Block

- TriMatrix memory consists of three types RAM blocks
  - M512
  - M4K
  - M-RAM blocks
- Each Row in the RAM section represents a design module which the following information must be entered by you.
  - Type of RAM being used
    - Single port
    - Simple Dual-port
    - True dual-port
    - ROM
  - The number of RAM implemented
  - The configuration of RAM block
  - Clock Frequency
  - The percentage of time the RAM clock is enabled
  - The percentage of time the port is writing compared to reading

- Generic Design: RAM
  - ✓ The number of RAM implemented = 5
  - ✓ The configuration of RAM block = M4K
  - ✓ Clock Frequency = 111.1 MHz
  - ✓ The percentage of time the RAM clock is enabled: 4 blocks = 50%, 1 Block = 100%
  - ✓ The percentage of time the port is writing compared to reading: 4 blocks = 50%, 1 Block = 100%

Digital Signal Processing (DSP)

- Dedicated DSP blocks that can be implemented for high speed DSP application.
- You must enter the following information for each DSP or multiplier module
  - Configuration
  - Clock frequency (fmax) in MHz
  - Number of instances
  - Toggle percentage of the data outputs
  - Whether or not the inputs and outputs are registered
  - Whether or not the module is pipelined

- Generic design: DSP
  - ✓ Clock Frequency =111.5 MHz
  - ✓ Number of instances = 1
  - ✓ Toggle rate = 50%
  - ✓ Outputs registered = yes
  - ✓ Configuration = DSP 18*18 multiplier with accumulator
  - ✓ Module pipelined = No

General I/O Pins

- You must enter the following parameters for each design module
  - I/O Standard
  - Clock frequency (fMAX) in MHz
  - Drive strength/On-chip termination
  - Number of output, input, and bidirectional pins
  - I/O Bank
  - Pin toggle percentage
  - Output enable percentage
  - Average capacitance of the load
  - I/O data rate
    - Note: The EPE will assume you are using external termination resistors
- Generic design: I/O
  - ✓ I/O Standard = LVTLL 3.3l, SSTL Class I 1.8, Diff HSTL Class I 1.5 , LVDS
  - ✓ Clock frequency = 500 MHz
  - ✓ Drive strength/On-chip termination = default
  - ✓ Number of output, input, and bidirectional pins = 0
  - ✓ I/O Bank = 1-6,9,12
  - ✓ Average Pin toggle percentage = 33%
  - ✓ Output enable percentage = 100%
  - ✓ Average capacitance of the load = 0
  - ✓ I/O data rate: LVDS input =1000 Mbps LVDS Output = 500 Mbps

High Speed Differential Interface (HSDI)

- HSDI section in EPE is divided two sections
  - Receiver
  - Transmitter

- You must enter the following parameter for the transmitter and receiver domain
  - Data rate (Mpbs)
  - Number of channels in that transmitter and Receiver domain
  - Toggle percentage

- HSDI power calculations only applies
  - Transmitter serializer block
  - Receiver deserializer block
    - Receiver power is the same whether or not the Dynamic phase alignment circuitry (DPA) is used
  - I/O and PLL power are calculated in their own sections

- Generic design: Receivers and Transmitters
  - ✓ Data rate = 1000 Mbps
  - ✓ Number of channels in transmitter = 2
  - ✓ Number of channels Receiver = 4
  - ✓ Toggle percentage = 50%

Phase-Locked Loops (PLLs)

- General and dedicated PLL
  - General usage
  - Enhanced PLL
  - Fast PLL
  - Dedicated PLL drives LVDS hardware
    - LVDS PLL
- You must enter the following parameters for the PLL
  - PLL type
  - Number of PLL blocks
  - Number of DPA buses
  - Output frequency
  - VCO frequency
- Generic design: PLL
  - ✓ PLL type = Fast
  - ✓ Number of PLL blocks = 2
  - ✓ Number of DPA buses = 0
  - ✓ Output frequency = 111.1 MHz
  - ✓ VCO frequency = 1000 MHz

Clocks

- The clock section represents a clock network in the domains
  - Global clock
  - Regional clock

    Note: Hardcopy makes no distinguish between the two clock domains

- You must enter the following parameters for the clock section
  - Clock Freq (MHz)
  - Total Fan-out
  - Global Enable%
  - Local Enable% -not applicable for Hardcopy II devices

- Generic design: Clock
  - ✓ Clock Freq (MHz) = 111.1 MHz
  - ✓ Total Fan-out = 84
  - ✓ Global Enable% = 100%
  - ✓ Local Enable% = 100%