Switching to the TimeQuest Timing Analyzer

Objectives

- Convert a design from using the Classic timing analyzer to using the TimeQuest timing analyzer
- Understand the differences between the two timing analysis engines
- Find sources for more information

Prerequisites

- Read TimeQuest Timing Analyzer in Volume III of the Quartus® II Handbook

  or

- View TimeQuest Timing Analyzer online training

- Have a copy of Switching to the TimeQuest Timing Analyzer chapter of Quartus II Handbook for reference

Agenda

- Introduction to switching
- Differences between the Classic and TimeQuest timing analyzers
  - Analysis
  - I/O timing constraints
  - Reporting
- Converting a design to the TimeQuest analyzer
- References

Introduction to Switching

- “Test drive” the TimeQuest tool with an existing project before switching
- SDC file required for constraints
  - Conversion utility helps convert QSF assignments to SDC file
- Switch on a per-project basis

Switching Options and Target Devices

- Default setting is to use Classic analyzer
- Exceptions
  - Projects targetting Arria™ GX devices
    - Must use TimeQuest analyzer
    - Cannot switch to Classic analyzer
  - New projects targetting Cyclone® III and Stratix® III devices
    - Default is TimeQuest analyzer
    - Can switch to Classic analyzer
- Check Quartus II Handbook, Help, or newer device handbook for other exceptions

Choosing Whether to Switch

- Switch if…
  - You are familiar with SDC
  - You have a design that is difficult to constrain with the Classic analyzer
    - DDR
    - Complex clocking structures
  - You prefer TimeQuest analysis and interface
- Don’t switch if…
  - Classic analyzer does everything you need

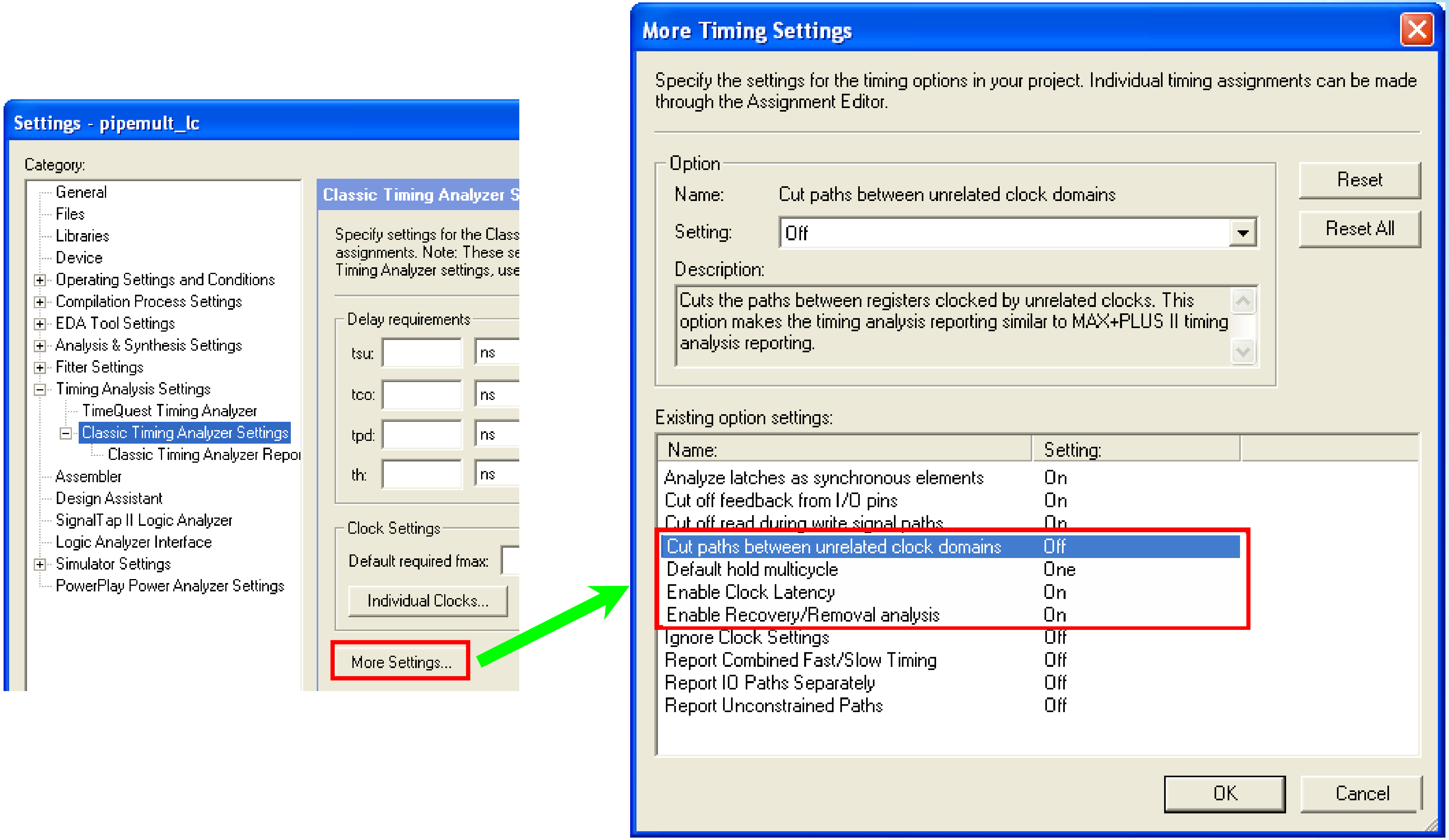
Switching to the TimeQuest Timing Analyzer

Analysis Differences

Classic Analyzer Settings for Switching

Setting	Classic Default	Recommended for Switching
Cut paths between unrelated clock domains	**ON**	**OFF**
Enable clock latency	**OFF**	**ON**
Enable recovery/removal analysis	**OFF**	**ON**
Default hold multicycle	**Same as Multicycle**	**One**

Change Classic Settings in GUI


Settings - pipemult_lc
Category:
General
Files
Libraries
Device
Operating Settings and Conditions
Compilation Process Settings
EDA Tool Settings
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
TimeQuest Timing Analyzer
Classic Timing Analyzer Settings
Classic Timing Analyzer Repoı
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
Simulator Settings
PowerPlay Power Analyzer Settings
Classic Timing Analyzer S
Individual Clocks...
More Settings...
More Timing Settings
Reset
Reset All
OK
Cancel

Specify settings for the Class assignments. Note: These se Timing Analyzer settings, use

Delay requirements

tsu: ns

tco: ns

tpd: ns

th: ns

Clock Settings

Default required fmax:

Specify the settings for the timing options in your project. Individual timing assignments can be made through the Assignment Editor.

Option

Name: Cut paths between unrelated clock domains

Setting: Off

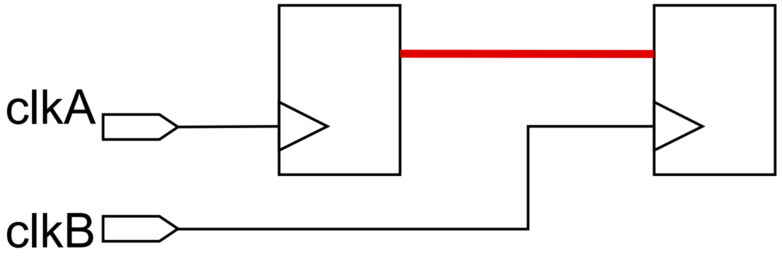
Description:

Cuts the paths between registers clocked by unrelated clocks. This option makes the timing analysis reporting similar to MAX+PLUS II timing analysis reporting.

Existing option settings:

Name:	Setting:
Analyze latches as synchronous elements	On
Cut off feedback from I/O pins	On
Cut off read during write signal paths	On
Cut paths between unrelated clock domains	Off
Default hold multicycle	One
Enable Clock Latency	On
Enable Recovery/Removal analysis	On
Ignore Clock Settings	Off
Report Combined Fast/Slow Timing	Off
Report IO Paths Separately	Off
Report Unconstrained Paths	Off

Cut Paths between Unrelated Clock Domains

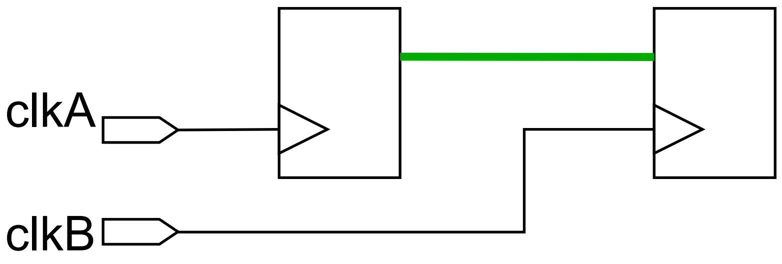


- Classic analyzer default: **ON**
  - Worst-case behavior (matches TimeQuest behavior): **OFF**
- Does not analyze paths between unrelated clock domains

Cut Paths between Unrelated Clock Domains

- Classic analyzer does not analyze paths between unrelated clock domains by default
  - May mask design problems
  - Timing Constraint Check tool helps show those paths
- Turn setting **OFF** and constrain cross-clock domain paths
  - Add cut or setup/hold relationship assignments

TimeQuest Behavior: Cross-Domain Paths

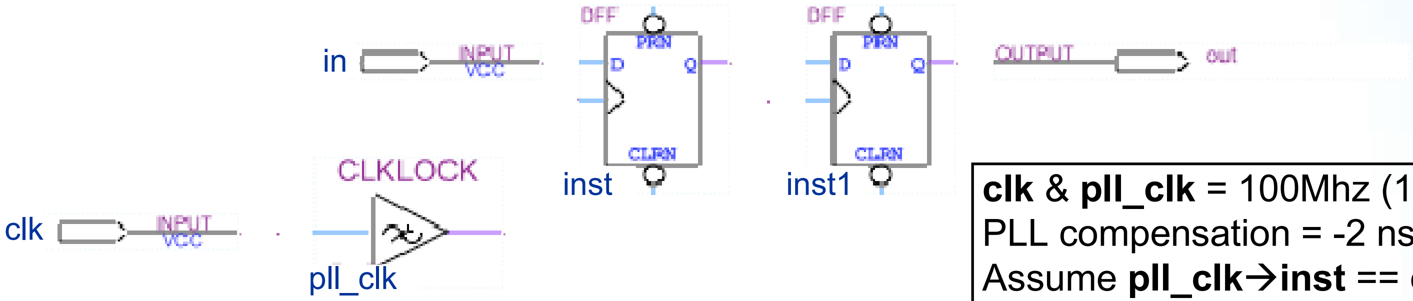


- Analyzes all paths between clock domains
- All clocks related
  - Matches turning OFF **Cut paths between unrelated clock domains**
  - Manually cut unrelated clock domains
    - `set_false_path` or `set_clock_groups`

Enable Clock Latency

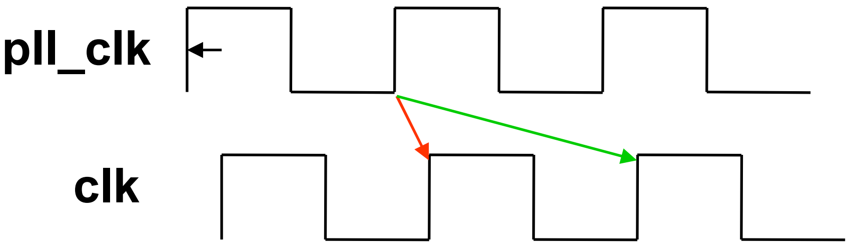
- Classic analyzer default: **OFF**
  - Treats clock path delays between base clock and derived clock as offset instead of latency
    - Example: PLL compensation delays
- Offset affects setup/hold relationships
  - Sometimes requires multicycle assignments to correct
  - Place and route changes can “break” corrections
- Latency affects clock skew
- Always turn this setting **ON**

Analysis Using Clock Offset



clk & **pll_clk** = 100Mhz (10 ns)
PLL compensation = -2 ns
Assume **pll_clk→inst** == **clk→inst1clk**
inst→inst1 = 3 ns

Using offset

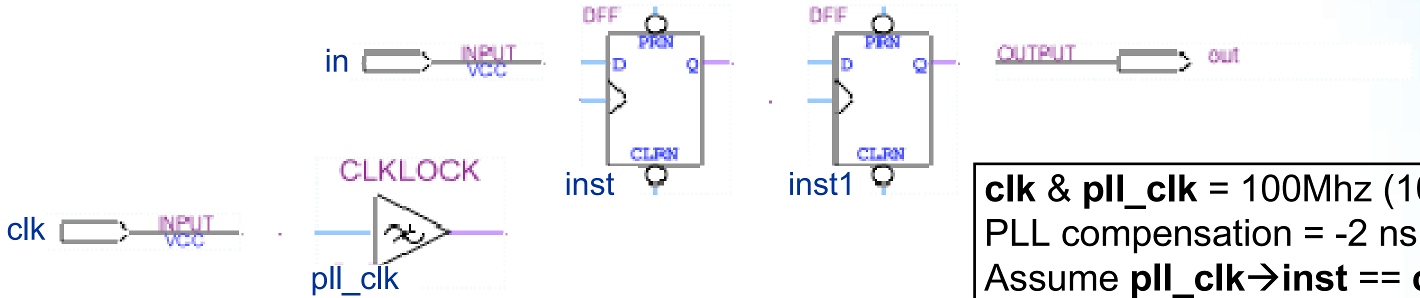


Offset = -2 ns
Clock skew = 0 ns

Setup relationship = 2 ns
Slack = 2 + 0 - 3 = -1 ns

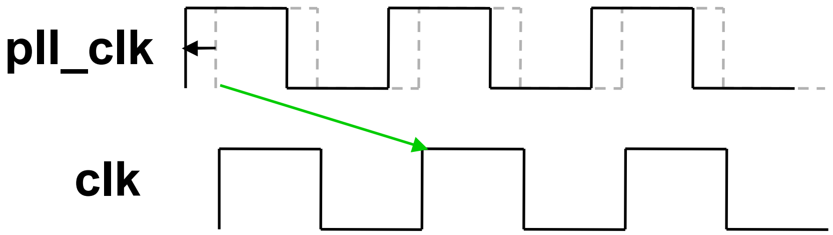
Requires multicycle = 2
Setup relationship = 12 ns
Slack = 12 + 0 - 3 = 9 ns

Analysis Using Clock Latency



clk & **pll_clk** = 100Mhz (10 ns)
PLL compensation = -2 ns
Assume **pll_clk→inst** == **clk→inst1clk**
inst→inst1 = 3 ns

Using latency



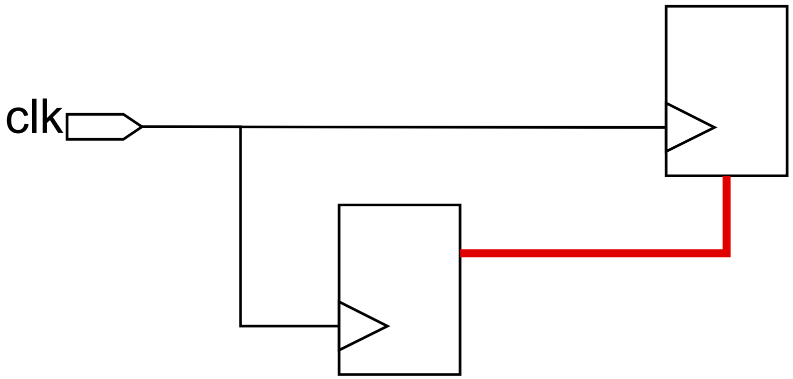
Latency = -2 ns
Clock skew = 2 ns

Setup relationship = 10 ns
Slack = 10 + 2 - 3 = 9 ns

TimeQuest Behavior: Clock Latency

- TimeQuest treats clock path delays between base clock and derived clock as latency
- Always uses latency, not offset

Enable Recovery/Removal Analysis

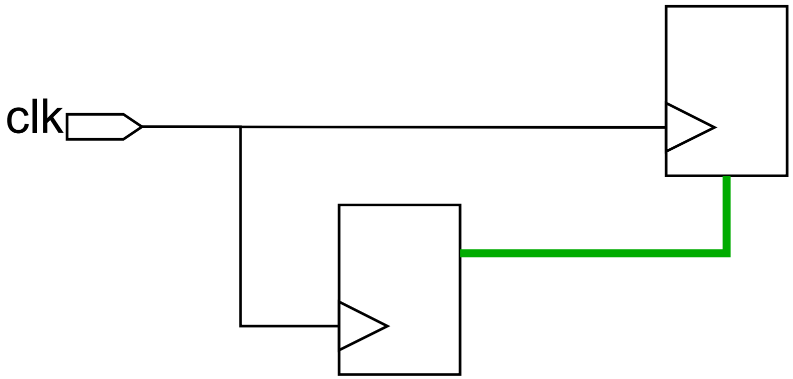


- Classic analyzer default: **OFF**
  - Worst-case behavior (matches TimeQuest behavior): **ON**
- Does not perform recovery & removal analysis on asynchronous control paths

Enable Recovery/Removal Analysis

- Classic analyzer does not analyze asynchronous control signals by default
  - Similar to setup/hold check for synchronous data paths
  - Tests assertion/de-assertion of asynchronous control signal near an active clock edge
- Turn this setting **ON**

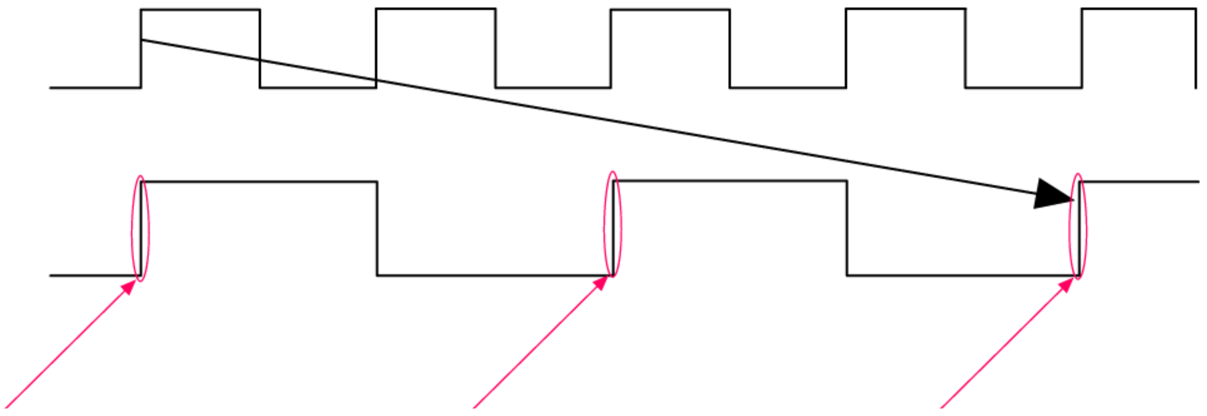
TimeQuest Behavior: Asynchronous Path Analysis



- Always performs recovery/removal analysis
- Analyzes asynchronous control paths

Default Hold Multicycle

- Edge to use for analysis when creating a *(setup)* multicycle assignment with no corresponding *hold* multicycle assignment
- Classic analyzer default: **Same as Multicycle**
  - Worst-case behavior: **One**



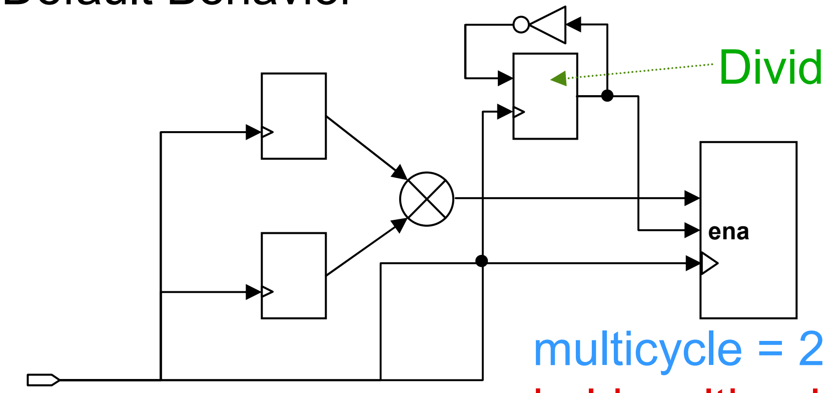
Same as Multicycle

One

Multicycle = 2

Classic Default Hold Multicycle

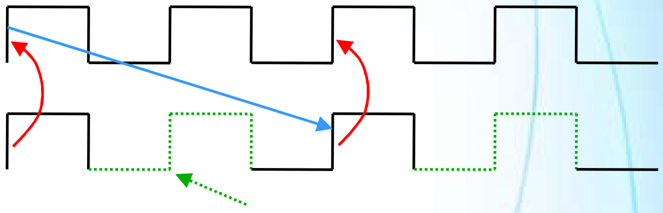
Default Behavior



Divide by 2

multicycle = 2

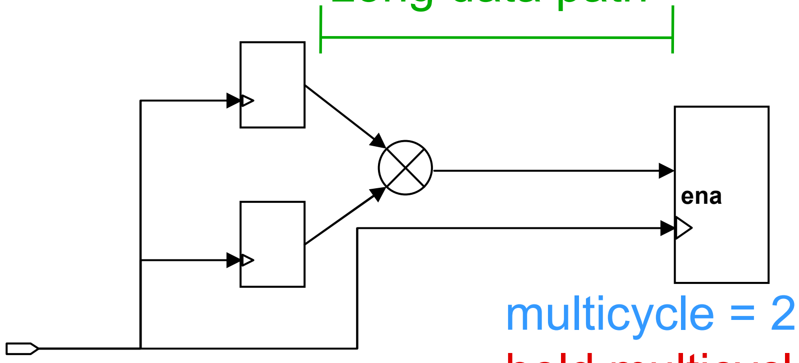
hold multicycle = 2



Disabled by divide-by-2 enable

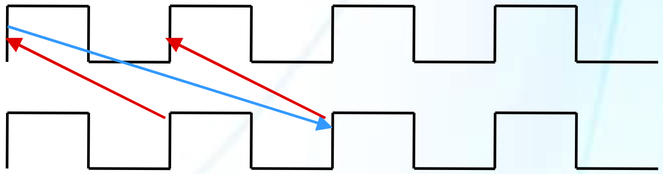
Worst-Case Behavior

Long data path



multicycle = 2

hold multicycle = 1



Classic Multicycle Recommendation

- Do not rely on a default value
  - Possibility of different assumptions
  - Multiple people designing modules
    - One person has default of **One**
    - One person has default of **Same as Multicycle**
- Specify a hold multicycle value for each multicycle assignment

TimeQuest Behavior: Hold Multicycle

- Hold multicycle default value is **0**
  - Equivalent to Classic setting of **One**
  - TimeQuest hold multicycle = Classic setting - 1
- Defaults to worst-case behavior

Switching to the TimeQuest Timing Analyzer

I/O Timing Constraint Differences

I/O Timing Assignments

- FPGA-centric: t_{SU}, t_{CO}, etc.
  - Between FPGA boundary and internal register
- System-centric: input delay, output delay
  - Between external register and internal register
    - Just a register-to-register path
- Often easier to use system-centric I/O assignments
  - Define external environment that I/O timing must meet

FPGA-Centric vs. System-Centric

- Table shows conversion for simple cases
  - Not appropriate in every situation
- Detailed information in Switching to TimeQuest chapter

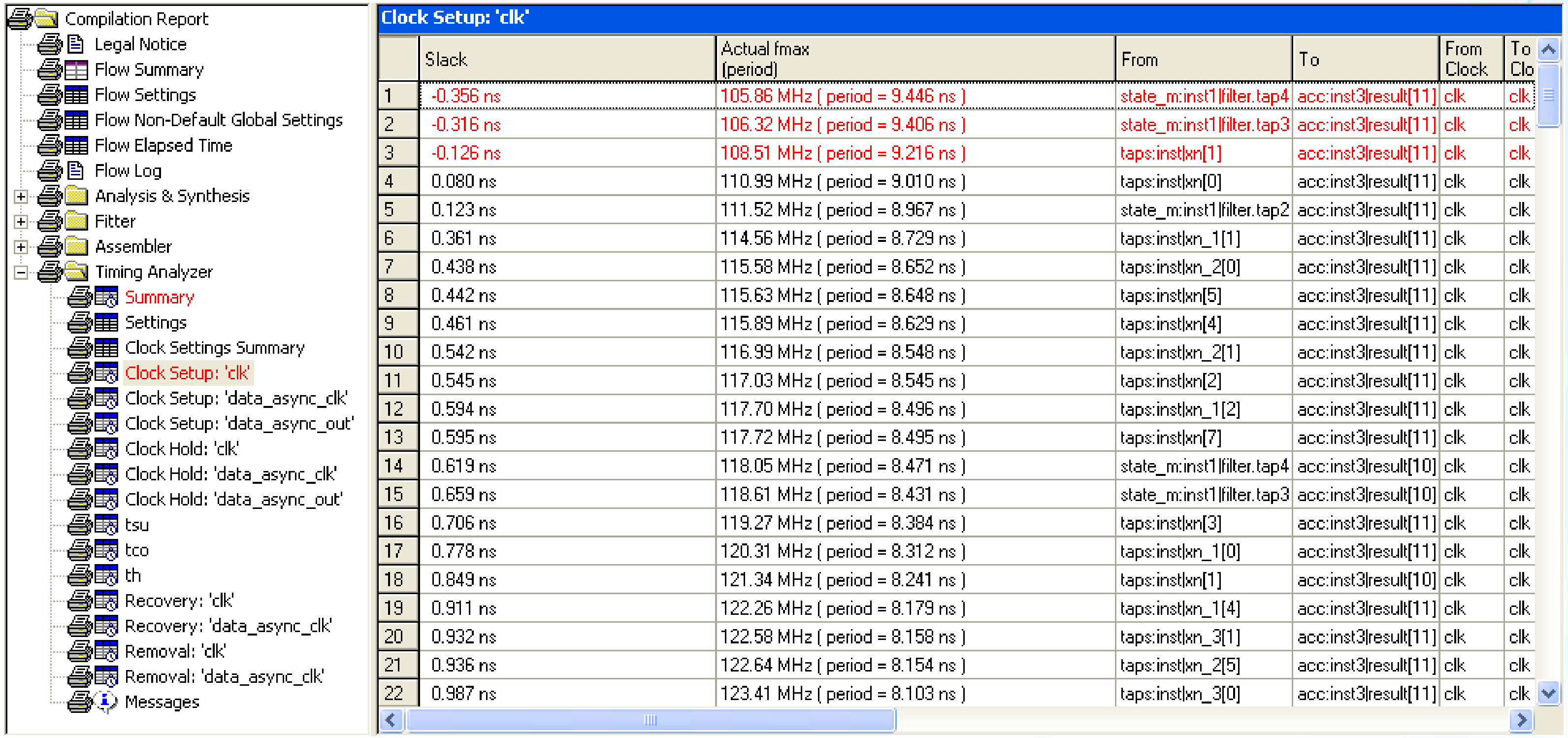
FPGA-Centric	System-Centric (SDC constraints)
t_{SU} requirement	set_input_delay -max <*period* - t_{SU}>
t_{H} requirement	set_input_delay -min <t_{H}>
t_{CO} requirement	set_output_delay -max <*period* - t_{CO}>
Minimum t_{CO} requirement	set_output_delay -min -<*min* t_{CO}>

Switching to the TimeQuest Timing Analyzer

Reporting Differences

Classic Analyzer Reporting

- Generates many reports by default
- Get further detail from default reports



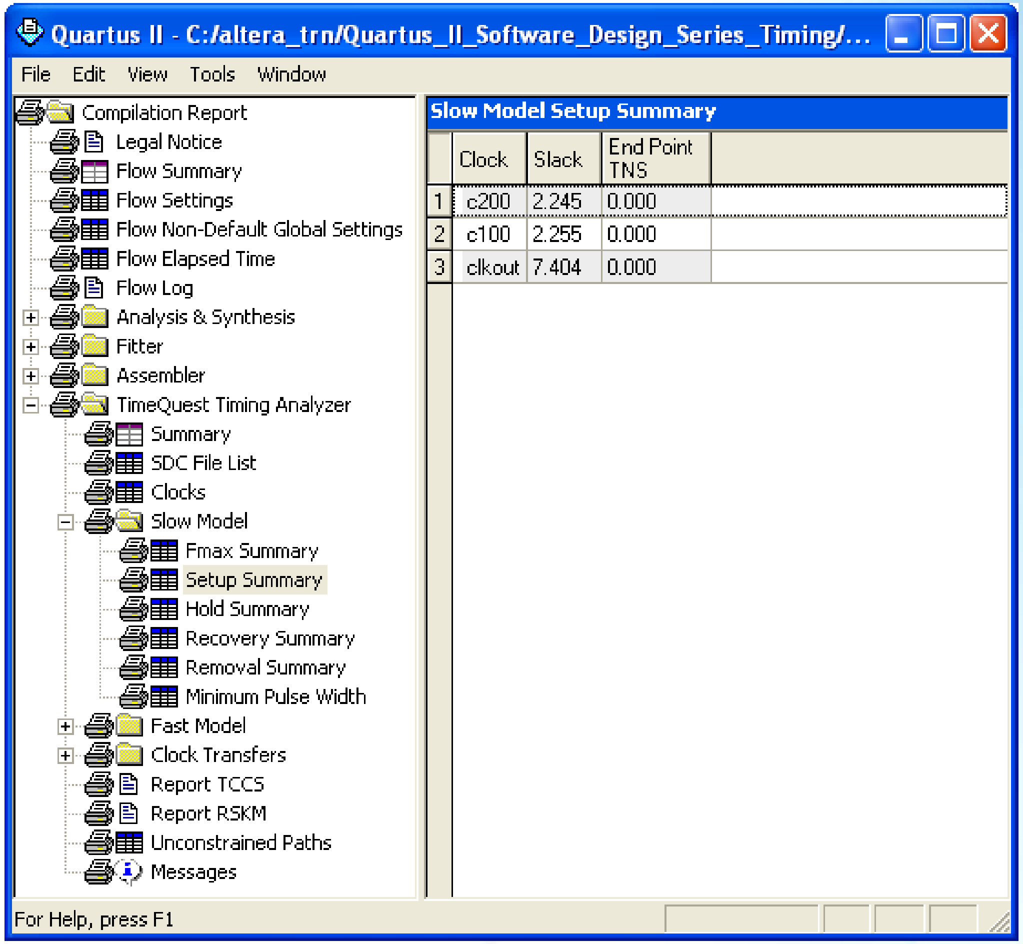
- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Settings
  - Flow Elapsed Time
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
    - Summary
    - Settings
    - Clock Settings Summary
    - Clock Setup: 'clk'
    - Clock Setup: 'data_async_clk'
    - Clock Setup: 'data_async_out'
    - Clock Hold: 'clk'
    - Clock Hold: 'data_async_clk'
    - Clock Hold: 'data_async_out'
    - tsu
    - tco
    - th
    - Recovery: 'clk'
    - Recovery: 'data_async_clk'
    - Removal: 'clk'
    - Removal: 'data_async_clk'
    - Messages

Clock Setup: 'clk'

	Slack	Actual fmax (period)	From	To	From Clock	To Clo
1	-0.356 ns	105.86 MHz (period = 9.446 ns)	state_m:inst1|filter.tap4	acc:inst3|result[11]	clk	clk
2	-0.316 ns	106.32 MHz (period = 9.406 ns)	state_m:inst1|filter.tap3	acc:inst3|result[11]	clk	clk
3	-0.126 ns	108.51 MHz (period = 9.216 ns)	taps:inst|xn[1]	acc:inst3|result[11]	clk	clk
4	0.080 ns	110.99 MHz (period = 9.010 ns)	taps:inst|xn[0]	acc:inst3|result[11]	clk	clk
5	0.123 ns	111.52 MHz (period = 8.967 ns)	state_m:inst1|filter.tap2	acc:inst3|result[11]	clk	clk
6	0.361 ns	114.56 MHz (period = 8.729 ns)	taps:inst|xn_1[1]	acc:inst3|result[11]	clk	clk
7	0.438 ns	115.58 MHz (period = 8.652 ns)	taps:inst|xn_2[0]	acc:inst3|result[11]	clk	clk
8	0.442 ns	115.63 MHz (period = 8.648 ns)	taps:inst|xn[5]	acc:inst3|result[11]	clk	clk
9	0.461 ns	115.89 MHz (period = 8.629 ns)	taps:inst|xn[4]	acc:inst3|result[11]	clk	clk
10	0.542 ns	116.99 MHz (period = 8.548 ns)	taps:inst|xn_2[1]	acc:inst3|result[11]	clk	clk
11	0.545 ns	117.03 MHz (period = 8.545 ns)	taps:inst|xn[2]	acc:inst3|result[11]	clk	clk
12	0.594 ns	117.70 MHz (period = 8.496 ns)	taps:inst|xn_1[2]	acc:inst3|result[11]	clk	clk
13	0.595 ns	117.72 MHz (period = 8.495 ns)	taps:inst|xn[7]	acc:inst3|result[11]	clk	clk
14	0.619 ns	118.05 MHz (period = 8.471 ns)	state_m:inst1|filter.tap4	acc:inst3|result[10]	clk	clk
15	0.659 ns	118.61 MHz (period = 8.431 ns)	state_m:inst1|filter.tap3	acc:inst3|result[10]	clk	clk
16	0.706 ns	119.27 MHz (period = 8.384 ns)	taps:inst|xn[3]	acc:inst3|result[11]	clk	clk
17	0.778 ns	120.31 MHz (period = 8.312 ns)	taps:inst|xn_1[0]	acc:inst3|result[11]	clk	clk
18	0.849 ns	121.34 MHz (period = 8.241 ns)	taps:inst|xn[1]	acc:inst3|result[10]	clk	clk
19	0.911 ns	122.26 MHz (period = 8.179 ns)	taps:inst|xn_1[4]	acc:inst3|result[11]	clk	clk
20	0.932 ns	122.58 MHz (period = 8.158 ns)	taps:inst|xn_3[1]	acc:inst3|result[11]	clk	clk
21	0.936 ns	122.64 MHz (period = 8.154 ns)	taps:inst|xn_2[5]	acc:inst3|result[11]	clk	clk
22	0.987 ns	123.41 MHz (period = 8.103 ns)	taps:inst|xn_3[0]	acc:inst3|result[11]	clk	clk

TimeQuest Analyzer Reporting

- TimeQuest analyzer generates 4 summary compilation reports when enabled
- Use TimeQuest interface for on-demand reporting
  - More efficient reporting, less cluttered interface



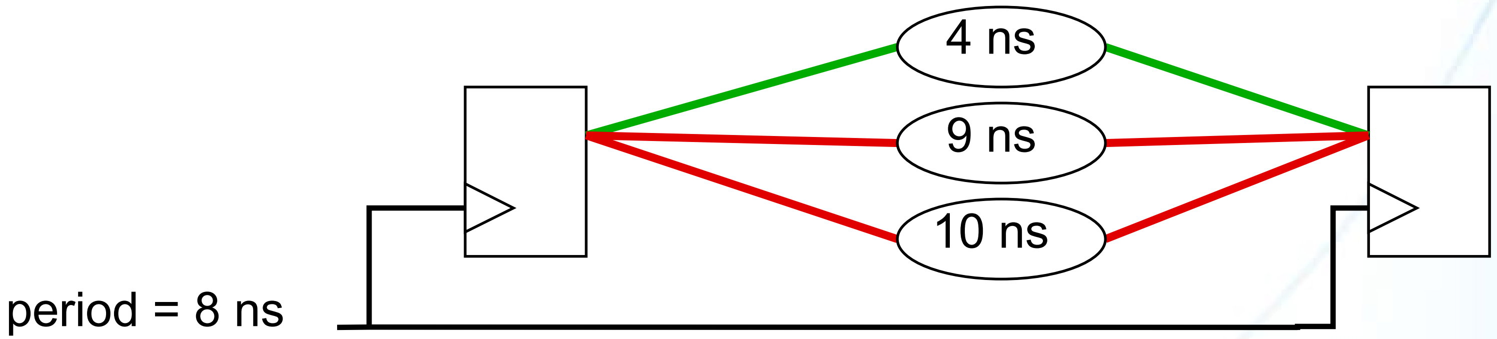
Quartus II - C:/altera_trn/Quartus_II_Software_Design_Series_Timing/...

Slow Model Setup Summary

	Clock	Slack	End Point TNS
1	c200	2.245	0.000
2	c100	2.255	0.000
3	clkout	7.404	0.000

Path-Based Reporting

- Classic analyzer reports only single worst-case path between registers
- TimeQuest analyzer reports all paths between registers
  - Can uncover more failing paths



Switching to the TimeQuest Timing Analyzer

Conversion

Convert a Design to the TimeQuest TA

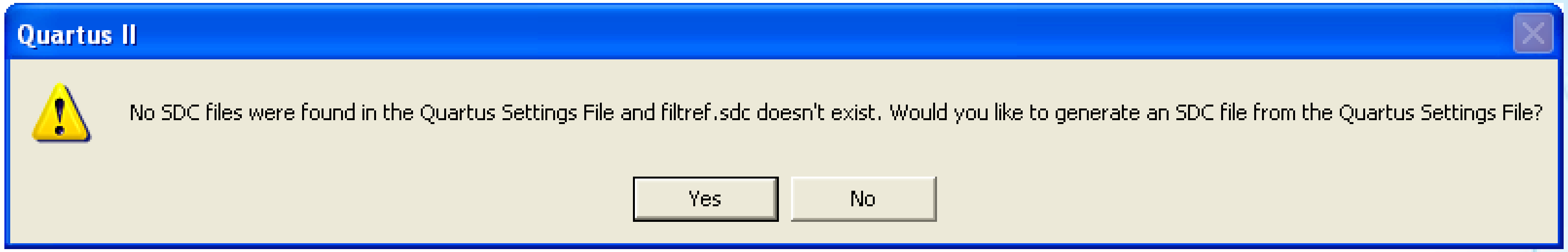
1. Compile design in the Quartus II software
2. Run conversion utility to create SDC file
3. Analyze design in TimeQuest interface and review timing reports
4. Turn on TimeQuest analyzer in Quartus II settings

- If you are comfortable with SDC, skip steps 1 and 2 and write your own SDC file

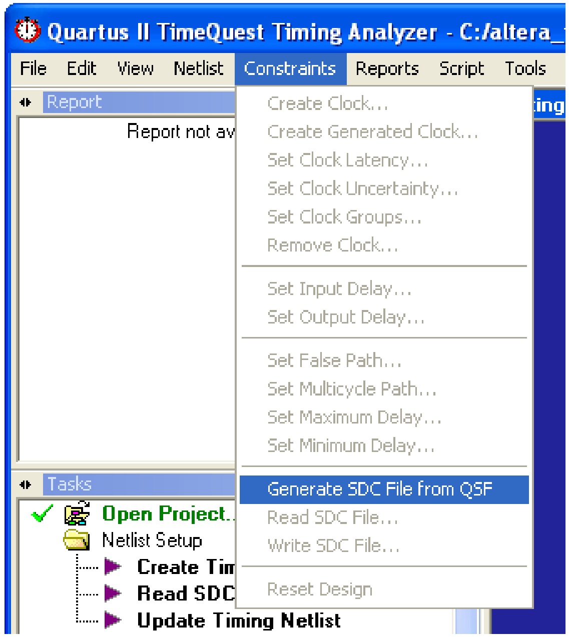
Compile Design in the Quartus II Software

- Some assignments not in QSF but are reported by Classic timing analyzer
  - Assignments in HDL source code
  - PLL input clocks
- Conversion utility reads timing analysis report if it exists
- Use recommended settings for Classic analyzer

Run Conversion Utility



No SDC files were found in the Quartus Settings File and filtref.sdc doesn't exist. Would you like to generate an SDC file from the Quartus Settings File?



```
C:\Projects> quartus_sta --qsf2sdc project_name
```

Conversion Utility Notes

- Not all QSF assignments are converted
- Conversion utility makes assumptions
  - May result in incorrect conversion if your assignments don't match assumptions
- Review SDC file to ensure accuracy
  - Add or update constraints as necessary
- Edit a copy of the SDC file so reconverting doesn't overwrite changes

Conversion Utility Assumptions

- Recommended global settings configured correctly
- All (setup) multicycle exceptions require matching hold multicycle exception
- Other assumptions detailed in Switching chapter

Sample Conversion (Clock & Multicycle)

```
# Original Clock Setting Name: clk
create_clock -period "100.0 MHz" -name clk clk
# ---------------------------------------------
# QSF: -name MULTICYCLE 2 -from inst1 -to inst2
set_multicycle_path -end -setup -from [get_keepers {inst1}] -to
   [get_keepers {inst2}] 2
set_multicycle_path -end -hold -from [get_keepers {inst1}] -to
   [get_keepers {inst2}] 0
# QSF: -name MULTICYCLE 2 -from inst1 -to inst3
set_multicycle_path -end -setup -from [get_keepers {inst1}] -to
   [get_keepers {inst3}] 2
set_multicycle_path -end -hold -from [get_keepers {inst1}] -to
   [get_keepers {inst3}] 0
```

Sample Conversion (T_{SU} & T_H Require.)

```
# QSF: -name TSU_REQUIREMENT 3 ns -from * -to in4
set_max_delay 3 -from [get_ports {in4}] -to [get_registers *]
# QSF: -name TSU_REQUIREMENT 5 ns -from * -to in1
set_max_delay 5 -from [get_ports {in1}] -to [get_registers *]
# QSF: -name TH_REQUIREMENT 1 ns -from * -to in2
set_min_delay -1.0 -from [get_ports {in2}] -to [get_registers *]
```

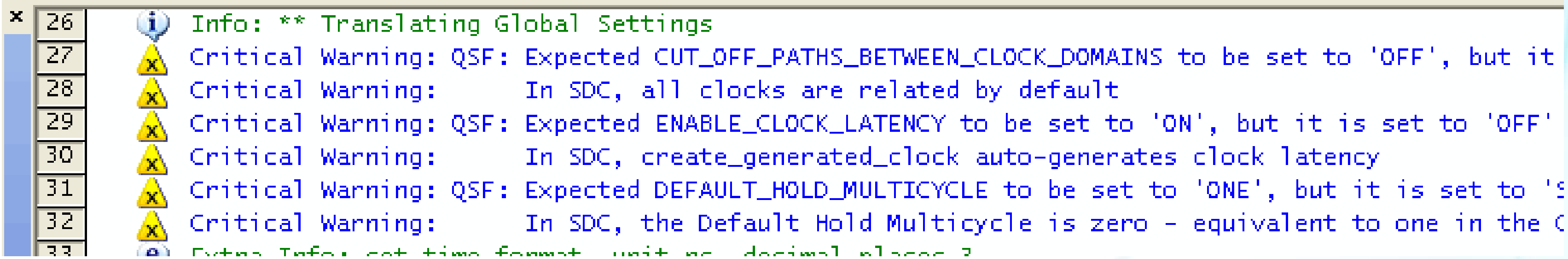
Analyze Design & Review Reports

- Perform timing analysis in TimeQuest analyzer
- If there are unexpected results…

1. Check recommended settings and re-convert if needed
2. Cut unrelated clock domains
3. Add hold multicycle exceptions if needed
   - Automatically added if setup multicycle exceptions exist
4. Ensure all clocks are constrained

Check Recommended Settings

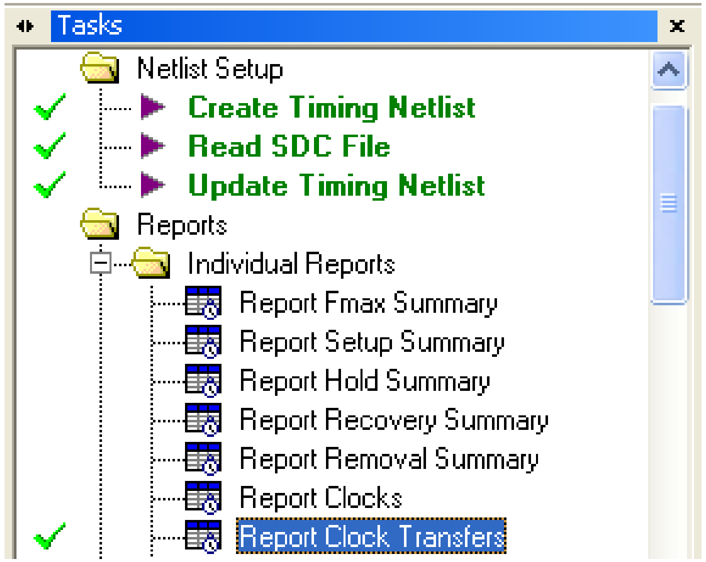
- Other recommended Classic settings exist
  - All can cause differences between Classic and TimeQuest analysis
- To fix:
  - Update settings in Classic analyzer
  - Re-analyze design (recompile and perform timing analysis again)
  - Run conversion again, or accept differences

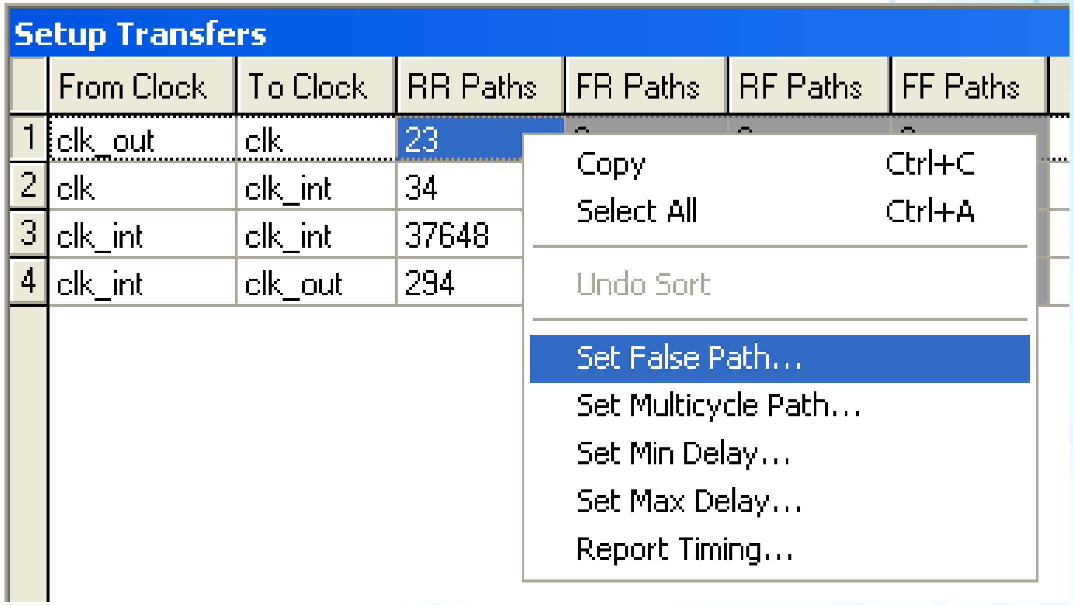


```
Info: ** Translating Global Settings
Critical Warning: QSF: Expected CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS to be set to 'OFF', but it
Critical Warning:      In SDC, all clocks are related by default
Critical Warning: QSF: Expected ENABLE_CLOCK_LATENCY to be set to 'ON', but it is set to 'OFF'
Critical Warning:      In SDC, create_generated_clock auto-generates clock latency
Critical Warning: QSF: Expected DEFAULT_HOLD_MULTICYCLE to be set to 'ONE', but it is set to 'S
Critical Warning:      In SDC, the Default Hold Multicycle is zero - equivalent to one in the C
Extra Info: set_time_format -unit ns -decimal_places 3
```

Report Clock Transfers

- Verify cross-clock domain paths
- Right-click to cut clock domains or add multicycle constraints
  - Applied to timing netlist in TimeQuest memory, *not* SDC file
  - Write out or manually edit SDC file

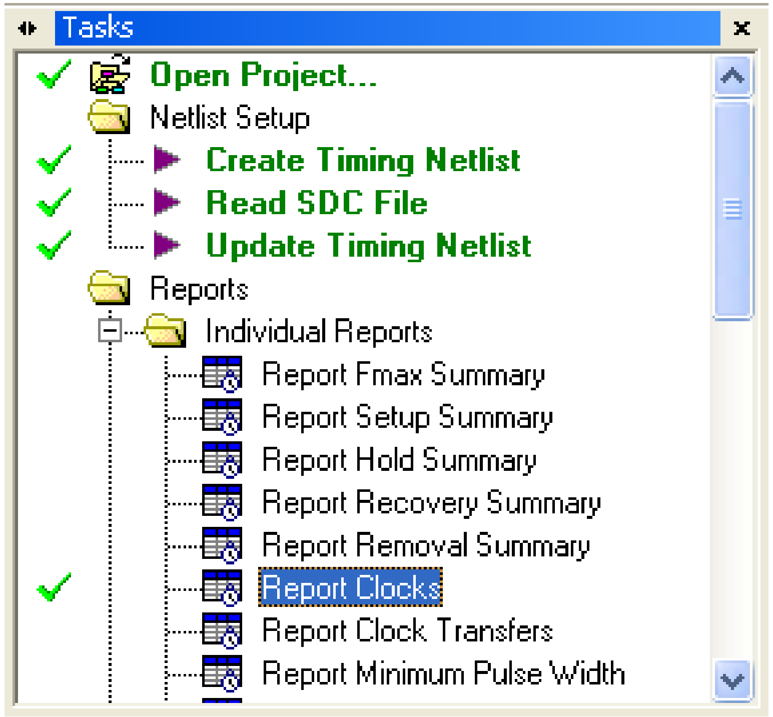



Setup Transfers

	From Clock	To Clock	RR Paths	FR Paths	RF Paths	FF Paths
1	clk_out	clk	23			
2	clk	clk_int	34			
3	clk_int	clk_int	37648			
4	clk_int	clk_out	294			

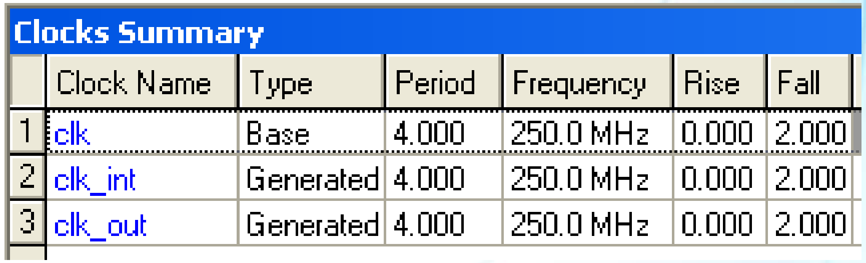
Report Clocks

- Are all clocks listed (constrained correctly)?
- Make necessary clock constraints
  - Create generated clocks on ripple clocks



Tasks

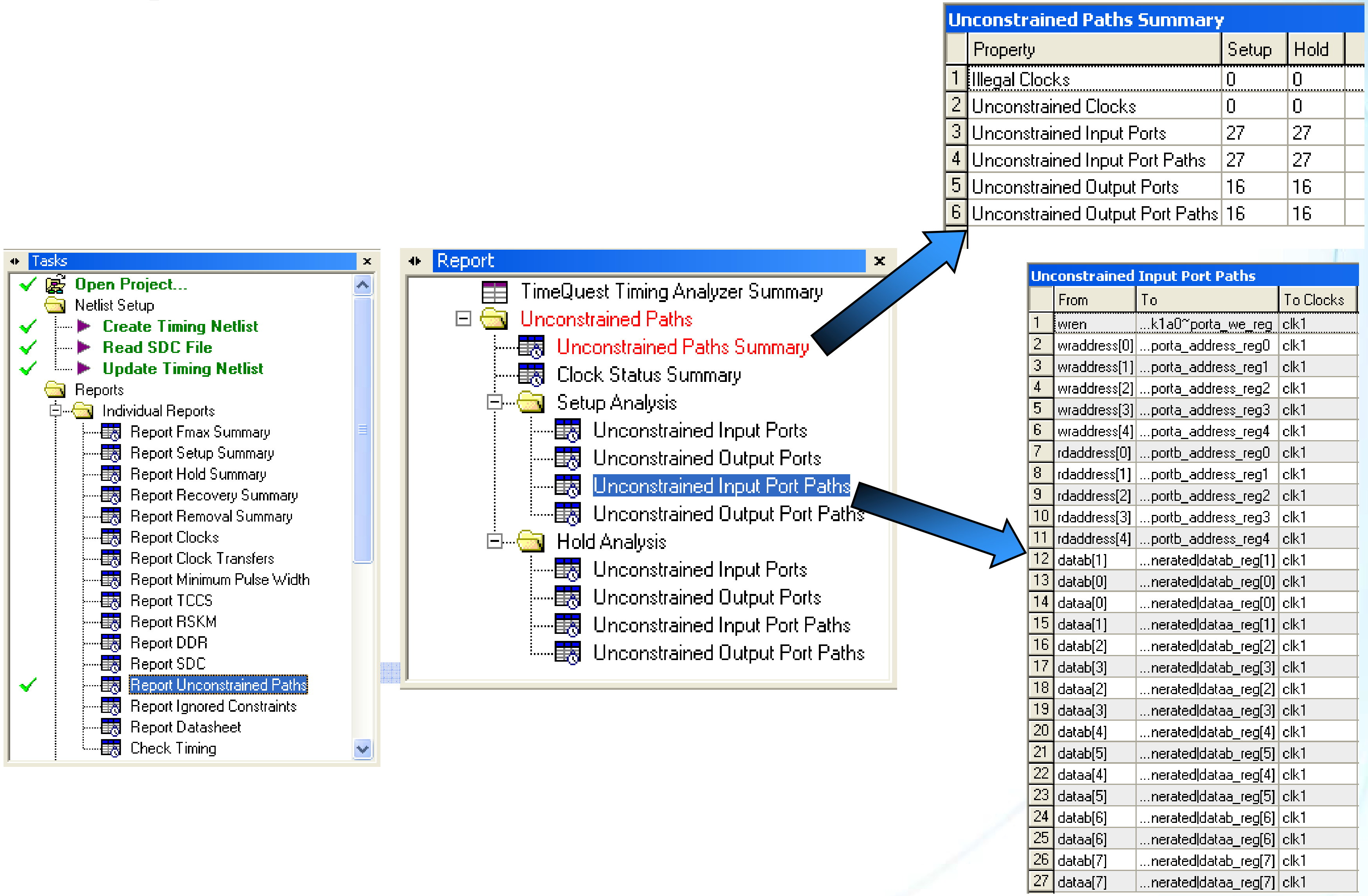
- ✓ Open Project...
- Netlist Setup
  - ✓ Create Timing Netlist
  - ✓ Read SDC File
  - ✓ Update Timing Netlist
- Reports
  - Individual Reports
    - Report Fmax Summary
    - Report Setup Summary
    - Report Hold Summary
    - Report Recovery Summary
    - Report Removal Summary
    - ✓ Report Clocks
    - Report Clock Transfers
    - Report Minimum Pulse Width



Clocks Summary

	Clock Name	Type	Period	Frequency	Rise	Fall
1	clk	Base	4.000	250.0 MHz	0.000	2.000
2	clk_int	Generated	4.000	250.0 MHz	0.000	2.000
3	clk_out	Generated	4.000	250.0 MHz	0.000	2.000

Report Unconstrained Paths



Tasks

- ✓ Open Project...
- Netlist Setup
  - ✓ Create Timing Netlist
  - ✓ Read SDC File
  - ✓ Update Timing Netlist
- Reports
  - Individual Reports
    - Report Fmax Summary
    - Report Setup Summary
    - Report Hold Summary
    - Report Recovery Summary
    - Report Removal Summary
    - Report Clocks
    - Report Clock Transfers
    - Report Minimum Pulse Width
    - Report TCCS
    - Report RSKM
    - Report DDR
    - Report SDC
    - ✓ Report Unconstrained Paths
    - Report Ignored Constraints
    - Report Datasheet
    - Check Timing

Report

- TimeQuest Timing Analyzer Summary
- Unconstrained Paths
  - Unconstrained Paths Summary
  - Clock Status Summary
  - Setup Analysis
    - Unconstrained Input Ports
    - Unconstrained Output Ports
    - Unconstrained Input Port Paths
    - Unconstrained Output Port Paths
  - Hold Analysis
    - Unconstrained Input Ports
    - Unconstrained Output Ports
    - Unconstrained Input Port Paths
    - Unconstrained Output Port Paths

Unconstrained Paths Summary

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	27	27
4	Unconstrained Input Port Paths	27	27
5	Unconstrained Output Ports	16	16
6	Unconstrained Output Port Paths	16	16

Unconstrained Input Port Paths

	From	To	To Clocks
1	wren	...k1a0~porta_we_reg	clk1
2	wraddress[0]	...porta_address_reg0	clk1
3	wraddress[1]	...porta_address_reg1	clk1
4	wraddress[2]	...porta_address_reg2	clk1
5	wraddress[3]	...porta_address_reg3	clk1
6	wraddress[4]	...porta_address_reg4	clk1
7	rdaddress[0]	...portb_address_reg0	clk1
8	rdaddress[1]	...portb_address_reg1	clk1
9	rdaddress[2]	...portb_address_reg2	clk1
10	rdaddress[3]	...portb_address_reg3	clk1
11	rdaddress[4]	...portb_address_reg4	clk1
12	datab[1]	...nerated|datab_reg[1]	clk1
13	datab[0]	...nerated|datab_reg[0]	clk1
14	dataa[0]	...nerated|dataa_reg[0]	clk1
15	dataa[1]	...nerated|dataa_reg[1]	clk1
16	datab[2]	...nerated|datab_reg[2]	clk1
17	datab[3]	...nerated|datab_reg[3]	clk1
18	dataa[2]	...nerated|dataa_reg[2]	clk1
19	dataa[3]	...nerated|dataa_reg[3]	clk1
20	datab[4]	...nerated|datab_reg[4]	clk1
21	datab[5]	...nerated|datab_reg[5]	clk1
22	dataa[4]	...nerated|dataa_reg[4]	clk1
23	dataa[5]	...nerated|dataa_reg[5]	clk1
24	datab[6]	...nerated|datab_reg[6]	clk1
25	dataa[6]	...nerated|dataa_reg[6]	clk1
26	datab[7]	...nerated|datab_reg[7]	clk1
27	dataa[7]	...nerated|dataa_reg[7]	clk1

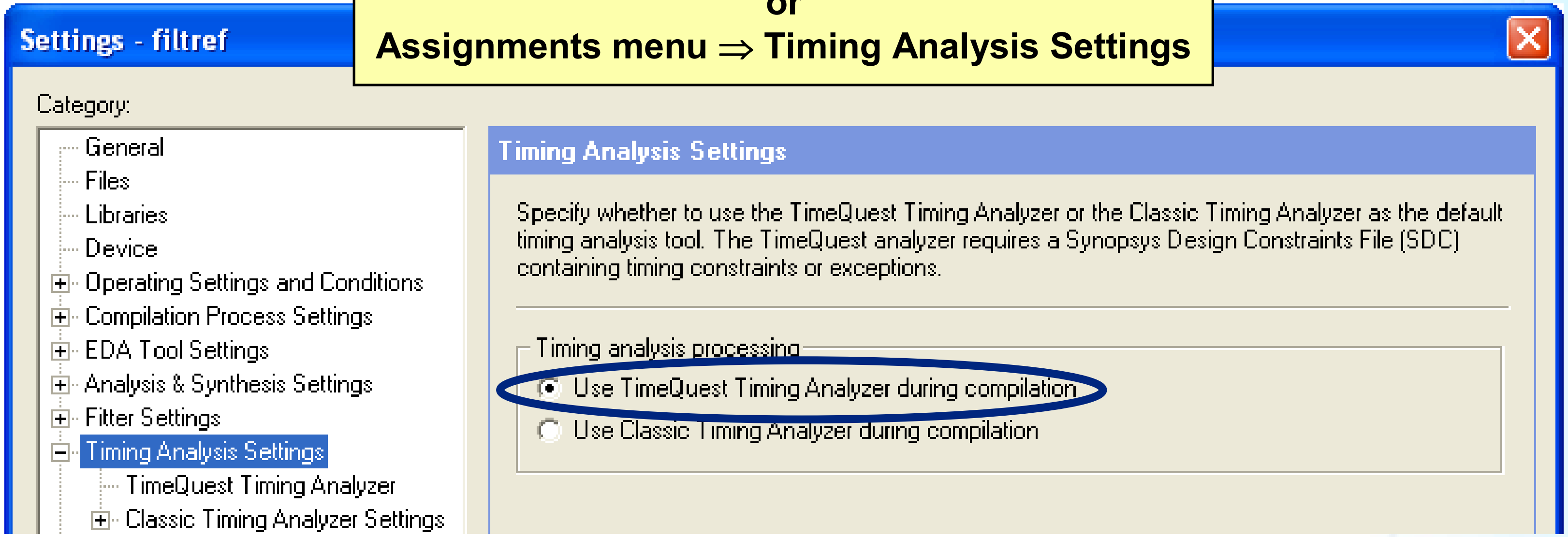
Compare Path Details

- List critical path in Classic analyzer
- Report timing on same path in TimeQuest analyzer
- Are slack values the same?
- Are source and destination clocks the same?
- Compare TimeQuest launch/latch time to Classic setup/hold relationship
  - TimeQuest launch/latch times are absolute
  - Classic launch/latch times are relative (launch is usually 0)
- Are clock latency values the same?

Switch to TimeQuest Timing Analyzer

- By default, Quartus II software uses Classic timing analyzer
  - Exceptions: all Arria GX projects and new Stratix III and Cyclone III projects
  - Timing assignments in QSF
- Change setting to use TimeQuest timing analyzer
  - Timing constraints in SDC file

Turn On TimeQuest Timing Analyzer



Assignments menu ⇒ Settings
or
Assignments menu ⇒ Timing Analysis Settings

Settings - filtref
Category:
General
Files
Libraries
Device
Operating Settings and Conditions
Compilation Process Settings
EDA Tool Settings
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
TimeQuest Timing Analyzer
Classic Timing Analyzer Settings
Timing Analysis Settings

Specify whether to use the TimeQuest Timing Analyzer or the Classic Timing Analyzer as the default timing analysis tool. The TimeQuest analyzer requires a Synopsys Design Constraints File (SDC) containing timing constraints or exceptions.

Timing analysis processing

● Use TimeQuest Timing Analyzer during compilation

○ Use Classic Timing Analyzer during compilation

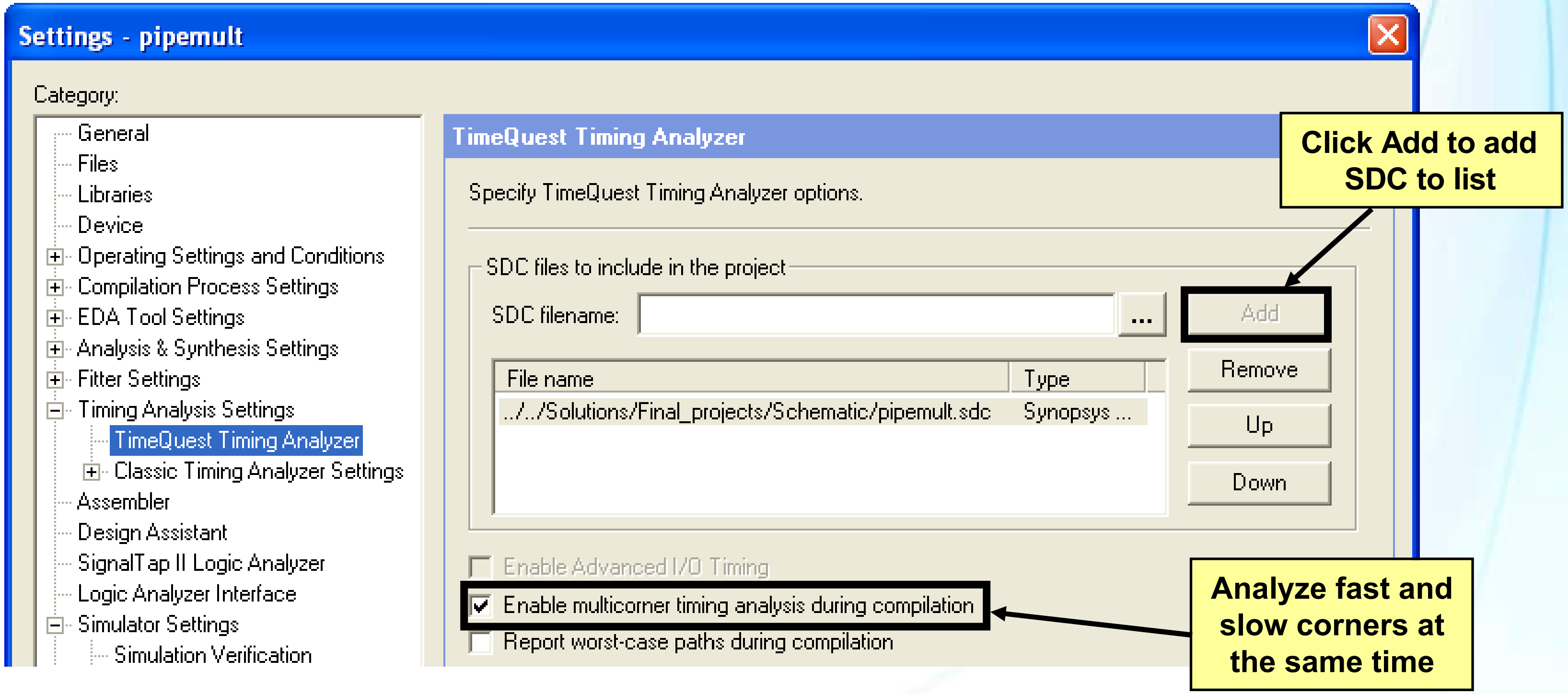
- Use GUI or add assignment to QSF file:

```
set_global_assignment -name USE_TIMEQUEST_TIMING_ANALYZER ON
```

- Switch on a per-project basis

Add SDC File(s) & Other Settings

- May want to manually add converted SDC file or other SDC files to project
- Multicorner analysis checks and compiles for all process corners in one analysis/compilation
  - On by default for Cyclone II & III, Stratix II & III devices



Settings - pipemult

Category:

- General
- Files
- Libraries
- Device
- ⊞ Operating Settings and Conditions
- ⊞ Compilation Process Settings
- ⊞ EDA Tool Settings
- ⊞ Analysis & Synthesis Settings
- ⊞ Fitter Settings
- ⊟ Timing Analysis Settings
  - TimeQuest Timing Analyzer
  - ⊞ Classic Timing Analyzer Settings
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- ⊟ Simulator Settings
  - Simulation Verification

TimeQuest Timing Analyzer

Specify TimeQuest Timing Analyzer options.

SDC files to include in the project

SDC filename: ...

File name	Type
../../Solutions/Final_projects/Schematic/pipemult.sdc	Synopsys ...

□ Enable Advanced I/O Timing

☑ Enable multicorner timing analysis during compilation

□ Report worst-case paths during compilation

Click Add to add SDC to list

Analyze fast and slow corners at the same time

Switch is Complete!

- Future compilations use constraints in SDC file(s)
- Perform timing analysis with TimeQuest tools

Switching to TimeQuest Summary

- Classic and TimeQuest timing analyzers behave differently
  - TimeQuest analysis more pessimistic
  - TimeQuest reporting on-demand
- Recommended process to convert to TimeQuest analyzer
- Review SDC file created by conversion utility

References

- Volume 3 of the Quartus II Handbook
  - Chapter 6: TimeQuest Timing Analyzer
  - Chapter 7: Switching to the TimeQuest Timing Analyzer
- SDC and TimeQuest API Reference Manual
- Online Training
  - TimeQuest Timing Analyzer

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With Altera's instructor-led training courses, you can:

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- Quartus II Software Design Series: Foundation
  - Project creation and management
  - Design entry methods and tools
  - Compilation and compilation results analysis
  - Creating and editing settings and assignments
  - I/O planning and management
  - **Introduction to timing analysis with TimeQuest Timing Analyzer**

- Quartus II Software Design Series: Verification
  - Basic design simulation with ModelSim®-Altera simulator
  - Power analysis
  - Device programming and configuration
  - Debugging solutions

- **Quartus II Software Design Series: Timing Analysis**
  - **Create timing constraints to meet and optimize timing**
  - **Perform detailed timing analysis on an Altera device**

- Quartus II Software Design Series: Optimization
  - Incremental compilation
  - Quartus II optimization features & techniques

Altera Technical Support

- Reference Quartus II software on-line help
- Quartus II Handbook
- Consult Altera applications (factory applications engineers)
  - MySupport: http://www.altera.com/mysupport
  - Hotline: (800) 800-EPLD (7:00 a.m. - 5:00 p.m. PST)
- Field applications engineers: contact your local Altera sales office
- Receive literature by mail: (888) 3-ALTERA
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