PowerPlay Power Analyzer

Altera Asia Pacific Regional Support Center

Agenda

- Power Fundamentals
- Power Analysis Flow
- Hierarchical Estimation
- User Interface
- Reporting
- Estimation Accuracy
- Conclusion

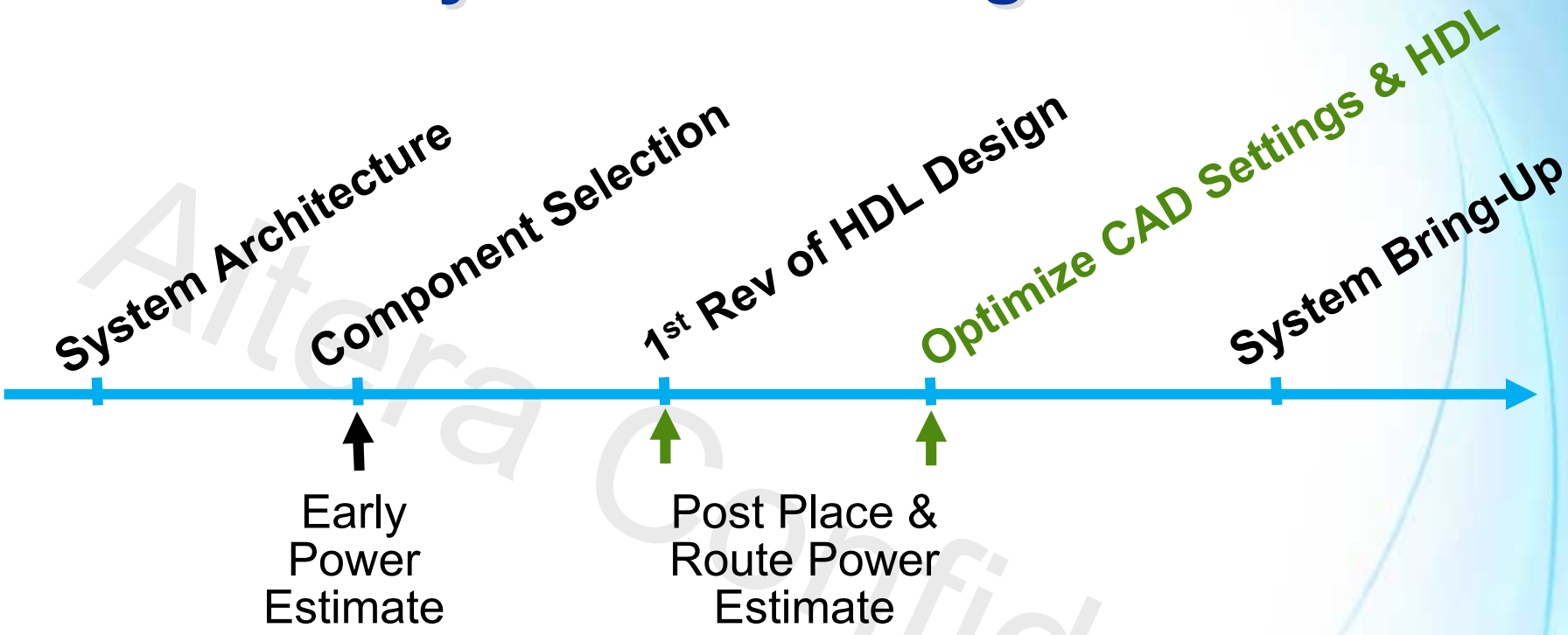
Power Fundamentals

- Total Power made up of 3 Components:
  - Core Static Power
  - Core Dynamic Power
  - I/O Power
- Core Static Power
  - Power drawn by device even when the clocks are stopped
  - Leakage current is main component
- Core Dynamic Power
  - Increases Linearly (or close to linearly) with clock Frequency
  - Power due to Charging and Discharging of Capacitance of Routing Wires and logic resources (LEs/ALMs).
- I/O Power
  - Also includes static power and dynamic power

Power Analysis

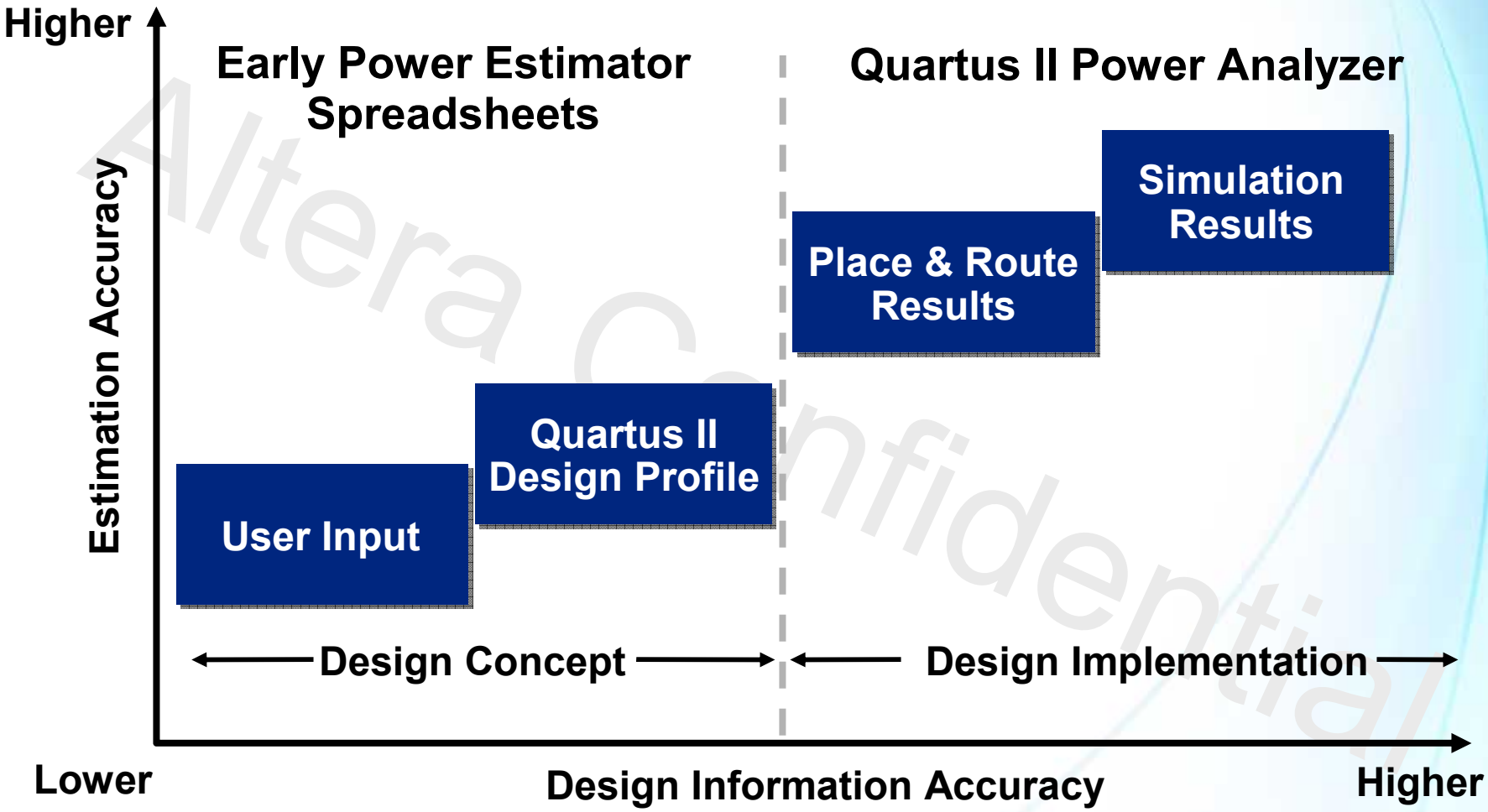
- Successful Power Estimation requires accurate power models and thorough operation condition specifications
  - Specifications apply to maximum static power
- Altera PowerPlay Power Analyzer
  - Accurate power models
  - Easy-to-use power analysis tools

Power Analysis in the Design Process



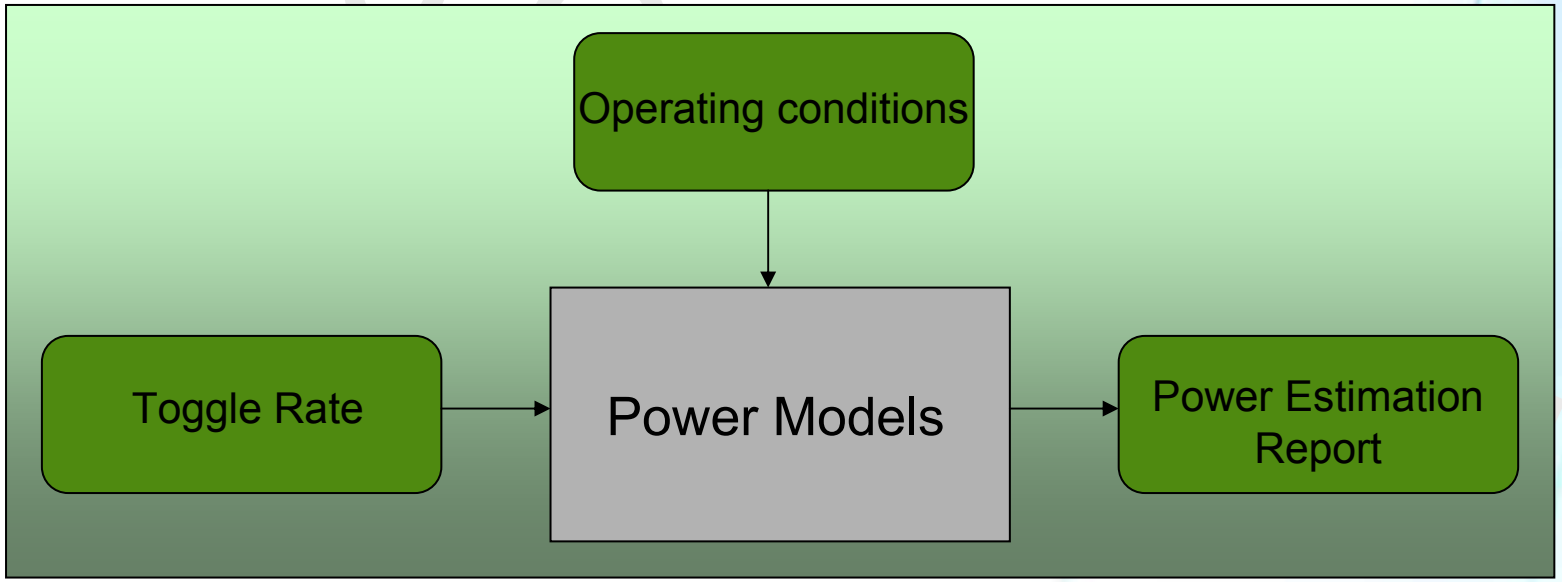
- Accurate power estimates & analysis allow
  - FPGA CAD software to optimize design power
  - Design decisions that reduce power

PowerPlay Power Estimation Tools



Successful Power Analysis

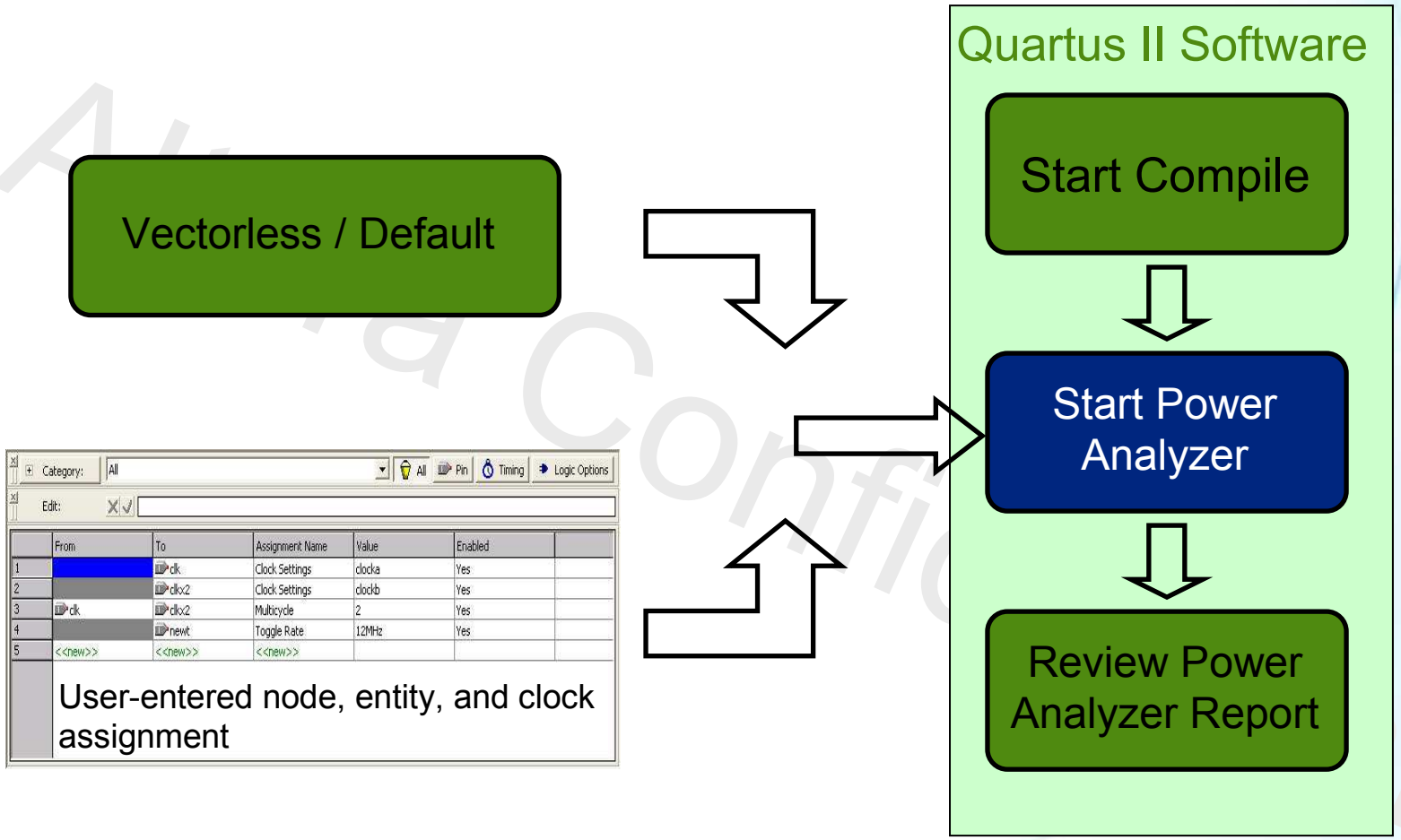
- Three required parts to high accuracy Power Estimation
  1. Accurate Toggle Rate data on each node (internal and external)
  2. Accurate Power Models of FPGA architecture
  3. Knowledge of actual device Operating Conditions
- Detailed Power Estimation Report available for analysis



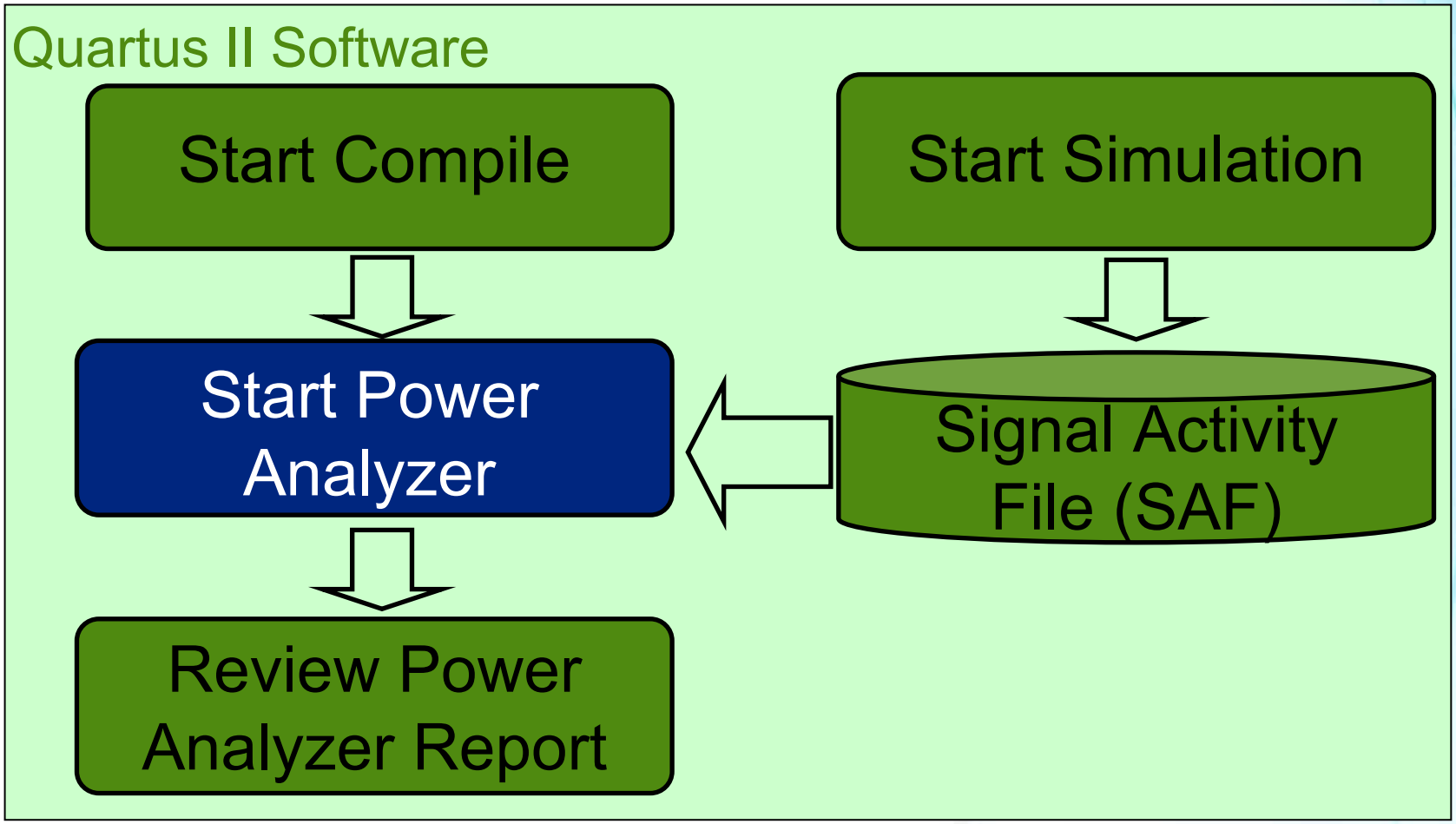
Power Analyzer Flow

- Different Power Analyzer Flows are available
  - User-Entry and Vectorless Estimation
  - Quartus II Simulator
  - 3rd-Party Simulation
  - Mix & Match
- Depends on stage of design process, availability of data

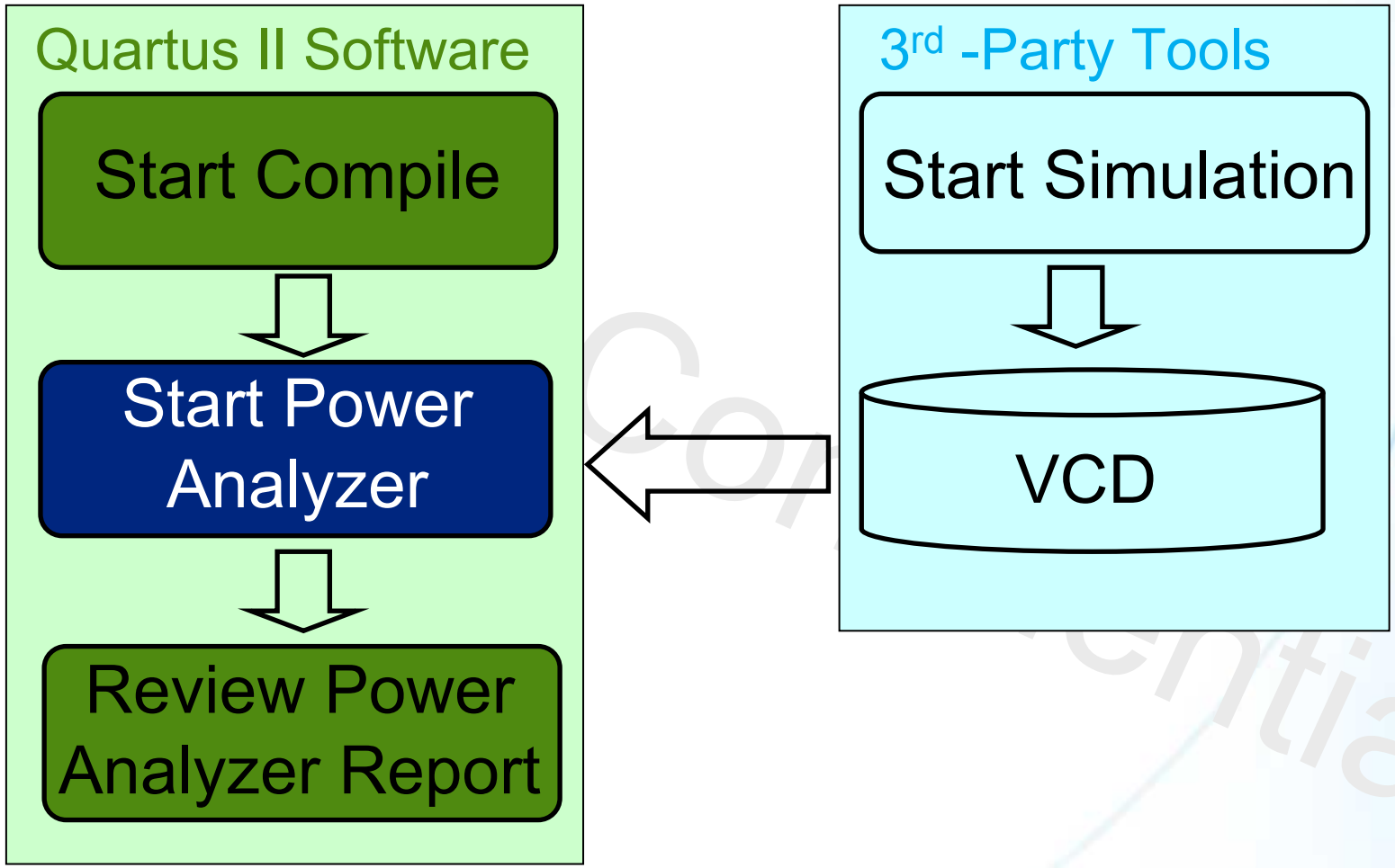
User-Entry and Vectorless Estimation



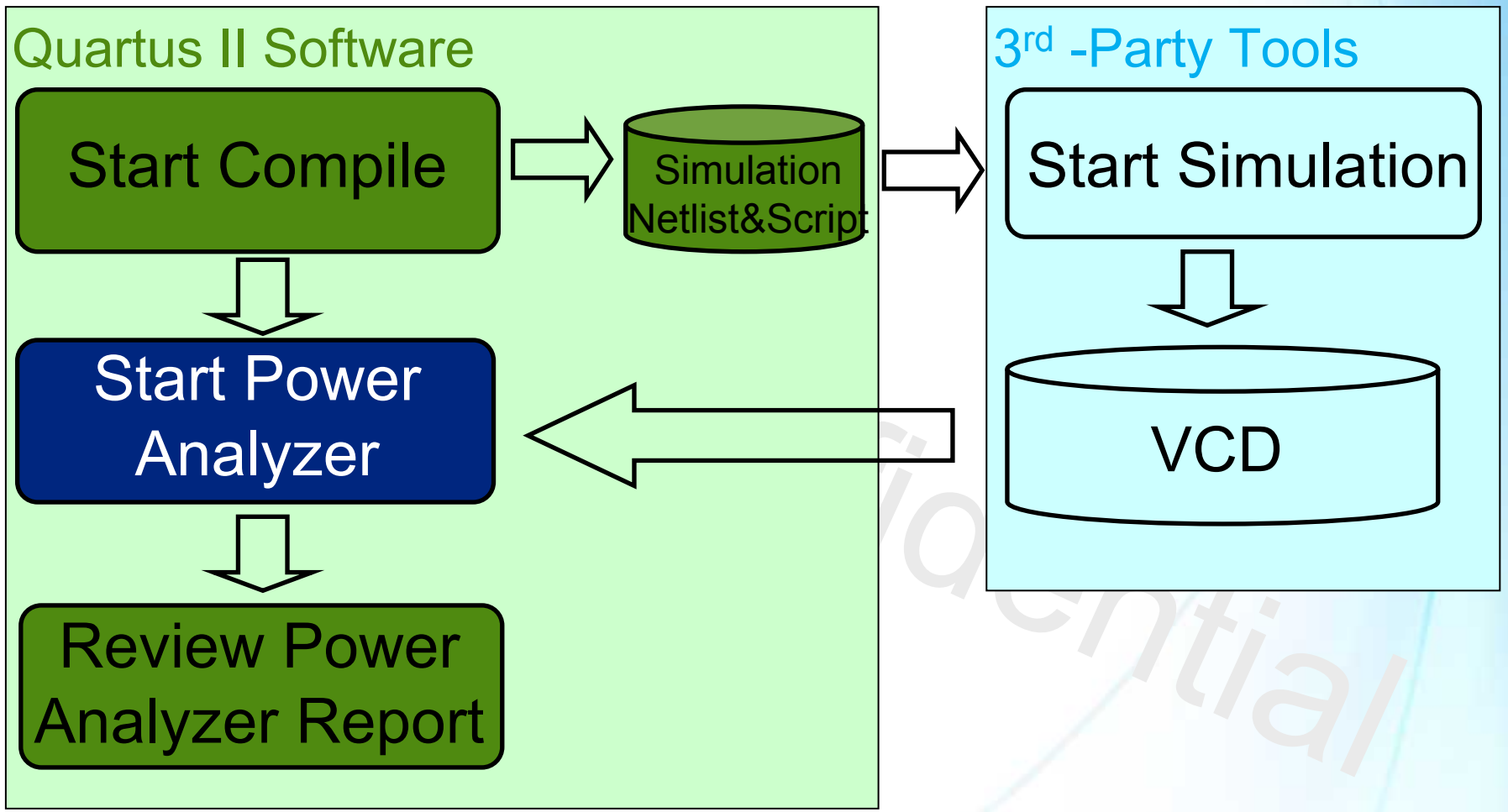
Quartus II Simulator



3rd-Party Simulation (RTL)

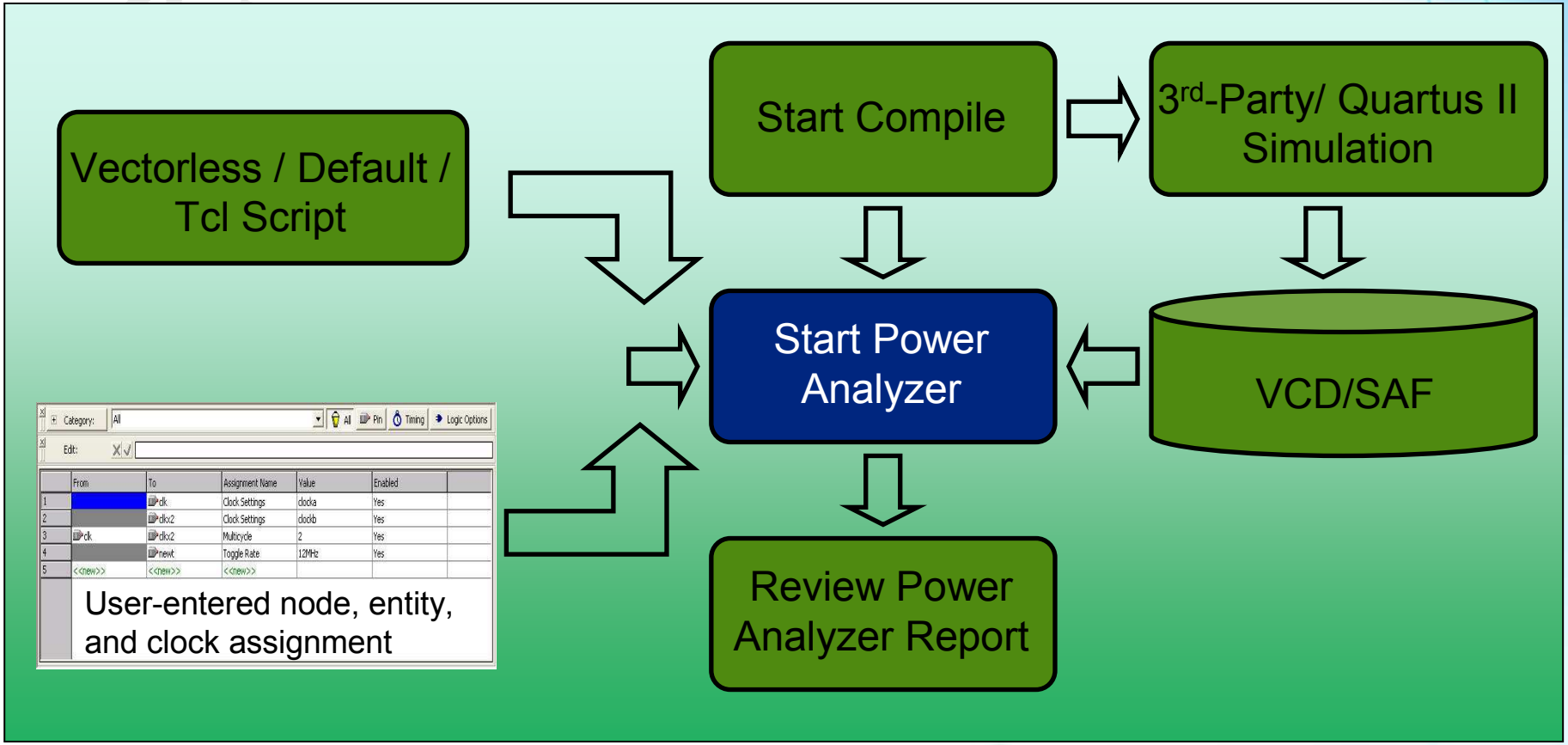


3rd-Party Simulation (Gate-Level)



Mix & Match Flow

- Simulation & User-Entered Activity Rate



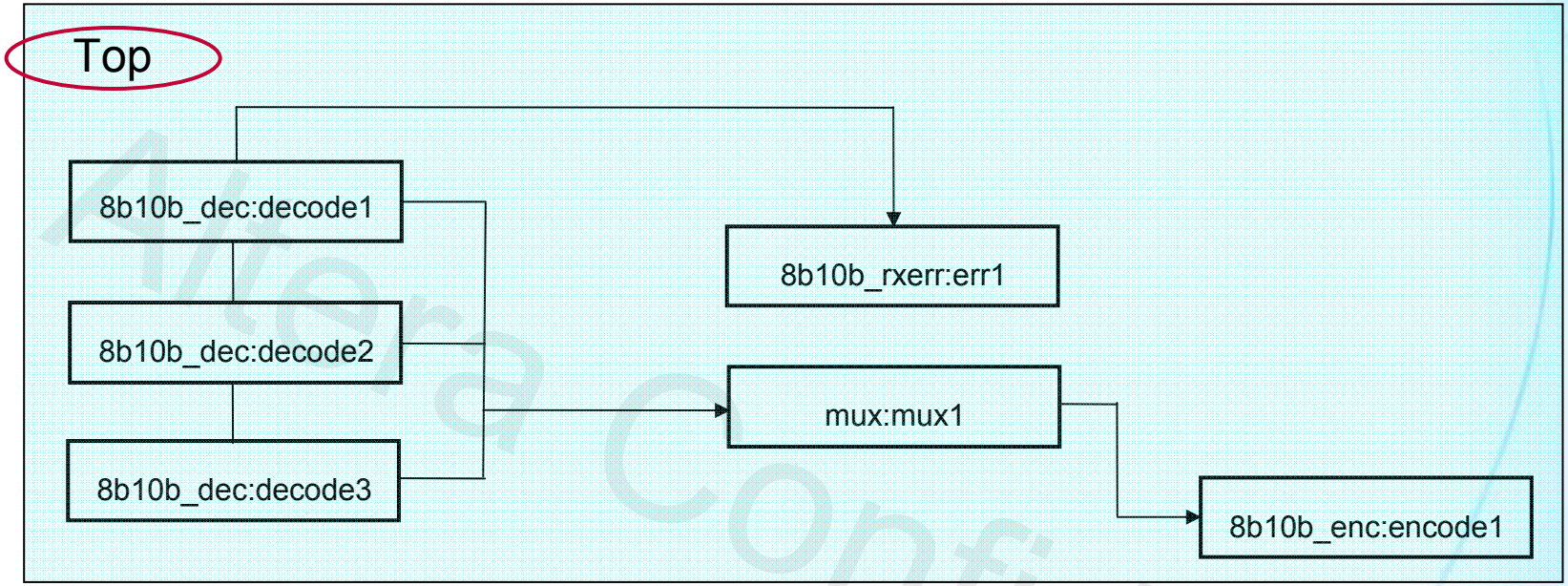
Multiple Simulation Files Supported

- Multiple simulation files supported in Power Analyzer
  - Combine VCD and SAF by instance hierarchy
- Benefits
  - Re-use of simulations out files in hierarchy design flow
  - Accurate power estimation results
  - Flexibility and control
  - Ease of use

Hierarchical Estimation

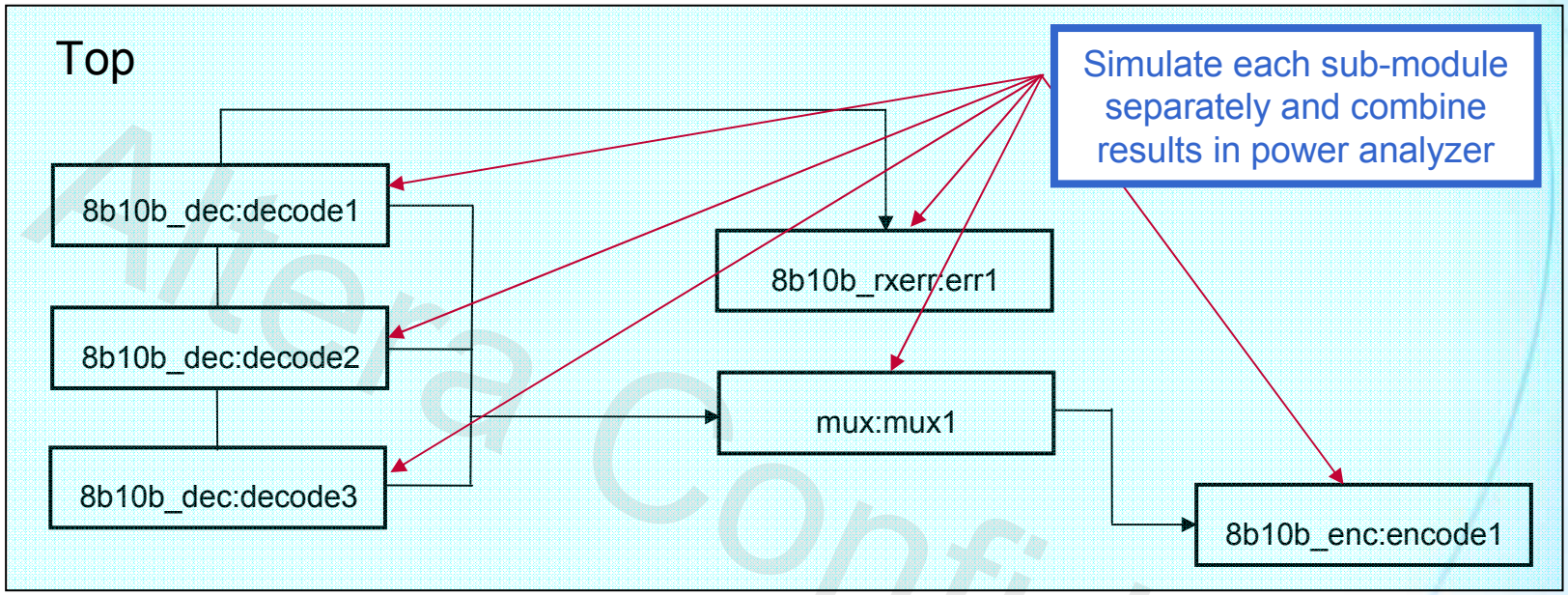
- Usage scenarios
  - Complete Design Estimation
  - Hierarchical Design Estimation
  - Multiple Estimations on the Same Entity
  - Overlapping Estimation
  - Partial Estimation

Complete Design Estimation



File Name (Power analyzer Input files)	Entity
full_design.vcd	Top

Hierarchical Design Estimation



File Name (Power analyzer Input files)	Entity
8b10b_dec.vcd	Top|8b10b_dec:decode1
8b10b_dec.vcd	Top|8b10b_dec:decode2
8b10b_dec.vcd	Top|8b10b_dec:decode3
8b10b_rxerr.vcd	Top|8b10b_rxerr:err1
mux.saf	Top|mux:mux1
8b10b_enc.vcd	Top|8b10b_enc:encode1

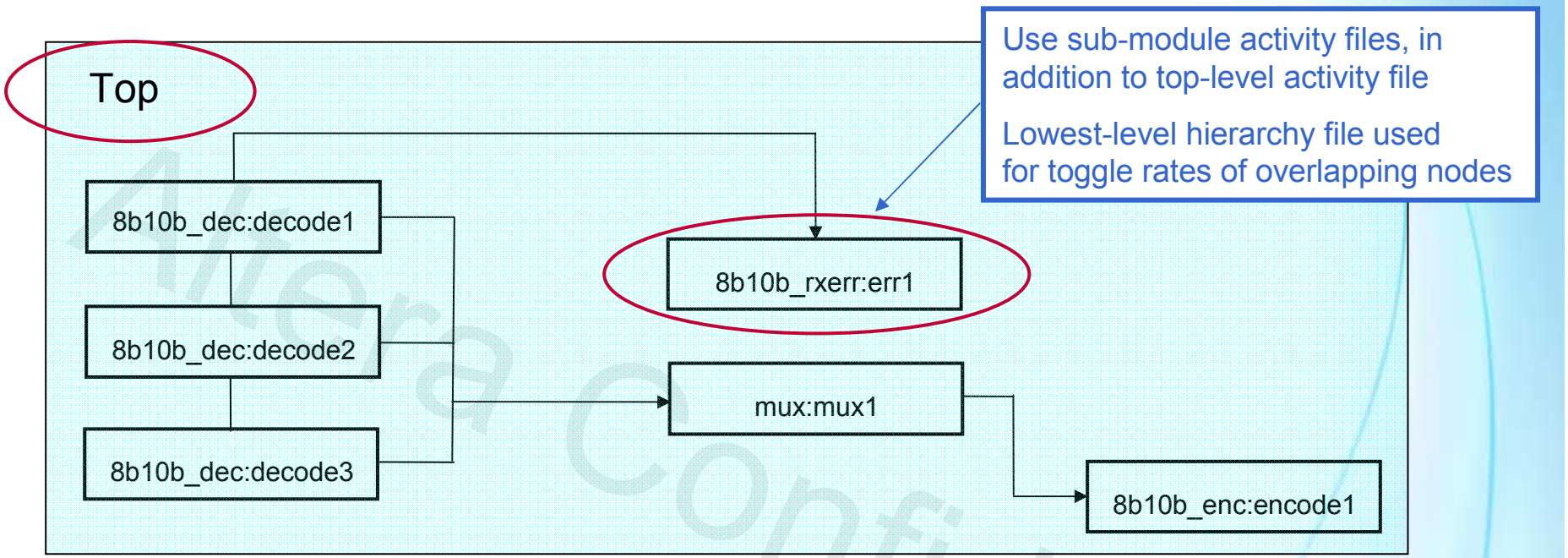
Multiple Estimations on the Same Entity

- Can use multiple simulations of full design or sub-modules
- Power Analyzer employs arithmetic average of toggle rates
  - Using below, err_out toggle rate calculates to 40 toggle/sec

File Name (Power analyzer Input files)	Signal "err_out"
normal.saf	0 toggles/sec
corner1.vcd	50 toggles/sec
corner2.vcd	70 toggles/sec

File Name (Power analyzer Input files)	Entity
normal.saf	Top
corner1.vcd	Top
corner2.vcd	Top

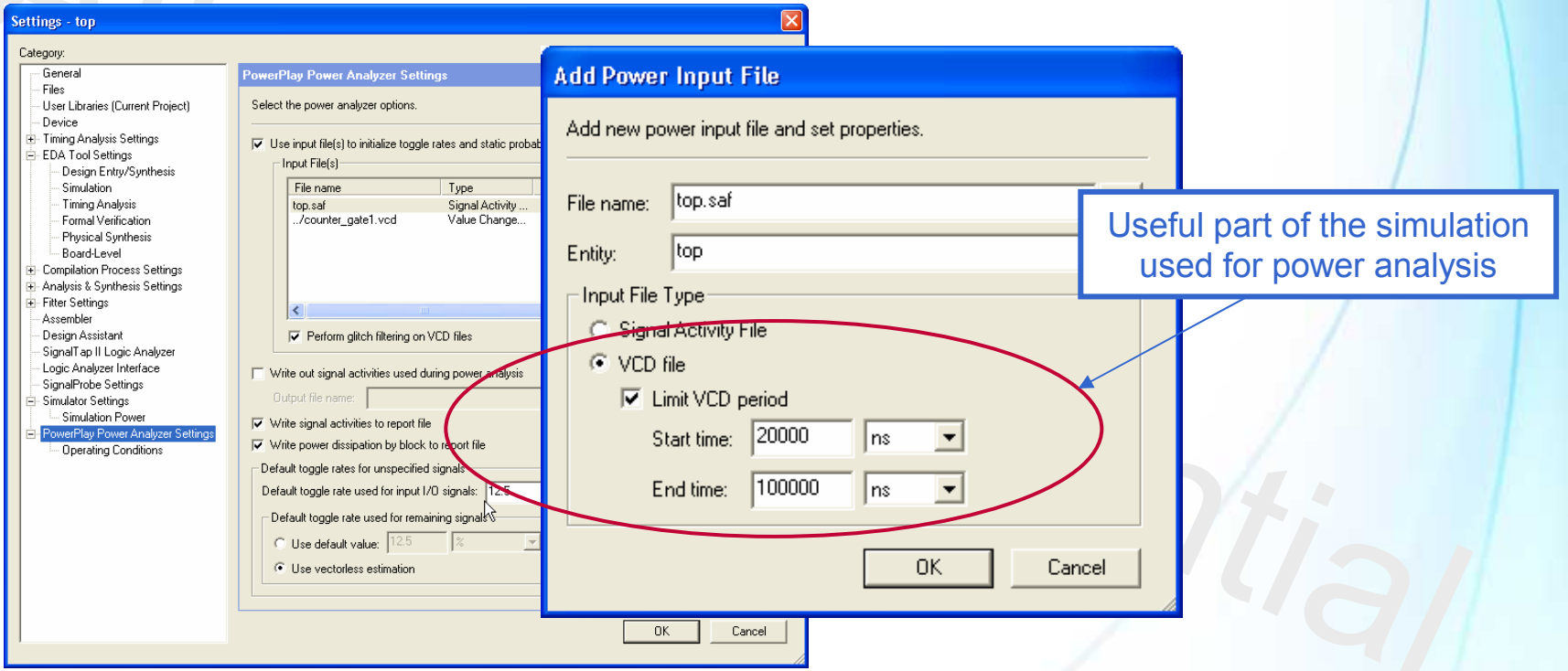
Overlapping Estimation



File Name (Power analyzer Input files)	Entity
full_design.vcd	Top
error_cases.saf	Top|8b10b_rxerr:err1

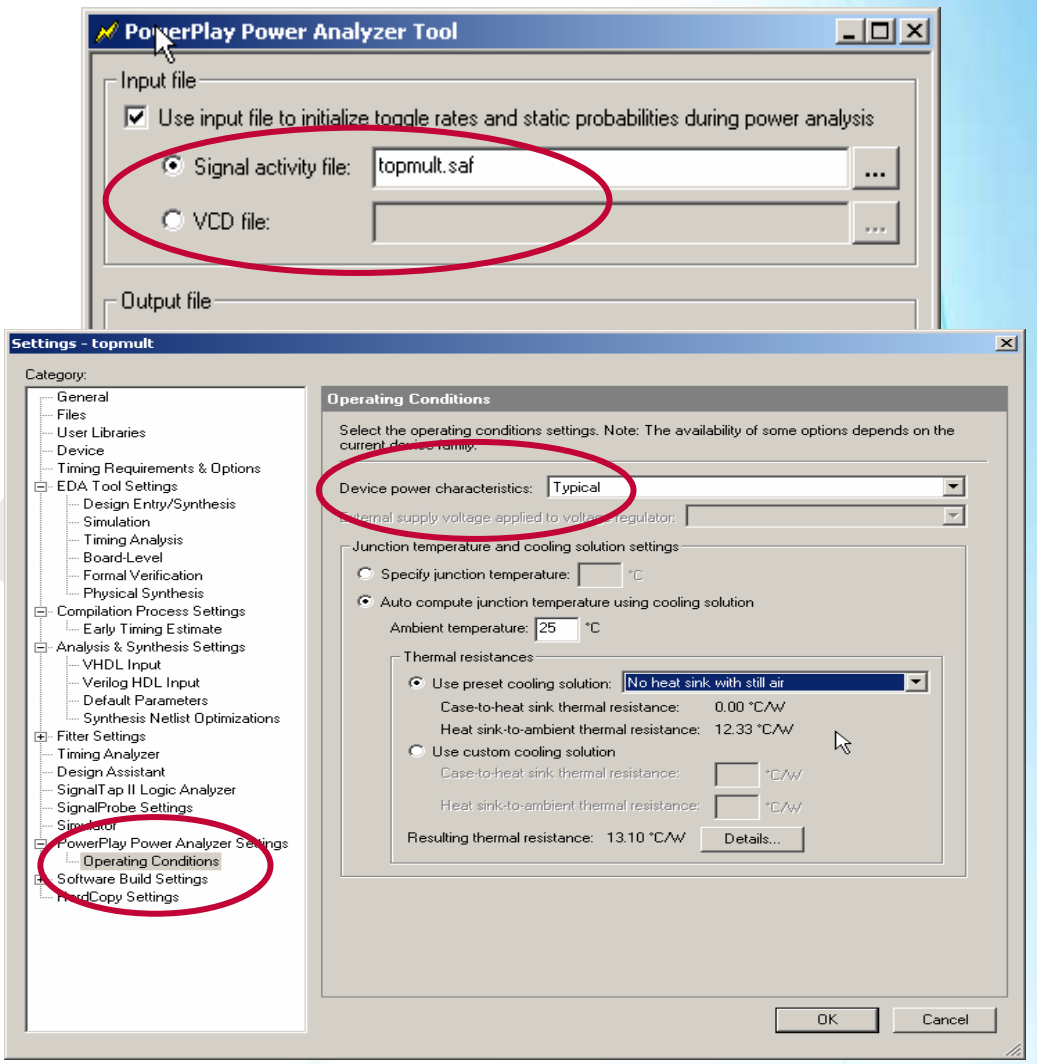
Partial Estimation

- Limit VCD file period for useful part of the simulation
  - Used to bypass long “startup” sequences



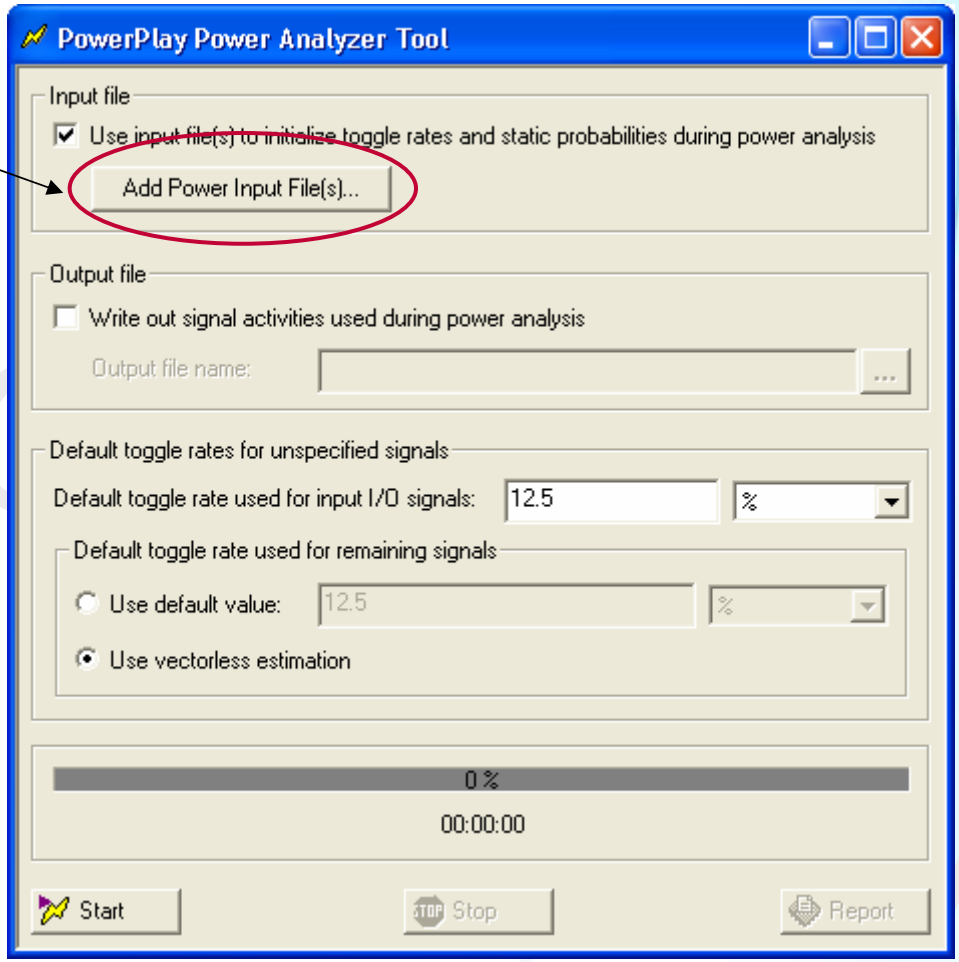
User Interface

- Power Analyzer
  - Processing Menu
- Enter Toggle Rates
  - Signal Activity File
    - From Quartus II Simulator
  - VCD
    - From 3rd-Party Simulators
  - Assignment Editor
  - Unspecified Toggle Rates
    - Default Toggle Rates
    - Vectorless Estimation
- Set Operation Conditions

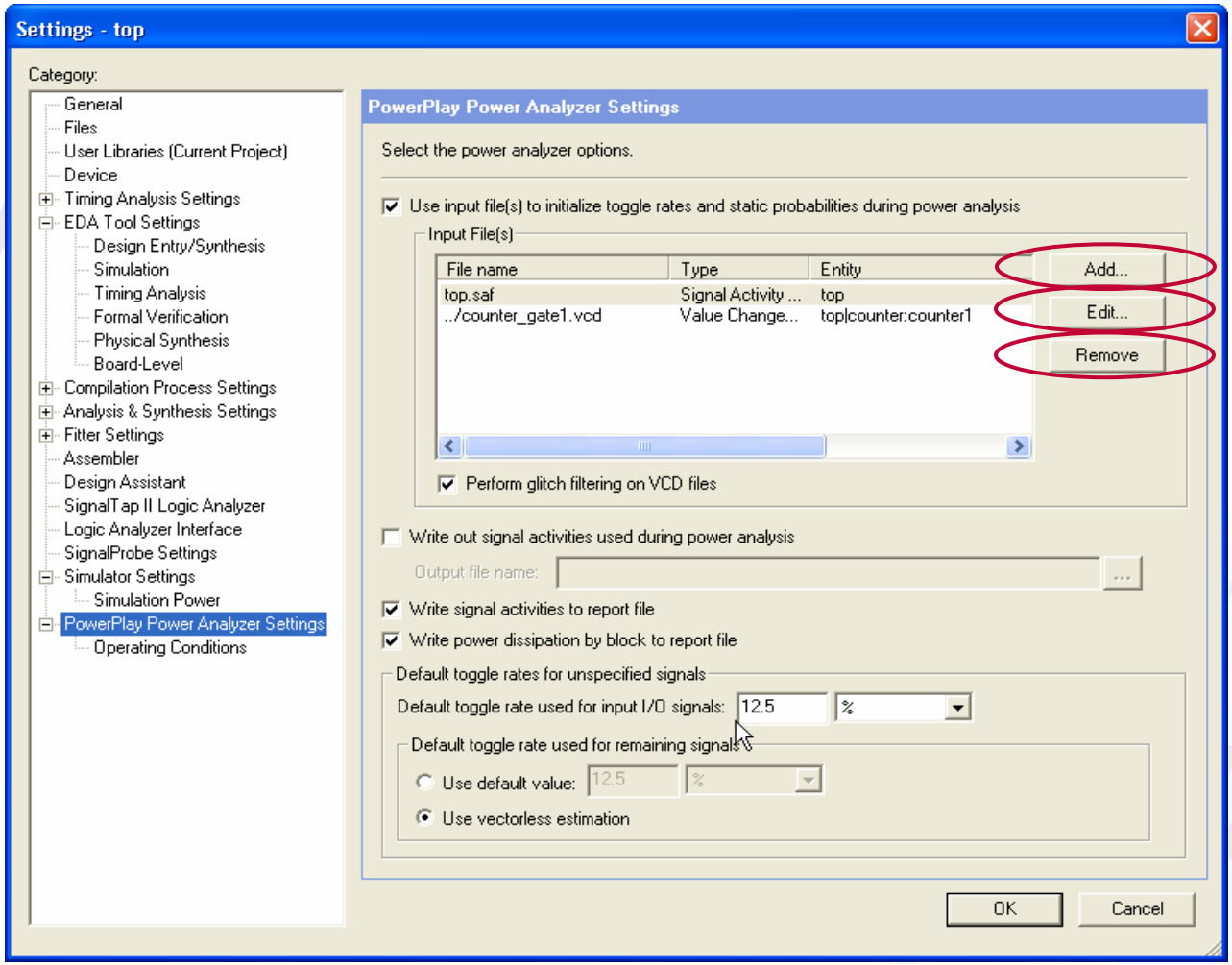


User Interface – Input Files

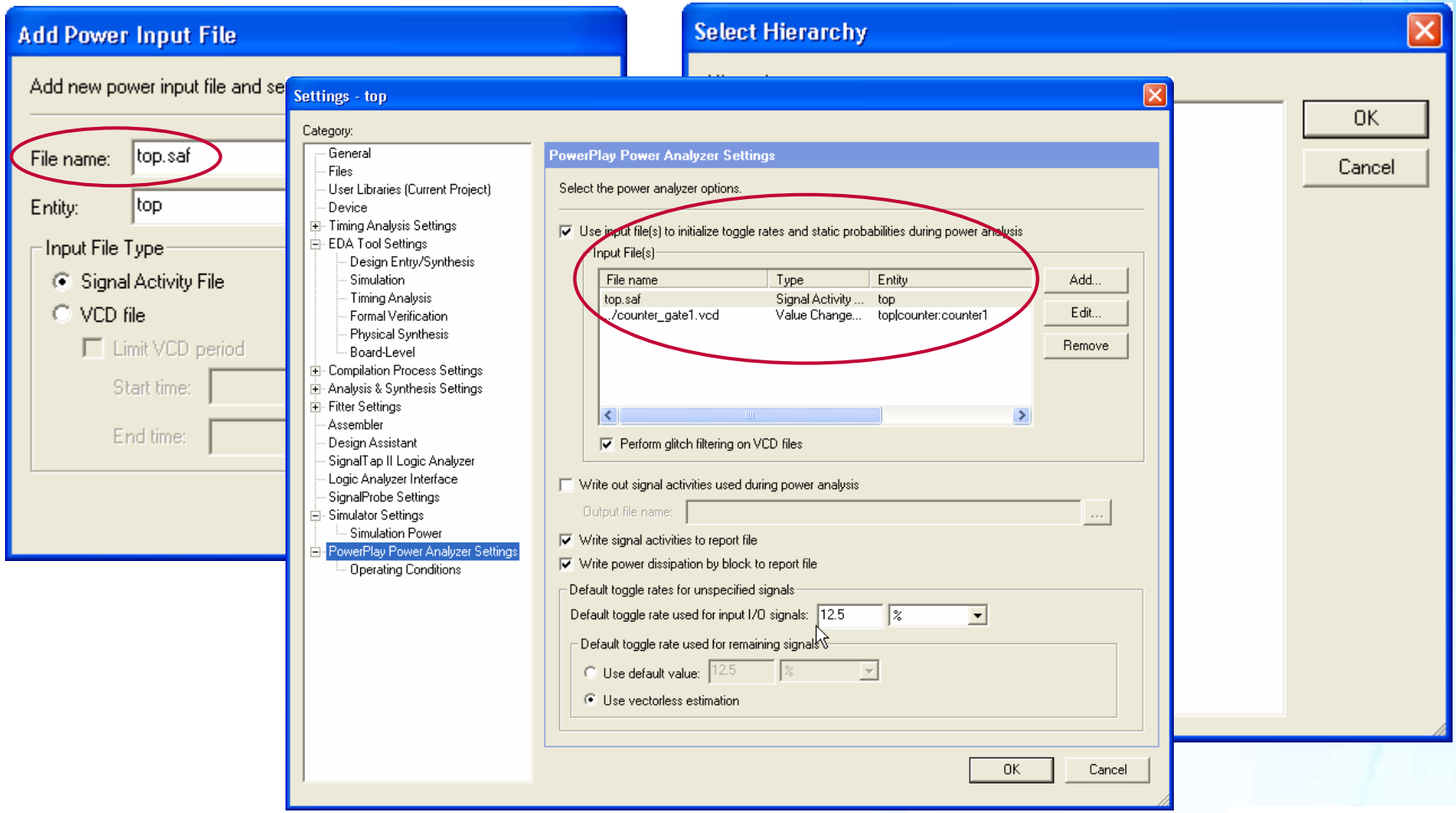
Supports multiple simulation output files



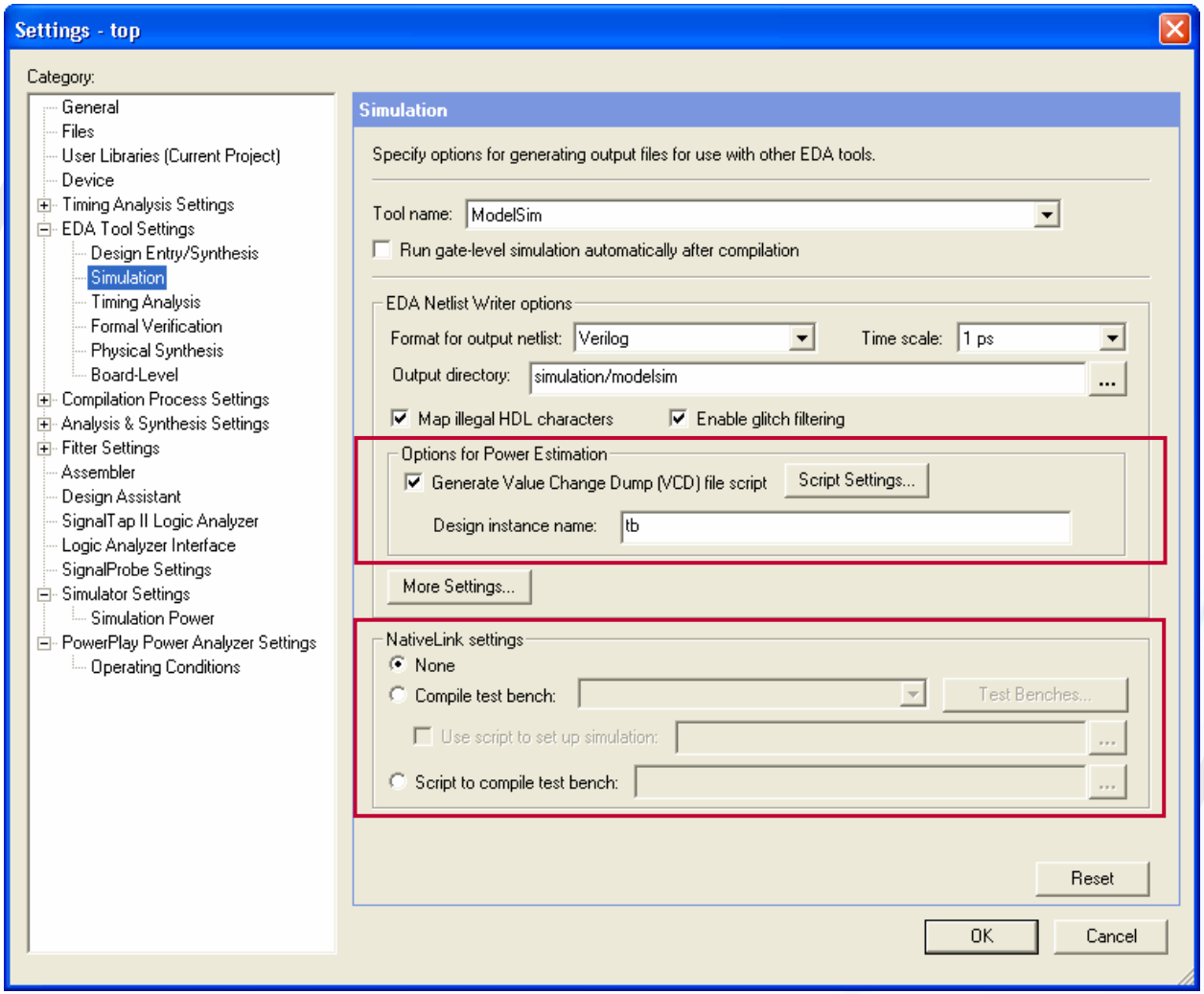
User Interface – Input Files



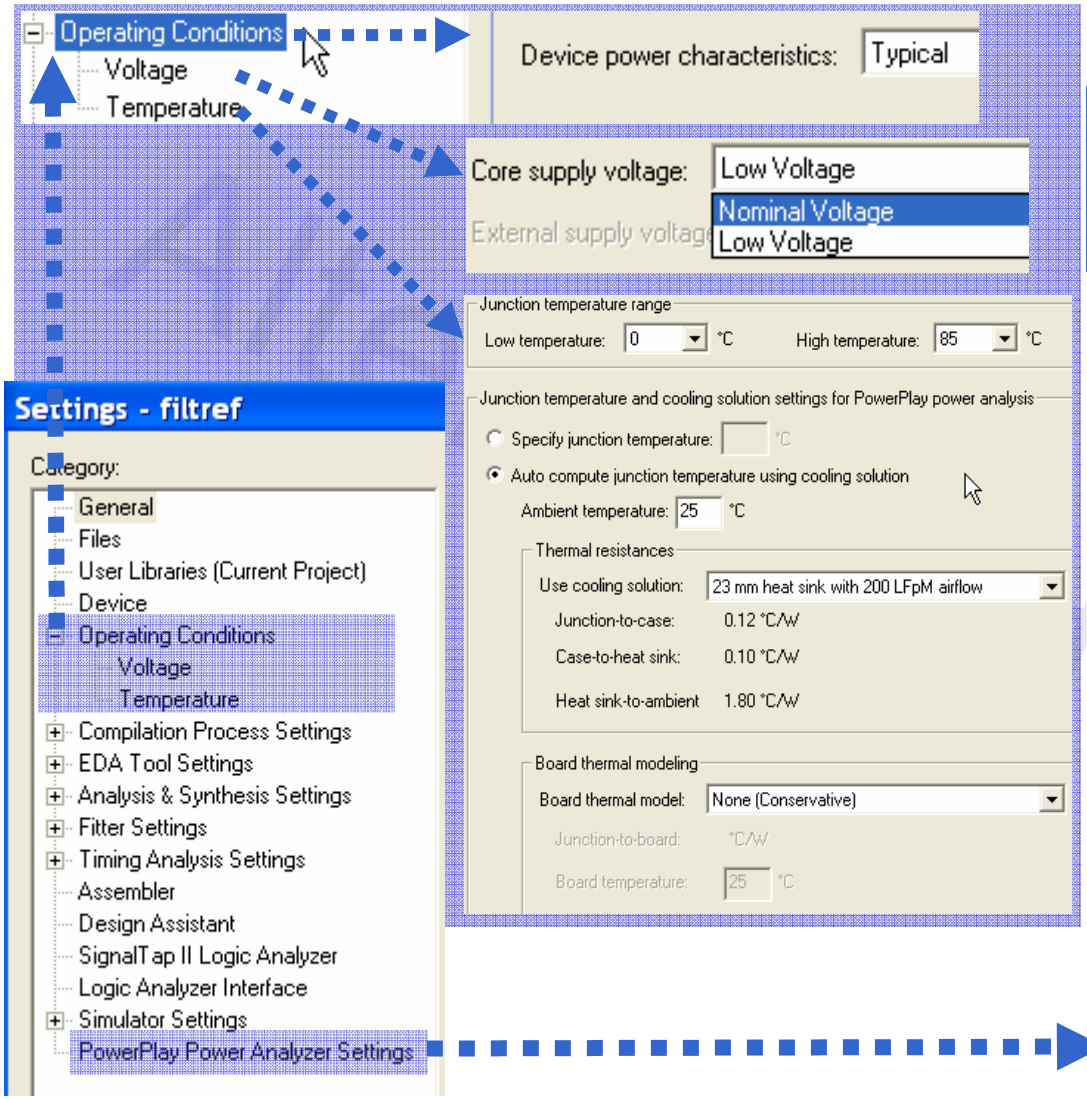
User Interface – Input Files



User Interface – Output Files

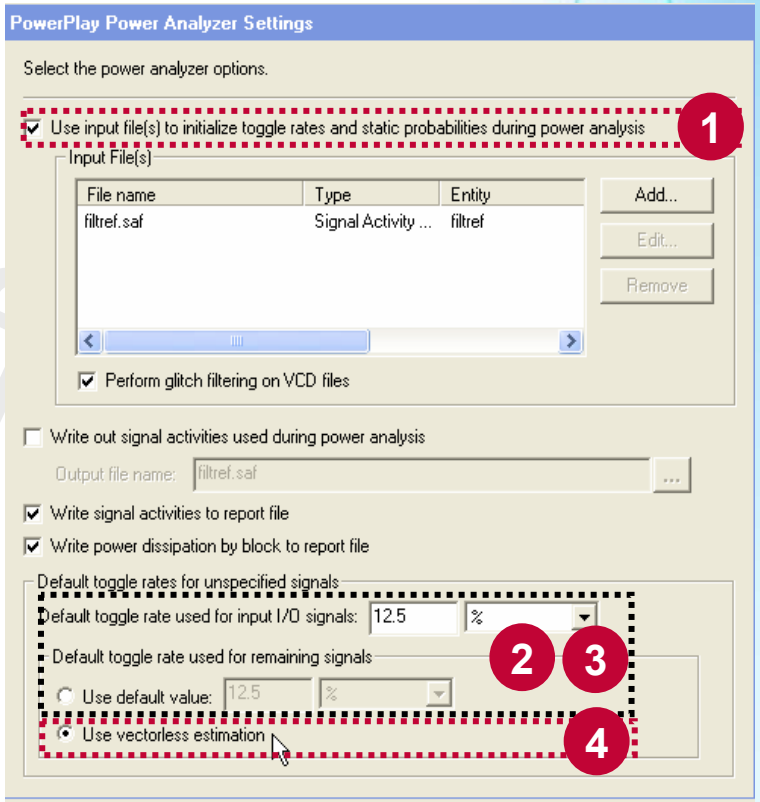


User Interface – Other Settings



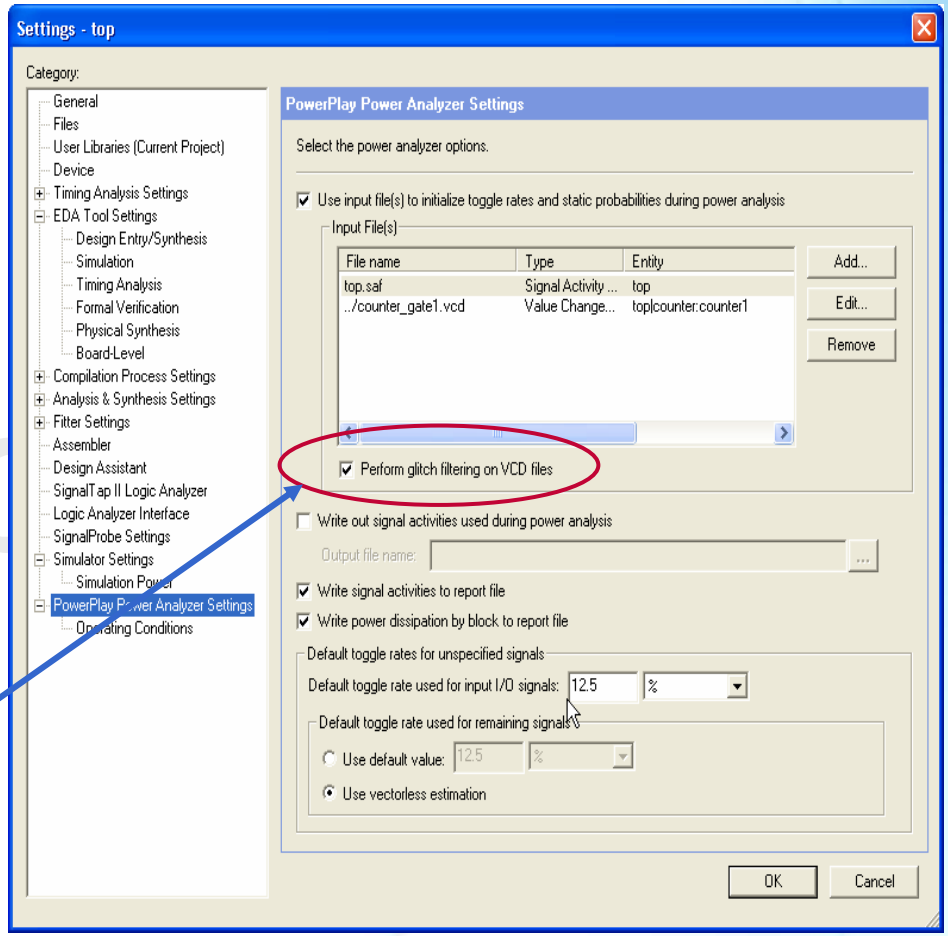
Signal activity levels produced by:

1. Simulation results
2. User-entered node, entity and clock assignment
3. User-entered default toggle rate assignment
4. Vectorless estimation

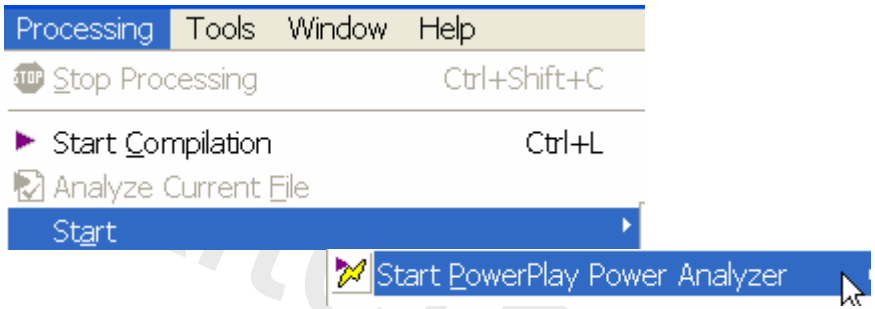


User Interface – Other Settings

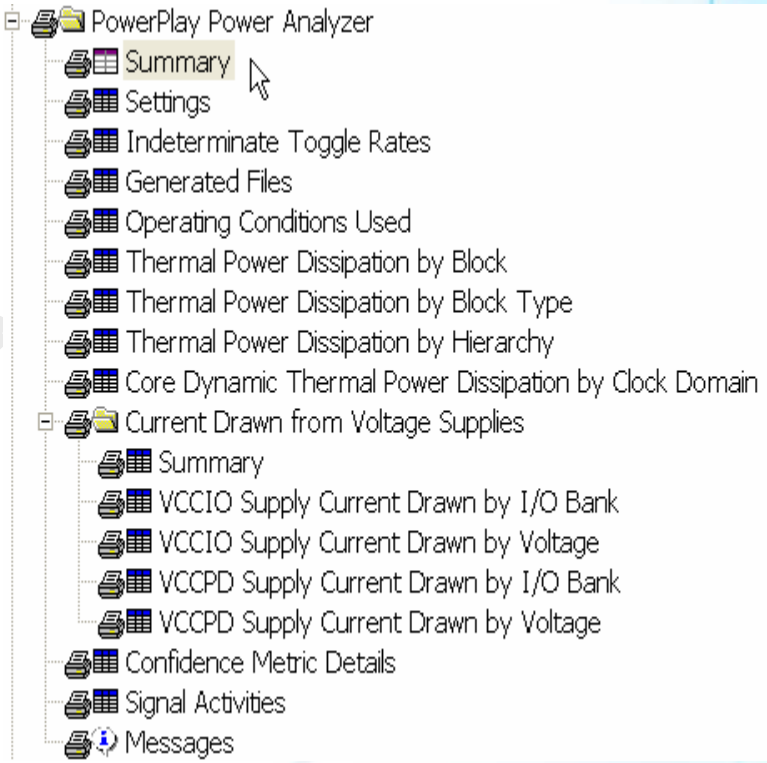
- Some logic produces many transitions/cycle
  - e.g. CRC/parity, multipliers
- 3rd party simulators can provide better glitch filtering than Quartus II
  - 3rd party simulators filter glitches at block outputs and in routing
  - Quartus II filters glitches in routing only
- Enable Glitch filtering



User Interface – Starting the PPPA



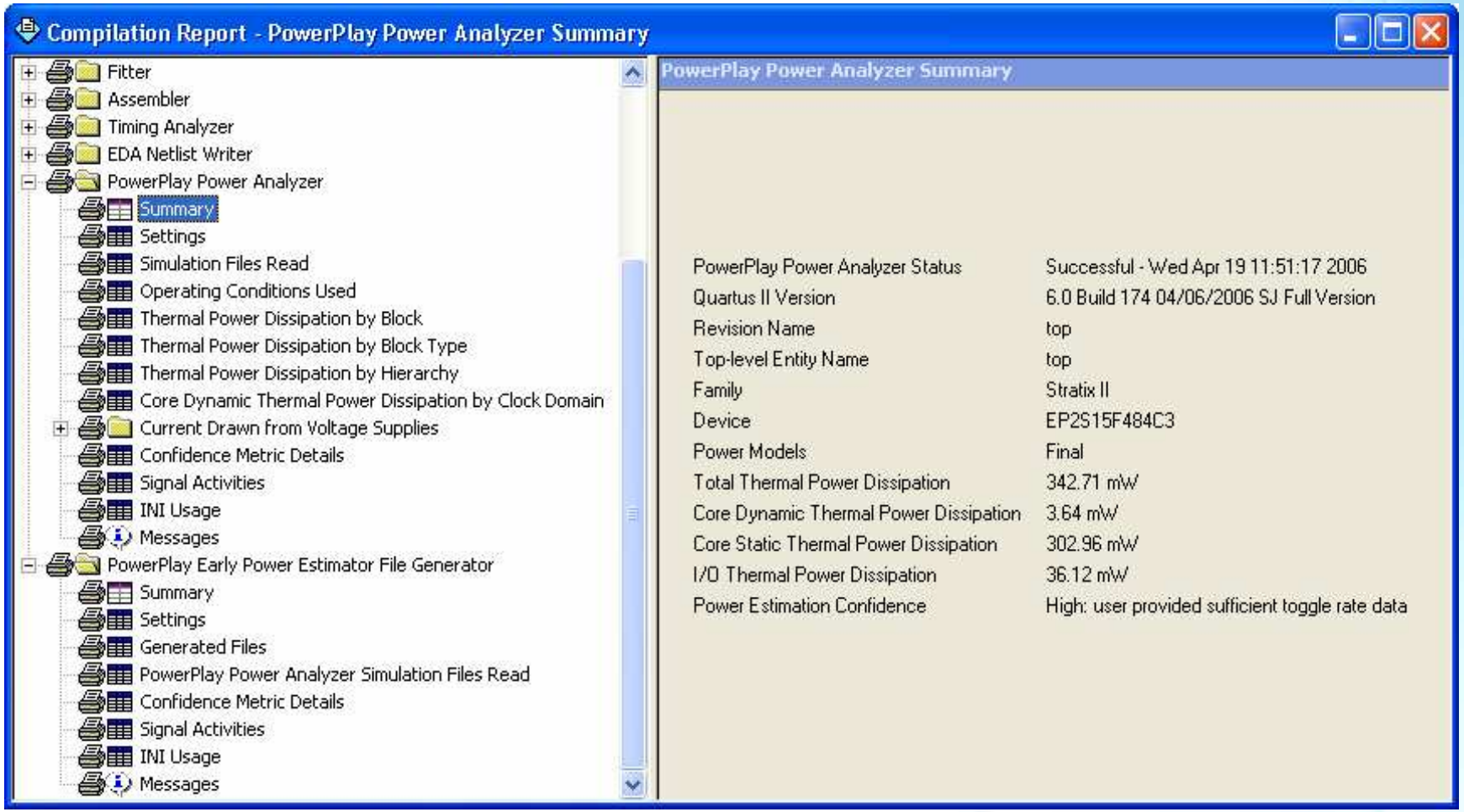
Compilation folder power report



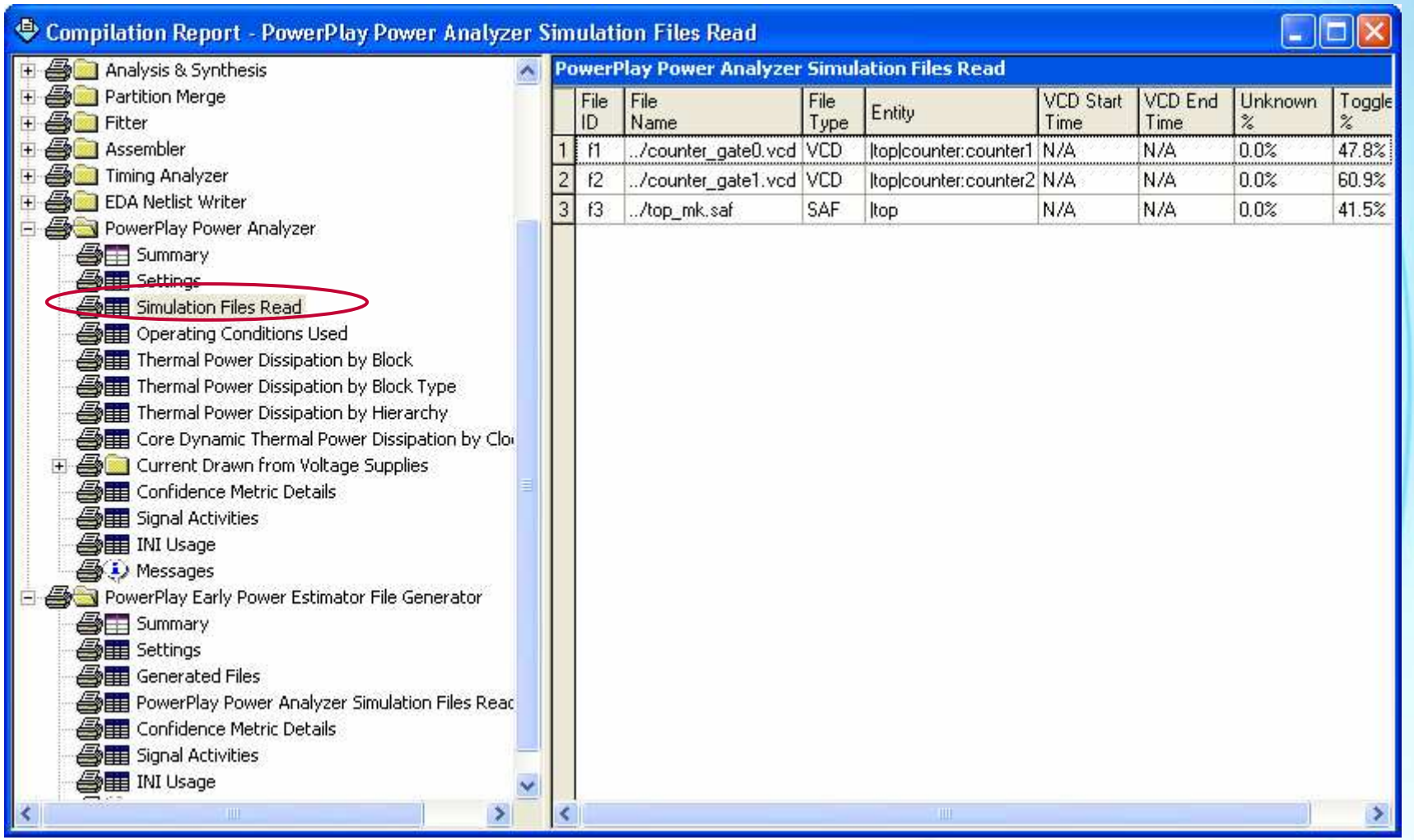
Reporting

- The Power Analyzer Report includes two kinds of info:
  - Data to verify that correct settings and inputs were used
    - Confidence metric
    - Signal activities (simulation files)
    - Operating conditions
  - Data that present the power estimate in many ways (slices):
    - Overall result
    - Power by block type
    - Power by block

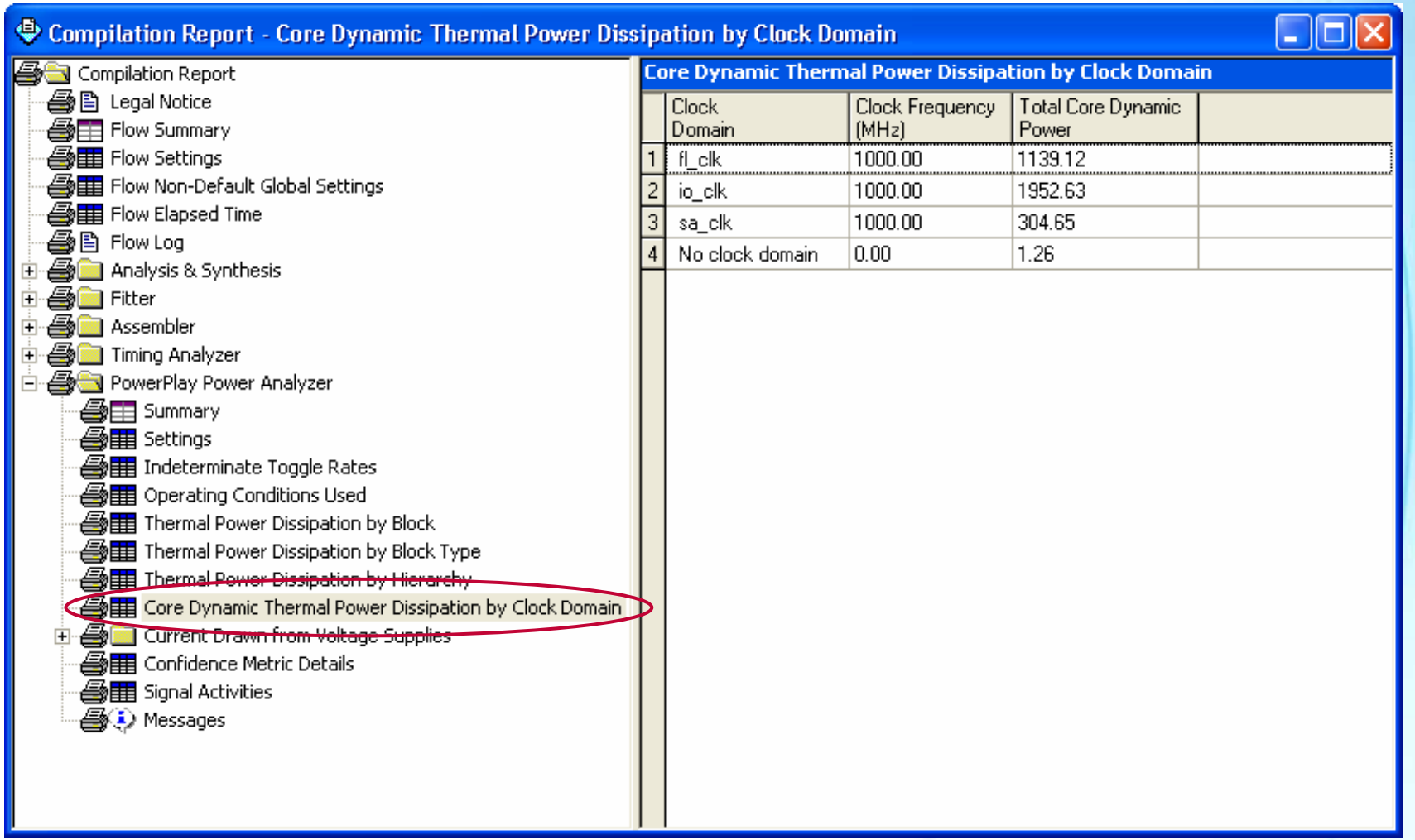
Reporting



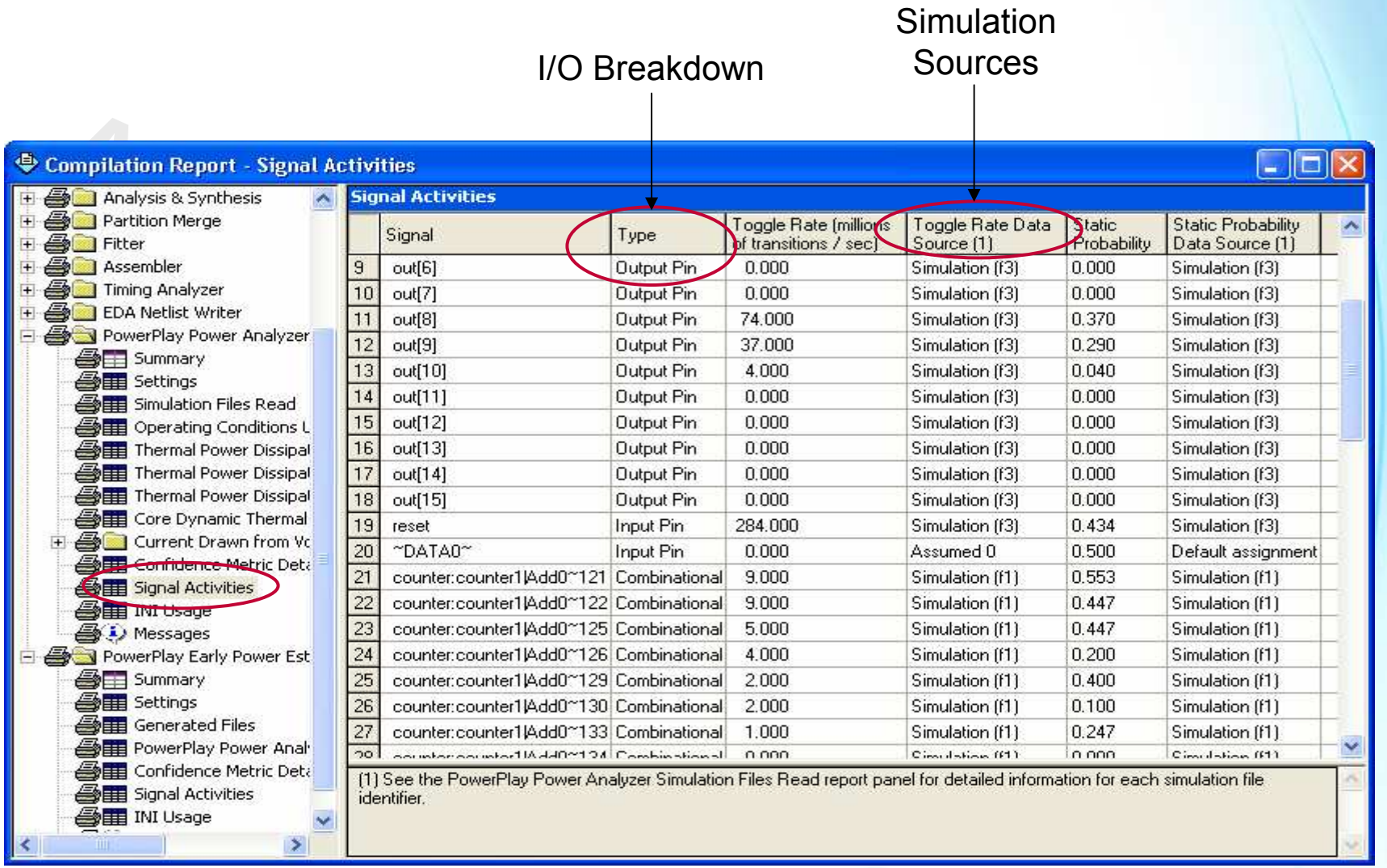
Reporting



Reporting

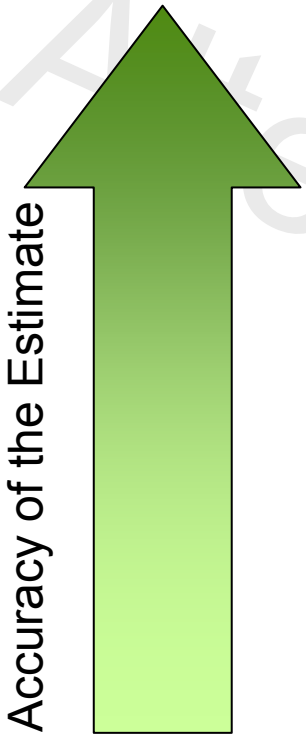


Reporting



	Signal	Type	Toggle Rate (millions of transitions / sec)	Toggle Rate Data Source (1)	Static Probability	Static Probability Data Source (1)
9	out[6]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
10	out[7]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
11	out[8]	Output Pin	74.000	Simulation (f3)	0.370	Simulation (f3)
12	out[9]	Output Pin	37.000	Simulation (f3)	0.290	Simulation (f3)
13	out[10]	Output Pin	4.000	Simulation (f3)	0.040	Simulation (f3)
14	out[11]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
15	out[12]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
16	out[13]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
17	out[14]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
18	out[15]	Output Pin	0.000	Simulation (f3)	0.000	Simulation (f3)
19	reset	Input Pin	284.000	Simulation (f3)	0.434	Simulation (f3)
20	~DATA0~	Input Pin	0.000	Assumed 0	0.500	Default assignment
21	counter:counter1|Add0~121	Combinational	9.000	Simulation (f1)	0.553	Simulation (f1)
22	counter:counter1|Add0~122	Combinational	9.000	Simulation (f1)	0.447	Simulation (f1)
23	counter:counter1|Add0~125	Combinational	5.000	Simulation (f1)	0.447	Simulation (f1)
24	counter:counter1|Add0~126	Combinational	4.000	Simulation (f1)	0.200	Simulation (f1)
25	counter:counter1|Add0~129	Combinational	2.000	Simulation (f1)	0.400	Simulation (f1)
26	counter:counter1|Add0~130	Combinational	2.000	Simulation (f1)	0.100	Simulation (f1)
27	counter:counter1|Add0~133	Combinational	1.000	Simulation (f1)	0.247	Simulation (f1)

Estimation Accuracy



Timing/Gate Level Simulation

RTL Simulation + Vectorless

Default Toggle Rate

Conclusion

- Successful power analysis comes from accurate power models and thorough operation condition specifications.
- Power Analyzer User Interface provides complete control
- Reporting provides full analysis capabilities
- Different levels of Estimation accuracy available
  - Incorrect usage may result in inaccurate estimation and poor optimization