



Early Power Estimator

Altera Asia Pacific Regional Support Center

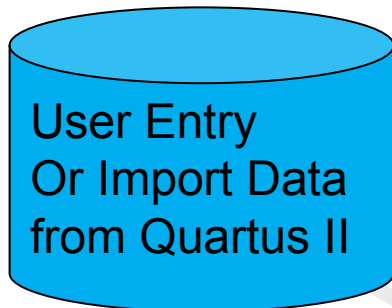


Agenda

- Overview
- Setup
- Using the EPE
- Lab

Overview

Inputs



Early Power Estimator

Reports

- Block Power
- Supply Power
- Thermal Analysis

- Accounts for device complexities, including temperature
- Allows quick, efficient “What-If” analysis
- Functional vectors not required
 - Accuracy will be affected, however
- Easily distributed as a spreadsheet

- Accurate FPGA power estimation require 3 components:



EPE Setup

- System Requirements
 - Windows NT/2000/XP Operating System
 - Microsoft Excel 2002 or higher
- Download and Installation
 - Available from Altera web site www.altera.com

Entering Information Into EPE

- Clearing All Values
 - Reset all EPE fields/values by clicking **Reset**
- Manually Entering Information
 - Enter values into input-designated cells (white, unshaded)
 - Other cells cannot be edited
 - Can specify module names per resource row
- Importing a Quartus II output .csv file
 - Generate .csv file from Quartus II
 - Launch the EPE Excel spreadsheet
 - Click “Import Quartus II File” button; follow directions

Importing Quartus II Output .csv File

1

Generate .CSV file for your design
design-name_early_pwr.csv

Project Assignments Processing Tools Window

Add Current File to Project
Add/Remove Files in Project...

Revisions...
Copy Project...

Archive Project...
Restore Archived Project...

Import Database...
Export Database...

Import Design Partition...
Export Design Partition...
Generate Bottom-Up Design Partition Scripts...

Generate Tcd File for Project...
Generate PowerPlay Early Power Estimator File

2

Launch the excel spreadsheet
Import design-name_early_pwr.csv

Input Parameters

Family: Stratix II
Device: EP2590
Package: F1508
Temperature Grade: Commercial
Power Characteristics: Typical

☐ User Entered Tj ☒ Auto Computed Tj

Ambient Temp, T_a (°C): 25

☐ Custom Theta JA ☒ Estimated Theta JA

Heat Sink: 23 mm - Medium Profile
Airflow: 200 lfm (1.0 m/s)
Custom θ_{JA} (°C/W): 1.50
Board Thermal Model: None (Conservative)
Custom θ_{JB} (°C/W): N/A
Board Temp, T_B (°C): N/A

Thermal Power (W)

Logic	0.003
RAM	0.010
DSP	0.007
I/O	0.360
HSDI	0.007
PLL	0.034
Clocks	0.009
ACOR	N/A
P _{static}	0.768
TOTAL	1.198

HardCopy II: N/A

Thermal Analysis

Junction Temp, T_J (°C): 27.0
θ_{JA} Junction-Ambient: 1.70
θ_{JB} Junction-Board: N/A
Maximum Allowed T_A (°C): 81.0

Power Supply Current (A)

I_{CCINT}: 0.828
I_{CCPD}: 0.013
I_{CCIO}: 0.062
I_{CCVCC}: N/A

Click buttons for details

Set Toggle % Reset Import Quartus II File Import EPE V6.0 View Report

3

Using the EPE

■ Device-related Input Parameters

- Family
- Device
- Package
- Temperature grade
- Power Characteristics

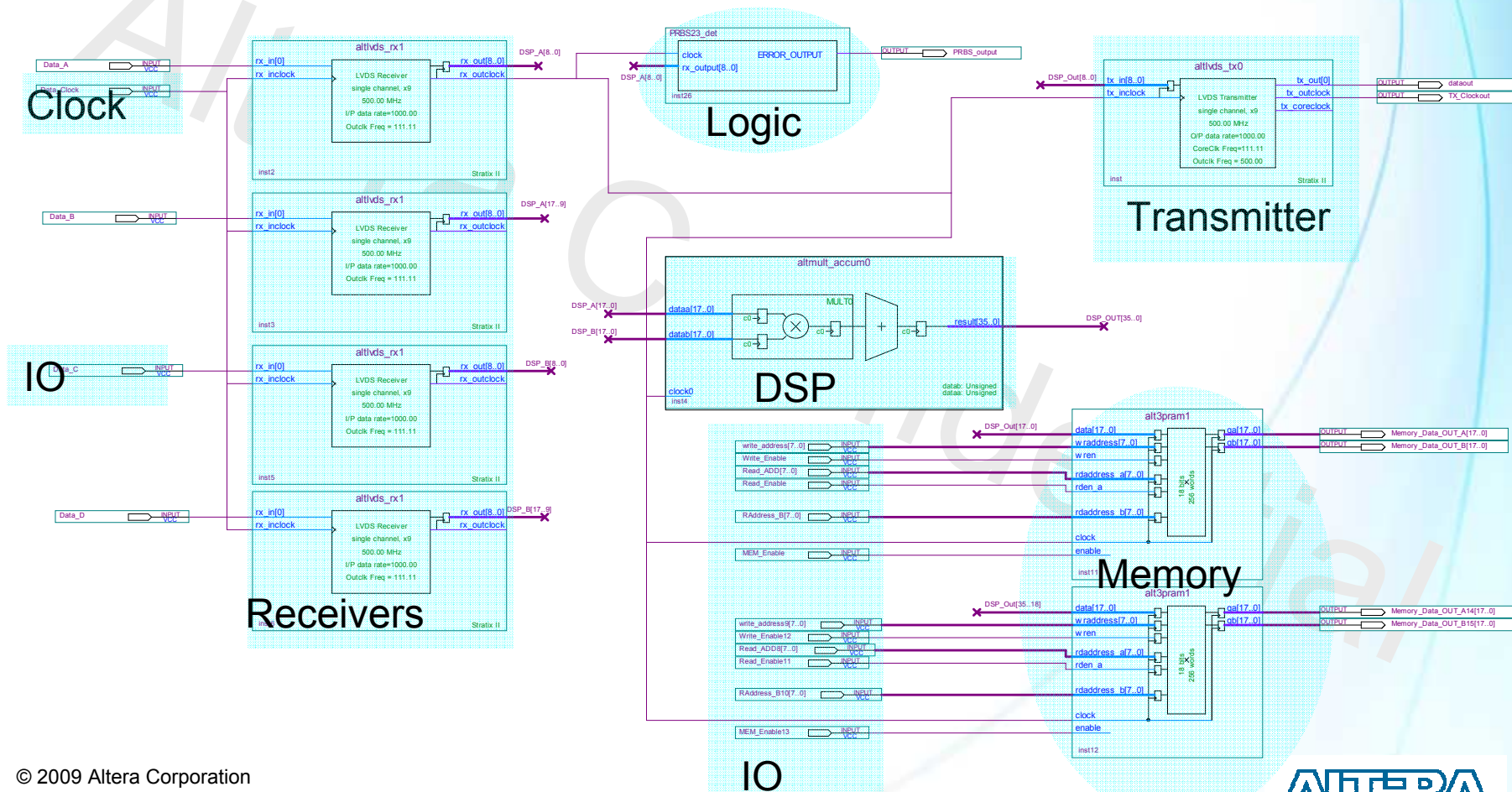
■ Thermal Input Parameters

- Ambient (or junction) temperature
- Heat sink used?
- Airflow
- Board thermal model
- Board temperature

Generic Design

■ Lab Design – Top Level Overview

- What are the resource usage estimates for the design?
- What are the clock frequencies, data rates, and toggle rates?



Using the Logic Resource Page

- Click “Logic” button to enter view Resource Page

The screenshot displays the Altera Logic Resource Page interface. The 'Input Parameters' section on the left includes dropdowns for Family (Stratix II), Device (EP2590), Package (F1508), Temperature Grade (Commercial), and Power Characteristics (Typical). It also has radio buttons for 'User Entered Tj' and 'Auto Computed Tj', with the latter selected. The 'Ambient Temp, T_a (°C)' is set to 25. The 'Heat Sink' is '23 mm - Medium Profile' and 'Airflow' is '200 lfm (1.0 m/s)'. The 'Board Thermal Model' is 'None (Conservative)'. The 'Thermal Power (W)' section in the center lists components: Logic (0.003), RAM (0.010), DSP (0.007), I/O (0.360), HSDI (0.007), PLL (0.034), Clocks (0.009), and XCVR (N/A). The 'TOTAL' is 1.198 W. The 'Thermal Analysis' section on the right shows 'Junction Temp, T_J (°C)' as 27.0, 'θ_{JA} Junction-Ambient' as 1.70, 'θ_{JB} Junction-Board' as N/A, and 'Maximum Allowed T_A (°C)' as 81.0. The 'Power Supply Current (A)' section shows I_{CCINT} (0.828), I_{CCPD} (0.013), I_{CCIO} (0.062), and I_{CCVCC} (N/A). A 'Logic' button is highlighted in the top left, and a 'Return to Main' button is next to it. A 'Set Toggle %' button is at the bottom left. A 'Thermal Power (W)' table is shown at the bottom, with a red circle around the 'Total' column value of 0.001 for the first module.

Module	Clock Frequency (MHz)	# Combinational ALUTs	# FFs	Toggle %	Routing	Block	Total	User Comments
1	111.1	12	0	42.7%	0.000	0.001	0.001	
2	111.1	0	72	18.8%	0.001	0.000	0.002	
	0.0	0	0	12.5%	0.000	0.000	0.000	

Using the RAM Resource Page

- Click “RAM” button to enter view Resource Page

The screenshot displays the Altera RAM Resource Page interface. The 'Input Parameters' section on the left includes dropdowns for Family (Stratix II), Device (EP2590), Package (F1508), Temperature Grade (Commercial), and Power Characteristics (Typical). It also features radio buttons for 'User Entered Tj' and 'Auto Computed Tj', with an 'Ambient Temp, T_a (°C)' field set to 25. Other parameters include Heat Sink (23 mm - Medium Profile), Airflow (200 lfm (1.0 m/s)), and Board Thermal Model (None (Conservative)).

The 'Thermal Power (W)' section in the center shows a list of components with their respective power values: Logic (0.003), RAM (0.010), DSP (0.007), I/O (0.360), HSDI (0.007), PLL (0.034), Clocks (0.009), XCVR (N/A), and P_{static} (0.768). The 'TOTAL' power is 1.198 W. A 'HardCopy II' button is also present.

The 'Thermal Analysis' section on the right shows 'Junction Temp, T_j (°C)' at 27.0, 'θ_{JA} Junction-Ambient' at 1.70, 'θ_{JB} Junction-Board' as N/A, and 'Maximum Allowed T_A (°C)' at 81.0. Below this, 'Power Supply Current (A)' is shown with values for I_{CCINT} (0.828), I_{CCPD} (0.013), I_{CCIO} (0.062), and I_{CCXCVR} (N/A).

At the bottom left, a summary box for 'RAM' shows 'Total Thermal Power (W)' as 0.010, with M512 Utilization at 0.0%, M4K Utilization at 1.2%, and MRAM Utilization at 0.0%.

The bottom table provides a detailed breakdown of RAM utilization across three modules:

Module	RAM Type	# RAM Blocks	Data Width	RAM Mode	Port A			Port B			Toggle %	Valid Width/Mode	Thermal Power (W)			User Comments
					Clock Freq (MHz)	Enable %	Write %	Clock Freq (MHz)	Enable %	R/W %			Routing	Block	Total	
1	M4K	2	18	Simple Dual-Port	111.1	50%	50%	111.1	50%	100%	25.0%	Yes	0.001	0.001	0.003	
2	M4K	2	18	Simple Dual-Port	111.1	50%	50%	111.1	50%	50%	25.0%	Yes	0.000	0.002	0.002	
3	M4K	1	32	Simple Dual-Port	111.1	100%	100%	111.1	100%	100%	50.0%	Yes	0.002	0.003	0.005	

Using the DSP Resource Page

- Click “DSP” button to enter view Resource Page

The screenshot displays the Altera DSP Resource Page interface. The 'Input Parameters' section on the left includes dropdowns for Family (Stratix II), Device (EP2590), Package (F1508), Temperature Grade (Commercial), and Power Characteristics (Typical). It also has radio buttons for 'User Entered Tj' and 'Auto Computed Tj', with 'Auto Computed Tj' selected. The 'Ambient Temp, T_a (°C)' is set to 25. The 'Heat Sink' is '23 mm - Medium Profile' and 'Airflow' is '200 lfm (1.0 m/s)'. The 'Board Thermal Model' is 'None (Conservative)'. The 'Thermal Power (W)' section shows a list of components: Logic (0.003), RAM (0.010), DSP (0.007), I/O (0.360), HSDI (0.007), PLL (0.034), Clocks (0.009), and XCVR (N/A). The 'TOTAL' is 0.768. The 'Thermal Analysis' section shows 'Junction Temp, T_J (°C)' as 27.0, 'θ_{JA} Junction-Ambient' as 1.70, 'θ_{JB} Junction-Board' as N/A, and 'Maximum Allowed T_A (°C)' as 81.0. The 'Power Supply Current (A)' section shows I_{CCINT} (0.828), I_{CCPD} (0.013), I_{CCIO} (0.062), and I_{CCCVR} (N/A). A 'DSP' button is highlighted in the top left, and a 'Return to Main' button is next to it. A '0.007' value is circled in red in the 'DSP Utilization' section. Below the main interface, a table titled 'Thermal Power (W)' provides a detailed breakdown of the DSP utilization.

									Thermal Power (W)			
Module	Configuration	Clock Freq (MHz)	# of Instances	Toggle %	Reg Inputs?	Reg Outputs?	Pipe-lined?	Routing	Block	Total	User Comments	
1	18x18 Mult-Accum	111.1	1	50.0%	Yes	No	Yes	0.003	0.004	0.007		
	9x9 Simple Mult	0.0	0	12.5%	Yes	Yes	No	0.000	0.000	0.000		

Using the I/O Resource Page

- Click "I/O" button to enter view Resource Page

I/O Return to Main

Total Thermal Power (W) **0.360**

I/O Utilization **15.0%**

	V _{CCIO}	I _{CCIO} (A)
I/O Bank 1	2.5	0.0173
I/O Bank 2	2.5	0.0059
I/O Bank 3	3.3	0.0003
I/O Bank 4	1.8	0.0138
I/O Bank 5	3.3	0.0193
I/O Bank 6	1.8	0.0019
I/O Bank 7	3.3	0.0003
I/O Bank 8	3.3	0.0003
I/O Bank 9	3.3	0.0016
I/O Bank 10	3.3	0.0003
I/O Bank 11	3.3	0.0003
I/O Bank 12	1.5	0.0007
Unassigned		0.0000

Input Parameters

Family: Stratix II
Device: EP2590
Package: F1508
Temperature Grade: Commercial
Power Characteristics: Typical

☐ User Entered T_J ☒ Auto Computed T_J

Ambient Temp, T_a (°C): 25

☐ Custom Theta JA ☒ Estimated Theta JA

Heat Sink: 23 mm - Medium Profile
Airflow: 200 lfm (1.0 m/s)
Custom θ_{JA} (°C/W): 1.50
Board Thermal Model: None (Conservative)
Custom θ_{JB} (°C/W): N/A
Board Temp, T_B (°C): N/A

Thermal Power (W)

Logic: 0.003
RAM: 0.010
DSP: 0.007
I/O: 0.360
HSDI: 0.007
PLL: 0.034
Clocks: 0.009
XCVB: N/A
P_{static}: 0.768
TOTAL: 1.198

HardCopy II: N/A

Thermal Analysis

Junction Temp, T_J (°C): **27.0**
θ_{JA} Junction-Ambient: 1.70
θ_{JB} Junction-Board: N/A
Maximum Allowed T_A (°C): 81.0

Details...

Power Supply Current (A)

I_{CCINT}: 0.828
I_{CCPD}: 0.013
I_{CCIO}: 0.062
I_{CCIO}: N/A

Click buttons for details

Set Toggle % Reset Import Quartus II File Import EPE V6.0 View Report

Module	I/O Standard	Drive Strength / On-Chip Termination	Clock Freq (MHz)	# Output Pins	# Input Pins	# Bidir Pins	I/O Bank	Toggle %	OE %	Load (pF)	Data Rate	Bank I/O Std Check	Bank Voltage Check	Routing	Block	Total	I _{CCINT}	I _{CCPD}	I _{CCIO}
1	LVTTTL 3.3-V	24 mA	111.1	6	0	0	9	25.0%	100.0%	0	SDR	PASS	PASS	0.000	0.008	0.008	0.000	0.001	0.001
2	LVTTTL 3.3-V	24 mA	111.1	1	0	0	3	0.8%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
3	SSTL Class I 1.8-V	12 mA	111.1	0	43	0	4	12.5%	100.0%	0	SDR	PASS	PASS	0.001	0.133	0.134	0.090	0.000	0.013
4	LVTTTL 3.3-V	24 mA	111.1	0	5	0	5	12.5%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000	0.000
5	Differential HSTL Class I 1.5-V	12 mA	111.1	0	1	0	12	12.5%	100.0%	0	SDR	PASS	PASS	0.000	0.003	0.003	0.002	0.000	0.000
6	LVDS	Default	222.2	2	0	0	1	50.0%	100.0%	0	SDR	PASS	PASS	0.000	0.041	0.041	0.001	0.000	0.017
7	LVDS	Default	500.0	0	1	0	2	200.0%	100.0%	0	SDR	PASS	PASS	0.002	0.009	0.011	0.007	0.000	0.001
8	SSTL Class I 1.8-V	12 mA	111.1	0	5	0	6	12.5%	100.0%	0	SDR	PASS	PASS	0.000	0.015	0.015	0.010	0.000	0.002
9	LVTTTL 3.3-V	12 mA	111.1	66	0	0	5	25.0%	100.0%	0	SDR	PASS	PASS	0.000	0.094	0.094	0.005	0.008	0.019
10	LVTTTL 3.3-V	24 mA	0.0	0	1	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
11	LVDS	Default	1000.0	0	4	0	2	12.5%	100.0%	0	SDR	PASS	PASS	0.001	0.027	0.028	0.014	0.000	0.004

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Using the HSDI Resource Page

- Click "HSDI" button to enter view Resource Page

Input Parameters

Family: Stratix II
 Device: EP2590
 Package: F1508
 Temperature Grade: Commercial
 Power Characteristics: Typical

☐ User Entered Tj ☒ Auto Computed Tj
 Ambient Temp, T_a (°C): 25
☐ Custom Theta JA ☒ Estimated Theta JA

Heat Sink: 23 mm - Medium Profile
 Airflow: 200 lfm (1.0 m/s)
 Custom θ_{SA} (°C/W): 1.50
 Board Thermal Model: None (Conservative)
 Custom θ_{JB} (°C/W): N/A
 Board Temp, T_B (°C): N/A

Thermal Power (W)

Logic	0.003
RAM	0.010
DSP	0.007
I/O	0.360
HSDI	0.007
PLL	0.034
Clocks	0.009
XCVH	N/A
P _{static}	0.768
TOTAL	1.198

Thermal Analysis

Junction Temp, T_J (°C): 27.0
 θ_{JA} Junction-Ambient: 1.70
 θ_{JB} Junction-Board: N/A
 Maximum Allowed T_A (°C): 81.0

Power Supply Current (A)

ICCINT: 0.828
 ICCPD: 0.013
 ICCIO: 0.062
 ICCVH: N/A

Summary:
 HSDI: 0.007
 Total Thermal Power (W): 0.007

This section only estimates power within the SERDES blocks and does not include the I/O power nor PLL power. Please enter the appropriate parameters in the "IO" section for I/O power, and "PLL" section for PLL power.

Tx Module	Data Rate (Mbps)	# of Channels	Toggle %	Total Power (W)	User Comments
1	1000	2	50.0%	0.002	
	0	0	50.0%	0.000	
	0	0	50.0%	0.000	
	0	0	50.0%	0.000	

Rx Module	Data Rate (Mbps)	# of Channels	Toggle %	Total Power (W)	User Comments
1	1000	4	50.0%	0.005	
	0	0	50.0%	0.000	

Using the PLL Resource Page

- Click "PLL" button to enter view Resource Page

PLL | **Return to Main**

Total Thermal Power (W)	0.034
Enhanced PLL Utilization	0.0%
Fast/LVDS PLL Utilization	25.0%

The screenshot shows the PLL Resource Page with the following data:

Input Parameters		Thermal Power (W)		Thermal Analysis	
Family	Stratix II	Logic	0.003	Junction Temp, T_J (°C)	27.0
Device	EP2590	RAM	0.010	θ_{JA} Junction-Ambient	1.70
Package	F1508	DSP	0.007	θ_{JB} Junction-Board	N/A
Temperature Grade	Commercial	I/O	0.360	Maximum Allowed T_A (°C)	81.0
Power Characteristics	Typical	HSDI	0.007		
		PLL	0.034		
		Clocks	0.009		
		XCVR	N/A		
		P_{static}	0.768		
		TOTAL	1.198		

Power Supply Current (A):

I_{CCINT}	0.828
I_{CCPD}	0.013
I_{CCIO}	0.062
I_{CCPLL}	N/A

This section only estimates power from the PLL control blocks and does not include the power from the PLL clock output networks. Please enter additional parameters in the "Clocks" section.

Module	PLL Type	# PLL Blocks	# DPA Buses	Output Freq (MHz)	VCO Freq (MHz)	Total Power (W)	User Comments
1	Fast	2	0	111.1	1000.0	0.034	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	

Using the Clock Resource Page

- Click “Clocks” button to enter view Resource Page

The screenshot shows the Altera Clock Resource Page interface. The 'Input Parameters' section includes dropdowns for Family (Stratix II), Device (EP2S90), Package (F1508), Temperature Grade (Commercial), and Power Characteristics (Typical). It also has radio buttons for 'User Entered Tj' and 'Auto Computed Tj', with 'Auto Computed Tj' selected. The 'Ambient Temp, T_a (°C)' is set to 25. The 'Heat Sink' is '23 mm - Medium Profile', 'Airflow' is '200 lfm (1.0 m/s)', and 'Custom θ_{SA} (°C/W)' is 1.50. The 'Board Thermal Model' is 'None (Conservative)'. The 'Thermal Power (W)' section shows a list of components with their power values: Logic (0.003), RAM (0.010), DSP (0.007), I/O (0.360), HSDI (0.007), PLL (0.034), Clocks (0.009), XCVR (N/A), P_{static} (0.768), and TOTAL (1.198). The 'Thermal Analysis' section shows 'Junction Temp, T_J (°C)' as 27.0, 'θ_{JA} Junction-Ambient' as 1.70, 'θ_{JB} Junction-Board' as N/A, and 'Maximum Allowed T_A (°C)' as 81.0. The 'Power Supply Current (A)' section shows 'I_{CCINT}' as 0.828, 'I_{CCPD}' as 0.013, 'I_{CCIO}' as 0.062, and 'I_{CCVCR}' as N/A. A 'Clocks' button is highlighted in the bottom left, and a 'Return to Main' button is next to it. The 'Total Thermal Power (W)' is 0.009, which is circled in red. A dotted line connects this value to the 'Total Power (W)' column in the table below.

Domain	Clock Freq (MHz)	Total Fanout	Global Enable %	Local Enable %	Total Power (W)	User Comments
1	111.1	84	100%	100%	0.009	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	

Using the Thermal Analysis Section

- Thermal Analysis on right-side of Main Page

Input Parameters

Family: Stratix II
 Device: EP2590
 Package: F1508
 Temperature Grade: Commercial
 Power Characteristics: Typical

☐ User Entered Tj ☒ Auto Computed Tj

Ambient Temp, T_a (°C): 25

☐ Custom Theta JA ☒ Estimated Theta JA

Heat Sink: 23 mm - Medium Profile
 Airflow: 200 lfm (1.0 m/s)
 Custom θ_{SA} (°C/W): 1.50
 Board Thermal Model: None (Conservative)
 Custom θ_{JB} (°C/W): N/A
 Board Temp, T_B (°C): N/A

Thermal Power (W)

Logic	0.003
RAM	0.010
DSP	0.007
I/O	0.360
HSDI	0.007
PLL	0.034
Clocks	0.009
XCVR	N/A
P_{static}	0.768
TOTAL	1.198

HardCopy II: N/A

Thermal Analysis

Junction Temp, T_J (°C): 27.0
 θ_{JA} Junction-Ambient: 1.70
 θ_{JB} Junction-Board: N/A
 Maximum Allowed T_A (°C): 81.0

[Details...](#)

Power Supply Current (A)

I_{CCINT}	0.828
I_{CCPD}	0.013
I_{CCIO}	0.062
I_{CCXCVR}	N/A

Click buttons for details

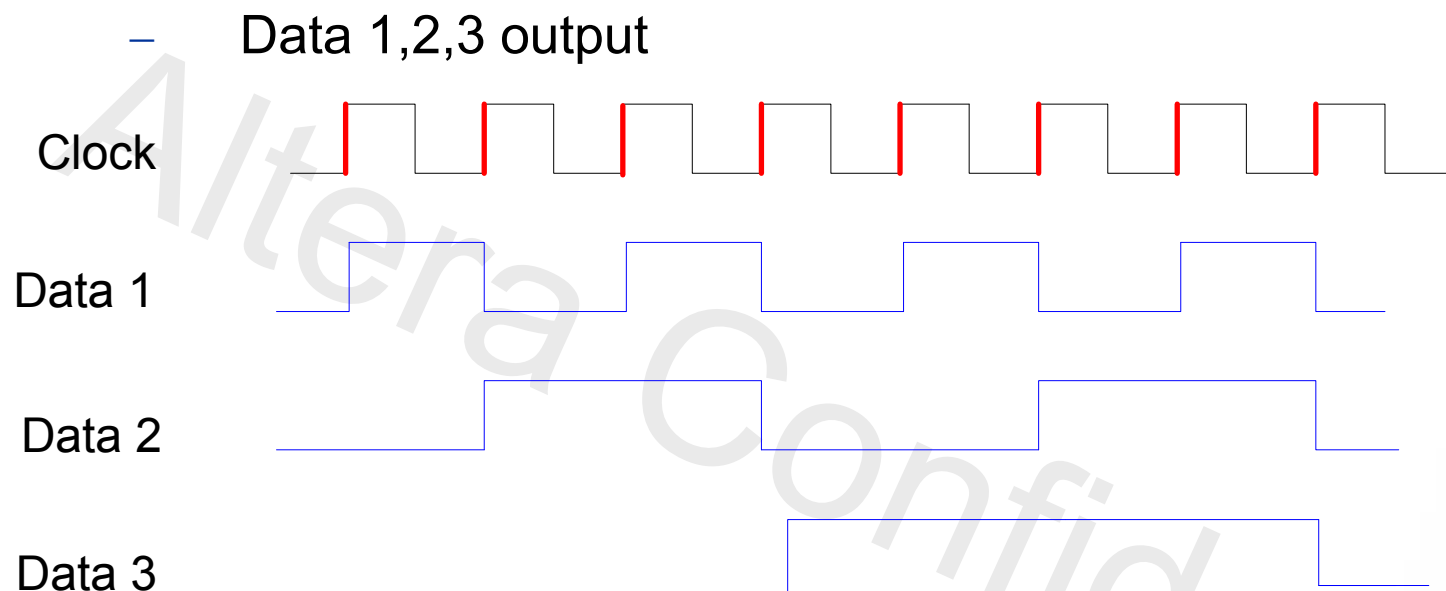
[Set Toggle %](#) [Reset](#) [Import Quartus II File](#) [Import EPE V6.0](#) [View Report](#)

Thermal Analysis

- Thermal Analysis provides the following:
 - Junction Temp (T_J)
 - Junction-to-ambient thermal resistance (T_{JA})
 - Junction-to-board thermal resistance (T_{JB})
 - Maximum allowed ambient temperature (T_A)
- To automatically compute T_J , the following is required:
 - System ambient temperature – 25 C
 - Airflow – 200 lfm (1.0 m/s)
 - Heat sink solution (optional) – 23mm Medium Profile
 - Board thermal model – None (Conservative)

Calculating Toggle Rates

■ Toggle Rate Calculations



Average Toggle Rate for Data 1,2 and 3 = $(100\% + 50\% + 25\%) / 3 = 58.33\%$

EPE Standard Default Toggle Rate = 12.5%

Conclusion

- Early Power Estimator provides components necessary for system power planning:
 - Thermal Power
 - Thermal Analysis
 - Power Supply Information
- Accuracy of power estimation depends on info provided:
 - Accurate resource usage
 - Correct toggling rate
 - Operating conditions

Appendix

■ EPE Block Resource Page – Detailed Descriptions

- Logic
- RAM
- DSP
- I/O
- HSDI
- PLL
- Clocks

Logic Block

- Most accurate power estimation, partition the design into different design modules
- The following information must be entered by you.

- Clock frequency (fmax) in MHz
- Number of combinational adaptive look-up tables (ALUTs)
- Number of registers
- Toggle percentage

The toggle rate describes how often the output changes with respect to the input clock which is usually between 6% and 12% for typical module for estimation purposes. This is a very critical piece of information for estimating your system dynamic power consumption. - Default toggle rate 12.5% for EPE

- Generic Design: Logic

- ✓ Clock frequency = 111.1 MHz
- ✓ Number of combinational adaptive look-up tables = 12
- ✓ Number of registers = 72
- ✓ Toggle percentage: ALUT = 42.7% & FFS= 18.8%

RAM Block

- TriMatrix memory consists of three types RAM blocks
 - M512
 - M4K
 - M-RAM blocks
- Each Row in the RAM section represents a design module which the following information must be entered by you.
 - Type of RAM being used
 - Single port
 - Simple Dual-port
 - True dual-port
 - ROM
 - The number of RAM implemented
 - The configuration of RAM block
 - Clock Frequency
 - The percentage of time the RAM clock is enabled
 - The percentage of time the port is writing compared to reading
- Generic Design: RAM
 - ✓ The number of RAM implemented = 5
 - ✓ The configuration of RAM block = M4K
 - ✓ Clock Frequency = 111.1 MHz
 - ✓ The percentage of time the RAM clock is enabled: 4 blocks = 50%, 1 Block = 100%
 - ✓ The percentage of time the port is writing compared to reading: 4 blocks = 50%, 1 Block = 100%

Digital Signal Processing (DSP)

- Dedicated DSP blocks that can be implemented for high speed DSP application.
- You must enter the following information for each DSP or multiplier module
 - Configuration
 - Clock frequency (fmax) in MHz
 - Number of instances
 - Toggle percentage of the data outputs
 - Whether or not the inputs and outputs are registered
 - Whether or not the module is pipelined
- Generic design: DSP
 - ✓ Clock Frequency = 111.5 MHz
 - ✓ Number of instances = 1
 - ✓ Toggle rate = 50%
 - ✓ Outputs registered = yes
 - ✓ Configuration = DSP 18*18 multiplier with accumulator
 - ✓ Module pipelined = No

General I/O Pins

- You must enter the following parameters for each design module
 - I/O Standard
 - Clock frequency (fMAX) in MHz
 - Drive strength/On-chip termination
 - Number of output, input, and bidirectional pins
 - I/O Bank
 - Pin toggle percentage
 - Output enable percentage
 - Average capacitance of the load
 - I/O data rate
 - Note: The EPE will assume you are using external termination resistors
- Generic design: I/O
 - ✓ I/O Standard = LVTTLL 3.3I, SSTL Class I 1.8, Diff HSTL Class I 1.5 , LVDS
 - ✓ Clock frequency = 500 MHz
 - ✓ Drive strength/On-chip termination = default
 - ✓ Number of output, input, and bidirectional pins = 0
 - ✓ I/O Bank = 1-6,9,12
 - ✓ Average Pin toggle percentage = 33%
 - ✓ Output enable percentage = 100%
 - ✓ Average capacitance of the load = 0
 - ✓ I/O data rate: LVDS input =1000 Mbps LVDS Output = 500 Mbps

High Speed Differential Interface (HSDI)

- HSDI section in EPE is divided two sections
 - Receiver
 - Transmitter
- You must enter the following parameter for the transmitter and receiver domain
 - Data rate (Mbps)
 - Number of channels in that transmitter and Receiver domain
 - Toggle percentage
- HSDI power calculations only applies
 - Transmitter serializer block
 - Receiver deserializer block
 - Receiver power is the same whether or not the Dynamic phase alignment circuitry (DPA) is used
 - I/O and PLL power are calculated in their own sections
- Generic design: Receivers and Transmitters
 - ✓ Data rate = 1000 Mbps
 - ✓ Number of channels in transmitter = 2
 - ✓ Number of channels Receiver = 4
 - ✓ Toggle percentage = 50%

Phase-Locked Loops (PLLs)

- General and dedicated PLL
 - General usage
 - Enhanced PLL
 - Fast PLL
 - Dedicated PLL drives LVDS hardware
 - LVDS PLL
- You must enter the following parameters for the PLL
 - PLL type
 - Number of PLL blocks
 - Number of DPA buses
 - Output frequency
 - VCO frequency
- Generic design: PLL
 - ✓ PLL type = Fast
 - ✓ Number of PLL blocks = 2
 - ✓ Number of DPA buses = 0
 - ✓ Output frequency = 111.1 MHz
 - ✓ VCO frequency = 1000 MHz

Clocks

- The clock section represents a clock network in the domains
 - Global clock
 - Regional clock

Note: Hardcopy makes no distinguish between the two clock domains
- You must enter the following parameters for the clock section
 - Clock Freq (MHz)
 - Total Fan-out
 - Global Enable%
 - Local Enable% -not applicable for Hardcopy II devices
- Generic design: Clock
 - ✓ Clock Freq (MHz) = 111.1 MHz
 - ✓ Total Fan-out = 84
 - ✓ Global Enable% = 100%
 - ✓ Local Enable% = 100%