

# nRF51 Series introduction

- A brief look at the underlying hardware



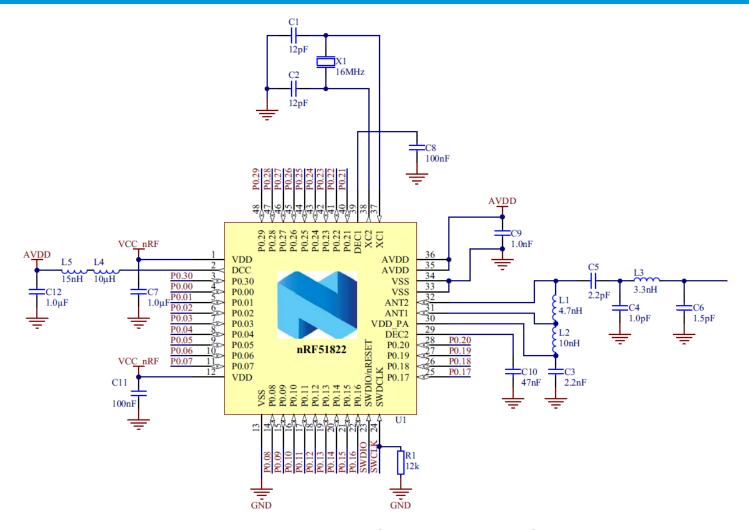
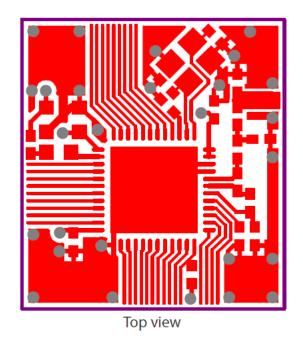
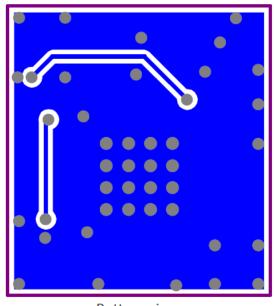


Figure 9 nRF51822-QFAA with DC/DC converter - Schematic









**Bottom view** 

Figure 10 nRF51822-QFAA with DC/DC regulator - Layout





Flexibility

Consistency

**Low Power** 





Flexibility

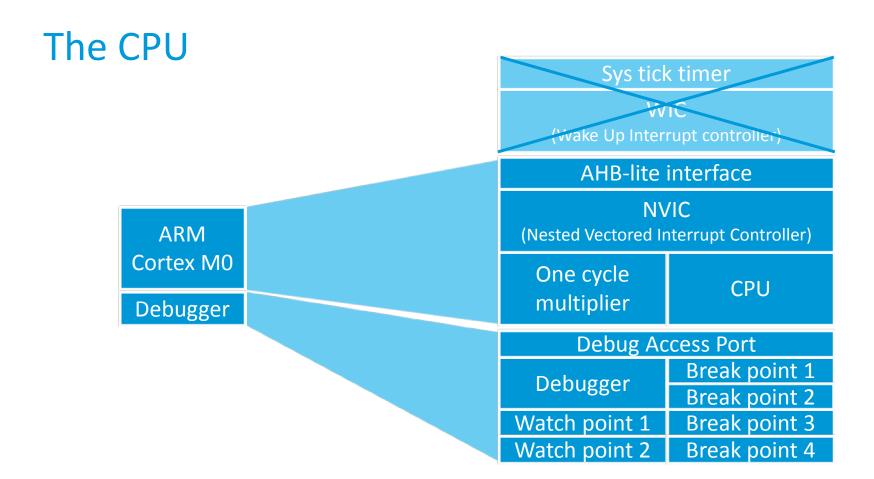
Consistency

**Low Power** 

Core functions











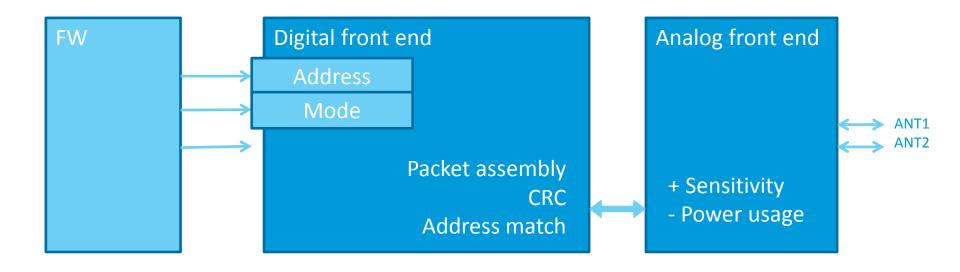
## Address map

0xE010 0000	reserved
0xE000 0000	Private Peripheral Bus
0XL000 0000	reserved
0x5000 0000	Peripherals
	reserved
0x4000 0000	Peripherals
02000 0000	reserved
0x2000 0000	RAM
	reserved
0x1000 1000	UCIR
	reserved
0x1000 0000	FICR
	reserved
0x0000 0000	Code





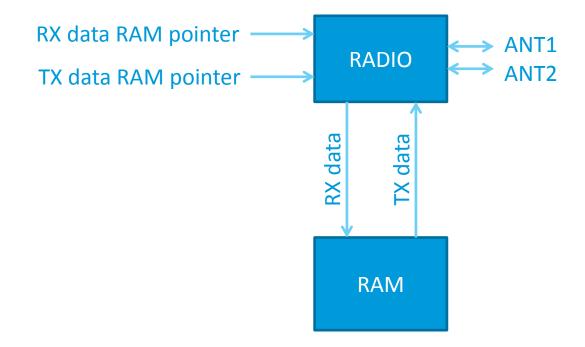
#### Multi Protocol Radio







### Easy DMA







Flexibility

Consistency

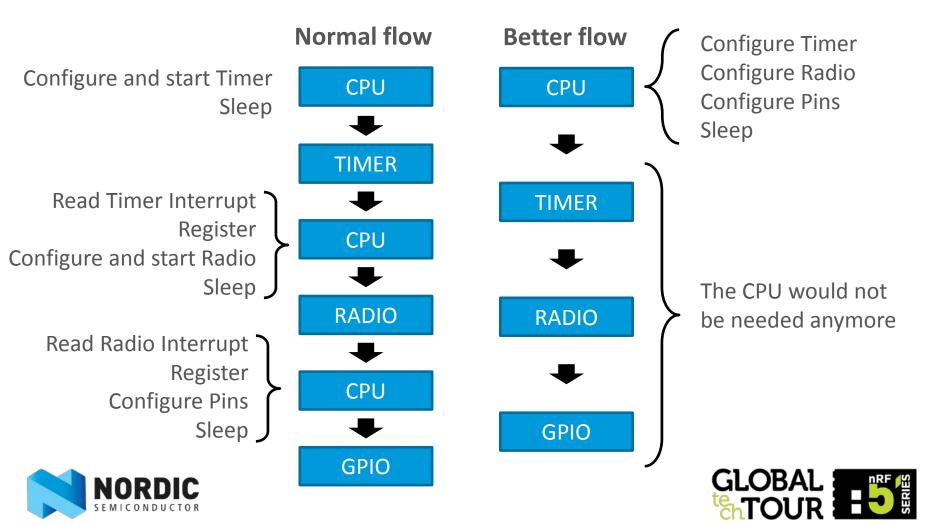
**Low Power** 

Signalling and Connectivity

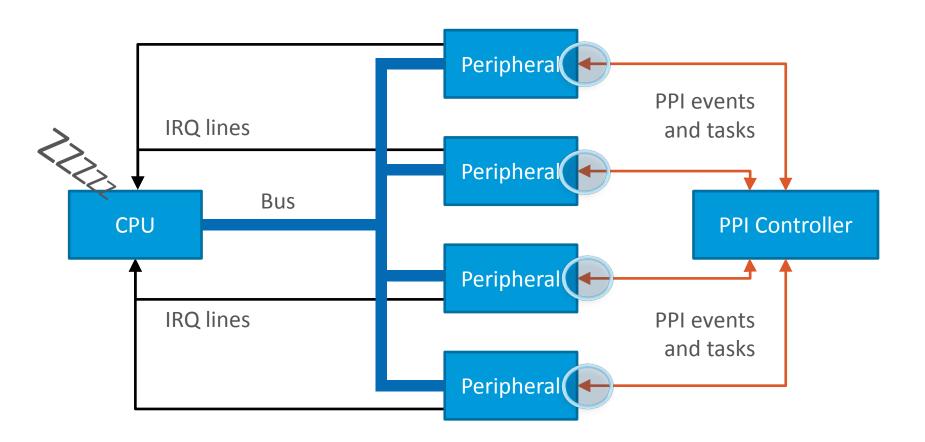




### Signalling flow between peripherals



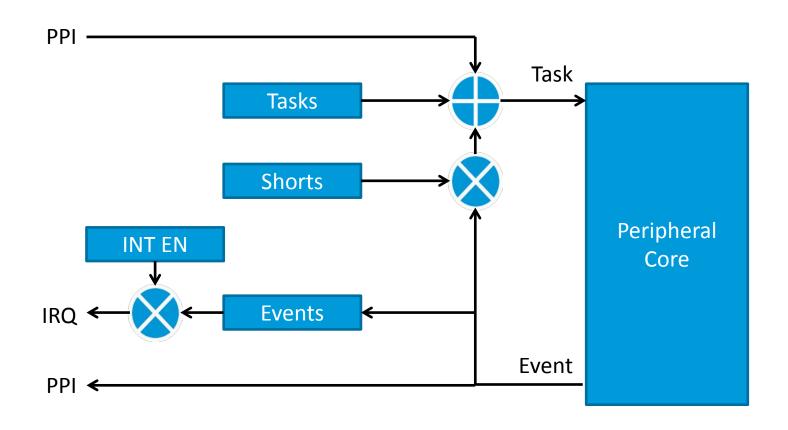
### IRQ vs Programmable Peripheral Interconnect (PPI)







### PPI - Block Diagram





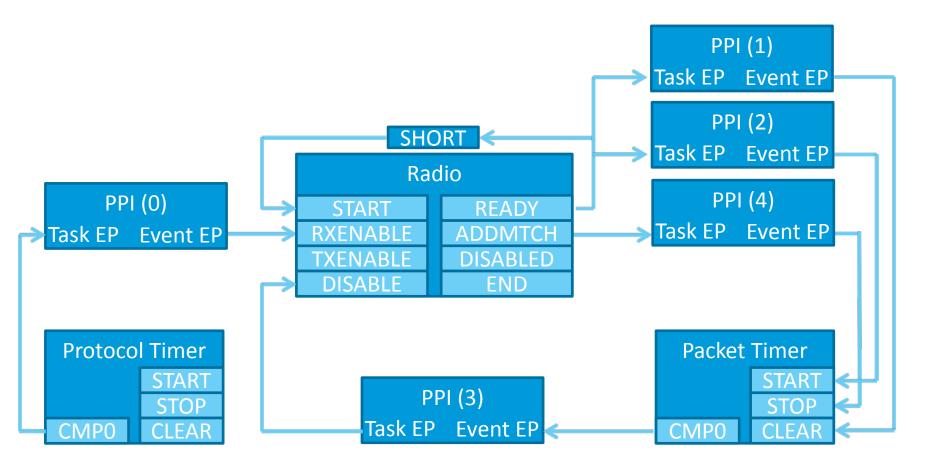


#### **PPI Connections Peripheral** Peripheral **Events** Peripheral **PPI Channels** Write your **event**'s address **Tasks** to the channel's event **Peripheral** endpoint register Write your task's address to the channel's task Peripheral endpoint register





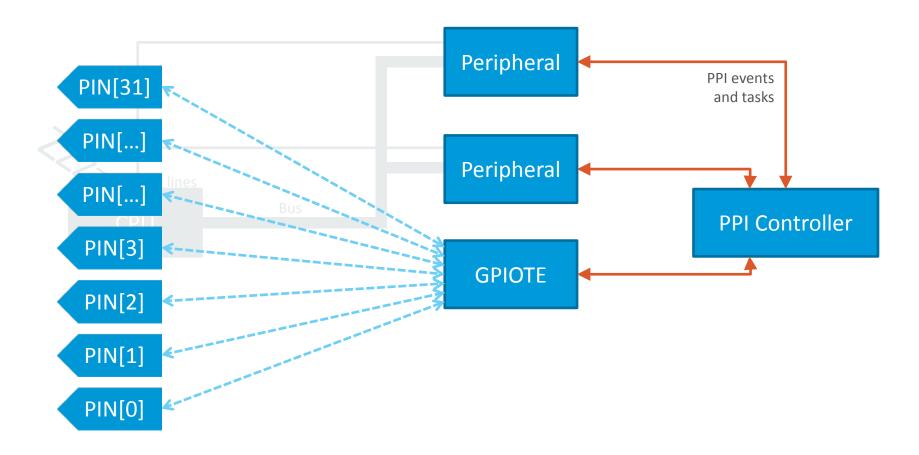
### PPI - Real-life example







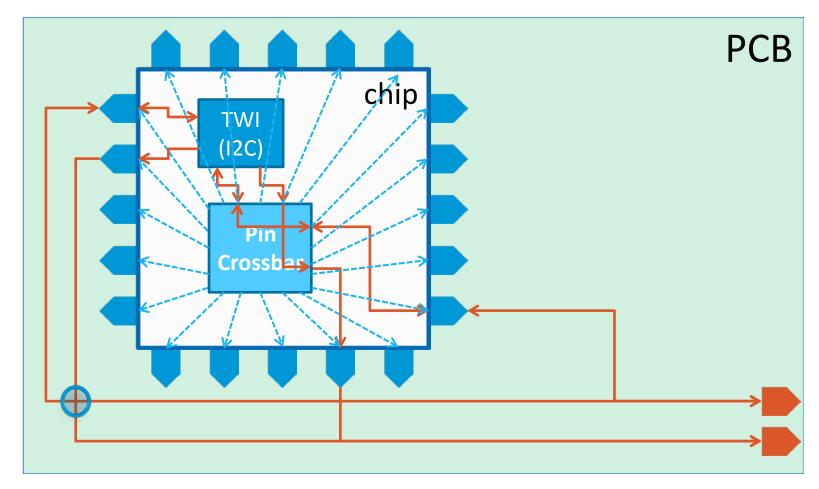
### **GPIOTE (GPIO Tasks and Events)**







## Peripheral pin access







Flexibility

Consistency

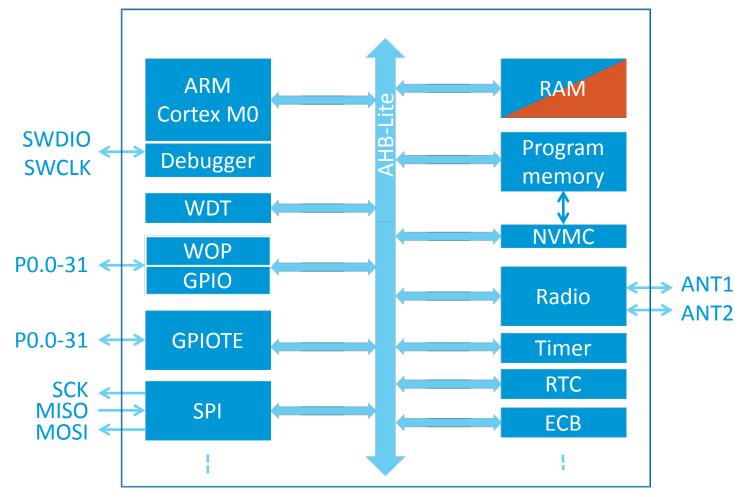
**Low Power** 

**Power and Clock** 





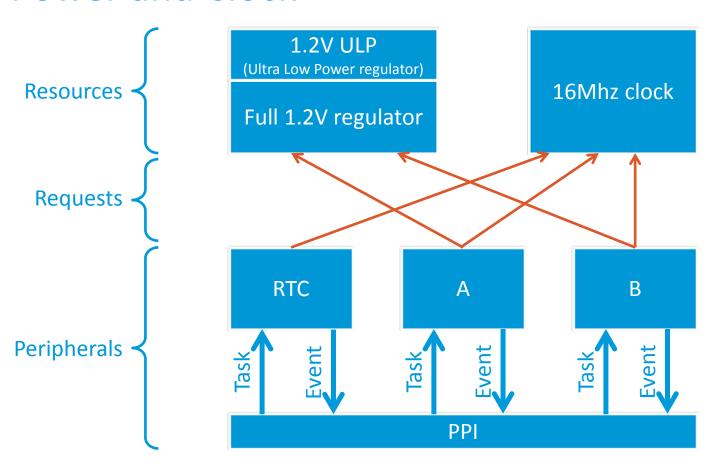
# Power Managemeystem Off







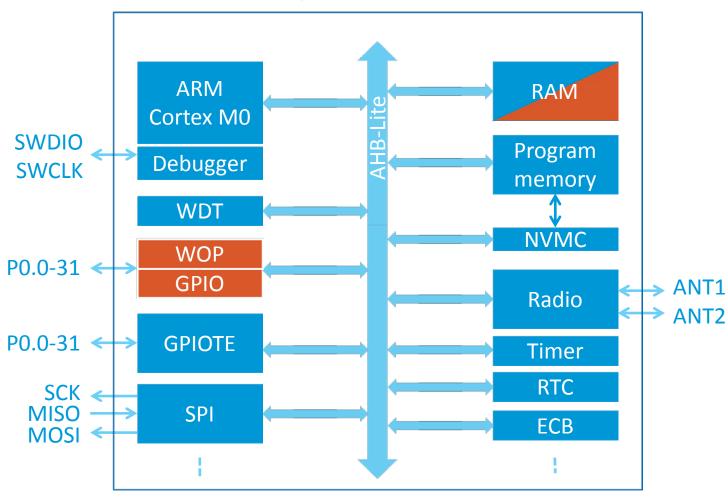
### **Power and Clock**







### System On







Flexibility

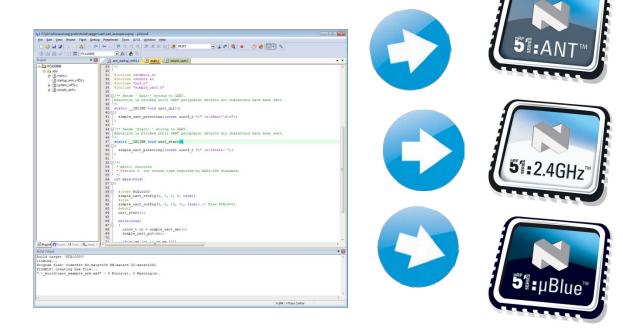
Consistency

**Low Power** 





### **Code Reuse**







Flexibility

Consistency

**Low Power** 

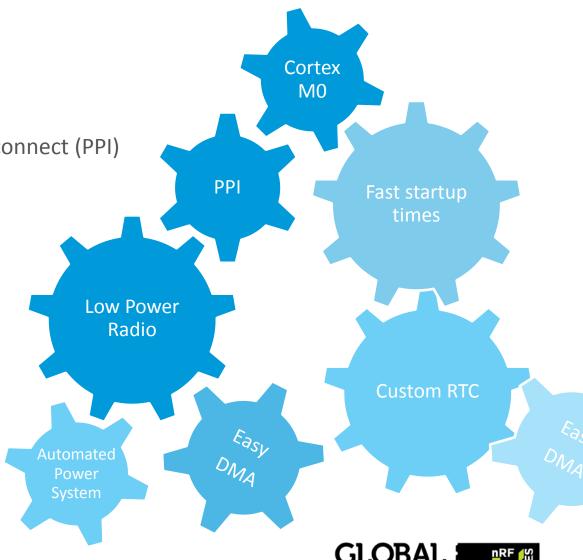




### Ultra low power

Programmable Peripheral Interconnect (PPI)

- Cortex M0
- Fast Startup Time
- Radio
- Automated Power System
- EasyDMA







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Thank you for your attention

