Nordic VLSI AS

Single chip 433/868/915 MHz Transceiver **nRF905**

FEATURES

- True single chip GFSK transceiver in a small 32-pin package (32L QFN 5x5mm)
- ShockBurst™ mode for low power operation
- Power supply range 1.9 to 3.6 V
- Multi channel operation – ETSI/FCC Compatible
- Channel switching time <650µs
- Extremely low cost Bill of Material (BOM)
- No external SAW filter
- Adjustable output power up to 10dBm
- Carrier detect for "listen before transmit" protocols
- Data Ready signal when a valid data package is received or transmitted
- Address Match for detection of incoming package
- Automatic retransmission of data packages
- Automatic CRC and preamble generation
- Low supply current (TX), typical 11mA @ -10dBm output power
- Low supply current (RX), typical 12.5mA

APPLICATIONS

- Wireless data communication
- Alarm and security systems
- Home Automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Industrial sensors
- Keyless entry
- Toys

GENERAL DESCRIPTION

nRF905 is a single-chip radio transceiver for the 433/868/915 MHz ISM band. The transceiver consists of a fully integrated frequency synthesiser, receiver chain with demodulator, a power amplifier, a crystal oscillator and a modulator. The ShockBurst™ feature automatically handles preamble and CRC. Configuration is easily programmable by use of the SPI interface. Current consumption is very low, in transmit only 11mA at an output power of -10dBm, and in receive mode 12.5mA. Built in power down modes makes power saving easily realizable.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum transmit output power	10	dBm
Transmitted data rate (Manchester-encoder embedded)	100	kbps
Supply current in transmit @ -10dBm output power	11	mA
Supply current in receive mode	12.5	mA
Temperature range	-40 to +85	°C
Typical Sensitivity	-100	dBm
Supply current in power down mode	2.5	µA

Table 1 nRF905 quick reference data.

ORDERING INFORMATION

Type Number	Description	Version
nRF905 IC	32L QFN 5x5mm	-
nRF905-EVKIT 433	Evaluation kit 433MHz	1.0
nRF905-EVKIT 868/915	Evaluation kit 868/915MHz	1.0

Table 2 nRF905 ordering information.

BLOCK DIAGRAM

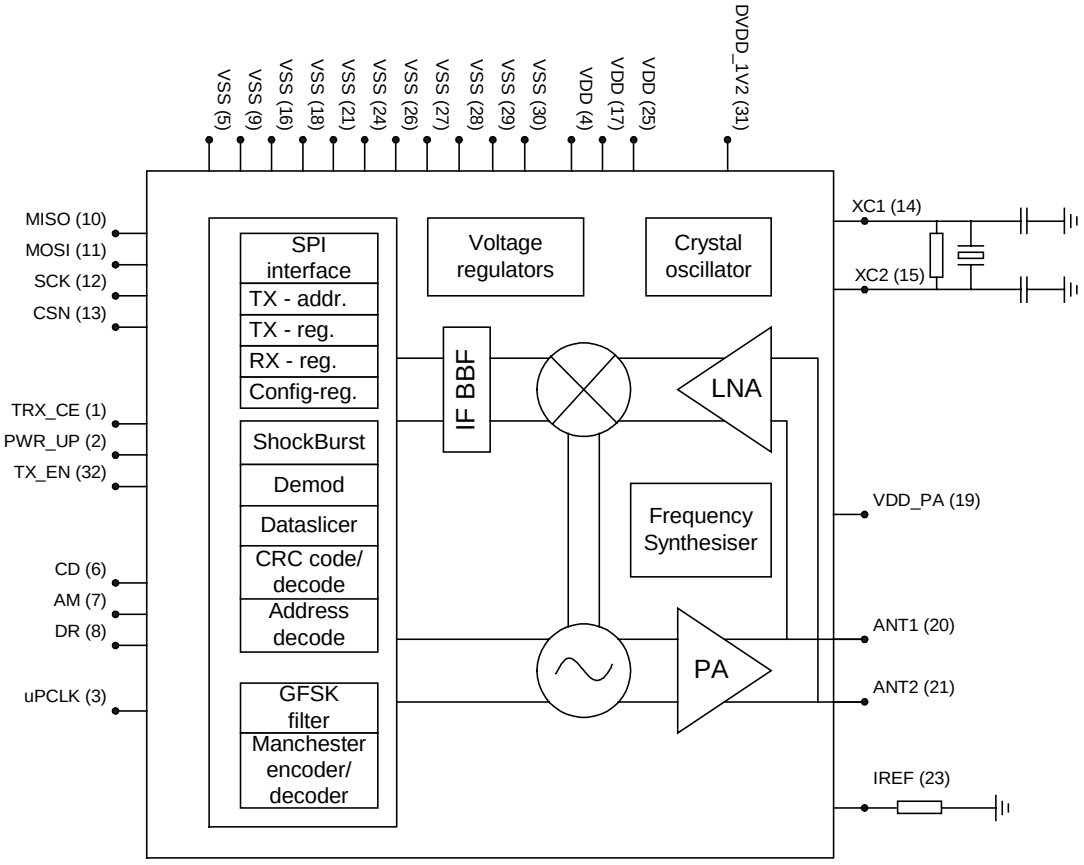


Figure 1 nRF905 with external components.

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	TRX_CE	Digital input	Enables chip for receive and transmit
2	PWR_UP	Digital input	Power up chip
3	uPCLK	Clock output	Output clock, divided crystal oscillator full-swing clock
4	VDD	Power	Power supply (+3V DC)
5	VSS	Power	Ground (0V)
6	CD	Digital output	Carrier Detect
7	AM	Digital output	Address Match
8	DR	Digital output	Receive and transmit Data Ready
9	VSS	Power	Ground (0V)
10	MISO	SPI - interface	SPI output
11	MOSI	SPI - interface	SPI input
12	SCK	SPI - Clock	SPI clock
13	CSN	SPI - enable	SPI enable, active low
14	XC1	Analog Input	Crystal pin 1/ External clock reference pin
15	XC2	Analog Output	Crystal pin 2
16	VSS	Power	Ground (0V)
17	VDD	Power	Power supply (+3V DC)
18	VSS	Power	Ground
19	VDD_PA	Power output	Positive supply (1.8V) to nRF905 power amplifier
20	ANT1	RF	Antenna interface 1
21	ANT2	RF	Antenna interface 2
22	VSS	Power	Ground (0V)
23	IREF	Analog Input	Reference current
24	VSS	Power	Ground (0V)
25	VDD	Power	Power supply (+3V DC)
26	VSS	Power	Ground (0V)
27	VSS	Power	Ground (0V)
28	VSS	Power	Ground (0V)
29	VSS	Power	Ground (0V)
30	VSS	Power	Ground (0V)
31	DVDD_1V2	Power	Low voltage positive digital supply output for de-coupling
32	TX_EN	Digital input	TX_EN=”1”TX mode, TX_EN=”0”RX mode

Table 3 nRF905 pin function.

PIN ASSIGNMENT

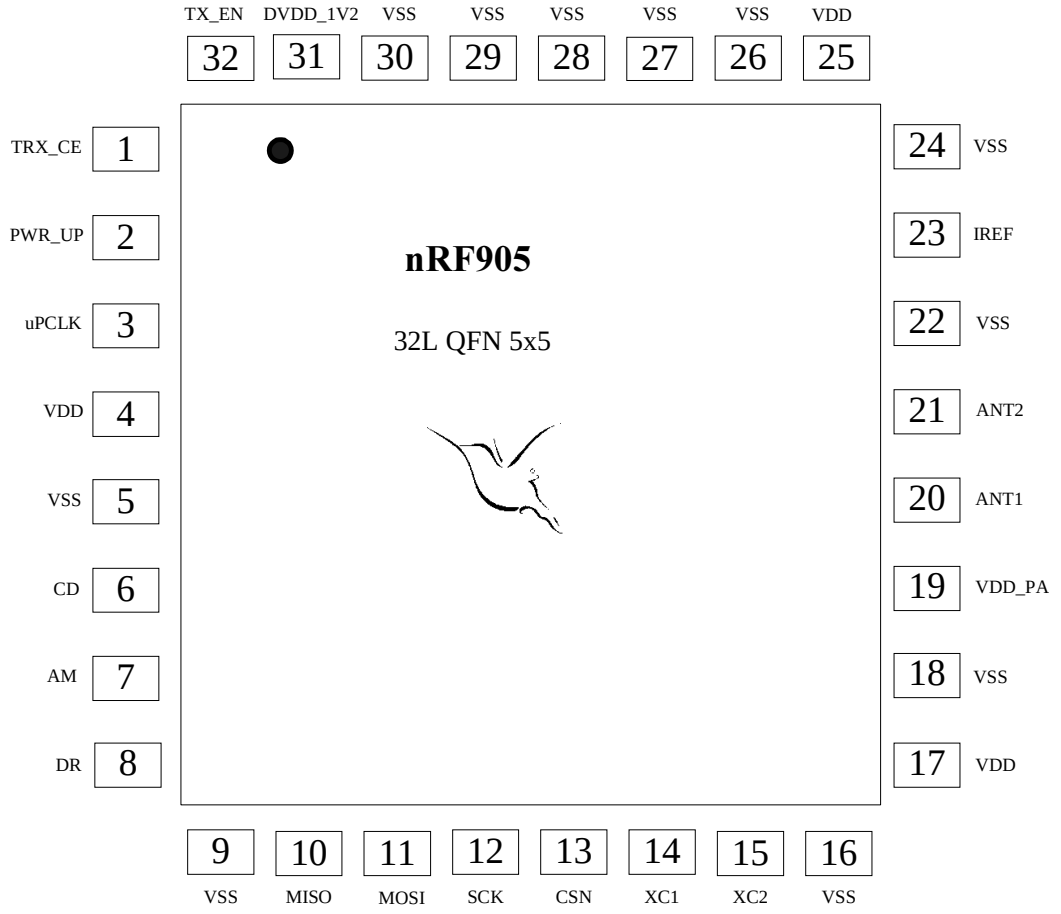


Figure 2 nRF905 pin assignment (top view) for a 32L QFN 5x5 package.

ELECTRICAL SPECIFICATIONS

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Operating conditions					
VDD	Supply voltage		1.9	3.0	3.6	V
TEMP	Operating temperature		-40	27	85	ºC
	Digital input pin					
V_{IH}	HIGH level input voltage		VDD-0.3		VDD	V
V_{IL}	LOW level input voltage		VSS		0.3	V
	Digital output pin					
V_{OH}	HIGH level input voltage (I_{OH}=-0.5mA)		VDD-0.3		VDD	V
V_{OL}	LOW level input voltage (I_{OL}=0.5mA)		VSS		0.3	V
	General electrical specification					
I_{stby_eclk}	Supply current in standby, uCLK enabled	1)		100		µA
I_{stby_dclk}	Supply current in standby, uCLK disabled	2)		12.5		µA
I_{PD}	Supply current in power down mode			2.5		µA
I_{SPI}	Supply current in SPI programming	3)		20		µA
	General RF conditions					
f_{OP}	Operating frequency	4)	430		928	MHz
f_{XTAL}	Crystal frequency	5)	4		20	MHz
Δf	Frequency deviation		±42	±50	±58	kHz
R_{GFSK}	GFSK data rate, Manchester-encoded			100		kbps
f_{CH433}	Channel spacing for 433MHz band			100		kHz
$f_{CH868/915}$	Channel spacing for 868/915MHz band			200		kHz
	Transmitter operation					
P_{RF10}	Output power 10dBm setting	6)	7	10	11	dBm
P_{RF6}	Output power 6dBm setting	6)	3	6	9	dBm
P_{RF-2}	Output power –2dBm setting	6)	-6	-2	2	dBm
P_{RF-10}	Output power -10dBm setting	6)	-14	-10	-6	dBm
P_{BW}	20dB bandwidth for modulated carrier			190		kHz
P_{RF1}	1st adjacent channel transmit power	7)		-27		dBc
P_{RF2}	2nd adjacent channel transmit power	7)		-54		dBc
$I_{TX10dBm}$	Supply current @ 10dBm output power			30		mA
$I_{TX-10dBm}$	Supply current @ -10dBm output power			11		mA
	Receiver operation					
I_{RX}	Supply current in receive mode			12.5		mA
RX_{SENS}	Sensitivity at 0.1%BER			-100		dBm
RX_{MAX}	Maximum received signal		0			dBm
C/I_{CO}	C/I Co-channel	8)		13		dB
C/I_{1ST}	1st adjacent channel selectivity C/I 200kHz	8)		-7		dB
C/I_{2ND}	2nd adjacent channel selectivity C/I 400kHz	8)		-16		dB
C/I_{IM}	Image rejection	8)		-30		dB

Table 4 nRF905 electrical specifications.

1) Output frequency is 4MHz load of external clock pin is 5pF, Crystal is 4MHz.
2) Crystal is 4MHz.
3) Chip in power down, SPI_SCK frequency is 1MHz.
4) Operates in the 433, 868 and 915 MHz ISM band.
5) The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz)
6) De-embedded Antenna load impedance = 400 Ω, please see peripheral RF information.
7) Channel width and channel spacing is 200kHz.
8) Channel Level +3dB over sensitivity, interfering signal a standard carrier wave.

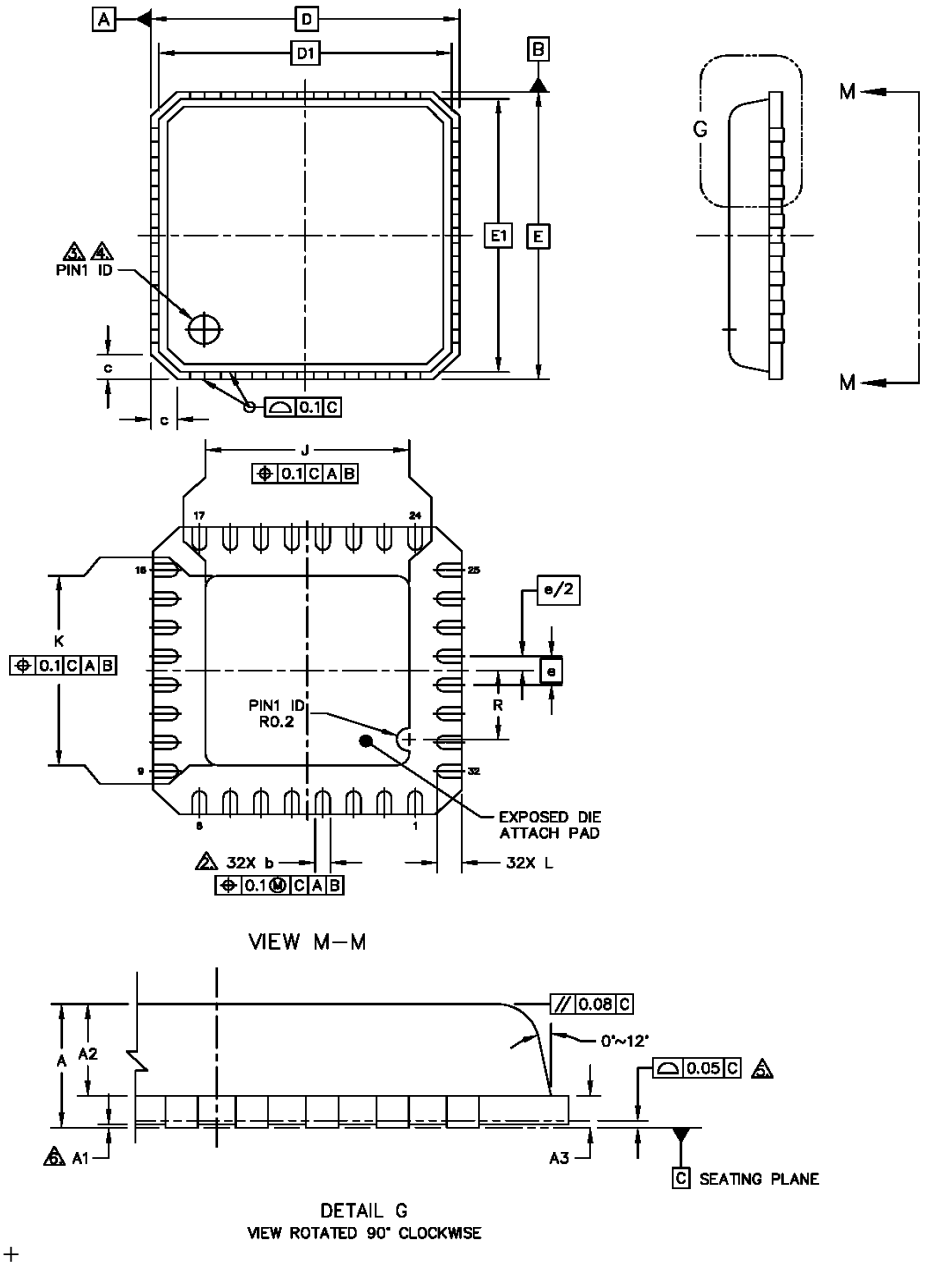
CURRENT CONSUMPTION

MODE	CRYSTAL FREQ. [MHZ]	OUTPUT CLOCK FREQ. [MHZ]	TYPICAL CURRENT
Power Down	16	OFF	2.5 uA
Standby	4	OFF	12 uA
Standby	8	OFF	25 uA
Standby	12	OFF	27 uA
Standby	16	OFF	32 uA
Standby	20	OFF	46 uA
Standby	4	0.5	110 uA
Standby	8	0.5	125 uA
Standby	12	0.5	130 uA
Standby	16	0.5	135 uA
Standby	20	0.5	150 uA
Standby	4	1	130 uA
Standby	8	1	145 uA
Standby	12	1	150 uA
Standby	16	1	155 uA
Standby	20	1	170 uA
Standby	4	2	170 uA
Standby	8	2	185 uA
Standby	12	2	190 uA
Standby	16	2	195 uA
Standby	20	2	210 uA
Standby	4	4	260 uA
Standby	8	4	275 uA
Standby	12	4	280 uA
Standby	16	4	285 uA
Standby	20	4	300 uA
Rx @ 433	16	OFF	12.2 mA
Rx @ 868/915	16	OFF	12.8 mA
Reduced Rx	16	OFF	10.5 mA
Tx @ 10dBm	16	OFF	30 mA
Tx @ 6dBm	16	OFF	20 mA
Tx @ -2dBm	16	OFF	14 mA
Tx @ -10dBm	16	OFF	11 mA
Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load capacitance of external clock = 13pF, Crystal load capacitance = 12pF			

Table 5 nRF905 current consumption.

PACKAGE OUTLINE

nRF905 uses the QFN 32L 5x5 green package with a mat tin finish. Dimensions are in mm. Recommended soldering reflow profile can be found in application note nAN400-08, QFN soldering reflow guidelines, www.nvlsi.no.



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Package Type		A	A_1	A2	b	D	E	e	J	K	L
QFN32	**Min**	0.8	0.0	0.65	0.18				3.2	3.2	0.3
(5x5 mm)	**typ.**				0.23	5 BSC	5 BSC	0.5 BSC	3.3	3.3	0.4
	Max	0.9	0.05	0.69	0.3				3.4	3.4	0.5

Figure 3 nRF905 package outline.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
VDD ..... - 0.3V to + 3.6V
VSS 0V

Input Voltage
V_I ..... - 0.3V to VDD + 0.3V

Output Voltage
V_O ..... - 0.3V to VDD + 0.3V

Total Power Dissipation
P_D (T_A=85°C).....200mW

Temperatures
Operating temperature..... - 40°C to + 85°C
Storage temperature.....- 40°C to + 125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic sensitive device.
Observe precaution for handling.

GLOSSARY OF TERMS

Term	Description
ADC	Analog to Digital Converter
AM	Address Match
CD	Carrier Detect
CLK	Clock
CRC	Cyclic Redundancy Check
DR	Data Ready
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
kSPS	kilo Samples per Second
MCU	Micro Controller Unit
PWR_DWN	Power Down
PWR_UP	Power Up
RX	Receive
SPI	Serial Programmable Interface
CSN	SPI Chip Select Not
MISO	SPI Master In Slave Out
MOSI	SPI Master Out Slave In
SCK	SPI Serial Clock
SPS	Samples per Second
STBY	Standby
TRX_EN	Transmit/Receive Enable
TX	Transmit
TX_EN	Transmit Enable

Table 6 Glossary of terms.

MODES OF OPERATION

The nRF905 has two active (RX/TX) modes and two power-saving modes

Active Modes

- ShockBurst™ RX
- ShockBurst™ TX

Power Saving Modes

- Power down and SPI - programming
- Standby and SPI - programming

The nRF905 mode is decided by the settings of TRX_CE, TX_EN and PWR_UP.

PWR_UP	TRX_CE	TX_EN	Operating Mode
0	X	X	Power down and SPI – programming
1	0	X	Standby and SPI – programming
1	1	0	Radio Enabled - ShockBurst™ RX
1	1	1	Radio Enabled - ShockBurst™ TX

Table 7 nRF905 operational modes.

nRF ShockBurst™ Mode

The nRF905 uses the Nordic VLSI ShockBurst™ feature. ShockBurst™ makes it possible to use the high data rate offered by the nRF905 without the need of a costly, high-speed micro controller (MCU) for data processing/clock recovery. By placing all high speed signal processing related to RF protocol on-chip, the nRF905 offers the application micro controller a simple SPI interface, the data rate is decided by the interface-speed the micro controller itself sets up. By allowing the digital part of the application to run at low speed, while maximizing the data rate on the RF link, the nRF905 ShockBurst™ mode reduces the average current consumption in applications. In ShockBurst™ RX, Address Match (AM) and Data Ready (DR) notifies the MCU when a valid address and payload is received respectively. In ShockBurst™ TX, the nRF905 automatically generates preamble and CRC. Data Ready (DR) notifies the MCU that the transmission is completed. All together, this means reduced memory demand in the MCU resulting in a low cost MCU, as well as reduced software development time.

Typical ShockBurst™ TX:

1. When the application MCU has data for a remote node, the address of the receiving node (TX-address) and payload data (TX-payload) are clocked into nRF905 via the SPI interface. The application protocol or MCU sets the speed of the interface.
2. MCU sets TRX_CE and TX_EN high, this activates a nRF905 ShockBurst™ transmission.
3. nRF905 ShockBurst™:
   - Radio is automatically powered up.
   - Data package is completed (preamble added, CRC calculated).
   - Data package is transmitted (100kbps, GFSK, Manchester-encoded).
   - Data Ready is set high when transmission is completed.
4. If AUTO_RETRAN is set high, the nRF905 continuously retransmits the package until TRX_CE is set low.
5. When TRX_CE is set low, the nRF905 finishes transmitting the outgoing package and then sets itself into standby mode.

The ShockBurst™ mode ensures that a transmitted package that has started always finishes regardless of what TRX_EN and TX_EN is set to during transmission. The new mode is activated when the transmission is completed. Please see subsequent chapters for detailed timing

For test purposes such as antenna tuning and measuring output power it is possible to set the transmitter so that a constant carrier is produced. To do this TRX_CE must be maintained high instead of being pulsed. In addition Auto Retransmit should be switched off. After the burst of data has been sent then the device will continue to send the unmodulated carrier.

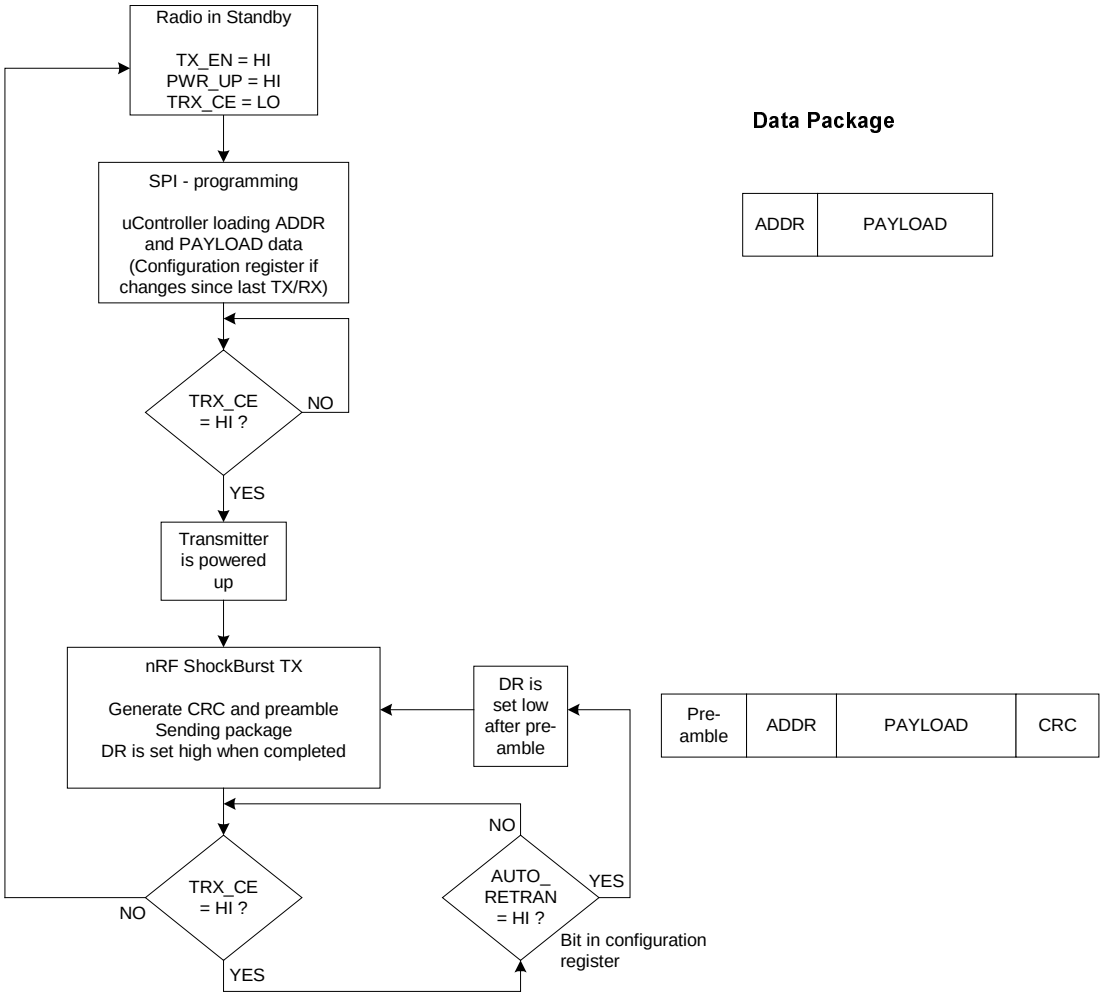


Figure 4 Flowchart ShockBurst™ transmit of nRF905.

NB: DR is set low under the following conditions after it has been set high:

- If TX_EN is set low
- If PWR_UP is set low

Typical ShockBurst™ RX:

1. ShockBurst™ RX is selected by setting TRX_CE high and TX_EN low.
2. After 650µs nRF905 is monitoring the air for incoming communication.
3. When the nRF905 senses a carrier at the receiving frequency, Carrier Detect (CD) pin is set high.
4. When a valid address is received, Address Match (AM) pin is set high.
5. When a valid package has been received (correct CRC found), nRF905 removes the preamble, address and CRC bits, and the Data Ready (DR) pin is set high.
6. MCU sets the TRX_CE low to enter standby mode (low current mode).
7. MCU can clock out the payload data at a suitable rate via the SPI interface.
8. When all payload data is retrieved, nRF905 sets Data Ready (DR) and Address Match (AM) low again.
9. The chip is now ready for entering ShockBurst™ RX, ShockBurst™ TX or power down mode.

If TRX_CE or TX_EN is changed during an incoming package, the nRF905 changes mode immediately and the package is lost. However, if the MCU is sensing the Address Match (AM) pin, it knows when the chip is receiving an incoming package and can therefore decide wheather to wait for the Data Ready (DR) signal or enter a different mode.

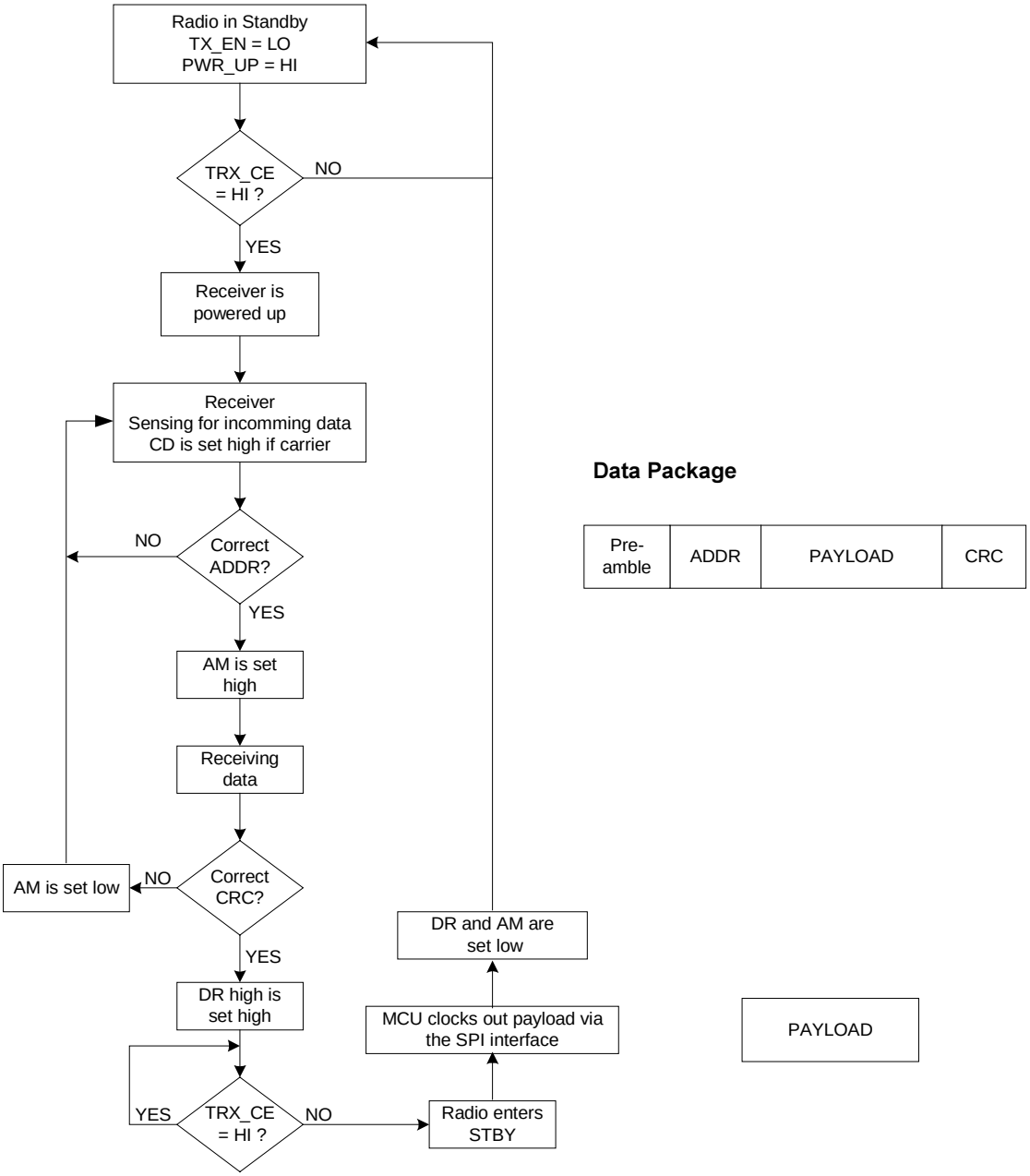


Figure 5 Flowchart ShockBurst™ receive of nRF905.

Power Down Mode

In power down the nRF905 is disabled with minimal current consumption, typically less than 2.5μA. When entering this mode the device is not active which will minimize average current consumption and maximizing battery lifetime. The configuration word content is maintained during power down.

Standby Mode

Standby mode is used to minimize average current consumption while maintaining short start up times to ShockBurst™ RX and ShockBurst™ TX. In this mode part of the crystal oscillator is active. Current consumption is dependent on crystal frequency, Ex: I_{DD}= 12μA @4MHz and I_{DD} =46μA @20MHz. If the uP-clock (pin 3) of nRF905 is enabled, current consumption increases and is dependent on the load capacitance and frequency. The configuration word content is maintained during standby.

DEVICE CONFIGURATION

All configuration of the nRF905 is via the SPI interface. The interface consists of five registers; a SPI instruction set is used to decide which operation shall be performed. The SPI interface can only be activated when the chip is in standby or power down mode.

SPI Register Configuration

The SPI interface consists of five internal registers. A register read-back mode is implemented to allow verification of the register contents.

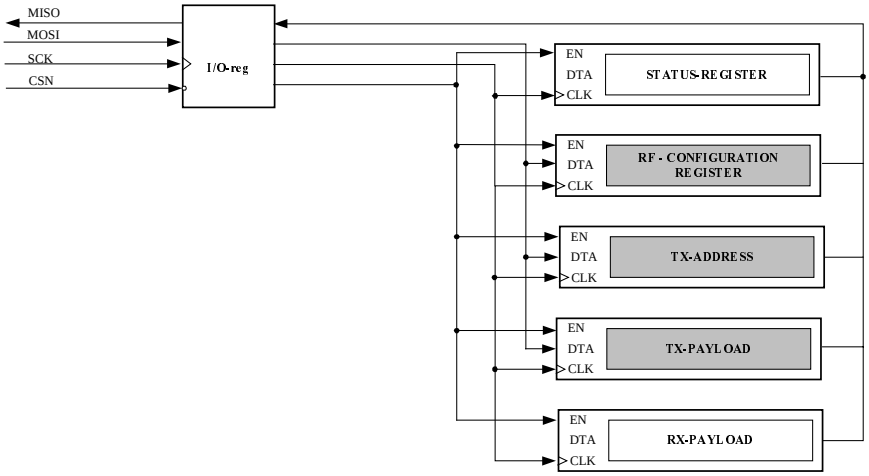


Figure 6 SPI – interface and the five internal registers.

Status – Register

Register contains status of Data Ready (DR) and Address Match (AM).

RF - Configuration Register

Register contains transceiver setup information such as frequency and output power ext.

TX – Address

Register contains address of target device. How many bytes used is set in the configuration register.

TX – Payload

Register containing the payload information to be sent in a ShockBurst ™ package. How many bytes used is set in the configuration register.

RX – Payload

Register containing the payload information derived from a received valid ShockBurst ™ package. How many bytes used is set in the configuration register. Valid data in the RX-Payload register is indicated with a high Date Ready (DR) signal.

SPI Instruction Set

The available commands to be used on the SPI interface is shown below. Whenever CSN is set low the interface expects an instruction. Every new instruction must be started by a high to low transition on CSN.

Instruction set for the nRF905 SPI Serial Interface		
Instruction Name	**Instruction Format**	**Operation**
W_CONFIG (WC)	0000 AAAA	Write Configuration-register. AAAA indicates which byte the write operation is to be started from. Number of bytes depends on start address AAAA.
R_CONFIG (RC)	0001 AAAA	Read Configuration-register. AAAA indicates which byte the read operation is to be started from. Number of bytes depends on start address AAAA.
W_TX_PAYLOAD (WTP)	0010 0000	Write TX-payload: 1 – 32 bytes. A write operation will always start at byte 0.
R_TX_PAYLOAD (RTP)	0010 0001	Read TX-payload: 1 – 32 bytes. A read operation will always start at byte 0.
W_TX_ADDRESS (WTA)	0010 0010	Write TX-address: 1 – 4 bytes. A write operation will always start at byte 0.
R_TX_ADDRESS (RTA)	0010 0011	Read TX-address: 1 – 4 bytes. A read operation will always start at byte 0
R_RX_PAYLOAD (RRP)	0010 0100	Read RX-payload: 1 – 32 bytes. A read operation will always start at byte 0.
CHANNEL_CONFIG (CC)	1000 pphc cccc cccc	Special command for fast setting of CH_NO, HFREQ_PLL and PA_PWR in the CONFIGURATION REGISTER. CH_NO= ccccccccc, HFREQ_PLL = h PA_PWR = pp

Table 8 Instruction set for the nRF905 SPI interface.

A read or a write operation may operate on a single byte or on a set of succeeding bytes from a given start address defined by the instruction. When accessing succeeding bytes one will read or write MSB of the byte with the smallest byte number first. The content of the status-register will always be read to MISO after a high to low transition on CSN.

SPI Timing

Data is clocked into or out of the device on the rising edge of the clock pulse. The clock speed is determined by the MCU and may be from 1Hz to 10MHz depending on the MCU. The device must be in one of the power saving modes for the configuration registers to be read or written to.

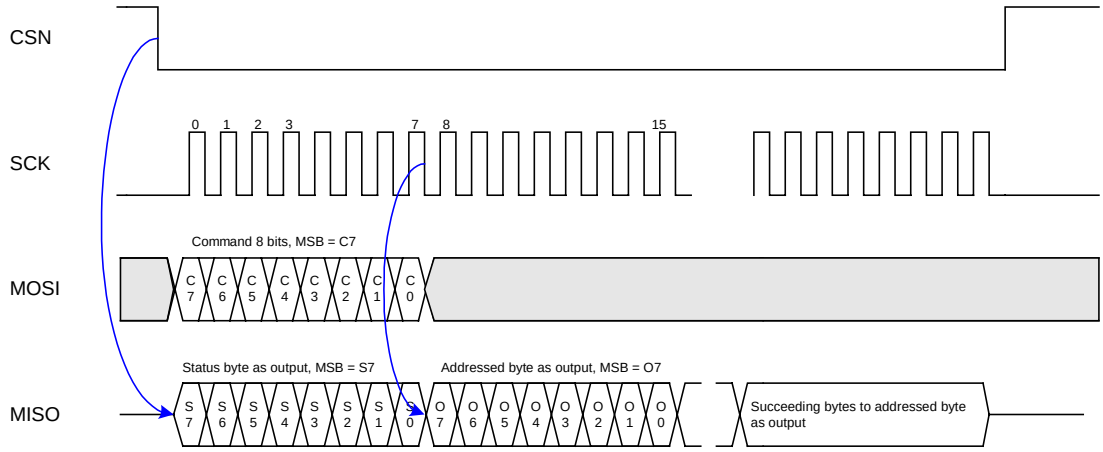


Figure 7 SPI read operation.

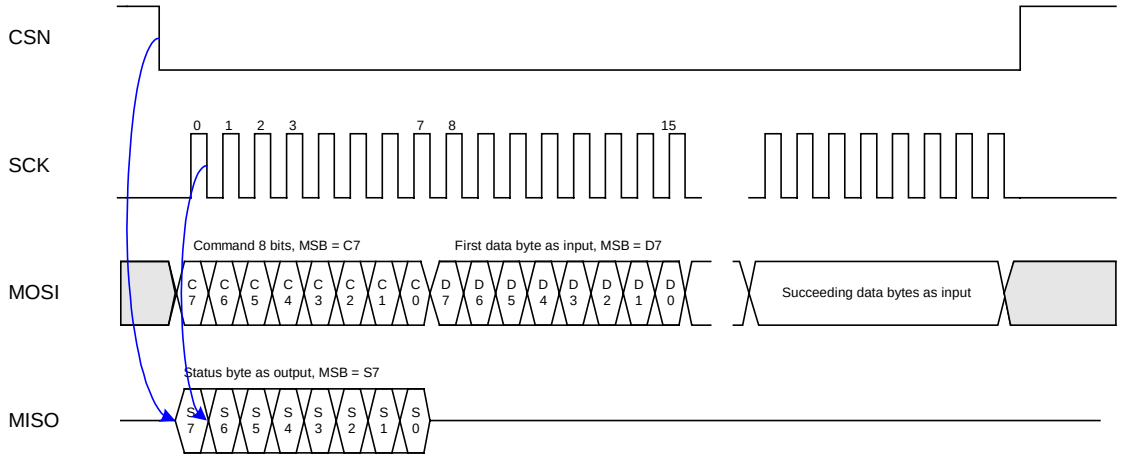


Figure 8 SPI write operation.

RF - Configuration – Register Description

Parameter	Bitwidth	Description
CH_NO	9	Sets center freq. together with HFREQ_PLL (default = $001101100_b = 108_d$). $f_{RF} = (422.4 + CH\_NO_d /10)*(1+HFREQ\_PLL_d)$ MHz
HFREQ_ PLL	1	Sets PLL in 433 or 868/915 MHz mode (default = 0). '0' – Chip operating in 433MHz band '1' – Chip operating in 868 or 915 MHz band
PA_PWR	2	Output power (default = 00). '00' -10dBm '01' -2dBm '10' +6dBm '11' +10dBm
RX_RED_ PWR	1	Reduces current in RX mode by 1.6mA. Sensitivity is reduced (default = 0). '0' – Normal operation '1' – Reduced power
AUTO_ RETRAN	1	Retransmit contents in TX register if TRX_CE and TXEN are high (default = 0). '0' – No retransmission '1' – Retransmission of data package
RX_AFW	3	RX-address width (default = 100). '001' – 1 byte RX address field width '100' – 4 byte RX address field width
TX_AFW	3	TX-address width (default = 100). '001' – 1 byte TX address field width '100' – 4 byte TX address field width
RX_PW	6	RX-payload width (default = 100000). '000001' – 1 byte RX payload field width '000010' – 2 byte RX payload field width . '100000' – 32 byte RX payload field width
TX_PW	6	TX-payload width (default = 100000). '000001' – 1 byte TX payload field width '000010' – 2 byte TX payload field width . '100000' – 32 byte TX payload field width
RX_ ADDRESS	32	RX address identity. Used bytes depend on RX_AFW (default = $E7E7E7E7_h$).
UP_CLK_ FREQ	2	Output clock frequency (default = 11). '00' – 4MHz '01' – 2MHz '10' – 1MHz '11' – 500kHz
UP_CLK_ EN	1	Output clock enable (default = 1). '0' – No external clock signal available '1' – External clock signal enabled
XOF	3	Crystal oscillator frequency. Must be set according to external crystal resonant-frequency (default = 100). '000' – 4MHz '001' – 8MHz '010' – 12MHz '011' – 16MHz '100' – 20MHz
CRC_EN	1	CRC – check enable (default = 1). '0' – Disable '1' – Enable
CRC_ MODE	1	CRC – mode (default = 1). '0' – 8 CRC check bit '1' – 16 CRC check bit

Table 9 Configuration-register description.

Register Contents

RF-CONFIG_REGISTER (R/W)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	CH_NO[7:0]	0110_1100
1	bit[7:6] not used, AUTO_RETRAN, RX_RED_PWR, PA_PWR[1:0], HFREQ_PLL, CH_NO[8]	0000_0000
2	bit[7] not used, TX_AFW[2:0] , bit[3] not used, RX_AFW[2:0]	0100_0100
3	bit[7:6] not used, RX_PW[5:0]	0010_0000
4	bit[7:6] not used, TX_PW[5:0]	0010_0000
5	RX_ADDRESS (device identity) byte 0	E7
6	RX_ADDRESS (device identity) byte 1	E7
7	RX_ADDRESS (device identity) byte 2	E7
8	RX_ADDRESS (device identity) byte 3	E7
9	CRC_MODE,CRC_EN, XOF[2:0], UP_CLK_EN, UP_CLK_FREQ[1:0]	1110_0111

TX_PAYLOAD (R/W)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	TX_PAYLOAD[7:0]	X
1	TX_PAYLOAD[15:8]	X
-	-	X
-	-	X
30	TX_PAYLOAD[247:240]	X
31	TX_PAYLOAD[255:248]	X

TX_ADDRESS (R/W)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	TX_ADDRESS[7:0]	E7
1	TX_ADDRESS[15:8]	E7
2	TX_ADDRESS[23:16]	E7
3	TX_ADDRESS[31:24]	E7

RX_PAYLOAD (R)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	RX_PAYLOAD[7:0]	X
1	RX_PAYLOAD[15:8]	X
	-	X
	-	X
30	RX_PAYLOAD[247:240]	X
31	RX_PAYLOAD[255:248]	X

STATUS_REGISTER (R)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	AM, bit [6] not used, DR, bit [0:4] not used	X

Table 10 RF register contents.

The length of all registers is fixed. However, the bytes in TX_PAYLOAD, RX_PAYLOAD, TX_ADDRESS and RX_ADDRESS used in ShockBurst ™ RX/TX are set in the configuration register. Register content is not lost when the device enters one of the power saving modes.

IMPORTANT TIMING DATA

The following timing must be obeyed during nRF905 operation.

Device Switching Times

nRF905 timing	Max.
PWR_DWN ➔ ST_BY mode	3 ms
STBY ➔ TX Shock Burst™	650 µs
STBY ➔ RX Shock Burst™	650 µs
RX Shock Burst™ ➔ TX Shock Burst™	550 [1]µs
TX Shock Burst™ ➔ RX Shock Burst™	550 [1]µs

Notes to table:

1) RX to TX or TX to RX switching is available without re-programming of the RF configuration register. The same frequency channel is maintained.

Table 11 Switching times for nRF905.

ShockBurst™ TX timing

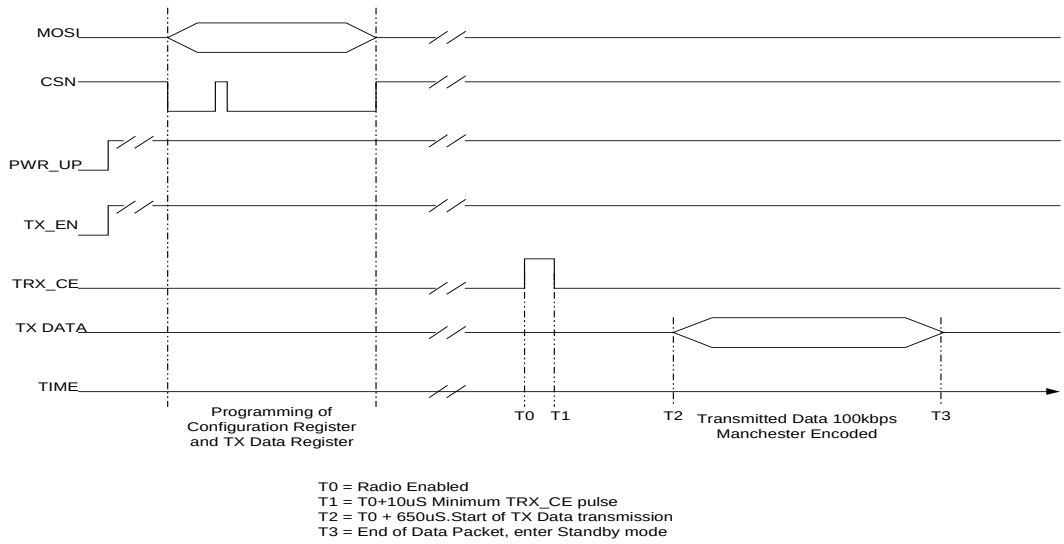


Figure 9 Timing diagram for standby to transmit.

After a data packet has finished transmitting the device will automatically enter Standby mode and wait for the next pulse of TRX_CE. If the Auto Re-Transmit function is enabled the data packet will continue re-sending the same data packet until TRX_CE is set low.

ShockBurst™ RX timing

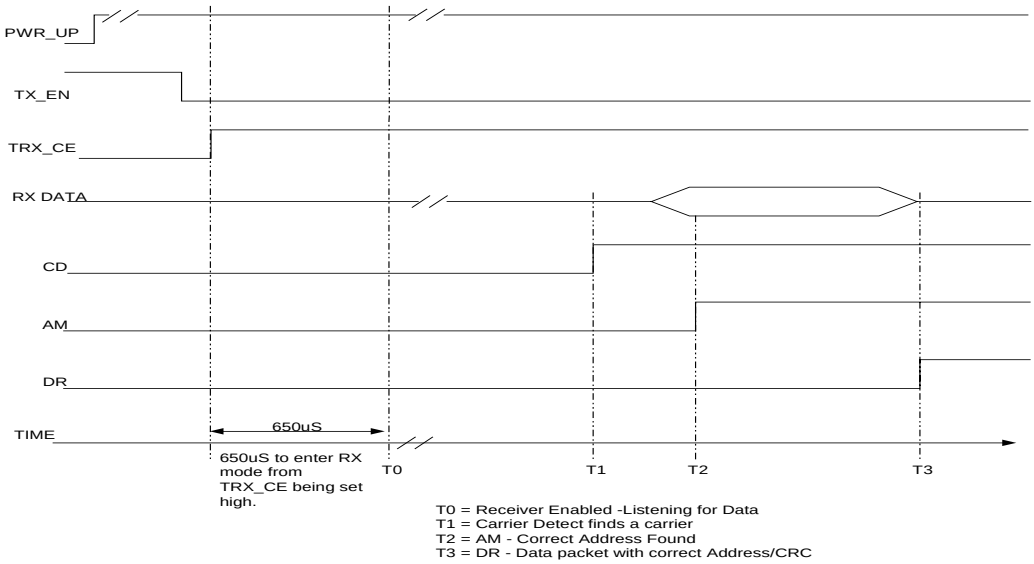


Figure 10 Timing diagram for standby to receiving.

After the Data Ready (DR) has been set high a valid data packet is available in the RX data register. This may be clocked out in RX mode or standby mode or even power down mode. After the data has been clocked out via the SPI interface the Data Ready (DR) and Address Match (AM) pins are reset to low.

PERIPHERAL RF INFORMATION

Crystal Specification

Tolerance includes initially accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance @ 868/915 MHz	Tolerance @ 433 MHz
4MHz	12pF	150Ω	7.0pF	±30ppm	±60ppm
8MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm
12MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm
16MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm
20MHz	12pF	100Ω	7.0pF	±30ppm	±60ppm

Table 12 Crystal specification of nRF905.

To achieve a crystal oscillator solution with low power consumption and fast start-up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying C_L =12pF is acceptable, but it is possible to use up to 16pF. Specifying a lower value of crystal parallel equivalent capacitance, Co=1.5pF is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_max=7.0pF.

External Clock Reference

An external reference clock, such as a MCU clock, may be used instead of a crystal. The clock signal should be applied directly to the XC1 pin, the XC2 pin can be left high impedance. When operating with an external clock instead of a crystal the clock must be applied in standby mode to achieve low current consumption. If the device is set into standby mode with no external clock or crystal then the current consumption will increase up to a maximum of 1mA.

Microprocessor Output Clock

By default a microprocessor clock output is provided. Providing an output clock will increase the current consumption in standby mode. The current consumption in standby will depend on frequency and load of external crystal, frequency of output clock and capacitive load of the provided output clock. Typical current consumption values are found in Table 5

Antenna Output

The "ANT1 & ANT2" output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either via a RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700Ω. A low load impedance (for instance 50Ω) can be obtained by fitting a simple matching network or a RF transformer (balun). Further information regarding balun structures and matching networks may be found in the Application Examples chapter.

Output Power Adjustment

The power amplifier in nRF905 can be programmed to four different output power settings by the configuration register. By reducing output power, the total TX current is reduced.

Power setting	RF output power	DC current consumption
00	-10 dBm	11.0 mA
01	-2 dBm	14.0 mA
10	6 dBm	20.0 mA
11	10 dBm	30.0 mA
Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 400 Ω.		

Table 13 RF output power setting for the nRF905**.**

Modulation

The modulation of nRF905 is Gaussian Frequency Shift Keying (GFSK) with a data-rate of 100kbps. Deviation is ±50kHz. GFSK modulation results in a more bandwidth effective transmission-link compared with ordinary FSK modulation.

The data is internally Manchester encoded (TX) and Manchester decoded (RX). That is, the effective symbol-rate of the link is 50kbps. By using internally Manchester encoding, no scrambling in the u-controller is needed.

Output Frequency

The operating RF-frequency of nRF905 is set in the configuration register by CH_NO and HFREQ_PLL. The operating frequency is given by:

$$f_{OP} = (422.4 + (CH\_NO/10)) \cdot (1 + HFREQ\_PLL)\ MHz$$

When HFREQ_PLL is '0' the frequency resolution is 100kHz and when it is '1' the resolution is 200kHz.
The application operating frequency has to be chosen to apply with the Short Range Devise regulation in the area of operation.

Operating frequency	HFREQ_PLL	CH_NO
430.0 MHz	[0]	[001001100]
433.1 MHz	[0]	[001101011]
433.2 MHz	[0]	[001101100]
434.7 MHz	[0]	[001111011]
862.0 MHz	[1]	[001010110]
868.2 MHz	[1]	[001110101]
868.4 MHz	[1]	[001110110]
869.8 MHz	[1]	[001111101]
902.2 MHz	[1]	[100011111]
902.4 MHz	[1]	[100100000]
927.8 MHz	[1]	[110011111]

Table 14 Examples of real operating frequencies.

PCB Layout and Decoupling Guidelines

nRF905 is an extremely robust RF device due to internal voltage regulators and requires the minimum of RF layout protocols. However the following design rules should still be incorporated into the layout design.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF905 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. It is preferable to mount a large surface mount capacitor (e.g. 4.7µF tantalum) in parallel with the smaller value capacitors. The nRF905 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF905 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to place via holes as close as possible to the VSS pins. A minimum of one via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

A fully qualified RF-layout for the nRF905 and its surrounding components, including antennas and matching networks, can be downloaded from **www.nvlsi.no**.

nRF905 FEATURES

Carrier Detect.

When the nRF905 is in ShockBurst ™ RX, the Carrier Detect (CD) pin is set high if a RF carrier is present at the channel the device is programmed to. This feature is very effective to avoid collision of packages from different transmitters operating at the same frequency. Whenever a device is ready to transmit it could first be set into receive mode and sense whether or not the wanted channel is available for outgoing data. This forms a very simple listen before transmit protocol. Operating Carrier Detect (CD) with Reduced RX Power mode is an extremely power efficient RF system. Typical Carrier Detect level (CD) is typically 5dB lower than sensitivity, i.e. if sensitivity is –100dBm then the Carrier Detect function will sense a carrier wave as low as –105dBm. Below –105dBm the Carrier Detect signal will be low, i.e. 0V. Above –95dBm the Carrier Detect signal will be high, i.e. Vdd. Between –105 to 106 the Carrier Detect Signal will toggle.

Address Match

When the nRF905 is in ShockBurst ™ RX mode, the Address Match (AM) pin is set high as soon as an incoming package with an address that is identical with the device's own identity is received. With the Address Match pin the controller is alerted that the nRF905 is receiving data actually before the Data Ready (DR) signal is set high. If the Data Ready (DR) pin is not set high i.e. the CRC is incorrect then the Address Match (AM) pin is reset to low at the end of the received data packet. This function can be very useful for an MCU. If Address Match (AM) is high then the MCU can make a decision to wait and see if Data Ready (DR) will be set high indicating a valid data package has been received or ignore that a possible package is being received and switch modes.

Data Ready

The Data Ready (DR) signal makes it possible to largely reduce the complexity of the MCU software program.
In ShockBurst ™ TX, the Data Ready (DR) signal is set high when a complete package is transmitted, telling the MCU that the nRF905 is ready for new actions. It is reset to low at the start of a new package transmission or when switched to a different mode i.e. receive mode or standby mode.
In ShockBurst ™ TX Auto Retransmit the Data Ready (DR) signal is set high at the beginning of the pre-amble and is set low at the end of the preamble. The Data Ready (DR) signal therefore pulses at the beginning of each transmitted data packet.
In ShockBurst ™ RX, the signal is set high when nRF905 has received a valid package, i.e. a valid address, package length and correct CRC. The MCU can then retrieve the payload via the SPI interface. The Data Ready (DR) pin is reset to low once the data has been clocked out of the data buffer or the device is switched to transmit mode.

Auto Retransmit

One way to increase system reliability in a noisy environment or in a system without collision control is to transmit a package several times. This is easily accomplished with the Auto Retransmit feature in nRF905. By setting the AUTO_RETRAN bit to "1" in the configuration register, the circuit keeps sending the same data package as long as TRX_CE and TX_EN is high. As soon as TRX_CE is set low the device will finish sending the packet it is currently transmitting and then return to standby mode.

RX Reduced Power Mode

To maximize battery lifetime in application where the nRF905 high sensitivity is not necessary; nRF905 offers a built in reduced power mode. In this mode, the receive current consumption reduces from 12.5mA to only 10.5mA. The sensitivity is reduced to typical –85dBm, ±10dB. Some degradation of the nRF905 blocking performance should be expected in this mode. The reduced power mode is an excellent option when using Carrier Detect to sense if the wanted channel is available for outgoing data.

APPLICATION EXAMPLE, DIFFERENTIAL CONNECTION TO A LOOP ANTENNA

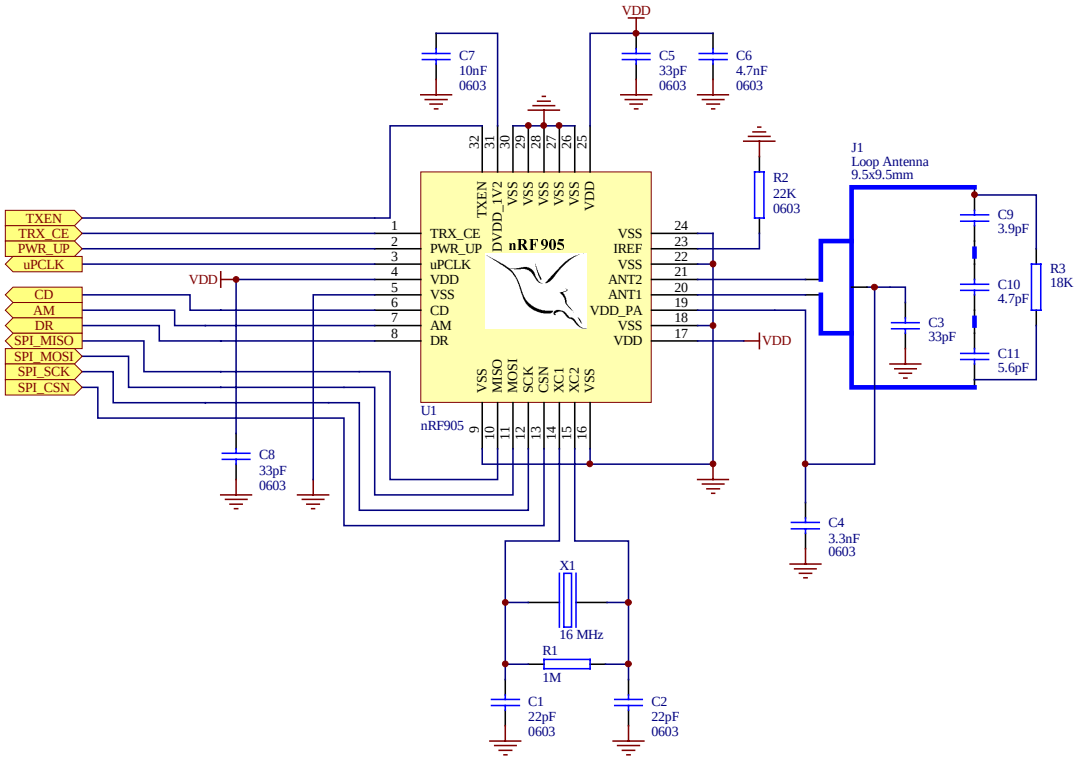


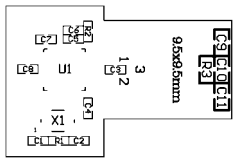
Figure 11 nRF905 Application schematic, differential connection to a loop antenna (868MHz).

Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C3	NP0 ceramic chip capacitor, (PA supply decoupling)	0603	33	±5%	pF
C4	X7R ceramic chip capacitor, (PA supply decoupling)	0603	3.3	±10%	nF
C5	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	10	±10%	nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C9	NP0 ceramic chip capacitor, (Antenna tuning)	0603	3.9	±0.1	pF
C10	NP0 ceramic chip capacitor, (Antenna tuning)	0603	4.7	±0.1	pF
C11	NP0 ceramic chip capacitor, (Antenna tuning)	0603	5.6	±0.1	pF
R1	0.1W chip resistor, (Crystal oscillator bias)	0603	1	±1%	MΩ
R2	0.1W chip resistor, (Reference bias)	0603	22	±1%	kΩ
R3	0.1W chip resistor, (Antenna Q reduction)	0603	18	±1%	kΩ
U1	**nRF905** Transceiver	QFN32L/5x5			
X1	Crystal	LxWxH = 4.0x2.5x0.8	16	±30ppm	MHz

Table 15 Recommended external components, differential connection to a loop antenna (868MHz).

PCB LAYOUT EXAMPLE, DIFFERENTIAL CONNECTION TO A LOOP ANTENNA

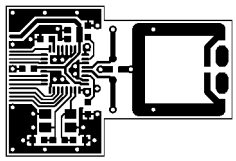
Figure 12 shows a PCB layout example for the application schematic in Figure 11. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.



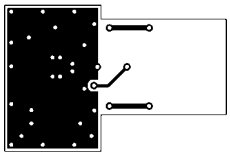
a) Top silk screen

No components in bottom layer

b) Bottom silk screen



c) Top view

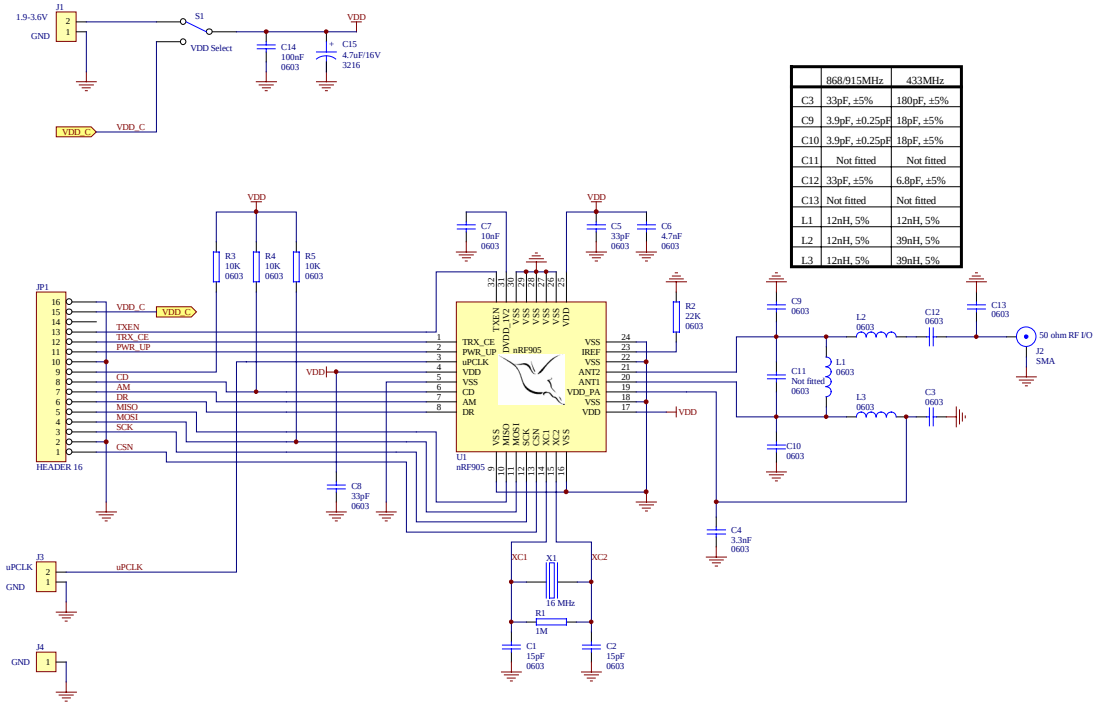


d) Bottom view

Figure 12 PCB layout example for nRF905, differential connection to a loop antenna.

A fully qualified RF-layout for the nRF905 and its surrounding components, including antennas and matching networks, can be downloaded from **www.nvlsi.no**.

APPLICATION EXAMPLE, SINGLE ENDED CONNECTION TO 50Ω ANTENNA



	868/915MHz	433MHz
C3	33pF, ±5%	180pF, ±5%
C9	3.9pF, ±0.25pF	18pF, ±5%
C10	3.9pF, ±0.25pF	18pF, ±5%
C11	Not fitted	Not fitted
C12	33pF, ±5%	6.8pF, ±5%
C13	Not fitted	Not fitted
L1	12nH, 5%	12nH, 5%
L2	12nH, 5%	39nH, 5%
L3	12nH, 5%	39nH, 5%

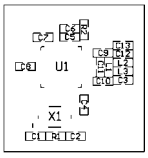
Figure 13 nRF905 Application schematic, single ended connection to 50Ω antenna by using a differential to single ended matching network.

Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C3	NP0 ceramic chip capacitor, (PA supply decoupling) @ 433MHz @ 868MHz @ 915MHz	0603	 180 33 33	±5%	pF
C4	X7R ceramic chip capacitor, (PA supply decoupling)	0603	3.3	±10%	nF
C5	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	10	±10%	nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C9	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 18 3.9 3.9	 ±5% <±0.25pF <±0.25pF	pF
C10	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 18 3.9 3.9	 ±5% <±0.25pF <±0.25pF	pF
C11	NP0 ceramic chip capacitor, (Impedance matching)	0603	Not fitted		pF
C12	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 6.8 33 33	 ±5% ±5% ±5%	pF
C13	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 Not fitted Not fitted Not fitted		pF
L1	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	 12 12 12	±5%	nH
L2	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	 39 12 12	 ±5% ±5% ±5%	nH
L3	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	 39 12 12	 ±5% ±5% ±5%	nH
R1	0.1W chip resistor, (Crystal oscillator bias)	0603	1	±1%	MΩ
R2	0.1W chip resistor, (Reference bias)	0603	22	±1%	kΩ
R3	0.1W chip resistor, (Antenna Q reduction)	0603	18	±1%	kΩ
U1	**nRF905** Transceiver	QFN32L/5x5			
X1	Crystal	LxWxH = 4.0x2.5x0.8	16	±30ppm	MHz

Table 16 Recommended external components, single ended connection to 50Ω antenna.

PCB LAYOUT EXAMPLE, SINGLE ENDED CONNECTION TO 50Ω ANTENNA

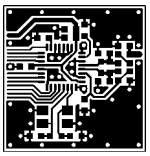
Figure 14 shows a PCB layout example for the application schematic in Figure 13. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.



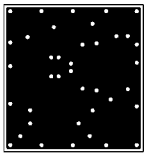
a) Top silk screen

No components in bottom layer

b) Bottom silk screen



c) Top view



d) Bottom view

Figure 14 PCB layout example for nRF905, single ended connection to 50Ω antenna by using a differential to single ended matching network.

A fully qualified RF-layout for the nRF905 and its surrounding components, including antennas and matching networks, can be downloaded from **www.nvlsi.no**.