Cyclone FPGA Series Package & I/O Matrix

104 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

Unless noted, all Cyclone® series devices are offered in commercial and industrial temperatures and lead-free packages.

		Cyclone II (1.2 V) Low Cost, High Volume									Cyclone (1.5 V) Low Cost, High Volume				
		EP2C5	EP2C8	EP2C8A[1]	EP2C15A[1]	EP2C20	EP2C20A[1]	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Thin Quad Flat Pack (T)	100-Pin TQFP										65				
	144-Pin TQFP	89	85								104		98		
Plastic Quad Flat Pack (Q)	208-Pin PQFP	142	138												
	240-Pin PQFP					142							185	173	
FineLine BGA® (F)	256-Pin FBGA	158	182	182	152	152	152						185	185	
	324-Pin FBGA											249		249	233
	400-Pin FBGA											301			301
	484-Pin FBGA				315	315	315	322	294						
	484-Pin UFBGA[2]							322	294						
	672-Pin FBGA							475	450	422					
	896-Pin FBGA									622					

[1] "A" devices differ only in reduced "power on reset" times.

[2] Ultra FineLine BGA.

Package Statistics	TQFP		PQFP		FBGA						UBGA
Number of Pins	100	144	240	208	256	324	400	484	672	896	484
Package Technology	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond	Wirebond
Nominal Length x Width (mm)	16 x 16	22 x 22	35 x 35	31 x 31	17 x 17	19 x 19	21 x 21	23 x 23	27 x 27	31 x 31	19 x 19
Maximum Surface Area (mm)[1]	262	493	1,215	952	296	369	449	538	740	974	369
Maximum Height (mm)	1.2	1.6	4.1	4.1	1.55	2.6	2.6	2.6	2.6	2.6	2.2
Nominal Lead Pitch (mm)	0.5	0.5	0.5	0.5	1	1	1	1	1	1	0.8
Maximum Lead Width (mm)	0.27	0.27	0.27	0.27	0.7	0.7	0.7	0.7	0.7	0.7	0.6

[1] Altera's maximum height specification is 2.6 mm. The 3.5 maximum height specification shown reflects the JEDEC specifications.

Configuration Devices	EP2C5	EP2C8	EP2C15	EP2C20	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Configuration File Size (Mbits)	1.26	1.98	3.89	3.89	6.85	9.96	14.31	0.63	0.93	1.17	2.32	3.56
Number of EPCS1 Devices (1 Mbit)	1	–	–	–	–	–	–	1	1	1	–	–
Number of EPCS4 Devices (4 Mbits)	1	1	1	1	–	–	–	1	1	1	1	1
Number of EPCS16 Devices (16 Mbits)	1	1	1	1	1	1	1	–	–	–	–	–
Number of EPCS64 Devices (64 Mbits)	1	1	1	1	1	1	1	–	–	–	–	–
Number of EPC2 Devices (1.6 Mbits)	1	1	2	2	4	5	7	1	1	1	2	2
Number of EPC4 Devices (4 Mbits)	1	1	1	1	–	–	–	1	1	1	1	1
Number of EPC8 Devices (8 Mbits)	1	1	1	1	1	1	–	1	1	1	1	1
Number of EPC16 Devices (16 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1

[1] K = 1,000 [2] Kbits = 1,024 bits [3] Requires external PHY device

Cyclone FPGA Series Features

		Cyclone II (1.2 V) Low Cost, High Volume							Cyclone (1.5 V) Low Cost, High Volume				
		EP2C5	EP2C8	EP2C15[2]	EP2C20	EP2C35	EP2C50	EP2C70	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Density & Speed	Logic Elements	4,608	8,256	14,448	18,752	33,216	50,528	68,416	2,910	4,000	5,980	12,060	20,060
	Total RAM Bits (K)[1]	120	166	240	240	484	594	1,152	60	78	92	240	295
	M4K RAM Blocks (4 Kbits + 512 Parity Bits)[2]	26	36	52	52	105	129	250	13	17	20	52	64
	Speed Grades (Fastest to Slowest)	-6, -7, -8							-6, -7, -8				
Architectural Features	Embedded Processor Available	Nios® II							Nios II				
	18-Bit x 18-Bit/9-Bit x 9-Bit Embedded Multipliers	13/26	18/36	26/52	26/52	35/70	86/172	150/300	–	–	–	–	–
	I/O Registers per I/O Element	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Global & Regional Clock Networks	8	8	16	16	16	16	16	8	8	8	8	8
	PLLs/Unique Outputs	2/6	2/6	4/12	4/12	4/12	4/12	4/12	1/3	2/6	2/6	2/6	2/6
	Industrial Device Offering	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	Lead-Free Device Offering	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O Features	I/O Voltage Levels Supported (V)	1.5, 1.8, 2.5, 3.3							1.5, 1.8, 2.5, 3.3				
	I/O Standards Supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I & II), Differential SSTL-2 (I & II), 1.5-V Differential HSTL (I & II), 1.8-V Differential HSTL (I & II), SSTL-18 (I & II), SSTL-2 (I & II), 1.5-V HSTL (I & II), PCI, PCI-X, PCI Express[3], LVTTL, LVCMOS							LVDS, RSDS, Differential SSTL-2, SSTL-2 (I & II), SSTL-3 (I & II), PCI, LVTTL, LVCMOS				
	LVDS Maximum Data Rate (Mbps) (Receive/Transmit)	805/640	805/640	805/640	805/640	805/640	805/640	805/640	640/640	640/640	640/640	640/640	640/640
	LVDS Channels	60	79	136	136	209	197	265	34	129	72	103	129
	RSDS Maximum Data Rate (Mbps) (Transmit)	311	311	311	311	311	311	311	311	311	311	311	311
	Mini-LVDS Maximum Data Rate (Mbps) (Transmit)	311	311	311	311	311	311	311	–	–	–	–	–
	Series On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
	Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
External Memory Interfaces	Memory Devices Supported	QDRII, DDR2, DDR, SDR							DDR, SDR				
	MegaCore® Controller With Clear Text Datapath	✓							✓				
	System Timing Analysis	✓							✓				
	Board Layout Guidelines	✓							✓				

[1] K = 1,00

[2] Kbits = 1,024 bits

[3] Requires external PHY device

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