AppoTech
卓荣集成

CW6676B

Bluetooth Headphone Microcontroller

Product Spec

[CW6676B-PS-EN]

Versions:1.1.0

Release Date: 2016/9/23

Unit705-707,7/F IC Development Centre,
No.6 Science Park West Ave,
Hong Kong Science Apark,
Shation,N.T.,HongKong.
香港新界沙田香港科学园科技大道西6号
集成电路开发中心7楼705-707室

Tel 电话: (852)26074090
Fax传真: (852)26074096
info@appotech.com

www.appotech.com www.buildwin.com

Table of content

Table of content II
1 Product Overview 1
1.1 Outline 1
1.2 Features 1
2 Pin Definitions 2
2.1 CW6676B 2
2.1.1 Package 2
2.1.2 Pin Assignment 2
2.1.3 Pin Description 2
3 Characteristics 5
3.1 PMU Parameters 5
3.2 CORE PLL Parameters 5
3.3 General purpose I/O Parameters 5
3.4 Audio ADDA Parameters 6
3.5 RF Analog Blocks 6
4 Package Outline Dimensions 8
4.1 QFN32 8
Revision History 10

Copyright © 2016, www.appotech.com. All Rights Reserved.

1 Product Overview

1.1 Outline

CW6676B is an MCS-51™ Compatible high performance mixed signal microcontroller. It integrates advanced digital and analog peripherals to suit for Bluetooth headphone applications. It has internal 4M bit FLASH (MCP FLASH) to store code and data.DAC support dual channel mode.CW6676B package is QFN32.

1.2 Features

- CPU Compatible with MCS-51TM instruction set;
- Supports Bluetooth v.4.2+EDR; backward-compatible with BT v.1.2, 2.0 and 2.1
- Support SCMS-T content protection method;
- Support HFP v1.6, HSP v1.2, A2DP 1.3, AVCTP 1.4, AVDTP 1.3 and AVRCP 1.5
- Class 2 power level, RF Performance: Tx:0dBm, Rx: -85dBm;
- Support simple pairing and auto reconnection function;
- Four Channels 10-bit SARADC;
- Support 16bit Stereo DAC with >90dB SNR, embedded with two class A/B headphone amplifier
- 16bit Mono ADC with >90dB DR
- Support Audio record function to MIC ADPCM;
- Two 8-bit timers, support Capture and PWM mode;
- Two 16-bit timers, support Capture and PWM mode;
- Watchdog Timer with on-chip RC oscillator;
- Support full-duplex IIS, UART, SPI interface;
- 2 channels 4 levels Low Voltage Detector;
- Power on Reset
- Support Full speed USB 2.0 PHY;
- Full speed USB 2.0 HOST/DEVICE controller;
- Internal crystal oscillator support 26M crystal;
- Internal LDO regulator:1.35V to 1.2V;4.2V to 3.3V
- Built-in buck converter,DC-DC:4.2V to 1.35V
- Build-in 4Mbit SPI Flash

Copyright © 2016, www.appotech.com. All Rights Reserved.

2 Pin Definitions

2.1 CW6676B

2.1.1 Package

QFN32

2.1.2 Pin Assignment

Figure 2-1 shows the pin assignments of QFN32 package.

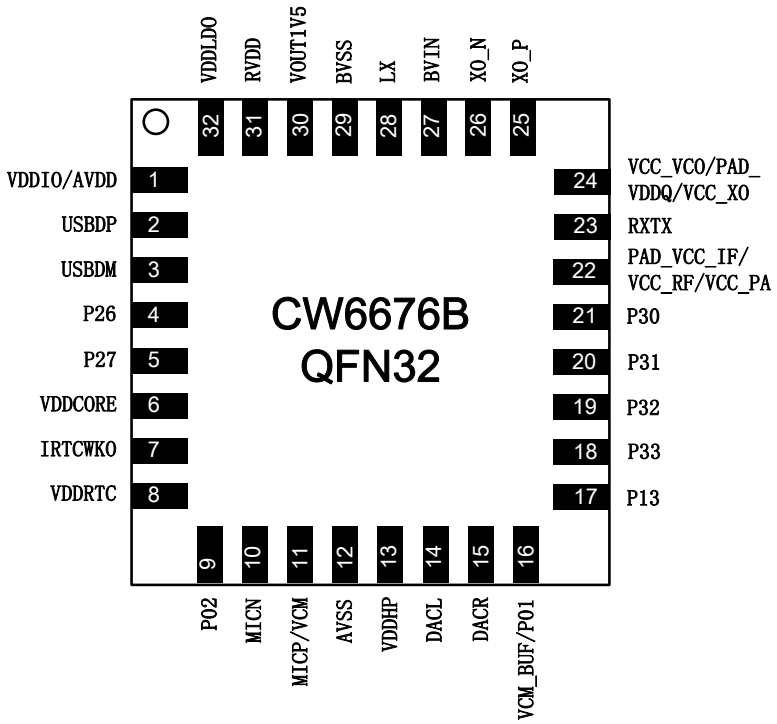


Figure 2-1 Pin Assignment of CW6676B

2.1.3 Pin Description

Table 2-1 shows the pin description of CW6676B.

Table 2-1 Pin Description of CW6676B

Pin No.QFN32	Name	Type	Function
1	VDDIO/AVDD	PWR	Power output VDDIO 3.3V
2	USBDP	I/O	USB Positive Input/output
3	USBDM	I/O	USB Negative Input/output
4	P26	I/O	GPIO

Copyright © 2016, www.appotech.com. All Rights Reserved.

Pin No.QFN32	Name	Type	Function
			BT UART1RX TMR2CKI IISWS0
5	P27	I/O	GPIO SDDAT0 EMIDAT7 SPI0DOUT0
6	VDDCORE	PWR	Core power VDD 1.2V
7	IRTCWKO	I/O	RTC wakeup
8	VDDRTC	PWR	RTC power input
9	P02	I/O	GPIO AUXL1 SPI0DOUT1 TMR1PWM
10	MICN	A	MIC Negative input
11	MICP/VCM	A	MIC Positive input DAC VCM output
12	AVSS	GND	Analog GND
13	VDDHP	PWR	Headphone power
14	DACL	A	DAC left output GPIO input
15	DACR	A	DAC right output GPIO input
16	P01/VCM_BUF	I/O	GPIO AUXR0 UARTTX1 PORTINT/WKUP0 DAC VCM buffer
17	P13	I/O	GPIO ADC5 IISBCLK0
18	P33	I/O	GPIO ADC0/LVD dect ir_input 32K/xosc12m sys_clk_output TRM1CAP
19	P32	I/O	GPIO SDDAT0 SPI0DOUT3/DIN3
20	P31	I/O	GPIO SDCMD

Copyright © 2016, www.appotech.com. All Rights Reserved.

Pin No.QFN32	Name	Type	Function
			SPI0DIN3
21	P30	I/O	GPIO ADC4 SDCLK SPI0CLK3
22	PAD_VCC_IF/VCC_RF/VCC_PA	PWR	Power VCC RF/PA Power VCC
23	RXTX	A	RF Rx and Tx pin
24	VCC_VCO/VCC_XO/PAD_VDDQ	PWR	Power VCC/ VDDQ
25	XO_P	A	BT 26MHz XOSC Positive Pin
26	XO_N	A	BT 26MHz XOSC Negative Pin
27	BVIN	PWR	PMU Power input Pin 4.2V(typ)
28	LX	A	Switch Node Connection to Inductor
29	BVSS	GND	GND
30	VOUT1V5	PWR	VOUT 1.5V
31	RVDD	PWR	RF power VDD
32	VDDLDO	PWR	LDO power input 4.2V(typ)

Copyright © 2016, www.appotech.com. All Rights Reserved.

3 Characteristics

3.1 PMU Parameters

Table 3-1 PMU Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
BVIN	Buck input voltage	2.8	4.2	4.6	V	
VDDLDO	VDDLDO input voltage	2.8	4.2	4.6	V	
VOUT1V5	Buck output voltage	1.15	1.35	1.6	V	
VDDCORE	1.2V output voltage	-	1.2	-	V	
VDDRTC	input voltage	2.2	4.2	4.6	V	
VDDHP	3.0V output voltage	2.8	3.0	3.3	V	
VCM	1.5V output voltage	-	1.35	-	V	
RVDD	output voltage	1.1	1.2	1.3	V	
VDDIO	3.3V output voltage	2.8	3.3	-	V	

3.2 CORE PLL Parameters

Table 3-2 PLL Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
F_{I1}	Frequency input	-	32.768	-	KHz	Low frequency OSC
F_{I2}	Frequency input	1	12	15	MHz	High frequency OSC
F_{OUT1}	Frequency output	-	48	-	MHz	
T_{LOCK1}	PLL locked time	-	2	-	ms	Use low frequency OSC as input reference
T_{LOCK2}	PLL locked time	-	0.1	-	ms	Use high frequency OSC as input reference

3.3 General purpose I/O Parameters

Table 3-3 I/O Parameters

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Low-Level input voltage	-	-	30% * VDDIO	V	VDDIO = 3.3V
V_{IH}	High-level input voltage	70% * VDDIO	-	-	V	VDDIO = 3.3V
R_{PUP0}	Internal pull-up resister 0	-	10	-	KΩ	
R_{PUP1}	Internal pull-up resister 1	-	200	-	KΩ	
R_{PUP2}	Internal pull-up resister 2	-	0.5	-	KΩ	
R_{PDN0}	Internal pull-down resister 0	-	10	-	KΩ	
R_{PDN1}	Internal pull-down resister 1	-	0.33	-	KΩ	
R_{PDN2}	Internal pull-down resister 2	-	0.5	-	KΩ	
I_{LEVEL1}	Level1 current driving	8	-	-	mA	For PORT1

Copyright © 2016, www.appotech.com. All Rights Reserved.

Symbol	Description	Min	Typ	Max	Units	Conditions
I_{LEVEL2}	Level2 current driving	24	-	-	mA	For Port1.1

3.4 **Audio ADDA Parameters**

Table 3-4 Audio DAC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
DAC SNR&DR		-	90	-	dB	48PIN
DAC SNR&DR		-	90	-	dB	28PIN & 20 PIN
DAC THD+N		-	-80	-	dB	10Kohm loading
PWR_{AB}	ClassAB AMP power output	-	-	16	mW	32ohm loading
V_{PP}	Maximum output voltage	-	-	2.6	V	10Kohm loading
ADC SNR/DR			93		dB	In Voice Band
ADC THD+N			89		dB	In Voice Band

3.5 **RF Analog Blocks**

Table 3-5 Frequency Synthesizer Parameters

Parameter	Condition		MIN	typ	max	Unit
Synthesizer						
Synthesizer settling time	Within +/- 25 KHz accuracy		-	70	-	us
Phase Noise	Fc=2.4GHz	ΔF=1 MHz	-	-110	-	dBc/Hz
		ΔF=2 MHz	-	-118	-	dBc/Hz
		ΔF≥3 MHz	-	-123	-	dBc/Hz
XTAL Oscillator						
Frequency range			-	26	-	MHz
Frequency Trimming Range	6 bits		-1	-	+1	kHz

Table 3-6 Receive path Parameters

Parameter	Condition		MIN	typ	max	Unit
Receiver Channel						
Minimum Usable Signal	RX sensitivity		-	-80	-	dBm
LNA						
Gain		High Gain	-	25	-	dB
		Mid Gain	-	15	-	dB
		Low Gain	-	5	-	dB
Mixer						
Conversion Gain			-	0	-	dB
IFamp						
Gain	5/9/12/15/18 dB		-	12	-	

Copyright © 2016, www.appotech.com. All Rights Reserved.

Parameter	Condition	MIN	typ	max	Unit
Complex BPF					
Band pass -3 dB BW	Figure 1.	-	2	-	MHz
Image Rejection		-	30	-	dB
VGA					
Gain Range		-6	-	+68	dB
Gain Step		-	+1/+6	-	dB
ADMOD					
SNDR	Freq = +- BW	-	>50	-	dB

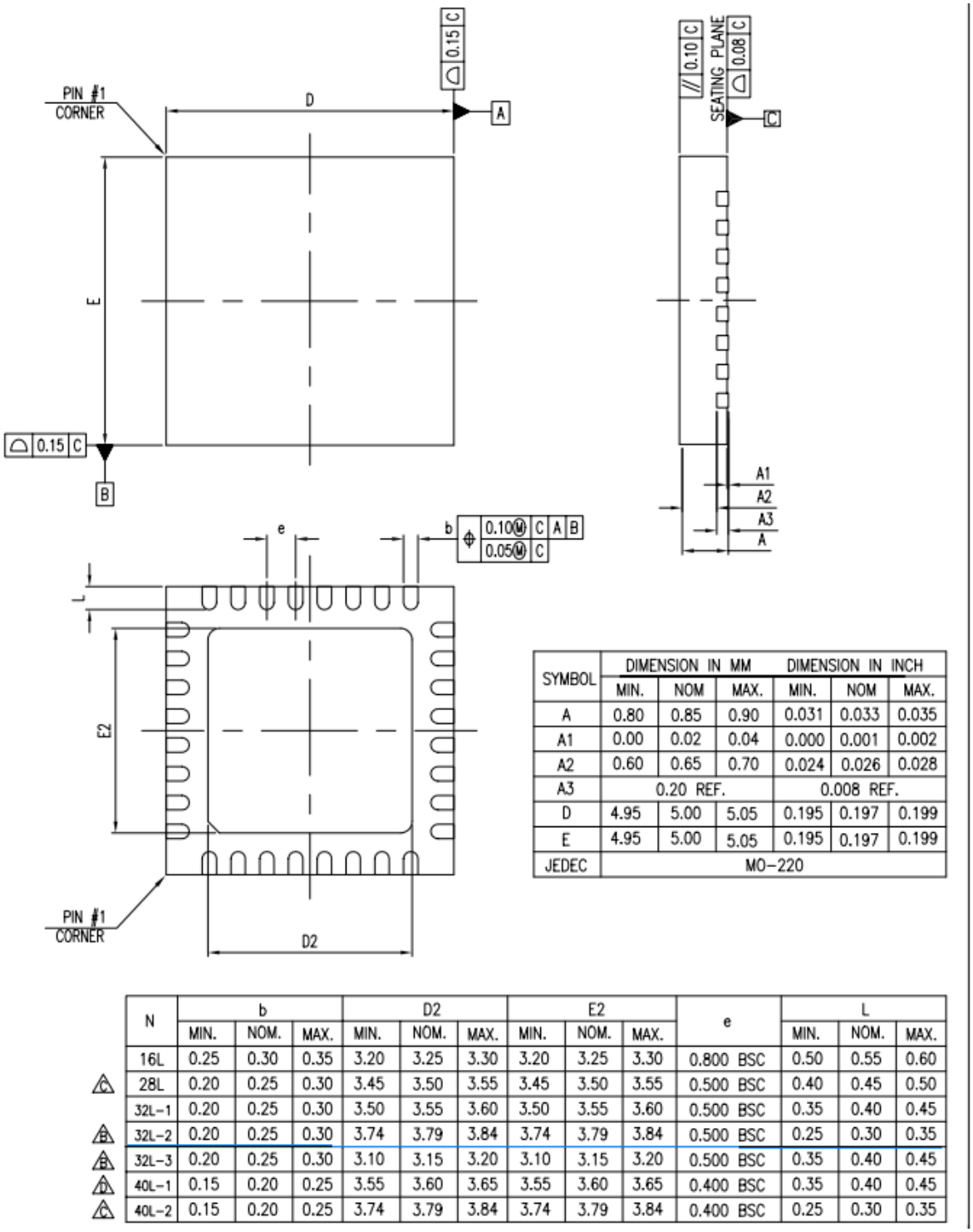
Table 3-7 Transmit path Parameters

Parameter	Condition		MIN	typ	max	Unit
Transmit Channel						
Available output power			-2	0	1.5	dBm
Side Band Suppression			-	-30	-	dBm
LPF						
Low pass -3 dB BW	Figure 2.		-	1	-	MHz
TXVGA						
Gain Step			-7	-	7	dB
PA						
Gain Range	Set paPWR[2:0] of Control Register #16	GFSK	-12	-	4	dBm
		DPSK	-15	-	1	dBm

Copyright © 2016, www.appotech.com. All Rights Reserved.

4 Package Outline Dimensions

4.1 QFN32



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.04	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF.			0.008 REF.		
D	4.95	5.00	5.05	0.195	0.197	0.199
E	4.95	5.00	5.05	0.195	0.197	0.199
JEDEC	MO-220					

	N	b			D2			E2			e	L		
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
	16L	0.25	0.30	0.35	3.20	3.25	3.30	3.20	3.25	3.30	0.800 BSC	0.50	0.55	0.60
6	28L	0.20	0.25	0.30	3.45	3.50	3.55	3.45	3.50	3.55	0.500 BSC	0.40	0.45	0.50
	32L-1	0.20	0.25	0.30	3.50	3.55	3.60	3.50	3.55	3.60	0.500 BSC	0.35	0.40	0.45
8	32L-2	0.20	0.25	0.30	3.74	3.79	3.84	3.74	3.79	3.84	0.500 BSC	0.25	0.30	0.35
8	32L-3	0.20	0.25	0.30	3.10	3.15	3.20	3.10	3.15	3.20	0.500 BSC	0.35	0.40	0.45
1	40L-1	0.15	0.20	0.25	3.55	3.60	3.65	3.55	3.60	3.65	0.400 BSC	0.35	0.40	0.45
6	40L-2	0.15	0.20	0.25	3.74	3.79	3.84	3.74	3.79	3.84	0.400 BSC	0.25	0.30	0.35

Copyright © 2016, www.appotech.com. All Rights Reserved.

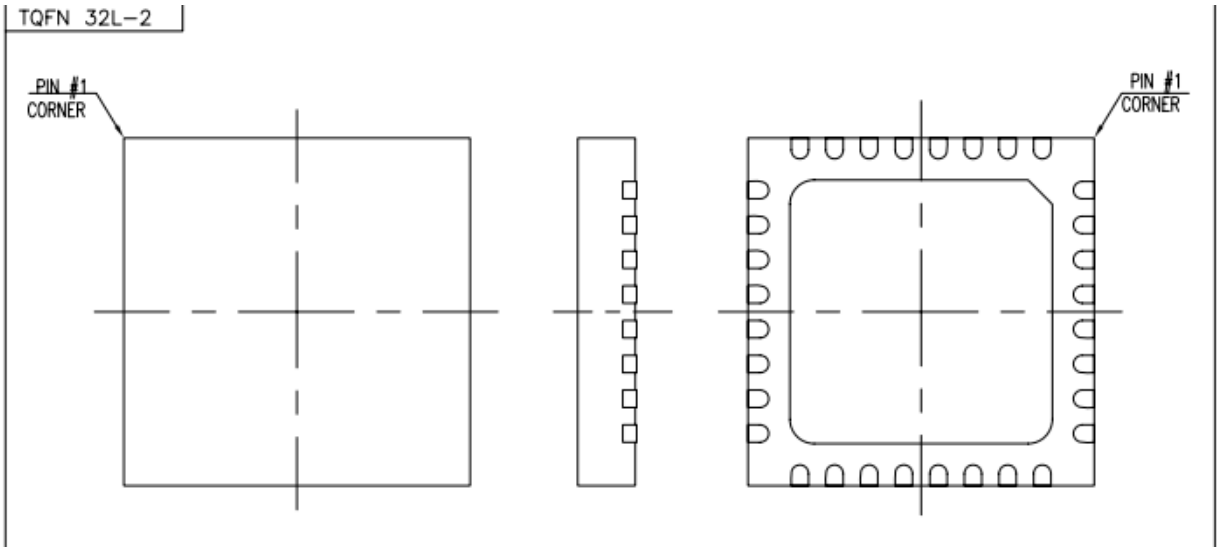


Figure 4-1 QFN32 Package Outline Dimension

Copyright © 2016, www.appotech.com. All Rights Reserved.

Revision History

Date	Version	Comments	Revised by
2016/7/19	0.0.1	Initial version	YX
2016/7/22	0.0.2	Checked	GAO
2016/7/26	1.0.0	Released	YX
2016/9/23	1.0.1	Modify work voltage	YX
2016/9/23	1.1.0	Release	YX

Copyright © 2016, www.appotech.com. All Rights Reserved.