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# **CW6680E/CW6681E/ CW6682E**

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## **Bluetooth Audio Player Microcontroller User Manual**

[CW6680E/CW6681E/CW6682E-UM-110-EN]

Versions: 1.1.0

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# 1 Product Overview

## 1.1 Outline

CW6680E/CW6681E/CW6682E is an MCS-51<sup>TM</sup> Compatible high performance mixed signal microcontroller. It integrates advanced digital and analog peripherals to suit for Bluetooth Audio Player applications.

## 1.2 Features

- Compatible with MCS-51<sup>TM</sup> instruction set;
- Maximum 48MHz operating frequency;
- Supports MP3 decoder;
- Supports WMA decoder;
- Supports WAV decoder;
- Supports MP3 encoder;
- Keypad tone mixer;
- Two multi-function 8-bit timers, support Capture and PWM mode;
- Two multi-function 16-bit timers, support Capture and PWM mode;
- Watchdog Timer with on-chip RC oscillator;
- one full-duplex UART;
- Two SPI;
- CW6680E support Full-speed USB 2.0 Device controller;
- CW6681E support Full-speed USB 2.0 Device/Host controller;
- Independent powered RTCC;
- 48MHz PLL-based clock generator;
- Six Channels 10-bit SARADC;
- Power on Reset;
- Support Bluetooth phone.

## 2 Pin Definitions

### 2.1 CW6680E/CW6681E

#### 2.1.1 Package

LQFP48

#### 2.1.2 Pin Assignment

Figure 2-1 shows the pin assignments of LQFP48 package

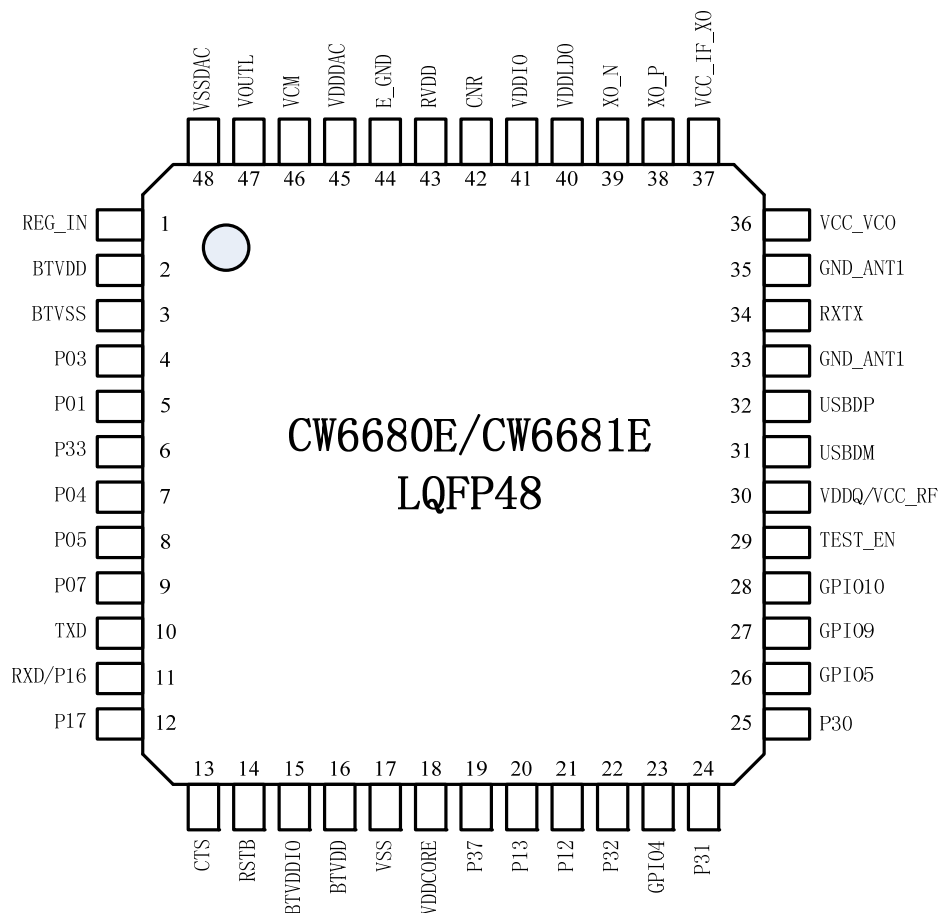


Figure 2-1 Pin Assignment for LQFP48

#### 2.1.3 Pin Description

Table 2-1 shows the pin descriptions of LQFP48 package.

Table 2-1 LQFP48 pin description



Pin No.	Name	Type	Function
1	REG_IN	I	This pin serves as an input of the on-chip VDD and RVDD LDO regulators
2	BTVDD	PWR	Bluetooth VDD
3	BTVSS	GND	Bluetooth ground
4	P03	AI	MICIN1 VCMBUF AUXL2
5	P01	I/O	AUXR0 SDDAT2 UART0TX1 GPIO
6	P33	I/O	ADC0 PWRWKUP LVDDDET CLKO GPIO
7	P04	I/O	ADC2 INT0 SPI1DO1 SPI1DODI1 PWM1 SPI0DODI1 SPI0DO1 GPIO
8	P05	I/O	ADC3 INT1 SPI1CLK1 CAP0 SPI0CLK1 GPIO
9	P07	I/O	INT3 CAP1 GPIO
10	TXD	O	UART Serial data output port for the HCI UART interface. This pin should be left unconnected if UART is not used or can be configured to GPIO
11	RXD	I	UART Serial data input port for the HCI UART interface. This pin should be left unconnected if UART is not used or can be configured to GPIO
	P16	I/O	ADC6

Pin No.	Name	Type	Function
			TMR2 PWM2 IISREFCLK AMIN CAP2 UART0TX0 GPIO
12	P17	I/O	TMR2 IISWS GPIO
13	CTS	I	UART Clear to Send-active low for HCI UART interface when the hardware flow control feature enable. This pin is used to set the system clock rate if the flow control feature is disabled
14	RSTB	I	Active low system reset. This pin contains a weak pull-up
15	BTVDDIO	I	Power supply for GPIOs
16	BTVDD	PWR	Bluetooth VDD
17	VSS	GND	Ground
18	VDDCORE	PWR	Digital 1.2V Power
19	P37	I/O	AUXL1 GPIO
20	P13	I/O	ADC5 GPIO
21	P12	I/O	GPIO
22	P32	I/O	SPI1DO0 SPI1DODI0 SDDAT01 GPIO
23	GPIO4	I/O	3.3V tolerant GPIO pin with programmable pull-up
24	P31	I/O	SPI1DI0 SDCMD1 GPIO
25	P30	I/O	ADC4 SPI1CLK0 SDCLK1 GPIO
26	GPIO5	I/O	3.3V tolerant GPIO pin with programmable pull-up
27	GPIO9	I/O	3.3V tolerant GPIO pin with

Pin No.	Name	Type	Function
			programmable pull-up
28	GPIO10	I/O	3.3V tolerant GPIO pin with programmable pull-up
29	TEST_EN	I	The test mode enable pin. This pin should be left unconnected for field application.
30	VDDQ	I	Digital block of RF circuit power supply. This pin must connect to RVDD
	VCC_RF	I	RF circuit power supply. This pin must connect to RVDD
31	USBDM	I/O	USB Negative Input/output
32	USBDP	I/O	USB Positive Input/output
33	GND_ANT1	-	Ground connection of RF I/O antenna. These pins must connect to RVSS
34	RXTX	-	RF I/O antenna pin
35	GND_ANT1	-	Ground connection of RF I/O antenna. These pins must connect to RVSS
36	VCC_VCO	I	VCO circuit power supply. This pin must connect to RVDD
37	VCC_IF_XO	I	IF and internal Crystal Oscillator circuit power supply. This pin must connect to RVDD
38	XO_P	I	Crystal or frequency reference input
39	XO_N	O	Crystal Oscillator output. Connect with XO_P if the reference clock is supplied
40	VDDLDO	PWP	LDO 5V Power
41	VDDIO	PWR	IO 3.3V Power
42	CNR	O	On-Chip RVDD LDO external decoupling capacitor pin
43	RVDD	-	On-chip 1.8V RVDD LDO output to supply internal RF circuits, this pin output typical voltage is 1.8V
44	E-GND	GND	Ground
45	VDDDAC	PWR	DAC 3.3V Power HeadPhone 3.3V Power
46	VCM	AO	DAC Bandgap voltage reference
47	DACL	AO	DAC Left Channel
48	VSSDAC	GND	DAC Ground

**I**: input; **O**: output; **PWR**: power; **GND**: ground; **AO**: Analog Output; **AI**: Analog Input; **NC**: not connect

## 2.2 CW6682E

### 2.2.1 Package

LQFP48

### 2.2.2 Pin Assignment

Figure 2-2 shows the pin assignments of LQFP48 package

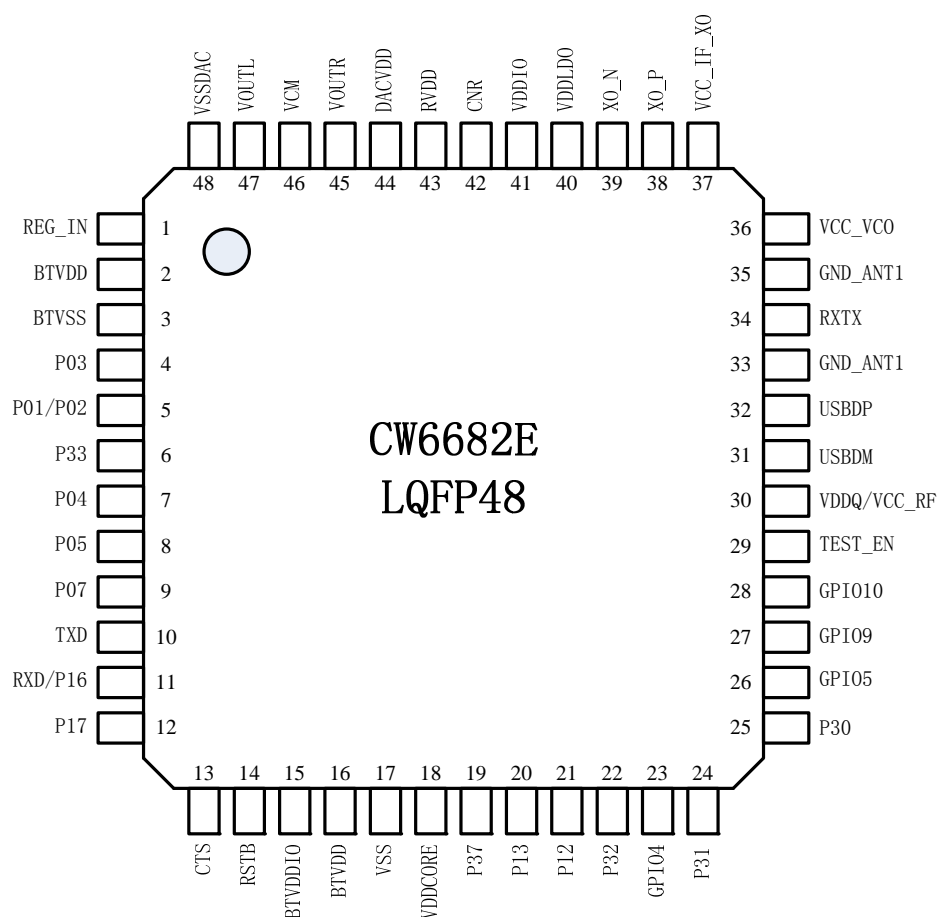


Figure 2-2 Pin Assignment for LQFP48

### 2.2.3 Pin Description

Table 2-2 shows the pin descriptions of LQFP48 package.

Table 2-2 LQFP48 pin description

Pin No.	Name	Type	Function
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Pin No.	Name	Type	Function
3	BTVSS	GND	Bluetooth ground
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5	P01	I/O	AUXR0 SDDAT2 UART0TX1 GPIO
	P02	I/O	AUXR2 MICIN0 GPIO
6	P33	I/O	ADC0 PWRWKUP LVDDDET CLKO GPIO
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20	P13	I/O	ADC5 GPIO
21	P12	I/O	GPIO
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23	GPIO4	I/O	3.3V tolerant GPIO pin with programmable pull-up
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	VCC_RF	I	RF circuit power supply. This pin must connect to RVDD
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32	USBDP	I/O	USB Positive Input/output
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34	RXTX	-	RF I/O antenna pin
35	GND_ANT1	-	Ground connection of RF I/O antenna. These pins must connect to RVSS
36	VCC_VCO	I	VCO circuit power supply. This pin must connect to RVDD
37	VCC_IF_XO	I	IF and internal Crystal Oscillator circuit power supply. This pin must connect to RVDD
38	XO_P	I	Crystal or frequency reference input
39	XO_N	O	Crystal Oscillator output. Connect with XO_P if the reference clock is supplied
40	VDDLDO	PWP	LDO 5V Power
41	VDDIO	PWR	IO 3.3V Power
42	CNR	O	On-Chip RVDD LDO external decoupling capacitor pin
43	RVDD	-	On-chip 1.8V RVDD LDO output to supply internal RF circuits, this pin output typical voltage is 1.8V
44	DACVDD	PWR	DAC 3.3V Power HeadPhone 3.3V Power
45	VOUTR	AO	DAC Right Channel
46	VCM	AO	DAC Bandgap voltage reference
47	VOUTL	AO	DAC Left Channel
48	VSSDAC	GND	DAC Ground

I: input; O: output; PWR: power; GND: ground; AO: Analog Output; AI: Analog Input; NC: not connect

## 3 CPU Core Information

### 3.1 Architecture

The AXC51-CORE of CW6680E/CW6681E/CW6682E is fully compatible with the MCS-51™ instruction set.

The AXC51-CORE employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12MHz. By contrast, the AXC51-CORE executes most of its instructions in 1 system clock cycle. With system clock running at 48 MHz, it has a peak throughput of 48 MIPS running in on-chip SRAM area.

### 3.2 Instruction Set

The instruction set of the AXC51-CORE is fully compatible with the standard MCS-51™ instruction set; standard 8051 development tools can be used to develop software for the AXC51-CORE. All instructions of AXC51-CORE are the binary and functional equivalent of their MCS-51™ counterparts, including op-codes, addressing modes and effect on PSW flags. However, instruction timing is different than that of the standard 8051. [Table 3-1](#) shows AXC51-CORE Instruction Set Summary

Table 3-1 AXC51-CORE Instruction Set Summary

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in SRAM)
1	NOP		1
2	AJMP	code addr	3
3	LJMP	code addr	3
1	RR	A	1
1	INC	A	1
1	INC	data addr	1
1	INC	@Ri	1
1	INC	Rn	1
3	JBC	bit addr, code addr	1 or 3
2	ACALL	code addr	3
3	LCALL	code addr	3
1	RRC	A	1
1	DEC	A	1
2	DEC	data addr	1
1	DEC	@Ri	1
1	DEC	Rn	1
3	JB	bit addr, code addr	1 or 3
1	RET		4
1	RL	A	1
2	ADD	A, #data	1



Number of Bytes	Mnemonic	Operands	Clock Cycles (running in SRAM)
2	ADD	A, data addr	1
1	ADD	A, @Ri	1
1	ADD	A, Rn	1
3	JNB	bit addr, code addr	1 or 3
1	RETI		4
1	RLC	A	1
2	ADDC	A, #data	1
2	ADDC	A, data addr	1
1	ADDC	A, @Ri	1
1	ADDC	A, Rn	1
2	JC	code addr	1 or 3
2	ORL	data addr, A	1
3	ORL	data addr, #data	1
2	ORL	A, #data	1
2	ORL	A, data addr	1
1	ORL	A, @Ri	1
1	ORL	A, Rn	1
2	JNC	code addr	1 or 3
2	ANL	data addr, A	1
2	ANL	data addr, #data	1
1	ANL	A, @Ri	1
1	ANL	A, Rn	1
2	JZ	code addr	1 or 3
2	XRL	data addr, A	1
3	XRL	data addr, #data	1
2	XRL	A, #data	1
2	XRL	A, data addr	1
1	XRL	A, @Ri	1
1	XRL	A, Rn	1
2	JNZ	code addr	1 or 3
2	ORL	C, bit addr	1
1	JMP	@A+DPTR	3
2	MOV	A, #data	1
3	MOV	data addr, #data	1
2	MOV	@Ri, #data	1
2	MOV	Rn, #data	1
2	SJMP	code addr	3
2	ANL	C, bit addr	1
1	MOVC*	A, @A+PC	1
1	DIV	AB	1
3	MOV	data addr, data addr	1

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in SRAM)
2	MOV	data addr, @Ri	1
2	MOV	data addr, Rn	1
3	MOV	DPTR, #data	1
2	MOV	bit addr, C	1
1	MOVC*	A, @A+DPTR	2
2	SUBB	A, #data	1
2	SUBB	A, data addr	1
1	SUBB	A, @Ri	1
1	SUBB	A, Rn	1
2	ORL	C, bit addr	1
2	MOV	C, bit addr	1
1	INC	DPTR	1
1	MUL	AB	1
2	MOV	@Ri, data addr	1
2	MOV	Rn, data addr	1
2	ANL	C, bit addr	1
2	CPL	bit addr	1
2	CPL	C	1
3	CJNE	A, #data, code addr	1 or 3
3	CJNE	A, data addr, code addr	1 or 3
3	CJNE	@Ri, #data, code addr	1 or 3
3	CJNE	Rn, #data, code addr	1 or 3
2	PUSH	data addr	1
2	CLR	bit addr	1
1	CLR	C	1
1	SWAP	A	1
2	XCH	A, data addr	1
1	XCH	A, @Ri	1
1	XCH	A, Rn	1
2	POP	data addr	1
2	SETB	bit addr	1
1	SETB	C	1
1	DA	A	1
3	DJNZ	data addr, code addr	1 or 3
1	XCHD	A, @Ri	1
2	DJNZ	Rn, code addr	1 or 3
1	MOVB	A, @DPTR	2
1	MOVB	A, @Ri	2
1	CLR	A	1
2	MOV	A, data addr	1
1	MOV	A, @Ri	1

Number of Bytes	Mnemonic	Operands	Clock Cycles (running in SRAM)
1	MOV	A, Rn	1
1	MOVX	@DPTR, A	1
1	MOVX	@Ri, A	1
1	CPL	A	1
2	MOV	data addr, A	1
1	MOV	@Ri, A	1
1	MOV	Rn, A	1

## 3.3 Memory Mapping

### 3.3.1 Program Memory Mapping

As illustrated in [Figure 3-1](#), CW6680E/CW6681E/CW6682E program include 16KB IRAM at the address form 0x0000 to 0x3FFF.

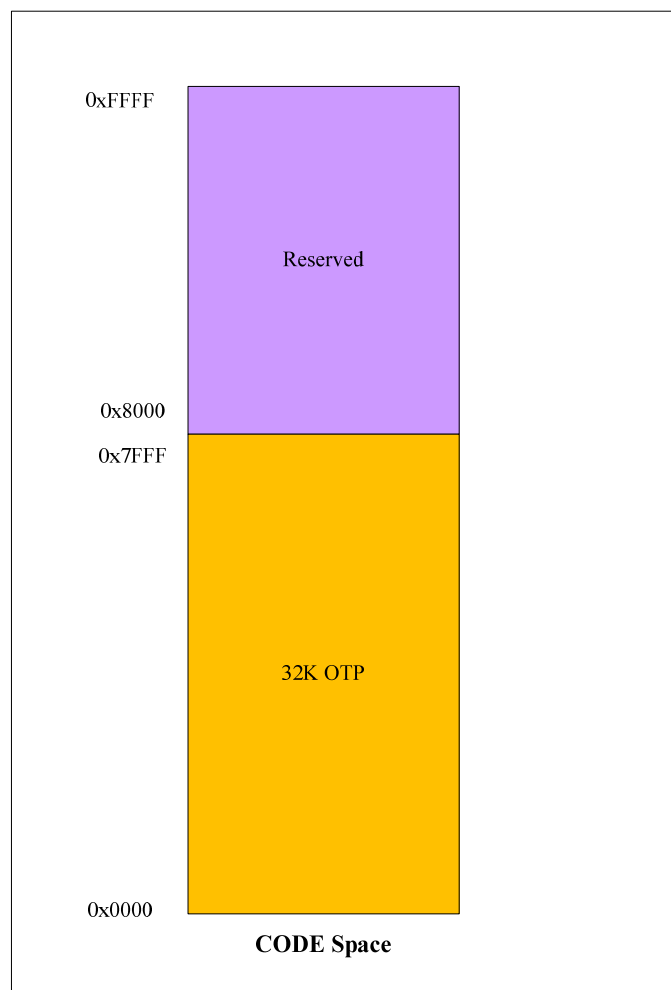


Figure 3-1 Program Memory Organization

### 3.3.2 External Data Memory Mapping

*Figure 3-2* Illustrated External Data Memory Mapping.

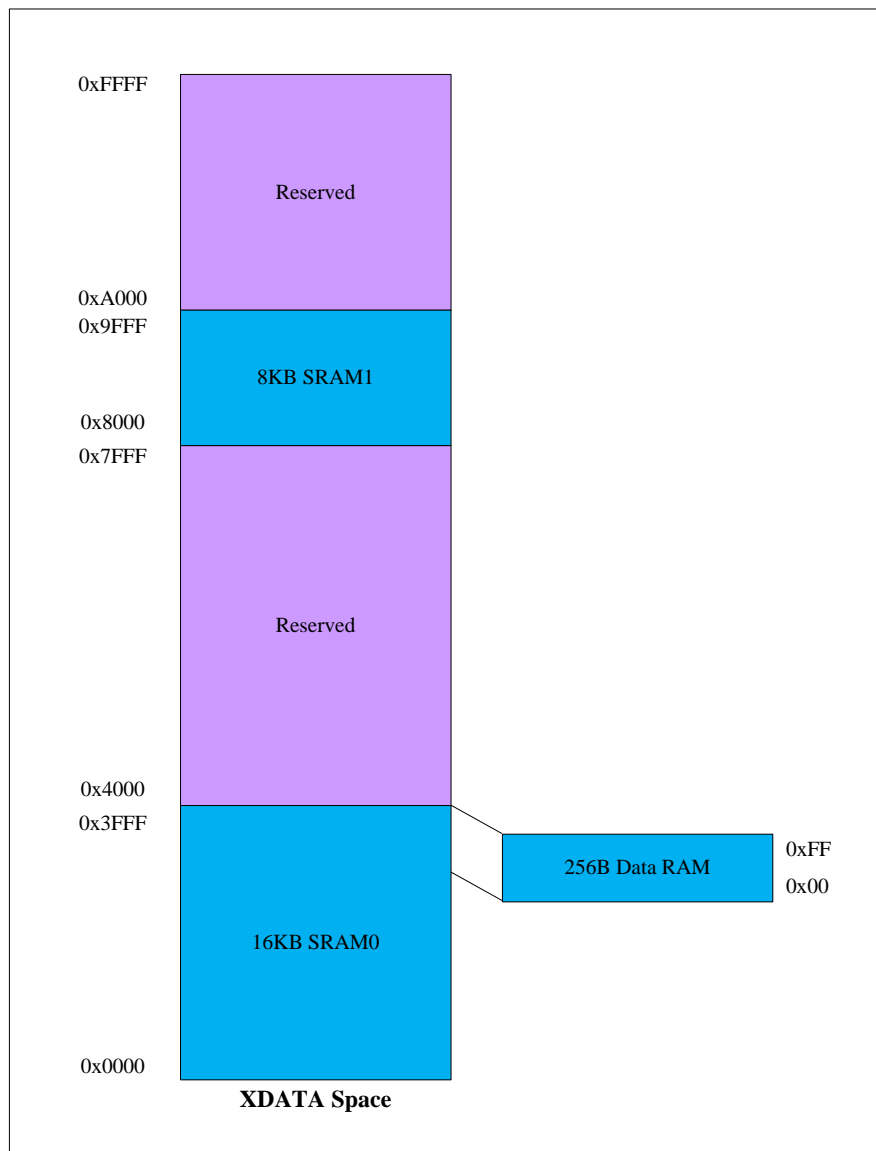


Figure 3-2 External Data Memory Mapping

### 3.3.3 Internal Data Memory Mapping

Internal data memory locates in SRAM1 at the address from 0x3F00 to 0x3FFF as showed in *Figure 3-2*. Internal data memory is mapped in *Figure 3-3*. The memory space is shown divided into three blocks, which are generally referred to as the Lower 128, the Upper 128, and SFR space.

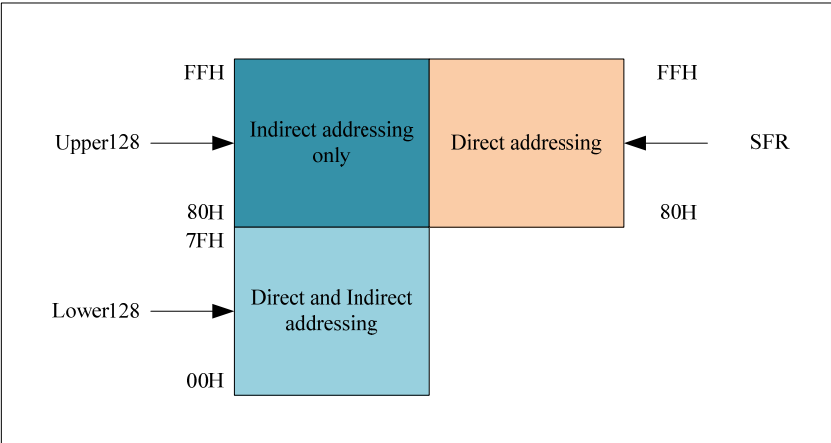


Figure 3-3 Internal data memory mapping

As shown in [Figure 3-4](#) the Lowest 32 bytes in Lower 128 are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the PSW select which register bank are in use.

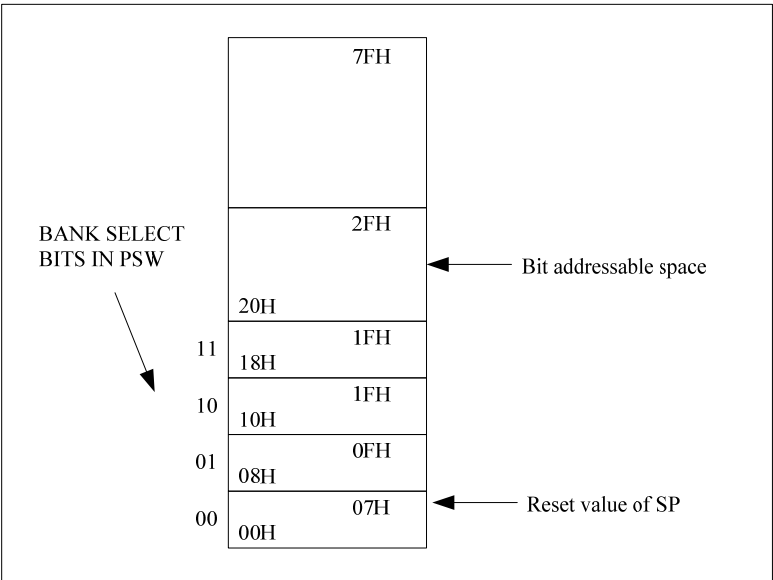


Figure 3-4 Lowest 32 bytes in Internal data memory Lower 128

### 3.4 Interrupt Processing

#### 3.4.1 Interrupt sources

The CW6680E/CW6681E/CW6682E provides 15 interrupt sources. All interrupts are controlled by a series combination of individual enable bits and a global enable (EA) in the interrupt-enable register (IE0.7). Setting EA to logic 1 allows individual interrupts to be enabled. Setting EA to logic 0 disables all interrupts regardless of the individual interrupt-enable settings. The interrupt enables and priorities are functionally identical to those of the 80C52.

The CW6680E/CW6681E/CW6682E provides 1 set of vectors entry addresses, starting from 0x0003. The vector base address is set by DPCON [7:6]. [Table 3-2](#) lists the interrupt summary.

Table 3-2 Interrupt Summary

Interrupt Sources	Interrupt Vector	Interrupt Number	Natural Order	Interrupt Flag	Interrupt Enable Bit	Priority Control Bit
SINT0	0x0003	0	1	SPMODE.7	IE0.0	IPH0.0 IP0.0
SINT1	0x000B	1	2	SPMODE.6	IE0.1	IPH0.1 IP0.1
Timer 1	0x0013	2	3	TMR1CON.7 TMR1CON.6	IE0.2	IPH0.2 IP0.2
Timer 2	0x001B	3	4	TMR2CON.7 TMR2CON.6	IE0.3	IPH0.3 IP0.3
MP3	0x0023	4	5	AUCON7.6 AUCON7.5 AUCON7.4 AUCON7.3 AUCON7.2 AUCON7.1 AUCON7.0	IE0.4	IPH0.4 IP0.4
USBSOF	0x0033	6	7	USBCON2.1	IE0.6	IPH0.6 IP0.6
USBCTL	0x003B	7	8		IE1.0	IPH1.0 IP1.0
SDC	0x0043	8	9	SDCON1.5 SDCON1.4	IE1.1	IPH1.1 IP1.1
PORT	0x004B	9	10	WKPND	IE1.2	IPH1.2 IP1.2
SPI0	0x0053	10	11	SPI0CON.7	IE1.3	IPH1.3 IP1.3
Timer 3	0x005B	11	12	TMR3CON.7	IE1.4	IPH1.4 IP1.4
Timer 0	0x0063	12	13	TMR0CON.7	IE1.5	IPH1.5 IP1.5
RTCC UART0 UART1 WDT LVD IIS	0x006B	13	14	RTCON.7 UARTSTA.5&UARTSTA.4 UART1STA.3&UART1STA2 IP0.7 LVDCON.7 IIS_CON1.7	IE1.6	IPH1.6 IP1.6
SPI1	0x0073	14	15	SPI1CON.7	IE1.7	IPH1.7 IP1.7

### 3.4.2 Interrupt Priority

There are 4 levels of interrupt priority: Level 3 to 0. All interrupts have individual priority bits in the interrupt priority registers to allow each interrupt to be assigned a priority level from 3 to 0. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in [Table 3-2](#).

The processor indicates that an interrupt condition occurred by setting the respective flag bit. This bit is set regardless of whether the interrupt is enabled or disabled.

## 3.5 CPU and Memory related SFR Description

Register 3-1 DPCON – Data Pointer Configure Register

Position	7	6	5	4	3	2	1	0
Name	IA		DPID0	DPID1	DPAID	DPTSL	EINSTEN	DPSEL
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IA:** Select Interrupt Vector's Base Address

00 = Base address is 0x0003

01 = Reserved

10 = Reserved

11 = Reserved

**DPID0:** DPTR0 increase direction control

0 = DPTR increase

1 = DPTR decrease

**DPID1:** DPTR1 increase direction control

0 = DPTR increase

1 = DPTR decrease

**DPAID:** DPTR auto increment enables

0 = Auto increment disable

1 = Auto increment enable

**DPTSL:** DPSEL toggle enable

0 = DPSEL toggle disable

1 = DPSEL toggle enable

**EINSTEN:** Extern instruction enables

0 = Disable

1 = Enable

**DPSEL:** DPTR Select

0 = Active DPTR0

1 = Active DPTR1

Data Pointer Register is an 16-bit address pointer, it can split up into two registers, DPL and DPH. Data pointer register always used as indirect addressing register.

Register 3-2 DPL0 – Data Pointer Low Byte

Position	7	6	5	4	3	2	1	0
Name	DPL0							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 3-3 DPL1 – Data Pointer Low Byte

Position	7	6	5	4	3	2	1	0
Name	DPL1							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 3-4 DPH0 – Data Pointer High Byte

Position	7	6	5	4	3	2	1	0
Name	DPH0							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 3-5 DPH1 – Data Pointer High Byte

Position	7	6	5	4	3	2	1	0
Name	DPH1							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The data pointers (DPTR0 and DPTR1) are used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM location. Two pointers are useful when moving data from one memory area to another. The user can select the active pointer through a dedicated SFR bit (DPSEL: DPCON.0), or can activate an automatic toggling feature for altering the pointer selection (DPTSL: DPCON.2). An additional feature, if selected, provides automatic incrementing or decrementing of the current DPTR.

Data pointer increment/decrement bits DPID0 (DPCON.5) and DPID1 (DPCON.4) define how the INC DPTR instruction functions in relation to the active DPTR.

The CW6680E/CW6681E/CW6682E offers a programmable option that allows any instructions related to data pointer to toggle the DPSEL bit automatically. This option is enabled by setting the toggle-select-enable bit (DPTSL) to logic 1.

Once enabled, the DPSEL bit is automatically toggled after the execution of one of the following 5 DPTR related instructions:

`MOV C A, @A+DPTR`

`MOVX A, @DPTR`

`MOVX @DPTR, A`



**INC DPTR****MOV DPTR, #data16**

The CW6680E/CW6681E/CW6682E also offers a programmable option that automatically increases (or decreases) the contents of the selected data pointer by 1 after the execution of a DPTR-related instruction. The actual function (increment or decrement) is dependent on the setting of the DPAID bits. This option is enabled by setting the automatic increment/decrement enable (DPAID: DPCON.3) to a logic 1 and is affected by one of the following 3 DPTR-related instructions.

DPTR-related instructions are:

**MOVC A, @A+DPTR****MOVX A, @DPTR****MOVX @DPTR, A**

Register 3-6 SP – Stack Pointer Low Byte

Position	7	6	5	4	3	2	1	0
Name	SP							
Default	0	0	0	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 3-7 SPH – Stack Pointer High Byte

Position	7	6	5	4	3	2	1	0
Name	SPH							
Default	0	0	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In a standard 8051, there is only an 8-bit stack pointer (SP). It can only use the internal 256 byte data memory as stack memory. To increase the stack space for more complex application, CW6680E/CW6681E/CW6682E supports a 16-bit extend stack pointer, it can use both internal data RAM and the 20K byte on-chip SRAM as stack memory. There are 2 registers for stack control.

Register 3-8 PSW – Processor Status Word

Position	7	6	5	4	3	2	1	0
Name	CY	AC	EC	RS1	RS0	OV	EZ	P
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**CY:** Carry Flag

**AC:** Auxiliary carry flag

**EC:** Extern instruction Carry flag

**RS1, RS0:** Register bank select

00 = bank0

01 = bank1

10 = bank2

11 = bank3

**OV:** Overflow flag

**EZ:** Extern instruction zero flag

**P:** Odd parity check of ACC

0 = There are even number of '1' bits in ACC

1 = There are odd number of '1' bits in ACC

Register 3-9 SPMODE – Special mode

Position	7	6	5	4	3	2	1	0
Name	SINT0	SINT1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**SINT0:** Software 0 interrupts pending

0 = No software 0 interrupt

1 = Software 0 interrupt

**SINT1:** Software 1 interrupts pending

0 = No software 1 interrupt

1 = Software 1 interrupt

Register 3-10 IE0 – Interrupt Enable 0

Position	7	6	5	4	3	2	1	0
Name	EA	IE06	IE05	IE04	IE03	IE02	IE01	IE00
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**EA:** Global interrupt enable

0 = Disable

1 = Enable

**IE06:** USB SOF interrupt enable

0 = Disable

1 = Enable

**IE05:** Huffman interrupt enable

0 = Disable

1 = Enable

**IE04:** MP3 decoder and encoder interrupt enable

0 = Disable

1 = Enable

**IE03:** Timer2 interrupt enable

0 = Disable

1 = Enable

**IE02:** Timer1 interrupt enable

0 = Disable

1 = Enable

**IE01:** SINT1 interrupt enable

0 = Disable

1 = Enable

**IE00:** SINT0 interrupt enable

0 = Disable

1 = Enable

Register 3-11 IE1 – Interrupt Enable 1

Position	7	6	5	4	3	2	1	0
Name	IE17	IE16	IE15	IE14	IE13	IE12	IE11	IE10
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IE17:** SPI1 interrupt enable

0 = Disable

1 = Enable

**IE16:** RTCC/UART0/UART1/LVD/WDT/IIS interrupt enable

0 = Disable

1 = Enable

**IE15:** Timer0 interrupt enable

0 = Disable

1 = Enable

**IE14:** Timer 3 interrupt enable

0 = Disable

1 = Enable

**IE13:** SPI interrupt enable

0 = Disable

1 = Enable

**IE12:** Port interrupt enable

0 = Disable

1 = Enable

**IE11:** SDC interrupt enable

0 = Disable

1 = Enable

**IE10:** USB control interrupt enable

0 = Disable

1 = Enable

Register 3-12 IPH0 – Interrupt Priority high 0

Position	7	6	5	4	3	2	1	0
Name	IPH07	IPH06	IPH05	IPH04	IPH03	IPH02	IPH01	IPH00
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 3-13 IP0 – Interrupt Priority 0

Position	7	6	5	4	3	2	1	0
Name	IP07	IP06	IP05	IP04	IP03	IP02	IP01	IP00
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IPH07, IP07:** Watch Dog interrupt Priority select

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH06, IP06:** USB SOF interrupts priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH05, IP05:** Huffman interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH04, IP04:** MP3 decoder interrupts priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH03, IP03:** Timer2 interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH02, IP02:** Timer1 interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH01, IP01:** SINT1 interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH00, IP00:** SINT0 interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

## Register 3-14 IPH1 – Interrupt Priority high 1

Position	7	6	5	4	3	2	1	0
Name	IPH17	IPH16	IPH15	IPH14	IPH13	IPH12	IPH11	IPH10
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

## Register 3-15 IP1 – Interrupt Priority 1

Position	7	6	5	4	3	2	1	0
Name	IP17	IP16	IP15	IP14	IP13	IP12	IP11	IP10
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IPH17, IP17:** SPI1 interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH16, IP16:** RTCC/UART/LVD/WDT/IIS interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH15, IP15:** Timer0 interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH14, IP14:** Timer 3 interrupts priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH13, IP13:** SPI interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH12, IP12:** Port interrupts priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH11, IP11:** SDC interrupt priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

**IPH10, IP10:** USB control interrupts priority

11 = level 3 highest priority

10 = level 2

01 = level 1

00 = level 0 lowest priority

## 4 Reset Generation

### 4.1 Power-on Reset (POR)

CW6680E/CW6681E/CW6682E provides an on-chip Power-On-Reset (POR) circuit to detect power-on and to reset internal logic before VDD reaches the pre-determined POR threshold voltage. When VDD=1.2V, the POR threshold voltage is set to be about 0.47V~0.67V.

Sometimes, when the VDD is power-off and quickly power-on again, there might be cases that the POR will work improperly and internal reset might not be generated. For this reason, CW6680E/CW6681E/CW6682E POR circuit incorporates an internal self-reset module to discharge PORB output during power-off to ensure each power cycle will work properly.

However, it is also highly recommended user should have a long time between power-off and next power-on to ensure proper start-up. The time depends on actual system board environment and how much decoupling capacitors between power and ground. User has to take into account this effect during board level design.

*Figure 4-1* illustrates the power-on and reset signals waveform during proper power-on. Internally, there is TPOR and TRC time for both the POR circuit and the internal counter. TPOR is the time for the POR circuit to stay at zero voltage until it reaches VPOR and the time varies for different VDD rise-up time. It can be assumed to be about 2/3 of the VDD rise-up time. TRC is the time for internal counter to count 4ms using internal RC-oscillator when the counter sees a high logic from PORB signal. As a result, the overall internal reset time is the sum of TPOR and TRC. Such a long time is required to ensure the Power is stable for system use. It also ensures all internal logics are properly reset.

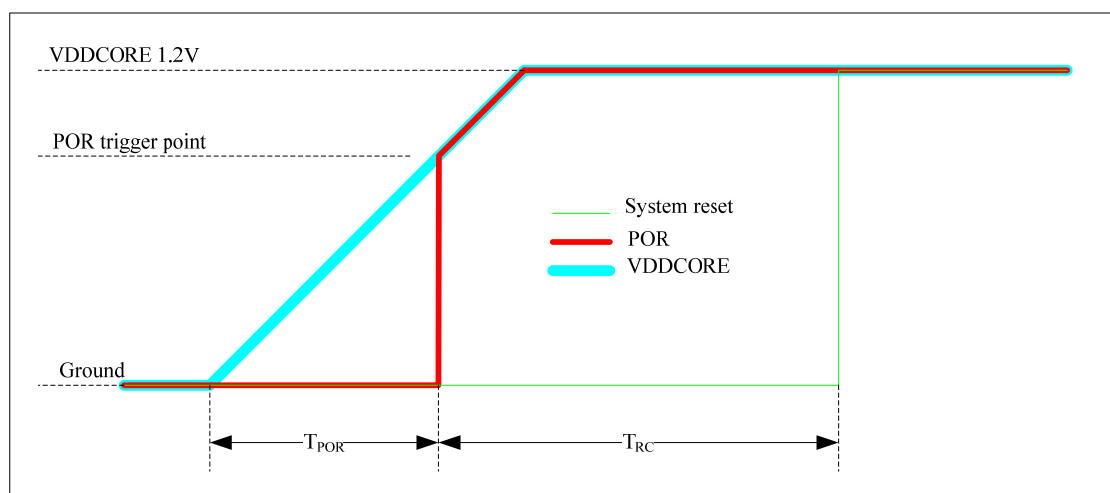


Figure 4-1 Power on reset

### 4.2 System Reset

All reset signals are OR'ed together inside the device to generate an overall system reset to reset the chip. Once reset, the program memory address is reset to 8000h, which is the start address of the Normal Mode. *Figure 4-2* illustrates the reset sources.

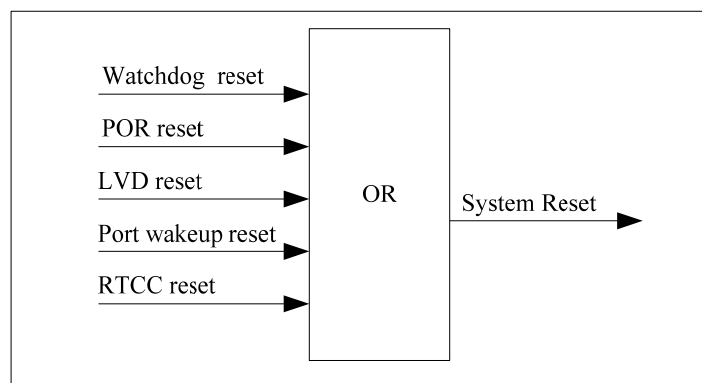


Figure 4-2 Reset Sources

### 4.2.1 LVD

CW6680E/CW6681E/CW6682E provides 4 levels programmable Low Voltage Detector (LVD) for user to detect VDDLDO power supply voltage or external pin voltage multiplexed with GPIO P3.3. It is for doing so since VDDLDO is the input voltage source for on-chip Low-Drop-Out regulator (LDO) and that supplies power to internal VDDCORE. User for such reason can momentarily monitor the VDDLDO power if externally connects to some batteries and detect if external power source starts dropping to a level that CW6680E/CW6681E/CW6682E LDO cannot tolerate and can do proper actions in the system program.

LVD can also be used to monitor external voltage source through the GPIO P3.3 to enhance programmability for different voltage levels. One of the examples can be used to monitor external power sources or batteries voltage or some voltages related to say pressure or temperature. It is there to provide a simple interface compared to ADC since ADC requires more programming space and procedures to detect precise voltage level. If user requires un-precise voltage detection without fine voltage range, LVD will be a good choice compared to ADC measurement. [Table 4-1](#) illustrates different voltage detection levels.

**Remark:**

- When LVD\_ENB is enabled, there is approximately 100us for the band-gap and the comparator to be stable before the end-user can use it as low voltage detection. During the time, LVD\_OEB has to be H in order to disable the LVD output with possibly fluctuating signal level.
- Different power supply falling time will affect the voltage detection. It is recommended that the power supply falling time should be larger than 1ms for stable low voltage detection.

Upon detection occurs, interrupt can be generated if LVD interrupt is enabled, or, CW6680E/CW6681E/CW6682E can undergo reset if interrupt is disabled.

Note that the detection is slightly dependent on power supply falling rate and noise fluctuation during power drop may alter the detection results. For this reason, internally the comparator has about 150mV hysteresis voltage level defined as  $V_{HYS} = V_{LVDR} - V_{LVDS}$  to filter out the noise may occur. Also, the detection level may have a maximum of 100mV difference compared to the value stated in [Table 4-1](#).

Table 4-1 LVD level setting

LVDS	LVDDDET Detection Level (V)	VDDLDO Detection Level (V)
00	1.8	2.2



LVDS	LVDDDET Detection Level (V)	VDDLDO Detection Level (V)
01	1.95	2.4
10	2.2	2.7
11	2.5	3.1

For the best operation, below shows a recommended operation for the LVD.

1. Select either VDDLDO or external pin to be monitored. Set VD1\_ENB = 0 for VDDLDO or VD2\_ENB = 0 for external pin
2. Select the detection voltage by setting bits BORS0, BORS1
3. Enable the LVD by setting LVD\_ENB = 0
4. Wait for at least 30us for the internal band-gap and comparator to become stable
5. Enable the LVD output by setting LVD\_OEB = 0
6. The EX\_PIN detect voltage must be less than VDDIO

Register 4-1 LVDCON– LVD control

Position	7	6	5	4	3	2	1	0
Name	LVDIF	LVDRSTEN	LV DEN	LVDOE	VD2EN	VD1EN	LVDS	
Default	0	1	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**LVDIF:** LVD interrupt pending bit.

0 = When LVD threshold not detect. Cleared by writing a 0 to it

1 = When LVD threshold is detected

**LVDRSTEN:** LVD Reset enable bit.

0 = LVD Reset is disabled

1 = LVD is enabled

**LV DEN:** LVD enable bit. Low active

0 = LVD is enabled

1 = LVD is disabled

**LVDOE:** LVD output enable bit. Low active

0 = LVD output is enabled

1 = LVD output is disabled

**VD2EN:** External pin (P33) voltage enable bit. Low active

0 = External pin voltage detection is enabled

1 = External pin voltage detection is disabled

**VD1EN:** VDDLDO voltage enable bit. Low active

0 = VDDLDO voltage detection is enabled

1 = VDDLDO voltage detection is disabled

**LVDS:** Voltage detection level select

00 = 2.2V/1.8V

01 = 2.4V/1.95V

10 = 2.7V/2.2V

11 = 3.1V/2.5V

## 4.2.2 RTCC Reset

CW6680E/CW6681E/CW6682E can be reset by RTCC second and alarm interrupt when ITRSTEN bit in RTCON is set to 1.

## 4.2.3 Watchdog Reset

If Watchdog timer is enabled, and WDTCON [5] is not written by 1 within watchdog overflow time period, CW6680E/CW6681E/CW6682E will be reset by Watchdog overflow.

## 4.2.4 Port Wakeup Reset

During SLEEP mode, port wakeup event will cause CW6680E/CW6681E/CW6682E reset.

# 4.3 Clock System

## 4.3.1 Clock Control

CW6680E/CW6681E/CW6682E embeds 32K/4M/12M/24M OSC internal oscillator circuits. External crystal is needed to generate a clock source. One internal PLL can generate 48MHz from the crystal clock source. One internal RC oscillator is also embedded.

To make sure the USB module operate properly, the USB clock must set to be 48MHz. In this case, system clock can be 48 MHz or 24MHz.

Register 4-2 PCON0 – Power control 0

Position	7	6	5	4	3	2	1	0
Name	DRAMCEN	IRAMCEN	IROMCEN	RAM2CEN	Reserved	IDLE	HOLD	SLEEP
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**DRAMCEN:** DECRAM clock enable

0 = Enable

1 = Disable

**IRAMCEN:** IRAM clock enable

0 = Enable

1 = Disable

**IROMCEN:** IROM clock enable

0 = Enable

1 = Disable

**RAM2CEN:** RAM2 clock enable

0 = Enable

1 = Disable

**IDLE:** IDLE mode

0 = Disable

1 = Enable IDLE mode

**HOLD:** HOLD mode

0 = Disable

1 = Enable HOLD mode

**SLEEP:** SLEEP mode

0 = Disable

1 = Enable SLEEP mode

Register 4-3 PCON1 – Power control 1

Position	7	6	5	4	3	2	1	0
Name	DACCEN	MP3CEN	IISCEN	TMRCEN	UARTCEN	SDCCEN	WMACEN	SPICEN
Default	1	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**DACCEN:** DAC clock enable

0 = Enable

1 = Disable

**MP3CEN:** MP3 decoder clock enable

0 = Enable

1 = Disable

**IISCEN:** IIS clock enable

0 = Enable

1 = Disable

**TMRCEN:** Timer clock enable

0 = Enable

1 = Disable

**UARTCEN:** UART clock enable

0 = Enable

1 = Disable

**SDCCEN:** SDC clock enable

0 = Enable

1 = Disable

**WMACEN:** WMA Decode clock enable

0 = Enable

1 = Disable

**SPICEN:** SPI clock enable

0 = Enable

1 = Disable

Register 4-4 PCON2 – Power control 2

Position	7	6	5	4	3	2	1	0
Name	MP3ECEN	USBCEN	OTPCEN	EMICEN	RTCCEN	WDTCCEN	LVDCEN	ADCCEN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**MP3ECEN:** MP3 Decode clock enable

0 = Enable

1 = Disable

**USBCEN:** USB clock enable

0 = Enable

1 = Disable

**OTPCEN:** OTP clock enable

0 = Enable

1 = Disable

**EMICEN:** EMI clock enable

0 = Enable

1 = Disable

**RTCCEN:** RTCC clock enable

0 = Enable

1 = Disable

**WDTCCEN:** WDT clock enable

0 = Enable

1 = Disable

**LVDCEN:** LVD clock enable

0 = Enable

1 = Disable

**ADCCEN:** ADC clock enable

0 = Enable

1 = Disable

Register 4-5 PCON3 – Power control 3

Position	7	6	5	4	3	2	1	0
Name	IISREFCSEL	OTP2ICEN	BASSCEN	AUALUEN	reserved	reserved	RCEN	ISPCEN
Default	0	0	1	1	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IISREFCSEL:** IIS Reference clock source select

0 = Select system clock

1 = Select XOSC12M

**OTP2ICEN:** OTP to IRAM clock enable

0 = Enable

1 = Disable

**BASSCEN:** Bass clock enable

0 = Enable

1 = Disable

**AUALUEN:** Audio clock enable

0 = Enable

1 = Disable

**RCEN:** RC enable bit

0 = Disable

1 = Enable

**ISPCEN:** ISP clock enable

0 = Enable

1 = Disable

Register 4-6 CLKCON – Clock control

Position	7	6	5	4	3	2	1	0
Name	OTPDIV	RCSEL		WDTCSSEL	RTCCS		SCSEL	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**OTPDIV:** OTP clock divide 2 from system clock

0 = Disable

1 = Enable

**RCSEL:** RC frequency select

00 = RC 512K

01 = RC 32K

10 = RC 6M

11 = RC 12M

**WDTCSSEL:** WDT clock section

0 = Internal 32 KHz RC oscillator output

1 = External 32 KHz or 12MHz crystal oscillator controlled by CLKCON2 [6] and CLKCON2 [7] as shown in [Figure 4-3](#)

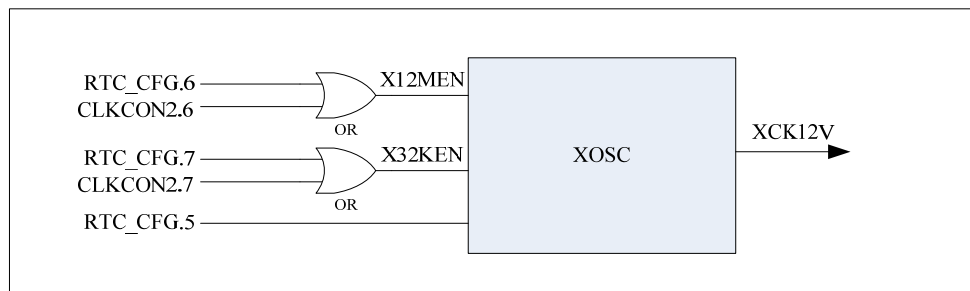


Figure 4-3 Source of XCK12V

**RTCCS:** RTCC clock source select

00 = External 32 KHz or 12MHz crystal oscillator controlled by CLKCON2 [6] and CLKCON2 [7] as shown in [Figure 4-3](#)

01 = Internal 32 KHz RC oscillator output

10 = Select 32 KHz clock source derived from external 12MHz crystal oscillator

11 = Reserved

**SCSEL:** System clock select

00 = Internal 512 KHz RC oscillator output

01 = External 32 KHz or 12MHz crystal oscillator controlled by PCON3 [5]

10 = PLL 48/24/16/12 MHz output, controlled by CLKCON [1:0]

11 = Reserved

Register 4-7 CLKCON1 – Clock control 1

Position	7	6	5	4	3	2	1	0
Name	ATCLKSEL		IISBCSEL	DECDIV	SYSDIV		PLLDIVSEL	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**ATCLKSEL:** Audio clock select

00 = Select external 12MHz crystal oscillator invert

01 = Select external 12MHz crystal oscillator

10 = Select PLL 24MHz output invert

11 = Select PLL 24MHz output

**IISBCSEL:** IIS BCLK generate clock source select

0 = Select system clock

1 = Select external 12MHz crystal oscillator

**DECDIV:** Decoder clock divide 2 from system clock

0 = Disable

1 = Enable

**SYSDIV:** System clock divide from clock source

00 = System clock source

01 = Divided by 2 from system clock source

10 = Divided by 4 from system clock source

11 = Divided by 8 from system clock source

**PLLDIVSEL:** PLL output divide select

00 = Select 48MHz output

01 = Select 24MHz output

10 = Select 16MHz output

11 = Select 12MHz output

Register 4-8 CLKCON2 – Clock control 2

Position	7	6	5	4	3	2	1	0
Name	XOSC32K_EN	XOSC12M_EN	XOSC2X_EN	Reserved	Reserved	Reserved	Reserved	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**XOSC32K\_EN:** XOSC 32K enable

0 = Disable

1 = Enable

**XOSC12M\_EN:** XOSC 12M enable

0 = Disable

1 = Enable

**XOSC2X\_EN:** XOSC frequency double enables

0 = Disable

1 = Enable

## 4.3.2 Phase Lock Loop (PLL)

CW6680E/CW6681E/CW6682E provides one on-chip Phase Locked Loop (PLL 48M) clock generators. The PLL has reference clock from external 32 KHz/4M/12 M crystal oscillators to provide a stable reference clock and the reference clock is multiplied to provide the final PLL output.

Register 4-9 PLLCON – PLL Configuration

Position	7	6	5	4	3	2	1	0
Name	RC_SEL	OSC_SEL	OFFSET_EN	X12EN	REF_SEL		PLLDEN	PLLAEN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**PLLAEN:** PLL analog module enables

0 = Disable

1 = Enable

**PLLDEN:** PLL digital module enables

0 = Disable

1 = Enable

When change the divider, also need write 1 to PLLDEN

**REF\_SEL:** PLL input reference clock select

00 = 12M XOSC

01 = 4M XOSC

10 = 32K XOSC

11 = RC

**X12EN:** XOSC 12M 374 divider enable bit

0 = Disable

1 = Enable

**OFFSET\_EN:** enable SSC

0 = Disable

1 = Enable

**OSC\_SEL:** PLL XOSC input select

0 = Select XOSC output (4M, 12M or 32.768K)

1 = Select XOSC 12.288M 374 divide clock

**RC\_SEL:** PLL input RC select

0 = Select RC output

1 = Select XOSC



## 5 Low Power Management

### 5.1 Power Saving Mode

CW6680E/CW6681E/CW6682E device has the low power management mode that can help reducing power consumption when the device does not require intensive CPU resources and speed. There are four low power modes available: SLEEP mode, Hold mode, IDLE mode and deep sleep mode.

#### 5.1.1 Sleep Mode

SLEEP mode is an ultimate power reduction mode that will stop all the clock sources, and all the memory chip select signals are disabled to further reduce power consumption. However, before entering sleep mode, all peripherals should be disabled separately, especially those analog peripherals and memory, unless those peripherals will stop themselves if no clock source is applied to the peripherals.

**Note:** Before Entering SLEEP mode, the system clock is recommended to change back to oscillator clock as the system clock.

To enter SLEEP mode, user need to write a '1' to SLEEP register (Bit0 of PCON0).

During SLEEP mode, the device can be wake up by either external port wakeup reset or watchdog reset or RTCC reset.

After exit SLEEP mode by wakeup, the device will be reset.

SLEEP mode will enable DEGRAM and IRAM and system clock automatically.

#### 5.1.2 Hold Mode

HOLD mode will stop the clock from entering to system. The system clock is gated with the HOLD mode control. Once enter HOLD mode, clock to the system logic halts. Therefore, there will be no clock switching entering the system logic so that power consumption is minimized due to no AC switching. However, the clock sources are not disabled and they are still running. This allows the clock to be resumed in real time without waiting for the PLL to lock again. Watchdog interrupt, RTCC interrupt, Port interrupt and all reset event will cause system to exit HOLD mode.

TO enter HOLD mode, user need to write a '1' to HOLD register (Bit1 of PCON0).

When wakeup from HOLD Mode by port or RTCC, if interrupt is enabled, CW6680E/CW6681E/CW6682E enters corresponding interrupt service subroutine (ISR), else CW6680E/CW6681E/CW6682E will execute the instruction following HOLD.

When wakeup from HOLD Mode by watchdog, if watchdog reset enable, CW6680E/CW6681E/CW6682E will be reset, else if watchdog interrupt is enabled, CW6680E/CW6681E/CW6682E will enter watchdog's ISR. Else CW6680E/CW6681E/CW6682E will execute the instruction following HOLD.

#### 5.1.3 Idle Mode

IDLE mode will stop the clock from entering to the CPU. The CPU clock is gated with the IDLE mode control. Once enter IDLE mode, clock to the CPU logic halts. Therefore, there will be no clock switching entering the CPU logic so CPU power consumption is minimized.

All interrupt sources will cause system to exit IDLE mode, which include all peripheral interrupt.

TO enter IDLE mode, user need to write a '1' to IDLE register (Bit2 of PCON0).

When exit IDLE mode, CW6680E/CW6681E/CW6682E will enter interrupt service subroutine if EA is enable. If EA is disabled, the instruction next to IDLE will be executed.

## 5.2 Power Supply

CW6680E/CW6681E/CW6682E provides two on-chip low drop-out regulators (LDO) to convert from 5V to 3.3V, 3.3V to 1.2V for internal core power use. It is there to provide high power supply noise rejection and also to minimize power consumption. LDO is always enabled.

To provide a more stable and reliable power source to internal core logic, it is recommended to add frequency compensation through external component. [Figure 5-1](#) shows the connection.

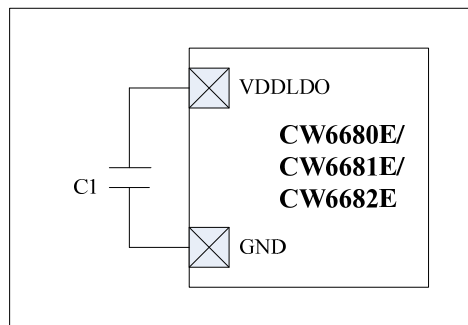


Figure 5-1 Frequency compensation through external component

### Note:

- The recommended value for C1 is 10Uf.
- C1 should be placed closely to the chip.

LDO enable and current select configure, please refer to “Register 9-19 PWRCON – Power control”

Register 5-1 PWRCON1 – Power control 1

Position	7	6	5	4	3	2	1	0
Name	Reserved		BATO_OE	SDPG_EN	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**BATO\_OE:** battery output enable bit

0 = Disabled

1 = Enabled

**SDPG\_EN:** SD power gate enable bit

0 = Disabled

1 = Enabled

## 6 General Purpose Input/Output (GPIO)

### 6.1 Overview

The general purpose input/output port (GPIO) provides 30 dedicated general purpose one-bit contacts that can be individually configured as either inputs or outputs. Contacts configured as outputs reflect internal register values, and those configured as inputs can be detected by reading internal registers. All GPIOs are divided into 4 groups: Port0, Port1, Port2, and Port3.

### 6.2 Features

The GPIO includes the following features:

- Drive specific data to output using the data register;
- Control the direction of the signal using the GPIO direction register;
- Enable CPU to sample the status of the corresponding inputs by reading the data register;
- Enable internal pull-up resistor using pull-up resistor control register;
- Select suitable pull-up resistor value;
- Enable internal pull-up resistor using pull-down resistor control register;
- Select suitable pull-down resistor value;
- Select suitable output driving current capability;

There are 4 types of GPIO that can meet the variation of application requirements. [Table 6-1](#) shows the difference between pad types

Table 6-1 Pad types

Type	Driving (mA)		Pull-up resistor (Kohm)			Pull-down resistor (Kohm)				Mode
A	8	/	10	/	/	10	/	/	/	Normal
B	8	/	10	2	/	10	2	/	/	Normal
C	8	/	10	2	/	10	2	0.2	/	Normal
D	8	/	10	2	/	10	2	/	/	Reserved
E	8	24	10	2	0.5	10	2	3.3	0.5	Reserved
F	8	/	10	2	0.5	10	2	3.3	0.5	Reserved
G	8	24	10	2	/	10	2	/	/	Reserved
H	8	24	10	2	0.5	10	2	/	0.5	Reserved
I	/	/	/	/	/	/	/	/	/	Analog

## 6.3 Function multiplexing

In order to provide more flexible port functions and to minimize pin counts, some of the ports are multiplexed with other peripherals or functions. [Table 6-2](#) illustrates the “Ports multiplexed mapping”.

Several GPIO are multiplexed with analog module. GPIO digital input and output must be disabled when the corresponding analog module is enabled.

Table 6-2 Ports multiplexed mapping

Pins	Func1	Func2	Func 3	Func4	Func5	Func6	Func7	Func8	Type
P00	/	/	AUXL0	/	SDDAT1	/	SPI0DI2	UART0RX1	B
P01	/	/	AUXR0	/	SDDAT2	/	/	UART0TX1	B
P02	MICIN0	/	AUXR2	/	/	/	/	/	I
P03	MICIN1	VCMBUF	AUXL2	/	/	/	/	/	I
P04	ADC2	INT0	SPI1DO1	SPI1DODI1	PWM1	SPI0DODI1	SPI0DO1	/	D
P05	ADC3	INT1	SPI1CLK1	/	/	CAP0	SPI0CLK1	/	D
P06	ADC1	/	SPI1DI1	/	TMR1	TMR0	SPI0DI1	/	B
P07	/	INT3	/	/	CAP1	IR0	/	/	A
P10	/	EMIWR	/	/	/	/	/	/	G
P11	/	/	/	/	/	/	/	/	G
P12	/	/	/	/	/	/	/	/	G
P13	ADC5	/	/	/	/	/	/	/	H
P14	/	PWM3	CAP3	/	SDDAT3	SPI0DODI2	SPI0DO2	/	D
P15	/	TMR3	/	/	/	/	/	/	C
P16	ADC8	PWM2	IISREFCLK	AMIN	CAP2	UART1TX1	/	UART0TX0	B
P17	/	TMR2	IISWS	/	/	UART1RX1	/	/	B
P20	/	EMID0	IISBCLK	/	SDCMD0	/	/	/	F
P21	/	EMID1	IISDI0	/	SDCLK0	/	/	/	F
P22	/	EMID2	IISDO0	/	/	/	/	/	F
P23	/	EMID3	IISDI1	/	/	/	/	/	F
P24	/	EMID4	IISDO1	/	/	/	/	/	F
P25	/	EMID5	/	/	SPI0DO3	/	SPI0DI0	/	F
P26	/	EMID6	/	/	/	/	SPI0CLK0	/	F
P27	/	EMID7	/	/	SDDAT00	SPI0DODI0	SPI0DO0	/	E
P30	ADC4	/	SPI1CLK0	/	SDCLK1	/	/	/	F
P31	/	/	SPI1DI0	/	SDCMD1	/	/	/	F
P32	/	/	SPI1DO0	SPI1DODI0	SDDAT01	/	/	/	E
P33	ADC0	PWRWKUP	LVDDDET	/	/	IR1	CLKO	/	B
P34	/	INT2	/	/	/	PWM0	SPI0CLK2	UART0RX0	B
P35	UDSW	/	/	/	/	/	/	/	A
P36	/	VPG33	AUXR1	/	/	UART1TX0	/	/	B
P37	/	/	AUXL1	/	/	UART1RX0	/	/	C

## 6.4 Port interrupt and wakeup

CW6680E/CW6681E/CW6682E supports Port interrupt and wakeup function.

The PWKEN registers (Wakeup Enable Register) allow P04, P05, P34/DP/DM and P07 to cause wakeup.

The PWKEN registers are set to 0Fh upon reset. Clearing bit0-3 in the PWKEN register enables wakeup on corresponding pin of P04, P05, P34/DP/DM and P07. The trigger condition on the selected pin can be either rising edge or falling edge. The WKED register (Wakeup Edge Select) selects the desired transition edge. Setting a bit in WKED register selects the falling edge of the corresponding P04, P05, P34/DP/DM and P07 pin. Resetting the bit selects the rising edge.

Once a valid transition occurs on the selected pin, the WKPND (PWKEN.7~PWKEN.4) register (Wakeup Pending Register) latches the transition in the corresponding bit position. Logic '1' indicates the occurrence of the selected trigger edge on the corresponding Port pins. Upon reset, logic '0' is set to all bits of WKPND.

### Note:

- To Wakeup initialization, to avoid any false signaling to port, the followings would be a recommended procedure for Wakeup initialization:
  - Configure the edge select of Port 0 pins on WKEDG register,
  - Clear the corresponding bits on WKPND Wakeup Pending Register
  - Clear the corresponding bits in the PWKEN registers to enable the wakeup on the corresponding port pins
- Upon exiting the sleep down mode, the Multi-Input Wakeup logic causes full chip reset.

## 6.5 GPIO Special Function Registers

Register 6-1 P0DIR-P0 direction Register

Position	7	6	5	4	3	2	1	0
Name	P0DIR							
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P0DIR [0:1] and P0DIR [4:7]:** P0x direction control

0 = Output

1 = Input

**P0DIR [2]:** P03 direction control

0 = Output

1 = Input

**P0DIR [3]:** P02 direction control

0 = Output

1 = Input

**NOTE:** P0DIR [2] control P03, P0DIR [3] control P02.

Register 6-2 P1DIR-P1 direction Register

Position	7	6	5	4	3	2	1	0
Name	P1DIR							
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P1xDIR:** P1x direction control

0 = Output

1 = Input

Register 6-3 P2DIR-P2 direction Register

Position	7	6	5	4	3	2	1	0
Name	P2DIR							
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P2xDIR:** P2x direction control

0 = Output

1 = Input

Register 6-4 P3DIR-P3 direction Register

Position	7	6	5	4	3	2	1	0
Name	P3DIR							
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P3xDIR:** P3x direction control

0 = Output

1 = Input

Register 6-5 P0 – P0 data register

Position	7	6	5	4	3	2	1	0
Name	P0							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P0[x]: P0x data. Valid when P0x is used as GPIO

0 = P0x is in low state when read and output low at P0x when write

1 = P0x is in high state when read and output high at P0x when write

**NOTE:** P0 [3:2] are reserved.

Register 6-6 P1 – P1 data register

Position	7	6	5	4	3	2	1	0
Name	P1							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

P1[x]: P1x data. Valid when P1x is used as GPIO

0 = P1x is in low state when read and output low at P1x when write

1 = P1x is in high state when read and output high at P1x when write

Register 6-7 P2 – P2 data register

Position	7	6	5	4	3	2	1	0
Name	P2							
Default	x	x	x	x	x	x	x	x
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P2[x]: P2x data. Valid when P2x is used as GPIO

0 = P2x is in low state when read and output low at P2x when write

1 = P2x is in high state when read and output high at P2x when write

Register 6-8 P3 – P3 data register

Position	7	6	5	4	3	2	1	0
Name	P3							
Default	x	x	x	x	x	x	x	x
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P3[x]: P3x data. Valid when P3x is used as GPIO

0 = P3x is in low state when read and output low at P3x when write

1 = P3x is in high state when read and output high at P3x when write

Register 6-9 P0PU0 – P0 pull-up resistor control

Position	7	6	5	4	3	2	1	0
Name	P07PU0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P07PU0: P07 10KΩ pull-up resistor control. Valid when P07 is used as input

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

Register 6-10 P1PU0 – P1 pull-up resistor control

Position	7	6	5	4	3	2	1	0
Name	P1PU7	P1PU6	P1PU5	P1PU4	P1PU3	P1PU2	P1PU1	P1PU0
Default	0	0	0	0	1	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P1PU7: P17 10KΩ pull-up resistor control. Valid when P17 is used as input

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU6: P16 10KΩ pull-up resistor control. Valid when P16 is used as input.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU5: P15 10KΩ pull-up resistor control. Valid when P15 is used as input.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU4: P14 10KΩ pull-up resistor control. Valid when P14 is used as input.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU3: P13 10KΩ pull-up resistor control. Valid when P13 is used as input

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU2: P12 10KΩ pull-up resistor control. Valid when P12 is used as input

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU1: P11 10KΩ pull-up resistor control. Valid when P11 is used as input.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P1PU0: P10 10KΩ pull-up resistor control. Valid when P10 is used as input.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

Register 6-11 P2PU0 – P2 pull-up resistor control low byte

Position	7	6	5	4	3	2	1	0
Name	P23PU0		P22PU0		P21PU0		P20PU0	
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P2xPU0 [x]: P2x pull-up resistor control. Valid when P2x is used as input

00 = resistor disabled

01 = 10KΩ pull-up resistor enabled

10 = 500Ω pull-up resistor enabled

11 = reserved

Register 6-12 P2PU1 – P2 pull-up resistor control high byte

Position	7	6	5	4	3	2	1	0
Name	P27PU1		P26PU1		P25PU1		P24PU1	
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P2xPU0 [x]: P2x pull-up resistor control. Valid when P2x is used as input

00 = resistor disabled

01 = 10KΩ pull-up resistor enabled

10 = 500Ω pull-up resistor enabled

11 = reserved



Register 6-13 P3PU0 – P3 pull-up resistor control

Position	7	6	5	4	3	2	1	0
Name	P34PU0	P33PU0	P32PU0		P31PU0		P30PU0	
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P34PU0/ P33PU0: P34/P33 10K $\Omega$  pull-up resistor control. Valid when P34/P33 is used as input

0 = resistor disabled

1 = 10K $\Omega$  pull-up resistor enabled

P32PU0/ P31PU0/ P30PU0: P32/P31/P30 pull-up resistor control. Valid when P32/P31/P30 is used as input

00 = resistor disabled

01 = 10K $\Omega$  pull-up resistor enabled

10 = 500 $\Omega$  pull-up resistor enabled

11 = reserved

Register 6-14 P0PD0 – P0 pull-down resistor control

Position	7	6	5	4	3	2	1	0
Name	P07PD0	P06PD0	P05PD0	P04PD0	Reserved	Reserved	P01PD0	P00PD0
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P0xPD0: P0x 10K $\Omega$  pull-down resistor control. Valid when P0x is used as input

0 = 10K $\Omega$  pull-down resistor disabled

1 = 10K $\Omega$  pull-down resistor enabled

Register 6-15 P1PD0 – P1 10K $\Omega$  pull-down resistor control

Position	7	6	5	4	3	2	1	0
Name	P1PD0							
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

PDN1[x]: P1x 10K $\Omega$  pull-down resistor control. Valid when P1x is used as input

0 = 10K $\Omega$  pull-down resistor disabled

1 = 10K $\Omega$  pull-down resistor enabled

Register 6-16 P2PD0 – P2 3.3K $\Omega$  pull-down resistor control

Position	7	6	5	4	3	2	1	0
Name	P23PD0		P22PD0		P21PD0		P20PD0	
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P2PD0: P2x pull-down resistor control. Valid when P2x is used as input

00 = resistor disabled

01 = 10K $\Omega$  pull-down resistor enabled

10 = 500 $\Omega$  pull-down resistor enabled

11 = 3.3KΩ pull-down resistor enabled

Register 6-17 P2PD1 – P2 0.5KΩ pull-down resistor control

Position	7	6	5	4	3	2	1	0
Name	P27PD1		P26PD1		P25PD1		P24PD1	
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P2PD0: P2x pull-down resistor control. Valid when P2x is used as input

00 = resistor disabled

01 = 10KΩ pull-down resistor enabled

10 = 500Ω pull-down resistor enabled

11 = 3.3KΩ pull-down resistor enabled

Register 6-18 P3PD0 – P3 10KΩ pull-down resistor control

Position	7	6	5	4	3	2	1	0
Name	P34PD0	P33PD0	P32PD0		P31PD0		P30PD0	
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P34PD0/P33PD0: P34/P33 10KΩ pull-down resistor control. Valid when P34/P33 is used as input

0 = 10KΩ pull-down resistor disabled

1 = 10KΩ pull-down resistor enabled

P32PD0/P31PD0/P30PD0: P32/P31 /P30 10KΩ pull-down resistor control. Valid when P32/P31/P30 is used as input

00 = 1 resistor disabled

01 = 10KΩ pull-down resistor enabled

10 = 500Ω pull-down resistor enabled

11 = 3.3KΩ pull-down resistor enabled

Register 6-19 P3PUD1 – P3 10KΩ pull-down resistor control

Position	7	6	5	4	3	2	1	0
Name	P13HPD	P13HPU	P37PU	P36PU	P35PU	P37PD	P36PD	P35PD
Default	0	0	0	0	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

P13HPD: P13 500Ω pull-down resistor control. Valid when P13 is used as input

0 = 500Ω pull-down resistor disabled

1 = 500Ω pull-down resistor enabled

P13HPU: P13 500Ω pull-up resistor control.

0 = 500Ω pull-up resistor disabled

1 = 500Ω pull-up resistor enabled

P37PU/P36PU/P35PU: P37PU/P36PU/P35PU pull-up resistor control.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

P37PD/P36PD/P35PD: P37PD/P36PD/P35PD pull-down resistor control.

0 = 10KΩ pull-down resistor disabled

1 = 10KΩ pull-down resistor enabled

Register 6-20 PIE0 – Port digital input enable control

Position	7	6	5	4	3	2	1	0
Name	PIE07	PIE06	PIE05	PIE04	PIE03	PIE02	PIE01	PIE00
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**PIE07:** P07 digital input enables bit (For VPP input)

0 = P07 Input Disabled

1 = P07 Input Enabled

**PIE06:** P06 digital input enables bit (For ADC1 input)

0 = P06 Input Disabled

1 = P06 Input Enabled

**PIE05:** P05 digital input enables bit (For ADC3 input)

0 = P05 Input Disabled

1 = P05 Input Enabled

**PIE04:** P04 digital input enables bit (For ADC2 input)

0 = P04 Input Disabled

1 = P04 Input Enabled

**PIE03:** P13 Digital Input Enable Bit (For ADC5 input)

0 = P13 Input Disabled

1 = P13 Input Enabled

**PIE02:** P30 Digital Input Enable Bit (For ADC4 input)

0 = P30 Input Disabled

1 = P30 Input Enabled

**PIE01:** P01 Digital Input Enable Bit (For AUXR0)

0 = P01 Input Disabled

1 = P01 Input Enabled

**PIE00:** P00 Digital Input Enable Bit (For AUXL0)

0 = P00 Input Disabled

1 = P00 Input Enabled

Register 6-21 PIE1 – Port digital input enable control1

Position	7	6	5	4	3	2	1	0
Name	-	-	PIE15	PIE14	PIE13	PIE12	PIE11	PIE10
Default	-	-	1	1	1	1	1	1
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

**PIE15:** P37 Digital Input Enable Bit (For AUXL1)

0 = P37 digital Input Disabled

1 = P37 digital Input Enabled

**PIE14:** P36 Digital Input Enable Bit (For AUXR1)

0 = P36 digital Input Disabled

1 = P36 digital Input Enabled

**PIE13:** P35 Digital Input Enable Bit (For UDSW).

0 = P35 digital Input Enabled

1 = P35 digital Input Disabled

**PIE12:** P33 Digital Input Enable Bit (For ADC0/LVDDDET input)

0 = P33 digital Input Disabled

1 = P33 digital Input Enabled

**PIE11:** P17 Digital Input Enable Bit

0 = P17 digital Input Disabled

1 = P17 digital Input Enabled

**PIE10:** P16 Digital Input Enable Bit (For AMIN or ADC8 input)

0 = P16 digital Input Disabled

1 = P16 digital Input Enabled

Register 6-22 P0DRV0 – Port 0 Driving control

Position	7	6	5	4	3	2	1	0
Name	P07DRV	P06DRV	P05DRV	P04DRV	Reserved	Reserved	P01DRV	P00DRV
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P07DRV:** P07 Driving selection Bit

0 = P07 Driving is 8mA

1 = P07 Driving is 10Kohm pull-up/pull-down resistor

**P06DRV:** P06 10KΩ pull-up resistor control.

0 = 10KΩ pull-down resistor disabled

1 = 10KΩ pull-down resistor enabled

**P05DRV:** P05 10KΩ pull-up resistor control.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

**P04DRV:** P04 10KΩ pull-up resistor control.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

**P01DRV:** P01 10KΩ pull-up resistor control.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

**P00DRV:** P00 10KΩ pull-up resistor control.

0 = 10KΩ pull-up resistor disabled

1 = 10KΩ pull-up resistor enabled

Register 6-23 P1DRV0 – Port 1 Driving control 0

Position	7	6	5	4	3	2	1	0
Name	P13DRV		P12DRV		P11DRV		P10DRV	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P13DRV:** P13 Driving selection Bit

00 = P13 Driving is 8mA

01 = P13 Driving is 2Kohm pull-up/pull-down resistor

1x = P13 Driving is 24mA

**P12DRV:** P12 Driving selection Bit

00 = P12 Driving is 8mA

01 = P12 Driving is 2Kohm pull-up/pull-down resistor

1x = P12 Driving is 24mA

**P11DRV:** P11 Driving selection Bit

00 = P11 Driving is 8mA

01 = P11 Driving is 2Kohm pull-up/pull-down resistor

1x = P11 Driving is 24mA

**P10DRV:** P10 Driving selection Bit

00 = P10 Driving is 8mA

01 = P10 Driving is 2Kohm pull-up/pull-down resistor

1x = P10 Driving is 24mA

Register 6-24 P1DRV1 – Port 1 Driving control 1

Position	7	6	5	4	3	2	1	0
Name	reserved	P2SD_DRVEN	P3SD_DRVEN	SDDRV	P17DRV	P16DRV	P15DRV	P14DRV
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P2SD\_DRVEN:** P20/P21/P27 (SDC IO for 3 wires mode) Driving control

0 = P20/P21/P27 is drive by push-pull mode

1 = P20/P21/P27 is drive by 10K/500 ohm pull-up/pull-down resistor

**P3SD\_DRVEN:** P30/P31/P32 (SDC IO for 3 wires mode) Driving control

0 = P30/P31/P32 is drive by push-pull mode

1 = P30/P31/P32 is drive by 10K/500 ohm pull-up/pull-down resistor

**SD\_DRV:** Pull-up/pull-down resistor selection for SDC IO driving

0 = 10K ohm

1 = 500 ohm

**P17DRV:** P17 Driving selection Bit

0 = P17 Driving is 8mA

1 = P17 Driving is 2Kohm pull-up/pull-down resistor

**P16DRV:** P16 Driving selection Bit

0 = P16 Driving is 8mA

1 = P16 Driving is 2Kohm pull-up/pull-down resistor

**P15DRV:** P15 Driving selection Bit

0 = P15 Driving is 8mA

1 = P15 Driving is 2Kohm pull-up/pull-down resistor

**P14DRV:** P14 Driving selection Bit

0 = P14 Driving is 8mA

1 = P14 Driving is 2Kohm pull-up/pull-down resistor

Register 6-25 P2DRV0 – Port 2 Driving control

Position	7	6	5	4	3	2	1	0
Name	USBSR0	P26DRV	P25DRV	P24DRV	P23DRV	P22DRV	P21DRV	P20DRV
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**USBSR0:** USB DP/DM slew rate control selection Bit 0

**P26DRV:** P26 Driving selection Bit

0 = P26 Driving is 8mA

1 = P26 Driving is 2Kohm pull-up/pull-down resistor

**P25DRV:** P25 Driving selection Bit

0 = P25 Driving is 8mA

1 = P25 Driving is 2Kohm pull-up/pull-down resistor

**P24DRV:** P24 Driving selection Bit

0 = P24 Driving is 8mA

1 = P24 Driving is 2Kohm pull-up/pull-down resistor

**P23DRV:** P23 Driving selection Bit

0 = P23 Driving is 8mA

1 = P23 Driving is 2Kohm pull-up/pull-down resistor

**P22DRV:** P22 Driving selection Bit

0 = P22 Driving is 8mA

1 = P22 Driving is 2Kohm pull-up/pull-down resistor

**P21DRV:** P21 Driving selection Bit

0 = P21 Driving is 8mA

1 = P21 Driving is 2Kohm pull-up/pull-down resistor

**P20DRV:** P20 Driving selection Bit

0 = P20 Driving is 8mA

1 = P20 Driving is 2Kohm pull-up/pull-down resistor

Register 6-26 P3DRV0 – Port 3 Driving control

Position	7	6	5	4	3	2	1	0
Name	P27DRV		P34DRV	P33DRV	P32DRV		P31DRV	P30DRV
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**P27DRV:** P27 Driving selection Bit

00 = P27 Driving is 8mA

01 = P27 Driving is 2Kohm pull-up/pull-down resistor

10 = P27 Driving is 24mA

11 = P27 Driving is 24mA

**P34DRV:** P34 Driving selection Bit

0 = P34 Driving is 8mA

1 = P34 Driving is 2Kohm pull-up/pull-down resistor

**P33DRV:** P33 Driving selection Bit

0 = P33 Driving is 8mA

1 = P33 Driving is 2Kohm pull-up/pull-down resistor

**P32DRV:** P32 Driving selection Bit

00 = P32 Driving is 8mA

01 = P32 Driving is 2Kohm pull-up/pull-down resistor

10 = P32 Driving is 24mA

11 = P32 Driving is 24mA

**P31DRV:** P31 Driving selection Bit

0 = P31 Driving is 8mA

1 = P31 Driving is 2Kohm pull-up/pull-down resistor

**P30DRV:** P30 Driving selection Bit

0 = P30 Driving is 8mA

1 = P30 Driving is 2Kohm pull-up/pull-down resistor

Register 6-27 P3DRV1 – Port 3 Driving control

Position	7	6	5	4	3	2	1	0
Name	P37DRV	P36DRV	P35DRV	reserved	-	-	-	-
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	RO	RO	RO	RO

**P37DRV:** P37 Driving selection Bit.

0 = P37 Driving is 8mA

1 = P37 Driving is 2Kohm pull-up/pull-down resistor

**P36DRV:** P36 Driving selection Bit

0 = P36 Driving is 8mA

1 = P36 Driving is 2Kohm pull-up/pull-down resistor

**P35DRV:** P35 Driving selection Bit

0 = P35 Driving is 8mA

1 = P35 Driving is 10Kohm pull-up/pull-down resistor

Register 6-28 PMUXCON0 – Port Function MUX control 0

Position	7	6	5	4	3	2	1	0
Name	Reserved	UART1_MAP	SPI1_MAP	SPI0_DO_P25	WKPIN_SEL		SDTWO	P2SDEN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**UART1\_MAP:** UART1 port mapping

0 = Select P36, P37

1 = Select P16, P17

**SPI1\_MAP:** SPI1 port mapping

0 = Select P04, P05, P06

1 = Select P30, P31, P32

**SPI0\_DO\_P25:** SPI0 DOUT output at P25

0 = Disable

1 = Enable

**WKPIN\_SEL:** Port interrupt/wakeup event 2 sources selection

00 = Select INT2

01 = Select DP

10 = Select DM

11 = Select IRTWKO

**SDTWO:** Dual SD card mode control

0 = only support one SD card plugged in at the same time

1 = support two SD cards plugged in at the same time. P30 is SDCLK shared by these two SD cards.

**P2SDEN:** SDCCLK, SDCCMD and SDCDAT0 port mapping control

0 = SDCCLK, SDCCMD and SDCDAT0 are mapped to P30, P31 and P32.

1 = SDCCLK, SDCCMD and SDCDAT0 are mapped to P20, P21 and P27

## 6.5.1 Wakeup registers

Register 6-29 PWKEN – Port wakeup enable

Position	7	6	5	4	3	2	1	0
Name	WKPND3	WKPND2	WKPND1	WKPND0	PWKEN3	PWKEN2	PWKEN1	PWKEN0
Default	0	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**WKPND3**

0 = No INT3 wakeup event occurred

1 = INT3 wakeup event occurred

**WKPND2**



0 = No INT2/DP/DM/IRTWKO wakeup event occurred

1 = INT2/DP/DM/IRTWKO wakeup event occurred

#### WKPND1

0 = No INT1 wakeup event occurred

1 = INT1 wakeup event occurred

#### WKPND0

0 = No INT0 wakeup event occurred

1 = INT0 wakeup event occurred

#### PWKEN3

0 = Enable INT3 Wakeup

1 = Disable INT3 Wakeup

#### PWKEN2

0 = Enable INT3/DP/DM/IRTWKO Wakeup

1 = Disable INT3/DP/DM/IRTWKO Wakeup

#### PWKEN1

0 = Enable INT1 Wakeup

1 = Disable INT1 Wakeup

#### PWKEN0

0 = Enable INT0 Wakeup

1 = Disable INT0 Wakeup

#### Note:

1. to enable WKPNDx, set PWKENx to '0'.
2. To clear WKPNDx, write '0' to WKPNDx. WKPNDx will be '0' 2 clocks later after write '0' to WKPNDx.
3. WKPNDx is cleared when PWKENx is '1'.

Register 6-30 PWKEDGE – Port wakeup Event select

Position	7	6	5	4	3	2	1	0
Name	LDOBGOE	SPI0PS1	COSEL		WKEDG3	WKEDG2	WKEDG1	WKEDG0
Default	0	0	0	0	x	x	x	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**LDOBGOE:** LDO Bandgap output enable

0 = Disable

1 = Enable

**SPI0PS1:** SPI0 port select 1. See chapter 16 SPI0

**COSEL:** CLKO sources selection

00 = P3 [3]

01 = PLL 12MHz

10 = System clock

11 = XOSCO

**WKEDGx:** Port interrupt Edge Select

0 = Select rising edge as interrupt trigger event

1 = Select falling edge as interrupt trigger event

## 6.6 Operation Guide

Port 0 to Port 3 are memory-mapped into the Data Memory addressing space. They are respectively mapped into 80h, 90h, A0h and B0h registers for ports P0, P1, P2 and P3. Writing to a port data register sets the voltage levels of the corresponding port pins that have been configured to operate as outputs. Reading from a data register reads the voltage levels of the corresponding port pins.

As illustrated in Figure 8-1, there are major differences reading the port values when the port is set as input and output. When the port is set as output, the CPU will read the port value from Px register instead of the port pin value. When the port is set as input, the CPU will read the value from port pin directly instead of the port value from Px register. As a result, the user should be very careful when using Read-then-Write instructions to access the ports and change PxDIR before write the output value to Px when using port as output. For example:

Code assembler:

```
ANL P0DIR, #0FEH
MOV P0, #01h
```

Code C51:

```
P0DIR &= 0Xfe;
P0 = 0x01;
```

The first instruction in this example configures P00 as output, and then the second instruction writes the Port 0 data register (P0), which controls the output levels of the Port 0 pins, P00 through P07. Figure 8-1 shows the internal hardware structure and configuration registers for each pin of Port 0~3.

## 7 Timers

### 7.1 Timer0

Timer0 is an 8-bit timer/counter with a 7-bit prescaler. It can be configured as timer, counter or PWM generator.

#### 7.1.1 Timer0 Features

- 8bits counter
- 7bits pre-scaler
- Counter mode (clock source from system clock or TMR0)
- Capture mode (event source from CAP0)
- PWM mode (PWM signal output to PWM0)

#### 7.1.2 Timer0 Special Function Registers

Register 7-1 TMR0CON – Timer0 control

Position	7	6	5	4	3	2	1	0
Name	T0PND	T0ES	T0M		T0IS	T0PSR		
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**T0PND:** Timer0 Pending Flag

0 = Not Pending

1 = Pending

**T0ES:** Timer0 Capture Mode Edge Select

0 = CAP0 Rising Edge

1 = CAP0 Falling Edge

**T0M:** Timer0 Mode

00 = Timer0 is disabled

01 = Timer0 is enabled and works in Counter Mode

10 = Timer0 is enabled and works in PWM Mode

11 = Timer0 is enabled and works in Capture Mode

**T0IS:** Timer0 Increase Source

0 = Select system clock cycle

1 = Select TMR0 rising edge

**T0PSR:** Timer0 Prescaler

000 = Timer0 counts at every counting source event

001 = Timer0 counts at every 2 counting source events

010 = Timer0 counts at every 4 counting source events

011 = Timer0 counts at every 8 counting source events

100 = Timer0 counts at every 16 counting source events

101 = Timer0 counts at every 32 counting source events

110 = Timer0 counts at every 64 counting source events

111 = Timer0 counts at every 128 counting source events

Register 7-2 TMR0CNT – Timer0 Counter

Position	7	6	5	4	3	2	1	0
Name	TMR0CNT							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** Timer0 will increase in proper condition while it is enabled. It overflows when TMR0CNT = TMR0PR, TMR0CNT will be clear to 0x00 when overflow occurs, and the interrupt flag will be set '1' by hardware.

Register 7-3 TMR0PR – Timer0 Period

Position	7	6	5	4	3	2	1	0
Name	TMR0PR							
Default	1	1	1	1	1	1	1	1
Access	WO	WO	WO	WO	WO	WO	WO	WO

**Note:** The overflow period of the timer is:  $T_{inc-source} * T0PSR * (T0PR + 1)$ .

Register 7-4 TMR0PWM – Timer0 PWM duty

Position	7	6	5	4	3	2	1	0
Name	TMR0PWM							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** TMR0PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting. In capture mode, the value of TMR0CNT will be captured to TMR0PWM when selected event occurs.

## 7.2 Timer1

Timer1 is a 16-bit timer/counter with a 7-bit prescaler. It can be configured as timer, counter or PWM generator.

### 7.2.1 Timer1 Features

- 16bits counter
- 7bits pre-scaler
- Counter mode (clock source from system clock or TMR1)
- Capture mode (event source from CAP1)
- PWM mode (PWM signal output to PWM1)

## 7.2.2 Timer1 Special Function Registers

Register 7-5 TMR1CON0 – Timer1 control 0

Position	7	6	5	4	3	2	1	0
Name	T1ES		T1M		T1CPSEL	T1IS		
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**T1ES:** Timer1 Capture Edge Select

00 = CAP1 Rising Edge

01 = CAP1 Falling Edge

1X= CAP1 Rising Edge and Falling Edge

**T1M:** Timer1 Mode Select

00 = Timer1 is disabled

01 = Timer1 is enabled and works in Counter Mode

10 = Timer1 is enabled and works in PWM Mode

11 = Timer1 is enabled and works in Capture Mode

**T1CPSEL:** Timer1 capture input pin select

0 = Capture CAP1

1 = Capture IR1

**T1IS:** Timer1 Increase Source

000 = TMR1 Rising Edge

001 = TMR1 Falling Edge

010 = TMR1 Rising and Falling Edge

011 = External 32 KHz crystal oscillator

1xx = System clock cycle

Register 7-6 TMR1CON1 – Timer1 control 1

Position	7	6	5	4	3	2	1	0
Name	T1TPND	T1CPND	T1TIE	T1CIE	-	T1PSR		
Default	0	0	0	0	-	0	0	0
Access	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

**T1TPND:** Timer1 over Flow Pending Bit

0 = Not Pending

1 = Pending

**T1CPND:** Timer1 Capture mode Pending Bit

0 = Not Pending

1 = Pending

**T1TIE:** Timer1 over Flow Interrupt Enable Bit

0 = Interrupt Disable

1 = Interrupt Enable

**T1CIE:** Timer1 Capture mode Interrupt Enable Bit

0 = Disable

1 = Enable

**T1PSR:** Timer1 Prescaler

000 = Timer1 counts at every counting source event

001 = Timer1 counts at every 2 counting source events

010 = Timer1 counts at every 4 counting source events

011 = Timer1 counts at every 8 counting source events

100 = Timer1 counts at every 16 counting source events

101 = Timer1 counts at every 32 counting source events

110 = Timer1 counts at every 64 counting source events

111 = Timer1 counts at every 128 counting source events

Register 7-7 TMR1CNTH/TMR1CNTL – Timer1 Counter

Position	7	6	5	4	3	2	1	0
Name	TMR1CNTH/TMR1CNTL							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** Timer1 will increase in proper condition while it is enable, it overflows when TMR1CNT = TMR1PR, TMR1CNT will be cleared to 0x0000 when overflow, and the interrupt flag will be set '1' by hardware.

Register 7-8 TMR1PRH/TMR1PRL – Timer1 Period

Position	7	6	5	4	3	2	1	0
Name	TMR1PRH/TMR1PRL							
Default	1	1	1	1	1	1	1	1
Access	WO	WO	WO	WO	WO	WO	WO	WO

The overflow period of the timer is: Tinc-source \* T1PSR \* (T1PR + 1).

Register 7-9 TMR1PWMH/TMR1PWML – Timer1 PWM duty

Position	7	6	5	4	3	2	1	0
Name	TMR1PWMH/TMR1PWML							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** TMR1PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting. In capture mode, the value of TMR1CNT will be captured to TMR1PWM when selected event occurs.

## 7.3 Timer2

Timer2 is a 16-bit timer/counter with a 7-bit prescaler. It can be configured as timer, counter or PWM generator.

## 7.3.1 Timer2 Features

- 16bits counter
- 7bits pre-scaler
- Counter mode (clock source from system clock or TMR2)
- Capture mode (event source from CAP2)
- PWM mode (PWM signal output to PWM2)

## 7.3.2 Timer2 Special Function Registers

Register 7-10 TMR2CON0 – Timer2 control 0

Position	7	6	5	4	3	2	1	0
Name	T2ES		T2M		Reserved	T2IS		
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**T2ES:** Timer2 Capture Edge Select

00 = CAP2 Rising Edge

01 = CAP2 Falling Edge

1X= CAP2 Rising Edge and Falling Edge

**T2M:** Timer2 Mode Select

00 = Timer2 is disabled

01 = Timer2 is enabled and works in Counter Mode

10 = Timer2 is enabled and works in PWM Mode

11 = Timer2 is enabled and works in Capture Mode

**T2IS:** Timer2 Increase Source

000 = TMR2 Rising Edge

001 = TMR2 Falling Edge

010 = TMR2 Rising and Falling Edge

011 = External 32 KHz crystal oscillator

1xx = System Clock cycle

Register 7-11 TMR2CON1 – Timer2 control 1

Position	7	6	5	4	3	2	1	0
Name	T2TPND	T2CPND	T2TIE	T2CIE	-	T2PSR		
Default	0	0	0	0	-	0	0	0
Access	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

**T2TPND:** Timer2 over Flow Pending Bit

0 = Not Pending

1 = Pending

**T2CPND:** Timer2 Capture mode Pending Bit

0 = Not Pending

1 = Pending

**T2TIE:** Timer2 over Flow Interrupt Enable Bit

0 = Interrupt Disable

1 = Interrupt Enable

**T2CIE:** Timer2 Capture mode Interrupt Enable Bit

0 = Disable

1 = Enable

**T2PSR:** Timer2 Prescaler

000 = Timer2 counts at every counting source event

001 = Timer2 counts at every 2 counting source events

010 = Timer2 counts at every 4 counting source events

011 = Timer2 counts at every 8 counting source events

100 = Timer2 counts at every 16 counting source events

101 = Timer2 counts at every 32 counting source events

110 = Timer2 counts at every 64 counting source events

111 = Timer2 counts at every 128 counting source events

Register 7-12 TMR2CNTH/TMR2CNTL – Timer2 Counter

Position	7	6	5	4	3	2	1	0
Name	TMR2CNTH/TMR2CNTL							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** Timer2 will increase in proper condition while it is enable, it overflows when TMR2CNT = TMR2PR, TMR2CNT will be clear to 0x0000 when overflow, and the interrupt flag will be set '1' by hardware.

Register 7-13 TMR2PRH/TMR2PRL – Timer2 Period

Position	7	6	5	4	3	2	1	0
Name	TMR2PRH/TMR2PRL							
Default	1	1	1	1	1	1	1	1
Access	WO	WO	WO	WO	WO	WO	WO	WO

The overflow period of the timer is:  $T_{inc-source} * T2PSR * (T2PR + 1)$ .

Register 7-14 TMR2PWMH/TMR2PWML – Timer2 PWM duty

Position	7	6	5	4	3	2	1	0
Name	TMR2PWMH/TMR2PWML							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** TMR2PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting. In capture mode, the value of TMR2CNT will be captured to TMR2PWM when selected event occurs.



## 7.4 Timer3

Timer3 is an 8-bit timer/counter with a 7-bit prescaler. It can be configured as timer, counter or PWM generator.

### 7.4.1 Timer3 Features

- 8bits counter
- 7bits pre-scaler
- Counter mode (clock source from system clock or TMR3)
- Capture mode (event source from CAP3)
- PWM mode (PWM signal output to PWM3)

### 7.4.2 Timer3 Special Function Registers

Register 7-15 TMR3CON – Timer3 control

Position	7	6	5	4	3	2	1	0
Name	T3PND	T3ES	T3M		T3IS	T3PSR		
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**T3PND:** Timer3 Pending Flag

0 = Not Pending

1 = Pending

**T3ES:** Timer3 Capture Mode Edge Select

0 = CAP3 Rising Edge

1 = CAP3 Falling Edge

**T3M:** Timer3 Mode

00 = Timer3 is disabled

01 = Timer3 is enabled and works in Counter Mode

10 = Timer3 is enabled and works in PWM Mode

11 = Timer3 is enabled and works in Capture Mode

**T3IS:** Timer3 Increase Source

0 = System Clock

1 = TMR3 rising edge

**T3PSR:** Timer3 Prescaler

000 = Timer3 counts at every counting source event

001 = Timer3 counts at every 2 counting source events

010 = Timer3 counts at every 4 counting source events

011 = Timer3 counts at every 8 counting source events

100 = Timer3 counts at every 16 counting source events

101 = Timer3 counts at every 32 counting source events

110 = Timer3 counts at every 64 counting source events

111 = Timer3 counts at every 128 counting source events

Register 7-16 TMR3CNT – Timer3 Counter

Position	7	6	5	4	3	2	1	0
Name	T3CNT							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** Timer3 will increase in proper condition while it is enabled. It overflows when TMR3CNT = TMR3PR, TMR3CNT will be clear to 0x00 when overflow occurs, and the interrupt flag will be set '1' by hardware.

Register 7-17 TMR3PR – Timer3 Period

Position	7	6	5	4	3	2	1	0
Name	TMR3PR							
Default	1	1	1	1	1	1	1	1
Access	WO	WO	WO	WO	WO	WO	WO	WO

**Note:** The overflow period of the timer is: Tinc-source \* T3PSR \* (T3PR + 1).

Register 7-18 TMR3PWM – Timer3 PWM duty

Position	7	6	5	4	3	2	1	0
Name	TMR3PWM							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Note:** TMR3PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting. In capture mode, the value of TMR3CNT will be captured to TMR3PWM when selected event occurs.

## 7.5 Watchdog Timer (WDT)

The Watchdog Timer (WDT) logic consists of a 20bit Watchdog Timer. The Watchdog Timer is clocked by internal RC oscillator running at 32 KHz. When device resets, the WDT is disabled and user should enable the WDT if it is needed.

In the default configuration, WDT overflows in 2ms. The application program needs to write a '1' into WDTCON [5] at least once 2 ms to prevent WDT time out. The lower 3 bits of the WDTCON register control the selection of overflow time period.

### 7.5.1 Watchdog Wake up

WDT can be used to wake up CW6680E/CW6681E/CW6682E from Idle, Hold or Sleep mode. RSTEN bit (WDTCON [3]) is used to determine the actions after WDT wake up. When RSTEN sets to 0, the watchdog will generate a non-reset wake up after counter overflows. And When RSTEN sets to 1, the watchdog will wake up CW6680E/CW6681E/CW6682E by resetting the whole chip. After non-reset wake up CW6680E/CW6681E/CW6682E will continue to execute next instruction.

- During Idle mode, CW6680E/CW6681E/CW6682E can be wake up by WDT with interrupt or reset.

- During Hold mode, CW6680E/CW6681E/CW6682E can be wakeup by WDT with interrupt or reset or just continue to execute the next instruction.
- During Sleep mode, CW6680E/CW6681E/CW6682E can be wakeup by WDT with reset.
- During Deep Sleep mode, CW6680E/CW6681E/CW6682E cannot be wakeup by WDT.

## 7.5.2 Watchdog SFR

Register 7-19 WDTCON – Watchdog control

Position	7	6	5	4	3	2	1	0
Name	WDTPD	WDTTO	CLRWDT	WDTEN	RSTEN	WDTPS		
Default	0	0	0	0	0	0	0	0
Access	RO	RO	WO	R/W	R/W	R/W	R/W	R/W

### WDTPD:

0 = read '0' before sleep operation

1 = read '1' after sleep operation

### WDTTO:

0 = Read '0' after clear Watchdog or Power up

1 = Read '1' after Watchdog time out

### CLRWDT:

1 = Clear WDT counter

0 = No action

### WDTEN:

0 = Disables the Watchdog timer

1 = Enables the Watchdog timer

### RSTEN:

0 = Disables the Watchdog reset

1 = Enables the Watchdog reset

### WDTPS: WDT time out period setting

000 = 2ms

001 = 8ms

010 = 32ms

011 = 128ms

100 = 512ms

101 = 2048ms

110 = 8192ms

111 = 32768ms

## 7.6 Independent Power Real Time Clock Counter (IRTCC)

### 7.6.1 IRTCC Controller

IRTCC control can generate two interrupts: interrupt every Second and interrupt with Alarm.

IRTCC second interrupt can be enabled by writing 1 to IRTIE bit. When IRTCC works and IRTIE = 1, IRTCC second interrupt will be generated every 1 second by setting I RTPND to 1. I RTPND can be cleared by software by writing 0 to I RTPND bit.

IRTCC alarm interrupt can be enabled by writing 1 to IRTALIE bit. When IRTCC works and IRTALIE = 1, IRTCC alarm interrupt will be generated when the current time is equal to the pre-set time by setting IRTALPND to 1. IRTALPND can be cleared by software by writing 0 to IRTALPND bit.

IRTCC is divided to two parts; one part is IRTCC control. The power of IRTCC control is VDDCORE. Another part is IRTCC. The part of IRTCC is VDDRTC. The communication between two parts is use like SPI protocol.

### 7.6.2 IRTCC Timer

IRTCC timer can be power independently. It can work even other logic in CW6680E/CW6681E/CW6682E is power off.

There is 6-bit valid address for the 64-byte user RAM. So the upper 2-bit of address in the writing RTC\_RAM or reading RTC\_RAM command are ignored. After one byte write/read, the internal address can increase automatically, this characteristic provide a burst mode to write/read the RAM. If the internal addresses increase greater than 63, it will roll back to 0.

### 7.6.3 Communication with IRTCC Timer

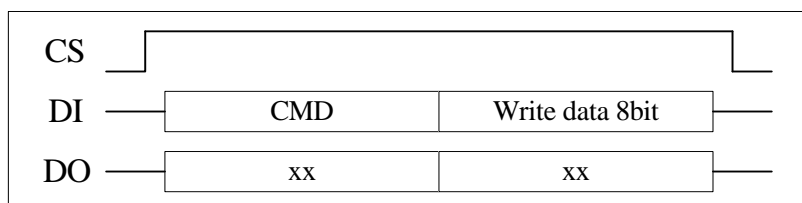
Special commands and corresponding parameters are used to communicate with IRTCC timer internal control or status registers and SRAM.

Table 7-1 IRTCC components communication commands

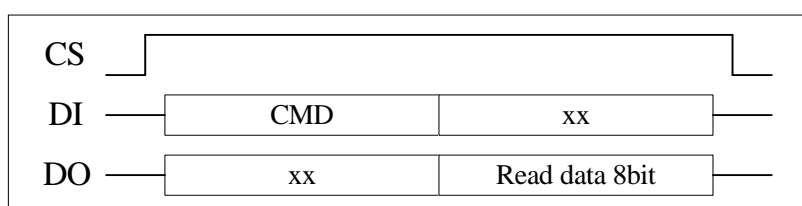
IRTCC component	Component type	Operation	Command Code	Command Parameters
RTCCFG	A	Write	0x55	One byte
		Read	0x54	One byte
PWRCTL	A	Write	0x59	One byte
		Read	0x58	One byte
WKEN	A	Write	0xa7	One byte
		Read	0xa6	One byte
WKSTA	A	Read	0xa1	One byte
RTCCNT	C	Write	0xf0	Five byte
		Read	0xe0	Five byte
RTCALM	D	Write	0x53	Three byte
		Read	0x52	Three byte
RTCRAM	E	Write	0x57	One byte address and N byte data
		Read	0x56	One byte address and N byte data

**Communication operations:****1, Read or write A type components**

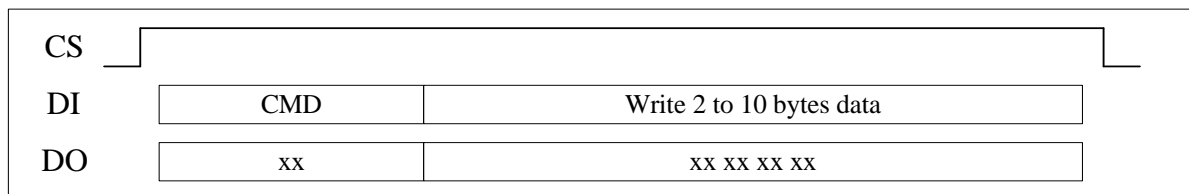
Write:



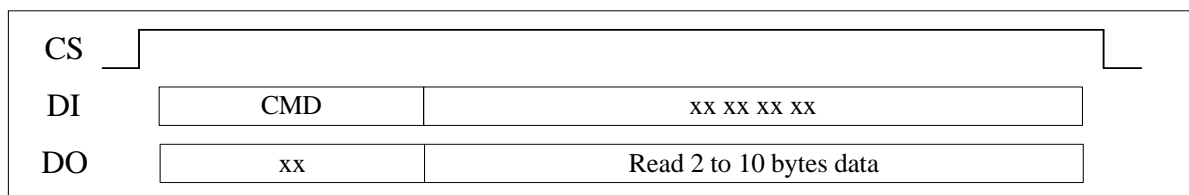
Read:

**2, Read or write B type components**

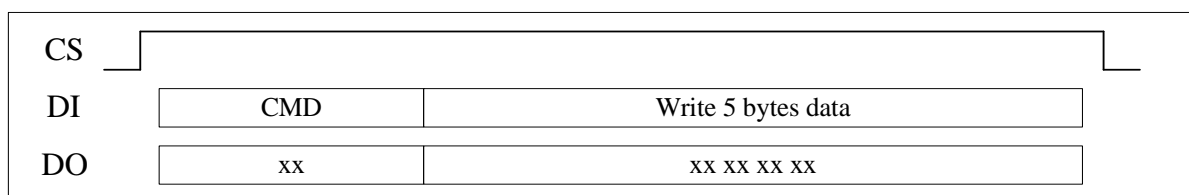
Write:



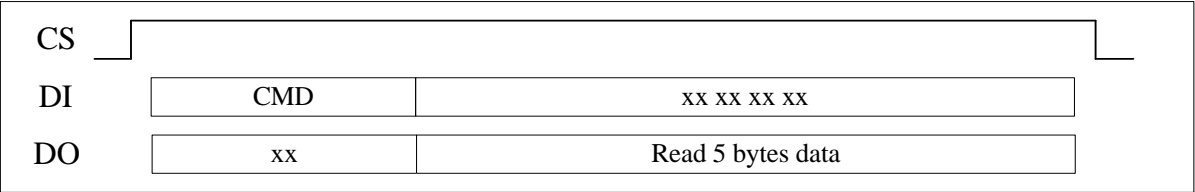
Read:

**3, Read or write C type components**

Write:

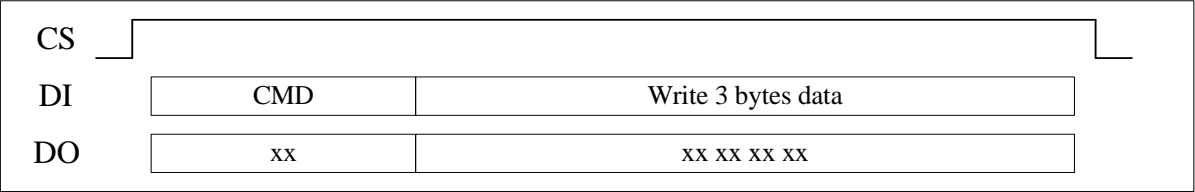


Read:

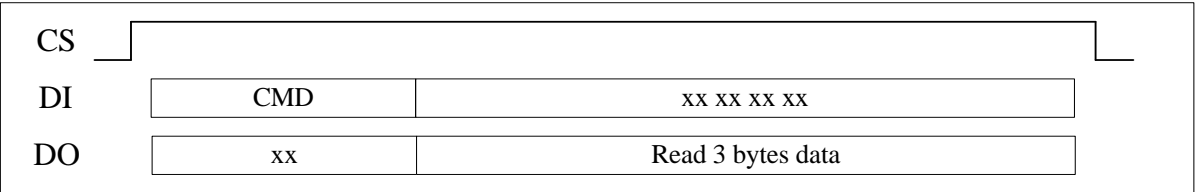


4, Read or write D type components

Write:

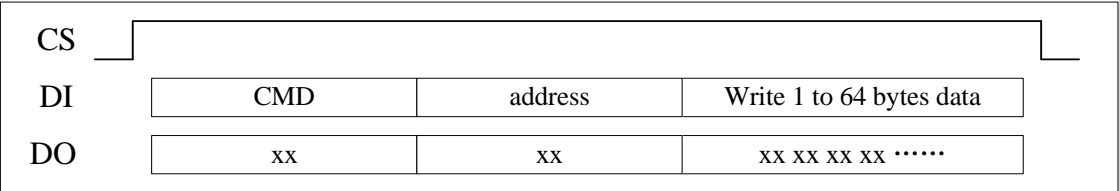


Read:

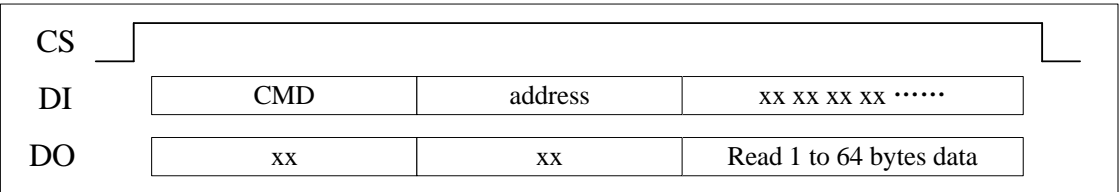


5, Read or write E type components

Write:



Read:



7.6.4 IRTCC components description

Register 7-20 RTCCFG - IRTCC configuration

Position	7	6	5	4	3	2	1	0
Name	X32KEN	X12MEN	XOPD_EN	WKPIN_STA	F1HZEN	-	EX32KSEL	reserved
Default	0	0	1	0	0	1	0	0

Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
--------	-----	-----	-----	-----	-----	-----	-----	-----

**X32KEN:** Oscillator for external 32KHz crystal resonator enable

0 = Disable

1 = Enable

**X12MEN:** Oscillator for external 12MHz crystal resonator enable

0 = Disable

1 = Enable

**XOPD\_EN:** OSC output PIN pull-down resistor enable

0 = Disable pull-down resistor

1 = Enable pull-down resistor

**WKPIN\_STA:** Force IRTWKO pin output state

0 = IRTWKO is controlled by IRTCC alarm function

1 = IRTWKO is forced to output 1

**F1HZEN:** 1Hz signal for core output enables

0 = Disabled

1 = Enabled

**EX32KSEL:** IRTCC clock source select

0 = IRTCC works with IRTOSC 32 KHz

1 = IRTCC works with XOSC 32K.

#### Register 7-21 PWRCON – Power control

Position	7	6	5	4	3	2	1	0
Name	LVD_EN	Reserved	Reserved	Reserved	Reserved	RCEN	Reserved	Reserved
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**LVD\_EN:** LVD enable

0 = Disabled

1 = Enabled

**RCEN:** Internal RC 12MHz oscillator enables

0 = Enabled

1 = Disabled

#### Register 7-22 WKEN - IRTCC wake up control

Position	7	6	5	4	3	2	1	0
Name	IOSEL	ALMOE	PDFLAG	DAY_WKEN	MIN_WKEN	IOWK_EN	WKO_EN	ALMEN
Default	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IOSEL:** Deep sleep mode and power down mode wakeup pin select

0 = Select P07

1 = Select P33

**ALMOE:** Alarm output at IRTWKO pin enable

0 = Disabled

1 = Enabled

**PDFLAG:** IRTCC timer power down flag

0 = IRTCC timer is working

1 = IRTCC timer is just power on

**DAY\_WKEN:** One day wakeup function enable

0 = One day wakeup function disabled

1 = One day wakeup function enabled

**MIN\_WKEN:** One minute wakeup function enable

0 = One minute wakeup function disabled

1 = One minute wakeup function enabled

**IOWK\_EN:** Deep sleep mode and power down mode wakeup by P33 or P07 function enable

0 = Disabled

1 = Enabled

**WKO\_EN:** IRTWKO pin wake up function enable

0 = Disabled

1 = Enabled

**ALMEN:** Alarm function enables

0 = Disabled

1 = Enabled

Register 7-23 WKSTA - IRTCC Status register

Position	7	6	5	4	3	2	1	0
Name	OSCO_STA	HVDR	PDFLAG	LVDPND	TMR_PND	IOWK_PND	WKO_PND	ALMOT
Default	0	0	1	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

**OSCO\_STA:** OSCO PIN status

0 = reserved

1 = High state means Normal mode

**HVDR:** HVD flag

0 = VDDLDO is not higher than 4V

1 = VDDLDO is higher than 4V

**PDFLAG:** RTCC timer power down flag

0 = RTCC timer is working

1 = RTCC timer is just power on

**LVDPND:** LVD pending

0 = VDDLDO is higher than 2V

1 = VDDLDO is lower than 2V

**TMR\_PND:** RTC each minute or date wake up pending



0 = No wake up

1 = Minute or date wake up pending

**IOWK\_PND**: P33 or P07 pin wake up pending

0 = No wake up

1 = P33 or P07 pin wake up pending

**WKO\_PND**: IRTWKO pin wake up pending

0 = No wake up

1 = IRTWKO pin wake up pending

**ALMOT**: Alarm match flag.

0 = No alarm match happen

1 = Alarm match

Register 7-24 RTCCNT4 - IRTCC counter byte 4

Position	7	6	5	4	3	2	1	0
Name	RTCCNT byte 4							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 7-25 RTCCNT3 - IRTCC counter byte 3

Position	7	6	5	4	3	2	1	0
Name	RTCCNT byte 3							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

{RTCCNT4, RTCCNT3} is the day counter

Register 7-26 RTCCNT2 - IRTCC counter byte 2

Position	7	6	5	4	3	2	1	0
Name	-	-	RTCCNT byte 2					
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCCNT2 is the hour counter; this is BCD code

Register 7-27 RTCCNT1 - IRTCC counter byte 1

Position	7	6	5	4	3	2	1	0
Name	-	RTCCNT byte 1						
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCCNT1 is the minute counter; this is BCD code

Register 7-28 RTCCNT0 - IRTCC counter byte 0

Position	7	6	5	4	3	2	1	0
Name	-	RTCCNT byte 0						

Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCCNT0 is the secode counter; this is BCD code

**NOTE:** When use “Write RTCCNT” command to configure this RTC counter, the first parameter byte is for RTCCNT4, and the following parameter bytes are for RTCCNT3/2/1/0. When use “Read RTCCNT” command to read this counter, the first byte output is RTCCNT4 and the following output is RTCCNT3/2/1/0.

Register 7-29 RTCALM2 - IRTCC alarm hour byte

Position	7	6	5	4	3	2	1	0
Name	-	-	RTCALM hour byte					
Default	x	x	X	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCALM2 is the hour alarm; this is BCD code

Register 7-30 RTCALM1 - IRTCC alarm minute byte

Position	7	6	5	4	3	2	1	0
Name	-	RTCALM minute byte						
Default	x	X	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCALM1 is the minute alarm; this is BCD code

Register 7-31 RTCALM0 - IRTCC alarm second byte

Position	7	6	5	4	3	2	1	0
Name	-	RTCALM second byte						
Default	x	X	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

RTCALM0 is the second alarm; this is BCD code

**NOTE:** When use “Write RTCALM” command to configure alarm, the first parameter byte is for RTCALM2 and the following are for RTCALM1/0. When use “Read RTCALM” command to read alarm, the first byte output is RTCALM2 and the following is RTCALM1/0.

## 7.6.5 IRTCC Special Function Registers

Register 7-32 RTCON – RTCC control

Position	7	6	5	4	3	2	1	0
Name	IRTRSTEN	RD_RTC	IRTALPND	IRTALIE	IRTPND	IRTIE	DONE	EN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**IRTRSTEN:** IRTCC second reset enable

0 = Disabled

1 = Enabled

**RD\_RTC:** Read IRTCC counter enable

0 = Disable Read IRTCC counter function

1 = Enable Read IRTCC counter function

**IRTALPND:** IRTCC alarm pending

0 = No pending (Write 0 to clear pending)

1 = Pending

**IRTALIE:** IRTCC alarm interrupt enable

0 = Disable

1 = Enable

**NOTE:** IRTALIE must be '1' if IRTCC alarm is used to wake up system.

**IRTPND:** IRTCC second pending

0 = No pending (Write 0 to clear pending)

1 = Pending

**IRTIE:** IRTCC second interrupt enable

0 = Disable

1 = Enable

**NOTE:** IRTIE must be '1' if IRTCC second is used to wake up system.

**DONE:** Communication done flag

0 = Done

1 = Not done

**EN:** IRTCC communications enable

0 = Disable

1 = Enable

Register 7-33 RTCDAT – RTCC communication data

Position	7	6	5	4	3	2	1	0
Name	RTCDAT							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Write to RTCDAT will start IRTCC communication and set DONE flag to 1.

Read RTCDAT will return IRTCC data.

Register 7-34 SECCNT – IRTCC second counter

Position	7	6	5	4	3	2	1	0
Name	SECCNT							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

IRTCC second counter

Register 7-35 RTCON1 – IRTCC control1

Position	7	6	5	4	3	2	1	0
Name	WKO_STA	RTC_POR	Reserved	Reserved	BAUD_SEL		SECPND	SECIE
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W

**WKO\_STA:** IRTWKO pin status

0 = IRTWKO pin is low

1 = IRTWKO pin is high

**RTC\_POR:** IRTCC POR status

0 = IRTCC power is low, still in reset status

1 = IRTCC power is high, can work normally

**BAUD\_SEL:** IRTCC communication baud rate selection

00 = every 2 system clock cycles

01 = every 4 system clock cycles

1x = every 1 system clock cycle

**SECPND:** Second pending

0 = No pending (Write 0 to clear pending)

1 = When SECCNT equal to internal counter

**SECIE:** Second pending interrupt enable

0 = Disabled

1 = Enabled

## 7.6.6 IRTCC Operating Guide

### 1. Write Data to register

- 1) Enable CS (RTCON.0)
- 2) Write command to RTCDAT register
- 3) Wait for transmission done (RTCON.1)
- 4) Write data to RTCDAT register
- 5) Wait for transmission done (RTCON.1); If send more than one data, please repeat steps 4 and 5
- 6) Disable CS (RTCON.0)

### 2. Read Data from register

- 1) Enable CS (RTCON.0)
- 2) Write command to RTCDAT register
- 3) Wait for transmission done (RTCON.1)
- 4) Write "0x00" to RTCDAT register
- 5) Wait for transmission done (RTCON.1)
- 6) Read data from RTCDAT; If read more than one data, please repeat steps 4, 5 and 6
- 7) Disable CS (RTCON.0)

**For Example:**

Send\_Dat\_PND macro

```
MOV    A, RTCON
JB     ACC.1, $-2
```

endm

-----

; Write RTC Config

Write\_Cfg:

```
ORL     RTCON, # (1<<0)      ; RTC enable steps 1
MOV     RTCDAT, #55H         ; steps 2
Send_Dat_PND                      ; steps 3
MOV     RTCDAT, #0CDH        ; steps 4
Send_Dat_PND                      ; steps 5
ANL     RTCON, #~ (1<<0)     ; RTC Disable steps 6
RET
```

-----

; Read Config

Read\_Cfg:

```
ORL     RTCON, # (1<<0)      ; RTC enable steps 1
MOV     RTCDAT, #54H         ; steps 2
Send_Dat_PND                      ; steps 3
MOV     RTCDAT, #00H        ; steps 4
Send_Dat_PND                      ; steps 5
MOV     A, RTCDAT           ; steps 6
ANL     RTCON, #~ (1<<0)     ; RTC Disable steps 7
RET
```

## 8 Universal Asynchronous Receiver/Transmitter (UART)

### 8.1 UART0

#### 8.1.1 Overview

UART0 is a serial port capable of asynchronous transmission. The UART0 can function in full duplex mode. Receive data is buffered in a holding register. This allows the UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

When PSEL = 0

- Receive pin (RX) – UART0RX0 (P34)
- Transmit pin (TX) – UART0TX0 (P16)

When PSEL = 1

- Receive pin (RX) – UART0RX1 (P00)
- Transmit pin (TX) – UART0TX1 (P01)

#### 8.1.2 UART0 Special Function Registers

Register 8-1 UARTCON – UART0 control

Position	7	6	5	4	3	2	1	0
Name	UTSBS	UTTXNB	NBITEN	UTEN	UTTXINV	UTRXINV	TXIE	RXIE
Default	0	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**UTSBS:** Stop Bit Select

0 = 1 bit as Stop Bit

1 = 2 bits as Stop Bit

**UTTXNB:** The ninth bit data of transmitter buffer. Write the ninth bit into this location that you want to transmit

**NBITEN:** Nine-BIT mode Enable Bit

0 = Eight-bit mode

1 = Nine-bit mode

**UTEN:** UART Enable Bit

0 = Disable UART module

1 = Enable UART module

**UTTXINV:** Transmit Invert Selection Bit

0 = Transmitter output without inverted

1 = Transmitter output inverted

**UTRXINV:** Receive Invert Selection Bit

0 = Receiver input without inverted

1 = Receiver input inverted

**TXIE:** Transmit Interrupt Enable

0 = Transmit interrupt disable

1 = Transmit interrupt enable

**RXIE:** Receive Interrupt Enable

0 = Receiver interrupt disable

1 = Receiver interrupt enable

Register 8-2 UARTSTA – UART0 status

Position	7	6	5	4	3	2	1	0
Name	UTRXNB	FEF	RXIF	TXIF	-	-	-	PSEL
Default	x	x	0	1	-	-	-	0
Access	R/W	R/W	R/W	RO	-	-	-	R/W

**UTRXNB:** The ninth bit data of receiver buffer

**FEF:** Frame Error Flag

0 = the stop bit is '1' in the last received frame

1 = the stop bit is '0' in the last received frame

**RXIF:** RX Interrupt Flag

0 = RX not done

1 = RX done

**TXIF:** TX Interrupt Flag

0 = TX not done

1 = TX done

Writing data to UTBUF will clear this flag.

**PSEL:** UART0 Port Select

0 = Select UART0RX0 and UART0TX0

1 = Select UART0RX1 and UART0TX1

Register 8-3 UARTBAUDL – UART0 Baud Rate Low Byte

Position	7	6	5	4	3	2	1	0
Name	UARTBAUDL							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Register 8-4 UARTBAUDH – UART0 Baud Rate High Byte

Position	7	6	5	4	3	2	1	0
Name	UARTBAUDH							
Default	0	0	0	0	0	0	0	0

Access	WO	WO	WO	WO	WO	WO	WO	WO
--------	----	----	----	----	----	----	----	----

UARTBAUD = {UARTBAUDH, UARTBAUDL}

Baud Rate =  $F_{\text{sys clock}} / [8(\text{UARTBAUD} + 1)]$

Register 8-5 UARTDATA – UART0 Data

Position	7	6	5	4	3	2	1	0
Name	UARTDATA							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Write this location will load the data to transmitter buffer. And read this location will read the data from the receiver buffer.

## 8.2 UART1

### 8.2.1 Overview

UART1 is a serial port capable of asynchronous transmission. The UART1 can function in normal and DMA full duplex mode. Please see PMUXCON0 bit 6 descriptions

- Receive pin (RX) – UART1RX0 (P37)
- Transmit pin (TX) – UART1TX0 (P36)

Or

- Receive pin (RX) – UART1RX1 (P17)
- Transmit pin (TX) – UART1TX1 (P16)

### 8.2.2 UART1 Special Function Registers

Register 8-6 UART1CON – UART1 control

Position	7	6	5	4	3	2	1	0
Name	UTSBS	UTTXNB	NBITEN	UTEN	TXIE	RXIE	RXAUIE	DMASEL
Default	0	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**UTSBS:** Stop Bit Select

0 = 1 bit as Stop Bit

1 = 2 bits as Stop Bit

**UTTXNB:** The ninth bit data of transmitter buffer. Write the ninth bit into this location that you want to transmit

**NBITEN:** Nine-BIT mode Enable Bit

0 = Eight-bit mode

1 = Nine-bit mode



**UTEN:** UART Enable Bit

0 = Disable UART module

1 = Enable UART module

**TXIE:** Transmit Interrupt Enable

0 = Transmit interrupt disable

1 = Transmit interrupt enable

**RXIE:** Receive Interrupt Enable

0 = Normal Receive interrupt disable or AUTO DMA mode Receive one word Interrupt disable

1 = Normal Receive interrupt enable or AUTO DMA mode Receive one word Interrupt enable

**RXAUIE:** Receive AUTO DMA mode 256 bytes interrupt enable

0 = AUTO DMA mode Receive 256 bytes Interrupt disable

1 = AUTO DMA mode Receive 256 bytes Interrupt enable

**DMASEL:** AUTO DMA choose

0 = AUTO DMA mode off

1 = AUTO DMA mode on

## Register 8-7 UART1STA – UART1 status

Position	7	6	5	4	3	2	1	0
Name	-	-	UTRXNB	RX_BYTE_HIGH	RXIF	TXIF	RXDMAIF	AUTOERR
Default	0	0	x	0	0	1	0	0
Access	-	-	R/W	RO	R/W	RO	R/W	RO

**UTRXNB:** The ninth bit data of receiver buffer**RX\_BYTE\_HIGH:** receive data high byte (only for DMA)

0 = waiting receive data low byte

1 = waiting receive data high byte

**RXIF:** UART RX Interrupt Flag

0 = Normal Receive or AUTO DMA mode Receive one word not done

1 = Normal Receive or AUTO DMA mode Receive one word done

In normal mode, it become “1” every byte, but in DMA mode, it become “1” every word.

**TXIF:** UART TX Interrupt Flag

0 = UART transmit not done

1 = UART transmit done

Writing data to UTBUF or Writing UARTDMATXCNT will clear this flag.

**RXDMAIF:** AUTO DMA mode Receive 256 bytes interrupt Flag

0 = UART AUTO DMA receive 256 bytes not done

1 = UART AUTO DMA receive 256 bytes done

**AUTOERR:** UART AUTO DMA receive overflow error Flag

0 = UART AUTO DMA receive not overflow

1 = UART AUTO DMA receive overflow

When the first 256 bytes of UART receiver already have not read and the second 256 bytes data are also already

received , AUTOERR Flag will be '1'.

Register 8-8 UARTDIV – UART1 baud rate high

Position	7	6	5	4	3	2	1	0
Name	UARTDIV							
Default	0	0	0	0	0	0	0	0
Access	-	-	-	-	WO	WO	WO	WO

Register 8-9 UART1BAUD – UART1 baud rate low

Position	7	6	5	4	3	2	1	0
Name	UARTBAUD							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

$$\text{Baud Rate} = F_{\text{sys clock}} / [(UARTDIV + 1) \times (UART1BAUD + 1)]$$

Register 8-10 UART1DATA – UART1 Data buffer

Position	7	6	5	4	3	2	1	0
Name	UART1DATA							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Write this location will load the data to transmitter buffer. And read this location will read the data from the receiver buffer.

Register 8-11 UARTDMATXCNT –UART DMA Transmit counter

Portion	7	6	5	4	3	2	1	0
Name	UARTDMATXCNT							
Default	x	x	x	x	x	x	X	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$$N_{\text{unit}} = \text{UARTDMATXCNT} + 1$$

$$N_{\text{byte}} = N_{\text{unit}} * 2 = (\text{UARTDMATXCNT} + 1) * 2$$

Register 8-12 UARTDMATXPTR–UART DMA Transmit Start Pointer byte

Portion	7	6	5	4	3	2	1	0
Name	UARTDMATXPTR							
Default	x	x	x	x	x	x	x	x
Access	W	W	W	W	W	W	W	W

In order to get the correct DMA Start Pointer, you should write this register twice. First write the higher byte, then the low byte.

Register 8-13 UARTDMARXPTR–UART DMA receive Start Pointer byte

Portion	7	6	5	4	3	2	1	0
Name	UARTDMARXPTR							
Default	x	x	x	x	x	x	x	x

Access	W	W	W	W	W	W	W	W
--------	---	---	---	---	---	---	---	---

In order to get the correct DMA Start Pointer, you should only write this register only one. It is high 8 bits of address. But the "0" bit will be neglected

## 8.2.3 UART1 Operation Guide

### UART1 Normal mode Operation Flow:

1. Set IO in the correct direction.
2. Configure UARTDIV and UART1BAUD to choose sample rate and baud.
3. Enable UART1 by setting UTEN to '1'
4. Set TXIE or RXIE 'to 1' if needed
5. write data to UART1DATA
6. Wait for PND to change to '1', or wait for interrupt
7. Read received data from UART1DATA if needed
8. Go to Step 5 to start another process if needed or turn off UART1 by UTEN.

### UART1 DMA M0ode Operation Flow:

1. Set IO in the correct direction.
2. Configure UARTDIV and UART1BAUD to choose sample rate and baud.

Configure UART1CON Select DMA.

Enable UART1 by setting UTEN to '1'.

Set TXIE ,RXAUIE or RXIE 'to 1' if needed

According to Step 3, write the start DMA address. For receive, write data to UARTDMARXPTR to kick-start a DMA receive process

Write data to UARTDMATXCNT to kick-start a DMA transmit process

Wait for PND to change to '1', or wait for interrupt

Go to Step 5 or 6 to start another DMA process if needed or turn off UART1 by clearing TXIE or TXIE and UTEN

## 9 SPI

### 9.1 SPI0

SPI0 can serve as master or slave. It can operate in normal or DMA mode.

SPI0 map to three group ports, one is P27, P25, P26, the other is P04, P06, P05, another is P14, P00, and P34. This is configured by SPI0PS1 and SPI0PS0.

**When PWKEDGE.6=0, SPI0CON.3 = 0, it uses 2 pins for 2-wire mode: P2.7, P2.6**

1. Serial Data (SPI0DIDO0) – P2.7
2. Serial Clock (SPI0CLK0) – P2.6

**Or 3 pins for 3-wire mode: P2.7, P2.5, P2.6**

- Serial Data Out (SPI0DO0) – P2.7
- Serial Data In (SPI0DI0) – P2.5
- Serial Clock (SPI0CLK0) – P2.6

**When PWKEDGE.6=0, SPI0CON.3 = 1, it uses 2 pins for 2-wire mode: P0.4, P0.5**

- Serial Data (SPI0DIDO1) – P0.4
- Serial Clock (SPI0CLK1) – P0.5

**Or 3 pins for 3-wire mode: P0.4, P0.6, P0.5**

- Serial Data Out (SPI0DO1) – P0.4
- Serial Data In (SPI0DI1) – P0.6
- Serial Clock (SPI0CLK1) – P0.5

**When PWKEDGE.6=1, SPI0CON.3 = 0, it uses 2 pins for 2-wire mode: P1.4, P3.4**

- Serial Data (SPI0DIDO2) – P1.4
- Serial Clock (SPI0CLK2) – P3.4

**Or 3 pins for 3-wire mode: P1.4, P0.0, P3.4**

- Serial Data Out (SPI0DO2) – P1.4
- Serial Data In (SPI0DI2) – P0.0
- Serial Clock (SPI0CLK2) – P3.4

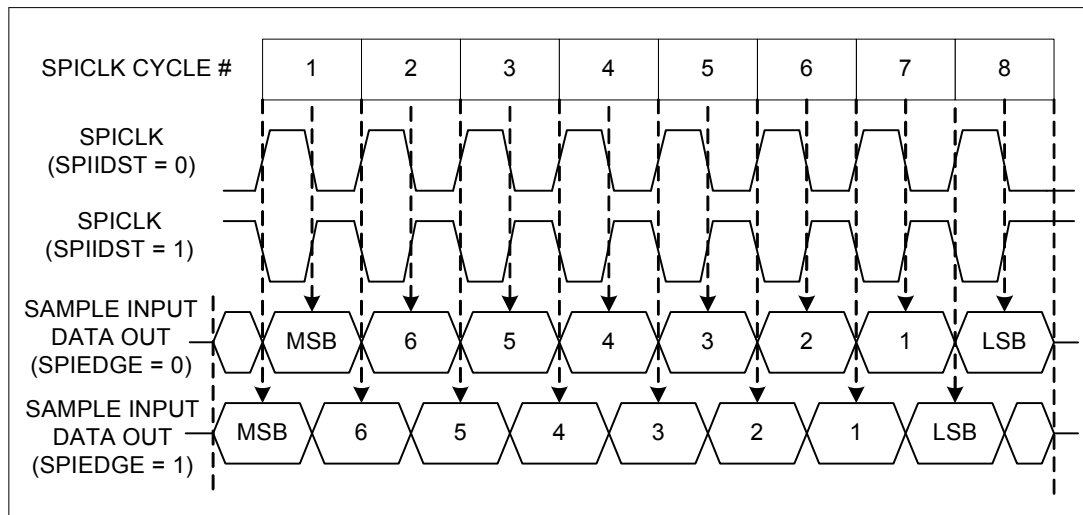


Figure 9-1 SPI timing

### 9.1.1 SPI0 Special Function Registers

Register 9-1 SPI0CON – SPI0 control

Position	7	6	5	4	3	2	1	0
Name	SPI0PND	SPI0SM	SPI0RT	SPI0WS	SPI0PS0	SPI0EDGE	SPI0IDST	SPI0EN
Default	1	0	0	0	0	0	0	0
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**SPI0PND:** SPI0 Pending bit (read only, writing SPI0BUF will clear this bit)

0 = Transmission is not finish

1 = Transmission finish

**SPI0SM:** SPI0 mode selection

0 = Master mode

1 = Slave mode

**SPI0RT:** SPI0 RX/TX select bit in 2-wire mode or DMA mode

0 = TX

1 = RX

In 3-wire mode, SPI0 can both Transmit and receive at the same time. But when using DMA mode or 2-wire mode, just one direction (TX or RX) is allowed. Use this bit to select TX or RX.

**SPI0WS:** SPI0 2-wire mode/3-wire mode select bit

0 = 3-wire mode

1 = 2-wire mode

**SPI0PS0:** SPI0 Port select 0

0 = Select P27, P25, P26 when SPI0PS1 = 0; Select P14, P00, P34 when SPI0PS1 = 1

1 = Select P04, P06, P05 when SPI0PS1 = 0

**SPI0EDGE:** SPI0 sampling edge select bit

When SPI0IDST = 0:

0 = Sample at falling edge

1 = Sample at rising edge

When SPI0IDST = 1:

0 = Sample at rising edge

1 = Sample at falling edge

**SPI0IDST:** SPI0 clock signal idle state

0 = Clock signal stay at 0 when idle

1 = Clock signal stay at 1 when idle

**SPI0EN:** SPI0 enable bit

0 = SPI0 disable

1 = SPI0 enable

Register 9-2 SPI0BAUD – SPI0 Baud Rate

Position	7	6	5	4	3	2	1	0
Name	SPI0BAUD							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Baud rate =  $F_{\text{system\_clock}} / [2(\text{SPI0BAUD}+1)]$

Register 9-3 SPI0BUF – SPI0 Data Buffer

Position	7	6	5	4	3	2	1	0
Name	SPI0BUF							
Default	x	x	x	x	x	x	x	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 9-4 SPI0DMACNT – SPI0 DMA counter

Position	7	6	5	4	3	2	1	0
Name	SPI0DMACNT							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Nunit = SPI0DMACNT + 1

Nbyte = Nunit \* 2 = (SPI0DMACNT + 1) \* 2

Register 9-5 SPI0DMAPTRH– SPI0 DMA Start Pointer high byte

Position	7	6	5	4	3	2	1	0
Name	SPI0DMAPTRH							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Register 9-6 SPI0DMAPTRL– SPI0 DMA Start Pointer low byte

Position	7	6	5	4	3	2	1	0
Name	SPI0DMAPTRL							

Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

## 9.1.2 SPI0 Operation Guide

When SPI0CON1.1=0,

### SPI0 Normal Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPI0RT in 2-wire mode if 2-wire mode is selected
3. Select master mode or slave mode
4. Configure clock frequency when master mode is selected in step 3
5. Select one of the four timing mode (refer to [Figure 9-1](#))
6. Enable SPI0 module by setting SPI0EN '1'
7. Set SPI0IE '1' if needed
8. Write data to SPI0BUF to kick-start the process
9. Wait for SPI0PND to change to '1', or wait for interrupt
10. Read received data from SPI0BUF if needed
11. Go to Step 8 to start another process if needed or turn off SPI0 by clearing SPI0IE and SPI0EN

### SPI0 DMA Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPI0RT for DMA direction
3. Select master mode or slave mode
4. Configure clock frequency when master mode is selected in step 3
5. Select one of the four timing modes (refer to [Figure 9-1](#))
6. Enable SPI0 module by setting SPI0EN to '1'
7. Set SPI0IE '1' if needed
8. Write the start address to SPI0DMASP
9. Write data to SPI0DMACNT to kick-start a DMA process
10. Wait for SPI0PND to change to '1', or wait for interrupt
11. Go to Step 8 to start another DMA process if needed or turn off SPI0 by clearing SPI0IE and SPI0EN

## 9.2 SPI1

CW6680E/CW6681E/CW6682E SPI1 is an accelerated SPI. It can serve as master only. It can operate in normal or DMA mode. Please see PMUXCON0 bit 5 descriptions

### SPI1 uses 2 pins for 2 wire mode:

When SPI1\_MAP = 0,

- Serial Data (SPIDIDO1) - P04

- Serial Clock (SPICLK1) - P05

When SPI1\_MAP = 1,

- Serial Data (SPIDIDO0) - P32
- Serial Clock (SPICLK0) - P30

#### **SPI1 uses 3 pins for 3 wire mode:**

When SPI1\_MAP = 0,

- Serial Data Out (SPIDO1) - P04
- Serial Data In (SPIDI1) - P06
- Serial Clock (SPICLK1) - P05

When SPI1\_MAP = 1,

- Serial Data Out (SPIDO0) - P32
- Serial Data In (SPIDI0) - P31
- Serial Clock (SPICLK0) - P30

## **9.2.1 SPI1 Special Function Registers**

Register 9-7 SPI1CON – SPI1 Configure Register

Position	7	6	5	4	3	2	1	0
Name	SPI1PND	DMAERR	SPI1RT	SPI1WS	SPI1DEC	SPI1SPS		SPI1EN
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**SPI1PND:** SPI1 Pending bit (read only, writing SPI1BUF will clear this bit)

0 = Transmission has not finished

1 = Transmission finish

**DMAERR:** SPI1 DMA Error flag

0 = No DMA error

1 = DMA error happened.

**SPI1RT:** SPI1 RX/TX select bit in 2-wire or DMA mode

0 = TX

1 = RX

In 3-wire mode, SPI1 can both Transmit and receive at the same time. But if we use DMA mode or 2-wire mode, just one direction (TX or RX) is allowed. Use this bit to select TX or RX.

**SPI1WS:** SPI1 2-wire mode/3-wire mode select bit

0 = 3-wire mode

1 = 2-wire mode

**SPI1DEC:** SPI1 decryption function enables

0 = Disabled

1 = Enabled

**SPI1SPS:** SPI1 Speed Select:



00 = Low speed. Bit clock frequency = system clock frequency /4

01 = Low speed. Bit clock frequency = system clock frequency /2

1x = High speed. Bit clock frequency = system clock frequency /1

**SPI1EN:** SPI1 enable bit

0 = SPI1 disabled

1 = SPI1 enabled

Register 9-8 SPI1CON1 – SPI1 Configure Register1

Position	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	CRCEN	ENCRYPT
Default	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R/W	R/W

**CRCEN:** SPI1 CRC enable when SPI1 receiving data

0 = Disabled

1 = Enabled

**ENCRYPT:** SPI1 output encryption function enable

0 = Disabled

1 = Enabled

**NOTE:** *ENCRYPT and SPI1DEC cannot be 1 at the same time.*

Register 9-9 SPI1BUF – SPI1 Data Buffer

Position	7	6	5	4	3	2	1	0
Name	SPI1BUF							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Write this location to load the data to transmitter buffer and kick start the SPI transmission, read this location will read the data from the receiver buffer.

Register 9-10 SPI1DMASPH– SPI1 DMA Pointer

Position	7	6	5	4	3	2	1	0
Name	-	-	SPI1DMASPH					
Default	0	0	x	x	x	x	x	x
Access	-	-	WO	WO	WO	WO	WO	WO

SPI DMA start address pointer, point to the start address in IRAM that the data to be transmitted or data to be stored.

Register 9-11 SPI1DMASPL– SPI1 DMA Pointer

Position	7	6	5	4	3	2	1	0
Name	SPI1DMASPL							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Register 9-12 SPI1DMACNT – SPI1 DMA Counter

Position	7	6	5	4	3	2	1	0
Name	SPI1DMACNT							
Default	X	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

SPI DMA counter, decide the amount of units to be transmitted or received. There is 2 bytes in a unit.

And there is a formula as follow:

$Nunit = SPIDMACNT + 1$

$Nbyte = Nunit * 2 = (SPIDMACNT + 1) * 2$

Write this location will enable DMA and kick start a DMA process .Caution: do not write 0 to this register.

## 9.2.2 SPI1 Operation Guide

### A. SPI Normal Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPI1WS in 2-wire mode or 3 wire mode.
3. Select SPI1RT for reception or transmission.
4. Configure clock frequency using bit SPI1SP.
5. Enable SPI module by setting SPI1EN '1'
6. Set SPI1IE '1' if needed
7. Write data to SPI1BUF to kick-start the process
8. Wait for SPI1PND change to '1', or wait for interrupt
9. Read received data from SPI1BUF if needed
10. Go to Step 7 to start another process if needed or turn off SPI1 by clearing SPI1PND and SPI1EN

### B. SPI DMA Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPI1RT for DMA direction
3. Select SPI1WS in 2-wire mode or 3 wire mode
4. Configure clock frequency using bit SPI1SP
5. Enable SPI module by setting SPI1EN '1'
6. Set SPI1IE '1' if needed
7. Write the start address to SPI1DMASP
8. Write data to SPI1DMACNT to kick-start the DMA process.
9. Wait for bit SPI1PND to change to '1', or wait for interrupt
10. Go to Step 7 to start another DMA process if needed or turn off SPI by clearing SPI1PND and SPI1EN

## 10 External Memory Interface (EMI)

CW6680E/CW6681E/CW6682E provides External Memory Interface (EMI) to accelerate data transfer. [Figure 10-1](#) shows EMI timing.

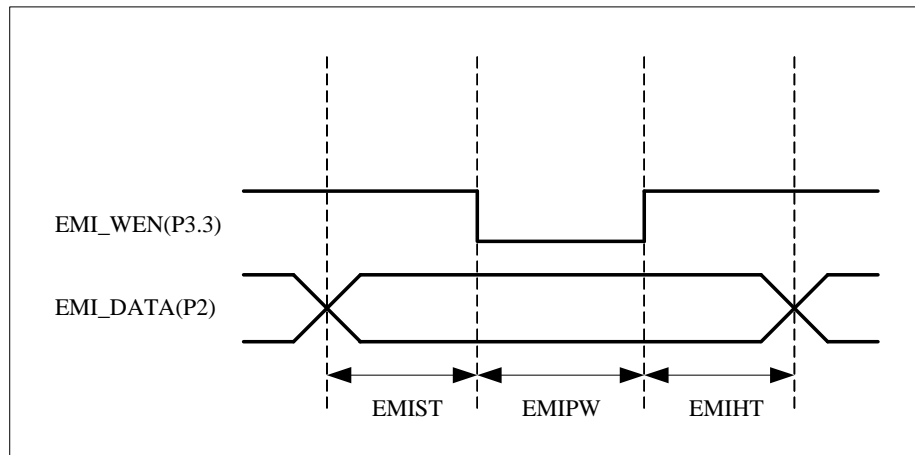


Figure 10-1 EMI timing

### 10.1 EMI Control Registers

Register 10-1 EMICON0 – EMI control0

Position	7	6	5	4	3	2	1	0
Name	EMIEN	EMIPW			EMIHT		EMIST	
Default	1	0	0	0	0	0	0	0
Access	WO	WO	WO	WO	WO	WO	WO	WO

#### EMIEN:

When writing: EMI Enable

0 = Disable

1 = Enable

#### EMIPW: EMI pulse width

000 = 1 system clock cycle

001 = 2 system clock cycles

010 = 3 system clock cycles

011 = 4 system clock cycles

100 = 5 system clock cycles

101 = 6 system clock cycles

110 = 7 system clock cycles

111 = 8 system clock cycles

#### EMIHT: EMI hold time

00 = 1 system clock cycle

01 = 2 system clock cycles

10 = 3 system clock cycles

11 = 4 system clock cycles

**EMIST:** EMI setup time

00 = 1 system clock cycle

01 = 2 system clock cycles

10 = 3 system clock cycles

11 = 4 system clock cycles

Register 10-2 EMICON1 – EMI control1

Position	7	6	5	4	3	2	1	0
Name	EMIPND	CLKSEL	OUTSEL	PWMEN	EMIDMAB		EMIDMAM	EMIM
Default	1	0	0	0	0	0	0	0
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**EMIPND:** When Read EMI done flag

0 = EMI is transmitting data

1 = EMI is IDLE

When Write “0”, clear write buffer counter; write “1” affect another

**CLKSEL:** PWM module work clock select

0 = 24MHz

1 = 48MHz

**OUTSEL:** PWM output select

0 = LED anode display

1 = LED cathode display

**PWMEN:** PWM enable

0 = Disable

1 = Enable

**EMIDMAB:** EMI DMA converts byte select

00 = reserved

01 = 1 byte

10 = 2 byte

11 = 3 byte

**EMIDMAM:** EMI DMA mode

0 = no convert

1 = bit convert to byte

**EMIM:** EMI mode

0 = work when CPU kick start

1 = work with SPI1 DMA

Register 10-3 EMIBUF – EMI output buffer

Position	7	6	5	4	3	2	1	0
Name	EMIBUF							

Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

EMIBUF is the entrance of 6 bytes EMI output buffer. The 6 bytes EMI output buffer is emibuf0, emibuf1, emibuf2, emibuf3, emibuf4 and emibuf5. When CPU writes to EMIBUF, internal counter will add "1", CPU data is pushed corresponding buffer. You should clear internal counter by writing "0" to emicon1 bit 7;

PWM mode: should write eight times for eight channels PWM of P2

When EMIM = 0, emibuf0 will output to P2. Emibuf0 is updated with CPU write data.

When EMIM = 1 and in no convert mode, emibuf0 will output to P2. Emibuf0 is updated with SPI1 DMA data.

When SPI2EMI = 1 and in convert mode, there are 3 output modes:

Corresponding bit	0			1		
1 byte mode	emibuf0			emibuf3		
2 byte mode	emibuf0		emibuf1	emibuf3		emibuf4
3 byte mode	emibuf0	emibuf1	emibuf2	emibuf3	emibuf4	emibuf5

When EMIM = 0 and EMIEN = 1, EMI transfer will be started by writing to EMIBUF.

When EMIM = 1 and EMIEN = 1, EMI transfer will be started by SPI DMA.

#### PWM Operation Guide

1. Configure EMICON1 register;
2. Read data from FFT output buffer;
3. Write data to PWMDAT register.

# 11 Audio Terminal (DAC)

## 11.1 Features

CW6680E/CW6681E/CW6682E provides a high performance stereo 16-bit resolution audio DAC:

- Sample Rate 8 / 11.025 / 12 / 16 / 22.05 / 24 / 32 / 44.1 / 48KHz
- Low Clock Jitter Sensitivity
- Soft Mute and -48Db Attenuator
- Class AB headphone amplifier
- 32 Level analog Gain/attenuation from Db to Db

## 11.2 DAC Special Function Registers

There are 2 SFR to support DAC registers read/write function:

Register 11-1 ATADR - audio terminal address

Position	7	6	5	4	3	2	1	0
Name	DONE	DIR	ATADR					
Default	x	x	x	x	x	x	x	x
Access	RW	RW	RW	RW	RW	RW	RW	RW

**DONE:** read/write operation done flag

0 = read/write operation is done

1 =read/write operation is running

**DIR:** read/write direction select

0 =read register

1 = write register

**ATADR:** Address of DAC registers

Register 11-2 ATDAT - audio terminal data

Position	7	6	5	4	3	2	1	0
Name	ATDAT							
Default	x	x	x	x	x	x	x	x
Access	RW	RW	RW	RW	RW	RW	RW	RW

ATDAT:

After read operation, CPU read this register to get the data.

Before write operation, CPU writes data to this register.

### 11.2.1 DAC Register Mapping

Table 11-1 DAC registers address mapping:

Name	Address	Descriptions
DACCFG	0	DAC configuration register
DACSM	1	DAC soft mute configuration register
DACSPR	2	DAC sample rate register
DACVOLL	3	DAC volume setting low byte register
DACVOLH	4	DAC volume setting high byte register
DACVCON	5	DAC volume control register
BASSCON1	12	BASS and EQ configuration register1
BASSCOF	13	BASS and EQ coefficient FIFO
BASSCON2	14	BASS and EQ configuration register2
BASSVOLIN	15	BASS and EQ data input volume configuration register
AUADCON1	16	Audio ADC configuration register1
AUADCON2	17	Audio ADC configuration register2
AUADCBAUD	18	Audio ADC sample clock configuration register

## 11.2.2 Function of DAC Control Registers

Register 11-3 DACCFG - DAC configuration register

Position	7	6	5	4	3	2	1	0
Name	-	-	-	MIX			OSSL	DACEN
Default	-	-	-	0	0	0	0	0
Access	-	-	-	RW	RW	RW	RW	RW

**MIX:** DAC output mode

000 = Normal mode (L, R)

001 = Two channels output the left channel data (L, L)

010 = Two channels output the right channel data(R, R)

011 = Two channel output average data  $((L+R)/2, (L+R)/2)$

100 = Left channel output average, right channel output inverse average  $((L+R)/2, -(L+R)/2)$

101 = Two channel output the minus of the data (L-R, L-R)

**OSSL:** DAC over sample mode select

0 = Normal speed mode

1 = Double speed mode

**DACEN:** DAC digital filter/delta-sigma modulator enable

0 = Disabled

1 = Enabled

Register 11-4 DACSM - DAC soft mute configuration register

Position	7	6	5	4	3	2	1	0
Name	DACSM							
Default	0	1	1	1	1	1	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW

DAC soft mute configuration, the reset value of DACSM is 126, user should not change it.

Register 11-5 DACSPR - DAC sample rate register

Position	7	6	5	4	3	2	1	0
Name	-	-	-	-	SRSEL			
Default	-	-	-	-	0	0	0	1
Access	-	-	-	-	RW	RW	RW	RW

**SRSEL:** DAC sample rate select

0000 = 48 KHz

0001 = 44.1 KHz

0010 = 32 KHz

0011 = Reserved

0100 = 24 KHz

0101 = 22.05 KHz

0110 = 16 KHz

0111 = Reserved

1000 = 12 KHz

1001 = 11.025 KHz

1010 = 8 KHz

1011 = Reserved

1100 = 48K synchronized with OBUF (+-0.8% max)

1101 = 44.1K synchronized with OBUF (+-0.8% max)

1110 = 32K synchronized with OBUF (+-0.8% max)

1111 = Reserved

Register 11-6 DACVOLL - DAC volume setting low byte register

Position	7	6	5	4	3	2	1	0
Name	DACVPND	DACVOLL						
Default	1	1	1	1	1	1	1	1
Access	RW	RW	RW	RW	RW	RW	RW	RW

**DACVPND:** DAC volume adjust done pending

Read "0": not done

Read "1": done

Write "0" clear pending

Write "1" affects nothing

Register 11-7 DACVOLH- DAC volume setting high byte register

Position	7	6	5	4	3	2	1	0
Name	DACVOLH							
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W



**Note:** When read DACVOLL and DACVOLH, the value isn't the setting value, but the actual DAC volume value

Register 11-8 DACVCON– DAC volume control register

Position	7	6	5	4	3	2	1	0
Name	-	-	-	DACVSET	-	DACVEN	DACVSTEP	
Default	-	-	-	0	-	0	0	0
Access	-	-	-	WO	-	R/W	R/W	R/W

**DACVSET:** Direct set DAC volume value

Write “1” to direct set DAC volume value

Write “0” affects nothing

**DACVEN:** DAC volume adjust enable

0 = Disable DAC volume adjust, keep the current volume

1 = Enable DAC volume adjust

**DACVSTEP:** DAC adjust volume steps

00 = Steps is “1”

01 = Steps is “2”

10 = Steps is “4”

11 = Steps is “8”

## 11.3 Operation Guide

### DAC Operation Guide

1. Configure DACVOLL & DACVOLH
2. Configure DACVCON
3. Clear DACVPND to kick start adjust volume

## 12 SARADC

### 12.1 Features

CW6680E/CW6681E/CW6682E provides an eight-channel moderate conversion speed and a moderate resolution 10-bit successive approximated register Analog to Digital Converter (SARADC) for users to develop applications in the following areas:

- Voice grade applications
- Audio applications requiring moderate performance
- Measurement requiring moderate performance and speed

SARADC conversion clock must be slower than 1 MHz

### 12.2 ADC Pin Mapping

Table 12-1 pin used

ADC Channel	Function	Description
ADC8	P16	Normal ADC channel
ADC7	LDO Band GAP	
ADC6	LDO in	Battery voltage
ADC5	P13	Normal ADC channel
ADC4	P30	Normal ADC channel
ADC3	P05	Normal ADC channel
ADC2	P04	Normal ADC channel
ADC1	P06	Normal ADC channel
ADC0	P33	Normal ADC channel

### 12.3 SARADC Special Function Registers

Register 12-1 ADCCON– SARADC control

Position	7	6	5	4	3	2	1	0
Name	ADCGO	EOC	TMREN	ADCTL	ADCEN	ADCSEL		
Default	0	0	x	x	0	0	0	0
Access	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W

**ADCGO:** ADC Conversion Start

When read:

0 = Conversion finished

1 = Conversion not finished

When write:

0 = N/A

1 = Start conversion

**EOC:** Check if end of conversion

0 = Finished

1 = Not finished

**TMREN:** Timer Input Enable

0 = Disabled

1 = Enabled

**ADCTL:** Timer Source Select

0 = Timer0

1 = Timer1

**ADCEN:** ADC Module Enable

0 = Disabled

1 = Enabled

**ADCS3, ADCSEL:** ADC Channel Select

0000 = P3.3 (ADC0)

0001 = P0.6 (ADC1)

0010 = P0.4 (ADC2)

0011 = P0.5 (ADC3)

0100 = P3.0 (ADC4)

0101 = P1.3 (ADC5)

0110 = Battery voltage

0111 = LDO\_BG

1000 = P16 (ADC8)

Register 12-2 ADCMODE– SARADC mode control

Position	7	6	5	4	3	2	1	0
Name	-	-	-	ADCS3	AUTOS	ADCSEL_SH		
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W

**ADCS3:** ADC Channel Select 3

**AUTOS:** Auto channel switching mode

0 = Not switch

1 = Auto load ADCSEL\_SH into ADCSEL after conversion finished

**ADCSEL\_SH:** ADCSEL shadow

Register 12-3 ADCBAUD– SARADC baud rate control

Position	7	6	5	4	3	2	1	0
Name	-	-	ADCBAUD					
Default	-	-	x	x	x	x	x	x
Access	-	-	WO	WO	WO	WO	WO	WO

ADC conversion clock = system clock / (2 x (ADCBAUD + 1))

Register 12-4 ADCDATAL– SARADC Buffer low byte control

Position	7	6	5	4	3	2	1	0
Name	ADCDATAL		-	-	-	-	-	-
Default	x	x	-	-	-	-	-	-
Access	RO	RO	-	-	-	-	-	-

Register 12-5 Register 21-4 ADCDATAH– SARADC Buffer high byte control

Position	7	6	5	4	3	2	1	0
Name	ADCDATAH							
Default	x	x	x	x	x	x	x	x
Access	RO	RO	RO	RO	RO	RO	RO	RO

## 13 Characteristics

### 13.1 LDO Parameters

Table 13-1 LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
V <sub>in</sub>	LDO input voltage	3.2	4.0	5.5	V	
V <sub>out1.2</sub>	1.2V output voltage	-	1.2	-	V	
V <sub>out3.3</sub>	3.3V output voltage	-	3.3	-	V	
I <sub>out1.2</sub>	1.2V output current	-	50	-	mA	
I <sub>out3.3</sub>	3.3V output current	-	150	-	mA	

### 13.2 PLL Parameters

Table 13-2 PLL Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
F <sub>I1</sub>	Frequency input	-	32.768	-	KHz	Low frequency OSC
F <sub>I2</sub>	Frequency input	1	12	15	MHz	High frequency OSC
F <sub>OUT1</sub>	Frequency output	-	48	-	MHz	
T <sub>LOCK1</sub>	PLL locked time	-	2	-	ms	Use low frequency OSC as input reference
T <sub>LOCK2</sub>	PLL locked time	-	0.1	-	ms	Use high frequency OSC as input reference

### 13.3 I/O Parameters

Table 13-3 I/O Parameters

Symbol	Description	Min	Typ	Max	Units	Conditions
V <sub>IL</sub>	Low-Level input voltage	-	-	30% * VDDIO	V	VDDIO = 3.3V
V <sub>IH</sub>	High-level input voltage	70% * VDDIO	-	-	V	VDDIO = 3.3V
R <sub>PUP0</sub>	Internal pull-up resistor 0	2.64	3.3	3.96	KΩ	For PORT2
R <sub>PDN0</sub>	Internal pull-down resistor 0	2.64	3.3	3.96	KΩ	For PORT2
R <sub>PUP1</sub>	Internal pull-up resistor 1	12.067	10	13.734	KΩ	For PORT0/1/3
R <sub>PDN1</sub>	Internal pull-down resistor 1	12.067	10	13.734	KΩ	For PORT0/1/3
I <sub>LEVEL1</sub>	Level1 current driving	8	-	-	mA	For PORT1
I <sub>LEVEL2</sub>	Level2 current driving	24	-	-	mA	For Port1.1

## 13.4 Audio DAC Parameters

Table 13-4 Audio DAC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
SNR&DR		-	92	-	dB	48PIN
SNR&DR		-	82	-	dB	28PIN & 20 PIN
THD+N		-	-70	-	dB	10Kohm loading
PWR <sub>AB</sub>	ClassAB AMP power output	-	-	16	mW	32ohm loading
V <sub>PP</sub>	Maximum output voltage	-	-	2.8	V	10Kohm loading

# 14 Package Dimensions

## 14.1 CW6680E/CW6681E/CW6682E LQFP48

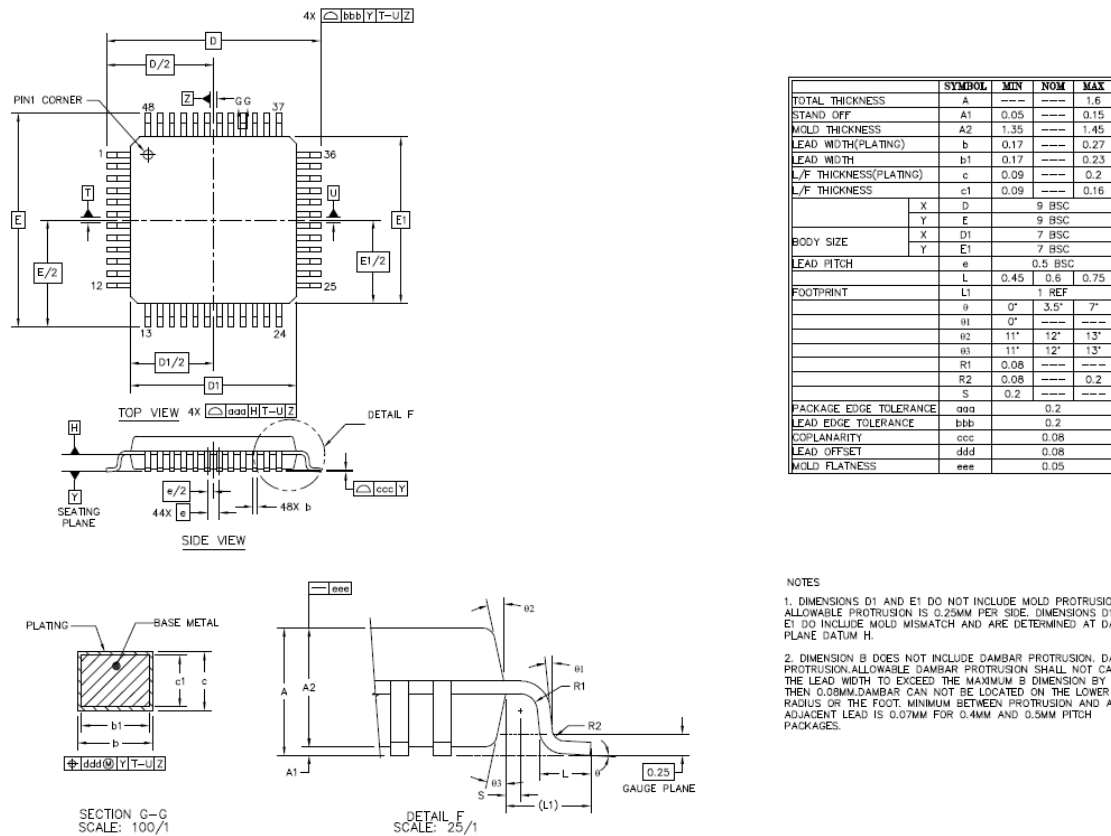


Figure 14-1 CW6680E/CW6681E/CW6682E LQFP48 package dimensions





## Appendix I Revision History

Date	Version	Comments	Revised by
2014-8-8	0.0.1	CW6680E/CW6681E Initial Version	YX
2014-8-8	0.0.2	Checked	JF
2014-8-8	1.0.0	Released	YX
2014-10-11	1.1.0	Add CW6682E package information	LD

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