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AX3153A

Audio Player Microcontroller

User Manual

[AX3153A-UM-EN]

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1 Product Overview

Audio Player Microcontroller

1.1 General Description

AX3153A is a 32-bit data RISC microcontroller, and an 32-bit audio DSP processer. This product is designed to provide all audio decode applications with cost-effective, low-power, and high-performance microcontroller solution in a small die size.

AX3153A is a high performance mixed signal microcontroller. It integrates advanced digital and analog peripherals to audio decode player applications.

1.2 Features

- 32bit RISC CPU and DSP;
- Maximum 120MHz operating frequency;
- Two SD Host controller
- Two SPI;
- Four UART;
- SPDIF receiver;
- IR with TX and RX;
- Independent powered RTCC;
- IIC master interface;
- Two IIS whith PCM format;
- TouchKey with 12 channels;
- Eigth Bank EQ
- AEC & FFT
- DRC
- Watchdog
- Segment LCD/LED controller supports 32pins
- USB1.1 Device and Host
- USB2.0 Device and Host
- Two SARADC with 12-channels
- Two MIC and AGC
- Three Groups Stereo AUX
- Stereo Audio ADC with 95dB SNR
- Three Audio DAC with 100dB SNR
- Two shadow audio DAC channels with gain control
- Stereo class A/B audio AMP
- Oscillator for external 32.768KHz crystal resonator;
- Oscillator for external 12MHz crystal resonator;
- internal 10MHz RC oscillator;
- internal 4MHz RC oscillator
- internal 1MHz RC oscillator
- channels 4 levels Low Voltage Detector;
- Two internal LDO regulator;
- PLL-based clock generator;
- Power on Reset.

2 Pin Definitions

2.1 AX3153A

2.1.1 Package

AX3153A

2.1.2 Pin Assignment

Figure 2-1 shows the pin assignments of AX3153A package.

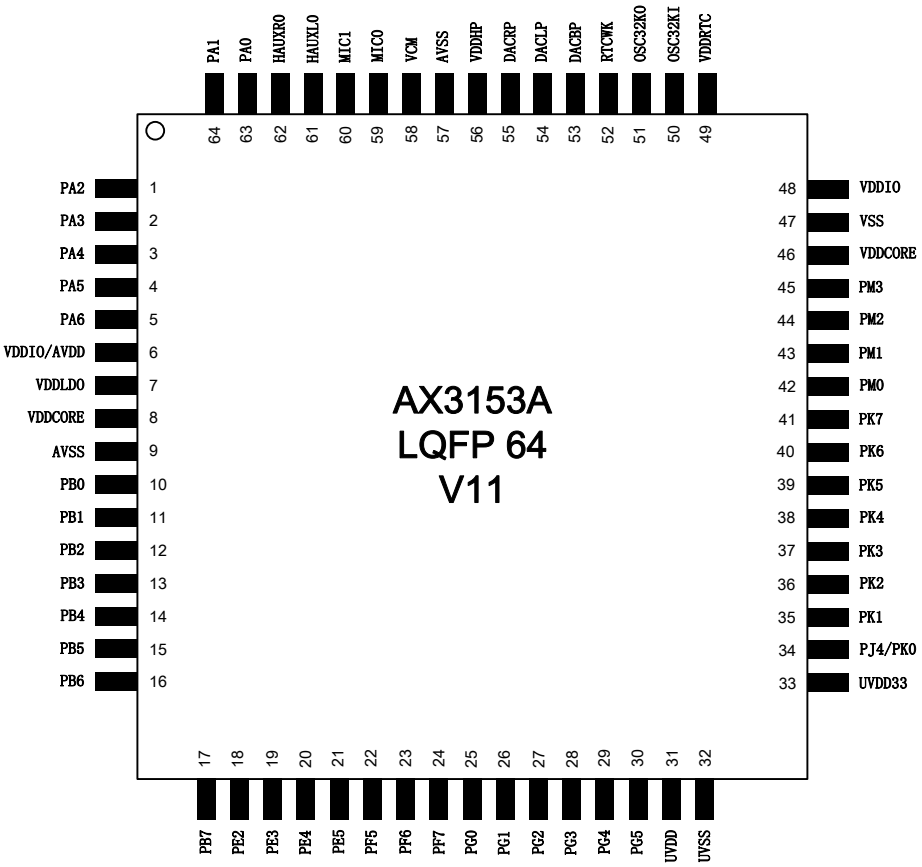

Figure 2-1 Pin assignment for AX3153A

2.1.3 Pin Descriptions

Table 2-1 shows the pin descriptions of AX3153A package.

Table 2-1 AX3153A pin description

Pin No.LQFP64	Name	Type	Function
1	PA2	IO1B1	MIC_DET
2	PA3	IO1B1	BTLDO_EN
3	PA4	IO1B1	SPDIF_OPTICAL
4	PA5	IO1B1	SPDIF_RCA
5	PA6	IO1B1	ADKEY
6	VDDIO/AVDD	PWR	VDDIO
7	VDDLDO	PWR	VCC5V
8	VDDCORE	PWR	VDDCORE
9	AVSS	GND	Ground

Pin No.LQFP64	Name	Type	Function
10	PB0	IO1B1	PA_MCLK
11	PB1	IO1B1	PA_SCLK
12	PB2	IO1B1	PA_LRCLK
13	PB3	IO1B1	PA_SDIN
14	PB4	IO1D1	PA_SHUTDOWN
15	PB5	IO1B1	PA_RESET
16	PB6	IO1B1	STANDBY
17	PB7	IO1B1	IRDAT
18	PE2	IO1B1	SPI_MISO
19	PE3	IO1B1	SPI_CLK
20	PE4	IO1B1	SPI_MOSI
21	PE5	IO1B1	SPI_CS
22	PF5	IO1B1	UART_RX
23	PF6	IO1B1	UART_TX
24	PF7	IO1B1	BT_WAKEUP
25	PG0	IO1B1	BT_RST
26	PG1	IO1B1	SD_DAT/I2C_DAT
27	PG2	IO1B1	SD_CLK
28	PG3	IO1B1	SD_CMD/I2C_CLK
29	PG4	IO1B1	USBDM
30	PG5	IO1B1	USBDP
31	UVDD	PWR	VDDCORE
32	UVSS	GND	Ground
33	UVDD33	PWR	VDDIO
34	PJ4/PK0	IO1B2/IO1B3	LCD_COM4
35	PK1	IO1B3	LCD_COM3
36	PK2	IO1B3	LCD_COM2
37	PK3	IO1B3	LCD_COM1
38	PK4	IO1B3	LCD_COM0
39	PK5	IO1B3	LCD_D0
40	PK6	IO1B3	LCD_D1
41	PK7	IO1B3	LCD_D2
42	PM0	IO1B2	LCD_D3
43	PM1	IO1B2	LCD_D4
44	PM2	IO1B2	LCD_D5
45	PM3	IO1B2	LCD_D6
46	VDDCORE	PWR	VDDCORE
47	DVSS	GND	Ground
48	VDDIO	PWR	VDDIO
49	VDDRTC	PWR	VDDRTC
50	OSC32KI	AIO	OSC32KI
51	OSC32KO	AIO	OSC32KO
52	RTCWK	AIO	RTCWK
53	DACBP	AIO	DACB
54	DACLP	AIO	DACL
55	DACRP	AIO	DACR
56	VDDHP	PWR	VDDHP
57	AVSS	GND	Ground
58	VCM	AIO	VCM
59	MIC0	AIO	MIC0
60	MIC1	AIO	MIC1
61	HAUXL0	AIO	AUXL
62	HAUXR0	AIO	AUXR
63	PA0	IO1B1	FM_OUTL
64	PA1	IO1B1	FM_OUTR

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Part 2 *Memory System*

3 CPU Core Information

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3 CPU Core Information

3.1 Architecture

AX3153A has been developed using the advanced 32 bit RISC core. The RISC core features are:

- 32 general-purpose 32-bit registers
- 5-stage pipeline with extensive clock-gating
- Static branch prediction
- Return address stack
- Vector interrupts for internal interrupt controller,support up to 32 hardware vector interrupt signals,not need to external interrupt conctroller in system.
- 3 HW-level nested interruption
- User and super-user mode support
- Memory-mapped I/O
- Address space up to 4GB
- 16/32-bit mixed instruction format for enhance code density and reduce code size
- Saturation extension ISA
- Inline funciton call extension ISA
- DSP ISA extension

3.2 Interruption processing

3.2.1 Interruption Vectored Entry Point

AX3153A RISC core has a IVIC(internal vector interrupt controller) which has 41 entry points(9 exception + 32 HW interrupt).The entry point address = IVB.IVBASE + (entry number)*IVB.ESZ. It supports for preemptive interrupt with programmable priority.

Table 3-1 Entry points for Internal VIC mode

Entry number	Entry point	Entry type
0	/	Core exceptions
1	/	
2	/	
3	/	
4	/	
5	/	
6	/	
7	/	
8	/	
9	timer_intr[0]	External Hardware interrupt source
10	timer_intr[1]	
11	timer_intr[2]	
12	timer_intr[3]	
13	timer_intr[4]	
14	/	
15	spi0_intr	
16	spi1_intr	
17	iic_int	
18	sdc_int	
19	/	
20	uart0_intr/ uart3_intr	
21	/	
22	ir_int/ irtx_int	
23	rtc_intr/ wdt_intr/ lvd_int	
24	tk0_int/ tk1_int	
25	sw_int	

Entry number	Entry point	Entry type
26	/	
27	iis_int_o	
28	portwakeup	
29	/	
30	obuf_int	
31	/	
32	/	
33	/	
34	fsusb_sof_intr	
35	/	
36	MC_NINT	
37	spdif_int	
38	lcd_intr	
39	blt_int	
40	sdadc_sp_int	

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Part 3 *Power Management*

4 Reset Management

5 Low Power Management

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4 Reset Management

4.1 Power-on Reset (POR)

AX3153A provides an on-chip Power-On-Reset (POR) circuit to detect power-on and to reset internal logic before VDD reaches the pre-determined POR threshold voltage. POR releasing voltage is about 0.7V.

POR circuit incorporates an internal self-reset module to discharge during power-off to ensure each power cycle will work properly. The discharging voltage is about 0.47V.

It is also highly recommended user should have a long time between power-off and next power-on to ensure proper start-up. The time depends on actual system board environment and total decoupling capacitors between power and ground. User has to take into account this effect during board level design.

Figure 5-1 illustrates the power-on and reset signals waveform during proper power-on. Internally, there is T_{POR} and T_{RC} time for both the POR circuit and the internal counter. T_{POR} is the time for the POR circuit to stay at zero voltage until it reaches V_{POR} and the time varies for different VDD rise-up time. It can be assumed to be about 2/3 of the VDD rise-up time. T_{RC} is the time for internal counter to count 4ms using internal RC-oscillator after POR signal released. As a result, the overall internal reset time is the sum of T_{POR} and T_{RC}. Such a long time is required to ensure the Power is stable for system use. It also ensures all internal logics are properly reset.

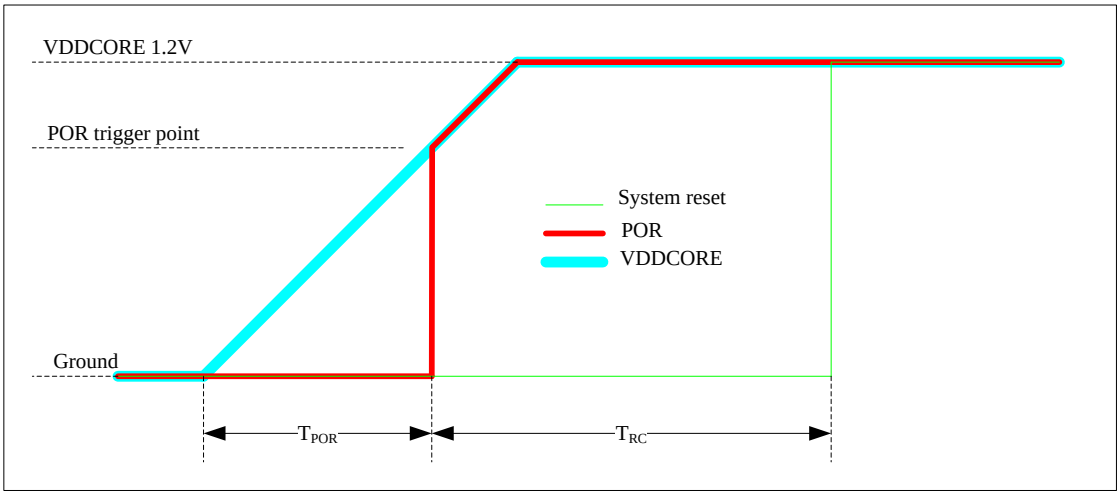

Figure 4-1 Power on reset

4.2 LVD

AX3153A provides 4 levels programmable Low Voltage Detector (LVD) for user to detect VDDLDO power supply voltage or external pin voltage multiplexed with GPIO PA6. It is for doing so since VDDLDO is the input voltage source for on-chip Low-Drop-Out regulator (LDO) and that supplies power to internal VDDCORE. User for such reason can momentarily monitor the VDDLDO power if externally connects to some batteries and detect if external power source starts dropping to a level that AX3153A LDO cannot tolerate and can do proper actions in the system program.

LVD can also be used to monitor external voltage source through the GPIO PA6 to enhance programmability for different voltage levels. One of the examples can be used to monitor external power sources or batteries voltage or some voltages related to say pressure or temperature. It is there to provide a simple interface compared to ADC since ADC requires more programming space and procedures to detect precise voltage level. If user requires un-precise voltage detection without fine voltage range, LVD will be a good choice compared to ADC measurement. *Table 4-1* illustrates different voltage detection levels.

Remark:

1. When LVD_ENB is enabled, there is approximately 100us for the band-gap and the comparator to be stable before the end-user can use it as low voltage detection. During the time, LVD_OEB has to be H in order to disable the LVD output with possibly fluctuating signal level.
2. Different power supply falling time will affect the voltage detection. It is recommended that the power supply falling time should be larger than 1ms for stable low voltage detection.

Upon detection occurs, interrupt can be generated if LVD interrupt is enabled, or can undergo reset if interrupt is disabled.

Note that the detection is slightly dependent on power supply falling rate and noise fluctuation during power drop

may alter the detection results. For this reason, internally the comparator has about 150mV hysteresis voltage level defined as VHYS = VLVDR-VLVDS to filter out the noise may occur. Also, the detection level may have a maximum of 100mV difference compared to the value stated in *Table 4-1*.

Table 4-1 LVD level setting

LVDS	EX_PIN Detection Level (V)	VDDLDO Detection Level (V)
00	1.8	2.2
01	1.95	2.4
10	2.2	2.7
11	2.5	3.1

For the best operation, below shows a recommended operation for the LVD.

1. Select either VDDLDO or external pin to be monitored. Set VDI_EN = 0 for VDDLDO or VDP_EN = 0 for external pin
2. Select the detection voltage by setting bits LVDS.
3. Enable the LVD by setting LVD_EN = 0.
4. Wait for at least 30us for the internal band-gap and comparator to become stable .
5. Enable the LVD output by setting LVD_OE = 0 .
6. The EX_PIN detect voltage must be less than VDDIO.

Register 4-1 LVDCON– LVD control Register

Bit	Name	Mode	Default	Description
9	CLVDIF	WO	0	Clear LVD interrupt pending bit. 0 = No active 1 = Clear LVD interrupt pending bit
7	LVDIF	RO	0	LVD interrupt pending bit. 0 = When LVD threshold not detect. 1 = When LVD threshold is detected
6	LVD_IE	RW	0	LVD interrupt enable bit. 0 = LVD interrupt is disabled 1 = LVD interrupt is enabled
5	LVD_RSTEN	RW	1	LVD Reset enable bit. 0 = LVD Reset is disabled 1 = LVD Reset is enabled
4	LVD_EN	RW	1	LVD enable bit. Low active 0 = LVD is enabled 1 = LVD is disabled
3	LVD_OE	RW	0	LVD output enable bit. Low active 0 = LVD output is enabled 1 = LVD output is disabled
2	VDP_EN	RW	0	External pin (PA6) voltage enable bit. Low active 0 = External pin voltage detection is enabled 1 = External pin voltage detection is disabled
1:0	LVDS	RW	2'b00	LVD voltage detection level select 00 = Detect VDI-2.2V; Detect VDP 1.8V 01 = Detect VDI-2.4V; Detect VDP 1.95V 10 = Detect VDI-2.7V; Detect VDP 2.2V 11 = Detect VDI-3.1V; Detect VDP 2.5V

4.3 Reset System

4.3.1 MCLR Reset

AX3153A provides MCLR PIN for Reset. MCLR default 200K pull up resister. External capacitor is need when MCLR pin is used. There is 1ms digital filter for MCLR pull down reset. So MCLR must be pulled down longer than 1ms for Reset system.

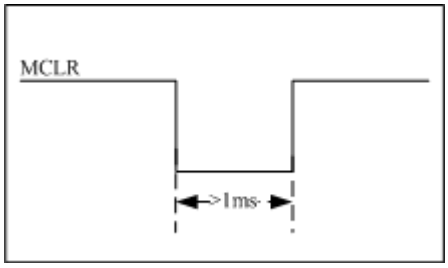

Figure 4-2 MCLR reset

4.3.2 RTCC Reset

AX3153A can be reset by RTCC second and alarm interrupt when IRTRSTEN bit enable in IRTCON.

4.3.3 Watchdog Reset

If Watchdog timer is enabled, and watchdog reset is enabled, and s not clear watchdog counter within watchdog overflow time period, AX3153A will be reset by Watchdog overflow.

4.3.4 Port Wakeup Reset

During SLEEP mode, port wakeup event will cause AX3153A reset.

5 Low Power Management

5.1 Power Supply

There are two system on-chip low drop-out regulators (LDO).

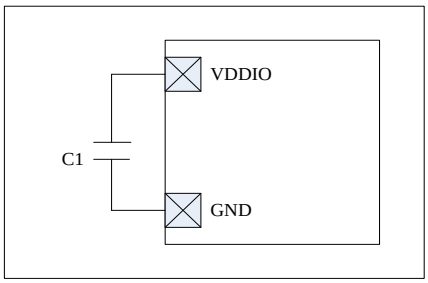

Figure 5-1 Frequency compensation through external component

Note:

1. The recommended value for C1 is 10uf.
2. C1 should be placed closely to the chip.

5.2 Power Saving Mode

AX3153A has the low power management mode that can help reducing power consumption when the device does not require intensive CPU resources and speed. There are four low power modes available: POWER_DOWN mode, SLEEP mode, HOLD mode, IDLE mode.

5.2.1 Power_down mode

Power down mode means VDDIO and VDDCORE are power off by disabling LDO0 and LDO1. LDO0 and LDO1 can be turn on by IRTCC. When VDDLDO is high than 4.2V, LDO0 and LDO1 should not be disabled.

5.2.2 Sleep Mode

SLEEP mode is an ultimate power reduction mode that will stop all the clock sources, and all the memory chip select signals are disabled to further reduce power consumption. However, before entering sleep mode, all peripherals should be disabled separately, especially analog peripherals and memory, unless those peripherals will stop themselves if no clock source is applied to the peripherals.

Note: Before Entering SLEEP mode, the system clock is recommended to change back to RC4M oscillator clock as the system clock. RC4M oscillator will be disabled automatically in SLEEP mode.

To enter SLEEP mode, user need to write a ‘1’ to SLEEP register (PCON0).

During SLEEP mode, the device can be wake up by

1) MCLR reset

2) External port wakeup reset

3) Watchdog reset

4) RTCC reset

After exit SLEEP mode by wakeup, the device will be reset.

5.2.3 Hold Mode

HOLD mode will stop the clock from entering to system. The system clock is gated with the HOLD mode control. Once enter HOLD mode, clock to the system logic halts. Therefore, there will be no clock switching entering the system logic so that power consumption is minimized due to no AC switching. However, the clock sources are not disabled and they are still running. This allows the clock to be resumed in real time without waiting for the PLL to lock again.

TO enter HOLD mode, user need to write a ‘1’ to HOLD register (PCON0).

During HOLD mode, the device can be wake up by

1) watchdog interrupt

2) RTCC interrupt

3) Port interrupt

4) All reset source

When wakeup from HOLD Mode by port or RTCC, if interrupt is enabled, AX3153A enters corresponding interrupt service subroutine (ISR), else AX3153A will execute the instruction following HOLD.

When wakeup from HOLD Mode by watchdog, if watchdog reset enable, AX3153A will be reset, else if watchdog reset is disable, AX3153A will enter watchdog's ISR. Else AX3153A will execute the instruction following HOLD.

5.2.4 Idle Mode

IDLE mode will stop the clock from entering to the CPU. The CPU clock is gated with the IDLE mode control. Once enter IDLE mode, clock to the CPU logic halts. Therefore, there will be no clock switching entering the CPU logic so CPU power consumption is minimized.

All interrupt sources will cause system to exit IDLE mode, which include all peripheral interrupt.

TO enter IDLE mode, user need to write a '1' to IDLE register (PCON0).

When exit IDLE mode, AX3153A will enter interrupt service subroutine if EA is enable. If EA is disabled, the instruction next to IDLE will be executed.

5.2.5 3.3V Power Output

AX3153A provides 3.3V power output through VOUT pin. VOUT maximum current driving is 250mA supported by LDO0. VOUT can be shut down by software. VOUT internal resistor is about 2R.

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Part 4 *System Peripheral*

6 General Purpose Input/Output (GPIO)

7 Timers

8 SARADC

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6 General Purpose Input/Output (GPIO)

6.1 Overview

The general purpose input/output port (GPIO) provides 105 dedicated general purpose one-bit contacts that can be individually configured as either inputs or outputs. Contacts configured as outputs reflect internal register values, and those configured as inputs can be detected by reading internal registers. All GPIOs are divided into 14 groups: PortA, PortB, PortD, PortE, PortF, PortG, PortH, , PortJ, , PortK, , PortM, , PortN, PortQ, , PortR and PortS.

6.2 Features

The GPIO includes the following features:

1. Drive specific data to output using the data register;
2. Control the direction of the signal using the GPIO direction register;
3. Enable CPU to sample the status of the corresponding inputs by reading the data register;
4. Enable internal pull-up resistor using pull-up resistor control register;
5. Enable internal pull-down resistor using pull-down resistor control register;
6. Select suitable output driving current capability;

6.3 Function multiplexing

Register 6-1 PxFMAP: Port function mapping Configure Register(x=A,B,D,E,F,G,H,J,K,M,N,Q,R,S)

Bit	Name	Mode	Default	Description
7	PORTx7FS	RW	1	Px7 function mapping selection 0=Px7 is GPIO Pin 1=Px7 is Function Pin
6	PORTx6FS	RW	1	Px6 function mapping selection 0=Px6 is GPIO Pin 1=Px6 is Function Pin
5	PORTx5FS	RW	1	Px5 function mapping selection 0=Px5 is GPIO Pin 1=Px5 is Function Pin
4	PORTx4FS	RW	1	Px4 function mapping selection 0=Px4 is GPIO Pin 1=Px4 is Function Pin
3	PORTx3FS	RW	1	Px3 function mapping selection 0=Px3 is GPIO Pin 1=Px3 is Function Pin
2	PORTx2FS	RW	1	Px2 function mapping selection 0=Px2 is GPIO Pin 1=Px2 is Function Pin
1	PORTx1FS	RW	1	Px1 function mapping selection 0=Px1 is GPIO Pin 1=Px1 is Function Pin
0	PORTx0FS	RW	1	Px0 function mapping selection 0=Px0 is GPIO Pin 1=Px0 is Function Pin

6.4 Port interrupt and wakeup

AX3153A supports Port interrupt and wakeup function. There are 32 wake up circuit sources.

Wake up circuit	Wake up source
0	PA2
1	PA3
2	PA4
3	PA5
4	PA6
5	PB0

Wake up circuit	Wake up source
6	PB4
7	PB5
8	PB6
9	PB7
10	PD4
11	PD5
12	PD6
13	PD7
14	PF0
15	PF1
16	PF2
17	PF3
18	PF4
19	PF5 or FSUSB0DM
20	PF6 or FSUSB0DP
21	PF7
22	PG0
23	PG4 or FSUSB1DM
24	PG5 or FSUSB1DP
25	PJ7
26	PN0
27	PN1
28	PN2
29	HSUSBDM
30	HSUSBDP
31	RTCWK
32	PB2
33	PD2
34	PK2
35	PK5
36	PK6

The PORTWKEN registers (Wakeup Enable Register) allow each group wake up circuit to cause wakeup.

The PORTWKEN registers are set to 00h upon reset. Seting bits in the PORTWKEN register enables wakeup on corresponding wake up circuit. The trigger condition on the selected pin can be either rising edge or falling edge. The PORTWKEDG register (Wakeup Edge Select) selects the desired transition edge. Setting a bit in PORTWKEDG register selects the falling edge of the corresponding wake up circuit. Resetting the bit selects the rising edge.

Once a valid transition occurs on the selected pin, the WKPND register (Wakeup Pending Register) latches the transition in the corresponding bit position. Logic ‘1’ indicates the occurrence of the selected trigger edge on the corresponding Port pins. Upon reset, logic ‘0’ is set to all bits of WKPND.

Note:

1. To Wakeup initialization, to avoid any false signaling to port, the followings would be a recommended procedure for Wakeup initialization:
2. Configure the edge select of wakeup pins on PORTWKEDG register,
3. Clear the corresponding bits on WKPND Wakeup Pending Register
4. Set the corresponding bits in the PORTWKEN registers to enable the wakeup on the corresponding port pins
5. Upon exiting the SLEEP mode, the Multi-Input Wakeup logic causes full chip reset.

Register 6-2 PORTWKPND: PORT wakeup pending flag

Bit	Name	Mode	Default	Description
31:0	PORTWKPND	RW	32'hxxxxxxxx	Port wake up pending flag.

Register 6-3 PORTWKPND1: PORT wakeup pending flag 1

Bit	Name	Mode	Default	Description

Bit	Name	Mode	Default	Description
31:5	Reserved	Reserved	Reserved	Reserved
4:0	PORTWKPND1	RW	4'hx	

Register 6-4 PORTWKEN: PORT wakeup enable

Bit	Name	Mode	Default	Description
31:0	PORTWKEN	RW	32'h0	Port wake up enable bit.

Register 6-5 PORTWKEN1: PORT wakeup enable 1

Bit	Name	Mode	Default	Description
31:5	Reserved	Reserved	Reserved	Reserved
4:0	PORTWKEN1	RW	4'h0	Port wakeup enable bit.

Register 6-6 PORTWKEDG: PORT wakeup edge

Bit	Name	Mode	Default	Description
31:0	PORTWKEDG	RW	32'h0	Port wake up edge select bit.

Register 6-7 PORTWKEDG1: PORT wakeup edge 1

Bit	Name	Mode	Default	Description
31:5	Reserved	Reserved	Reserved	Reserved
4:0	PORTWKEDG1	RW	4'h0	Port wake up edge select bit.

Note:

1. to enable WKPNDx, set PWKENx to ‘0’.
2. To clear WKPNDx, write ‘0’ to WKPNDx. WKPNDx will be ‘0’ 2 clocks later after write ‘0’ to WKPNDx.
3. WKPNDx is cleared when PWKENx is ‘1’.
4. **This register avoid using "OR" and "AND" operation, should be use direct write or read operation.**
5. **when PORTWKEDGx write 1,capture port rising;write 0,capture port falling.**

6.5 GPIO Special Function Registers

Register 6-8 PxDIR: PORTx direction Register(x=A,B,D,E,F,G,H,J,K,M,N,Q,R,S)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxDIR	RW	8'h0	Px direction control 0 = Output 1 = Input

Register 6-9 PORTx: PORTx Data Register(x=A,B,D,E,F,G,H,J,K,M,N,Q,R,S)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PORTx	RW	8'h0	Px data. Valid when Px is used as GPIO 0 = Px is in low state when read and output low at Px when write 1 = Px is in high state when read and output high at Px when write

Register 6-316-10 PxPU10K: PORTx pull-up 10K resistor control(x=A,B,D,E,F,G,H,J,K,M,Q,S)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPU10K	RW	8'h0	Px 10KΩ pull-up resister control. Valid when Px is used as input 0 = 10KΩ pull-up resistor disabled 1 = 10KΩ pull-up resistor enabled

Register 6-32 PxPD10K: PORTx pull-down 10K resistor control(x=A,B,D,E,F,G,H,J,K,M,Q,S)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPD10K	RW	8'h0	Px 10KΩ pull-down resister control. Valid when Px is used as input 0 = 10KΩ pull-dwon resistor disabled 1 = 10KΩ pull-dwon resistor enabled

Register 6-33 PxPU20K: PORTx pull-up 20K resistor control(x=H, K, M, Q, N)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPU20K	RW	8'h0	Px 20KΩ pull-up resister control. Valid when Px is used as input 0 = 20KΩ pull-up resistor disabled 1 = 20KΩ pull-up resistor enabled

Register 6-34 PxPD20K: PORTx pull-down 20K resistor control(x=H, J, K, M, Q)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPD20K	RW	8'h0	Px 20KΩ pull-down resister control. Valid when Px is used as input 0 = 20KΩ pull-down resistor disabled 1 = 20KΩ pull-down resistor enabled

Register 6-35 PxPU200: PORTx pull-up 200 resistor control(x=H, J, K, M, Q)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPU200	RW	8'h0	Px 200Ω pull-up resister control. Valid when Px is used as input 0 = 200Ω pull-up resistor disabled 1 = 200Ω pull-up resistor enabled

Register 6-36 PxPD200: PORTx pull-down 200 resistor control(x=H, J, K, M, Q)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPD200	RW	8'h0	Px 200Ω pull-down resister control. Valid when Px is used as input 0 = 200Ω pull-down resistor disabled 1 = 200Ω pull-down resistor enabled

Register 6-37 PxPU400: PORTx pull-up 400 resistor control(x=H, J, K, M, Q)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPU400	RW	8'h0	Px 400Ω pull-up resister control. Valid when Px is used as input 0 = 400Ω pull-up resistor disabled 1 = 400Ω pull-up resistor enabled

Register 6-38 PxPD400: PORTx pull-down 400 resistor control(x=H, J, K, M, Q)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxPD400	RW	8'h0	Px 400Ω pull-down resister control. Valid when Px is used as input 0 = 400Ω pull-down resistor disabled 1 = 400Ω pull-down resistor enabled

Register 6-39 PKPU200K: PORTx pull-up 200k resistor control

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved

Bit	Name	Mode	Default	Description
7:0	PKPU200K	RW	8'h0	Px 200KΩ pull-up resister control. Valid when Px is used as input 0 = 200KΩ pull-up resistor disabled 1 = 200KΩ pull-up resistor enabled

Register 6-40 PxDRV24: PORTx 24mA driving control(x=A,B,D,E,F,G,H,J,K,M,Q)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxDRV24	RW	8'h0	Px 24mA driving control 0 = 8mA 1 = 24mA

Register 6-41 PxDRV16: PORTx 16mA driving control(x=N, R)

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	Reserved	Reserved
7:0	PxDRV16	RW	8'h0	Px 16mA driving control 0 = 8mA 1 = 16mA

Register 6-42 PESRC: PORTE slew rate control

Bit	Name	Mode	Default	Description
31:18	Reserved	Reserved	Reserved	Reserved
17:16	PE5SRCSEL	R	2'h0	PE5 src sel
15:14	PE4SRCSEL	R	2'h0	PE4 src sel
13:12	PE3SRCSEL	R	2'h0	PE3 src sel
11:10	PE2SRCSEL	R	2'h0	PE2 src sel
9:8	PE1SRCSEL	R	2'h0	PE1 src sel
7:6	PE0SRCSEL	RW	2'h0	PE0 src sel
5	PE5SRCEN	RW	0	PE5 src enable 0 = disable 1 = enable
4	PE4SRCEN	RW	0	PE4 src enable 0 = disable 1 = enable
3	PE3SRCEN	RW	0	PE3 src enable 0 = disable 1 = enable
2	PE2SRCEN	RW	0	PE2 src enable 0 = disable 1 = enable
1	PE1SRCEN	RW	0	PE1 src enable 0 = disable 1 = enable
0	PE0SRCEN	RW	0	PE0 src enable 0 = disable 1 = enable

Register 6-43 PFSRC: PORTF slew rate control

Bit	Name	Mode	Default	Description
31:24	Reserved	Reserved	Reserved	Reserved
23:22	PF7SRCSEL	R	2'h0	PF7 src sel
21:20	PF6SRCSEL	R	2'h0	PF6 src sel
19:18	PF5SRCSEL	R	2'h0	PF5 src sel
17:16	PF4SRCSEL	R	2'h0	PF4 src sel
15:14	PF3SRCSEL	R	2'h0	PF3 src sel
13:12	PF2SRCSEL	R	2'h0	PF2 src sel
11:10	PF1SRCSEL	R	2'h0	PF1 src sel

Bit	Name	Mode	Default	Description
9:8	PF0SRCSEL	R	2'h0	PF0 src sel
7	PF7SRCEN	RW	0	PF7 src enable 0 = disable 1 = enable
6	PF6SRCEN	RW	0	PF6 src enable 0 = disable 1 = enable
5	PF5SRCEN	RW	0	PF5 src enable 0 = disable 1 = enable
4	PF4SRCEN	RW	0	PF4 src enable 0 = disable 1 = enable
3	PF3SRCEN	RW	0	PF3 src enable 0 = disable 1 = enable
2	PF2SRCEN	RW	0	PF2 src enable 0 = disable 1 = enable
1	PF1SRCEN	RW	0	PF1 src enable 0 = disable 1 = enable
0	PF0SRCEN	RW	0	PF0 src enable 0 = disable 1 = enable

Register 6-44PGSRC: PORTG slew rate control

Bit	Name	Mode	Default	Description
31:17	reserved	reserved	reserved	reserved
16:14	PG45SRCSEL	R	2'h0	PG4,PG5 src sel
13:12	PG3SRCSEL	R	2'h0	PG3 src sel
11:10	PG2SRCSEL	R	2'h0	PG2 src sel
9:8	PG1SRCSEL	R	2'h0	PG1 src sel
7:6	PG0SRCSEL	R	2'h0	PG0 src sel
5	PG5SRCEN	RW	0	PG5 src enable 0 = disable 1 = enable
4	PG4SRCEN	RW	0	PG4 src enable 0 = disable 1 = enable
3	PG3SRCEN	RW	0	PG3 src enable 0 = disable 1 = enable
2	PG2SRCEN	RW	0	PG2 src enable 0 = disable 1 = enable
1	PG1SRCEN	RW	0	PG1 src enable 0 = disable 1 = enable
0	PG0SRCEN	RW	0	PG0 src enable 0 = disable 1 = enable

7 Timers

7.1 Multi-function Timers (Timer0~4)

There are five 16-Bit Multi-Function Timers in AX3153A. They are Timer0 to Timer4.

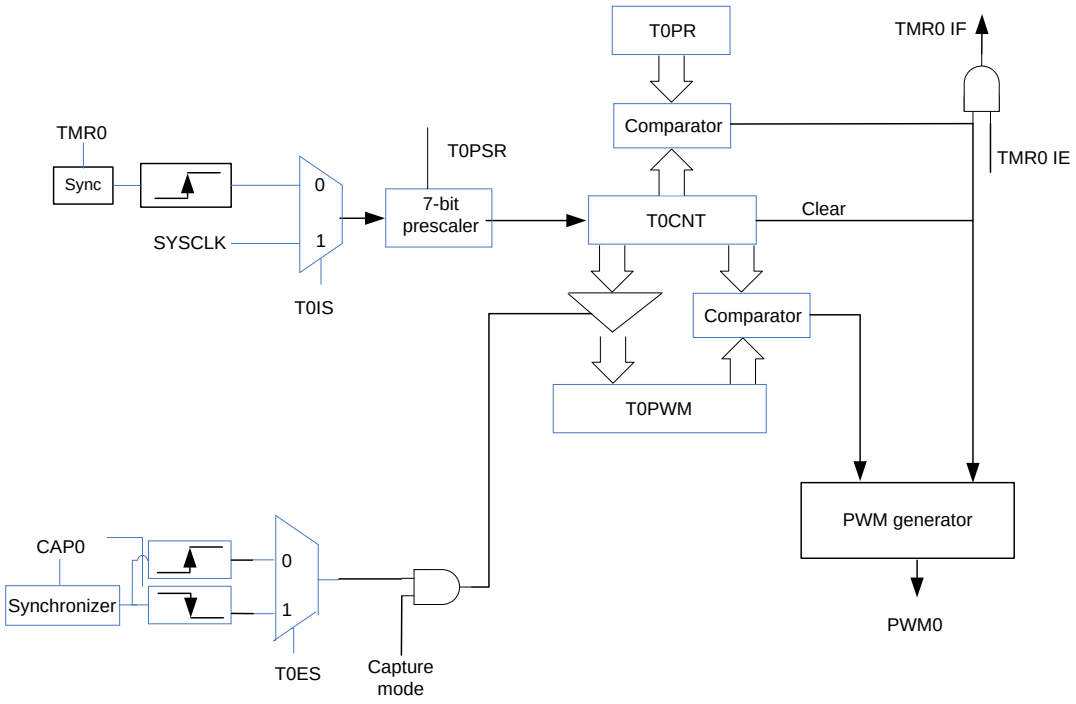


Figure 7-1 Block diagram of Multi-function Timers

Multi-function Timers can be configured to Timer-mode, Counter-mode, Capture-mode and PWM-mode. Each Timer has its Counter input, Capture input and PWM output. The following table shows the corresponding pin settings.

Register 7-1 TMRxCON: Timer Configure Register (x=0,1,2,3,4)

Bit	Name	Mode	Default	Description
31:14	reserved	reserved	reserved	reserved
13	TIE	RW	0	Overflow Interrupt Enable 0 = inactive 1 = active
12	CIE	RW	0	Capture Interrupt Enable 0 = inactive 1 = active
10:8	PSR[2:0]	RW	0	Timer Prescaler 000 = Timer counts at every counting source event 001 = Timer counts at every 2 counting source events 010 = Timer counts at every 4 counting source events 011 = Timer counts at every 8 counting source events 100 = Timer counts at every 16 counting source events 101 = Timer counts at every 32 counting source events 110 = Timer counts at every 64 counting source events 111 = Timer counts at every 128 counting source events
7:6	EDSEL[1:0]	RW	0	Timer Capture Edge Select 00 = CAP Rising Edge 01 = CAP Falling Edge 10/11 = CAP Rising Edge and Falling Edge

Bit	Name	Mode	Default	Description
5:4	Mode[1:0]	RW	0	Timer Mode Select 00 = Timer is disabled 01 = Timer is enabled and works in Counter Mode 10 = Timer is enabled and works in PWM Mode 11 = Timer is enabled and works in Capture Mode
3	CPSEL	RW	0	Capture input selection 0 = Normal timer capture PIN 1 = Supper IO compare output Note：Only in timer0 valid，this bit in timer1/2/3 is invalid
2:0	ISEL[2:0]	RW	0	Increase input selection 000 /010/011 = System Clock 001 = Counter input edge 100 = Counter input Rising 101 = Counter input falling 110 = Reserve 111 = Reserve

Register 7-2 TMRxPND: Timer Pending Register (x=0,1,2,3,4)

Bit	Name	Mode	Default	Description
31:2	reserved	reserved	reserved	reserved
1	OVPND	R	0	Overflow Pending 0 = Not Pending 1 = Pending
0	CPPND	R	0	Capture Pending 0 = Not Pending 1 = Pending

Register 7-3 TMRxCPND: Timer Clear Pending Register(x=0,1,2,3,4)

Bit	Name	Mode	Default	Description
31:2	reserved	reserved	reserved	reserved
1	CLROV	W	0	Clear Overflow Pending 0 = inactive 1 = active
0	CLRCP	W	0	Clear Capture Pending 0 = inactive 1 = active

Register 7-4 TMRxCNT: Timer Counter Register(x=0,1,2,3,4)

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:0	CNT	RW	15'h0	***Note***: TMRX_CNT will increase in proper condition while timer is enabled. It overflows when TMRX_CNT = TMRX_PR, TMRX_CNT will be clear to 0x0000 when overflow occurs, and the interrupt flag will be set '1' by hardware.

Register 7-5 TMRxPR: Timer Period Register (x=0,1,2,3,4)

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:0	PR	RW	15'hFF	***Note***: The overflow period of the timer is: Tinc-source * T0PSR * (T0PR + 1).

Register 7-6 TMRxPWM: Timer PWM Register (x=0,1,2,3,4)

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:0	PWM	RW	15'hxx	***Note***: TMRX_PWM is reserved in timer/counter mode. In PWM mode, it is used as duty cycle setting. In capture mode, the value of TMRX_CNT

Bit	Name	Mode	Default	Description
				will be captured to TMR0PWM when selected event occurs.

7.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) logic consists of a 20bit Watchdog Timer. The Watchdog Timer is clocked by internal RC oscillator running at 32 KHz. When device resets, the WDT is enabled.

In the default configuration, WDT overflows in 2s. The application program needs to clear WDT counter at least once 2 s to prevent WDT time out. The lower 3 bits of the WDTCON register control the selection of overflow time period.

7.2.1 Watchdog Wake up

WDT can be used to wake up AX3153A from Idle, Hold or Sleep mode. RSTEN bit is used to determine the actions after WDT wake up. When RSTEN sets to 0, the watchdog will generate a non-reset wake up after counter overflows. And When RSTEN sets to 1, the watchdog will wake up AX3153A by resetting the whole chip. After non-reset wake up AX3153A will continue to execute next instruction.

During Idle mode, AX3153A can be wake up by WDT with interrupt or reset.

During Hold mode, AX3153A can be wakeup by WDT with interrupt or reset or just continue to execute the next instruction.

During Sleep mode, AX3153A can be wakeup by WDT with reset.

7.2.2 Watchdog SFR

Register 7-7 WDTCON: Watchdog Configure Register

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:8	CLRWDT	w	8'hxx	Clear watchdog 8'h55:clear watchdog, WDTPD and WDTTO will also be clear; Others:not clear watchdog
7	WDTPD	R	0	0 = read '0' before sleep operation 1 = read '1' after sleep operation
6	WDTTO	R	0	0 = Read '0' after clear Watchdog or Power up 1 = Read '1' after Watchdog time out
5	reserved	reserved	reserved	reserved
4	WDTEN	R	0	0 = Disables the Watchdog timer 1 = Enables the Watchdog timer
3	RSTEN	R	0	0 = Disables the Watchdog reset 1 = Enables the Watchdog reset
2:0	WDTPS	R/W	3'h5	WDT time out period setting 000 = 2ms 001 = 8ms 010 = 32ms 011 = 128ms 100 = 512ms 101 = 2048ms 110 = 8192ms 111 = 32768ms

Register 7-8 WDTCON1: Watchdog Configure Register 1

Bit	Name	Mode	Default	Description
31:16	WDTRSTEN	W	16'h5555	16'haaaa = Disables the Watchdog reset others= Enables the Watchdog reset
15:0	WDTEN	W	16'h5555	16'haaaa = Disables the Watchdog timer others= Enables the Watchdog timer

7.3 Independent Power Real Time Clock Counter (IRTCC)

7.3.1 Overview

IRTCC divides two parts: one part is IRTCC controller in VDDLDO(VDDCORE) power domain; the other part is

RTCC(Real timer clock counter) in VDDRTC power domain. RTCC can only be accessed by IRTCC controller.

7.3.2 IRTCC Controller

IRTCC control can generate two interrupts: interrupt every Second and interrupt with Alarm.

IRTCC second interrupt can be enabled by writing 1 to IRTIE bit. When IRTCC works and IRTIE = 1, IRTCC second interrupt will be generated every 1 second by setting IRTPND to 1. IRTPND can be cleared by software by writing 0 to IRTPND bit.

IRTCC alarm interrupt can be enabled by writing 1 to IRTALIE bit. When IRTCC works and IRTALIE = 1, IRTCC alarm interrupt will be generated when the current time is equal to the pre-set time by setting IRTALPND to 1. IRTALPND can be cleared by software by writing 0 to IRTALPND bit.

7.3.3 IRTCC controller Special Function Register

Register 7-9 IRTCON: IRTCC Configure Register

Bit	Name	Mode	Default	Description
31:15	reserved	reserved	reserved	reserved
14	TSRTC	R/W	0	Test RTC enable 0 = RTC test disable 1 = RTC test enable
13	IRTCSTEN	R/W	0	IRTCC sleep wake up enable 0 = Disable 1 = Enable
12	RTCPOREN	R/W	0	RTCPOREN: IRTCC POR reset system clock enable 0 = Disable 1 = Enable
11	TIMERIE	R/W	0	Timer pending interrupt enable 0 = Disable 1 = Enable
10	IRTALIE	R/W	0	IRTCC alarm interrupt enable 0 = Disable 1 = Enable IRTALIE must be ‘1’ if IRTCC alarm is used to wake up system.
9	IRTIE	R/W	0	IRTCC second interrupt enable 0 = Disable 1 = Enable IRTIE must be ‘1’ if IRTCC second is used to wake up system.
8	CSEN	R/W	0	IRTCC communications enable 0 = Disable 1 = Enable
7:5	reserved	reserved	reserved	reserved
4	RTCPOR	R	0	RTCC POR bit 0 : RTCC POR be 0 1 : RTCC POR be 1 NOTE : only design specification can be known.
3	DONE	R	0	Communication done flag 0 = done 1 = not done
2	TMRPND	R	0	Timer pending 0 = No pending (Write 0 to clear pending) 1 = When SECCNT equal to internal counter
1	ALPND	R	0	IRTCC alarm pending 0 = No pending (Write 0 to clear pending) 1 = Pending
0	SECPND	R	0	IRTCC second pending 0 = No pending (Write 0 to clear pending) 1 = Pending

Register 7-10 IRTCPND: IRTCC Clear Pending Register

Bit	Name	Mode	Default	Description
31:3	reserved	reserved	reserved	reserved
2	CTMRPND	W	0	Clear IRTCC timer Pending 0 = inactive 1 = active
1	CALPND	W	0	Clear alarm Pending 0 = inactive 1 = active
0	CSECPND	W	0	Clear second Pending 0 = inactive 1 = active

Register 7-11 IRTDATA: IRTCC Communication Data Register

Bit	Name	Mode	Default	Description
31:3	reserved	reserved	reserved	reserved
7:0	IRTDATA	WR	0	Write to IRTCDAT will start IRTCC communication and set DONE flag to 1. Read IRTCDAT will return IRTCC data.

Register 7-12 IRTSECCNT: IRTCC Timer Counter Register

Bit	Name	Mode	Default	Description
31:8	reserved	reserved	reserved	reserved
7:0	IRT_SECCNT	WR	x	RTCC second counter

7.3.4 IRTCC Operating Guide

1. Write Data to RTC register

1) Enable CS (IRCCON.8)
2) Write command to IRCDATA register
3) Wait for transmission done (IRTCON.3)
4) Write data to IRTDATA register
5) Wait for transmission done (IRTCFG.3); If send more than one data, please repeat steps 4 and 5
6) Disable CS (IRTCON.8)

2. Read Data from RTC register

1) Enable CS (IRTCON.8)
2) Write command to IRTDATA register
3) Wait for transmission done (IRTCON.3)
4) Write “0x00” to IRTDATA register
5) Wait for transmission done (IRTCON.3)
6) Read data from IRTDATA; If read more than one data, please repeat steps 4, 5 and 6
7) Disable CS (IRTCON.8)

7.3.5 RTCC Timer

RTCC timer can be power independently. It can work even other logic in AX3153A is power off.

There is 6-bit valid address for the 64-byte user RAM. So the upper 2-bit of address in the writing RTC_RAM or reading RTC_RAM command are ignored. After one byte write/read, the internal address can increase automatically, this characteristic provide a burst mode to write/read the RAM. If the internal addresses increase greater than 63, it will roll back to 0.

7.3.6 Communication with IRTCC Timer

Special commands and corresponding parameters are used to communicate with IRTCC timer internal control or status registers and SRAM.

Table 9-7-1 IRTCC components communication commands

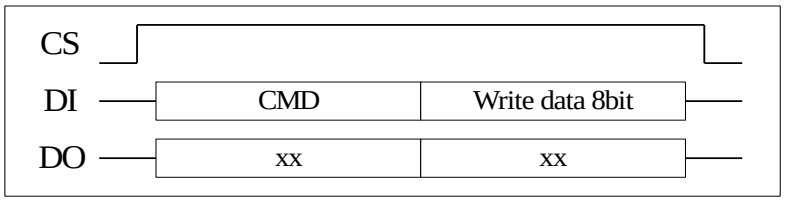
IRTCC component	Component type	Operation	Command Code	Command Parameters
Write_CFG(RTCCON)	A	Write	0x55	One byte

IRTCC component	Component type	Operation	Command Code	Command Parameters
Read_CFG(RTCCON)	A	Read	0x54	One byte
Write_CFG(RTCCON1)	A	Write	0x90	One byte
Read_CFG(RTCCON1)	A	Read	0x91	One byte
Write_ CFG(RTCDSL)	A	Write	0x59	One byte
Write_RTC	B	Write	0xF0	Four byte
Read_RTC	B	Read	0xE0	Four byte
Write_ALM	B	Write	0x53	Four byte
Read_ALM	B	Read	0x52	Four byte
Write_RAM	C	Write	0x57	One byte address and N byte data
Read_RAM	C	Read	0x56	One byte address and N byte data
Write_PWR(PWRCON)	A	Read	0x5a	One byte
Write_WKO(WKOCON)	A	Write	0x5b	One byte
Read_WKO(WKOCON)	A	Read	0xa1	One byte
Write_VCL(VOLTAGE)	A	Write	0xa2	One byte
Read_VCL(VOLTAGE)	A	Read	0xa3	One byte
Read_PWR(PWRCON)	A	Read	0x65	One byte
Write_STA(WKSTA)	A	Write	0x63	One byte
Read_STA(WKSTA)	A	Read	0x62	One byte

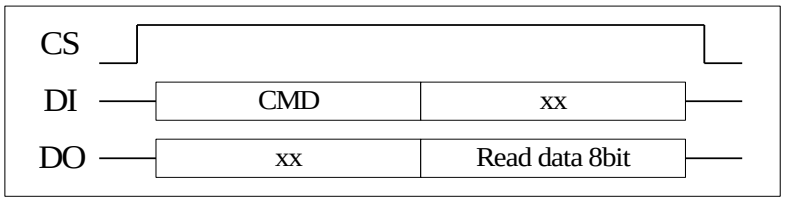
Communication operations:

1, Read or write A type components

Write:

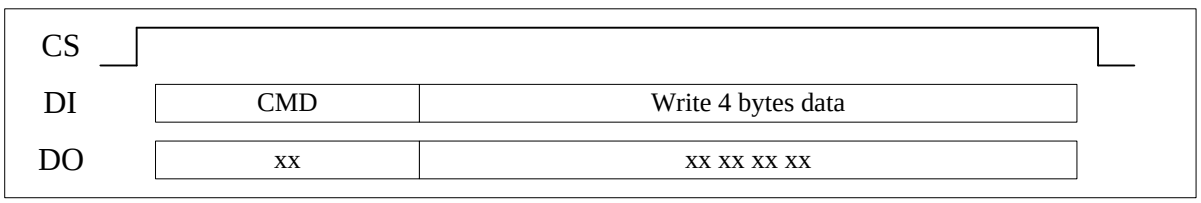


Read:

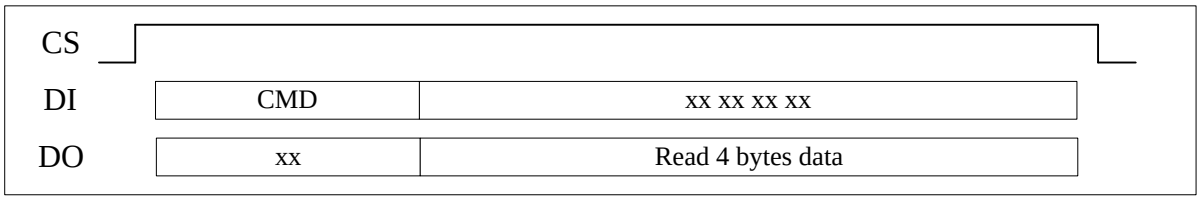


2, Read or write B type components

Write:

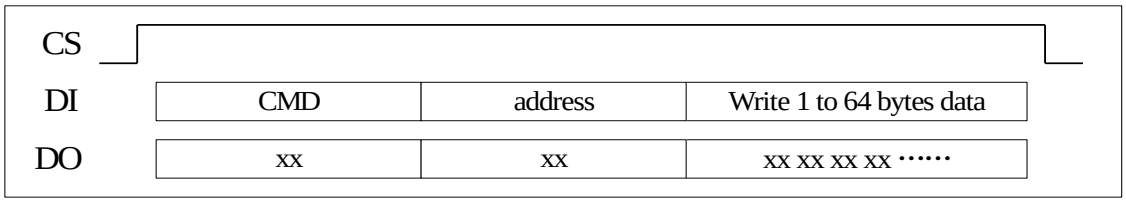


Read:

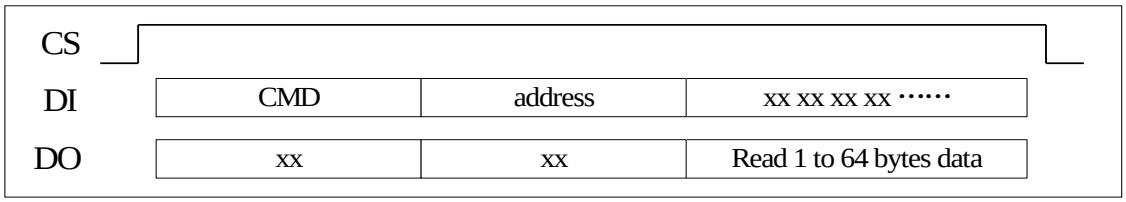


3, Read or write C type components

Write:



Read:



7.3.7 IRTCC components description

Register 7-13 RTCCON RTCC control

Position	7	6	5	4	3	2	1	0
Name	32K_EN	12M_EN	WKUP_POR_EN	WKO_CIN	F1HZEN	F32KHZEN	EX32KSEL	WKO32KOUT
Default	0	0	0	x	1	1	0	0
Access	R/W	R/W	R/W	RO	R/W	R/W	R/W	R/W

32K_EN : XOSC32k enable

0 = Disable

1 = Enable

12M_EN : XOSC12m enable

0 = Disable

1 = Enable

WKUP_POR_EN: wakeup power on reset enable bit
0: disable
1: enable

WKO_CIN: WKO pin state

0: low state
1: high state

F1HZEN: 1Hz signal output enable

0 = Disable

1 = Enable

F32KHZEN: 32KHz signal output enable

0 = Disable

1 = Enable

EX32KSEL: RTCC timer clock source select

0 = RTCC timer works with XOSC 32K.

1 = RTCC timer works with IRTOSC 32KHz

WKO32KOUT: WKO output RTC analog 32K XOSC

0 = Disable

1 = Enable

Register 7-14 WKOCON - WKO configure register

Position	7	6	5	4	3	2	1	0
Name	WKPIN_STA	FLTEN	ALMOE	WKOEN	WKOUTEN	WKOINEN	ALMEN	TSMD
Default	0	0	0	0	0	0	0	0
Access	R/W	W/R	W/R	W/R	W/R	W/R	R/W	R/W

WKPIN_STA: Wake up pin output state

0 = wake up pin output 0

1 = wake up pin output 1

FITEN: WKO 1ms filter enable

0 = disable

1 = enable

ALMOE: Alarm output enable at WKO PIN output enable
0 = Disable
1 = Enable
WKOEN: WKO PIN enable

0 = Disable

1 = Enabled

WKOUTEN: WKO PIN output enable bit
0 = Disable

1 = Enabled

WKOINEN: WKO PIN input enable bit
0 = Disable

1 = Enabled

ALMEN: Alarm function enable

0 = Disable

1 = Enable

TSMD: 1-pin XOSC TEST mode enable
0 = disable
1 = enable

Register 7-15 VCL VOLTAGE - VCL VOLTAGE control register

Position	7	6	5	4	3	2	1	0
Name	SC_RTC[4]	SC_RTC[3]	SC_RTC[2]	SC_RTC[1]	SC_RTC[0]	HVDS/ VDDIO_EN	HVDEN	LVDEN
Default	1	1	0	1	0	0	0	0
Access	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

SC_RTC [4]: OSCO OSCI capacitance select
SC_RTC [3:2]: OSCO capacitance select
SC_RTC [1:0]: OSCI capacitance select
HVDS/ VDDIO_EN:
When write this bit, will write HVDS. HVD level select
0 = 4.0V
1 = 4.2V
When read this bit, will read VDDIO_EN
HVDEN: HVD enable bit

0 = Disabled
1 = Enabled
LVDEN: LVD enable bit
0 = Disabled
1 = Enabled

Register 7-16 PWRCON - Power control register

Position	7	6	5	4	3	2	1	0
Name	-	-	-	-	-		PDFLAG	LDO_EN
Default	-	-	-	-	-		1	1
Access	-	-	-	-	-		R/W	R/W

PD_FLAG: Power down flag

LDO_EN: LDO enable bit

0: enable

1: disable

Register 7-17 WKSTA - Wake up status register

Position	7	6	5	4	3	2	1	0
Name				HVDS	HVDR	LVDPND	WKOPND	ALMOT
Default	x	x	x	0	1	0	0	0
Access	R/W	R/W	R/W	R	R	R/W	R	R

HVDS: HVD level select
0 = 4.0V
1 = 4.2V
HVDR: HVD flag

0: VDDLDO is no higher than configuration

1: VDDLDO is higher than configuration

LVDPND: LVD pending

0: VDDLDO is higher than 2V

1: VDDLDO is lower than 2V

Write this bit 0 will clear LVDPND

WKOPND: IRTWKO wake up pending

0: No wakeup

1: IRTWKO pin wake up pending

ALMOT: Alarm match flag.

0 = No alarm match happen

1 = Alarm match

Register 7-18 RTCCON1: RTCC control register 1

Position	7	6	5	4	3	2	1	0
Name	LDOENRTC							
Default	0	1	0	1	0	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LDOENRTC: LDO enable by RTC control enable

0 = Disable

1 = Enable

8 SARADC

8.1 SARAD0 Register Description

Register 8-1 HAUXADKACON0: HAUX ADKEY function configuration Register

Bit	Name	Mode	Default	Description
31:2	reserved	reserved	reserved	reserved
1:0	HAUXCON	WR	0	00: HAUX ADKEY channel HAUX0L enable. 01: HAUX ADKEY channel HAUX0R enable. 10: HAUX ADKEY channel HAUX1L enable. 11: HAUX ADKEY channel HAUX1R enable.

Register 8-2 ADCCON: SARADC configuration Register

Bit	Name	Mode	Default	Description
31:12	reserved	reserved	reserved	reserved
11:8	ADCSEL_SH	WR	0	ADCSEL shadow
7	BGOE	WR	0	Bangap output enable 0 = disable 1 = enable
6	AUTOSW	WR	0	Auto channel switching mode 0 = Not switch 1 = Auto load ADCSEL_SH into ADCSEL after conversion completes
5	TMREN	WR	0	ADC Timer kick start enable. Only support timer3. 0 = Disable 1 = Enable
4	ADCEN	WR	0	ADC Module Enable 0 = Disable ADC 1 = Enable ADC
3:0	ADCSEL	WR	0	ADC channel selection 0000 = PA2 0001 = PA3 0010 = PA4 0011 = PA5 0100 = PA6 0101 = ADKEY_OUT 0110 = PB4 0111 = PB5 1000 = PB6 1001 = PB7 1010 = PF0 1011 = PF1

Register 8-3 ADCPND: SARADC pending Register

Bit	Name	Mode	Default	Description
0	ADCGO	WR	0	ADCGO when write: 0 = N/A 1 = start conversion when read: 0 = convert end 1 = ADC running

Register 8-4 ADCBAUD: SARADC Baud Rate Divider Register

Bit	Name	Mode	Default	Description
31:7	reserved	reserved	reserved	reserved

Bit	Name	Mode	Default	Description
6:0	ADC BAUD	W	X	ADCBAUD controls ADC clock frequency, which can be derived by: $f_{ADC} = x = \frac{f_{sys}}{2x(ADCBAUD+1)}$ One ADC conversion can be completed in 13 ADC clock cycles. 0 – 255

Register 8-5 ADCDATA: SARADC DATA Register

Bit	Name	Mode	Default	Description
31:10	reserved	reserved	reserved	reserved
9:0	ADCDATA	R	X	ADC DATA

8.2 SARAD1 Register Description

Register 8-6 ADC1CON: SARADC1 configuration Register

Bit	Name	Mode	Default	Description
31:12	reserved	reserved	reserved	reserved
11:8	ADCSEL_SH	WR	0	ADCSEL shadow
7	BGOE	WR	0	Bangap output enable 0 = disable 1 = enable
6	AUTOSW	WR	0	Auto channel switching mode 0 = Not switch 1 = Auto load ADCSEL_SH into ADCSEL after conversion completes
5	TMREN	WR	0	ADC Timer kick start enable. Only support timer2 0 = Disable 1 = Enable
4	ADCEN	WR	0	ADC Module Enable 0 = Disable ADC 1 = Enable ADC
3:0	ADCSEL	WR	0	ADC1 channel selection 0000 = PF2 0001 = PF3 0010 = PF4 0011 = PF5 0100 = PF6 0101 = PF7 0110 = PG0 0111 = PN0 1000 = PN1 1001 = PN2 1010 = VBG 1011 = MVOUT

Register 8-7 ADC1PND: SARADC1 pending Register

Bit	Name	Mode	Default	Description
31:1	reserved	reserved	reserved	reserved
0	ADCGO	WR	0	ADCGO when write: 0 = N/A 1 = start conversion when read: 0 = convert end 1 = ADC running

Register 8-8 ADC1BAUD: SARADC Baud Rate Divider Register

Bit	Name	Mode	Default	Description
31:7	reserved	reserved	reserved	reserved
6:0	ADCBAUD	W	X	ADCBAUD controls ADC clock frequency, which can be derived by: $f_{ADC} = x = \frac{f_{sys}}{2x(ADCBAUD + 1)}$ One ADC conversion can be completed in 13 ADC clock cycles. 0 – 255

Register 8-9 ADC1DATA: SARADC DATA Register

Bit	Name	Mode	Default	Description
31:10	reserved	reserved	reserved	reserved
9:0	ADCDATA	R	X	ADC DATA

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Part 5 *Interface Peripheral*

9 Universal Asynchronous Receiver/Transmitter (UART)

10 IR receiver

11 SPI

12 I^2C-Master Core

13 IIS_CTL

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9 Universal Asynchronous Receiver/Transmitter (UART)

9.1 UART0/3

9.1.1 Overview

UART is a serial port capable of asynchronous transmission. The UART can function in full duplex mode. Receive data is buffered in a holding register. This allows the UART to start reception of a second incoming data byte before software has finished reading the previous data byte.

9.1.2 IO Mapping

UART0	PMAPCON4[19:16]	0x1	0x2			
	RX	PF3	PF4			
	TX	PF4	PF4			
UART3	PMAPCON4[23:20]	0x1	0x2	0x3	0x4	0x5
	RX	PA5	PA4	PG4	PG5	PE3
	TX	PA4	PA4	PG5	PG5	PE4

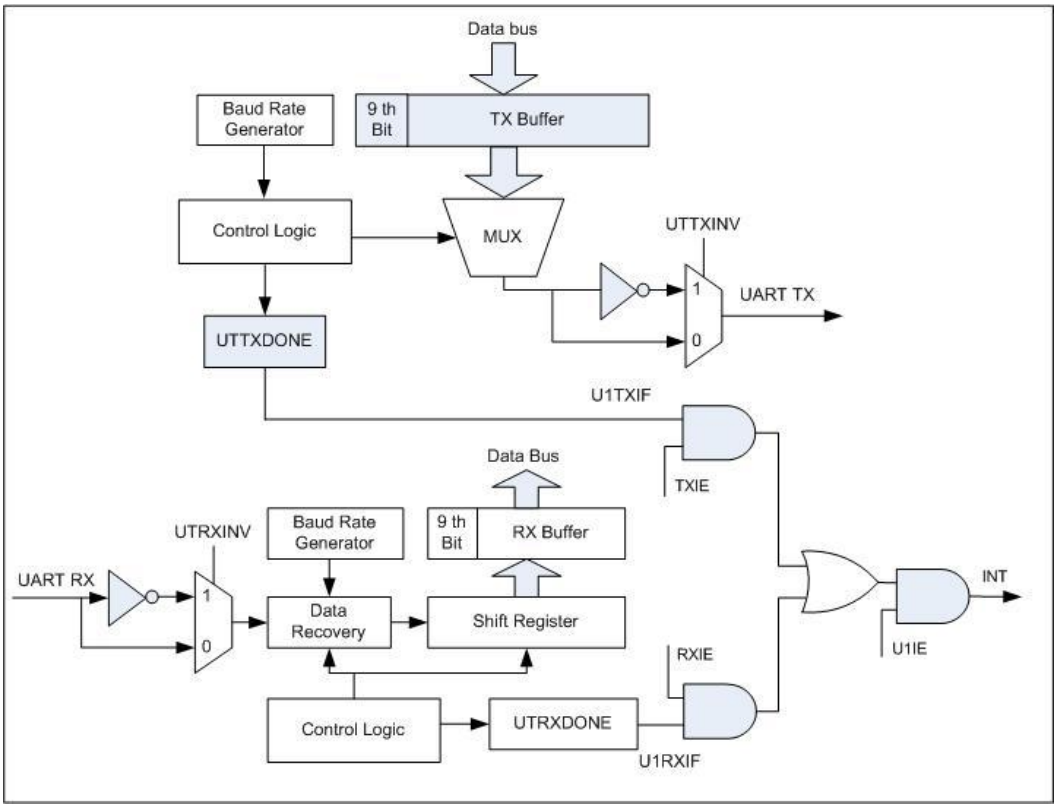


Figure 13-9-1 UART Block Diagram

Register 9-1 UART0/3CON: UART0/3 Configure Register

Bit	Name	Mode	Default	Description
31:8	reserved	reserved	reserved	reserved
7	UTSBS	WR	0	Stop Bit Select 0 = 1 bit as Stop Bit 1 = 2 bits as Stop Bit
6	reserved	reserved	reserved	reserved
5	NBITEN	WR	0	Nine-BIT mode Enable Bit 0 = Eight-bit mode 1 = Nine-bit mode
4	UTEN	WR	0	UART Enable Bit

Bit	Name	Mode	Default	Description
				0 = Disable UART module 1 = Enable UART module
3	UTTXINV	WR	0	Transmit Invert Selection Bit 0 = Transmitter output without inverted 1 = Transmitter output inverted
2	UTRXINV	WR	0	Receive Invert Selection Bit 0 = Receiver input without inverted 1 = Receiver input inverted
1	TXIE	WR	0	Transmit Interrupt Enable 0 = Transmit interrupt disable 1 = Transmit interrupt enable
0	RXIE	WR	0	Receive Interrupt Enable 0 = Receiver interrupt disable 1 = Receiver interrupt enable

Register 9-2 UART0/3PND: UART0/3 pending Register

Bit	Name	Mode	Default	Description
31:3	reserved	reserved	reserved	reserved
2	FEF	R	X	Frame Error Flag 0 = the stop bit is '1' in the last received frame 1 = the stop bit is '0' in the last received frame
1	TXIF	WR	0	UART TX Interrupt Flag: When read: 0 = UART transmit not done 1 = UART transmit done When write: 0 = N/A 1 = Clear TX Pending. Writing data to UTBUF will clear this flag too.
0	RXIF	WR	0	UART RX Interrupt Flag When read: 0 = UART receive not done 1 = UART receive done When write: 0 = N/A 1 = Clear RX Pending

Register 9-3 UART0/3BAUD: UART0/3 Baud Rate Register

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:0	UART0_BAUD	W	0	UART Baud Rate Baud Rate =Fsys clock / (UARTBAUD + 1)

Register 9-4 UART0/3DATA: UART0/3 Data Register

Bit	Name	Mode	Default	Description
31:9	reserved	reserved	reserved	reserved
8:0	UARTDATA	WR	X	UART Data Write this location will load the data to transmitter buffer. And read this location will read the data from the receiver buffer. If UARTDATA[8] is using to translate data, must enable the NBITEN.

9.1.3 UART0/3 Operation Guide

UART0/3 Operation Flow:

1. Set IO in the correct direction.
2. Configure UART0/3BAUD to choose sample rate and baud.
3. Enable UART0/3 by setting UTEN to '1'
4. Set TXIE or RXIE 'to 1' if needed
5. write data to UART0/3DATA

6. Wait for PND to change to ‘1’, or wait for interrupt
7. Read received data from UART0/3DATA if needed
8. Go to Step 5 to start another process if needed or turn off UART0/3 by UTEN.

10 IR receiver

AX3153A provides digital IR receiver, it can receiver IR data then CPU can read IR data from IR data buffer.

10.1 IO Mapping

Table 10-1

Function	Pin(map0)	Pin(map1)	Pin(map2)	Pin(map3)	Pin(map4)
IR RX PIN	PORTB7	PORTD6	PORTF7	PORTG0	PORTN2

10.2 IR frame format

Figure 10-1 shows the IR data frame format

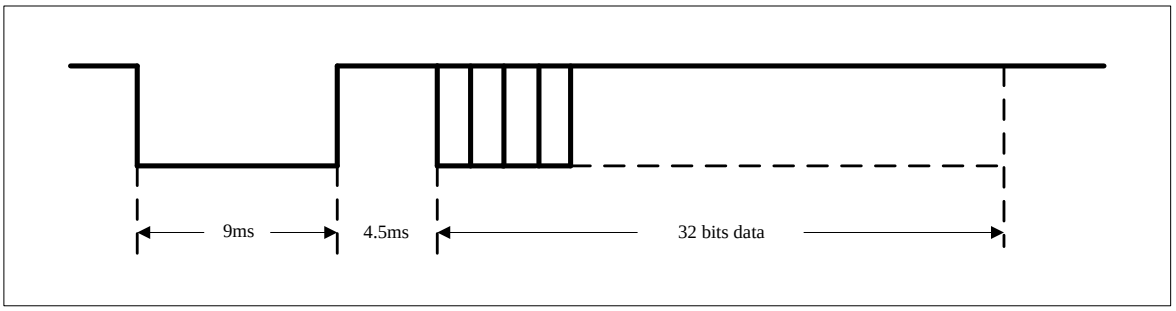


Figure 10-1 IR data frame format

Figure 10-2 shows the IR repeat frame format

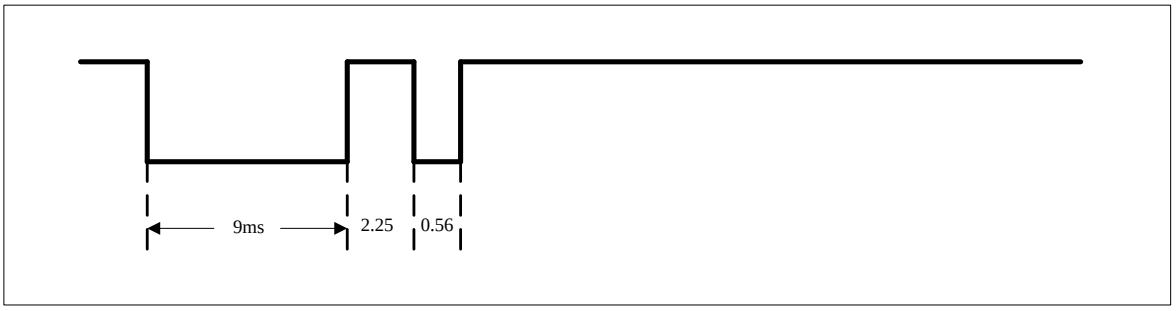


Figure 10-2 IR repeat frame format

Figure 10-3 shows the IR bit 0 and bit 1 format

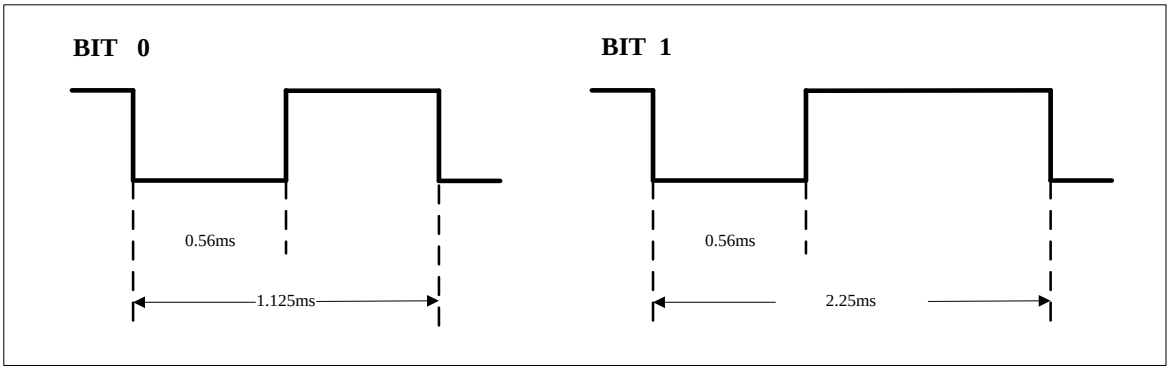


Figure 10-3 IR bit frame format

10.3 IR Receiver Control Registers

Register 10-1 IRRXCON0: IR receiver control register

Bit	Name	Mode	Default	Description
31:8	reserved	reserved	reserved	reserved
7	IR_CLK32K_SEL	WR	0	IR clock is 32k. 0 = IR clock is 1M 1 = IR clock is 32k
6	CIRDATA_ERROR	W	0	Clear IR receiver data error. 0 = not clear 1 = clear IRDATA_ERROR
5	IRDATA_ERROR	R	0	IR receive data error 0 = not error 1 =IR receive data is error
4	CPND	W	0	Clear IR receiver pending 0 = not clear 1 = clear pending
3	IRREPEAT	R	0	IR receiver repeating data 0 = Not repeat 1 = Repeat
2	IRPND	R	0	IR receiver done 0 = Undone 1 = Done
1	IRIE	WR	0	IR interrupt enable 0 = Disabled 1 = Enabled
0	IREN	WR	0	IR enable 0 = Disabled 1 = Enabled

Register 10-2 IRRXSCON: IR receiver start control register

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:8	ENDCNT	WR	8'h4	When IR clock is 1 MHz, (4.5ms*1MHz)/2048=BEGINCNT/2. So,It is recommended to set ENDCONT to 0x04. When IR clock is 32 KHz, (4.5ms*32KHz)/64=ENDCONT/2. So,It is recommended to set ENDCONT to 0x04.
7:0	BEGINCNT	WR	8'h8	When IR clock is 1 MHz: (9ms*1MHz)/2048=BEGINCNT/2. So,It is recommended to set BEGINCNT to 0x08. When IR clock is 32 KHz, (9ms*32KHz)/64=BEGINCNT/2 It is recommended to set BEGINCNT to 0x08.

Register 10-3 IRRXCYCCON: IR receiver data cycle control register

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:8	ONEFULL	WR	8'h9C	ONEFULL is use for calculate the time of IRDATA error. When IR clock is 1 MHz, (2.25ms*1MHz)/16 > ONEFULL So,It is recommended to set ONEFULL to 0x8C. When IR clock is 32 KHz, (2.25ms*32kHz) > ONEFULL So,It is recommended to set ONEFULL to 0x48
7:0	ZEROCYC	WR	8'h50	ZEROCYC is use for calculating the cycle of IR BIT 0 and BIT 1 division. When IR clock is 1 MHz, BIT 0 cycle < ZEROCYC*16 < BIT 1 cycle It is recommended to set ZEROCYC to 0x46. When IR clock is 32 KHz,

Bit	Name	Mode	Default	Description
				BIT 0 cycle < ZEROCYC < BIT 1 cycle It is recommended to set ZEROCYC to 0x24

Register 10-4 IRRXRPTCON: IR receiver repeat e control register

Bit	Name	Mode	Default	Description
31:8	reserved	reserved	reserved	reserved
7:0	REPEAT	WR	8'h04	When IR clock is 1 MHz, REPEATCNT*1024*2*CLKCYC us is the IR repeat pulse (2.3ms). It is recommended to set REPEATCNT to 0x04. When IR clock is 32 KHz, REPEATCNT*32*CLKCYC us is the IR repeat pulse (2.3ms). It is recommended to set REPEATCNT to 0x04.

NOTE: When IR clock is 1 MHz and BEGINCNT or ENDCNT or REPEATCNT is configured to N，BEGINCNT or ENDCNT detect range is N*2048*cycle ~ (N*2048+2047)*cycle, REPEATCNT detect range is N*1024*cycle ~ (N*1024+1023)*cycle

NOTE: When IR clock is 32 KHz and BEGINCNT or ENDCNT or REPEATCNT is configured to N，BEGINCNT or ENDCNT detect range is N*64*cycle ~ (N*64+63)*cycle, REPEATCNT detect range is N*32*cycle ~ (N*32+31)*cycle

Register 10-5 IRRXDATAL - IR receiver data buffer register

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:0	IRDATAL	R	0	IR receiver data buffe lowr register

Register 10-6 IRRXDATAH - IR receiver data buffer register

Bit	Name	Mode	Default	Description
31:16	reserved	reserved	reserved	reserved
15:0	IRDATAH	R	0	IR receiver data buffer high register

IRDATA = {IRDATAH,IRDATAL}

10.4 IR Receiver Operation Guide

1. Configure IR clock ;
2. Configure IRRXSCON and IRRXCYCCON if needed;
3. Configure IRRXRPTCON if needed;
4. Configure IRRXCON0;
5. Wait IRPND or IR interrupt;
6. Read IRDATA.

11 **SPI**

11.1 **SPI0**

AX3153A SPI0 can serve as master or slave. It can operate in normal or DMA mode.

this table is description for SPI0 IO mapping setting.

	PMAPCON5[15:12]	**0x1**	**0x2**
SPI0	SPI0HOLD(IO3)	PE0	PJ2
	SPI0WP(IO2)	PE1	PJ3
	SPI0DI(IO1)	PE2	PJ4
	SPI0CLK	PE3	PJ5
	SPI0DO(IO0)	PE4	PJ6

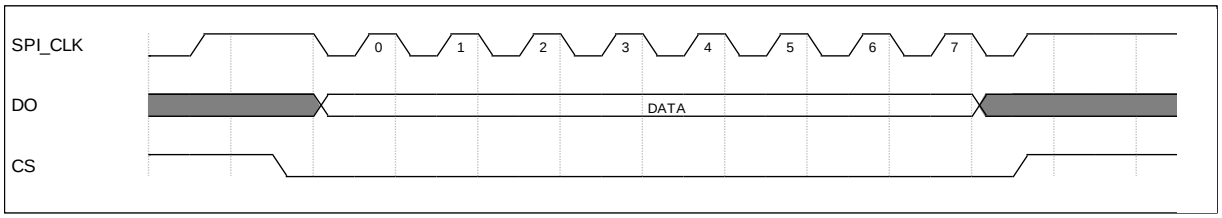


Figure SPI Standard Mode

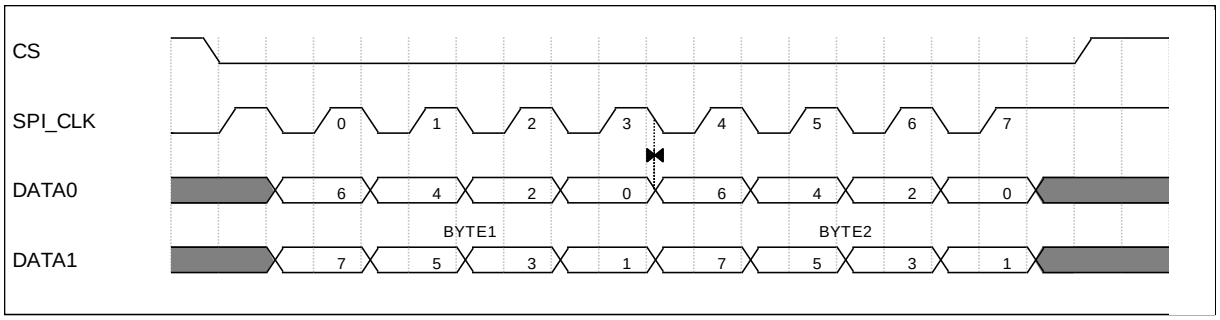


Figure SPI Dual Mode

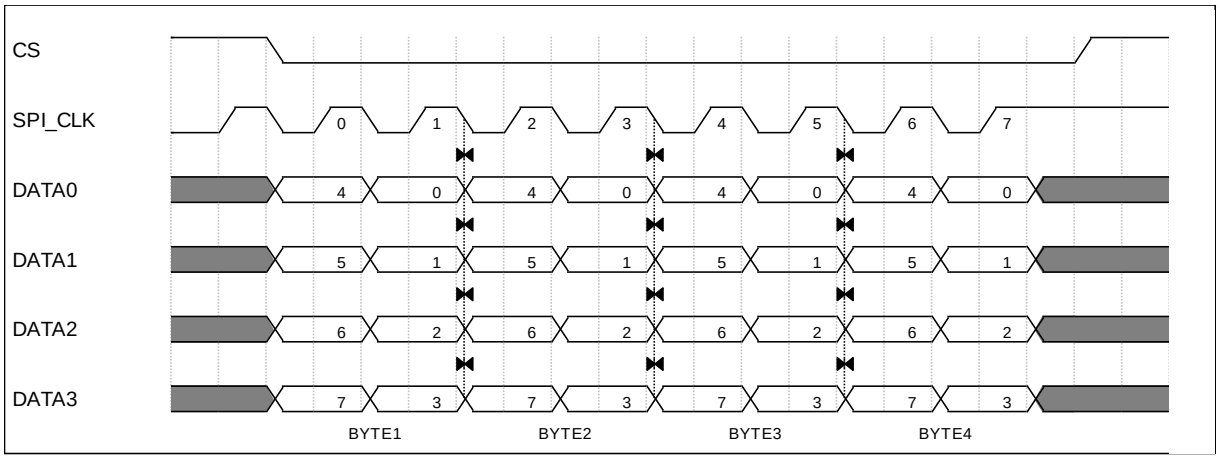


Figure SPI Quad Mode

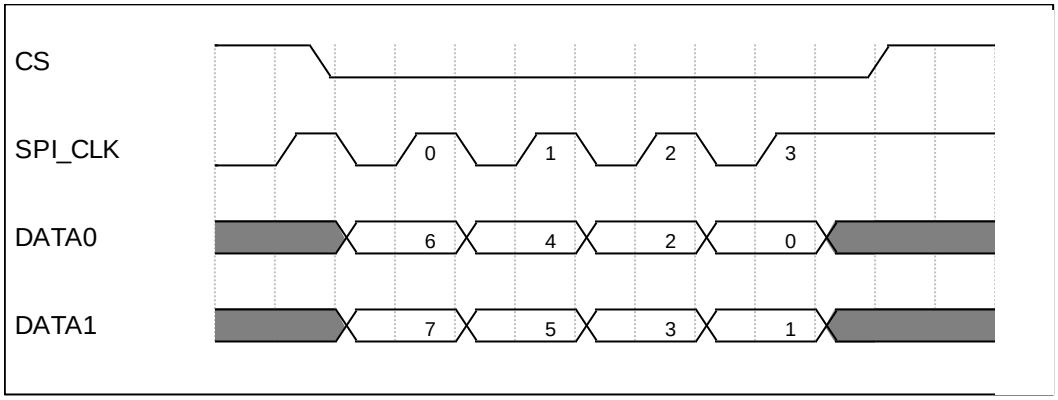


Figure PI Dual Fast Mode

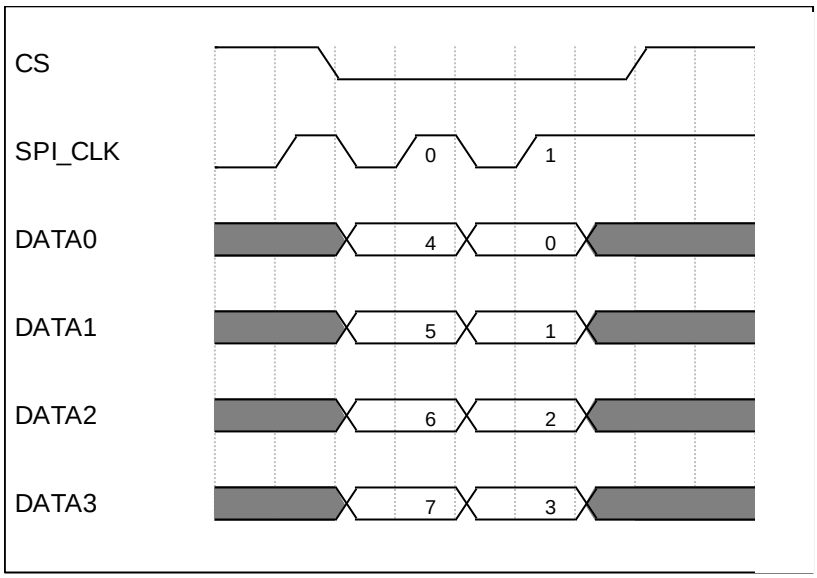


Figure SPI Quad Fast Mode

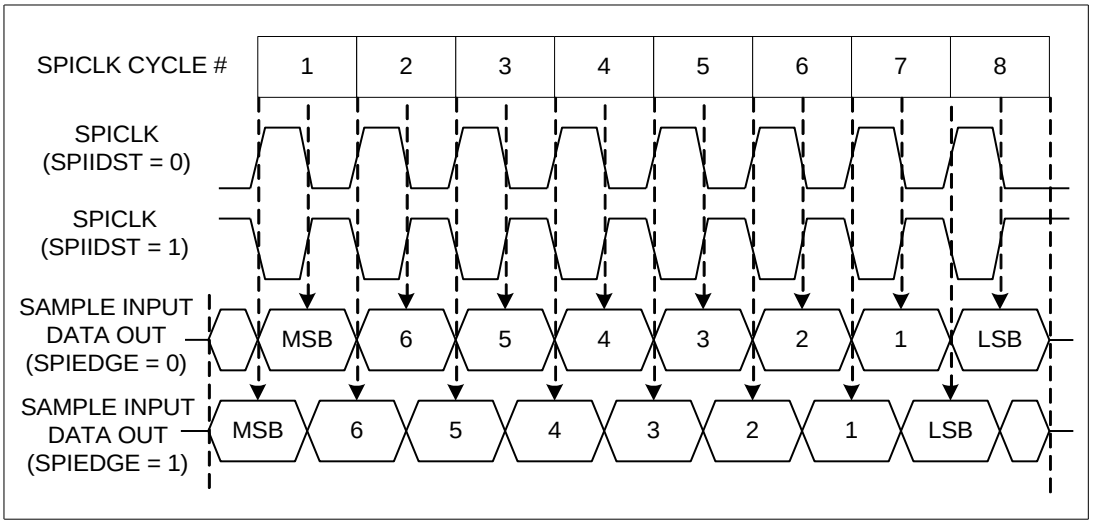


Figure 15-11-1 SPI timing

11.1.1 SPI0 Special Function Registers

Register 11-1 SPI0CON0: SPI control register

Position	8	7	6	5	4	3	2	1	0
Name	SPI_IE	SPIPND	HSMODE	SPIRT	SPIWS	-	SPIEDGE	SPIIDST	SPIEN
Default	0	1	0	0	0	-	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W

SPI_IE: SPI interrupt enalbe bit;

0 = disable

1 = enable

SPIPND: SPI Pending bit (read only, writing SPI0BUF will clear this bit)

0 = Transmission is not finish

1 = Transmission finish

HSMODE: High speed mode (baudrate=0) select bit

0 = Not high speed mode

1 = High speed mode

SPIRT: SPI0RX/TX select bit in 2-wire mode or DMA mode

0 = TX

1 = RX

In 3-wire mode, SPI can both Transmit and receive at the same time. But when using DMA mode or 2-wire mode, just one direction (TX or RX) is allowed. Use this bit to select TX or RX.

SPI0WS: SPI0 2-wire mode/3-wire mode select bit

0 = 3-wire mode

1 = 2-wire mode

SPIEDGE: SPI sampling edge select bit

When SPIIDST = 0:

0 = sample at falling edge

1 = sample at rising edge

When SPIIDST = 1:

0 = sample at rising edge

1 = sample at falling edge

SPIIDST: SPI clock signal idle state

0 = Clock signal stay at 0 when idle

1 = Clock signal stay at 1 when idle

SPIEN: SPI enable bit

0 = SPI disable

1 = SPI enable

Register 11-2 SPI0CON1: SPI control1 register

Position	7	6	5	4	3	2	1	0
Name	-	-	SPI_CRC_EN	FASTTX	ODDDIV	SAMPSEL	DBWIDTH	
Default	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W

SPI_CRC_EN: SPI CRC16 check enable bit

0 = disable

1 = enable

FASTTX: Normal mode fast transmit enable bit(write one byte kick normal transmit when 2-data or 4-data mode)

0 = disable

1 = enable (if not need fast transmit, this bit must keep 0)

ODDDIV: Odd divide frequency enable bit

0 = disable

1 = enable (if not need odd divide frequency, this bit must keep 0)

SAMPSEL: SPI receive sample edge select bit

0 = sample data at first edge

1 = sample data at second edge (Not supported in high speed mode)

DBWIDTH: Data bus width select bit

00 = 1bit bidirectional data bus (2-wire mode),or 3-wire mode 1bit data bus

01 = 2bit bidirectional data bus

10/11 = 4bit bidirectional data bus

Register 11-3 SPI0BAUD: SPI Baud Rate register

Position	7	6	5	4	3	2	1	0
Name	-	-	-	-	SPIBAUD			
Default	-	-	-	-	x	x	x	x
Access	-	-	-	-	WO	WO	WO	WO

Note: SPI_CLK = system_clk/ ((SPIBAUD+1)*2), when odd_div =0;

SPI_CLK = system_clk/ (SPIBAUD+1), when odd_div =1, but SPIBAUD must great than 2;

Register 11-4 SPI0BUF: SPI Data Buffer register

Position	7	6	5	4	3	2	1	0
Name	SPIBUF							
Default	x	x	x	x	x	x	x	x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 11-5 SPI0DMACNT: SPI DMA counter register

Position	19	18	.....	.....	.....	.....	1	0
Name	SPIDMACNT							
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Nbyte = Nunit * 4 = (SPIDMACNT + 1) * 4

Register 11-6 SPI0DMASP: SPI DMA address pointer register

Position	15	.....	0
Name	SPIDMASP		
Default	x	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

NOTE: SPI0_DMASP is word address,or physical address!

11.1.2 SPI0 Operation Guide

SPI Normal 1bit-Mode Operation Flow:

1. Set 3-wire mdoe or 2-wire mode and select the pin map
2. Select SPIRT for Transmit or receive
3. Configure clock frequency
4. Select one of the four timing mode
5. Enable SPI module by setting SPIEN ‘1’
6. Set SPIIE ‘1’ if needed
7. Write data to SPIBUF to kick-start the process
8. Wait for SPIPND to change to ‘1’, or wait for interrupt
9. Read received data from SPIBUF if needed
10. Go to Step 8 to start another process if needed or turn off SPI0by clearing SPIIE and SPIEN

SPI Normal multi-bit-Mode Operation Flow:

1. Set data bus width(bus4 or bus 2) and select the pin map
2. Select SPIRT for Transmit or receive
3. Configure clock frequency
4. Select one of the four timing mode (refer to Figure 16-1)
5. Enable SPI module by setting SPIEN ‘1’
6. Set SPIIE ‘1’ if needed
7. Write data to SPIBUF to kick-start the process
8. If data bus width are 2 bit, write SPIBUF twice kick-start the transmission
9. If data bus widths are 4 bit, write SPIBUF four times kick-start the transmission

10. However, when receive data, only need write once to kick-start receive process
11. Wait for SPIPND to change to ‘1’, or wait for interrupt
12. Read received data from SPIBUF if needed
13. if data bus width are 2 bit ,read SPIBUF twice to get received data
14. if data bus width are 4 bit ,read SPIBUF four times to get received data
15. Go to Step 8 to start another process if needed or turn off SPI by clearing SPIIE and SPIEN

SPI0 DMA Mode Operation Flow:

1. Set IO in the correct direction and data width mode.
2. Select SPIRT for DMA direction
3. Configure clock frequency
4. Select one of the four timing modes
5. Enable SPI module by setting SPIEN to ‘1’
6. Set SPIIE ‘1’ if needed
7. configure SPI0DMASP；
8. Write data to SPI0_DMACNT to kick-start a DMA process
9. Wait for SPIPND to change to ‘1’, or wait for interrupt
10. Go to Step 8 to start another DMA process if needed or turn off SPI0 by clearing SPI0EN

11.2 **SPI1**

AX3153A SPI1 can serve as master or slave. It can operate in normal or DMA mode.

	PMAPCON5[19:16]	**0x1**	**0x2**	**0x3**	**0x4**
SPI1	SPI1DO	PG1	PG1	PM0	PM0
	SPI1CLK	PG2	PG2	PM1	PM1
	SPI1DI	PG4	PG1	PM2	PM0

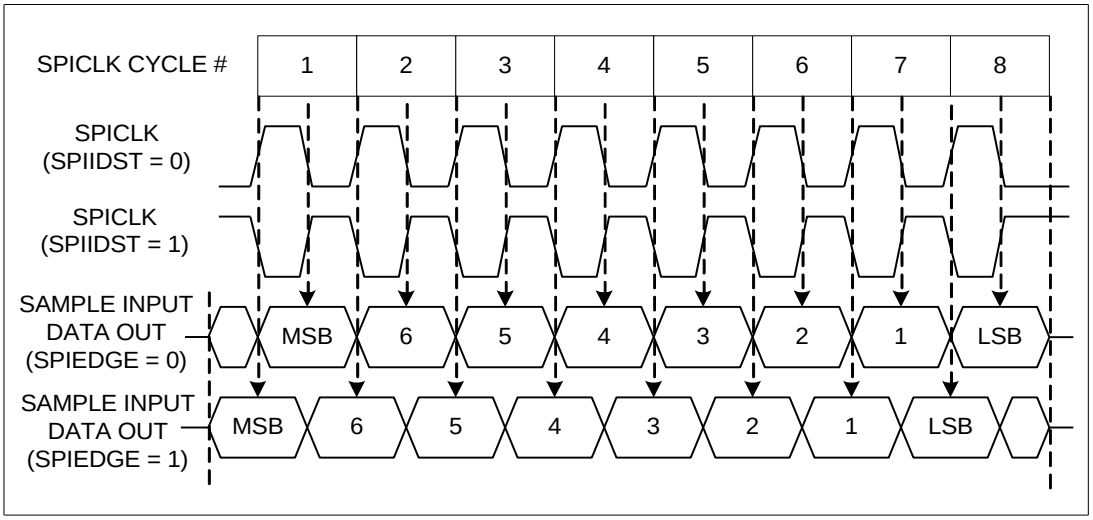


Figure 11-2 SPI timing

11.2.1 SPI1 Special Function Registers

Register 15-7 SPI1CON – SPI1 control

Position	8	7	6	5	4	3	2	1	0
Name	SPI1_IE	SPI1PND	SPI1SM	SPI1RT	SPI1WS	--	SPI1EDGE	SPI1IDST	SPI1EN
Default	0	1	0	0	0	0	0	0	0
Access	RW	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

SPI1_IE: SPI1 interrupt enable bit;

0 = disable

1 = enable

SPI1PND: SPI1 Pending bit (read only, writing SPI1BUF will clear this bit)

0 = Transmission is not finish

1 = Transmission finish

SPI1SM: SPI1 mode selection

0 = Master mode

1 = Slave mode

SPI1RT: SPI1 RX/TX select bit in 2-wire mode or DMA mode

0 = TX

1 = RX

In 3-wire mode, SPI1 can both Transmit and receive at the same time. But when using DMA mode or 2-wire mode, just one direction (TX or RX) is allowed. Use this bit to select TX or RX.

SPI0WS: SPI1 2-wire mode/3-wire mode select bit

0 = 3-wire mode

1 = 2-wire mode

SPI1EDGE: SPI1 sampling edge select bit

When SPI1IDST = 0:

0 = Sample at falling edge

1 = Sample at rising edge

When SPI1IDST = 1:

0 = Sample at rising edge

1 = Sample at falling edge

SPI1IDST: SPI1 clock signal idle state

0 = Clock signal stay at 0 when idle

1 = Clock signal stay at 1 when idle

SPI1EN: SPI1 enable bit

0 = SPI1 disable

1 = SPI1 enable

Register 15-8 SPI1_BAUD – SPI1 Baud Rate

Position	7	6	5	4	3	2	1	0
Name	SPI1_BAUD							
Default	X	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

Baud rate = F_{system_clock} / [2(SPI1_BAUD+1)]

Register 15-9 SPI1_BUF – SPI1 Data Buffer

Position	7	6	5	4	3	2	1	0
Name	SPI1_BUF							
Default	X	x	x	x	x	x	x	X
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register 15-10 SPI1_DMACNT – SPI1 DMA counter

Position	18	.....		0
Name	SPI1_DMACNT			
Default	X	x	x	x	x	x	x	x

Position	18	.....					0
Access	WO	WO	WO	WO	WO	WO	WO	WO

Nunit = SPI1_DMACNT + 1

Nbyte = Nunit * 4 = (SPI1_DMACNT + 1) * 4

Register 15-11 SPI1_DMASP – SPI1 DMA address pointer register

Position	15	.....					0
Name	SPI1_DMASP						
Default	X	x	x	x	x	x	x	x
Access	WO	WO	WO	WO	WO	WO	WO	WO

11.2.2 SPI1 Operation Guide

When SPI1CON1.1=0,

SPI1 Normal Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPI1RT in 2-wire mode if 2-wire mode is selected
3. Select master mode or slave mode
4. Configure clock frequency when master mode is selected in step 3
5. Select one of the four timing mode (refer to *Figure 15-11-1*)
6. Enable SPI1 module by setting SPI1EN '1'
7. Set SPI1IE '1' if needed
8. Write data to SPI1BUF to kick-start the process
9. Wait for SPI1PND to change to '1', or wait for interrupt
10. Read received data from SPI1BUF if needed
11. Go to Step 8 to start another process if needed or turn off SPI1 by clearing SPI1EN

SPI0 DMA Mode Operation Flow:

1. Set IO in the correct direction.
2. Select SPI1RT for DMA direction
3. Select master mode or slave mode
4. Configure clock frequency when master mode is selected in step 3
5. Select one of the four timing modes (refer to *Figure 15-11-1*)
6. Enable SPI1 module by setting SPI1EN to '1'
7. Set SPI1IE '1' if needed
8. configure SPI0DMASP.
9. Write data to SPI1DMACNT to kick-start a DMA process
10. Wait for SPI1PND to change to '1', or wait for interrupt
11. Go to Step 8 to start another DMA process if needed or turn off SPI1 by clearing SPI1EN

12 I²C-Master Core

12.1 Introduction

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

The interface defines 3 transmission speeds:

1. Normal: 100Kbps
2. Fast: 400Kbps
3. High speed: 3.5Mbps

Only 100Kbps and 400Kbps modes are supported directly. For High speed special IOs are needed. If these IOs are available and used, then High speed is also supported.

The I2C interface uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. Both lines must be pulled-up to VCC by external resistors.

The tri-state buffers for the SCL and SDA lines must be added at a higher hierarchical level. Connections should be made according to the following figure:

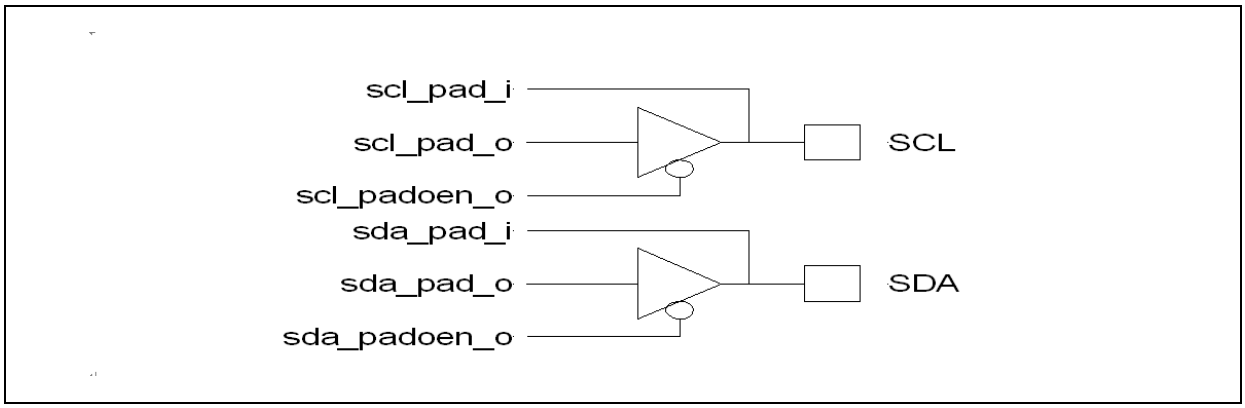


Figure 12-1

12.2 IO Mapping

Table 12-1 I2C_MAP = 1

Function	Pin
SCL	PB4
SDA	PB0

Table 12-2 I2C_MAP = 2

Function	Pin
SCL	PE0
SDA	PE1

Table 12-3 I2C_MAP = 3

Function	Pin
SCL	PG3
SDA	PG1

Table 12-4 I2C_MAP = 4

Function	Pin
SCL	PK5
SDA	PK4

Pre-scale Register

This register is used to pre-scale the SCL clock line. Due to the structure of the I^2C interface, the core uses a 5*SCL clock internally. The pre-scale register must be programmed to this 5*SCL frequency (minus 1). Change the value of the pre-scale register only when the ‘EN’ bit is cleared.

Example: IIC module clock(system clock) = 32MHz, desired SCL = 100KHz

$$\text{prescale} = \frac{32\text{MHz}}{5 * 100\text{KHz}} - 1 = 63(\text{dec}) = 3\text{F}(\text{hex})$$

Register 12-1 I2CPRER - Clock Pre-scale register

Bit	Name	Mode	Default	Description
31:16	reserved	WR	0	Reserved
15:0	FRER	WR	16’hFF	Clock Pre-scale register

Control register

The core responds to new commands only when the ‘EN’ bit is set. Pending commands are finished. Clear the ‘EN’ bit only when no transfer is in progress, i.e. after a STOP command, or when the command register has the STO bit set. When halted during a transfer, the core can hang the I2C bus.

Register 12-2 I2CCON - Control register

Bit	Name	Mode	Default	Description
31:8	Reserved	WR	0	Reserved
7	EN	WR	0	EN, I2C core enable bit. 0 = disable 1 = enable
6	IEN	WR	0	I2C core interrupt enable bit 0 = disable 1 = enable
5:0	reserved	WR	0	Reserved

Transmit register

Register 12-3 I2CTX - Transmit register

Bit	Name	Mode	Default	Description
31:8	Reserved	W	0	Reserved
7:1	TXR	W	0	Next byte to transmit via I2C
0	DIR	W	0	In case of a data transfer this bit represent the data’s LSB. In case of a slave address transfer this bit represents the RW bit. 1 = reading from slave 0 = writing to slave

Receive register

Register 12-4 I2CRCV - Receive register

Bit	Name	Mode	Default	Description
31:8	Reserved	R	0	Reserved
7:0	RXR	R	0	Last byte received via I2C

Command register

The STA, STO, RD, WR, and IACK bits are cleared automatically. These bits are always read as zeros.

Register 12-5 I2CCMD - Command register

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	0	Reserved
7	STA	W	0	generate (repeated) start condition
6	STO	W	0	generate stop condition
5	RD	W	0	Read from slave
4	WR	W	0	Write to slave

Bit	Name	Mode	Default	Description
3	ACK	W	0	when a receiver, sent ACK (ACK = ‘0’) or NACK (ACK = ‘1’)
2:1	Reserved	Reserved	0	Reserved
0	IACK		0	Interrupt acknowledge. When set, clears a pending interrupt.

Status register

Register 12-6 I2CSTA - Status register

Bit	Name	Mode	Default	Description
31:8	Reserved	Reserved	0	Reserved
7	RxACK	R	0	RxACK, Received acknowledge from slave. This flag represents acknowledge from the addressed slave. 1 = No acknowledge received 0 = Acknowledge received
6	Busy	R	0	Busy, I2C bus busy 1 = after START signal detected 0 = after STOP signal detected
5	AL	R	0	AL, Arbitration lost This bit is set when the core lost arbitration. Arbitration is lost when: a STOP signal is detected, but non requested The master drives SDA high, but SDA is low. See bus-arbitration section for more information.
4:2	Reserved	Reserved	0	Reserved
1	TIP	R	0	TIP, Transfer in progress. 1 = when transferring data 0 = when transfer complete
0	IF	R	0	IF, Interrupt Flag. This bit is set when an interrupt is pending, which will cause a processor interrupt request if the IEN bit is set. The Interrupt Flag is set when: one byte transfer has been completed arbitration is lost

12.3 System Configuration

The I2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistor.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (see START and STOP signals).

12.4 I^2C Protocol

Normally, a standard communication consists of four parts:

1. START signal generation
2. Slave address transfer
3. Data transfer
4. STOP signal generation

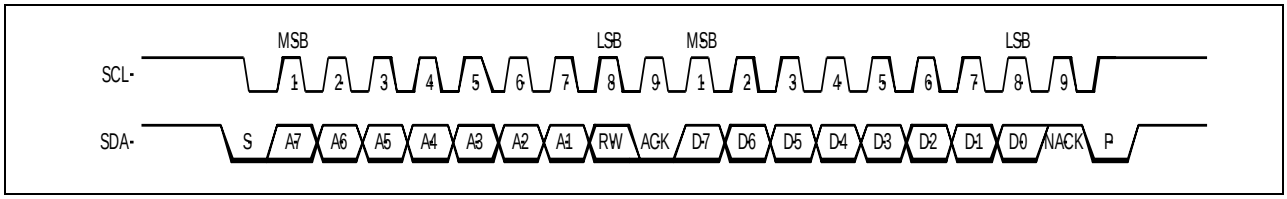


Figure 12-2

START signal

When the bus is free/idle, meaning no master device is engaging the bus (both SCL and SDA lines are high), a

master can initiate a transfer by sending a START signal. A START signal, usually referred to as the S-bit, is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.

A Repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus.

The core generates a START signal when the STA-bit in the Command Register is set and the RD or WR bits are set. Depending on the current status of the SCL line, a START or Repeated START is generated.

Slave Address Transfer

The first byte of data transferred by the master immediately after the START signal is the slave address. This is a seven-bits calling address followed by a RW bit. The RW bit signals the slave the data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

Note: The core supports 10bit slave addresses by generating two address transfers. See the Philips I2C specifications for more details.

The core treats a Slave Address Transfer as any other write action. Store the slave device's address in the Transmit Register and set the WR bit. The core will then transfer the slave address on the bus.

Data Transfer

Once successful slave addressing has been achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge, the master can generate a STOP signal to abort the data transfer or generate a Repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does not acknowledge the slave, the slave releases the SDA line for the master to generate a STOP or Repeated START signal.

To write data to a slave, store the data to be transmitted in the Transmit Register and set the WR bit. To read data from a slave, set the RD bit. During a transfer the core set the TIP flag, indicating that a Transfer is In Progress. When the transfer is done the TIP flag is reset, the IF flag set and, when enabled, an interrupt generated. The Receive Register contains valid data after the IF flag has been set. The user may issue a new write or read command when the TIP flag is reset.

STOP signal

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred to as the P-bit, is defined as a low-to-high transition of SDA while SCL is at logical ‘1’.

12.5 Programming examples

Example 1

Write 1 byte of data to a slave.

Slave address = 0x51 (b”1010001”)

Data to write = 0xAC

I2C Sequence:

1. generate start command
2. write slave address + write bit
3. receive acknowledge from slave
4. write data
5. receive acknowledge from slave
6. generate stop command

Commands:

1. write 0xA2 (address + write bit) to Transmit Register, set STA bit, set WR bit.

-- wait for interrupt or TIP flag to negate --

2. read RxACK bit from Status Register, should be ‘0’.

--write 0xAC to Transmit register, set STO bit, set WR bit.

-- wait for interrupt or TIP flag to negate --

3. read RxACK bit from Status Register, should be ‘0’.

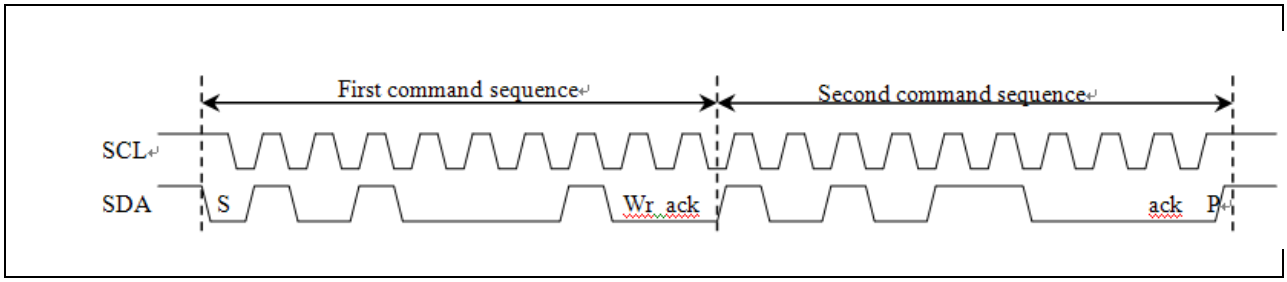


Figure 12-3

Example 2

Read a byte of data from an I2C memory device.

Slave address = 0x4E

Memory location to read from = 0x20

I2C sequence:

1. generate start signal
2. write slave address + write bit
3. receive acknowledge from slave
4. write memory location
5. receive acknowledge from slave
6. generate repeated start signal
7. write slave address + read bit
8. receive acknowledge from slave
9. read byte from slave
10. write no acknowledge (NACK) to slave, indicating end of transfer
11. generate stop signal

Commands:

1. write 0x9C (address + write bit) to Transmit Register, set STA bit, set WR bit.

-- wait for interrupt or TIP flag to negate --

2. read RxACK bit from Status Register, should be ‘0’.

--write 0x20 to Transmit register, set WR bit.

-- wait for interrupt or TIP flag to negate --

3. read RxACK bit from Status Register, should be ‘0’.

--write 0x9D (address + read bit) to Transmit Register, set STA bit, set WR bit.

-- wait for interrupt or TIP flag to negate --

4. set RD bit, set ACK to ‘1’ (NACK), set STO bit.

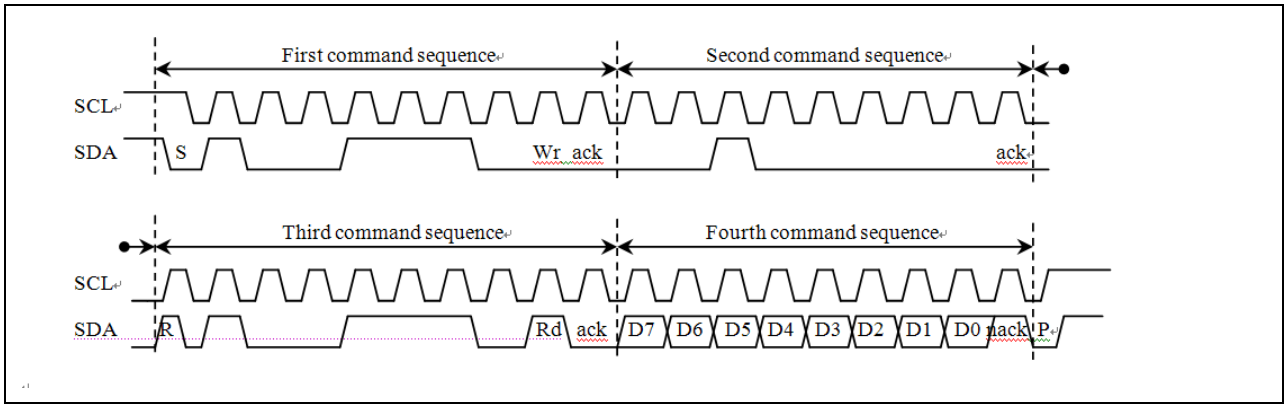


Figure 12-4

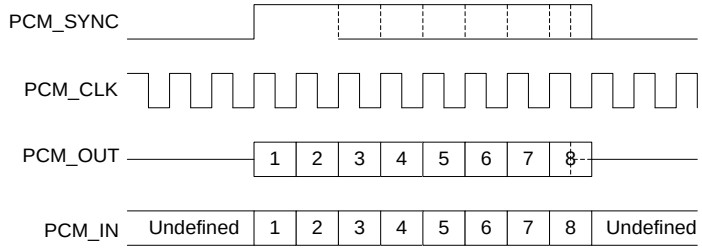
12.6 Operation Guide

Here is the general procedure for I2C :

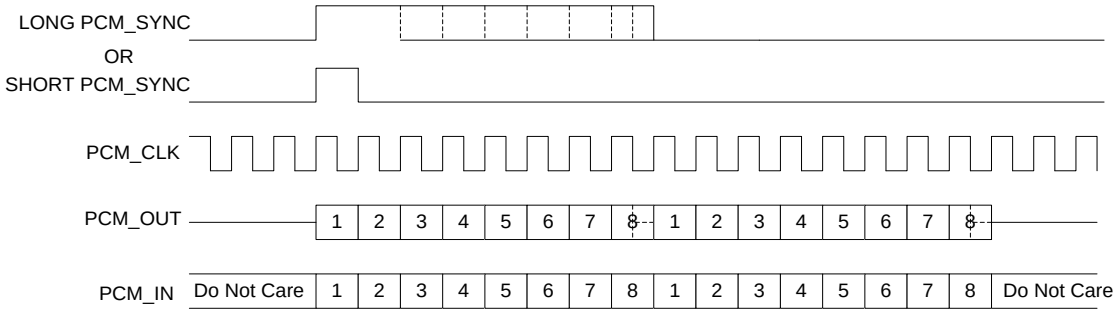
1. set the SCL port and SDA port direction to input;
2. put up SCL port and SDA port;
3. then you can operate as Programming examples says;

13 IIS_CTL

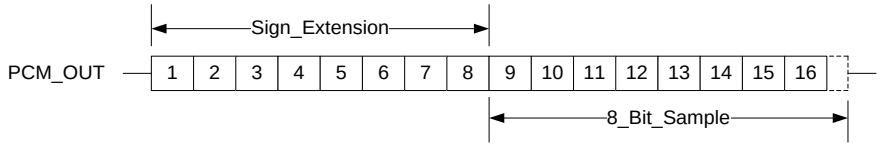
13.1 Timing diagram



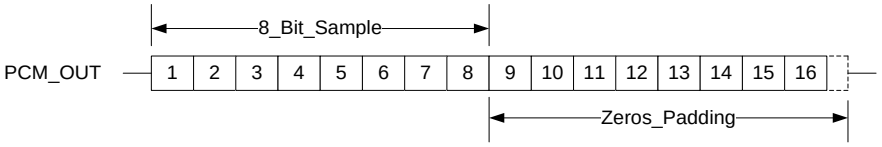
Long Frame Sync (Showm with 8-bit Companded Sample)



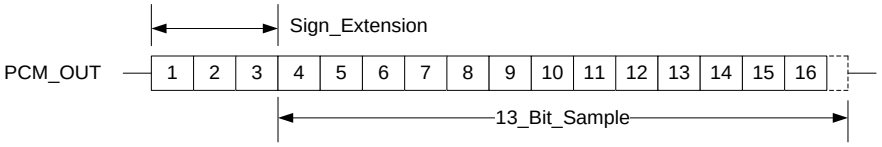
Multi_slot Operation with Two Slots and 8-bit Companded Samples



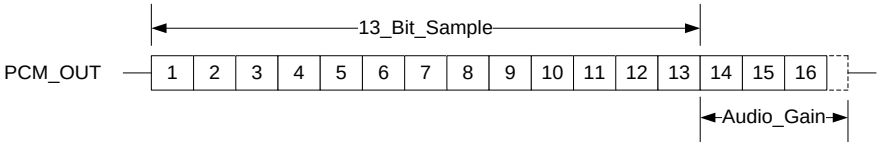
A 16-bit Slot with 8-bit companded sample and sign extension selected



A 16-bit Slot with 8-bit companded sample and zeros padding selected



A 16-bit Slot with 13-bit linear sample and sign extension selected



A 16-bit Slot with 13-bit linear sample and audio gain selected

Figure 13-1 PCM mode

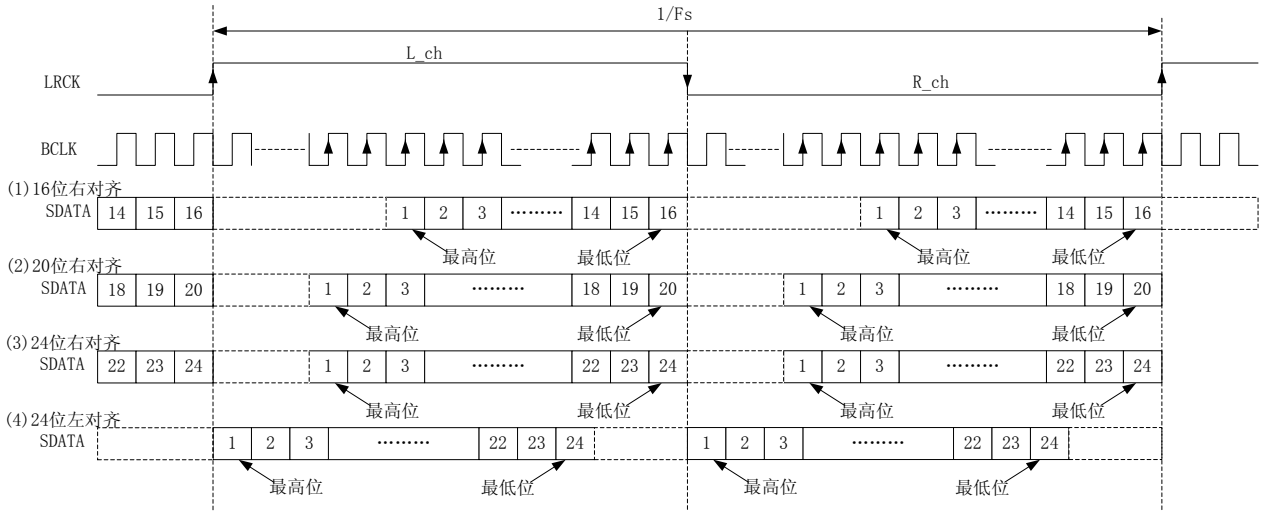


Figure 13-2 IIS mode

13.2 IIS Register

Register 13-1 IISCON0: IIS configuration Register 0.:（IISCON0，IIS1CON0）

Bit	Name	Mode	Default	Description
31:22	reserved	reserved	0	reserved
21	SLVMCLKE	WR	0	Slave mode output MCLK enalbe 0: disable 1:enable
20	TXMPTIE	WR	0	In cpu mode, tx interrupt enable.
19	WDMAIE	WR	0	In DMA TX mode,enable block dma done interrupt ie
18	RDMAIE	WR	0	In DMA RX mode,enable block dma done interrupt ie
17	EXCEPTIE	WR	0	enable TX/RX except interrupt.
16	TXRXIE	WR	0	IIS interrupt enable when send/received 1 sample 0: disable 1:enable
15:14	SMPSYNC	WR	0	sample IIS_DI by IO or synchronization input 00 = sample IO （master mode recommended） 01 =sample synchronization IO input(master mode) 1x =sample delay value of synchronization IO (slave mode recommended)
13:12	DACDATS	WR	0	Dac mode data source select 00=left & right dac data 01=low bass dac data 10=left + low bass dac data 11=right + low bass dac data
11:10	OPMOD	WR	0	IIS data operation mode 00 = data source come from cpu manual read/write 01 =data source come by DMA(to or from memorys) 10 =data source come from internal DAC output 11 =data source come from IO and to IO;LOOP_OP;Transfer out the data received,Data shift_in/shift_out by IO to IO;
9:8	TXRXMOD	WR	0	IIS data transfer work mode 00 =enable rx only 01 =enable tx only 10 =enable rx,tx at the same time 11 =reserve
7:6	DATAFMT	WR	0	IIS translate data format 00 =IIS format

Bit	Name	Mode	Default	Description
				01 =left align 10 =right align 11 = reserve
5:4	CHSEL	WR	0	Channel valid selection 00 = Both left and right channel is valid 01 = Only left channel valid 10 = Only right channel valid 11 = Reserve
3	LTHWS	WR	0	Left channel when WS is high 0 = Left channel data when WS is low; Right channel when WS is high 1 = Left channel data when WS is high; Right channel when WS is low
2	SMPEDGE	WR	0	IIS sample edge selection 0 = Rising edge drive data output, Falling edge sample data input 1 = Falling edge drive data output, Rising edge sample data input
1	SLVMODE	WR	0	IIS save mode selection 0 = Master mode 1 = Slave mode
0	IISEN	WR	0	IIS enable bit 0 = disable 1 = enable

Register 13-2 IISCKCON: IIS TX CLOCK configure （IISCKCON，IIS1CKCON）

Bit	Name	Mode	Default	Description
31:29	reserved	reserved	0	reserved
28::24	TRBITCNT	RW	0	configure IIS work BIT count mode if IIS work at N bit mode,then write N-1 to this register.
23:22	reserved	reserved	0	reserved
21:16	WSBITCNT	RW	0	the bclk counts inside WS L or H user must configure this counter, which is BCLKs. during WS High or Low
15:8	MCLKBAUD	RW	0	Output MCLK to slave device. Fmclk = Fiis/(MCLKBAUD+1),MCLKBAUD>=1
7:5	reserved	reserved	0	reserved
4:0	BCLKBAUD	RW	5'b00011	Master mode Bclk generate baudrate Fmclk/(BCLKBAUD+1), BCLKBAUD>=1

Register 13-3 IISTXDATA :IIS data tx register（IISTXDATA，IIS1TXDATA）

Bit	Name	Mode	Default	Description
31:0	IISTXDAT	W	0	CPU write data to this register to send out,this register can be write twice,then check IISCON0[19] if empty to write another two words. when IIS work at 16bit mode,this make 4 L only or 4 R only or 2 LR format data when IIS work at more bit than 16bit mode,write this twice kick two Single Left or Two single Right or 1 Left or Right data sample to send out

Register 13-4 IISRXDATA0:IIS data rx register0（IISRXDATA0，IIS1RXDATA0）

Bit	Name	Mode	Default	Description
31:0	IISRXDAT	R	0	recevied data 0,first data cpu read this register for received IIS format data.

Register 13-5 IISRXDATA1:IIS data rx register1（IISRXDATA1，IIS1RXDATA1）

Bit	Name	Mode	Default	Description
31:0	IISRXDAT1	R	0	recevied data 1,first data cpu read this register for received IIS format data.

Register 13-6 IISWSSMP：（IISWSSMP，IIS1WSSMP）

Bit	Name	Mode	Default	Description
31:30	reserved	RW	0	Reserved
29:16	SMPWSCNT	R	0	iis_clk count value from one WS posedge to the following one Sample rate = Fiis_clk/SMPWSCNT
15:1	reserved	R	0	reserved
0	SMPWSEN	RW	0	enable WS sample by calculate the iis_clk count between two posedge WS the result keep at WS_SMP [29:16] 0 = disable 1 = enable after sample done this bit will be clear automatic

Register 13-7 IISPND:IIS pending register .IIS0/IIS1 interrupt vector number is : 18（IISPND，IIS1PND）

Bit	Name	Mode	Default	Description
31:12	reserved	WR	0	reserved
11	WPNDCLR	W	0	Write this bit 1 to clear WDMAPND
10	RPNDCLR	W	0	Write this bit 1 to clear RDMAPND
9	ECPNDCLR	W	0	Write this bit 1 to clear ECPND
8	TXPNDCLR	W	0	Write this bit 1 to clear TXPND
7：6	reserved	WR	0	reserved
5	TXBUFEPT	WR	0	Tx buffer is empty 0= not empty 1= has empty
4	PCMECPND	WR	0	PCM EXCEPT happen pending
3	WDMAPND	R	0	Write DMA BLock done pending
2	RDMAPND	R	0	Rread DMA block done pending
1	ECPND	R	0	EXCEPT happen pending
0	TXPND	R	0	Pending when One sample TX/RX done Some sample data have been received in or sent out 0 = not done 1 = done 16bit data mode,then pending up after 2 Left & Right or 4 single left or 4 single right sample done other bit data mode,after 1 left & right or 2 left or 2 right sample channel data done,pnding up

Register 13-8 IISPCMCON：（IISPCMCON，IIS1PCMCON）

Bit	Name	Mode	Default	Description
31:16	reserved	R	0	reserved
15:13	SLOTCNT	WR	0	Slot count during one sample。count = SLOTCNT+1
12：8	SLOTBCNT	WR	0	Slot duration clock cycle (normal 8 bit or 16 bit)
7:6	reserved	WR	0	reserved
5:3	FSLEN	WR	0	PCM_SYNC length between 1clk to 8clk
2	HTH	WR	0	PCM_out configure to be high impedance on the half bclk 0: high-z at transmit edge of BCLK 1: high-z at sample edge of BCLK. --negedge edge of transmit edge
1	LENDIAN	WR	0	When PCM mode ,data transmitte select little endian transfer or big endian 0: big endian transmitted enable 1:little endian transmitted enable
0	PCMMODE	WR	0	IIS module PCM mode enable bit 0 = disable 1 = enable

Register 13-9 IISDMAWBADDR0：（IISDMAWBADDR0，IIS1DMAWBADDR0）

Bit	Name	Mode	Default	Description
31:19	resrved	R	0	reserved
18:0	DWBADR0	W	0	IIS RX DMA WRITE FIFO0 base address0. byte aligned

Bit	Name	Mode	Default	Description
				DWBADR0[1:0] should keep at 0

Register 13-10 IISDMAWBADDR1：（IISDMAWBADDR1，IIS1DMAWBADDR1）

Bit	Name	Mode	Default	Description
31:19	resrved	R	0	reserved
18:0	DWBADR1	W	0	IIS RX DMA WRITE FIFO0 base address1. byte aligned DWBADR1[1:0] should keep at 0

Register 13-11 IISDMARBADDR0：（IISDMARBADDR0，IIS1DMARBADDR0）

Bit	Name	Mode	Default	Description
31:19	Resrved	R	0	reserved
18:0	DRBADR0	W	0	IIS TX DMA READ FIFO0 base address0. byte aligned DRBADR0[1:0] should keep at 0

Register 13-12 IISDMARBADDR1：（IISDMARBADDR1，IIS1DMARBADDR1）

Bit	Name	Mode	Default	Description
31:19	Resrved	R	0	reserved
18:0	DRBADR1	W	0	IIS TX DMA READ FIFO0 base address1. byte aligned DRBADR1[1:0] should keep at 0

Register 13-13 IISDMAWFIFOCNT：（IISDMAWFIFOCNT，IIS1DMAWFIFOCNT）

Bit	Name	Mode	Default	Description
31:17	Resrved	R	0	reserved
16	FNUM	R	0	Return current active FIFO 0:FIFO0 1:FIFO1
15	F1FUL	R	0	Write FIFO1 full 0:not full 1: full
14	F0FUL	R	0	Write FIFO0 full 0:not full 1: full
13:0	DWCNT	WR	0	Write this register, set fifo0/fifo1 count . unit in word. Read this register ,return back current active fifo count received datas

Register 13-14 IISDMARFIFO0CNT：（IISDMARFIFO0CNT，IIS1DMARFIFO0CNT）

Bit	Name	Mode	Default	Description
31:15	Resrved	R	0	reserved
14	F0HALTEN	W	0	Control after read out all DRCNT data, IIS halt or not 0:not halt and toggle to FIFO1 1:halt till CPU clear this bit
13:0	DRCNT	W	0	Configure READ FIFO0 size in word

Register 13-15 IISDMARFIFO1CNT：（IISDMARFIFO1CNT，IIS1DMARFIFO1CNT）

Bit	Name	Mode	Default	Description
31:15	Resrved	R	0	reserved
14	F1HALTEN	W	0	Control after read out all DRCNT data, IIS halt or not 0:not halt and toggle to FIFO0 1:halt till CPU clear this bit
13:0	DRCNT	W	0	Configure READ FIFO1 size in word

13.3 Operate flow

13.3.1 CPU wr/rd

- For 2-wire data mode, set IO direction,1-wire Data input/output hardware auto control

configure other IO direction. such as WS,BCLK,REFCLK(if need)

- if master mode, set BAUDRATE, MST_BITCON, set TXRX_CNT ,WS_BIT_CNT for different bits transfer
- write IIS_CON for Slave mode, sample edge, LTHWS,CH_SEL,DATA_FMT,TXRX_MOD,OP_MOD,IIS_IE setting.
- enable IIS_EN kick start RX/TX or both

  For data receive ， if both left and right channel data available, then hardware will halt until left channel is coming.

  so if first receive right channel data ,hardware will ignore it.
- Write IIS_TX_DATA twice to send 2 data out
- wait TX_BUF_EMPTY = 1,then write another 2 data to send ,if tx
- wait IIS_PND = 1,when rx mode, then read IIS_RD_DATA0,IIS_RD_DATA1 out

13.3.2 loop op

this IIS support loop operation mode. that is send out data come from RX pin. and the tx data will delay 2-4 sample before really data come out. and the first 2-4 sample being send out is all 0s.must configure OP_MOD=2'b11;

13.3.3 PCM_Mode

- configure the length of PCM_SYNC by setting FSLEN
- enable big or little endian tx/rx
- enable output hi-z timing point
- set slot count
- set bit count during one slot
- others iis setting

  there are many ways to tx/rx PCM data. e.g. want to tx/rx 16 bit ,you can set txrx_cnt=7,Left & right channel effective. or you can set txrx_cnt=15,left channel or right channel effective.

  when want to tx/rx 24bit or 3 8-bit slot,you can set txrx_cnt=23,left or right channel effective.

  but all be in careful is all data tx/rx at the beginning of WS rising edge during PCM Mode.

14 Characteristics

14.1 LDO Parameters

Table 14-1 LDO Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
Vin	LDO input voltage	3.6	5	5.5	V	-40℃ ~ 125℃
Vout1.2	1.2V output voltage	0.9	1.2	1.35	V	-40℃ ~ 125℃
Vout3.3	3.3V output voltage	2.9	3.3	3.4	V	-40℃ ~ 125℃
Iout1.2	1.2V output current	-	-	200	mA	-40℃ ~ 125℃
Iout3.3	3.3V output current	-	-	250	mA	-40℃ ~ 125℃

14.2 PLL Parameters

Table 14-2 MPLL Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
F_I	Frequency input	32.768K	-	12M	Hz	-40℃ ~ 125℃
F_{OUT1}	Frequency output	150	-	300	MHz	-40℃ ~ 125℃
T_{LOCK}	PLL locked time for 32.768KHz	-	2	-	ms	-40℃ ~ 125℃
T_{LOCK1}	PLL locked time for 12MHz	-	0.4	-	ms	-40℃ ~ 125℃

Table 14-3 APLL Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
F_I	Frequency input	32.768K	-	12M	Hz	-40℃ ~ 125℃
F_{OUT1}	Frequency output	180	-	220	MHz	-40℃ ~ 125℃
T_{LOCK}	PLL locked time for 32.768KHz	-	2	-	ms	-40℃ ~ 125℃
T_{LOCK1}	PLL locked time for 12MHz	-	0.4	-	ms	-40℃ ~ 125℃

14.3 I/O Parameters

Table 14-4 I/O Parameters

IO1B2-- Electrical Characteristics

Parameters		Typical	MIN	MAX	Unit	Note
Driver Ability@24mA		43.34	28.51	62.28	mA	
Driver Ability@8mA		12.58	9.74	16.32	mA	
VIH		1.895	1.865	1.925	V	
VIL		1.435	1.395	1.475	V	
Rise/Fall time	Rise	2.80	2.14	3.66	ns	
@8mA 16pF	Fall	2.63	1.87	3.93	ns	
Rise/Fall time	Rise	0.934	0.663	1.334	ns	
@24mA 16pF	Fall	0.871	0.623	1.366	ns	

IO1B1/IO1B3/IO1B4-- Electrical Characteristics

Parameters		Typical	MIN	MAX	Unit	Note
Driver Ability@24mA		36.73	24.12	53.46	mA	
Driver Ability@8mA		12.38	8.11	18.09	mA	
VIH		1.895	1.865	1.925	V	
VIL		1.435	1.395	1.475	V	
Rise/Fall time	Rise	4.629	3.316	7.116	ns	
@8mA 25pF	Fall	4.307	2.973	7.225	ns	
Rise/Fall time	Rise	2.958	1.867	5.172	ns	
@24mA 16pF	Fall	2.333	1.430	4.732	ns	

IO1D1-- Electrical Characteristics

Parameters	Typical	MIN	MAX	Unit	Note

Parameters		Typical	MIN	MAX	Unit	Note
Driver Ability@8mA		12.58	16.32	9.737	mA	
VIH		1.915	1.875	1.965	V	
VIL		1.385	1.345	1.425	V	
Rise/Fall time @8mA 12pF	Rise	2.649	1.925	3.723	ns	
	Fall	2.180	1.444	3.358	ns	

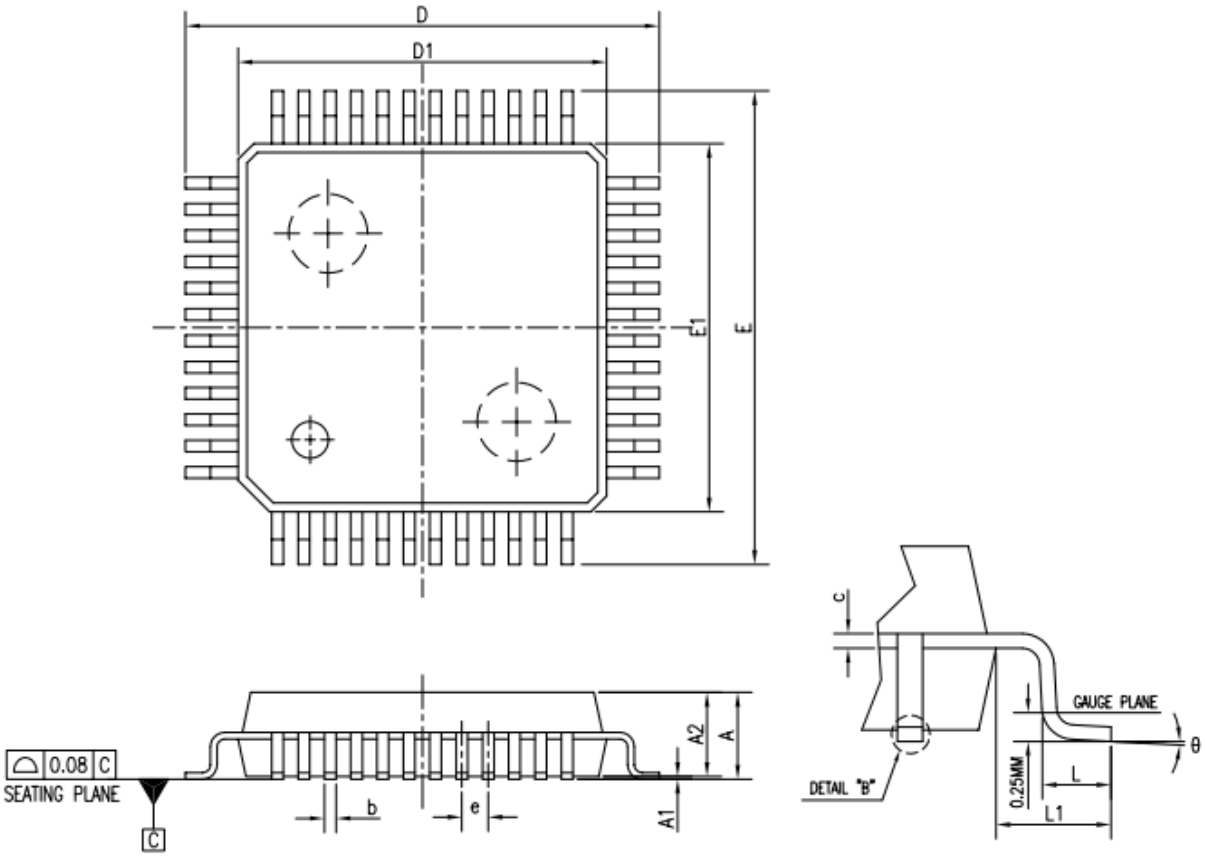
14.4 Audio DAC Parameters

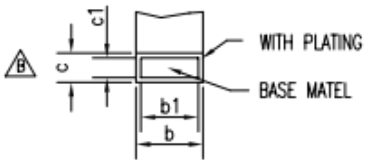
Table 14-6 Audio DAC Parameters

Sym	Characteristics	Min	Typ	Max	Unit	Conditions
SNR		-	98	-	dB	
THD+N		-80	-	-	dB	
PWR_{AB}	ClassAB AMP power output	-	-	16	Mw	
V_{PP}	Maximum output voltage	-	-	2.828	V	

15 **Package Outline Dimensions**

15.1 **AX3153A**





DETAIL "B"

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.09	–	0.20	0.004	–	0.008
c1	0.09	–	0.16	0.004	–	0.006
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.17	0.22	0.27	0.17	0.20	0.23		0.50 BSC.		MS-026 BBC
64L	0.13	0.18	0.23	0.13	0.16	0.19		0.40 BSC.		MS-026 BBD

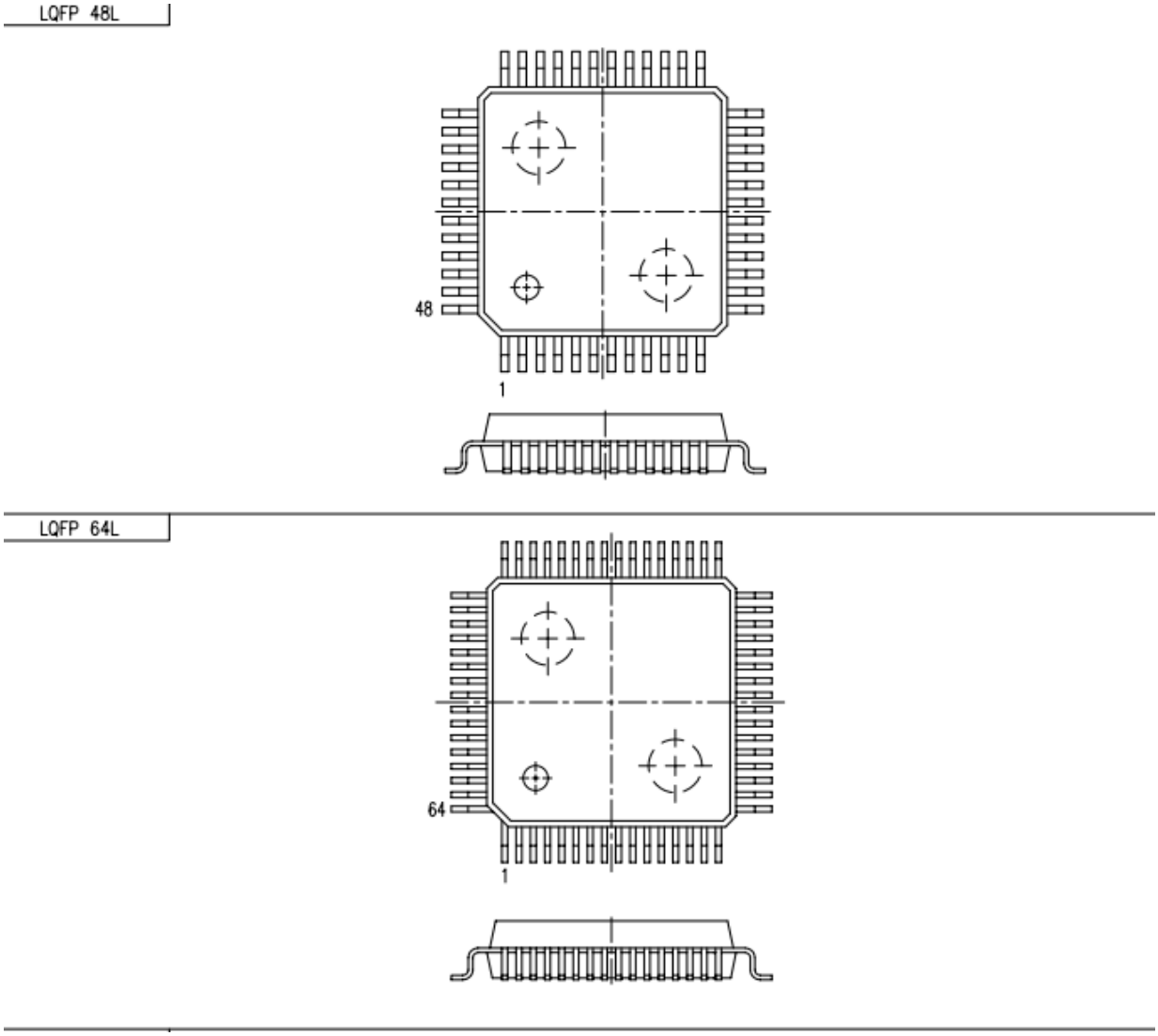


Figure 15-1 AX3153A Package Outline Dimension

Appendix I Revision History

Date	Version	Comments	Revised by
2016-2-24	0.0.1	Initial Version	YX
2016-2-29	0.0.2	Check	ZJ/HP
2016-3-2	1.0.0	Release	YX

In case of any questions or comments about this documentation, please feel free to contact AppoTech at documents@appotech.com .