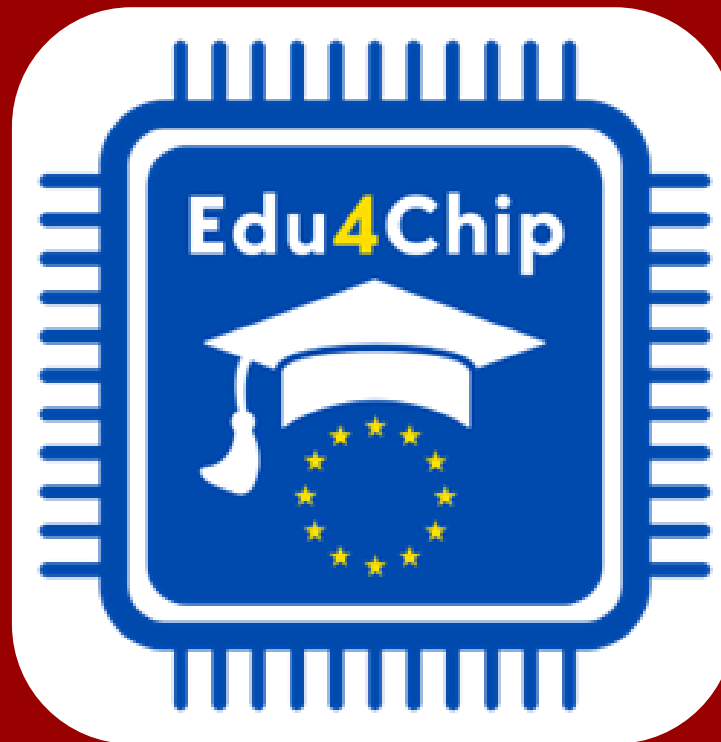
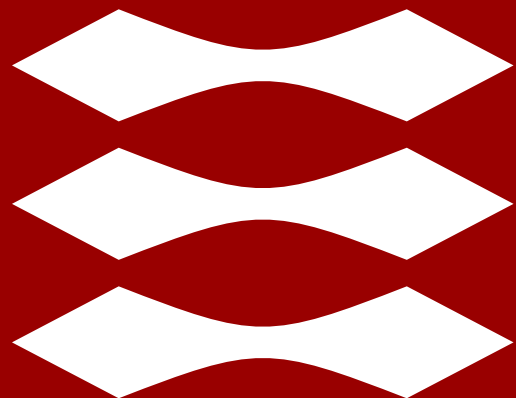


DTU



From Theory to Tape-Out: Chip Design Education with Edu4Chip

Matthias Bo Stuart, Luca Pezzarossa
Embedded Systems Engineering
Technical University of Denmark



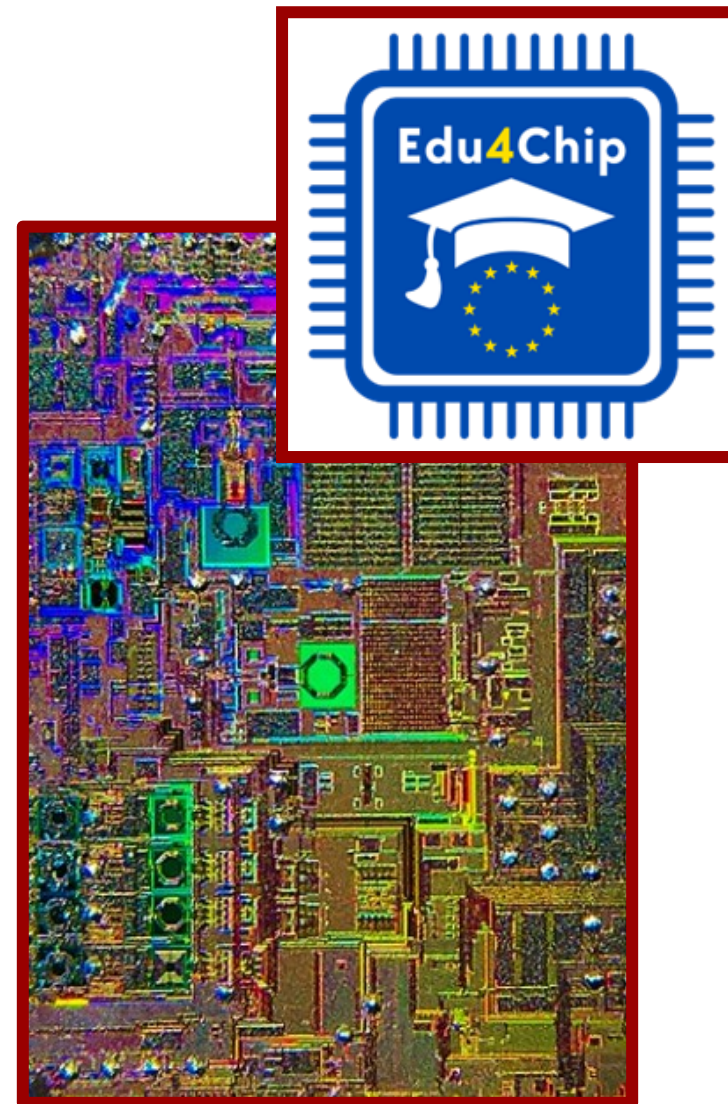
Funded by
the European Union

Who am I?

- MSc (2006), PhD (2010) on Network-on-Chip, DTU
- Postdoc, associate professor (2010-2022) in biomedical engineering
 - Center for Fast Ultrasound Imaging, DTU Electrical Engineering/Health Technology
 - World's largest ultrasound scanner, 320 Virtex-4 FPGAs
- Industry experience (2022–2024)
 - Systems engineer, BK Medical/General Electric/GE HealthCare
- Associate professor at DTU Compute, ESE since March 2024

Overview

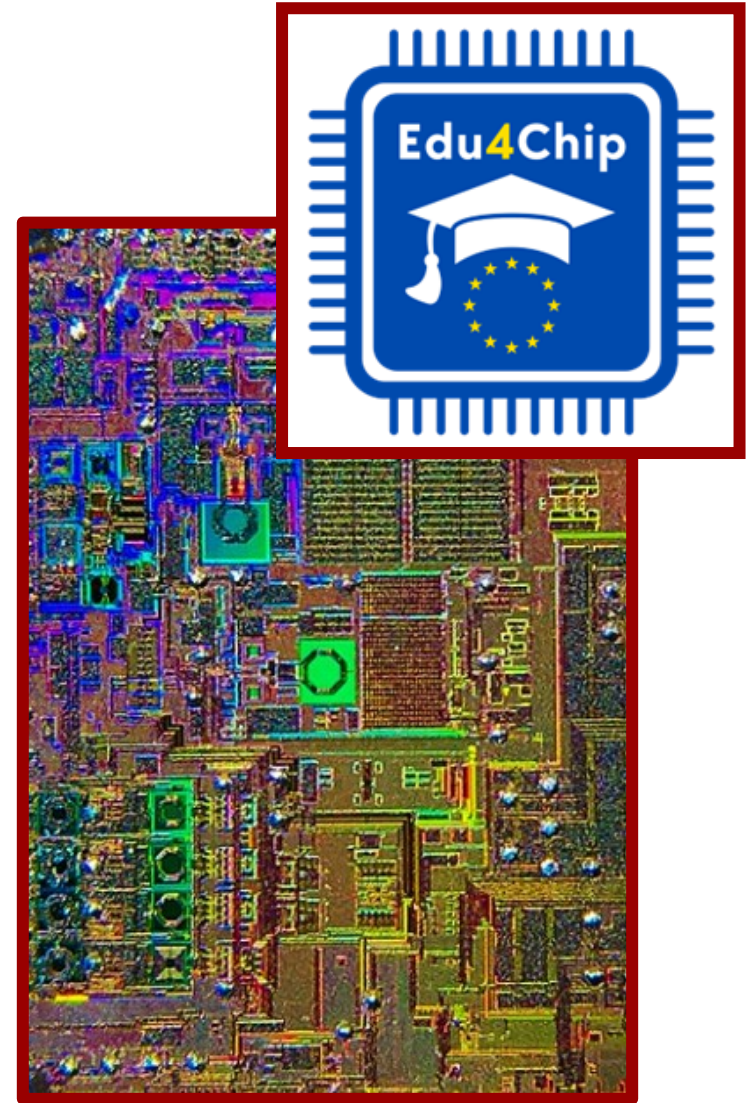
The EU Chips Act aims to promote EU sovereignty
in **chip design and manufacturing**



Overview

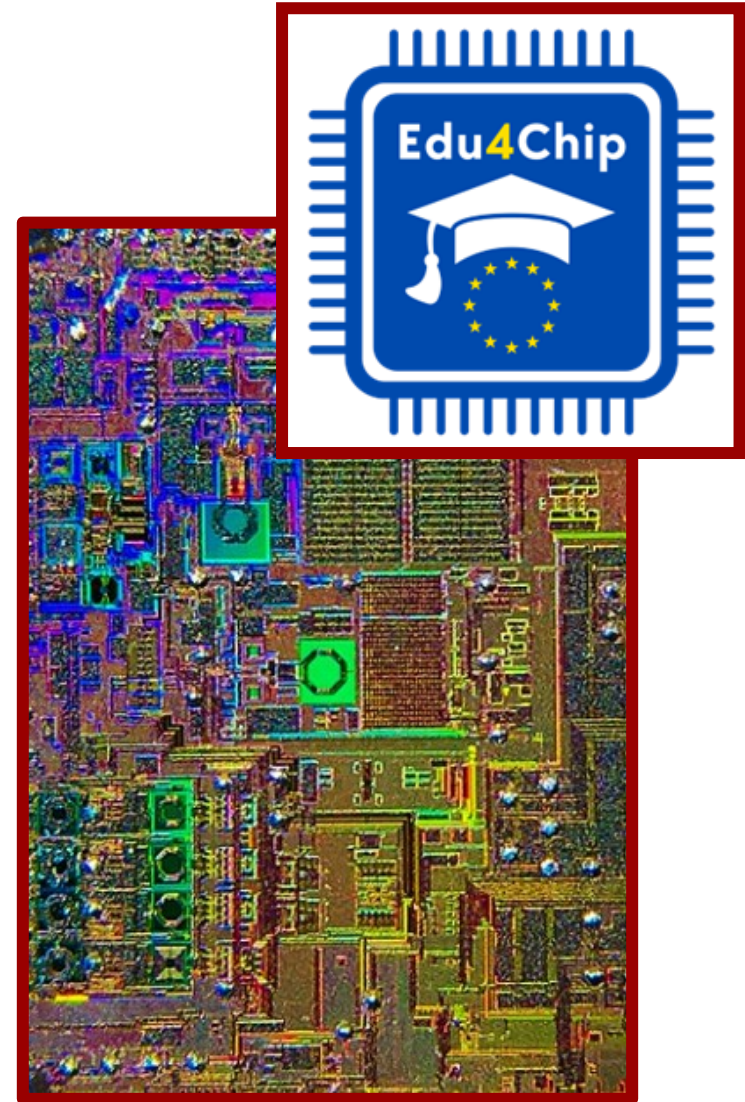
The EU Chips Act aims to promote EU sovereignty in **chip design and manufacturing**

We need **trained skilled professionals**



Overview

- Designing and implementing harmonized MSc programs between universities
- Enabling students to carry out a complete chip design project (from HDL to tape-out to testing)
- Enhancing the chip design capability in Europe by educating skilled engineers



New BSc program in Computer Engineering

- Response to the **EU Chip Act**
- Started fall 2023 at the Technical University of Denmark
- Includes a **chip-design specialization**:
 - Digital electronics theory and projects
 - Computer architecture
 - RISC-V in an FPGA
 - Chip design (using open-source tools)
 - Verification
 - HW/SW codesign
 - ...

New BSc program in Computer Engineering

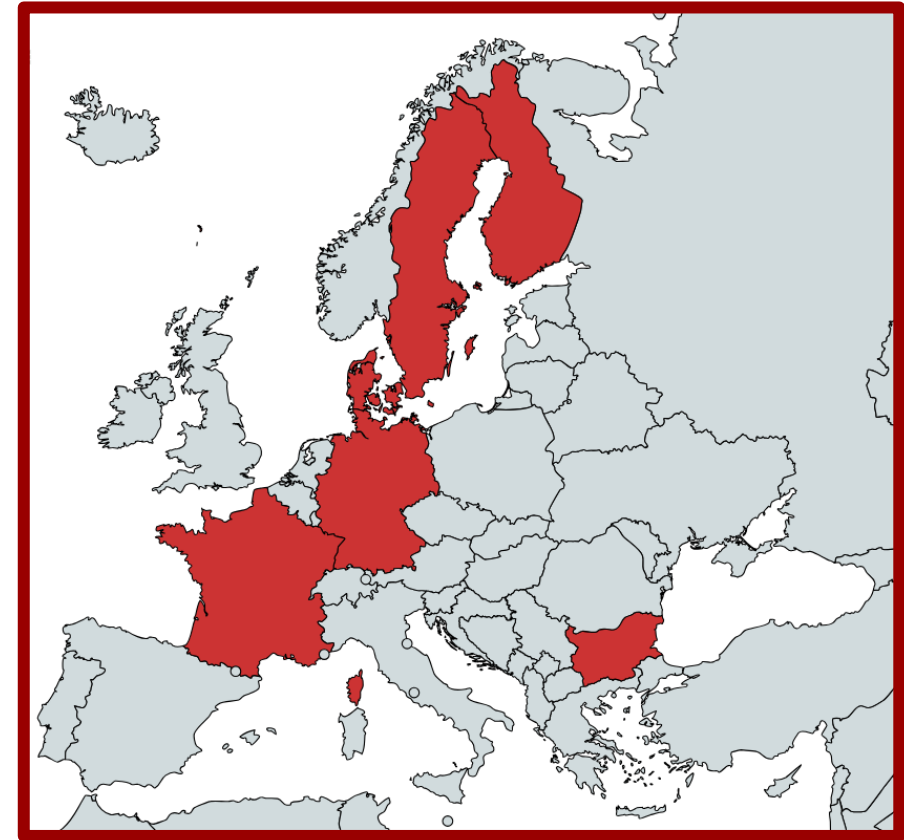
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 - Chip design (using open-source tools)
 - Verification
 - HW/SW codesign
 - ...

We already have a MSc
including chip design

How can we improve?

Edu4Chip in a nutshell

- **Universities:**
 - Technical University of Munich - TUM (DE)
 - Technical University of Denmark - DTU (DK)
 - Tampere University - TAU (FI)
 - Royal Institute of Technology - KTH (SE)
 - Mines-Telecom Institute - IMT (FR)
- **Companies:**
 - MINRES Technologies GmbH (DE)
 - Logiqworks Ltd (BU)
 - Syosil ApS (DK)
- **Institutions:**
 - Fraunhofer Institute (DE)



Edu4Chip in a nutshell

- Edu4Chip: Joint Education for Advanced Chip Design in Europe
- Funding from **Digital Europe Programme** (EU DIGITAL-2022-SKILLS-03)
- Period:
 - Started on the 1st of October 2023
 - Ends on the 30th September 2027
- Initial preparation phase + execution phase



Edu4Chip objectives



1 {

- Strengthen the chip design MSc programs including real tape-out projects

Edu4Chip objectives

- 1 {
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- 2 {
 - Develop common open-source training modules framed around a tape-out project

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- 3 {
 - Develop common open-source chip template

Edu4Chip objectives

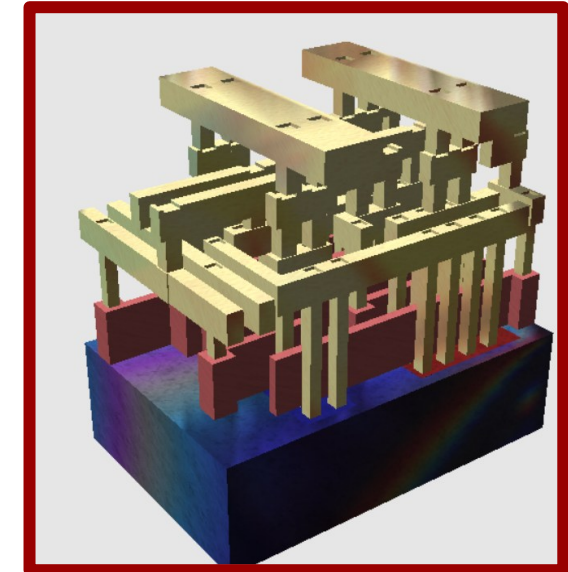
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 - Develop common open-source chip template
- 4 {
 - Allow student mobility between universities and share teaching material
- 5 {
 - Strengthen partnerships with local industry

A more practical MSc program

- Unique feature: **Emphasis on practical tape-out projects**
 - Students will experience the entire chip design process, from concept to fabrication and testing
 - Boost student engagement and motivation by working on real chip designs
- Cover digital, analog, and mixed-signal systems
- Enroll and train 150 students per year
- Lifelong Learning Modules:
 - Continuous professional development
 - Transitioning from other fields into chip design



Program outline

Term 1

Local Modules
(existing/new)

Remote Modules
(new/existing)

Term 2

Local Modules
(existing/new)

Remote Modules
(new/existing)

Term 3

Local Modules
(existing/new)

Remote Modules
(new/existing)

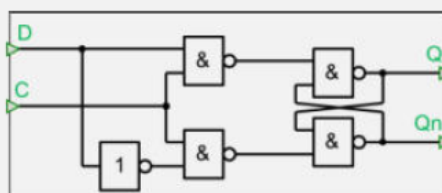
Research Internship
(Industry Partner)

Term 4

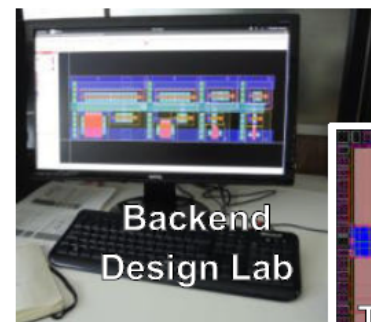
Master Thesis Project

```
architecture STRUCTURE of DEC2K4 is
  component IN1
    port (IN1 : in bit; OUT1 : out bit);
  end component;
  component NAND3
    port (A, B, C : in bit; OUT : out bit);
  end component;
  signal A00,B001 : bit;
begin -- Initialization of components
  I0: IN1 port map (A, A00);
  I1: IN1 port map (B, B00);
  O0: NAND3 port map (A00, B00, EN, D00);
  O1: NAND3 port map (A00, B, EN, D01);
  O2: NAND3 port map (A, B00, EN, D02);
  O3: NAND3 port map (A, B, EN, D03);
end STRUCTURE;
```

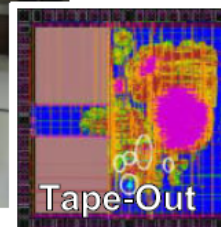
HDL Lab



Frontend Design Lab



Backend
Design Lab



Tape-Out

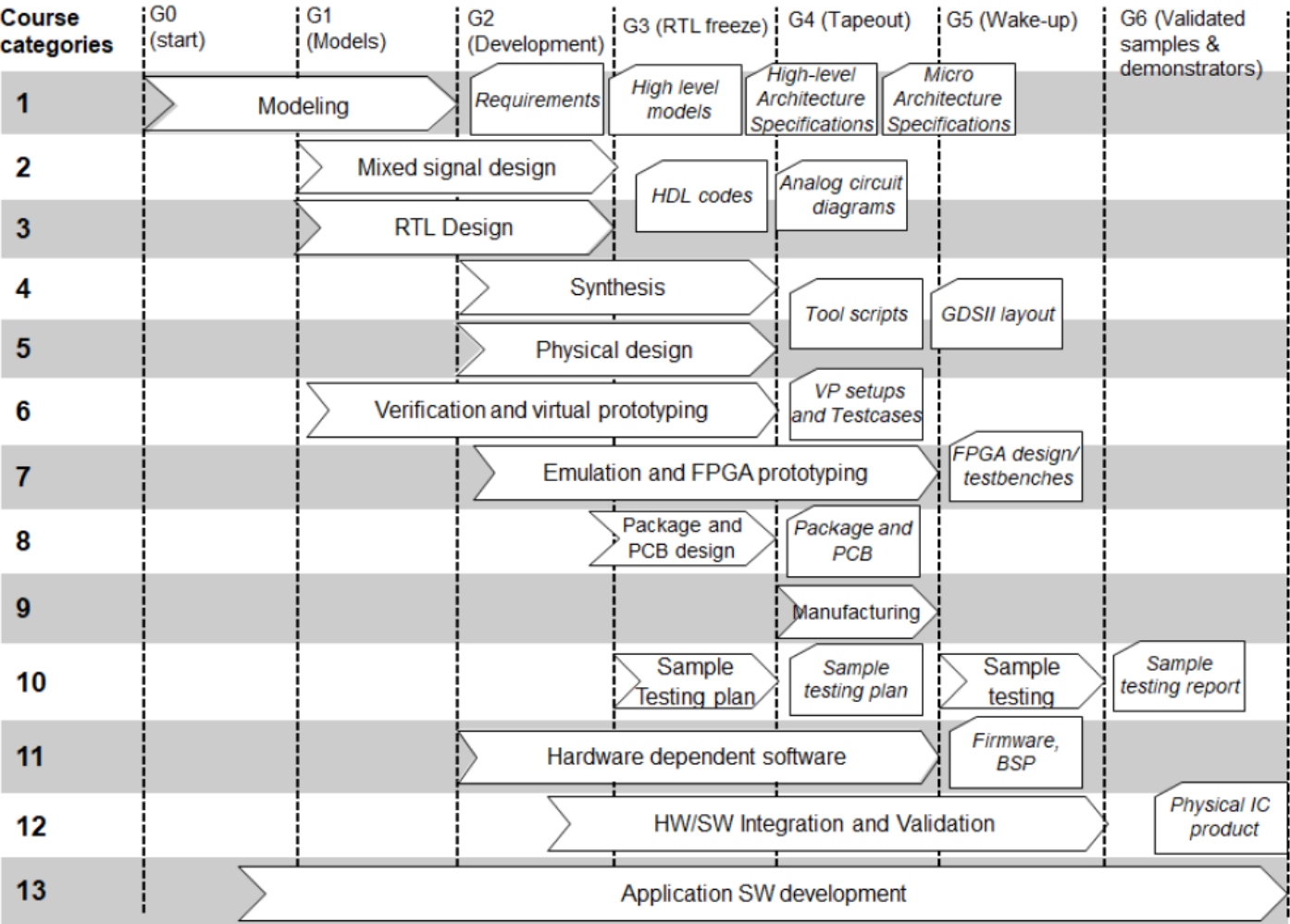


Test and
Evaluation Lab

Chip Design Tape-Out Project

Life-long learning modules

Mapping skills to courses



I want to make a chip!

What do I need to know?

Hard for a single university to offer everything

	DTU	IMT	IIS	KTH	LGQW	MNRS	SYO	TAU	TUM
Modelling	+	+	+	+	+	+			+
Mixed Signal Design		+	+		+				+
RTL Design	+	+	+	+		+	+	+	+
Synthesis		+	+	+	+		+	+	+
Physical Design		+	+	+				+	+
Verification & virtual prototyping	+		+		+	+	+	+	
Emulation & FPGA prototyping	+	+				+		+	+
Package and PCB design		+	+					+	
Manufacturing									
Sample testing plan								+	
Hardware dependent software	+				+	+		+	+
HW/SW integration & validation	+				+	+		+	+
Application SW development	+			+	+	+		+	+

- Leverages expertise across all partners
- Inter-university cooperation
- Allow students mobility
 - Physical
 - Virtual

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Sharing is key!

Sharing allows to have specializing courses

- Testing
- **Agile hardware design**
- Packaging
- FPGA-based emulation
- **Verification**
- **Asynchronous circuits**
- Low-power designs
- High-level synthesis
- **Open-source chip design**

```
def regPipeline[T <: Data](input: T,
    pipeDepth: Int, init: T): T = {
  if (pipeDepth <= 0) {
    val ret = input
    ret
  } else {
    val pipeReg = RegInit(
      VecInit(Seq.fill(pipeDepth)(init)))
    val ret = pipeReg(0)
    pipeReg(pipeDepth - 1) := input
    for (i <- 0 until pipeDepth - 1) {
      pipeReg(i) := pipeReg(i + 1)
    }
    ret
  }
}
```

Sharing allows to have specializing courses

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    }
    ret
  }
}
```

Many educational modules will be released to the public

Student mobility between universities

- Harmonized programs facilitate easy transfer between universities
 - Common/shared curriculum across participating universities
 - Share teaching materials and best practices
- Students have a **larger selection of courses**
- Foster strong, long-term partnerships among universities
- Edu4Chip offers travel grants to ensure students (and teachers) exchange

Program concept deliverable

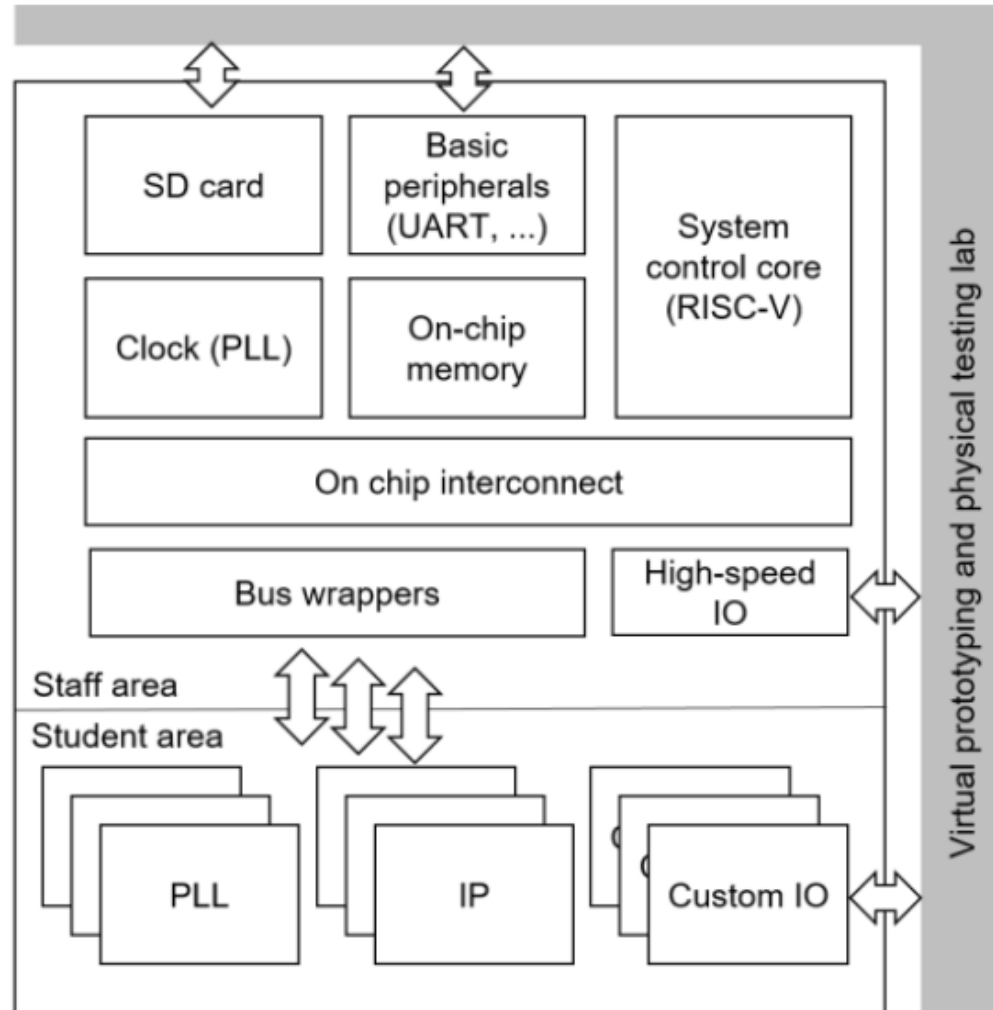
- Deliverable describing the program concept recently published
- Education structure and harmonization
- Challenge: Variations in university education administration in Europe
- Available on <https://edu4chip.github.io>

Content

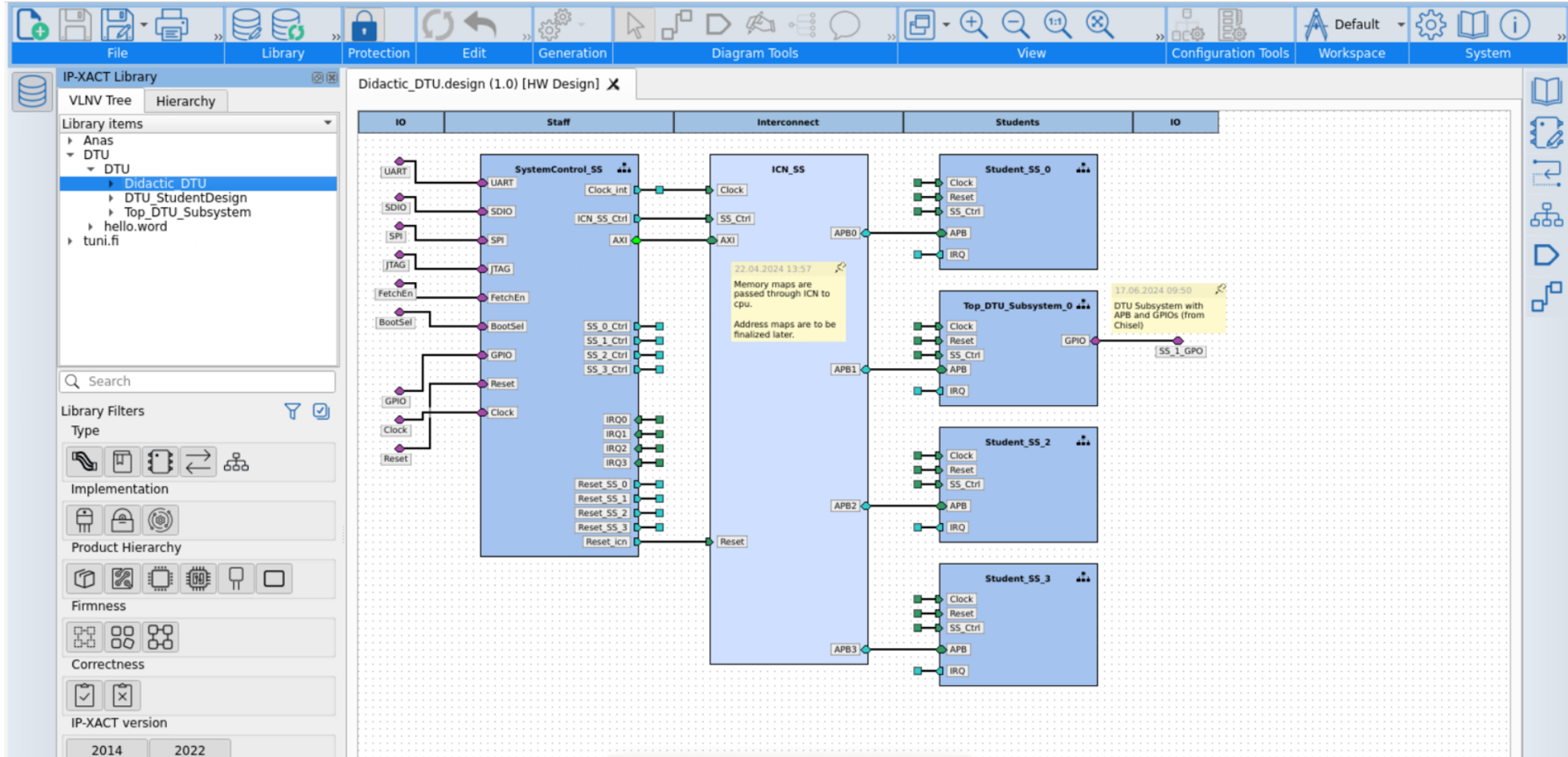
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A common open-source chip template

- Joint design template to support student projects tape-out
- Staff area + Student area
- Many student projects per chip
- Edu4Chip offers 1 tape-out per year per partner
- First test tape-out in Spring 2025

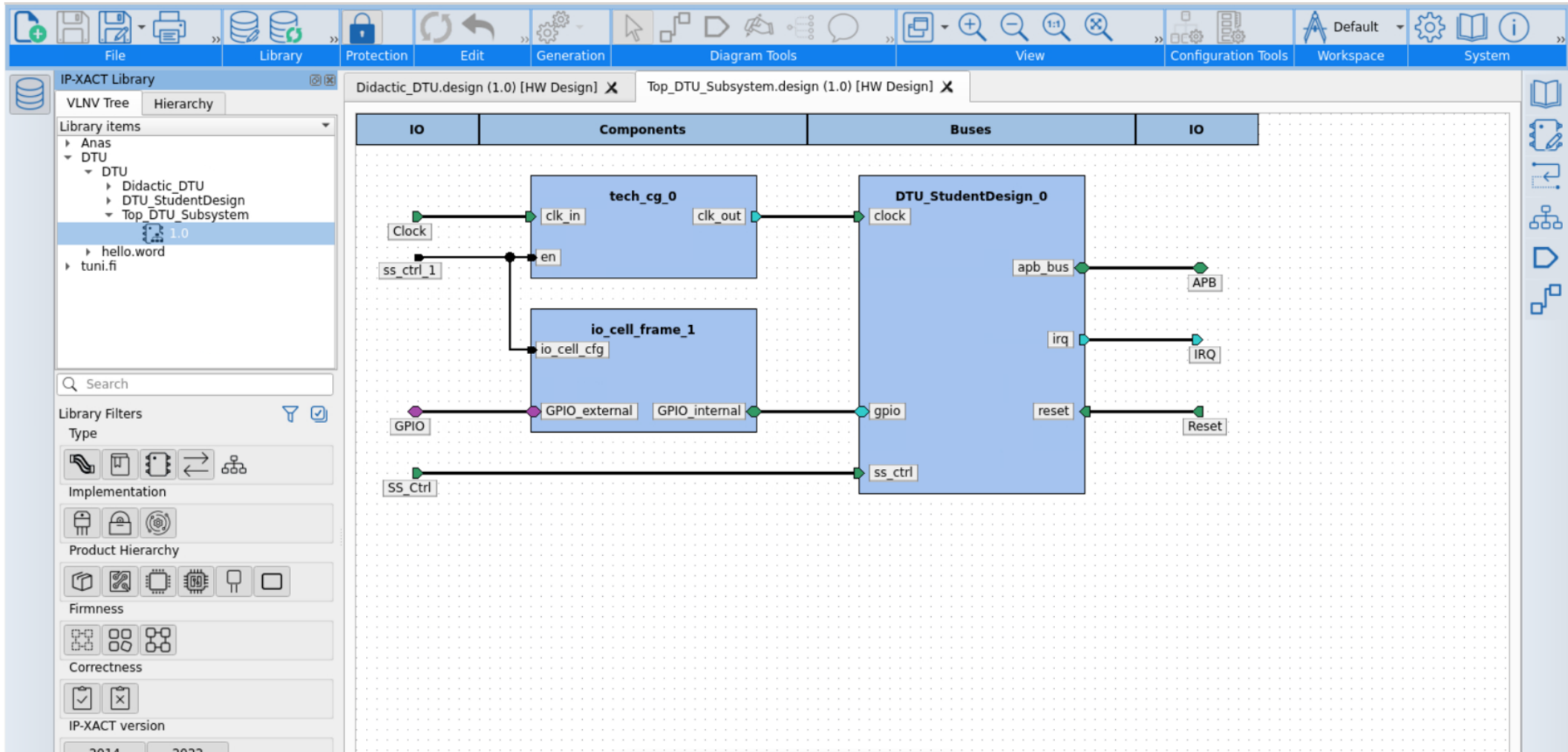


A common open-source chip template



- Modelled with the open source Kactus2 tool from Tampere University (IEEE IP-XACT)

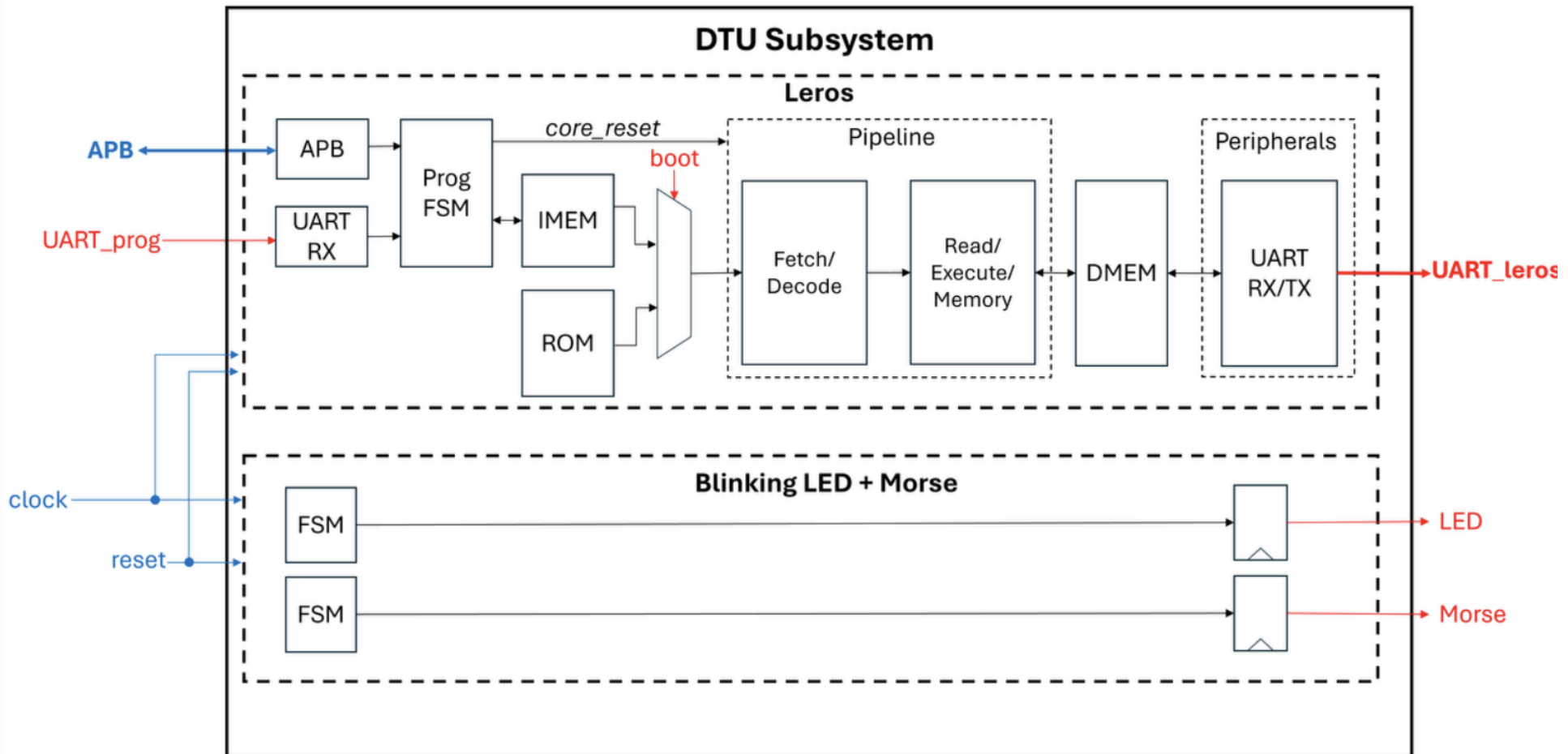
A common open-source chip template



- Modelled with the open source Kactus2 tool from Tampere University (IEEE IP-XACT)

DTU Subsystem for test run

- Leros microprocessor (Martin Schoeberl)
- Preprogrammed ROM and programmable from "staff area"



EDA toolchains

- **Balanced approach:**
 - Utilize both open-source and commercial EDA tools within the partner universities
- **Commercial tools:**
 - Industry-standard EDA Tools from Cadence, Synopsys, Mentor Graphics, Siemens
 - Students gain hands-on experience with tools used within the industry
- **DTU's open-source tool initiative for education:**
 - Driven by Martin Schoeberl and Luca Pezzarossa
 - Focus on accessible and affordable chip design education
 - No NDAs (and overhead)
 - Open-source tools and PDKs enable education outside the university walls
 - Pilot course: Test course using OpenRoad was very well-received
 - Next: BSc chip design course using TinyTapeout

Summer schools dedicated to chip design

2025
DTU
(Denmark)

2026
IMT
(France)

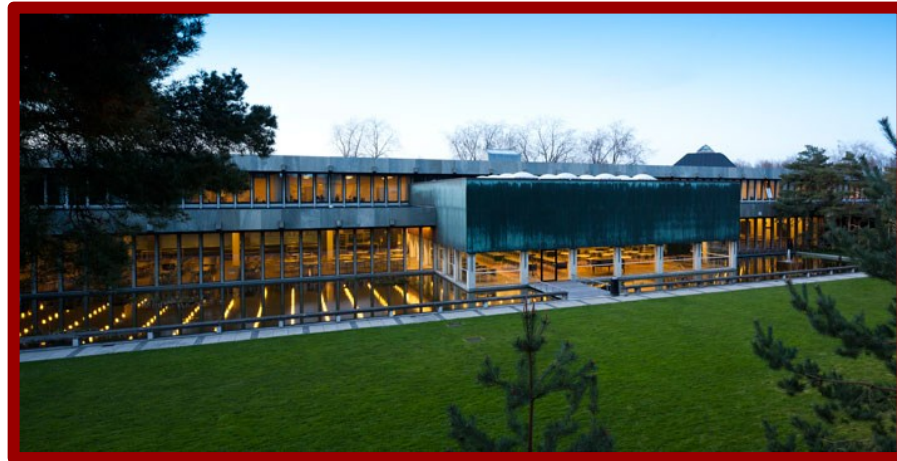
2027
TAU
(Finland)



- Open to the general public
- Grants available for students
- Promote interest in the field from students

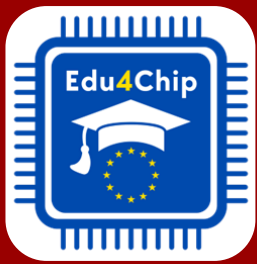
Summer school in 2025

- Organized and held by the Technical University of Denmark in 2025
- From the 18th to the 22nd of August 2025 (Monday to Friday)
- We plan to include a strong focus on open-source chip design



Summary of the outcomes

- Establish harmonized chip design programs at five European universities
- Develop and enhance teaching modules focused on chip design (hands-on tape-outs)
- Release a selection of teaching modules to the public
- Open-source repository for the technical material, tools, and resources (chip template)
- Share reference guidelines and evaluation results to inform and guide similar efforts



Funded by
the European Union

From Theory to Tape-Out: Chip Design Education with Edu4Chip

Web: <https://edu4chip.github.io>

Project GitHub: <https://github.com/edu4chip>

Contact:

- Luca Pezzarossa (lpez@dtu.dk)
- Martin Schoeberl (masca@dtu.dk)
- Matthias Bo Stuart (mbst@dtu.dk)



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