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14-513 18-613

Virtual Memory: Concepts

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15-213/18-213/14-5

Introduction to Com

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17th Lecture, October 27, 2020

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Informal Survey Summary

- **40% of Students Responded to the Survey**
  - Thank you!
- **Over 35% felt the labs were the strongest feature**
  - Another 25% thi
  - And 10% feel th written assignments
- **Around 20% of students note the pace is too fast**
  - Therefore, many feel that recorded lectures support their learning
- **Chat is a great avenue for asking questions**
  - Can also be distracting

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Informal Survey Summary (cont)

- **Many students feel welcomed and included**
  - Teaching Assistants and professors who care
- **TA OH are an important part of learning**
  - Keeping to 10 m ctations
  - Expect a separa
- **The instructors are happy to discuss the feedback further in their office hours**
  - Many other valuable points and suggestions

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Hmmm, How Does This Work?!

Process 1 **Process 2** **Process n**

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Solution: Virtual Memory (today and next lecture)

Today

- **Address spaces** CSAPP 9.1-9.2
- VM as a tool for caching CSAPP 9.3
- VM as a tool for memory management CSAPP 9.4
- VM as a tool for CSAPP 9.5
- Address translat CSAPP 9.6

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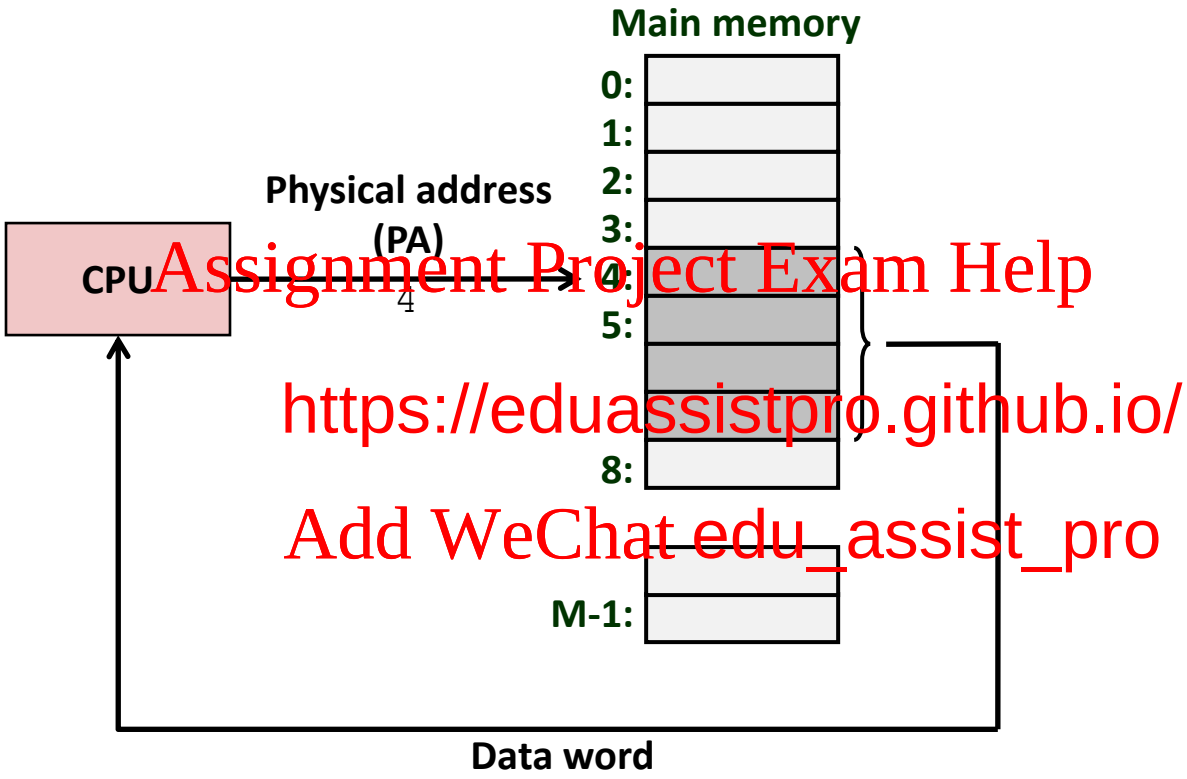
A System Using Physical Addressing



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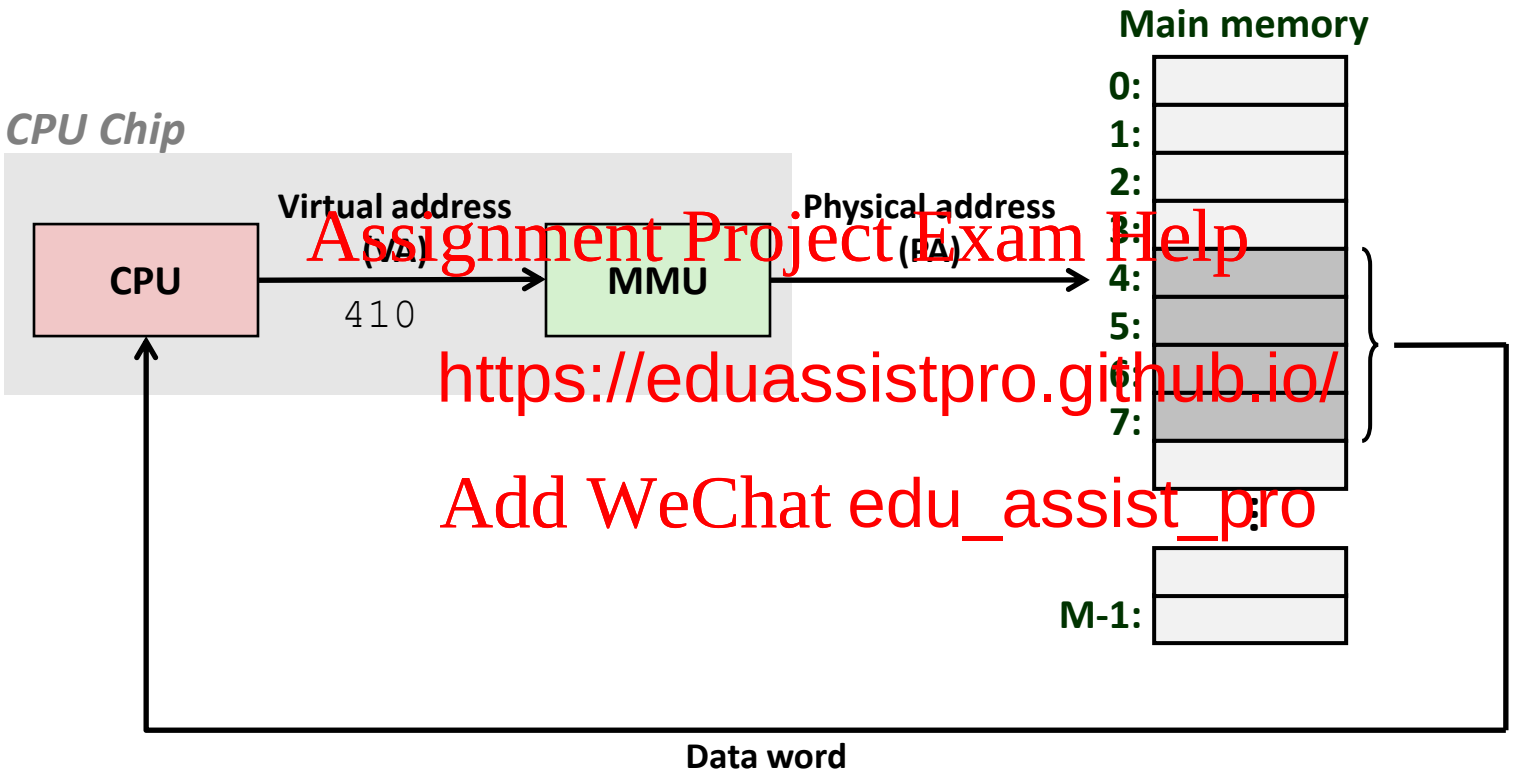
- Used in “simple” systems like embedded microcontrollers in devices like cars, elevators, and digital picture frames

A System Using Virtual Addressing



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- Used in all modern servers, laptops, and smart phones
- One of the great ideas in computer science

Address Spaces

- **Linear address space:** Ordered set of contiguous non-negative integer addresses:

  {0, 1, 2, 3 … }

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- **Virtual address space:** Set of N = 2^n virtual addresses

  {0, 1,

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- **Physical address space:** Set of M = 2^m sses

  {0, 1, 2, 3, …, M-1}

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Why Virtual Memory (VM)?

- **Uses main memory efficiently**
  - Use DRAM as a cache for parts of a virtual address space

- **Simplifies memory management**
  - Each process get ess space

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- **Isolates address spaces**
  - One process can't interfere with an y
  - User program cannot access privileged kernel information and code

Today

- Address spaces
- **VM as a tool for caching**
- VM as a tool for memory management
- VM as a tool for
- Address translat

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VM as a Tool for Caching

- Conceptually, ***virtual memory*** is an array of N contiguous bytes stored on disk.
- The contents of the array on disk are cached in ***physical memory*** (***DRAM cache***)
  - These cache blo 2^p bytes)

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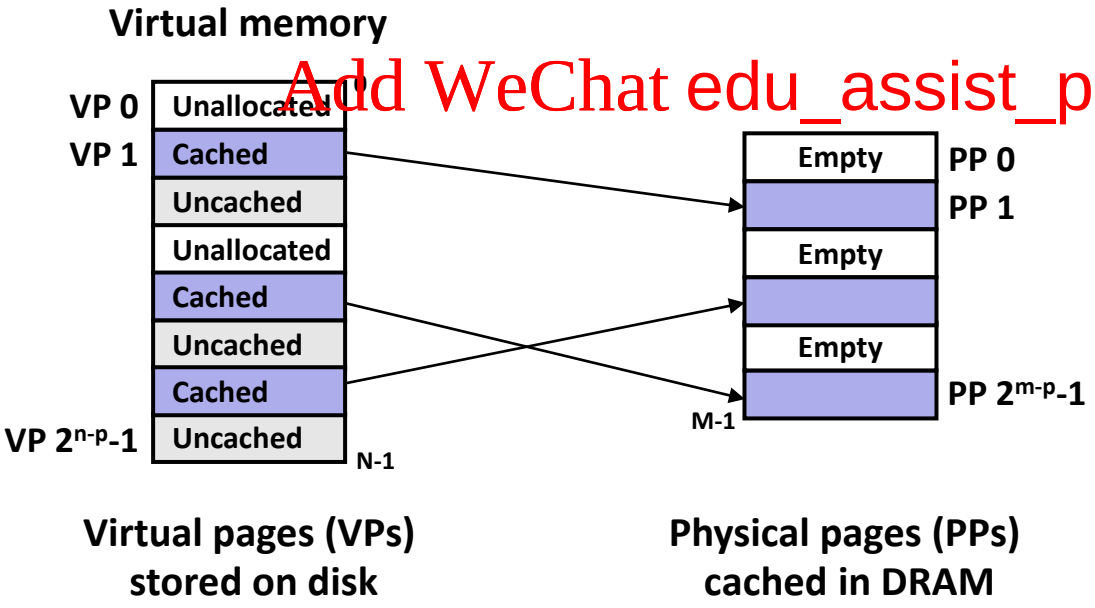

DRAM Cache Organization

- **DRAM cache organization driven by the enormous miss penalty**
  - DRAM is about ***10x*** slower than SRAM
  - Disk is about ***10,000x*** slower than DRAM
  - Time to load block from disk > 1ms (> 1 million clock cycles)
    - CPU can do a t time
- **Consequences**
  - Large page (block) size: typically 4 K
    - Linux “huge pages” are 2 MB (d
  - Fully associative
    - Any VP can be placed in any PP
    - Requires a “large” mapping function – different from cache memories
  - Highly sophisticated, expensive replacement algorithms
    - Too complicated and open-ended to be implemented in hardware
  - Write-back rather than write-through

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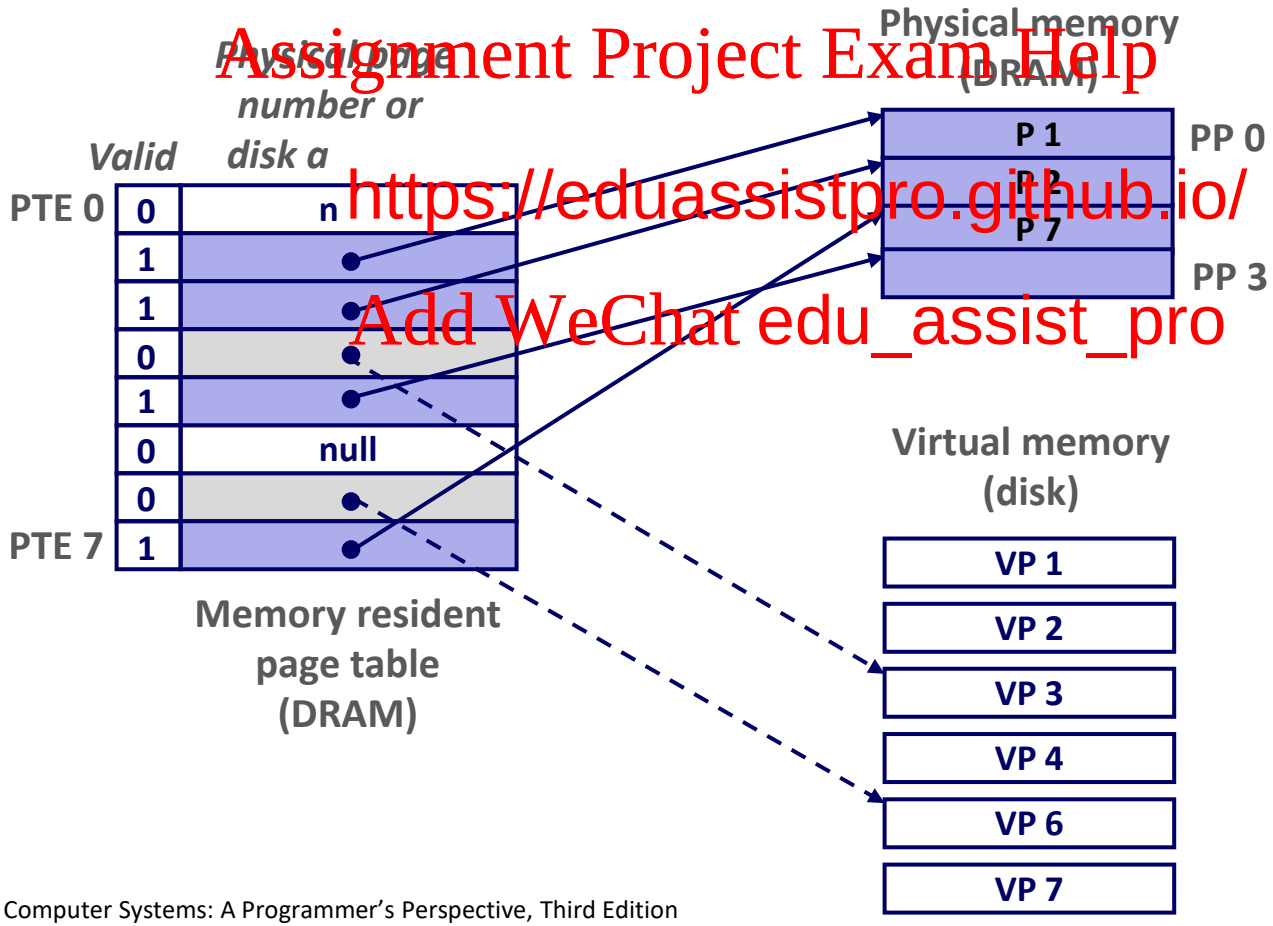
Enabling Data Structure: Page Table

- **A *page table* is an array of page table entries (PTEs) that maps virtual pages to physical pages.**
  - Per-process kernel data structure in DRAM



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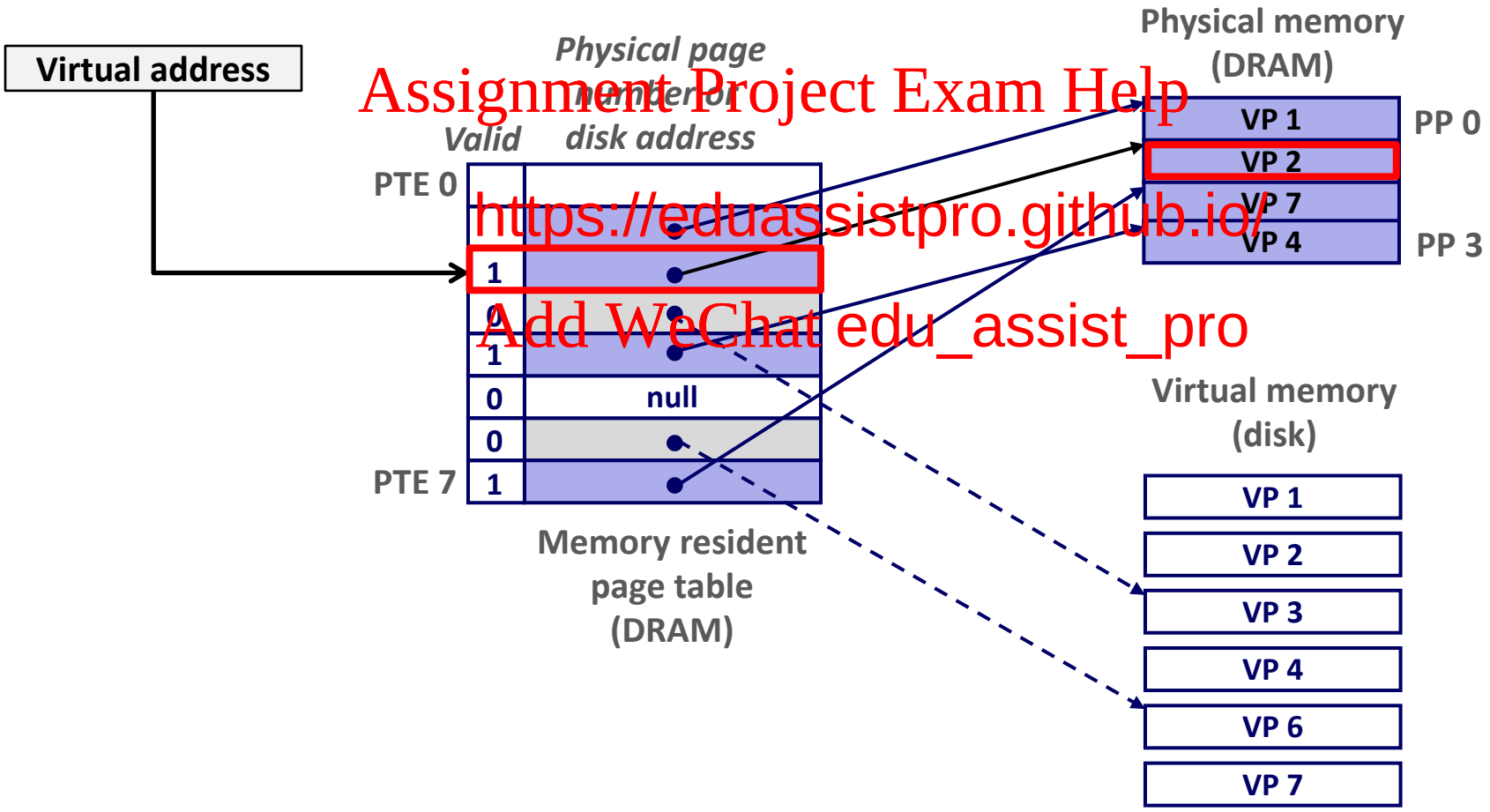
Page Hit

- ***Page hit:*** **reference to VM word that is in physical memory (DRAM cache hit)**



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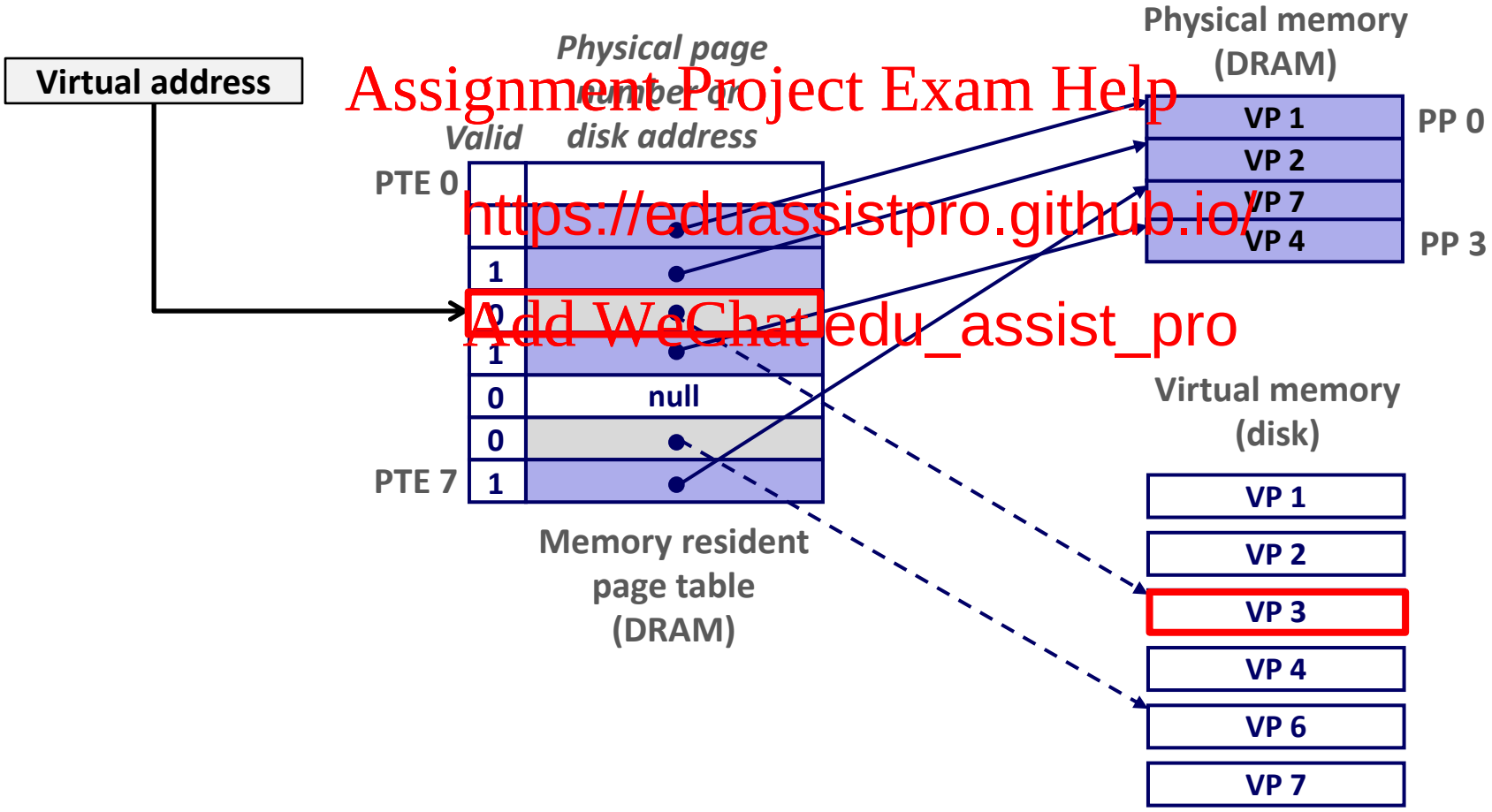
Page Fault

- ***Page fault:*** **reference to VM word that is not in physical memory (DRAM cache miss)**



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Triggering a Page Fault

- User writes to memory location

```
80483b7:      c7 05 10 9d 04 08 0d   movl   $0xd,0x8049d10
```

- That portion (page) of user's memory is currently on disk
- MMU triggers page
  - (More details in lat
  - Raise privilege level to supervisor mode
  - Causes procedure call to software page faul

```
int a[1000];
main ()
{
    a[500] = 13;
}
```

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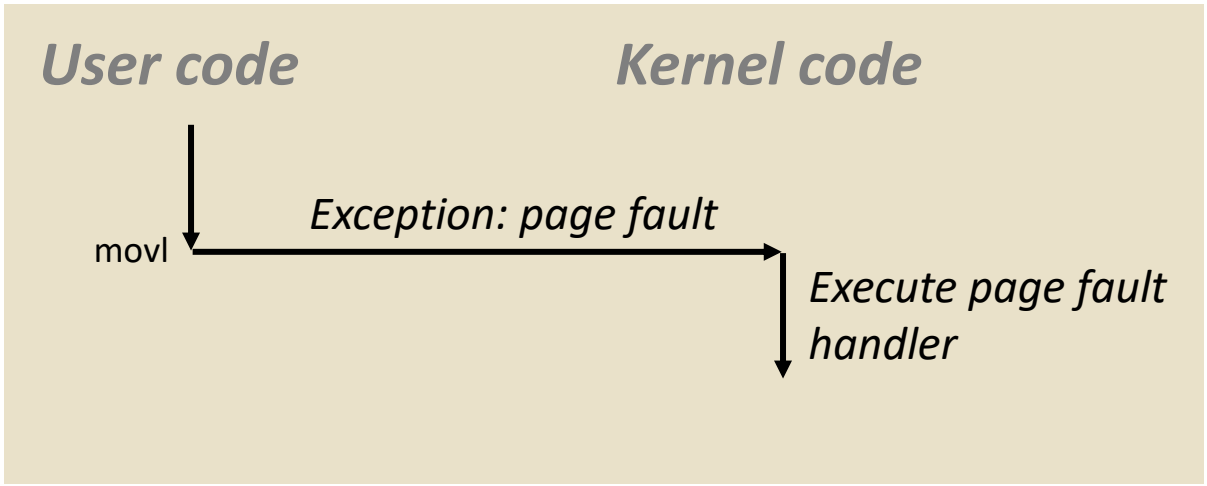
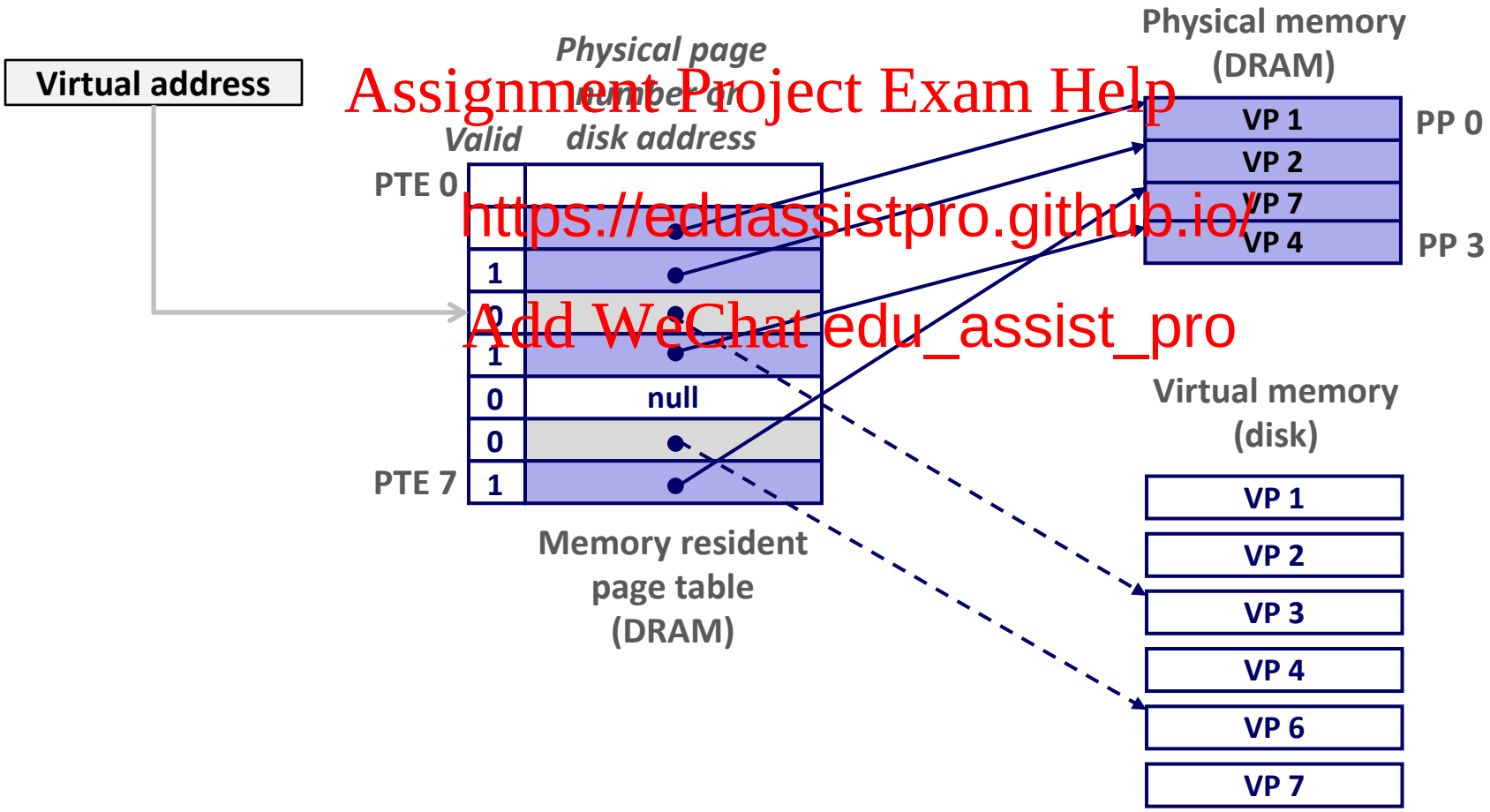


Handling Page Fault

- Page miss causes page fault (an exception)



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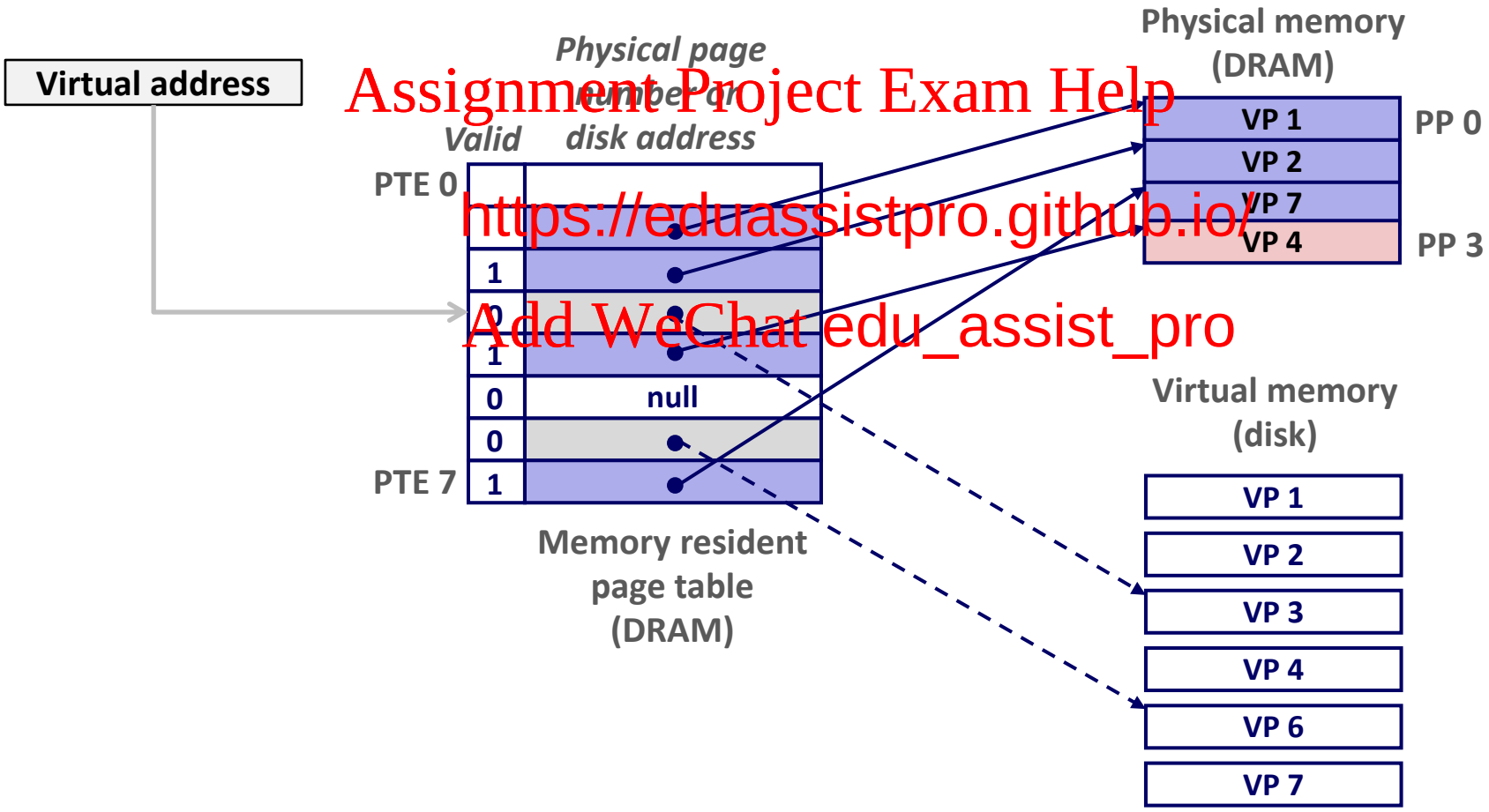
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a victim to be evicted (here VP 4)



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Handling Page Fault

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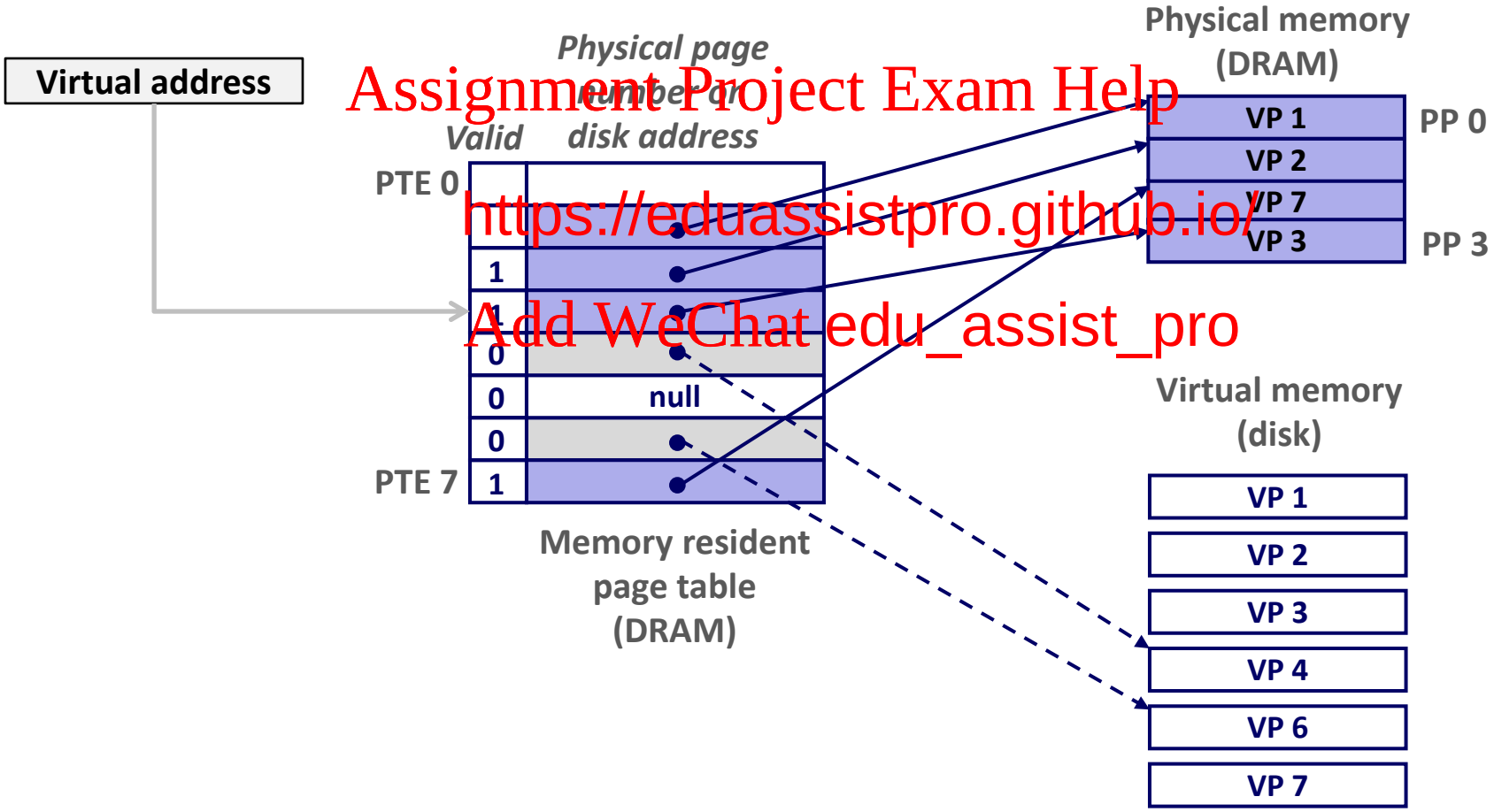

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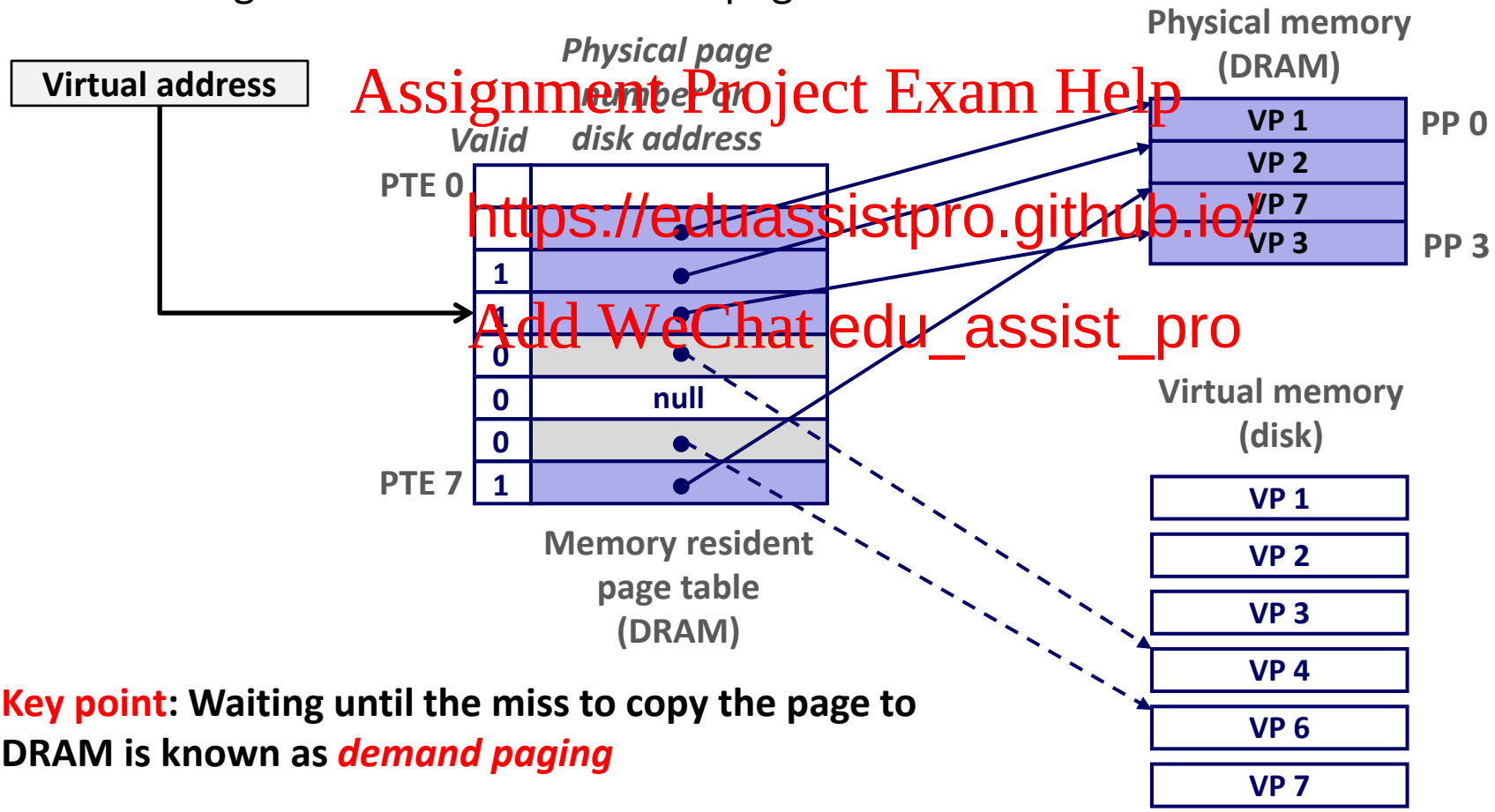
Handling Page Fault

- Page miss causes page fault (an exception)
- Page fault handler selects a victim to be evicted (here VP 4)
- Offending instruction is restarted: page hit!



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Key point: Waiting until the miss to copy the page to DRAM is known as *demand paging*

Completing page fault

- Page fault handler executes return from interrupt (**`iret`**) instruction
  - Like **`ret`** instruction, but also restores privilege level
  - Return to instruction that caused fault
  - But, this time there is no page fault

```
int a[1000];
main ()
{
    a[500] = 13;
}
```

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```
80483b7:                                    $0xd,0x8049d10
```

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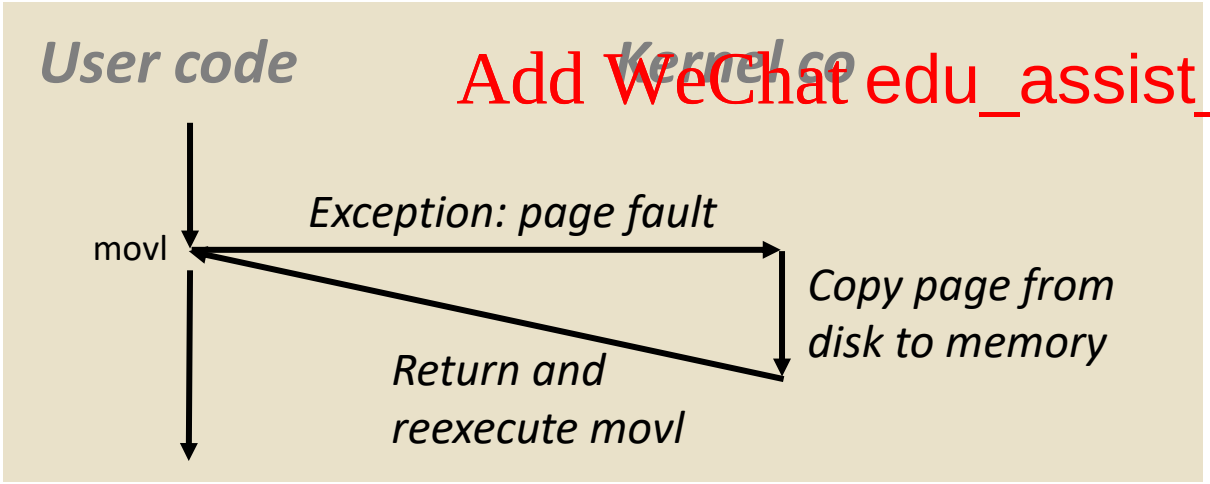
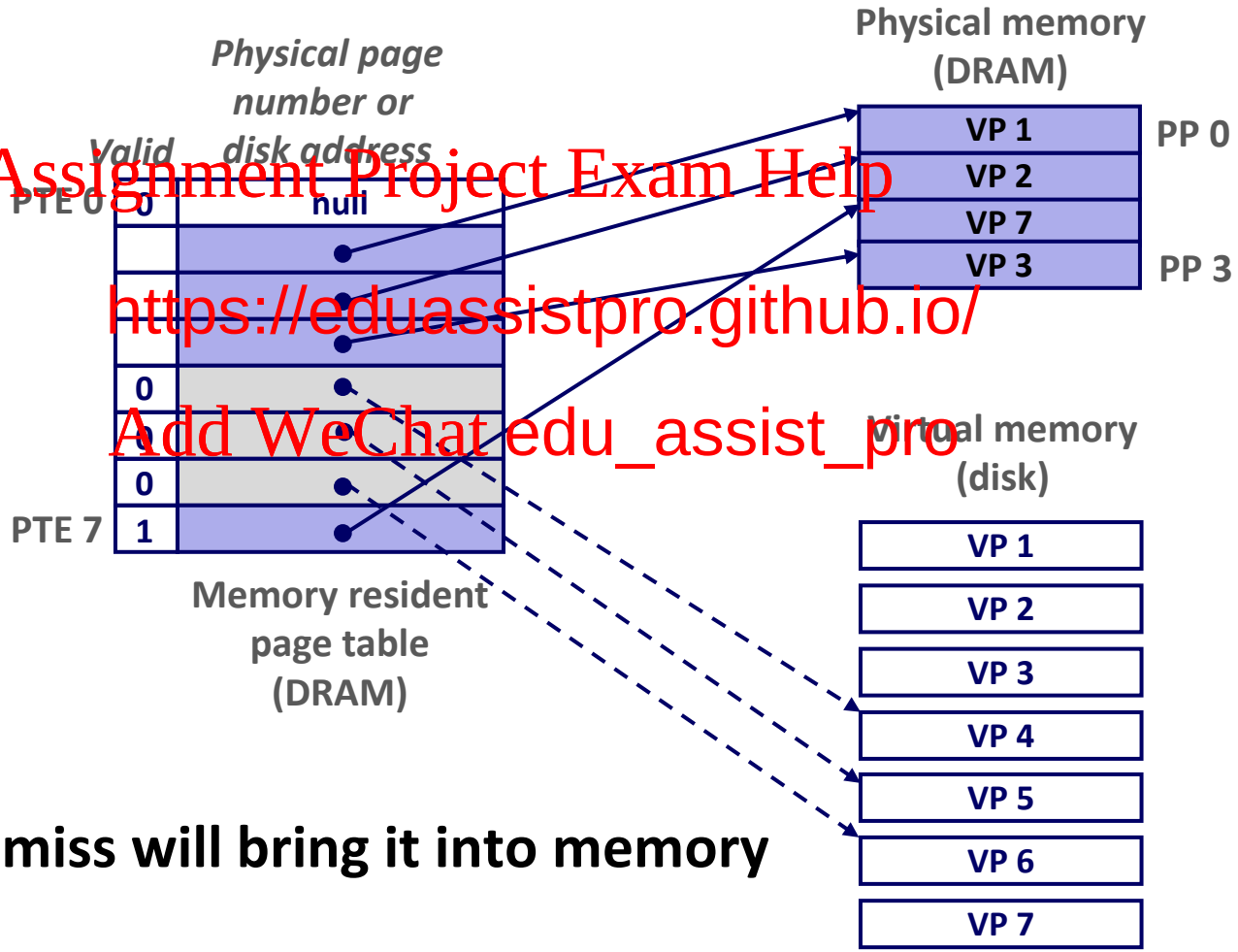


Allocating Pages

- Allocating a new page (VP 5) of virtual memory.



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- Subsequent miss will bring it into memory

Locality to the Rescue Again!

- **Virtual memory seems terribly inefficient, but it works because of locality.**

- **At any point in time, programs tend to access a set of active virtual pages called the *working set***
  - Programs with b e smaller working sets

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- **If (working set size < main mem**
  - Good performance for one process sses)

- **If (working set size > main memory size)**
  - *Thrashing:* Performance meltdown where pages are swapped (copied) in and out continuously
  - If multiple processes run at the same time, thrashing occurs if their total working set size > main memory size

Today

- Address spaces
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- **VM as a tool for memory management**
- VM as a tool for
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VM as a Tool for Memory Management

- **Key idea: each process has its own virtual address space**
  - It can view memory as a simple linear array
  - Mapping function scatters addresses through physical memory
    - Well-chosen mappings can improve locality

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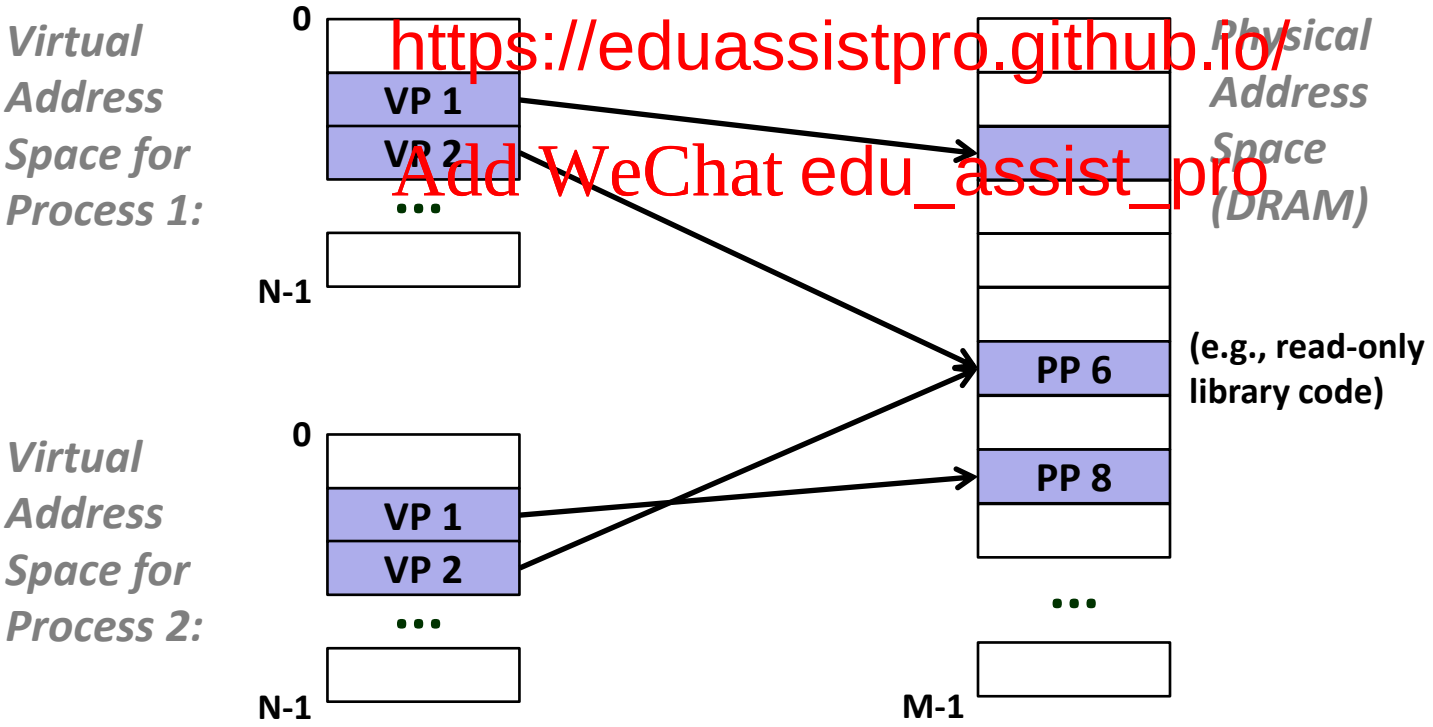

VM as a Tool for Memory Management

- **Simplifying memory allocation**
  - Each virtual page can be mapped to any physical page
  - A virtual page can be stored in different physical pages at different times
- **Sharing code and data among processes**
  - Map virtual pages to the same physical page (here: PP 6)

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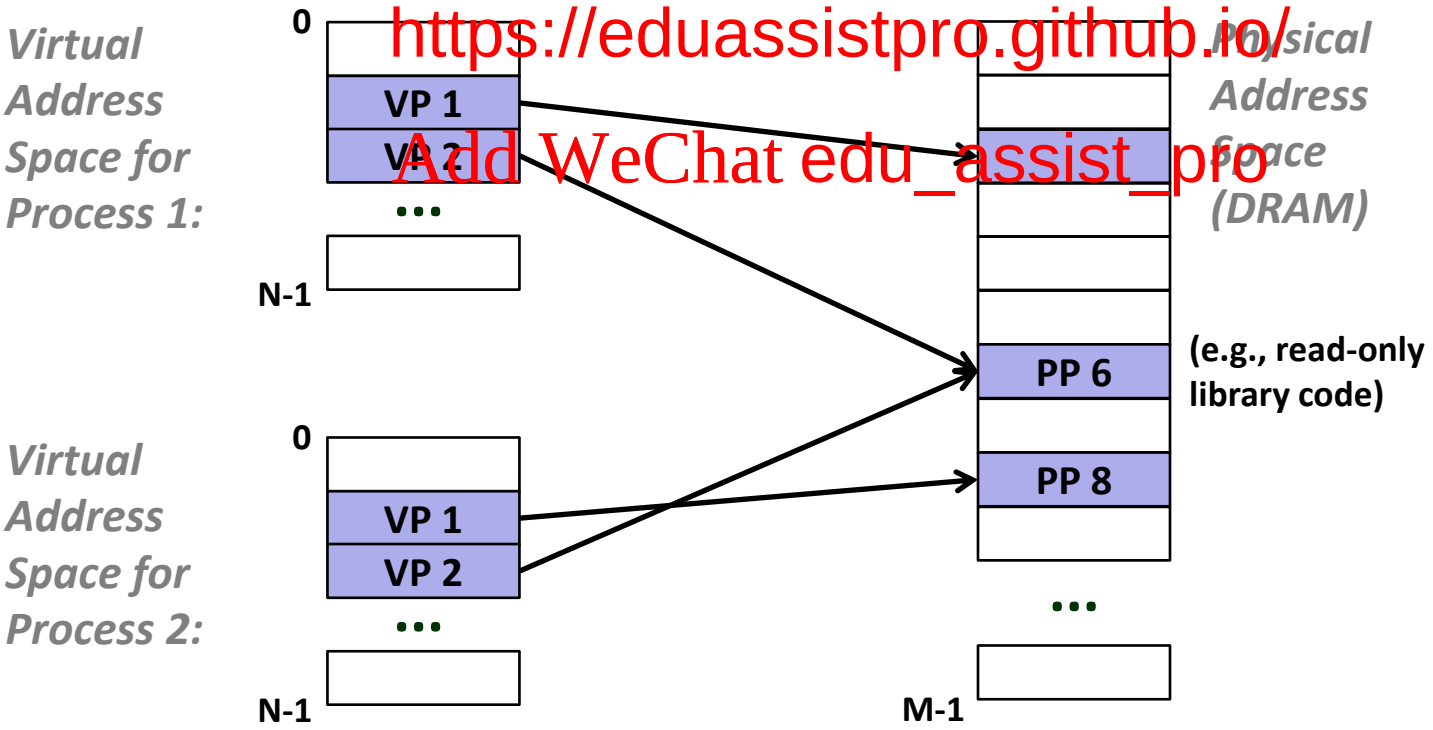

Simplifying Linking and Loading

- **Linking**
  - Each program has similar virtual address space
  - Code, data, and heap always start at the same addresse
- **Loading**
  - **`execve`** allocates virtual pages for .text and .data sections & creates PTEs marked as invalid
  - The **`.text`** and **`.data`** sections are copied, page by page, on demand by the virtual memory system

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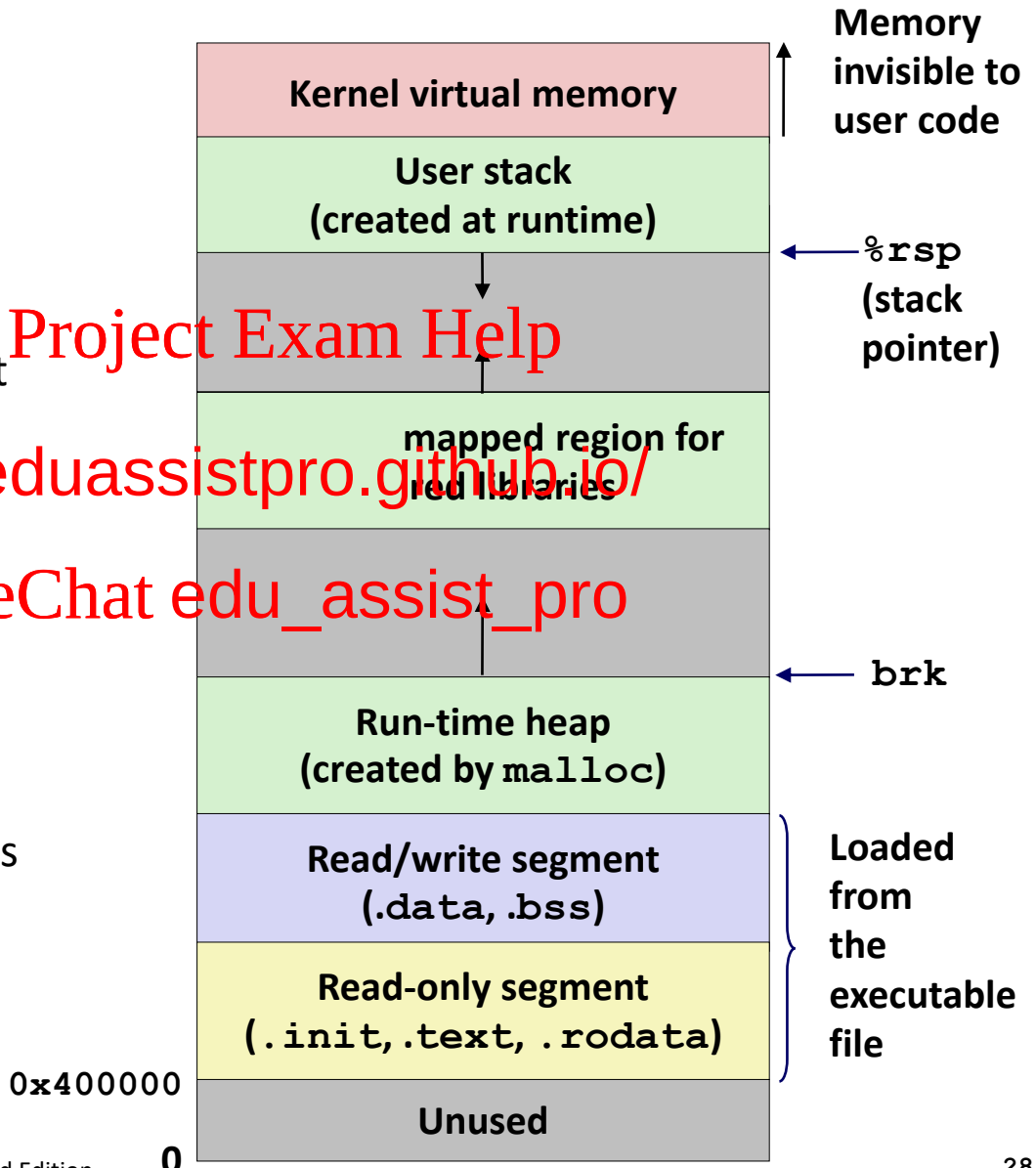

Today

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- VM as a tool for caching
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- **VM as a tool for**
- Address translat

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VM as a Tool for Memory Protection

- Extend PTEs with permission bits
- MMU checks these bits on each access

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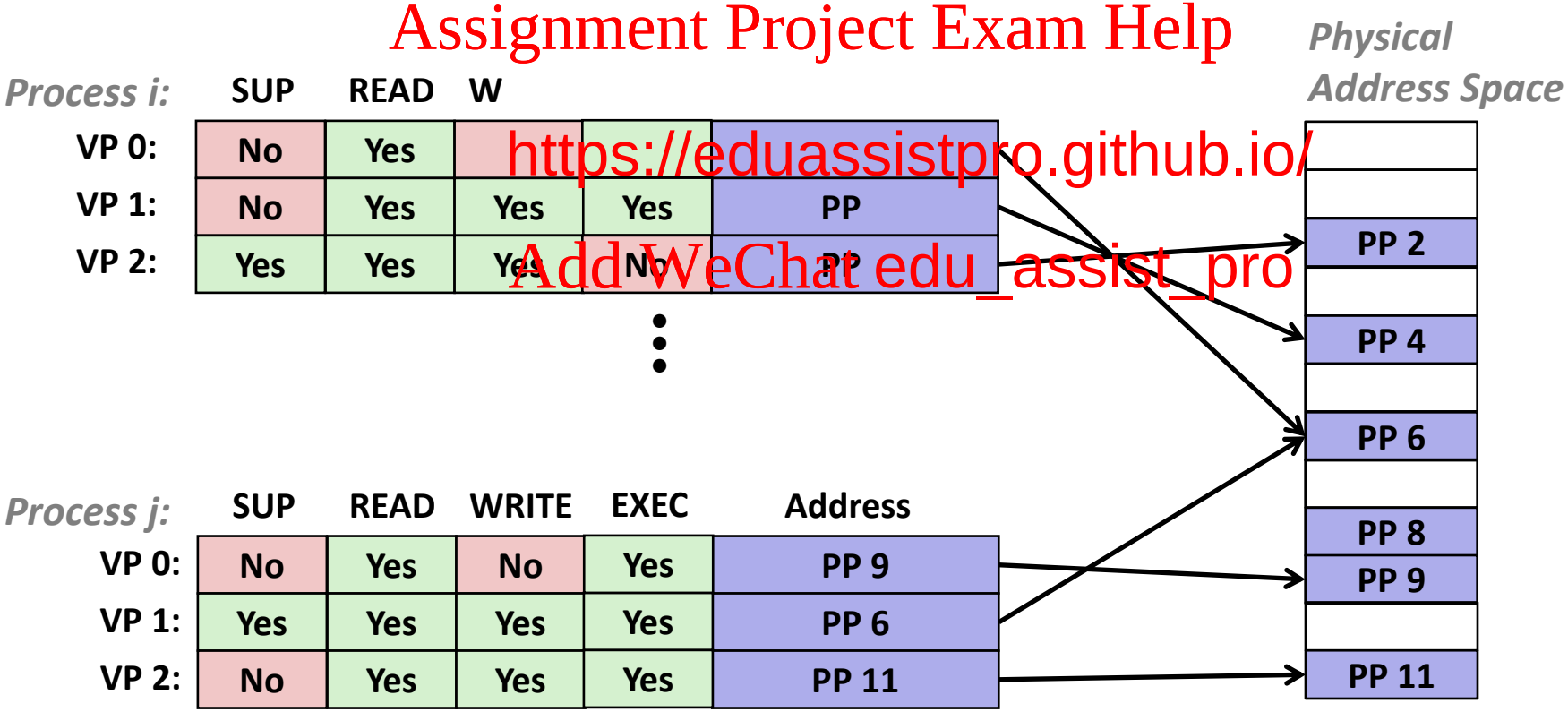

SUP: requires kernel mode

Quiz Time!

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Check out:

https://canvas.cmu.edu/courses/17808

Today

- Address spaces
- VM as a tool for caching
- VM as a tool for memory management
- VM as a tool for
- **Address translat**

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VM Address Translation

- **Virtual Address Space**
  - $V = \{0, 1, \ldots, N-1\}$
- **Physical Address Space**
  - $P = \{0, 1, \ldots, M-1\}$
- **Address Transla**
  - ***MAP: V → P U***
  - For virtual address ***a***:
    - ***MAP(a) = a'*** if data at virtual address ***a*** is at physical address ***a'*** in ***P***
    - ***MAP(a) = ∅*** if data at virtual address ***a*** is not in physical memory
      - Either invalid or stored on disk

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Summary of Address Translation Symbols

- **Basic Parameters**
  - **N = 2^n** : Number of addresses in virtual address space
  - **M = 2^m** : Number of addresses in physical address space
  - **P = 2^p** : Page size (bytes)
- **Components of**
  - **VPO**: Virtual pa
  - **VPN**: Virtual page number
- **Components of the physical address (PA)**
  - **PPO**: Physical page offset (same as VPO)
  - **PPN:** Physical page number

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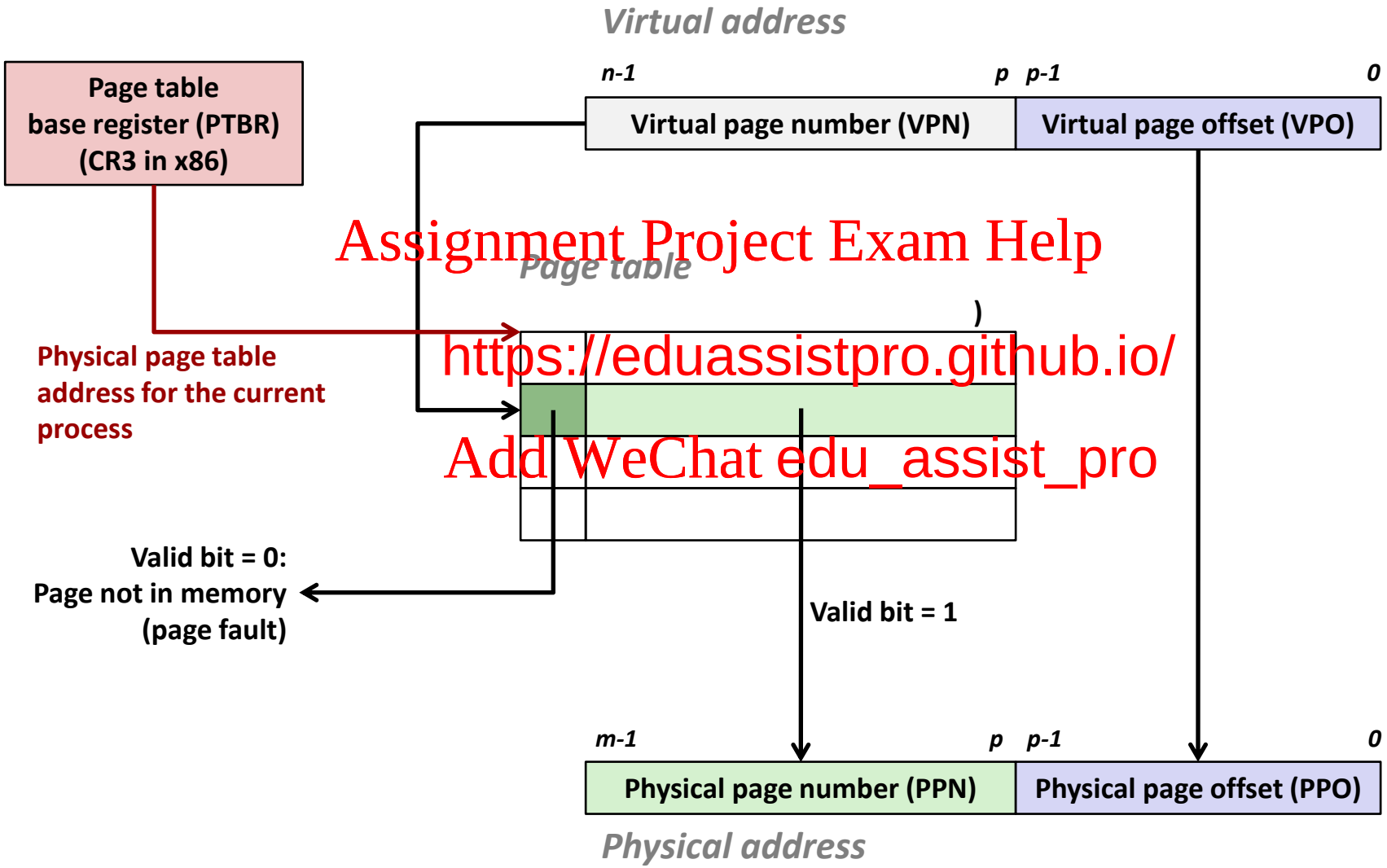
Address Translation With a Page Table



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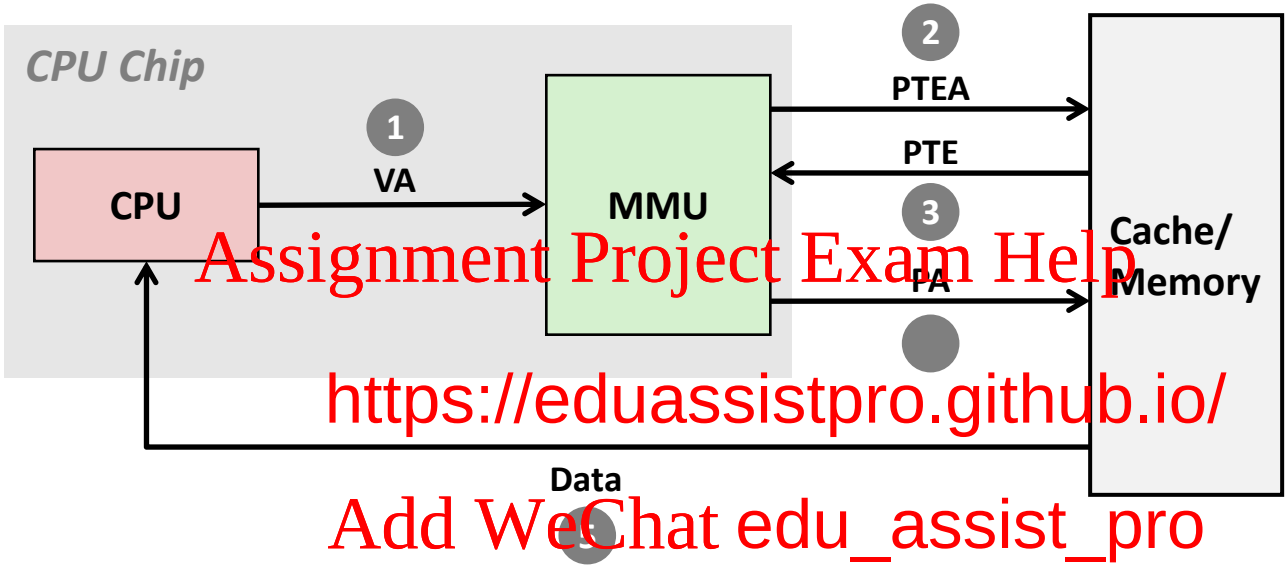
Address Translation: Page Hit



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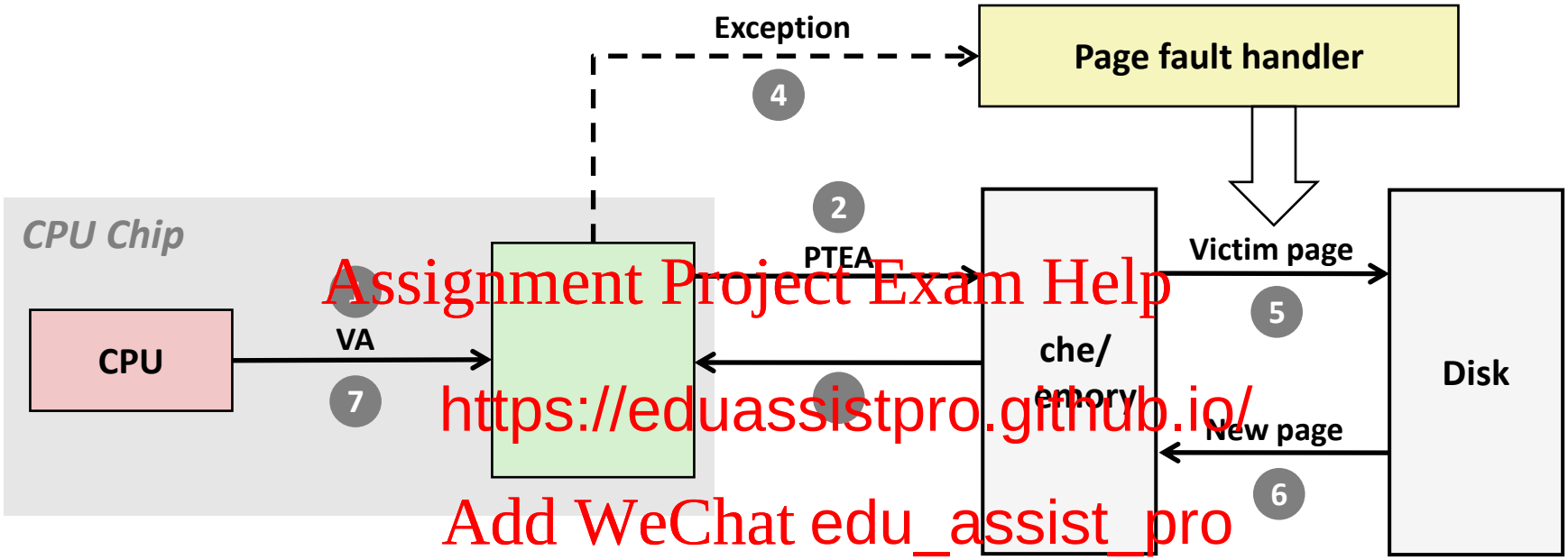
1) Processor sends virtual address to MMU

2-3) MMU fetches PTE from page table in memory

4) MMU sends physical address to cache/memory

5) Cache/memory sends data word to processor

Address Translation: Page Fault



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1) Processor sends virtual address to MMU

2-3) MMU fetches PTE from page table in memory

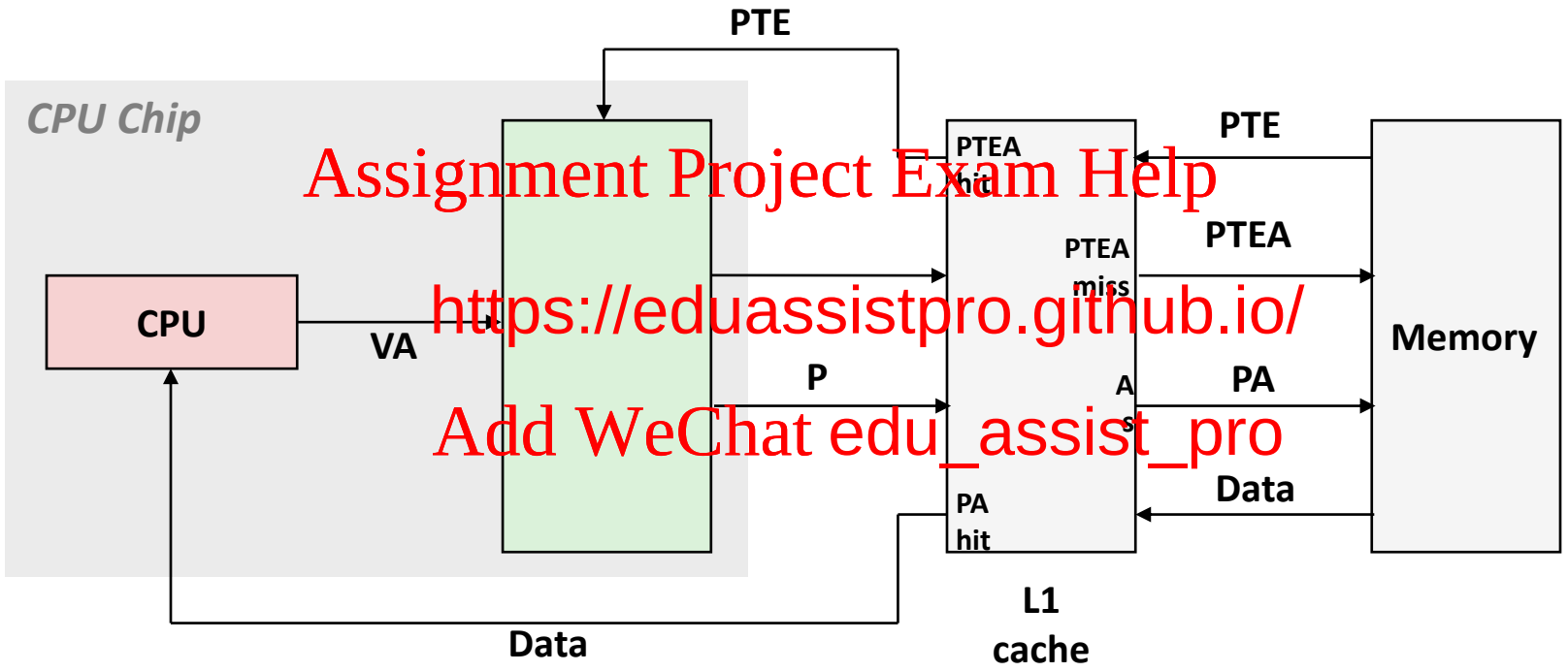
4) Valid bit is zero, so MMU triggers page fault exception

5) Handler identifies victim (and, if dirty, pages it out to disk)

6) Handler pages in new page and updates PTE in memory

7) Handler returns to original process, restarting faulting instruction

Integrating VM and Cache



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VA: virtual address, PA: physical address, PTE: page table entry, PTEA = PTE address

Speeding up Translation with a TLB

- **Page table entries (PTEs) are cached in L1 like any other memory word**
  - PTEs may be evicted by other data references
  - PTE hit still requires a small L1 delay
- **Solution: *Transl*** B)
  - Small set-associative hardware cac
  - Maps virtual page numbers to phy bers
  - Contains complete page table entries for small number of pages

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Summary of Address Translation Symbols

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  - **P = 2^p** : Page size (bytes)
- **Components of**
  - ***TLBI**: TLB index*
  - ***TLBT**: TLB tag*
  - **VPO**: Virtual page offset
  - **VPN**: Virtual page number
- **Components of the physical address (PA)**
  - **PPO**: Physical page offset (same as VPO)
  - **PPN:** Physical page number

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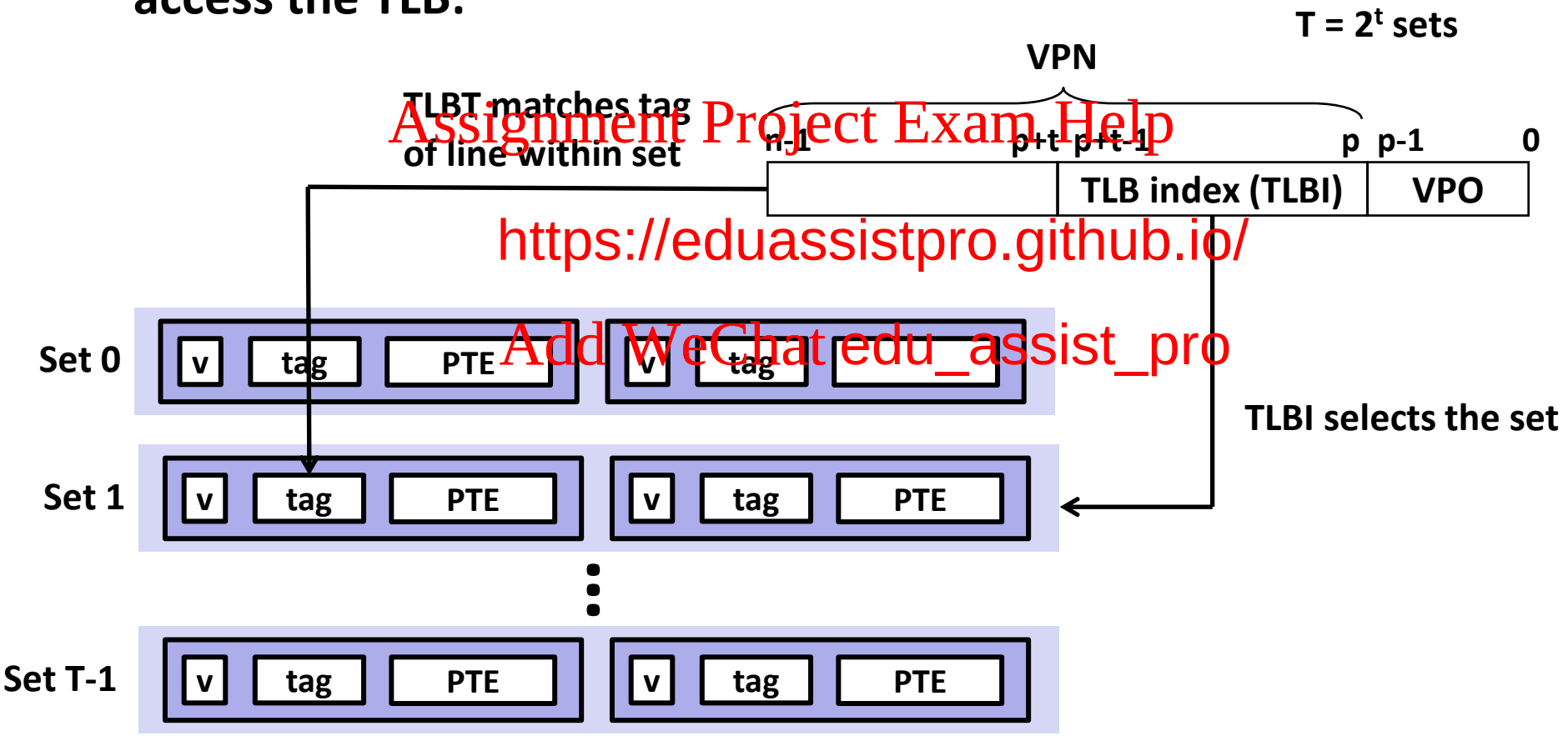
Accessing the TLB

- MMU uses the VPN portion of the virtual address to access the TLB:



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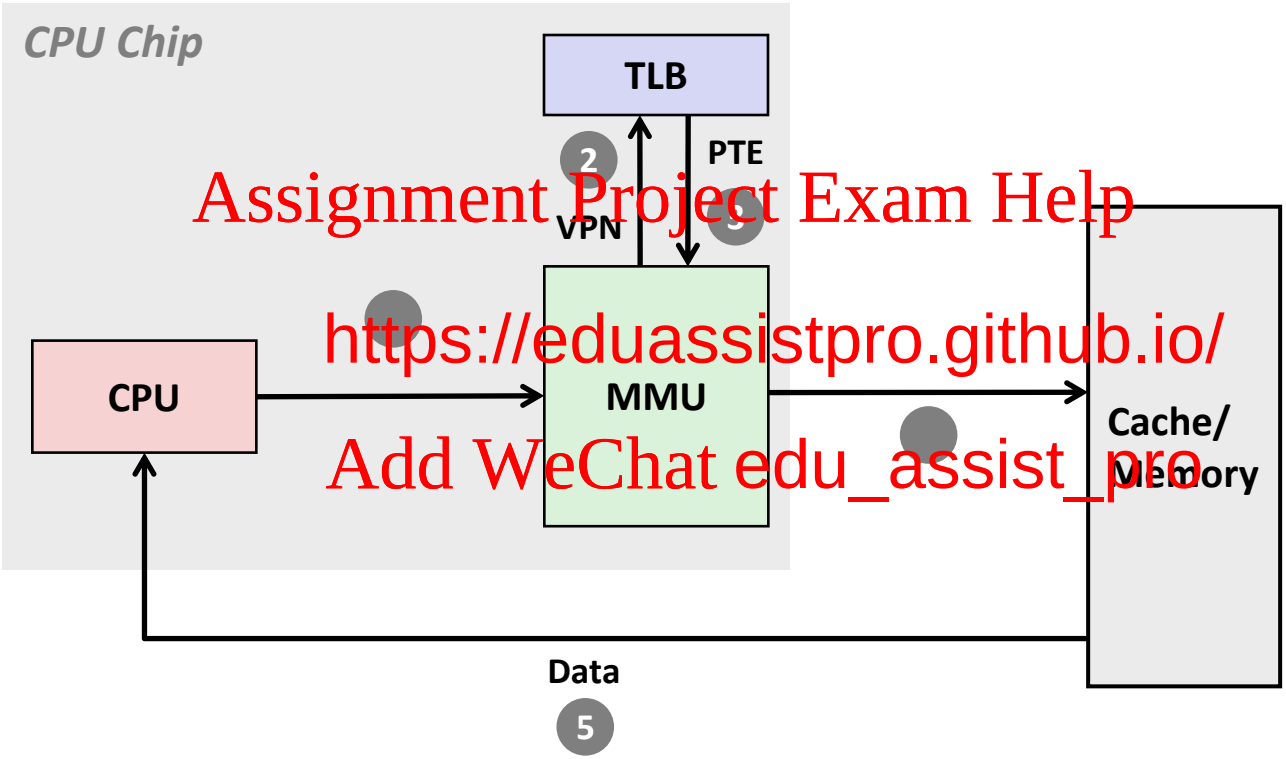
TLB Hit



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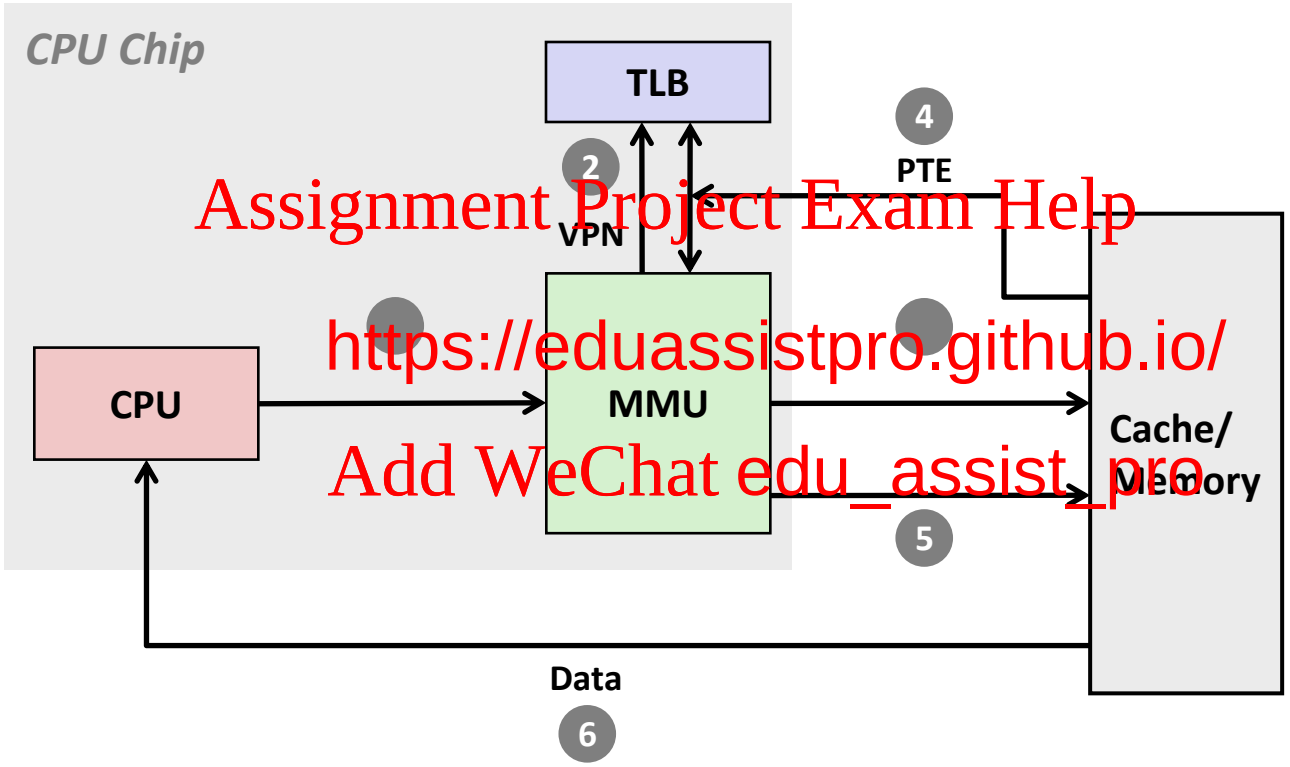
A TLB hit eliminates a cache/memory access

TLB Miss



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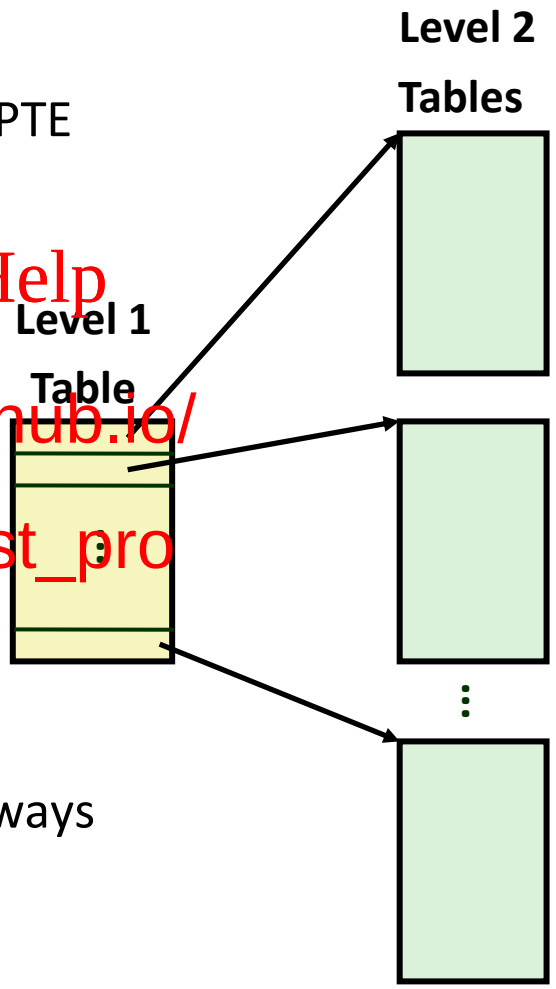
A TLB miss incurs an additional cache/memory access (the PTE)

Fortunately, TLB misses are rare. Why?

Multi-Level Page Tables

- **Suppose:**
  - 4KB (2^{12}) page size, 48-bit address space, 8-byte PTE
- **Problem:**
  - Would need a 5
    - $2^{48} * 2^{-12} * 2$
- **Common solution: Multi-level page table**
- **Example: 2-level page table**
  - Level 1 table: each PTE points to a page table (always memory resident)
  - Level 2 table: each PTE points to a page (paged in and out like any other data)



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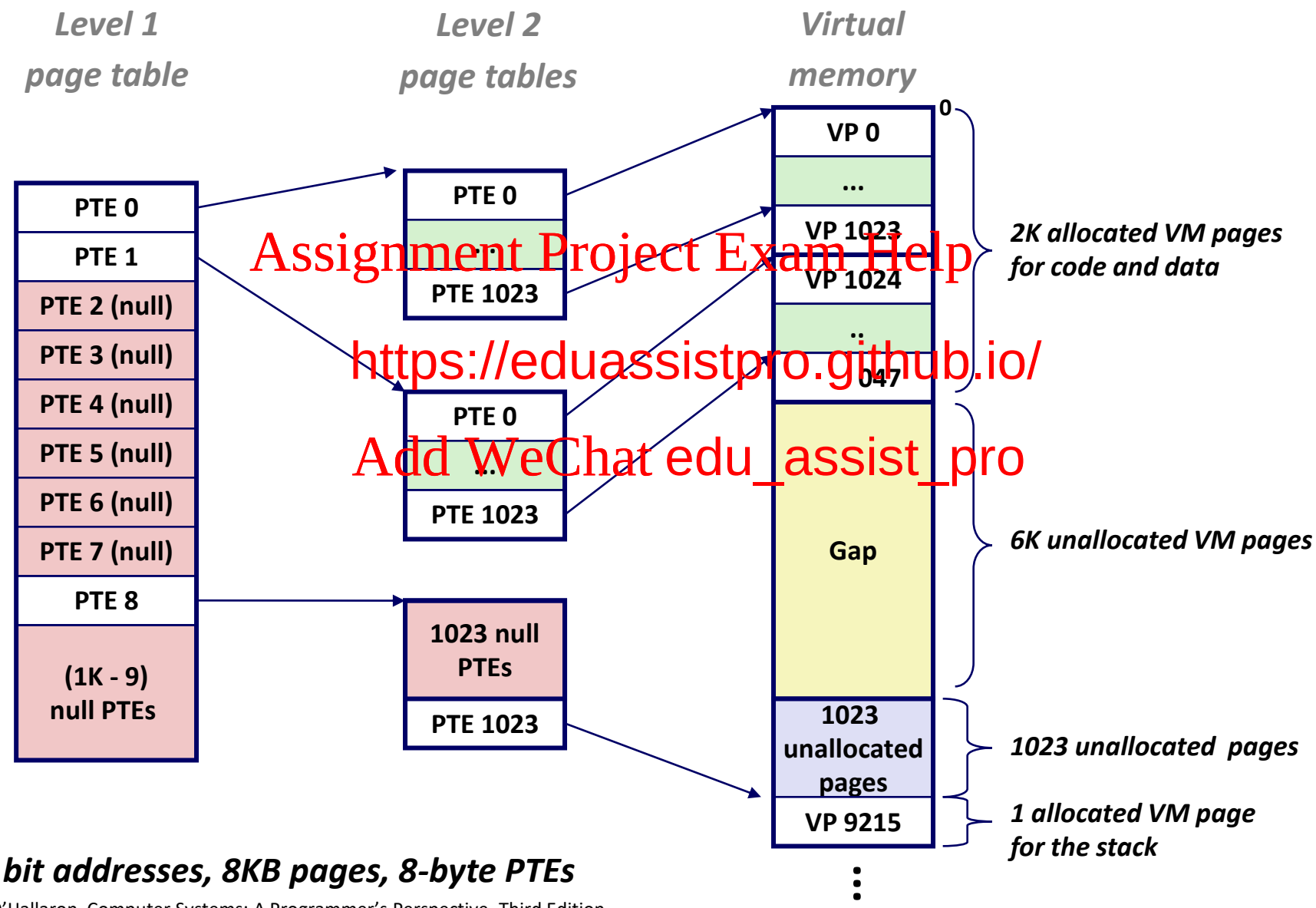
A Two-Level Page Table Hierarchy



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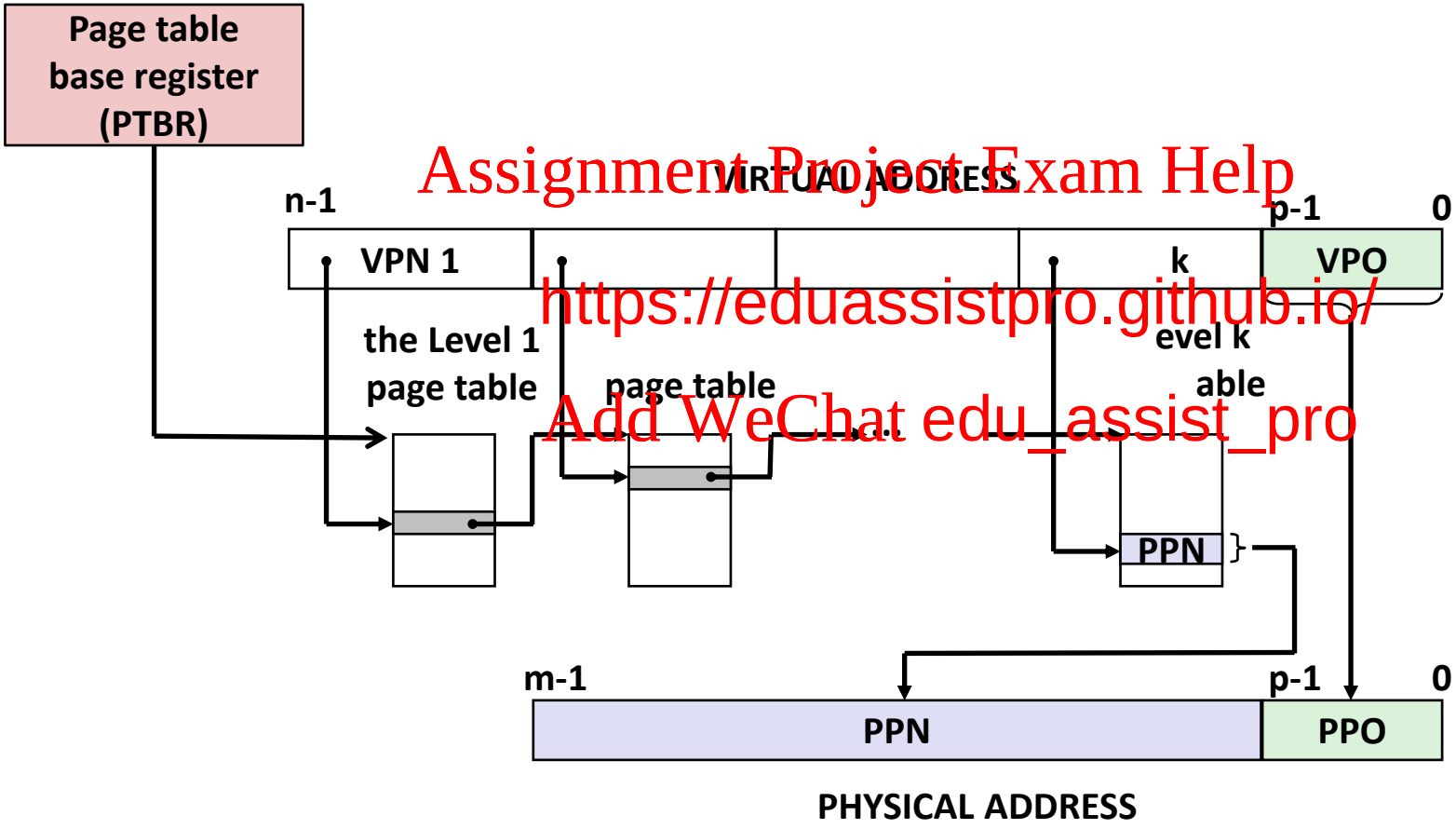
64 bit addresses, 8KB pages, 8-byte PTEs

Translating with a k-level Page Table



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Summary

- **Programmer's view of virtual memory**
  - Each process has its own private linear address space
  - Cannot be corrupted by other processes
- **System view of virtual memory**
  - Uses memory e mory pages
    - Efficient onl
  - Simplifies memory management a ng
  - Simplifies protection by providing a convenient interpositioning point to check permissions
- **Implemented via combination of hardware & software**
  - MMU, TLB, exception handling mechanisms part of hardware
  - Page fault handlers, TLB management performed in software

Assignment Project Exam Help
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