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CMPE 12 Final Exam - Version A

Winter 2019

Bits

1. How many bits are needed to encode one ASCII character?
   - ◯ A. 8 bits
   - ◯ B. 10 bits
   - ◯ C. 6 bits
   - ⊗ D. 7 bits
   - ◯ E. 9 bits
2. What is the size of a word in MIPS? Select all that apply.
   - ◯ A. 8 bytes
   - ⊗ B. 32 bits
   - ⊗ C. 8 nybbles
   - ⊗ D. 4 bytes
   - ◯ E. 32 bytes

Binary Arithmetic

3. Perform the following 12-b

```
    0b  0 1 1 1  1 1 0 0  0 1 0 0
  + 0b  0 0 0 0  0 0 0 1  1 1 0 0
```


   - ◯ A. `000011011100`
   - ◯ B. `000001010100`
   - ◯ C. `011111100001`
   - ◯ D. `000010100111`
   - ⊗ E. `011111100000`
4. Which of these 8-bit two's complement computations has carry out but no overflow? Select all that apply.
   - ◯ A. `0x1E + 0x26 = 0x44`
   - ⊗ B. `0xFA + 0xED = 0xE7`
   - ◯ C. `0x0F + 0x85 = 0x94`
   - ◯ D. `0x01 + 0x7F = 0x80`
   - ⊗ E. `0xFF + 0x01 = 0x00`
5. A logical right shift and an arithmetic right shift perform the same operation
   - ◯ A. True
   - ⊗ B. False

Data Representation

6. Which IEEE 754 single precision floating point number is furthest from zero?
   - ◯ A. `0xC70FFFFF`
   - ⊗ B. `0x47700000`
   - ◯ C. `0x1F8FFFFF`
   - ◯ D. `0x380FFFFF`
   - ◯ E. `0xB8700000`

7. What is the following base 9 number in base 5? 106_9
   - ◯ A. 123_5
   - ⊗ B. 322_5
   - ◯ C. 742_5
   - ◯ D. 305_5
   - ◯ E. 222_5

8. What is the range of values for an 8-bit two's complement integer?
   - ◯ A. 0 to 255
   - ⊗ B. -128 to 127
   - ◯ C. -127 to 128
   - ◯ D. -128 to 128
   - ◯ E. -127 to 127

9. What is the following 8-bit t

   `11010110`

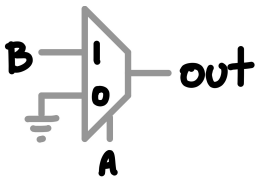
   - ◯ A. `10110110`
   - ⊗ B. `10101010`
   - ◯ C. `01010110`
   - ◯ D. `00101010`
   - ◯ E. `11010110`

10. What is the following base 3 number in base 7? 2101_3
    - ◯ A. 736_7
    - ◯ B. 123_7
    - ⊗ C. 121_7
    - ◯ D. 64_7
    - ◯ E. 46_7

11. 6-bit two's complement, signed magnitude, and unsigned all represent the same number of integers, some just have more negative than positive.
    - ◯ A. True
    - ⊗ B. False

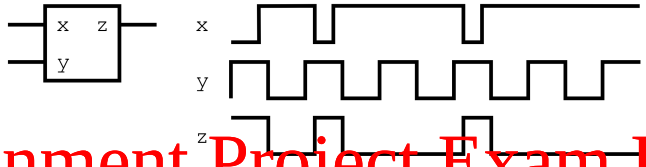
Logic Design

12. This figure is logically equivalent to which circuit?



- ◯ A. XNOR gate
- ◯ B. XOR gate
- ⊗ C. AND gate
- ◯ D. XOR gate
- ◯ E. Positive D-Latch

13. What device does this timing diagram represent?

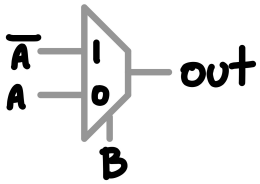


- ◯ A. Negative edge triggered D flip flop
- ◯ B. SR latch active high
- ◯ C. Positive edge trigge
- ◯ D. D latch
- ⊗ E. SR latch active low

14. This figure is logically equivalent to which circuit?

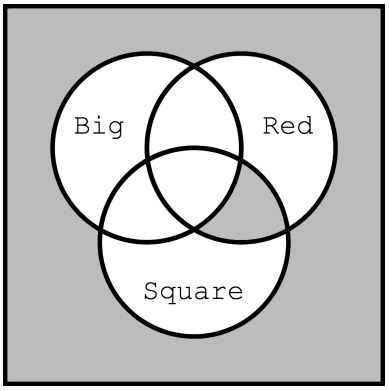
- ◯ A. AND gate
- ◯ B. XOR gate
- ◯ C. Negative D-Flip Flop
- ◯ D. XNOR gate
- ⊗ E. OR gate

15. This figure is logically equivalent to which circuit?



- ⊗ A. XOR gate
- ⊗ B. XOR gate
- ◯ C. Negative D-Latch
- ◯ D. Positive D-latch
- ◯ E. XNOR gate

16. Select the Boolean expression matching the filled areas of this Venn diagram.



- ◯ A. $(\texttt{Red} + \texttt{Square}) \cdot \overline{(\texttt{Big} \cdot \texttt{Red} \cdot \texttt{Square})} \cdot (\texttt{Big} + \texttt{Red} + \texttt{Square})$
- ◯ B. $\texttt{Red} \cdot \texttt{Square} \cdot \overline{(\texttt{Big} \cdot \texttt{Red} \cdot \texttt{Square})} \cdot \overline{(\texttt{Big} + \texttt{Red} + \texttt{Square})}$
- ◯ C. $(\texttt{Red} + \texttt{Square}) + \overline{(\texttt{Big} \cdot \texttt{Red} \cdot \texttt{Square})} \cdot (\texttt{Big} + \texttt{Red} + \texttt{Square})$
- ◯ D. $\texttt{Red} \cdot \texttt{Square} \cdot \overline{(\texttt{Big} \cdot \texttt{Red} \cdot \texttt{Square})}$
- ⊗ E. $\texttt{Red} \cdot \texttt{Square} \cdot \overline{(\texttt{Big} \cdot \texttt{Red} \cdot \texttt{Square})} + \overline{(\texttt{Big} + \texttt{Red} + \texttt{Square})}$

17. How many outputs does a 4-16 decoder have?

- ◯ A. 64
- ◯ B. 4
- ◯ C. 1
- ⊗ D. 16
- ◯ E. 32

Memory

18. How many bits are needed to represent a memory location address in a 4TB m addressable?

- ◯ A. 28
- ⊗ B. 36
- ◯ C. 64
- ◯ D. 34
- ◯ E. 2^{34}

19. How much memory is allocated with the following line of code?

```
.asciiz "ce_12"
```

- ⊗ A. 6 bytes
- ◯ B. 5 words
- ◯ C. 4 bytes
- ◯ D. 2 words
- ◯ E. 5 bytes

For the following two questions, assume a portion of data memory looks like this:

```
ADDRESS      CONTENTS
0x10011085   0xCD
0x10011084   0xAB
0x10011083   0x87
0x10011082   0x65
0x10011081   0x43
0x10011080   0x21
```

20. Assuming big endian memory storage, what is in $t7 after the following instructions?

```
ADDI $t0, $zero, 0x10011080
LH   $t7, 2($t0)
SW   $t7,  ($t0)
LW   $t7,  ($t0)
```

- ◯ A. 0x87654321
- ◯ B. 0x00008765
- ⊗ C. 0x00006587
- ◯ D. 0xFFFF8765
- ◯ E. 0x01004321

21. Assuming little endian memory storage, what is in $t0 after the following instructions?

```
LI $t3, 0x1001108
LW $t0, ($t3)
```


- ◯ A. 0x00008765
- ◯ B. 0x5678BADC
- ◯ C. 0x6587ABCD
- ⊗ D. Undefined. There will be an alignment error.
- ◯ E. 0xCDAB8765

ASCII

22. Decode the following ASCII string. Values are given in hex.

44 69 64 20 79 6f 75 20 65 76 65 72 20 68 65 61 72 20 74 68 65 20 74 72 61 67 65 64 79 20 6f 66 20 44 61 72 74 68 20 50 6c 61 67 75 65 69 73 20 74 68 65 20 57 69 73 65 3f

- ⊗ A. Did you ever hear the tragedy of Darth Plagueis the Wise?
- ◯ B. No! Try not. Do. Or do not. There is no try.
- ◯ C. Help me, Obi-Wan Kenobi. You're my only hope.
- ◯ D. I have a bad feeling about this.
- ◯ E. I find your lack of faith disturbing.

23. Say that a user enters a single ASCII character in the range'0'-'9'. Assume that the user input is stored in $v0. Which MIPS instruction would you use to convert their input into an integer in the range 0-9?

- ◯ A. `subi $t0, $v0, 49`
- ⊗ B. `subi $t0, $v0, 48`
- ◯ C. `addi $t0, $v0, 48`
- ◯ D. `subi $t0, $v0, 30`
- ◯ E. `subi $t0, $v0, 60`

MIPS

24. What is the value of $t0 after the following instructions are executed (represented in hex)?

```
li   $t1, 5
li   $t0, 5
loop:
   sll  $t0, $t0, 1
   addi $t1, $t1, -1
   bgez $t1, loop

   li   $v0, 10
   syscall
```

- (X) A. 0x00000140
- ( ) B. 0x0001FA00
- ( ) C. 0x000000A0
- ( ) D. 0x00001400
- ( ) E. 0x001000FA

25. Which MIPS32 native/basic instruction(s) perform the same function as the following pseudo instruction?

```
ORI $s0 $s3 0xABCDEF00
```


- ( ) A.
```
ADDIU $1  $0  0xAB
SRL   $1  $1  16
OR    $16 $13 $1
```
- ( ) B.
```
ORI   $16 $13 0xAB
```
- ( ) C.
```
LI    $1  0xABCDEF00
OR    $16 $13 $1
```
- ( ) D.
```
LUI   $1  0xEF00
OR    $16 $13 $1
ORI   $16 $16 0xABCD
```
- (X) E.
```
LUI   $1  0xABCD
ORI   $1  $1  0xEF00
OR    $16 $13 $1
```

26. Which register(s) in MIPS must the callee preserve?

- ( ) A. $t0 - $t9
- (X) B. $s0 - $s7
- ( ) C. $sp
- ( ) D. $v0 - $v1
- ( ) E. $a0 - $a3

27. What is the value of $t0 after the following instructions are executed?

```
li   $t0, 4
li   $t1, 5
add  $t0, $t1, $t0
addi $t0, $t0, -1
xor  $t0, $t0, $t0
```

- (X) A. 0
- ( ) B. 6
- ( ) C. 10
- ( ) D. 8
- ( ) E. Not enough information given

28. What is the least significant byte stored in $t0 after the following MIPS commands execute?

```
li   $t0, 0x9F
andi $t0, $t0, 0x0F
```

- (X) A. 00001111
- ( ) B. 10011111
- ( ) C. 11110000
- ( ) D. 00011111
- ( ) E. 00000000

29. What is printed to the screen after the following MIPS commands execute?

```
1   .data
2   prompt1: .asciiz "I"
3   prompt2: .asciiz " LOVE"
4   prompt3: .asciiz " CE 12 FINAL"
5
6   .text
7   li $v0, 4
8   la $a0, prompt1
9   syscall
```

- ( ) A. I
  LOVE
- ( ) B. I
- (X) C. I LOVE
- ( ) D. I LOVE CE12 FINAL
- ( ) E. nothing

30. Processing an instruction requires the following steps

    a. Execute operation/evaluate effective address
    b. Write value to register file
    c. Fetch instruction from memory
    d. Access data from memory
    e. Decode instruction

    What is the correct ordering for these steps?

    ◯ A. ecadb
    ⊗ B. ceadb
    ◯ C. caedb
    ◯ D. deacb
    ◯ E. aebdc

31. Which combination of MIPS instructions perform a pop operation of one word from the stack?

    ◯ A.
    ```
    sw   $t0, ($sp)
    subi $sp, $sp, 4
    ```
    ◯ B.
    ```
    addi $sp, $sp, 4
    lw   $t0, ($sp)
    ```
    ⊗ C.
    ```
    lw   $t0, ($sp)
    addi $sp, $sp, 4
    ```
    ◯ D.
    ```
    subi $sp, $sp, 4
    sw   $t0, ($sp)
    ```
    ◯ E. none of the above

The next four questions will refer t

```
1   .text
2   la    $a0, str1
3   addiu $v0, $zero, 4
4   syscall
5
6   la    $a0, str2
7   syscall
8
9   lbu   $a0, str3
10  addiu $v0, $zero, 11
11  syscall
12
13  addiu $v0, $zero, 1
14  syscall
15
16  addiu $v0, $zero, 10
17  syscall
18
19  .data
20  str1: .ascii "hello"
21  str2: .asciiz "there"
22  str3: .byte 0x21 0x21 0x00
```

32. Assume you changed line 21 in the original program from

```
str2: .asciiz "there"
```

to

```
str2: .ascii "there"
```

What will be printed to the screen after the altered program completes execution?

- ◯ A. hellothere!!33
- ◯ B. hellotherethere!33
- ◯ C. hellothere!33
- ⊗ D. hellothere!!there!!!33
- ◯ E. hellothere!!there!!33

33. What will be printed to the screen after the original program completes execution?

- ⊗ A. hellotherethere!33
- ◯ B. hellothere!!33
- ◯ C. hellotherethere!!33
- ◯ D. hellothere!33
- ◯ E. hellotherethere!21

34. Assume you changed line 13 in the original program from

```
addiu $v0, $zero, 1
```

to

```
addiu $v0, $zero, 35
```

What will be printed to the scr

- ⊗ A. hellotherethere!0
- ◯ B. hellothere!00000
- ◯ C. hellothere!!00000000000000000000000000100001
- ◯ D. hellotherethere!0x00000021
- ◯ E. hellotherethere!33

35. Given the branch instruction in machine code

```
000101 00010 01000 1111111111111100
```

Assume the branch target address is 0x2004, what is the address of the branch instruction?

- ◯ A. None of the other answers
- ◯ B. `0x2004`
- ⊗ C. `0x2010`
- ◯ D. `0x2018`
- ◯ E. `0x2014`

The addresses of some of the instructions of the following program are listed. Please refer to the program for the next two questions

```
            .text

            main:
0x00400000  jal   getString     #sets v0 to address of string
            move  $a0, $v0
            li    $v0, 4
0x0040000c  syscall

            li    $v0, 10
            syscall

0x00400018  getString:
            la     $v0, string1
0x00400020  jr     $ra


.data
string1:    .asciiz  "Greetings!"
```


36. What is the value of $pc right after the jal is taken?
    - ◯ A. 0x004000
    - ◯ B. 0x00400000
    - ⊗ C. 0x00400018
    - ◯ D. 0x00400020
    - ◯ E. 0x00400004

37. What is the value of $ra right after the jal is taken?
    - ◯ A. 0x0040000c
    - ◯ B. 0x00400000
    - ◯ C. 0x00400020
    - ◯ D. 0x00400018
    - ⊗ E. 0x00400004

Arrays

38. The next question refers to the following MIPS code. Assume all memory locations are initialized to 0x0000.

```
.text
la   $t0, space
li   $t1, 0
li   $t2, 0x39

loop:
sb   $t2, ($t0)
addi $t0, $t0, 1 # increment address
addi $t1, $t1, 1 # incrememt counter
subi $t2, $t2, 2
blt  $t1, 5, loop

la   $a0, space
li   $v0, 4
syscall

li   $v0, 10
syscall

.data
space: .space 10
```


What will be printed to the screen after the program completes executio

- ◯ A. 9753
- ◯ B. '%#!
- ⊗ C. 97531
- ◯ D. 0x39 0x37 0x35 0x33 0x31
- ◯ E. 97531/

Instruction Decoding

39. Assume an ISA with 8 general purpose registers and the following 16-bit instruction format:
| opcode | RD | RS | RT |
How many unique instructions can this ISA have?

- ◯ A. 16
- ◯ B. 9
- ◯ C. 7
- ⊗ D. 128
- ◯ E. 8

40. Decode the following MIPS32 instruction: `0x8D4C3210`

- ◯ A. `SW   $t2 0x0101 ($t3)`
- ◯ B. `AND  $t2 0x0123 $t4`
- ◯ C. `ANDI $t2 $t4 0x0123`
- ⊗ D. `LW   $t4 0x3210 ($t2)`
- ◯ E. `LW   $t2 0x3210 ($t4)`

41. Decode the following MIPS32 instruction: `0x01097820`. Select all that apply.
    - ◯ A. `ADD $t0 $t1 $t7`
    - ◯ B. `AND $8 $9 $15`
    - ◯ C. `ADD $8 $9 $15`
    - ⊗ D. `ADD $t7 $t0 $t1`
    - ⊗ E. `ADD $15 $8 $9`

Data Path

42. Assume $t0 = 5 and `LB $t0 4($t0)` is executed. The programmer has access to all memory locations. What is the value on wire 9?
    - ◯ A. 5
    - ◯ B. 9
    - ◯ C. Not enough information given
    - ⊗ D. 4
    - ◯ E. 8

43. The instruction `SUBI $t7 $t7 -1` is executed. What is the value on wire 4?
    - ◯ A. None of the other answers
    - ⊗ B. 0xFFFF
    - ◯ C. 0xF
    - ◯ D. 0xFFFFFFFF
    - ◯ E. Not enough information given

44. Assume the values on wires 5, 7, 10, 11, and 12 are 0x08, 0x12, 0x1A, 0x1B and 0x1B respectively. Which instruction could correspond to these values?
    - ◯ A. Not enough information given
    - ◯ B. `ADDI $12 $8 18`
    - ◯ C. `ADDI $s1 $s2 8`
    - ◯ D. `LW $t0 12($t1)`
    - ⊗ E. `LH $t8 8($t9)`

45. Assume $s0 = 0xAB, $s1 = 0xF4 and `SW $s1 8($s0)` is executed. What is the value on wire 8?
    - ⊗ A. 0xF4
    - ◯ B. 0x08
    - ◯ C. Not enough information given
    - ◯ D. 0x10
    - ◯ E. 0xAB