Final Exam

CMPE 012: Computer Systems and Assembly Language University of California, Santa Cruz

DO NOT BEGIN UNTIL YOU ARE TOLD TO DO SO.

This exam is closed book and closed notes. Only 4-function calculators are permitted. Answers must be marked on the Scantron form to be graded. All work must be written on the exam.

On the Scantron form, bubble in your name, student ID number, and test form (found in the footer of subsequent pages). In the center of the page write your CruzID, quarter, and exam type. On the back of the page, write the CruzIDs of students sitting to your left and right, and your row and seat number. See below.

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On this page, write your last name, first name, CruzID, row and seat numbers, and the CruzIDs of the people to your immediate left and right. Once you are permitted to begin, write your CruzID on all subsequent pages of the exam.

You must sit in your assigned seat. Keep your student or government issued ID on your desk. Brimmed hats must be removed or turned around backwards. Only unmarked water bottles are permitted. Backpacks must be placed at the front of the room or along the walls. Your cell phone must be on a setting where it will not make noise or vibrate.

There are 45 questions on this exam; you only need to answer 42 for full points. The additional three questions (of your choosing) will be counted as extra credit. All questions are multiple choice, and some questions have more than one correct answer. You must mark all correct answers to receive credit for a question. Some true/false questions might list False as answer A and True as answer B. Follow the answers on the exam, NOT the T F notation on the Scantron Form. You will have 120 minutes to complete this exam.

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Last Name		First Name	
CruzID of person to left		CruzID of person to right	

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CMPE 12 Final Exam - Version A

Winter 2019

Bits

1.	How man A. B.	y bits are needed to encode one ASCII character? 8 bits 10 bits
	C.D.E.	6 bits 7 bits 9 bits
2.	○ A.○ B.○ C.○ D.	ne size of a word in MIPS? Select all that apply. 8 bytes 32 bits 8 nybbles 4 bytes 32 Aytes signment Project Exam Help
Bi		rithmetic
3.		he following 1https://eduassistpro.github.io/
	 В. С.	000011011 A 0 dd WeChat edu_assist_pro 011111100001 011111100000
4.	○ A.○ B.○ C.○ D.	these 8-bit two's complement computations has carry out but no overflow? Select all that apply. $0 \times 1E + 0 \times 26 = 0 \times 44$ $0 \times FA + 0 \times ED = 0 \times E7$ $0 \times 0F + 0 \times 85 = 0 \times 94$ $0 \times 01 + 0 \times 7F = 0 \times 80$ $0 \times FF + 0 \times 01 = 0 \times 00$
5.	_	right shift and an arithmetic right shift perform the same operation True False

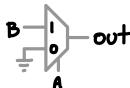
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Data Representation

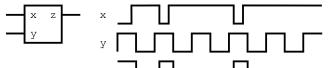
6.	Which IEEE 754 single precision floating point number is furthest from zero?
	○ A. 0xC70FFFFF
	○ B. 0x47700000
	○ C. 0x1F8FFFFF
	○ D. 0x380fffff
	○ E. 0xB8700000
7.	What is the following base 9 number in base 5? 106 ₉
	\bigcirc A. 123 ₅
	○ B. 322 ₅
	\bigcirc C. 742 ₅
	\bigcirc D. 305 ₅
	\bigcirc E. 222 ₅
8.	What is the range of values for an 8-bit two's complement integer?
	○ A. 0 to 255
	○ B128 to 127
	○ C127 to 128.
	O C127 to 128. O D124 to 127 gnment Project Exam Help O E127 to 127
	○ E127 to 127
9.	What is the following 8-bit t
	https://eduassistpro.github.io/
	$_{\odot}$ A. 10110110 Https://eduassistpro.gitriub.io/
	O B. 10101010
	O C. 01010110 A 1 1 XXX - C11 - 4
	D. 00101010 Add WeChat edu_assist_pro
	○ E. 11010110
10.	What is the following base 3 number in base 7? 2101 ₃
	\bigcirc A. 736 ₇
	○ B. 123 ₇
	○ C. 121 ₇
	O. 64 ₇
	\bigcirc E. 46_7
11.	6-bit two's complement, signed magnitude, and unsigned all represent the same number of integers, some just
	have more negative than positive.
	A. True
	○ B. False

Logic Design

12. This figure is logically equivalent to which circuit?



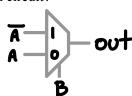
- A. XNOR gate
- O B. XOR gate
- C. AND gate
- O D. XOR gate
- O E. Positive D-Latch
- 13. What device does this timing diagram represent?



- O A. NASSignment Project Exam Help
- O B. SR latch active high
- C. Positive edge trigge
- O D. D latch https://eduassistpro.github.io/
- 14. This figure is logically equivalent to which circuit?

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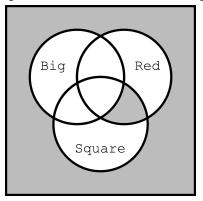
- A. AND gate
- O B. XOR gate
- O. Negative D-Flip Flop
- O D. XNOR gate
- O E. OR gate
- 15. This figure is logically equivalent to which circuit?



- A. XOR gate
- O B. XOR gate
- O. C. Negative D-Latch
- O. Positive D-latch
- E. XNOR gate

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16. Select the Boolean expression matching the filled areas of this Venn diagram.



- $\bigcirc \ A. \ (\texttt{Red} + \texttt{Square}) \cdot (\overline{\texttt{Big} \cdot \texttt{Red} \cdot \texttt{Square}}) \cdot (\texttt{Big} + \texttt{Red} + \texttt{Square})$
- \bigcirc B. Red·Square·(Big·Red·Square)·(Big+Red+Square)
- \bigcirc C. $(Red + Square) + (\overline{Big \cdot Red \cdot Square}) \cdot (Big + Red + Square)$
- O. Red·Square·(Big·Red·Square)
- \bigcirc E. Red Square \cdot (Big Red Square) + (Big + Red + Square)
- 17. How many outputs does a 4-16 decoder have?
 - O B. 64 Assignment Project Exam Help
 - O C. 1
 - O D. 16
 - E. 32

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Memory

18. How many bits are needed to represent a memory location address in a 41B m sist_pro addressable?

- B. 36
- C. 64
- O D. 34
- \bigcirc E. 2^{34}

19. How much memory is allocated with the following line of code?

.asciiz "ce_12"

- () A. 6 bytes
- O B. 5 words
- O. C. 4 bytes
- O D. 2 words
- O E. 5 bytes

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For the following two questions, assume a portion of data memory looks like this:

ADDRESS	CONTENTS
0x10011085	0xCD
0x10011084	0xAB
0x10011083	0x87
0x10011082	0x65
0x10011081	0x43
0x10011080	0x21

20. Assuming big endian memory storage, what is in \$t7 after the following instructions?

```
ADDI $t0, $zero, 0x10011080
LH $t7, 2($t0)
SW $t7, ($t0)
LW $t7, ($t0)
```

- A. 0x87654321
- B. 0x00008765
- C. 0x00006587
- O E. OXIFFF 8765 nment Project Exam Help
- 21. Assuming little endian memory storage, what is in \$t0 after the following instructions?

LII \$t3, 0x1001108 LW \$t0, (\$t3) https://eduassistpro.github.io/

- O B. 0x5678BADCAdd WeChat edu_assist_pro
- O D. Undefined. There will be an alignment error.
- E. 0xCDAB8765

ASCII

22. Decode the following ASCII string. Values are given in hex.

44 69 64 20 79 6f 75 20 65 76 65 72 20 68 65 61 72 20 74 68 65 20 74 72 61 67 65 64 79 20 6f 66 20 44 61 72 74 68 20 50 6c 61 67 75 65 69 73 20 74 68 65 20 57 69 73 65 3f

- A. Did you ever hear the tragedy of Darth Plagueis the Wise?
- O B. No! Try not. Do. Or do not. There is no try.
- C. Help me, Obi-Wan Kenobi. You're my only hope.
- O. I have a bad feeling about this.
- () E. I find your lack of faith disturbing.

23. Say that a user enters a single ASCII character in the range '0'-'9'. Assume that the user input is stored in \$v0. Which MIPS instruction would you use to convert their input into an integer in the range 0-9?

- A. subi \$t0, \$v0, 49
- O B. subi \$t0, \$v0, 48
- O. C. addi \$t0, \$v0, 48
- O. subi \$t0, \$v0, 30
- O E. subi \$t0, \$v0, 60

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MIPS

24. What is the value of \$t0 after the following instructions are executed (represented in hex)?

○ E. 0x001000FA

25. Which MIPS32 native/basic instruction(s) perform the same function as the following pseudo instruction?

ORI \$80 SASSIGNMENT Project Exam Help

```
0xAB
         $16 $13 0xAB // eduassistpro.github.io/
     SRL
     OR
\bigcirc B. ORI
             0xABCDEF00
\cap C. LI
                   WeChat edu_assist_pro
     OR
○ D. LUI
     OR
         $16 $13 $1
         $16 $16 0xABCD
     ORI
O E. LUI
         $1
             0xABCD
     ORI
         $1
             $1
                0xEF00
         $16 $13 $1
     OR
```

26. Which register(s) in MIPS must the callee preserve?

- O B. \$s0 \$s7
- C. \$sp
- O. \$v0 \$v1
- O E. \$a0 \$a3

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27. What is the value of \$t0 after the following instructions are executed?

```
$t0, 4
li
li
     $t1, 5
add $t0, $t1, $t0
addi $t0, $t0, -1
xor $t0, $t0, $t0
 \bigcirc A. 0
 ○ B. 6
 O C. 10
 O D. 8
```

() E. Not enough information given

28. What is the least significant byte stored in \$t0 after the following MIPS commands execute?

```
$t0, 0x9F
andi $t0, $t0, 0x0F
 ○ B. 10011111
 O C. 11110000
 O D. 00011111
```

O E. O Assignment Project Exam Help
29. What is printed to the screen after the following MIPs commands execute?

```
1
   .data
   prompt1: .aspittps://eduassistpro.github.io/
   prompt3: .asciiz " CE 12 FINAL"
5
             Add WeChat edu_assist_pro
   li $v0, 4
7
8
  la $a0, prompt1
  syscall
 LOVE
 \bigcirc B. I
 ○ C. I LOVE
 O D. I LOVE CE12 FINAL
 O E. nothing
```

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- 30. Processing an instruction requires the following steps
 - a. Execute operation/evaluate effective address
 - b. Write value to register file
 - c. Fetch instruction from memory
 - d. Access data from memory
 - e. Decode instruction

What is the correct ordering for these steps?

- () A. ecadb
- O B. ceadb
- O. caedb
- O D. deacb
- O E. aebdc
- 31. Which combination of MIPS instructions perform a pop operation of one word from the stack?
 - (\$sp) A. sw \$t0, (\$sp)
 - subi \$sp, \$sp, 4
 - O B. addi \$sp, \$sp, 4
 - lw \$t0, (\$sp)
 - O C. 1 A SSignment Project Exam Help
 - O. subi \$sp, \$sp, 4 sw \$t0, (\$sp)
 - © E. none of the a hyttps://eduassistpro.github.io/

The next four questions will refer t

```
1 .text Add WeChat edu_assist_pro
2 la $a0, strl Add WeChat edu_assist_pro
3 addiu $v0, $zero, 4
4 syscall
```

5

6 la \$a0, str2

7 syscall

8

9 lbu \$a0, str3

10 addiu \$v0, \$zero, 11

11 syscall

12

13 addiu \$v0, \$zero, 1

14 syscall

15

16 addiu \$v0, \$zero, 10

17 syscall

18

19 .data

- 20 str1: .ascii "hello"
- 21 str2: .asciiz "there"
- 22 str3: .byte 0x21 0x21 0x00

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22			1. 0.4				
37	A celime voli	changed	line 71	in the	original	nrogram	trom
JZ.	Assume you	changeu	1111C Z I	III tile	originar	program	110111

```
str2: .asciiz "there"
to
str2: .ascii "there"
What will be printed to the screen after the altered program completes execution?
 ○ A. hellothere!!33
 O B. hellotherethere!33
 ○ C. hellothere!33
 O. hellothere!!there!!!33
 E. hellothere!!there!!33
```

- 33. What will be printed to the screen after the original program completes execution?
 - A. hellotherethere!33
 - O B. hellothere!!33
 - C. hellotherethere!!33
 - O. hellothere!33
 - () E. hellotherethere!21

34. Assume you changed line 13 in the original program from

addiu \$v0A\$\$ighment Project Exam Help

addiu \$v0, \$zero, 35

What will be printed to the scr A. hellotherethe edtps://eduassistpro.github.io/

- O B. hellothere!00000
- hat edu_assist_pro
- () E. hellotherethere!33

35. Given the branch instruction in machine code

000101 00010 01000 1111111111111100

Assume the branch target address is 0x2004, what is the address of the branch instruction?

- A. None of the other answers
- B. 0x2004
- C. 0x2010
- O D. 0x2018
- O E. 0x2014

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CI uzib.	C desc.cad

The addresses of some of the instructions of the following program are listed. Please refer to the program for the next two questions

.text main: jal getString #sets v0 to address of string 0x00400000 move \$a0, \$v0 li \$v0, 4 0x0040000c syscall li \$v0, 10 svscall 0x00400018 getString: \$v0, string1 \$ra 0x00400020 jr

Assignment Project Exam Help string1:

- 36. What is the value of \$ponettos://eduassistpro.github.io/

 - B. 0x00400000
 - ${\circ\atop\circ}$ C. ${\circ\atop\circ}$ 0x0040001 ${\circ\atop\circ}$ Add WeChat edu_assist_pro

 - E. 0x00400004
- 37. What is the value of \$ra right after the jal is taken?
 - A. 0x0040000c
 - B. 0x00400000
 - C. 0x00400020
 - O D. 0x00400018
 - O E. 0x00400004

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Arrays

38. The next question refers to the following MIPS code. Assume all memory locations are initialized to 0x0000.

```
la
     $t0, space
li
     $t1, 0
    $t2, 0x39
li
loop:
     $t2, ($t0)
addi $t0, $t0, 1 # increment address
addi $t1, $t1, 1 # incrememt counter
subi $t2, $t2, 2
blt $t1, 5, loop
     $a0, space
la
     $v0, 4
li
syscall
```

Assignment Project Exam Help syscall

space: .space 10https://eduassistpro.github.io/

What will be printed to the screen after the program completes executio

- \bigcirc B. **′** 응#! O. C. 97531
 - Add WeChat edu_assist_pro
- O D. 0x39 0x37 0x35 0x33 0x31
- O E. 97531/

Instruction Decoding

39. Assume an ISA with 8 general purpose registers and the following 16-bit instruction format:

opcode | RD | RS | RT |

How many unique instructions can this ISA have?

- O A. 16
- O B. 9
- \bigcirc C. 7
- O D. 128
- E. 8

40. Decode the following MIPS32 instruction: 0x8D4C3210

- O B. AND \$t2 0x0123 \$t4
- C. ANDI \$t2 \$t4 0x0123
- \$t4 0x3210 (\$t2) \bigcirc D. LW
- E. LW \$t2 0x3210 (\$t4)

- 41. Decode the following MIPS32 instruction: 0x01097820. Select all that apply.
 - A. ADD \$t0 \$t1 \$t7
 - B. AND \$8 \$9 \$15
 - O C. ADD \$8 \$9 \$15
 - O D. ADD \$t7 \$t0 \$t1
 - O E. ADD \$15 \$8 \$9

Data Path

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- 42. Assume t0 = 5 and LB t0 4 (t0) is executed. The programmer has access to all memory locations. What is the value on wire 9?

 - B. 9
 - C. Not enough information given
 - O D. 4
 - O E. 8

43.	The instr	uction SUBI \$t7 \$t7 -1 is executed. What is the value on wire 4?
	○ A.	None of the other answers
	○ B.	0xFFFF
	○ C.	0xF
	○ D.	0xFFFFFFF
	○ E.	Not enough information given
44.		he values on wires 5, 7, 10, 11, and 12 are 0x08, 0x12, 0x1A, 0x1B and 0x1B respectively. Which n could correspond to these values?
	○ A.	Not enough information given
	_	ADDI \$12 \$8 18
	○ C.	ADDI \$s1 \$s2 8
	O D.	LW \$t0 12(\$t1)
	○ E.	LH \$t8 8(\$t9)
45.	○ A.	880 = 0xAB, $$s1 = 0xF4$ and SW $$s1$ 8 (\$s0) is executed. What is the value on wire 8? $0xF4$ $0x08$
	О С.	Not enough information given
		0x10
	○ E.	⁰ Assignment Project Exam Help
		https://eduassistpro.github.io/

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Set	REG NAME	REG #	MNEMONIC	MEANING	TYPE	OPCODE	FUNCT	MNEMONIC	MEANING	TYPE	OPCODE	FUNCT
Syst	\$zero	0	sll	Logical Shift Left	R	0x00	0x00	add	Add	R	0x00	0x20
System	\$at	1	srl	Logical Shift Right (0-extended)	R	0x00	0x02	addi	Add Immediate	I	0x08	NA
Sab	\$v0	2	sra	Arithmetic Shift Right (sign-extended)	R	0x00	0x03	addiu	Add Unsigned Immediate	I	0x09	NA
Sal	\$v1	3	jr	Jump to Address in Register	R	0x00	0x08	addu	Add Unsigned	R	0x00	0x21
\$a2	\$a0	4	mfhi	Move from HI Register	R	0x00	0x10	and	Bitwise AND	R	0x00	0x24
Sa3	\$a1	5	mflo	Move from LO Register	R	0x00	0x12	andi	Bitwise AND Immediate	I	0x0C	NA
St0	\$a2	6	mult	Multiply	R	0x00	0x18	beq	Branch if Equal	I	0x04	NA
St1	\$a3	7	multu	Unsigned Multiply	R	0x00	0x19	blez	Branch if Less Than or Equal to Zero	I	0x06	NA
\$t2	\$t0	8	div	Divide	R	0x00	0x1A	bne	Branch if Not Equal	I	0x05	NA
\$13	\$t1	9	divu	Unsigned Divide	R	0x00	0x1B	div	Divide	R	0x00	0x1A
\$t4 12 sub Subtract R 6x80 6x22 jal Jump and Link J 6x83 NA 5t5 13 subu Unsigned Subtract R 6x80 6x22 jal Jump and Link J 6x24 NA 5t5 13 or Bitwise AND R 6x80 6x24 lb Load Halfword Unsigned I 6x24 NA 5x51 17 nor Bitwise NOR (Bxclustuse-OR) R 6x80 6x26 lb Load Halfword Unsigned I 6x25 NA 5x51 17 nor Bitwise NOR (NOT-OR) R 6x80 6x26 lb Lb Load Halfword Unsigned I 6x25 NA 6x52 lb Store Byte I 6x25 NA 5x51 17 nor Bitwise NOR (NOT-OR) R 6x80 6x26 lb Lb Load Halfword Unsigned I 6x25 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 5x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 5x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 5x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) R 6x30 NA 6x51 17 nor Bitwise NOR (NOT-OR) NA 6x51 17 nor Bitwi	\$t2	10	add	Add	R	0x00	0x20	divu	Unsigned Divide	R	0x00	0x1B
St5	\$t3	11	addu	Add Unsigned	R	0x00	0x21	j	Jump to Address	J	0x02	NA
\$1 and Bitwise AND or Bitwise AND signature of	\$t4	12	sub	Subtract	R	0x00	0x22	jal	Jump and Link	J	0x03	NA
\$1	\$t5	13	subu	Unsigned Subtract	R	0x00	0x23	jr	Jump to Address in Register	R	0x00	0x08
See	\$t6	14	and	Bitwise AND	R	0x00	0x24	1 <u>b</u>	Load Byte 🕌 🕌	I	0x20	NA
See	\$t7	15	or	Bitwise A SS10nment		0:00	PAPE 1	ltu√X	Patry e urs gred 1)	I	0x24	NA
\$52 18 Slt Set to 1 if less T I 0x0F NA \$53 19 Sltu Set to 1 if less T I 0x0F NA \$54 20 J Jump to Address J 0x08 NA \$55 21 jal Jump and Link J 0x08 NA \$56 22 beq Branch if Equal I 0x0F NA \$57 23 bne Branch if Not Equal I 0x0F NA \$58 24 blez Branch if Less Than John Gulado I 0x0F NA \$58 25 addiu Add Unsigned Immediate I 0x08 NA \$58 26 addiu Add Unsigned Immediate I 0x08 NA \$58 27 Or Bitwise OR R 0x00 0x \$58 28 Sltiu Set to 1 if less Than Immediate I 0x0B NA \$59 29 Addio Bitwise AND Immediate I 0x0F NA \$50 29 Addio Bitwise OR Immediate I 0x0F NA \$50 29 Addio Bitwise OR Immediate I 0x0B NA \$50 20 Sitiu Set to 1 if less Than Unsigned Immediate I 0x0F NA \$50 20 Sitiu Set to 1 if less Than Unsigned Immediate I 0x0F NA \$50 20 Sitiu Set to 1 if less Than Unsigned Immediate I 0x0F NA \$50 20 Sitiu Set to 1 if less Than Unsigned Immediate I 0x0F NA \$50 21 Sitiu Set to 1 if less Than Unsigned Immediate I 0x0F NA \$50 22 Sitiu Set to 1 if less Than Unsigned Immediate I 0x0F NA \$50 25 Sitiu Set to 1 if less Than I 0x2F NA \$50 26 Sitiu Set to 1 if less Than I 0x2F NA \$50 27 Sitiu Set to 1 if less Than I 0x2F NA \$50 28 Sitiu Set to 1 if less Than I 0x2F NA \$50 29 Sitiu Set to 1 if less Than I 0x2F NA \$50 20 Sitiu Set to 1 if less Than I 0x2F NA \$50 20 Sitiu Set to 1 if less Than I 0x2F NA \$50 20 Sitiu Set to 1 if less Than I 0x0F NA \$50 21 Sitiu Set to 1 if less Than I 0x0F NA \$50 21 Sitiu Set to 1 if less Than I 0x0F NA \$50 21 Sitiu Set to 1 if less Than I 0x0F NA \$50 21 Sitiu Set to 1 if less Than I 0x0F NA \$50 22 Sitiu Set to 1 if less Than I 0x0F NA \$50 25 Sitiu Set to 1 if less Than I 0x0F NA \$50 26 Sitiu Set to 1 if less Than I 0x0F NA \$50 27 Sitiu Set to 1 if less Than I 0x0F NA	\$s0	16	xor		R	0x00	0x26	1h	Load Halfword	I	0x21	NA
\$\$3 19 \$1	\$s1	17	nor	Bitwise NOR (NOT-OR)	R	0x00	0x27	1hu	Load Halfword Unsigned	I	0x25	NA
\$55 21 jal Jump and Link J 0x03 NA mfhi Move from HI Register R 0x00 0x \$56 22 beq Branch if Equal I I 0x04 NA egister R 0x00 0x \$57 23 blez Branch if Less Than John Latro 2xxx C 1xxx L 2x \$58 24 blez Branch if Less Than John Latro 2xxx C 1xxx L 2x \$58 25 addi Add Immediate I 0x08 NA Or Bitwise OR R 0x00 0x \$58 26 addiu Add Unsigned Immediate I 0x09 NA Or Bitwise OR Immediate I 0x00 NA S \$58 29 28 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$59 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 5 sltiu Set to 1 if Less Than Unsigned Immediate I 0x08 NA S \$50 29 6 sltwise OR Immediate I 0x08 NA S \$50 29 8 sltiu Set to 1 if Less Than R \$50 0x00 0x1 \$50 0x00 0x1	\$s2	18	slt	Set to 1 if Less T				r Immedi	ate	I	0x0F	NA
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\$55 21 jal Jump and Link J 0x03 NA mfhi Move from HI Register R 0x00 0x \$56 22 beq Branch if Equal I Ox04 NA egister R 0x00 0x \$57 23 blez Branch if Less Than John Later Developed Park NA blez Branch if Less Than John Later Developed Park NA sub Store Byte Store Byte I 0x08 NA ori Bitwise OR Immediate I 0x08 NA ori Bitwise OR Immediate I 0x08 NA short Developed Park NA Short Develope	\$s4	20	j	Jump to Address	;u	ua	551	Dap ode		R	0x10	NA
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\$gp 28	\$k0	26	addiu	Add Unsigned Immediate	I	0x09	NA	or	Bitwise OR	R	0x00	0x25
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ori Bitwise OR Immediate I 0x0D NA sll Logical Shift Left R 0x00 0x1 xori Bitwise XOR (Exclusive-OR) Immediate I 0x0E NA slt Set to 1 if Less Than R 0x00 0x1 lui Load Upper Immediate I 0x0F NA slti Set to 1 if Less Than Immediate I 0x0B NA mfc0 Move from Coprocessor 0 R 0x10 NA sltiu Set to 1 if Less Than Unsigned Immediate I 0x0B NA lb Load Byte I 0x20 NA sltu Set to 1 if Less Than Unsigned R 0x00 0x1 lh Load Halfword I 0x21 NA sra Arithmetic Shift Right (sign-extended) R 0x00 0x1 lb Load Byte Unsigned I 0x23 NA srl Logical Shift Right (0-extended) R 0x00 0x1 lb Load Byte Unsigned I 0x24 NA sub Subtract R 0x00 0x1 lh Load Halfword Unsigned I 0x25 NA sub Unsigned Subtract R 0x00 0x1 sb Store Byte I 0x28 NA sw Store Word I 0x2B NA	\$gp	28	sltiu	Set to 1 if Less Than Unsigned Immediate	eΙ	0x0B	NA	sb	Store Byte	I	0x28	NA
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lwLoad WordI0x23NAsrlLogical Shift Right (0-extended)R0x000x1lbuLoad Byte UnsignedI0x24NAsubSubtractR0x000x1lhuLoad Halfword UnsignedI0x25NAsubuUnsigned SubtractR0x000x1sbStore ByteI0x28NAswStore WordI0x28NA			1b	Load Byte	I	0x20	NA	sltu	Set to 1 if Less Than Unsigned	R	0x00	0x2B
lbuLoad Byte UnsignedI0x24NAsubSubtractR0x000xlhuLoad Halfword UnsignedI0x25NAsubuUnsigned SubtractR0x000xsbStore ByteI0x28NAswStore WordI0x28NA			1h	Load Halfword	I	0x21	NA	sra	Arithmetic Shift Right (sign-extended)	R	0x00	0x03
1huLoad Halfword UnsignedI0x25NAsubuUnsigned SubtractR0x000xsbStore ByteI0x28NAswStore WordI0x28NA			lw	Load Word	I	0x23	NA	srl	Logical Shift Right (0-extended)	R	0x00	0x02
sb Store Byte I 0x28 NA sw Store Word I 0x2B NA			1bu	Load Byte Unsigned	I	0x24	NA	sub	Subtract	R	0x00	0x22
			lhu	Load Halfword Unsigned	I	0x25	NA	subu	Unsigned Subtract	R	0x00	0x23
sh Store Halfword I 0x29 NA xor Bitwise XOR (Exclusive-OR) R 0x00 0x			sb	Store Byte	I	0x28	NA	SW	Store Word	I	0x2B	NA
			sh	Store Halfword	I	0x29	NA	xor	Bitwise XOR (Exclusive-OR)	R	0x00	0x26
sw Store Word I 0x2B NA xori Bitwise XOR (Exclusive-OR) Immediate I 0x0E NA			SW	Store Word	I	0x2B	NA	xori	Bitwise XOR (Exclusive-OR) Immediate	I	0x0E	NA

```
R Type: instr rd rs rt (arithmetic, logical)
      instr rd rt shamt (shifts)
31 26 25 21 20
                                16 15 11 10
                                                       6 5
                        <- 5 bits -> <- 5 bits -> <- 5 bits ->
              <- 5 bits ->
                                                         <- 6 bits ->
                                                         funct
opcode
             rs
                                              shamt
I Type: instr rt rs immediate
                         (arithmetic, logical)
      branch rs rt immediate
                         (branches)
      instr rt immediate(rs)
                        (loads, stores)
           Assignment Project Exam Help
opcode
                                   immediate
                 https://eduassistpro.github.io/
J Type: j immediate (ju
                 Add WeChat edu_assist_pro
31 26 25
  <- 6 bits ->
```

opcode

immediate

	ASCI	I COD	ÞΕ					ASCI	I COL	E					ASCI	I COD	E			-	ASCI	I COL	DE		
BIN		ОСТ	DEC	HEX	CHARACTER	BI	N		ОСТ	DEC	HEX	CHARACTER		BIN		ОСТ	DEC	HEX	CHARACTER	BIN		ОСТ	DEC	HEX	CHARACTER
010	0000	40	32	20	space	0:	11	1000	70	56	38	8		101	0000	120	80	50	Р	110	1000	150	104	68	h
010	0001	41	33	21	!	0:	11	1001	71	57	39	9		101	0001	121	81	51	Q	110	1001	151	105	69	i
010	0010	42	34	22	"	0:	11	1010	72	58	3A	:		101	0010	122	82	52	R	110	1010	152	106	6A	j
010	0011	43	35	23	#	0:	11	1011	73	59	3B	;		101	0011	123	83	53	S	110	1011	153	107	6B	k
010	0100	44	36	24	\$	0:	11	1100	74	60	3C	<		101	0100	124	84	54	T	110	1100	154	108	6C	1
010	0101	45	37	25	%	0:	11	1101	75	61	3D	=		101	0101	125	85	55	U	110	1101	155	109	6D	m
010	0110	46	38	26	&	0:	11	1110	76	62	3E	>		101	0110	126	86	56	V	110	1110	156	110	6E	n
010	0111	47	39	27	'	0:	11	1111	77	63	3F	?		101	0111	127	87	57	W	110	1111	157	111	6F	0
010	1000	50	40	28	(10	00	0000	100	64	40	@		101	1000	130	88	58	Х	111	0000	160	112	70	р
010	1001	51	41	29)	10	00	0001	101	65	41	Α		101	1001	131	89	59	Υ	111	0001	161	113	71	q
010	1010	52	42	2A	*	∆ 10	00	9010	102	66	Δ^{42}	t Pro	ว่า	191	1010	132	39	5A	HAln	111	0010	162	114	72	r
010	1011	53	43	2B	+	4	99	001E	103	67	45	ll £ 10	J	101	1011	133	91	5B	TIATA	111	0011	163	115	73	S
010	1100	54	44	2C	,	10	00	0100	104	68	44	D		101	1100	134	92	5C	\	111	0100	164	116	74	t
010	1101	55	45	2D	-	10	00		44.		_ /	/							1		0101	165	117	75	u
010	1110	56	46	2E		10	00	01	ITT	SC	5://	'eau	a	SS	IST	pr	Ό.	g	ithub	.10	0110	166	118	76	V
010	1111	57	47	2F	/	10	00		•							•			-		0111	167	119	77	W
011	0000	60	48	30	0	10	00	1000	110	72	48	H (11		110						111	1000	170	120	78	Х
011	0001	61	49	31	1	10	00	1001	10	<u>C</u>	49	/e€r	12	110	edi	u	as	SS	ist 1)ro	1001	171	121	79	У
011	0010	62	50	32	2	10	00	1010	112	74	4A	J		110		_	•		b	111	1010	172	122	7A	Z
011	0011	63	51	33	3	10	00	1011	113	75	4B	K		110	0011	143	99	63	С	111	1011	173	123	7B	{
011	0100	64	52	34	4	10	00	1100	114	76	4C	L		110	0100	144	100	64	d	111	1100	174	124	7C	
011	0101	65	53	35	5	10	00	1101	115	77	4D	М		110	0101	145	101	65	e	111	1101	175	125	7D	}
011	0110	66	54	36	6	10	00	1110	116	78	4E	N		110	0110	146	102	66	f	111	1110	178	126	7E	~
011	0111	67	55	37	7	10	00	1111	117	79	4F	0		110	0111	147	103	67	g	111	1111	177	127	7F	DEL

SERVICE	CODE IN \$v0	ARGUMENTS	RESULT
print integer	1	\$a0 = integer to print	
print float	2	\$f12 = float to print	
print double	3	\$f12 = double to print	
print string	4	\$a0 = address of null-terminated string to print	
read integer	5		\$v0 contains integer read
read float	6		\$f0 contains float read
read double	7		\$f0 contains double read
read string	8	<pre>\$a0 = address of input buffer \$a1 = maximum number of characters to read</pre>	See note below table
sbrk (allocate	0	dag number of butter to allegate	\$v0 contains address of allocated
heap memory) exit (terminate execution)	9	\$a0 = number of bytes to allocate	memory
print character	11	\$a0 = character to print	See note below table
read character	12	pao - character to print	\$v0 contains character read
open file	A ₁₃ SS	\$a0 = address of null-terminated string containing filename Project E	Volcentains character read Volcentains character read Volcentains character read if error). See note below table
read from	1.4	of-file,	of characters read negative if error).
file	14	https://eduassistive	offorgithub.io/
write to file	15	\$a2 = number of characters to writ	,
close file exit2	16	Add WeChat edu	_assist_pro
(terminate with value)	17	\$a0 = termination result	See note below table
	ough 17 ar	e compatible with the SPIM simulator, other s below the table. Services 30 and higher ar	than Open File (13) as described in the
time (system time)	30		\$a0 = low order 32 bits of system time \$a1 = high order 32 bits of system time. See note below table
MIDI out	31	<pre>\$a0 = pitch (0-127) \$a1 = duration in milliseconds \$a2 = instrument (0-127) \$a3 = volume (0-127)</pre>	Generate tone and return immediately. See note below table
		\$a0 = the length of time to sleep in	Causes the MARS Java thread to sleep for (at least) the specified number of milliseconds. This timing will not be precise, as the Java implementation
sleep	32	milliseconds. \$a0 = pitch (0-127) \$a1 = duration in milliseconds	will add some overhead.
MIDI out synchronous	33	\$a2 = instrument (0-127) \$a3 = volume (0-127)	Generate tone and return upon tone completion. See note below table
print integer in hexadecimal	34	\$a0 = integer to print	Displayed value is 8 hexadecimal digits, left-padding with zeroes if necessary.
print integer in binary	35	\$a0 = integer to print	Displayed value is 32 bits, left- padding with zeroes if necessary.
print integer as unsigned	36	\$a0 = integer to print	Displayed as unsigned decimal value.

MIPS Address Space (Not to Scale)

0xffff	ffff	
0xffff	0000	MMIO
0x9000	0000	Kernel Data
0x7fff	fe00	Stack
A	SS	ignment Project Exam Help
		Neap J
0x1004	0000	https://eduassistpro.github.io/
0x1001	0000	Static Data
		Add.:WeChat edu_assist_pro
0x0040	0000	
0x0000	0000	Reserved