

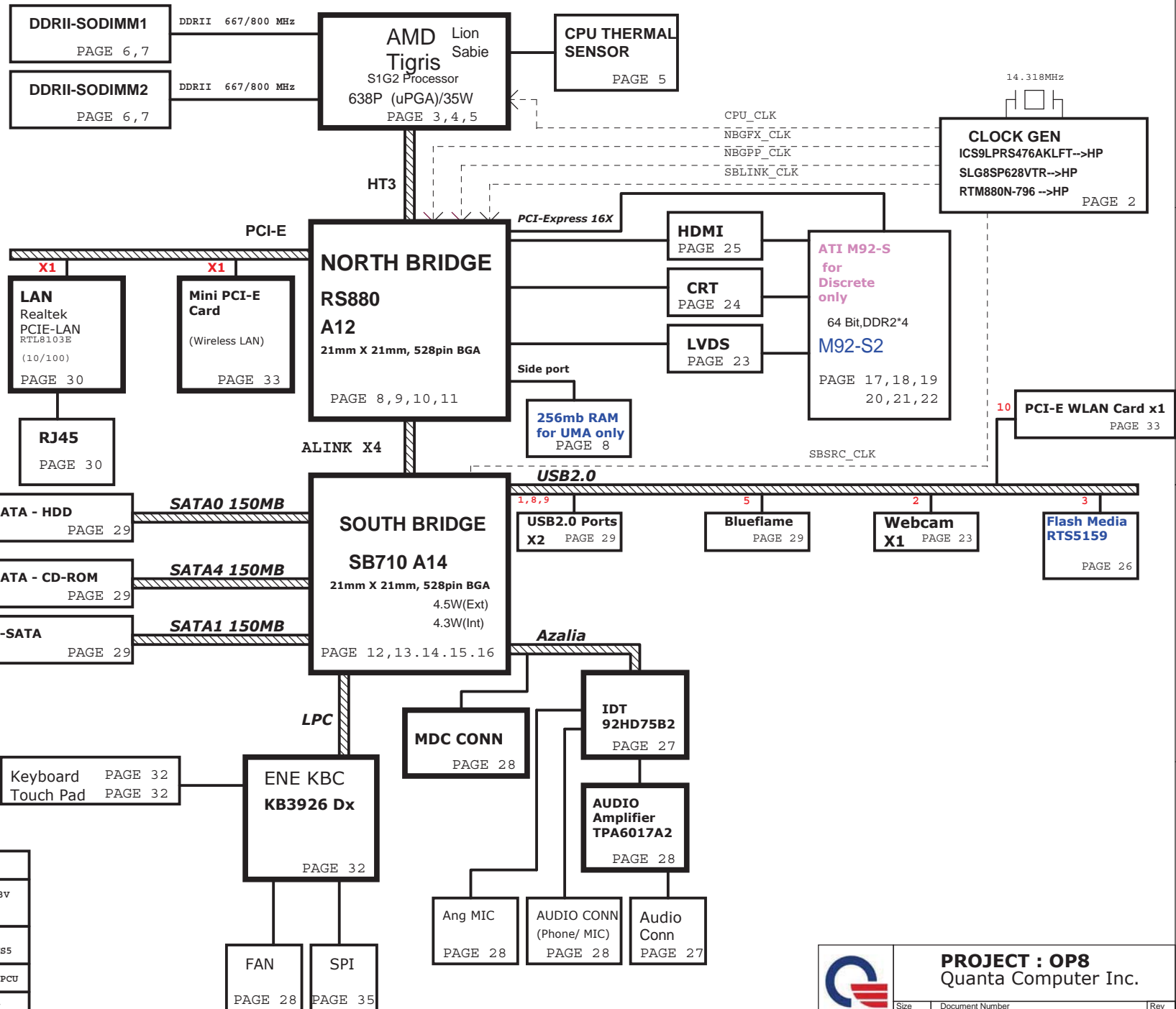
OP8 SYSTEM DIAGRAM



01

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : IN1
LAYER 3 : IN2
LAYER 4 : VCC
LAYER 5 : IN3
LAYER 6 : BOT

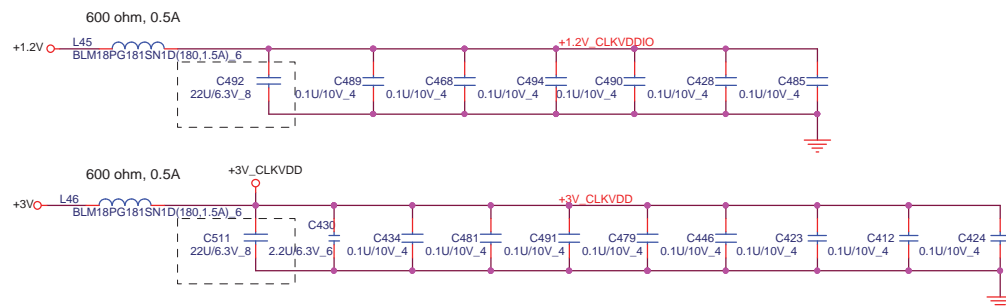


<http://hobi-elektronika.net>



PROJECT : OP8
Quanta Computer Inc.

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Date: Friday, March 20, 2009	Block Diagram	
Sheet 1	of 42	



Place very close to C/G

+3V_CLKVDD

L35

BLM18PG181SN1D(180, 1.5A), 6

+3V_CLK VDDA

C396

2.2uF/6.3V_6

C411

0.1uF/10V_4

U11

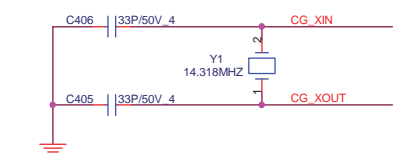
4 16 26 35 40 48 55 56 63

VDDDOT VDDSRC VDDATIG VDDSB VDD_SATA VDDCPU VDDHTT VDDREF VDD48

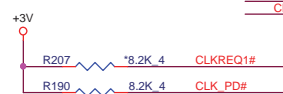
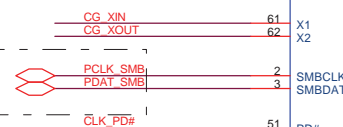
11 17 25 34 47

VDDSRC_IO VDDSRC_IO VDDATIG_IO VDDSB_IO VDDCPU_IO

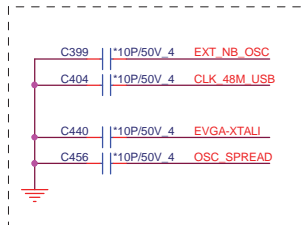
+1.2V_CLKVDDIO



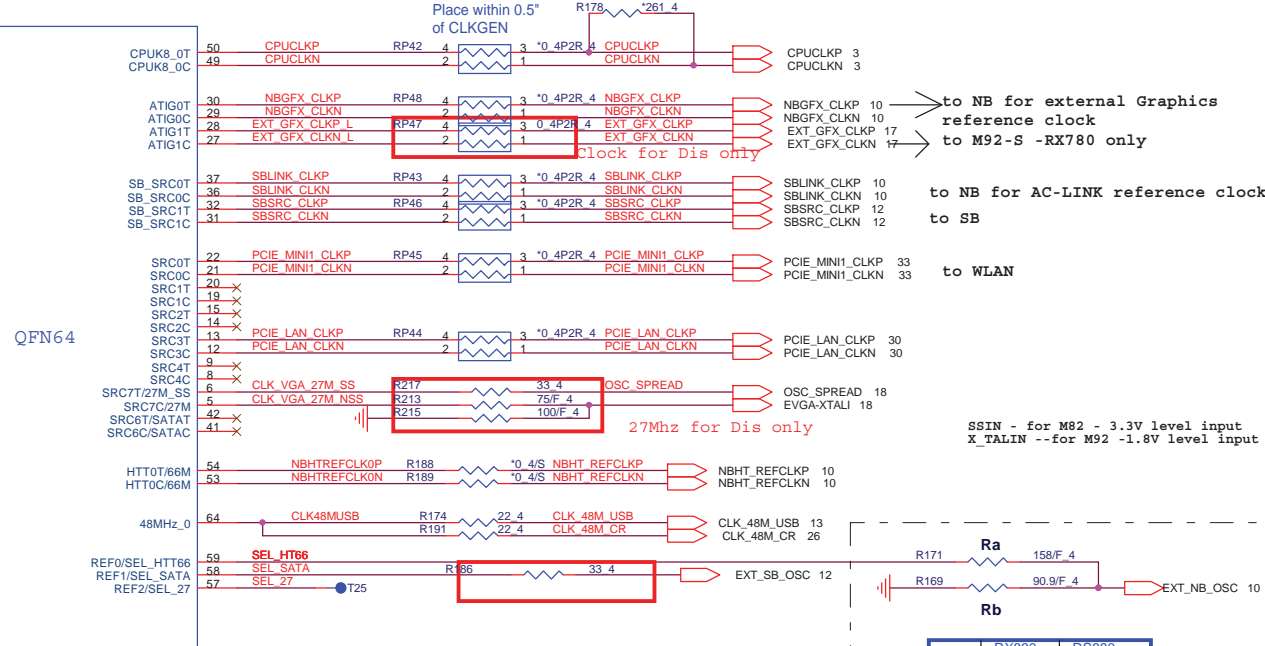
can remove MOSFET level shift
SB/clock gen / DDR2 is 3.3V/5V
power level



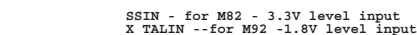
For EMI



```
if use clock
request pin , need
to pull Hi for
default setting
```

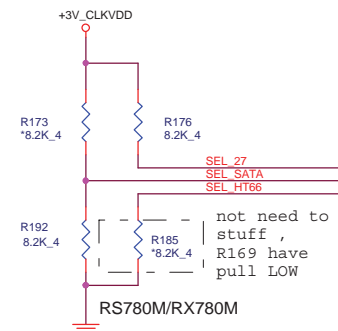


SI change 1.2V to 3.3V from AMD request



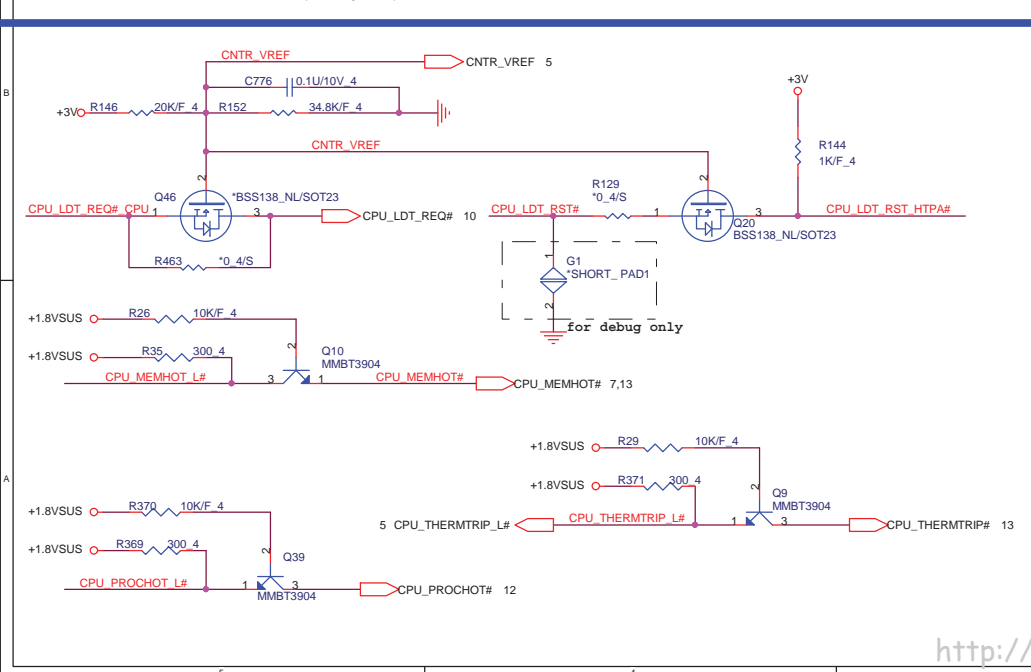
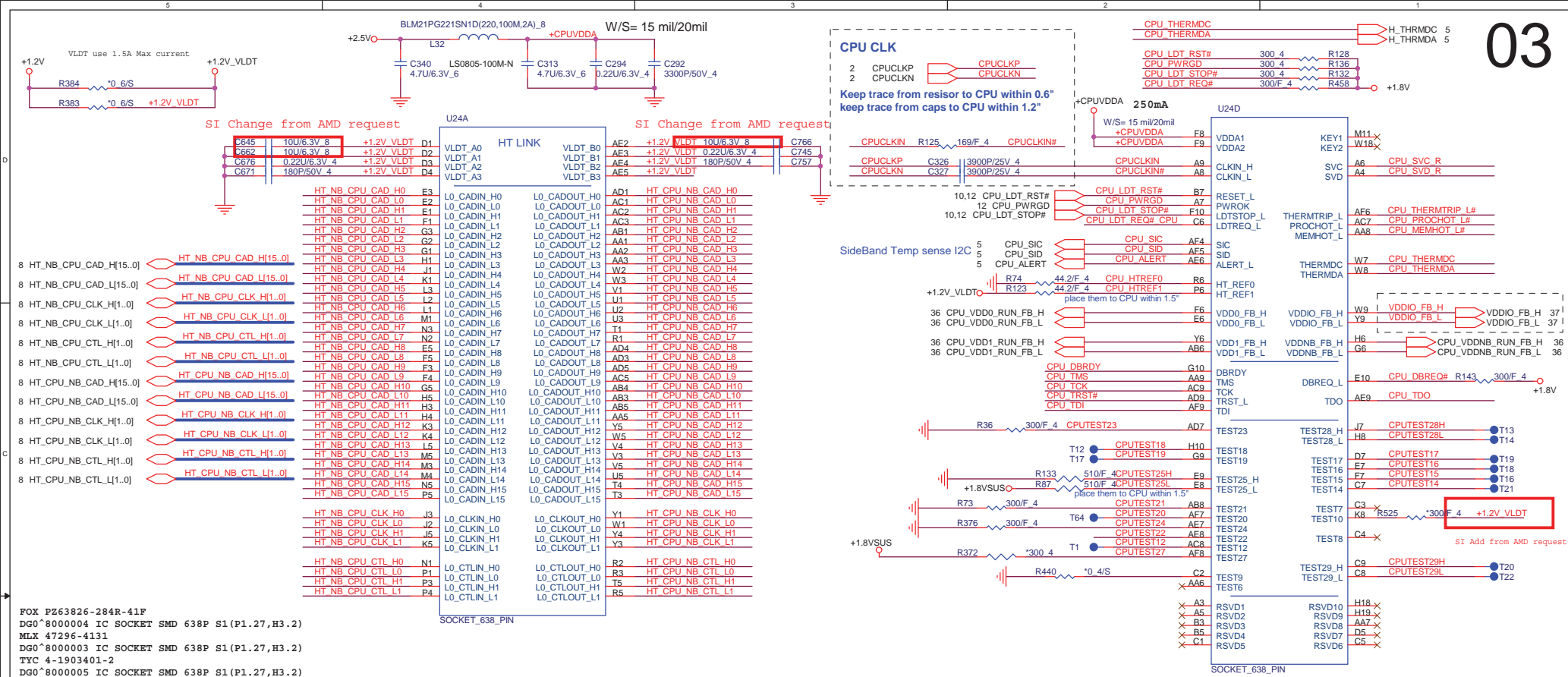
	RX880	RS880
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +1%(0402) -->CS08252FB11



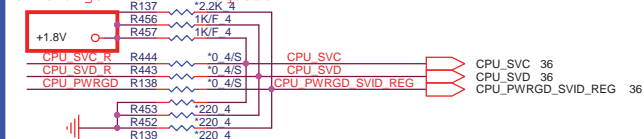
- Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

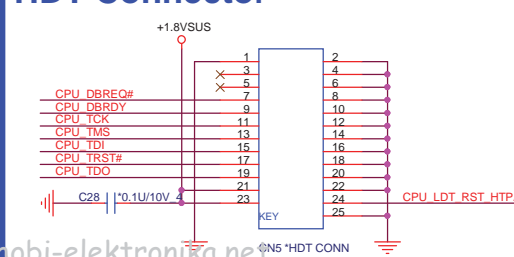


Serial VID

SI Change from AMD request

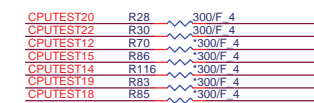


HDT Connector



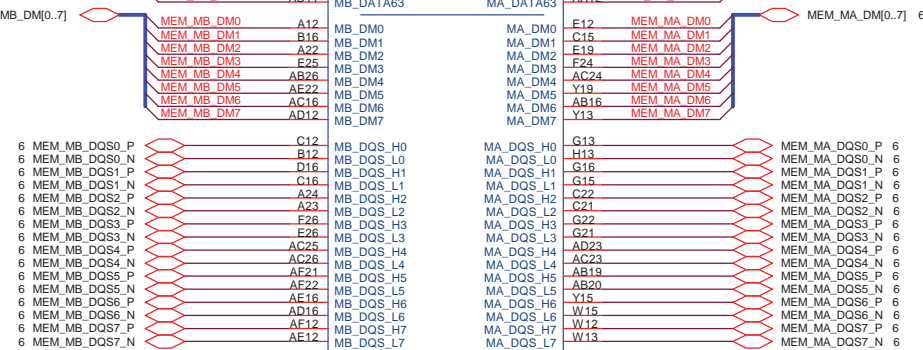
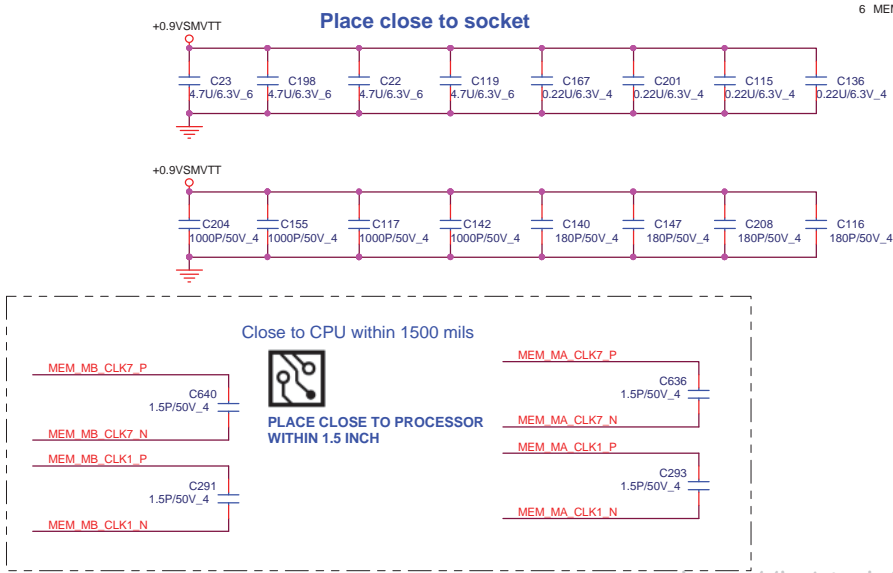
VFIX MODE VID Override Circuit

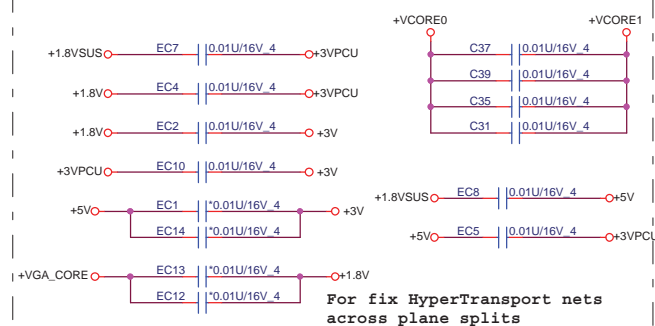
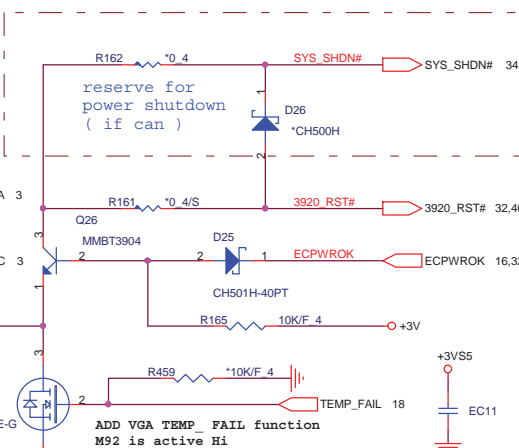
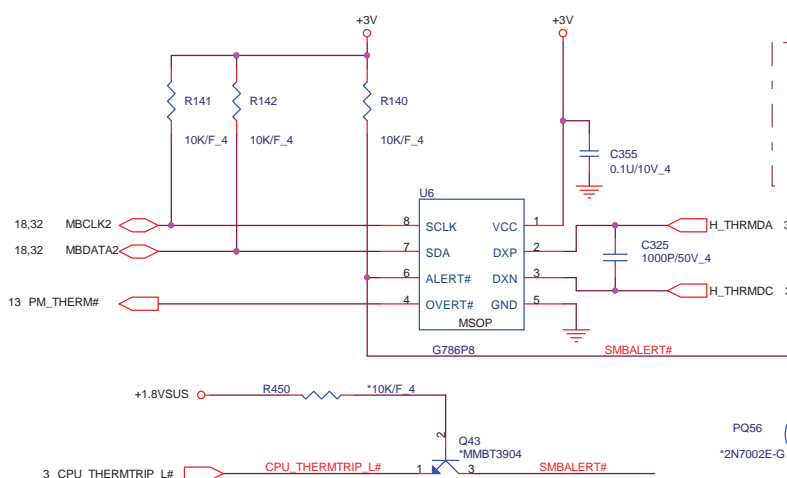
SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



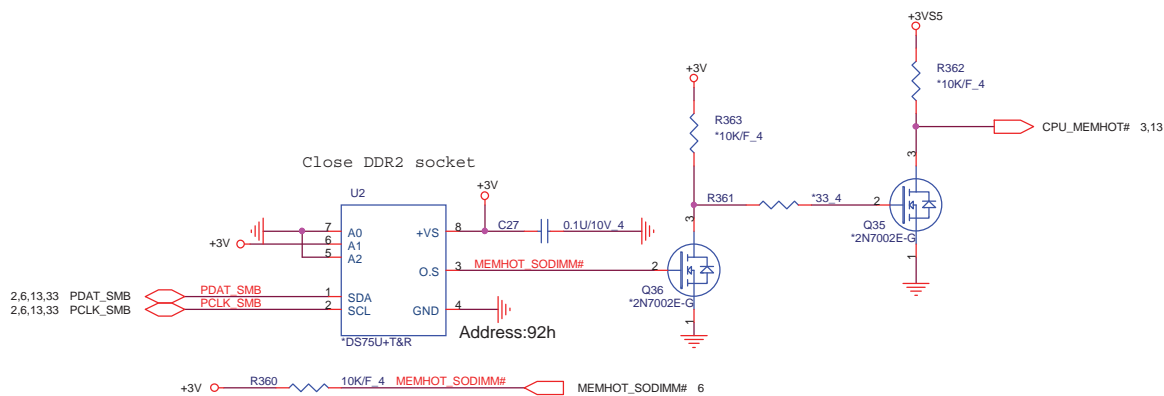
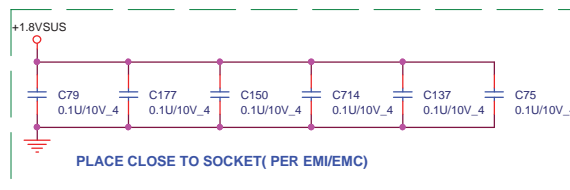
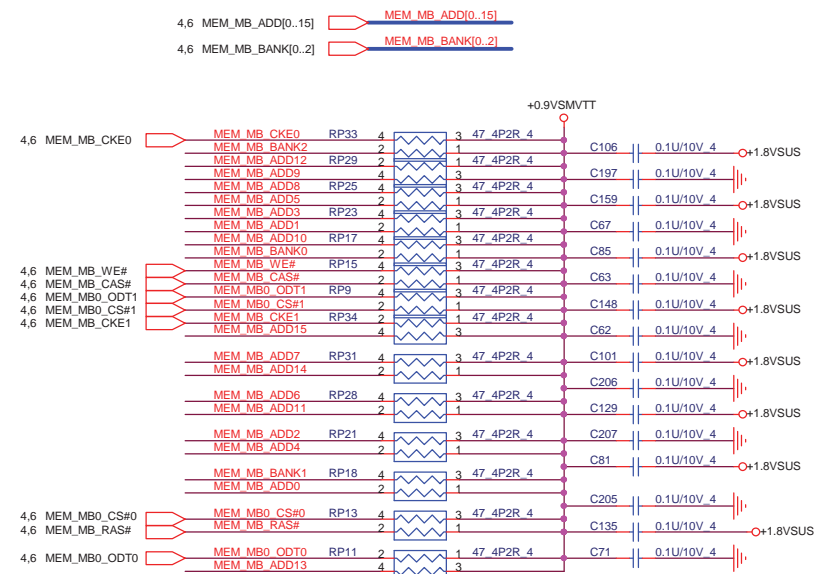
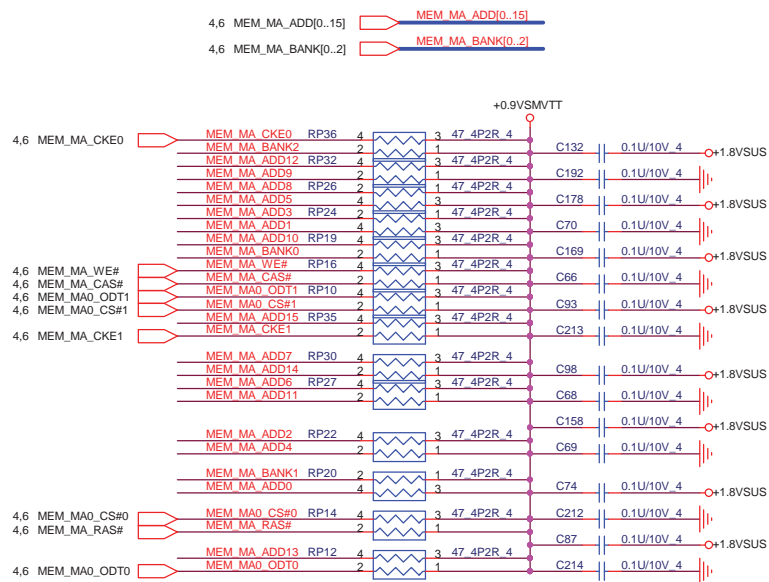
PROJECT : OP8
Quanta Computer Inc.

Size Custom	Document Number S1G2 HT,CTL I/F 1/3	Rev 1A
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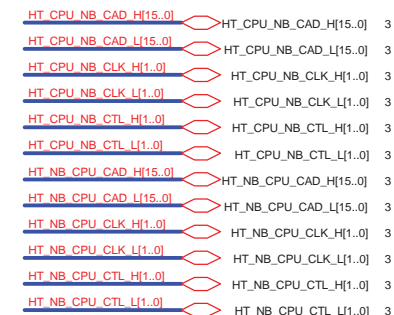






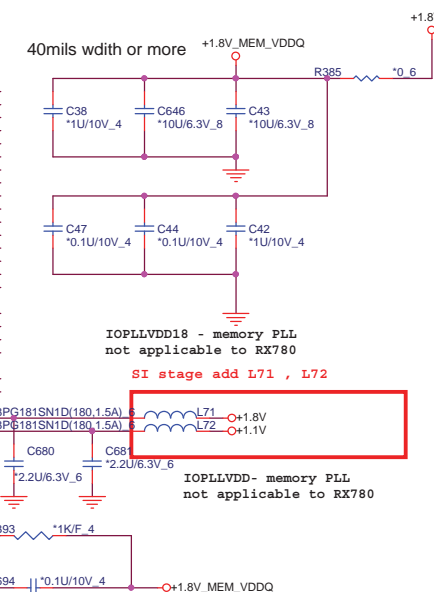
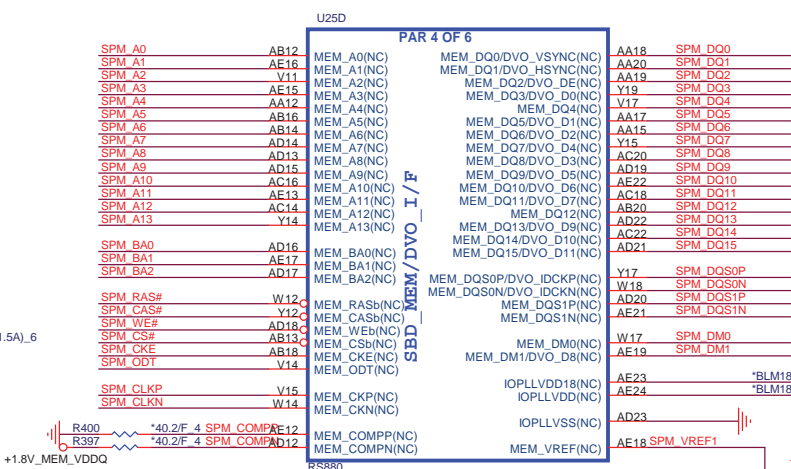
PROJECT : OP8
Quanta Computer Inc.

Size Custom Document Number
DDR2 SODIMMS TERMINATIONS Rev 1A
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signals	RS880	RX880
HT_TXCALP	R430 301 ohm 1%	R430 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R434 301 ohm 1%	R434 1.21k ohm 1%
HT_RXCALN		

RES CHIP 301 1/16W +-1%(0402)
P/N : CS13012FB14



IOPLLVDD18 - memory PLL
not applicable to RX780

SI stage add L71 , L72

IOPLLVDV- memory PLL
not applicable to RX780



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Quanta Computer Inc.

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PART 2 OF 6

PCIE I/F GFX

PEG_RX15	D4	GFX_RX0P	GFX_TX0P	A5	C_PEG_TX15	C332	0.1U/10V_4	PEG_TX15
PEG_RX#15	C4	GFX_RX0N	GFX_TX0N	B5	C_PEG_TX#15	C333	0.1U/10V_4	PEG_TX#15
PEG_RX14	A3	GFX_RX1P	GFX_TX1P	A4	C_PEG_TX14	C339	0.1U/10V_4	PEG_TX14
PEG_RX#14	B3	GFX_RX1N	GFX_TX1N	B4	C_PEG_TX#14	C338	0.1U/10V_4	PEG_TX#14
PEG_RX13	C2	GFX_RX2P	GFX_TX2P	C3	C_PEG_TX13	C336	0.1U/10V_4	PEG_TX13
PEG_RX#13	C1	GFX_RX2N	GFX_TX2N	B2	C_PEG_TX#13	C337	0.1U/10V_4	PEG_TX#13
PEG_RX12	E5	GFX_RX3P	GFX_TX3P	D1	C_PEG_TX12	C335	0.1U/10V_4	PEG_TX12
PEG_RX#12	F5	GFX_RX3N	GFX_TX3N	D2	C_PEG_TX#12	C334	0.1U/10V_4	PEG_TX#12
PEG_RX11	G5	GFX_RX4P	GFX_TX4P	E2	C_PEG_TX11	C735	0.1U/10V_4	PEG_TX11
PEG_RX#11	G6	GFX_RX4N	GFX_TX4N	E1	C_PEG_TX#11	C734	0.1U/10V_4	PEG_TX#11
PEG_RX10	H5	GFX_RX5P	GFX_TX5P	F4	C_PEG_TX10	C729	0.1U/10V_4	PEG_TX10
PEG_RX#10	H6	GFX_RX5N	GFX_TX5N	F3	C_PEG_TX#10	C730	0.1U/10V_4	PEG_TX#10
PEG_RX9	J6	GFX_RX6P	GFX_TX6P	E1	C_PEG_TX9	C727	0.1U/10V_4	PEG_TX9
PEG_RX#9	J5	GFX_RX6N	GFX_TX6N	H4	C_PEG_TX#9	C724	0.1U/10V_4	PEG_TX#9
PEG_RX8	J7	GFX_RX7P	GFX_TX7P	H3	C_PEG_TX8	C726	0.1U/10V_4	PEG_TX8
PEG_RX#8	J8	GFX_RX7N	GFX_TX7N	H1	C_PEG_TX#8	C725	0.1U/10V_4	PEG_TX#8
PEG_RX7	L5	GFX_RX8P	GFX_TX8P	H2	C_PEG_TX7	C723	0.1U/10V_4	PEG_TX7
PEG_RX#7	L6	GFX_RX8N	GFX_TX8N	H2	C_PEG_TX#7	C718	0.1U/10V_4	PEG_TX#7
PEG_RX6	M8	GFX_RX9P	GFX_TX9P	J2	C_PEG_TX6	C716	0.1U/10V_4	PEG_TX6
PEG_RX#6	L8	GFX_RX9N	GFX_TX9N	J1	C_PEG_TX#6	C717	0.1U/10V_4	PEG_TX#6
PEG_RX5	P7	GFX_RX10P	GFX_TX10P	K4	C_PEG_TX5	C710	0.1U/10V_4	PEG_TX5
PEG_RX#5	M7	GFX_RX10N	GFX_TX10N	K3	C_PEG_TX#5	C712	0.1U/10V_4	PEG_TX#5
PEG_RX4	P5	GFX_RX11P	GFX_TX11P	K1	C_PEG_TX4	C713	0.1U/10V_4	PEG_TX4
PEG_RX#4	M5	GFX_RX11N	GFX_TX11N	K2	C_PEG_TX#4	C715	0.1U/10V_4	PEG_TX#4
PEG_RX3	R8	GFX_RX12P	GFX_TX12P	M4	C_PEG_TX3	C707	0.1U/10V_4	PEG_TX3
PEG_RX#3	P8	GFX_RX12N	GFX_TX12N	M3	C_PEG_TX#3	C709	0.1U/10V_4	PEG_TX#3
PEG_RX2	R6	GFX_RX13P	GFX_TX13P	M1	C_PEG_TX2	C706	0.1U/10V_4	PEG_TX2
PEG_RX#2	R5	GFX_RX13N	GFX_TX13N	M2	C_PEG_TX#2	C705	0.1U/10V_4	PEG_TX#2
PEG_RX1	P4	GFX_RX14P	GFX_TX14P	N2	C_PEG_TX1	C703	0.1U/10V_4	PEG_TX1
PEG_RX#1	P3	GFX_RX14N	GFX_TX14N	N1	C_PEG_TX#1	C704	0.1U/10V_4	PEG_TX#1
PEG_RX0	T4	GFX_RX15P	GFX_TX15P	P1	C_PEG_TX0	C699	0.1U/10V_4	PEG_TX0
PEG_RX#0	T3	GFX_RX15N	GFX_TX15N	P2	C_PEG_TX#0	C701	0.1U/10V_4	PEG_TX#0

17 PEG_RX#[15:0] PEG_RX#[15:0] PEG_TX#[15:0] 17

17 PEG_RX[15:0] PEG_RX[15:0] PEG_TX[15:0] 17

Close to North Bridge

C_PEG_TX15 C_PEG_TX15 25

C_PEG_TX#15 C_PEG_TX#15 25

C_PEG_TX14 C_PEG_TX14 25

C_PEG_TX#14 C_PEG_TX#14 25

C_PEG_TX13 C_PEG_TX13 25

C_PEG_TX#13 C_PEG_TX#13 25

C_PEG_TX12 C_PEG_TX12 25

C_PEG_TX#12 C_PEG_TX#12 25

To HDMI CONN

PCIE I/F GPP

PCIE I/F SB

PCE_CALRP(PCE_BCALRP)

PCE_CALRN(PCE_BCALRN)

33 PCIE_RXP1	AE3	GPP_RX0P	GPP_TX0P	AC1				
33 PCIE_RXN1	AD4	GPP_RX0N	GPP_TX0N	AC2				
30 PCIE_RXP2_LAN	AE2	GPP_RX1P	GPP_TX1P	AB4	PCIE_TXP1 C	C88	0.1U/10V_4	PCIE_TXP1 33
30 PCIE_RXN2_LAN	AD3	GPP_RX1N	GPP_TX1N	AB3	PCIE_TXN1 C	C89	0.1U/10V_4	PCIE_TXN1 33
	AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_TXP2 C	C679	0.1U/10V_4	PCIE_TXP2_LAN 30
	AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_TXN2 C	C696	0.1U/10V_4	PCIE_TXN2_LAN 30
	V5	GPP_RX3P	GPP_TX3P	Y1				
	W6	GPP_RX3N	GPP_TX3N	Y2				
	U5	GPP_RX4P	GPP_TX4P	Y3				
	U6	GPP_RX4N	GPP_TX4N	Y4				
	U8	GPP_RX5P	GPP_TX5P	V1				
	U7	GPP_RX5N	GPP_TX5N	V2				
12 PCIE_SB_NB_RX0P	AA8	SB_RX0P	SB_TX0P	AD7	A_TX0P C	C686	0.1U/10V_4	PCIE_SB_NB_TX0P 12
12 PCIE_SB_NB_RX0N	Y8	SB_RX0N	SB_TX0N	AE7	A_TX0N C	C687	0.1U/10V_4	PCIE_SB_NB_TX0N 12
12 PCIE_SB_NB_RX1P	AA7	SB_RX1P	SB_TX1P	AE6	A_TX1P C	C685	0.1U/10V_4	PCIE_SB_NB_TX1P 12
12 PCIE_SB_NB_RX1N	Y7	SB_RX1N	SB_TX1N	AD6	A_TX1N C	C684	0.1U/10V_4	PCIE_SB_NB_TX1N 12
12 PCIE_SB_NB_RX2P	AA5	SB_RX2P	SB_TX2P	AB6	A_TX2P C	C690	0.1U/10V_4	PCIE_SB_NB_TX2P 12
12 PCIE_SB_NB_RX2N	AA6	SB_RX2N	SB_TX2N	AC6	A_TX2N C	C691	0.1U/10V_4	PCIE_SB_NB_TX2N 12
12 PCIE_SB_NB_RX3P	W5	SB_RX3P	SB_TX3P	AD5	A_TX3P C	C688	0.1U/10V_4	PCIE_SB_NB_TX3P 12
12 PCIE_SB_NB_RX3N	Y5	SB_RX3N	SB_TX3N	AE5	A_TX3N C	C689	0.1U/10V_4	PCIE_SB_NB_TX3N 12

TO WLAN

TO PCIE-LAN

RS880

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1



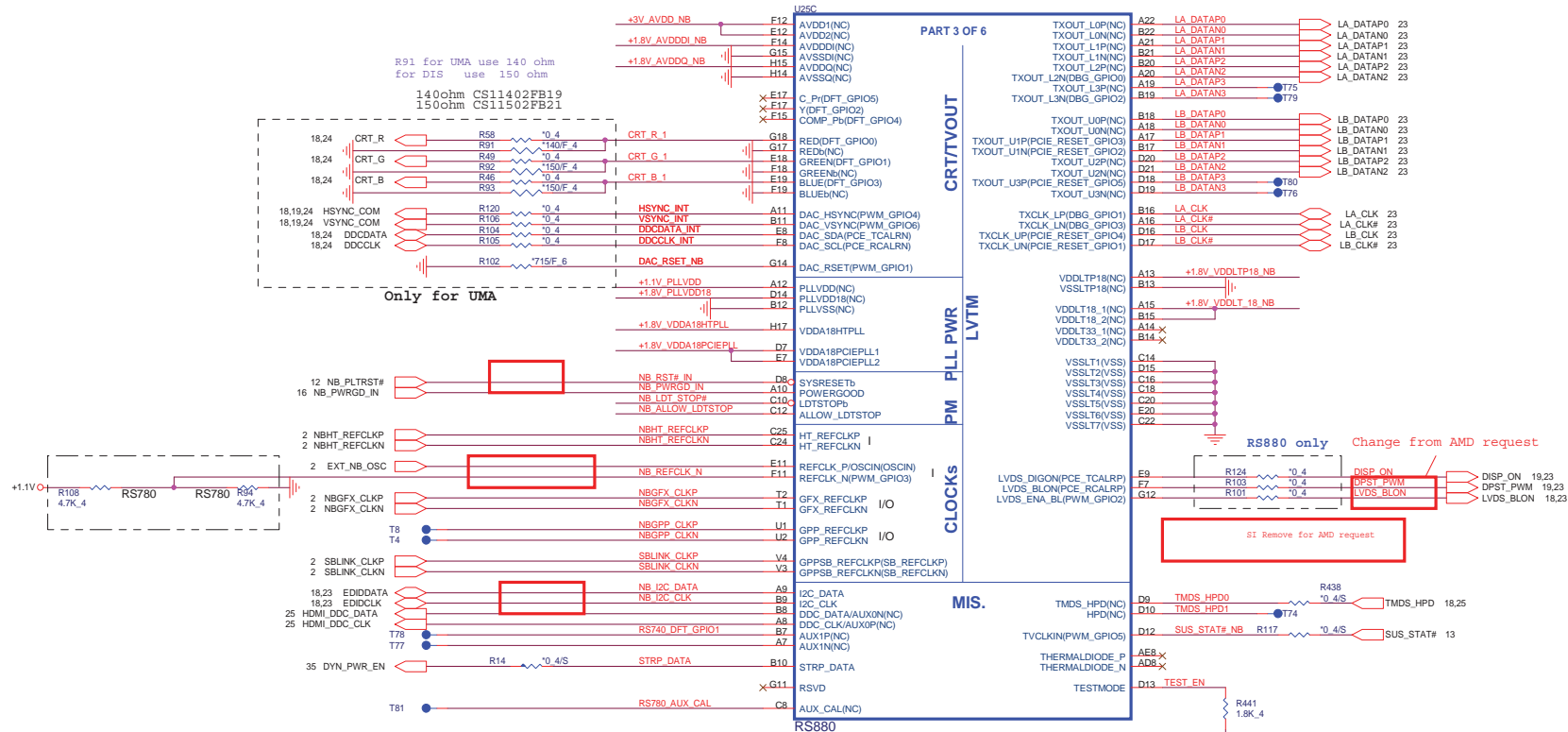
PROJECT : OP8
Quanta Computer Inc.

Size
Custom

Document Number
RS740/RS780-PCIE I/F 2/5

Rev
1A

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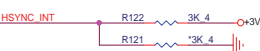
Enables Debug Bus access
through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)

```

RS780



```
| Indicates if memory Side port  
| is available or not  
0: available RS780 , Default  
1: Not available RS780  
( RS780 use HSYNC#)
```

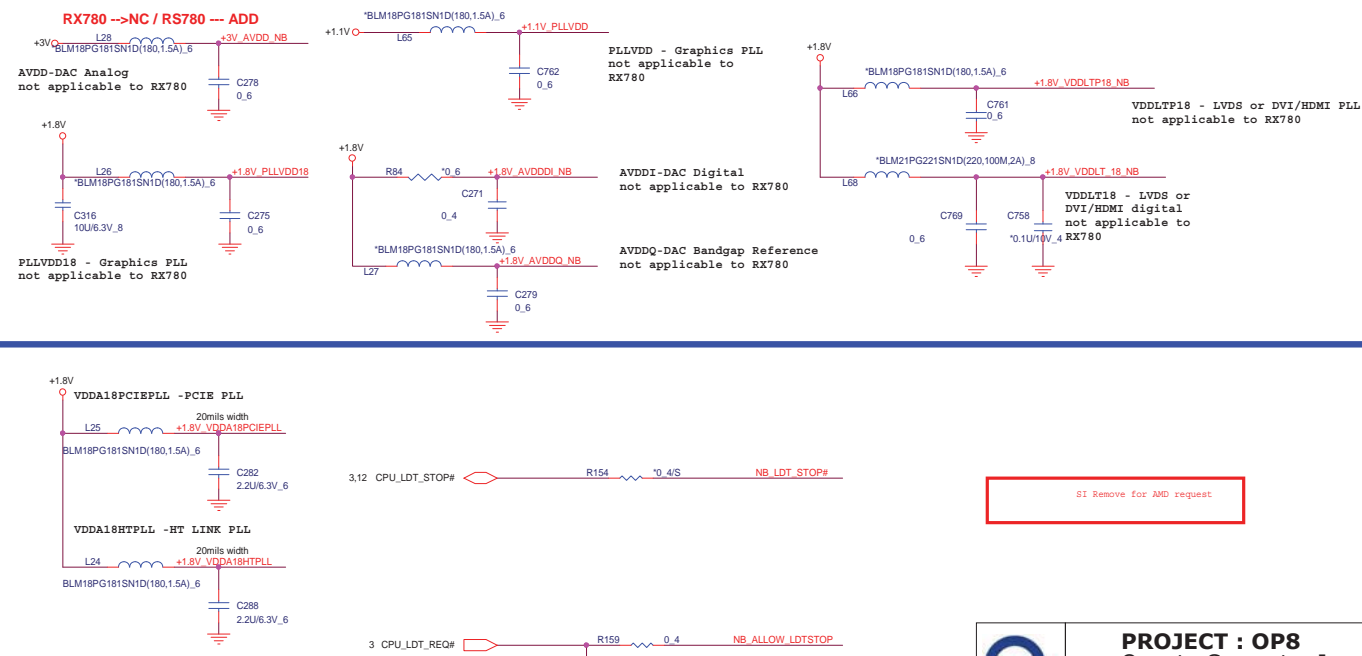
RS780

For extrnal EEPROM Debug only

RS780/RX780

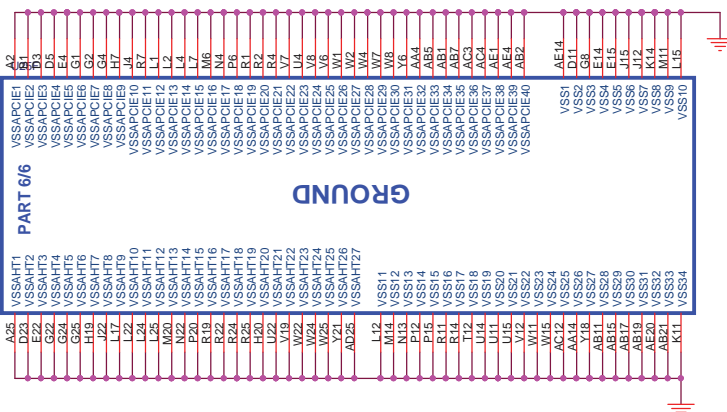


MV change:



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC



VDDHT - HT
LINK digital
I/O for
RX780/RS780

+1.1V 2A for RS880M

VDDHTRX - HT
LINK RX I/O for
RX780/RS780

0.45A

VDDHTTX - HT
LINK TX I/O for
RX780/RS780

+1.2V 2A for RS780M+SB700

0.5A

+1.8V 1A for RS780M+SB700

600mA

VDDA18PCIE -
PCIE TX stage
I/O for
RX780/RS780

VDD18 - RS780 I/O
transform

VDD18_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

U25E

PART 5/6

POWER

RS880

VDDPCIE - PCIE-E Main power

0.7A

VDDC - Core Logic power

7A

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

BLM21PG221SN1D(220,100M,2A)_8

1.8V(0.15A)

1.8V

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

0.005A

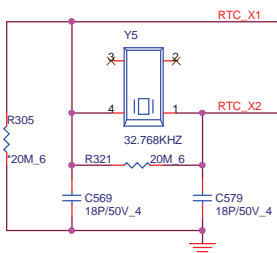
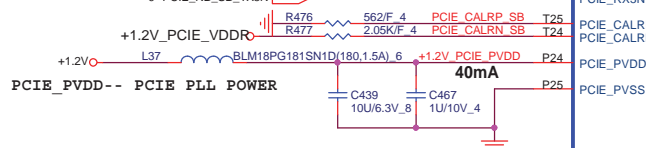
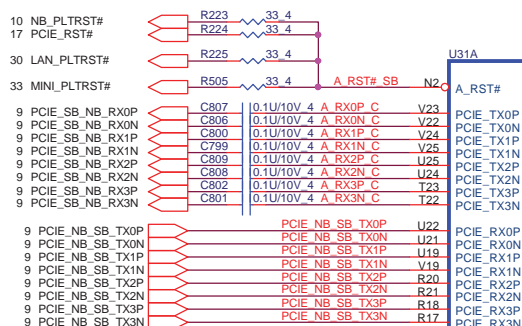


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Quanta Computer Inc.

Size Custom Document Number
RS740/RS780-POWER5/5
Date: Friday, March 20, 2009 Sheet 11 of 42 Rev 1A

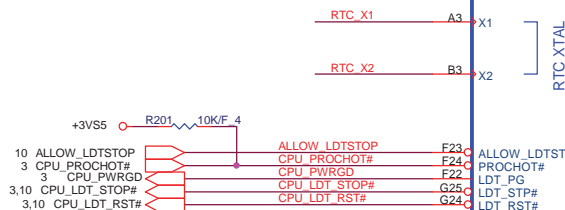
PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U600

To RS780



Change for SB710 chip

FOR A14 chip



SB710
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

SB710

Part 1 of 5

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

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PCI INTERFACE

CLOCK GENERATOR



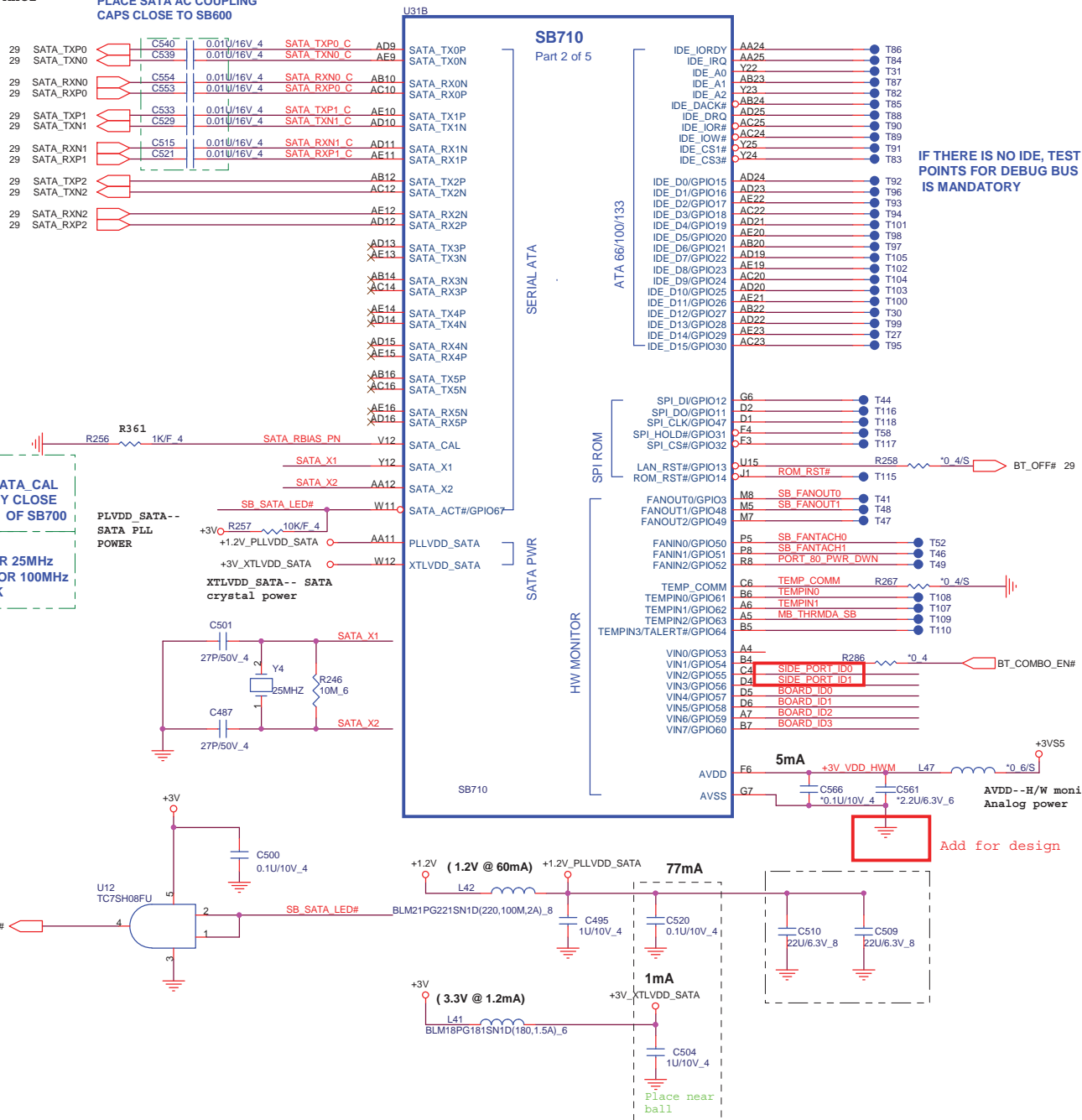
SATA PORT 0,1,2,3
can support AHCI
mode

**PLACE SATA AC COUPLING
CAPS CLOSE TO SB600**

SATA1

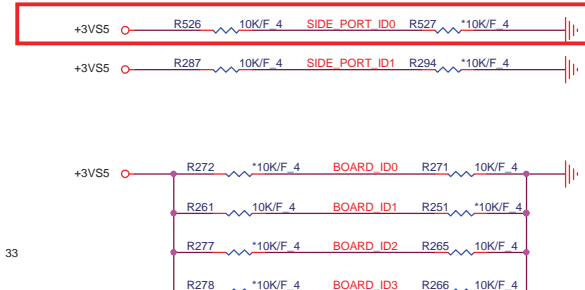
SATA ODD

E-SATA



IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no support side port



ID3	ID2	ID1	ID0	
0	0	0	0	OP8 UMA
0	0	0	1	OP9 UMA
0	0	1	0	OP8 Dis
0	0	1	1	OP9 Dis
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	



PROJECT : OP8
Quanta Computer Inc.

Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4
Date: Friday, March 20, 2009	Sheet 1

	Rev 1A
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Size Custom	Document Number SB700-PWR/DECOUPLING 4/4	Rev 1/
Date: Friday, March 20, 2009	Sheet 15 of 42	

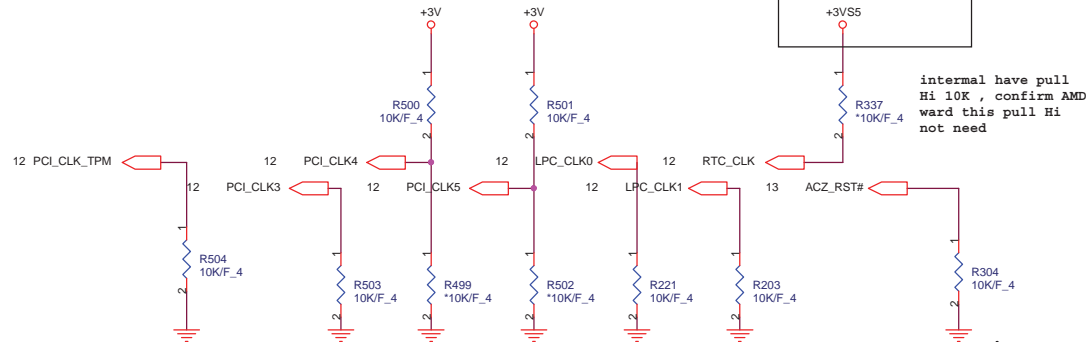


OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

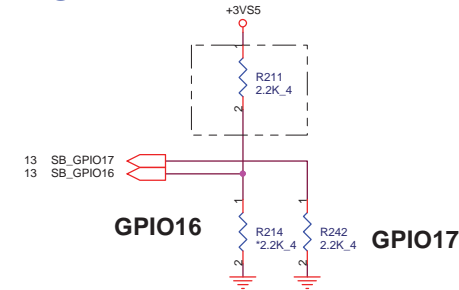
16

It must ready
before RSMRST#

REQUIRED STRAPS



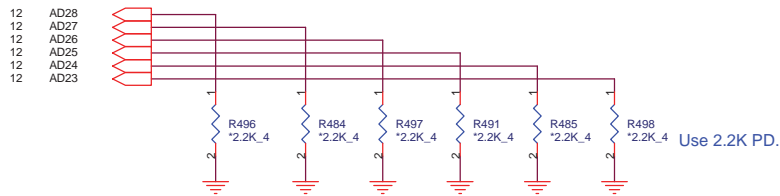
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

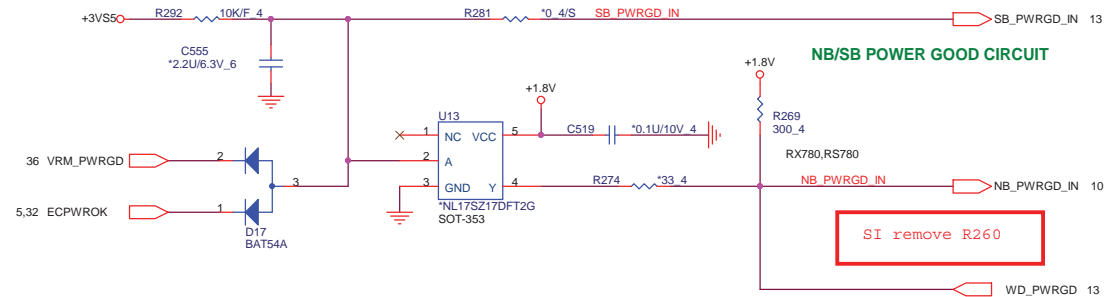
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

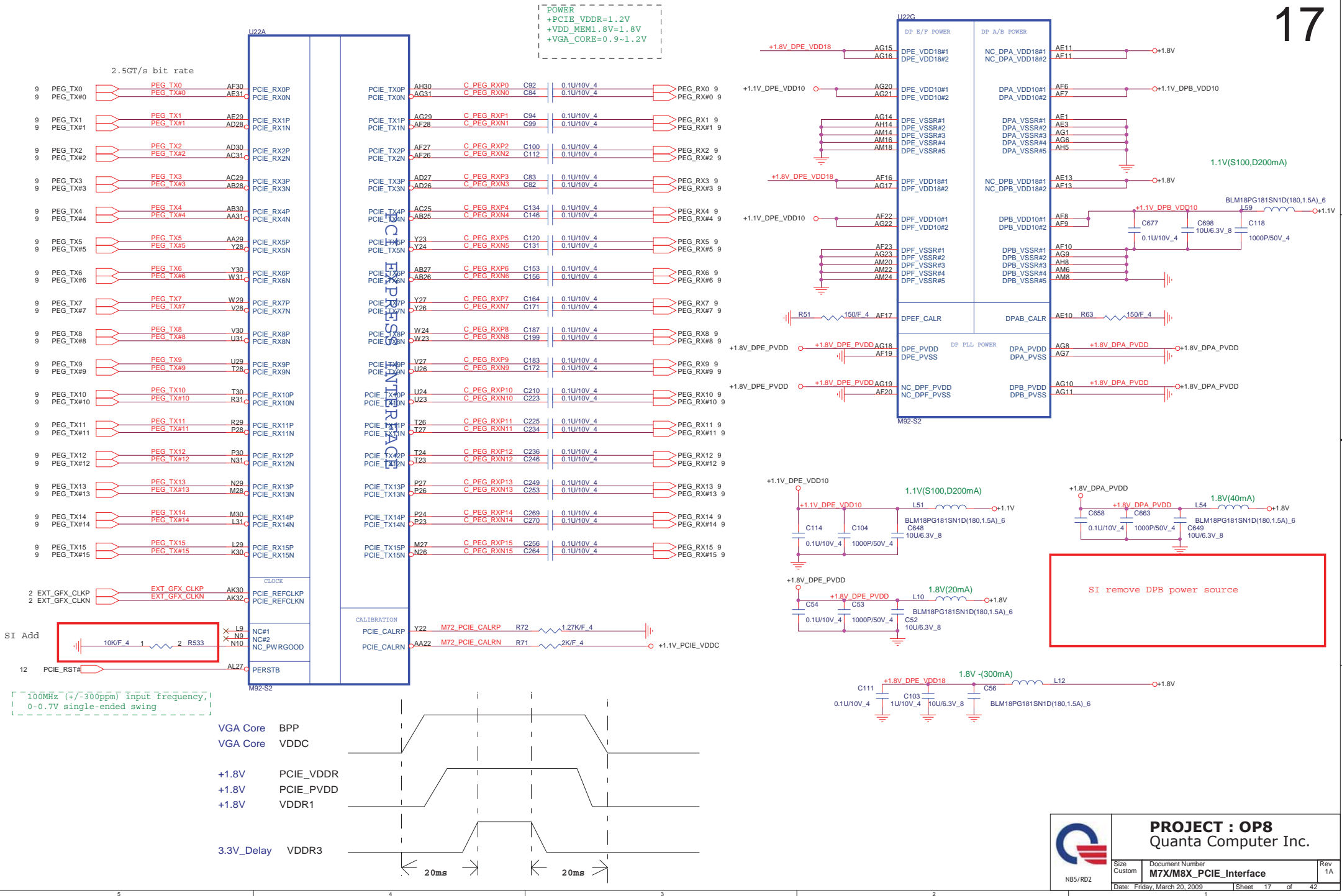


AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



PROJECT : OP8
Quanta Computer Inc.

Size Custom Document Number
SB700-STRAPS Rev 1A
Date: Friday, March 20, 2009 Sheet 16 of 42



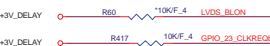


MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Hynix	4*16-500MHZ	HP516G3EPR-20L
0001	Samsung (S die)	4*16-500MHZ	KNIG164QE-HC20
0010	Qimonda (Infineon)	4*16-500MHZ	TD
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V

Need check again



SI Add GND from Check list

SI Add GND from Check list

SI Add GND from Check list

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+VDDR4

Memory ID

R401

R402

R403

R404

R405

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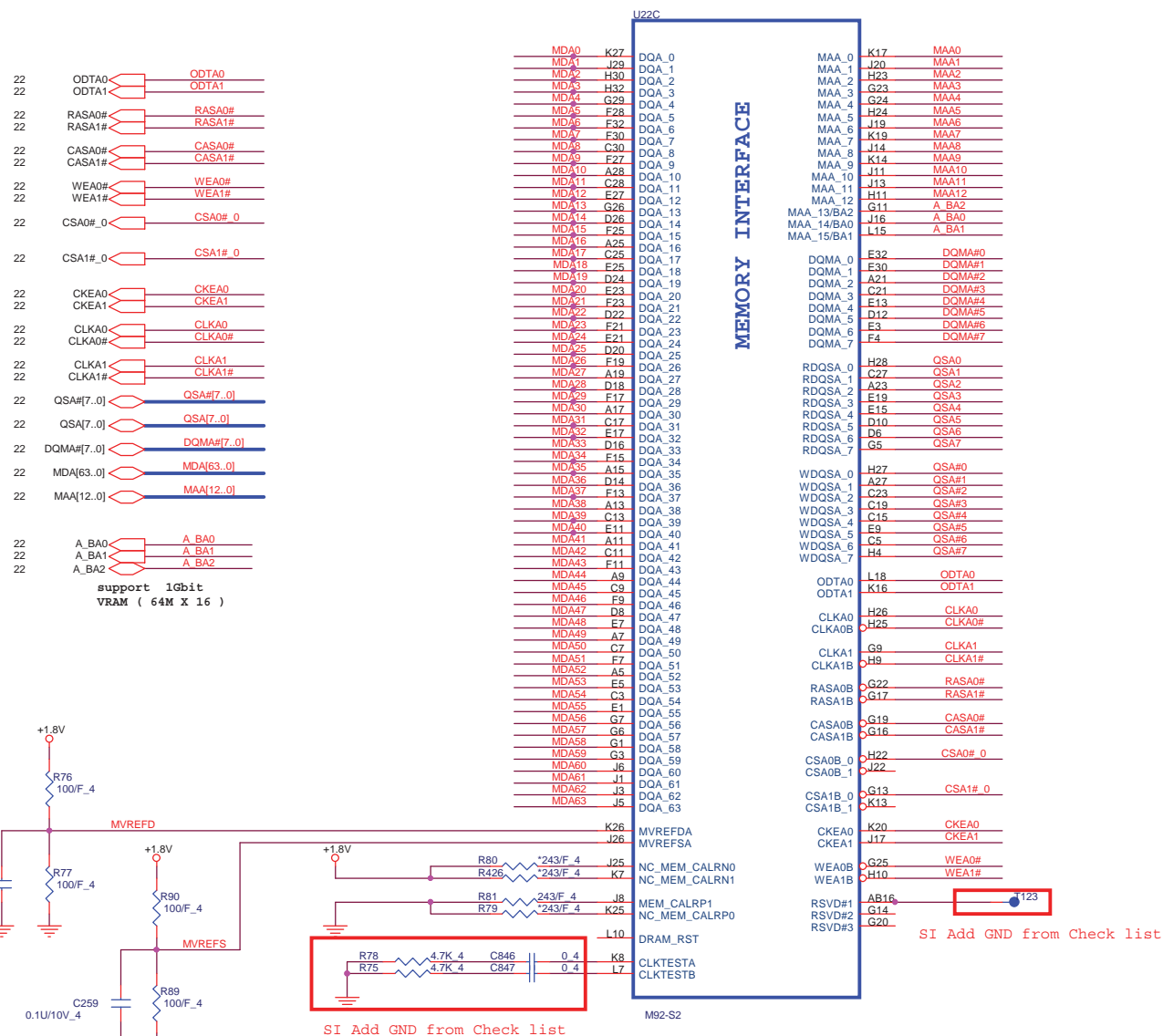
It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.



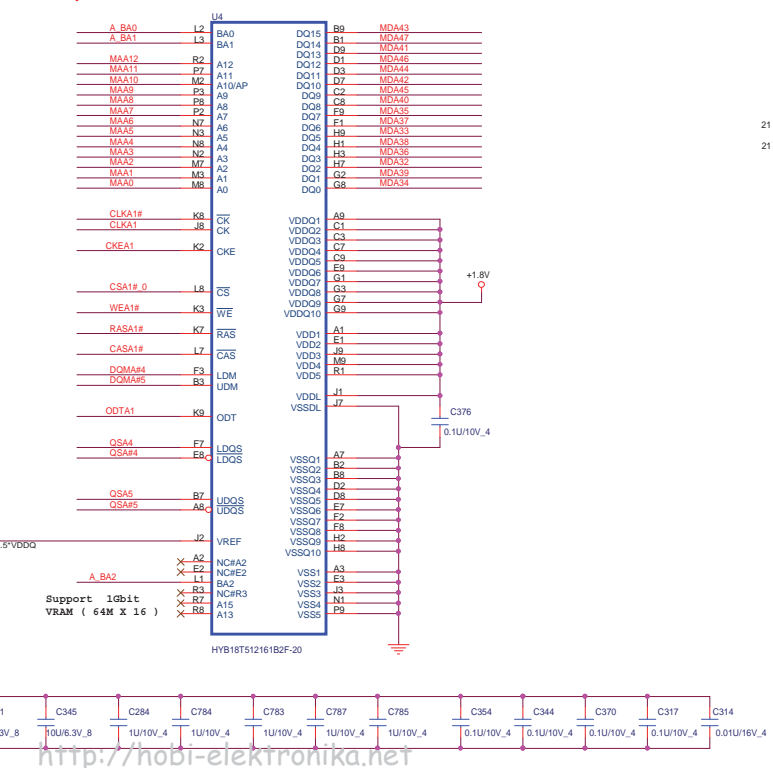
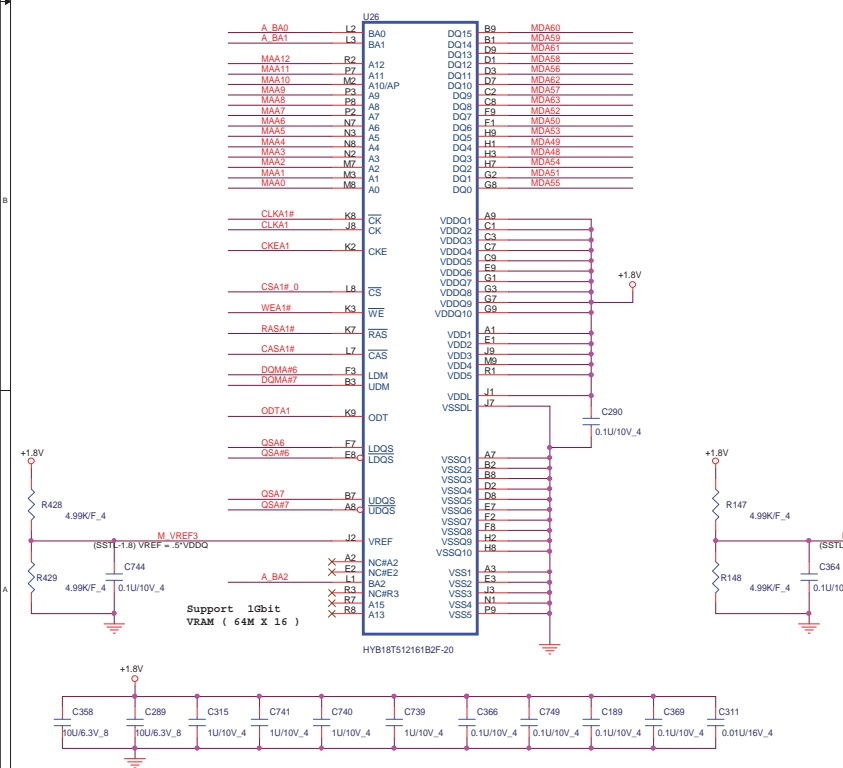
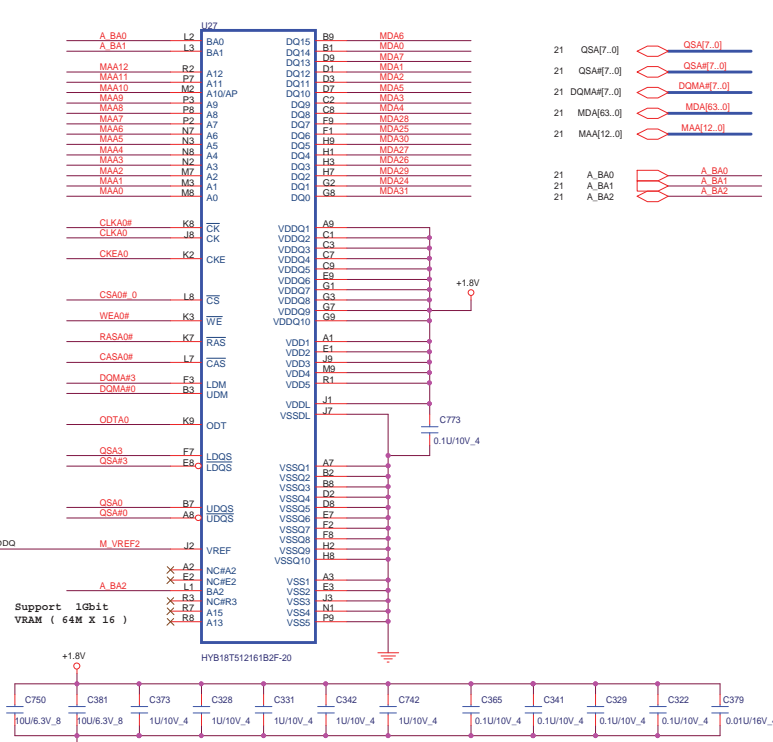
PROJECT : OP8
Quanta Computer Inc.

Size Custom	Document Number M7X/M8X_GND / LVDS/ Straps	Rev 1A
Date: Friday, March 20, 2009		Sheet 19 of 42





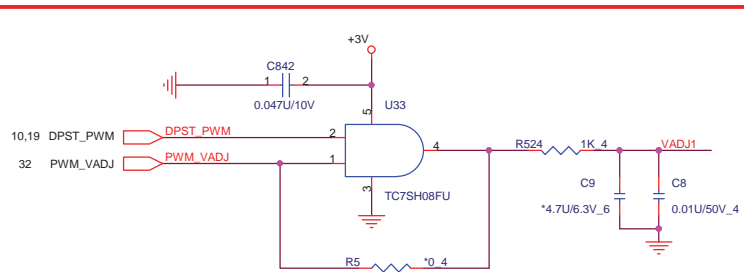
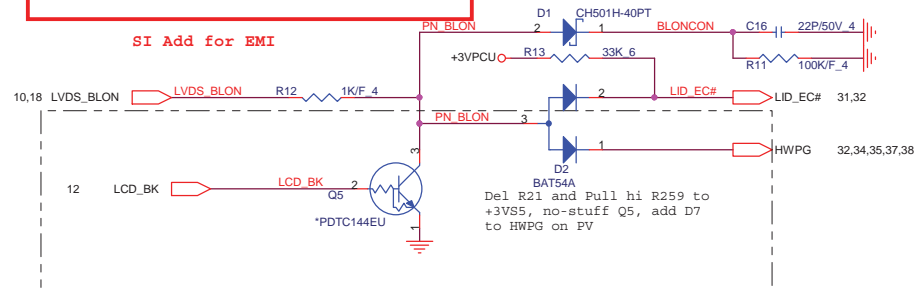
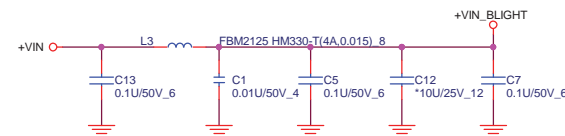
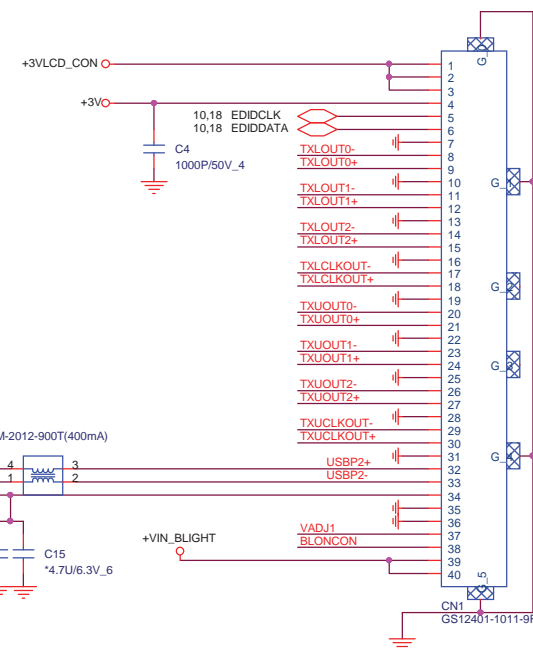
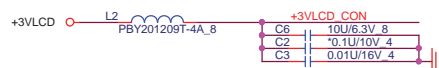
Change MEMTEST to 240 1%
ohm to GND , AMD update



Size C	Document Number M92/VRAM_A0,A1	Rev 1
Date: Friday, March 20, 2009	Sheet 22 of 42	

10	LA_CLK	LA_CLK	RP1	3	1	2	0	4P2R	4	TXCLKOUT+
10	LA_CLK#	LA_CLK#			1	2	0	4P2R	4	TXCLKOUT-
10	LA_DATAP0	LA_DATAP0	RP2	3	1	2	0	4P2R	4	TXOUT0+
10	LA_DATAN0	LA_DATAN0			1	2	0	4P2R	4	TXOUT0-
10	LA_DATAP1	LA_DATAP1	RP3	3	1	2	0	4P2R	4	TXOUT1+
10	LA_DATAN1	LA_DATAN1			1	2	0	4P2R	4	TXOUT1-
10	LA_DATAP2	LA_DATAP2	RP4	3	1	2	0	4P2R	4	TXOUT2+
10	LA_DATAN2	LA_DATAN2			1	2	0	4P2R	4	TXOUT2-
10	LB_CLK	LB_CLK	RP5	3	1	2	0	4P2R	4	TXCLKOUT+
10	LB_CLK#	LB_CLK#			1	2	0	4P2R	4	TXCLKOUT-
10	LB_DATAP0	LB_DATAP0	RP6	3	1	2	0	4P2R	4	TXOUT0+
10	LB_DATAN0	LB_DATAN0			1	2	0	4P2R	4	TXOUT0-
10	LB_DATAP1	LB_DATAP1	RP7	3	1	2	0	4P2R	4	TXOUT1+
10	LB_DATAN1	LB_DATAN1			1	2	0	4P2R	4	TXOUT1-
10	LB_DATAP2	LB_DATAP2	RP8	3	1	2	0	4P2R	4	TXOUT2+
10	LB_DATAN2	LB_DATAN2			3	4	0	4P2R	4	TXOUT2-

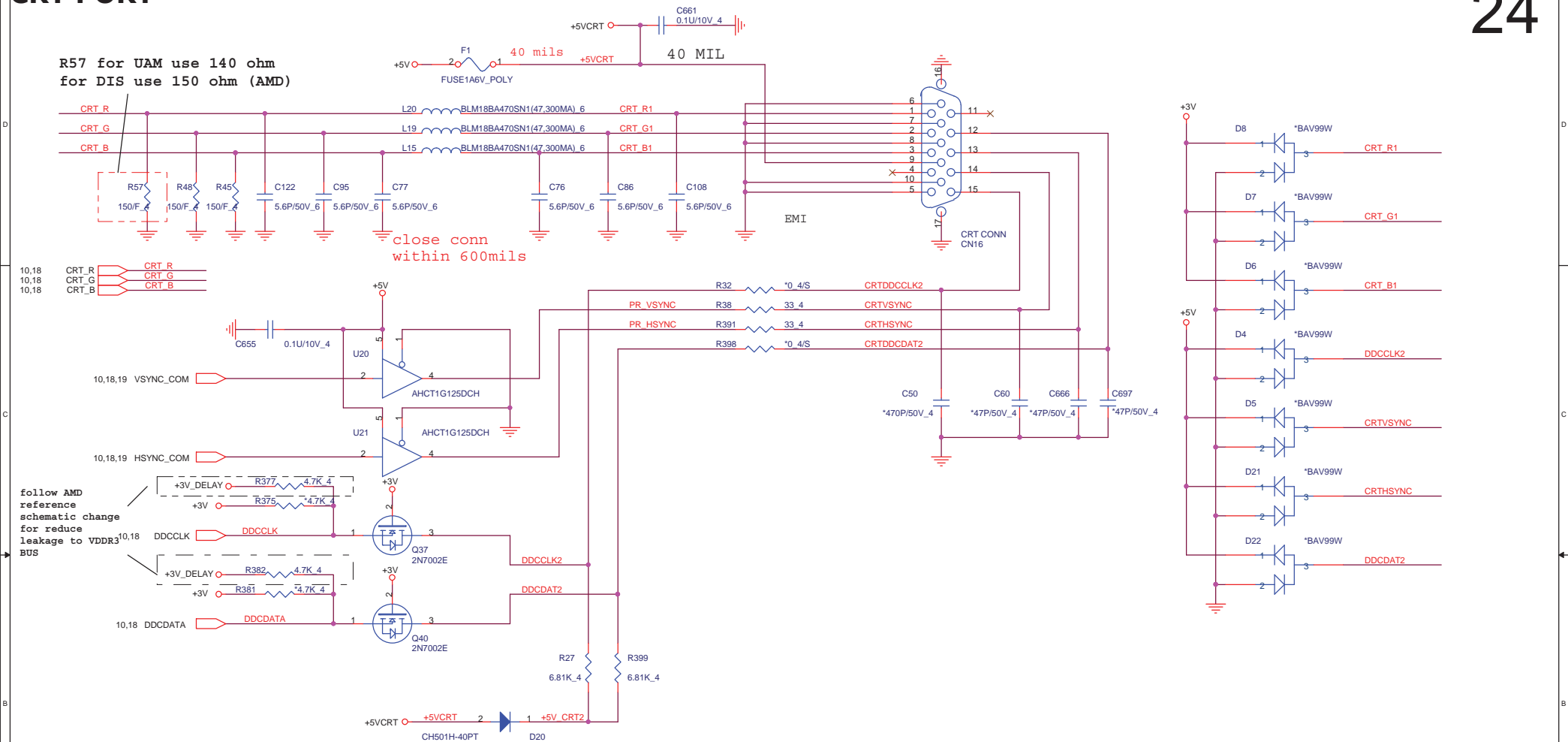
EXT_TXCLKOUT-	EXT_TXCLKOUT+	RP49	3	4	0_4P2R_4	TXCLKOUT-	TXCLKOUT+
19 EXT_TXCLKOUT-	EXT_TXCLKOUT-	RP49	3	1	2	TXCLKOUT-	TXCLKOUT+
19 EXT_TXCLKOUT+	EXT_TXCLKOUT+			2	4		
19 EXT_TXCLKOUT0-	EXT_TXCLKOUT0-	RP50	3	1	2	TXCLKOUT0-	TXCLKOUT0+
19 EXT_TXCLKOUT0+	EXT_TXCLKOUT0+			2	4		
19 EXT_TXCLKOUT1-	EXT_TXCLKOUT1-	RP51	3	1	2	TXCLKOUT1-	TXCLKOUT1+
19 EXT_TXCLKOUT1+	EXT_TXCLKOUT1+			2	4		
19 EXT_TXCLKOUT2-	EXT_TXCLKOUT2-	RP52	3	1	2	TXCLKOUT2-	TXCLKOUT2+
19 EXT_TXCLKOUT2+	EXT_TXCLKOUT2+			2	4		
19 EXT_TXCLKOUT7-	EXT_TXCLKOUT7-			3	4		
19 EXT_TXCLKOUT7+	EXT_TXCLKOUT7+	RP53	3	1	2	TXCLKOUT7-	TXCLKOUT7+
19 EXT_TXCLKOUT0+	EXT_TXCLKOUT0+			2	4		
19 EXT_TXCLKOUT0+	EXT_TXCLKOUT0+	RP54	3	1	2	TXCLKOUT0+	TXCLKOUT0+
19 EXT_TXCLKOUT0-	EXT_TXCLKOUT0-			2	4		
19 EXT_TXCLKOUT1-	EXT_TXCLKOUT1-	RP55	3	1	2	TXCLKOUT1-	TXCLKOUT1+
19 EXT_TXCLKOUT1+	EXT_TXCLKOUT1+			2	4		
19 EXT_TXCLKOUT1-	EXT_TXCLKOUT1-	RP56	3	1	2	TXCLKOUT1-	TXCLKOUT1+
19 EXT_TXCLKOUT1+	EXT_TXCLKOUT1+			2	4		
19 EXT_TXCLKOUT2-	EXT_TXCLKOUT2-			3	4		
19 EXT_TXCLKOUT2+	EXT_TXCLKOUT2+			2	4		



SI add U33,R524,C842 for Vari bright function

CRT PORT

R57 for UAM use 140 ohm
for DIS use 150 ohm (AMD)



NB5/RD2

PROJECT : OP8
Quanta Computer Inc.

Size
CustomDocument Number
CRTRev
1A

Date: Friday, March 20, 2009

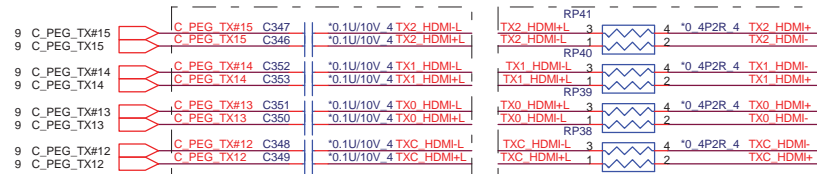
Sheet 24 of 42

UMA/DISCRETE select for HDMI

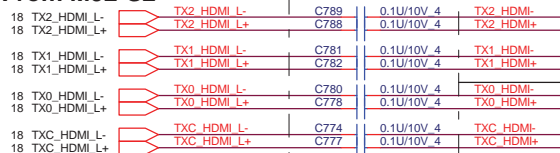
From RS780M

for Layout
concern
,placement close
north bridge

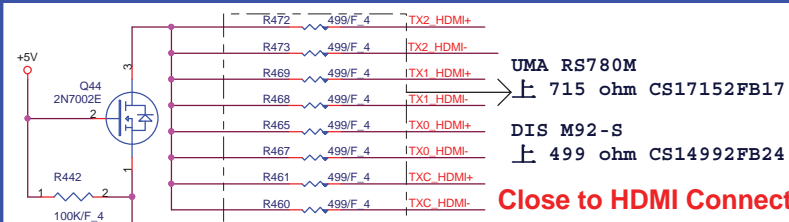
for Layout
concern
,placement close
HDMI conn



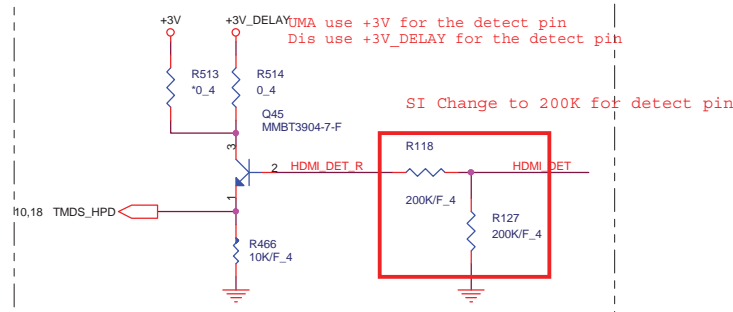
From M92-S2



for Layout
concern
,placement close
HDMI conn

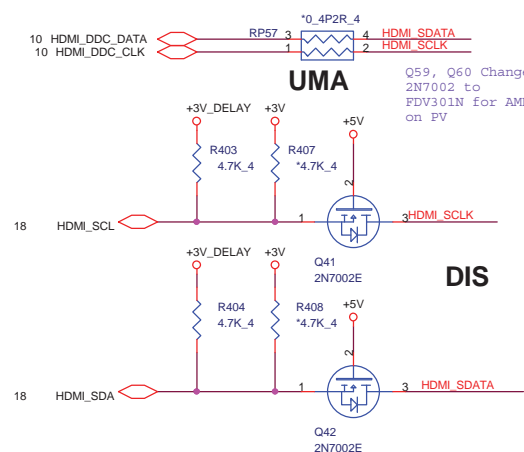


HDMI HPD SENSE



UMA AND DISCRETE HDMI I2C SELECT

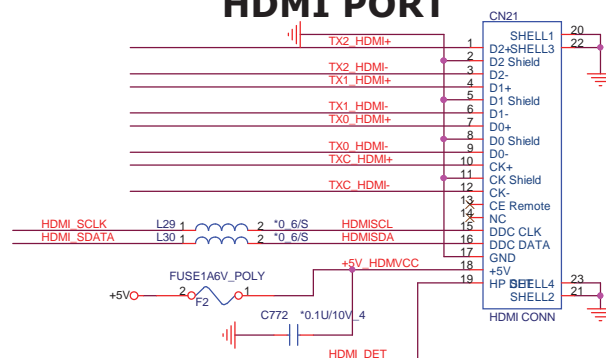
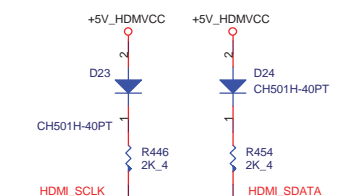
Close to HDMI Connector



Discrete DDC4 is 5V
tolerance, the MOSFET
level shifter no need
UMA DDC is 3V
tolerance, the MOSFET
level shifter is need

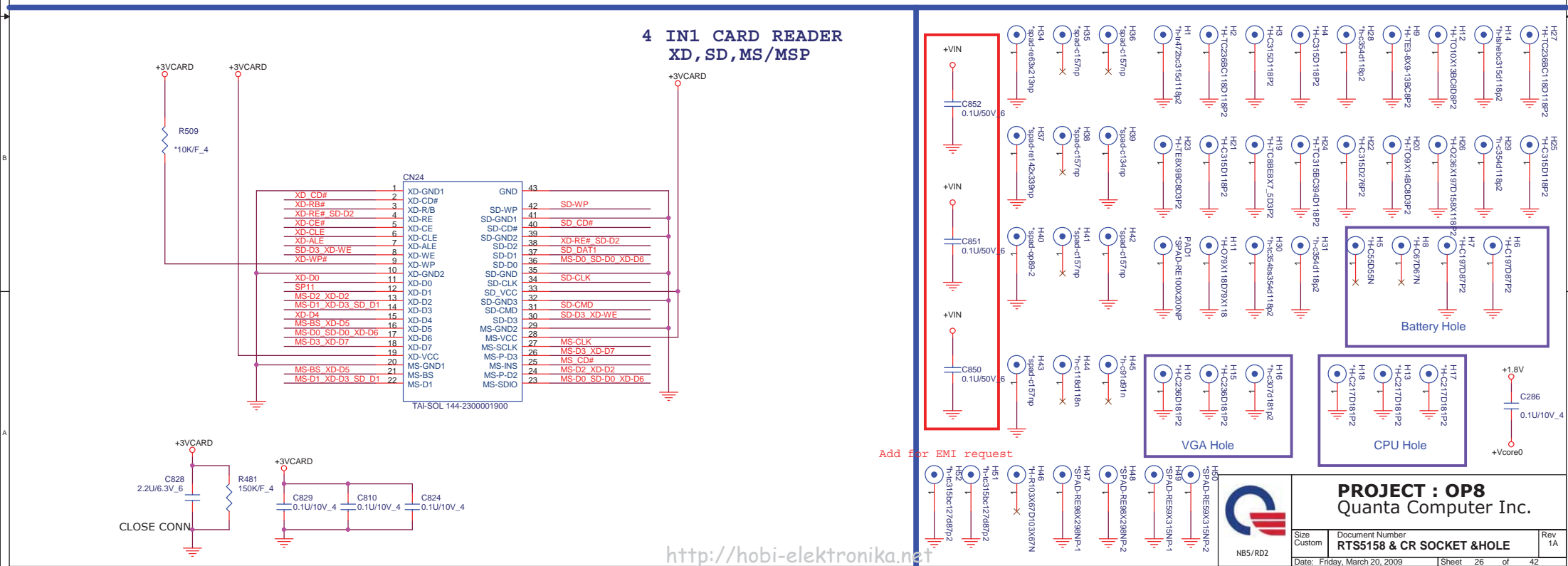
SI Change for DIS HDMI

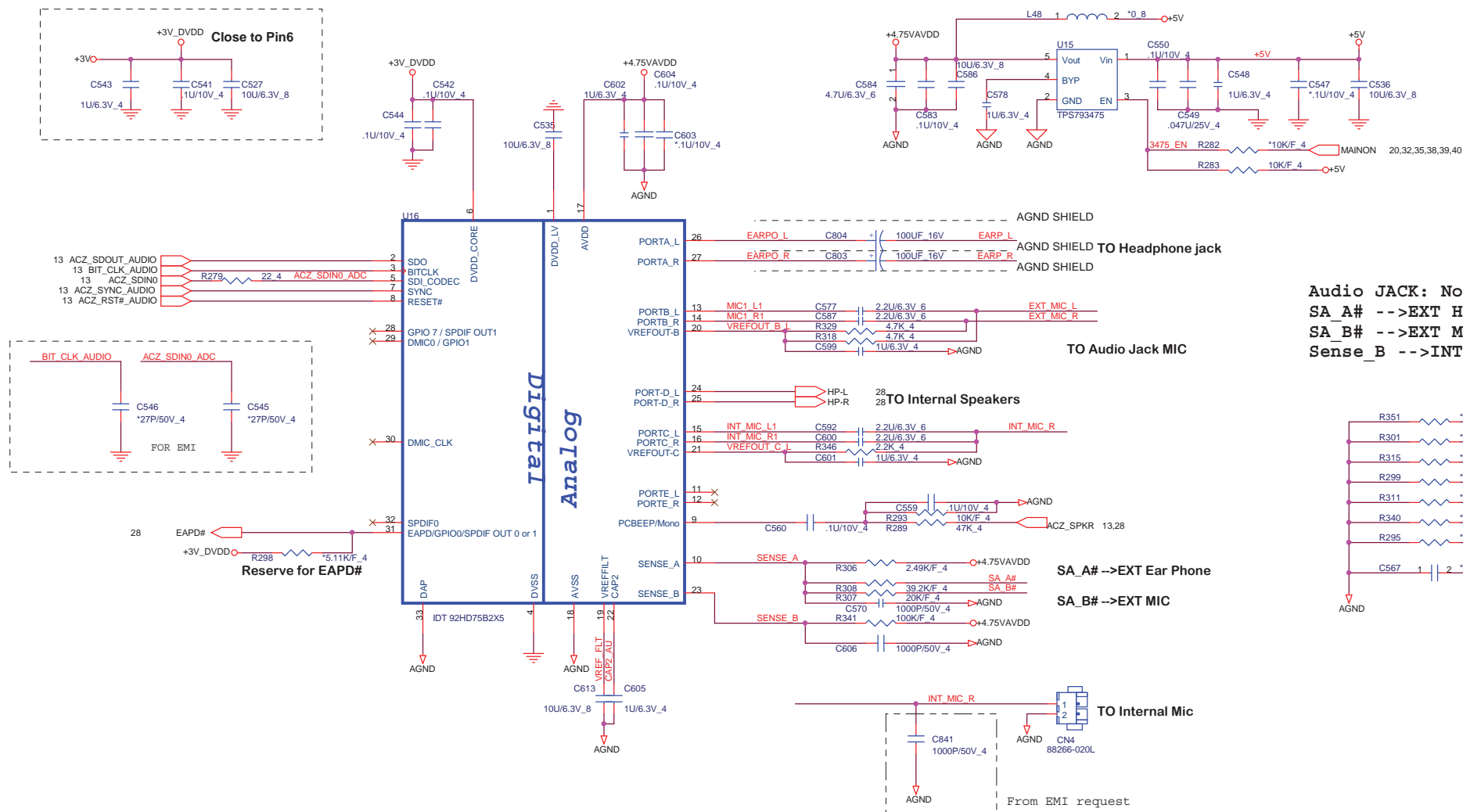
HDMI PORT



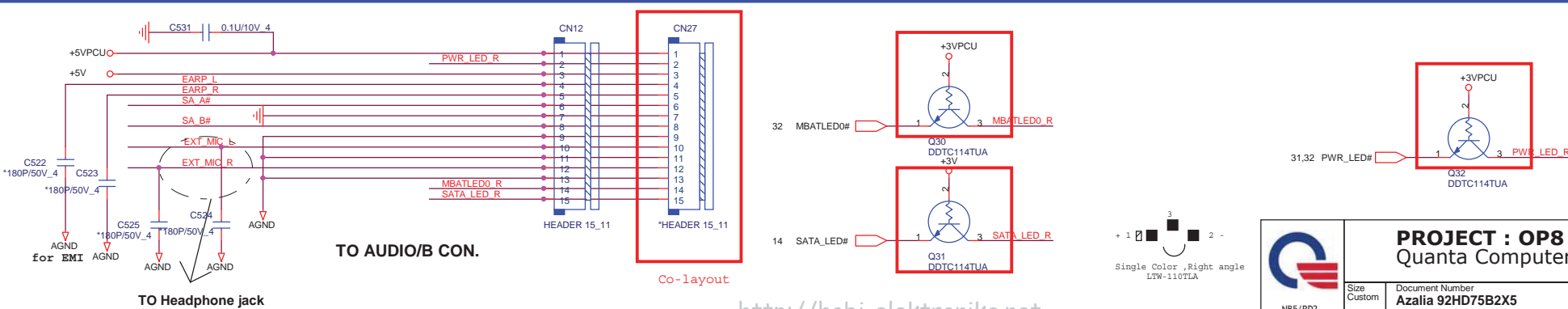
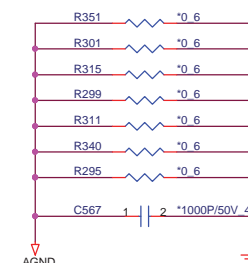
PROJECT : OP8
Quanta Computer Inc.

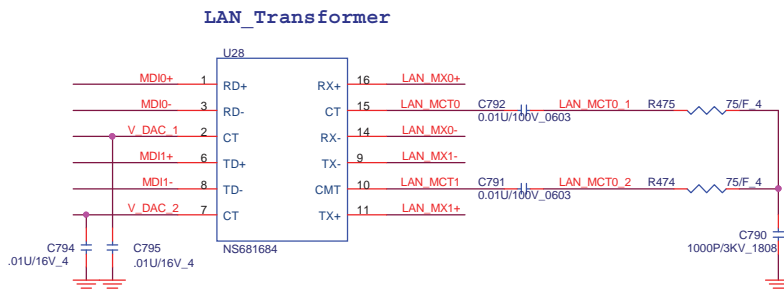
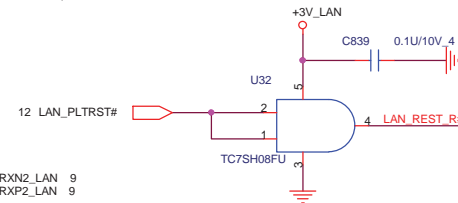
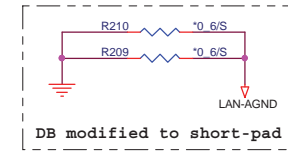
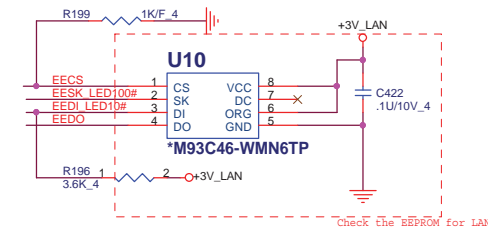
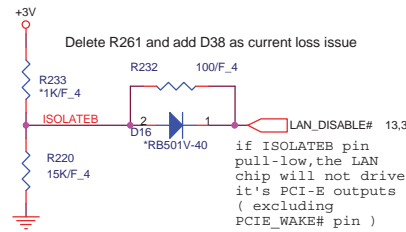
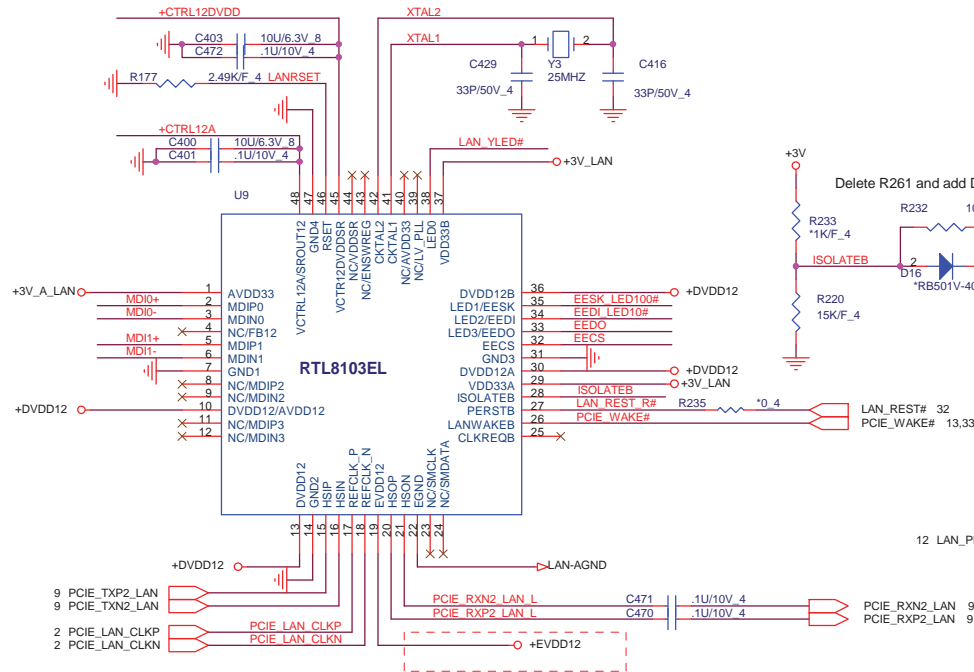
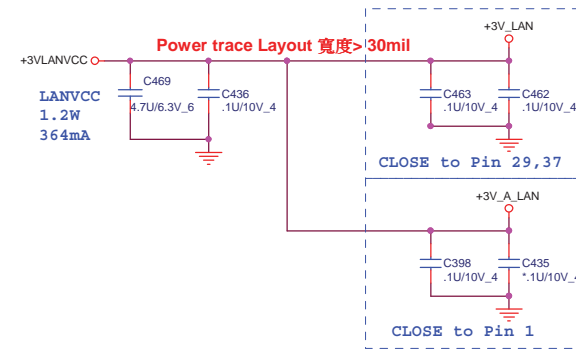
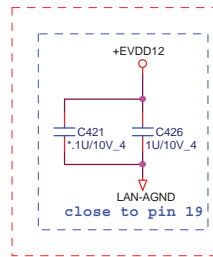
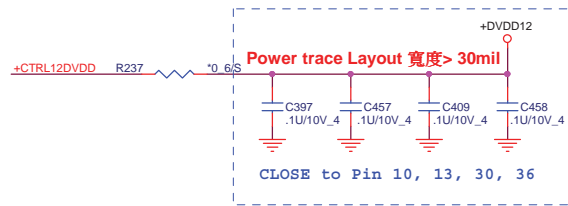
Size Custom	Document Number HDMI	Rev 1A
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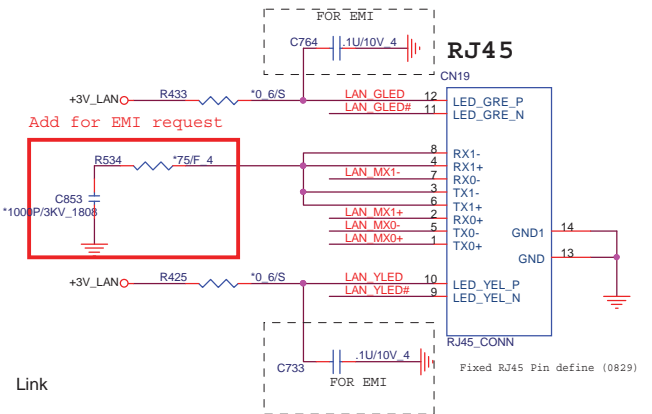
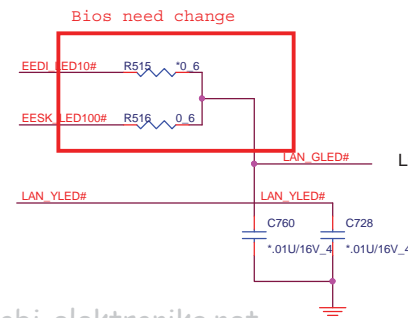


Audio JACK: Normal Open
SA_A# -->EXT HP
SA_B# -->EXT MIC
Sense_B -->INT MIC





Symbol	Type	Pin No (64-Pin)	Pin No (48-Pin)	Description
LED0	O	57	38	LED0 Tx/Rx
LED1	O	56	35	LED1 Tx/Rx
LED2	O	55	34	LED2 Tx/Rx
LED3	O	54	33	LED3 Tx/Rx

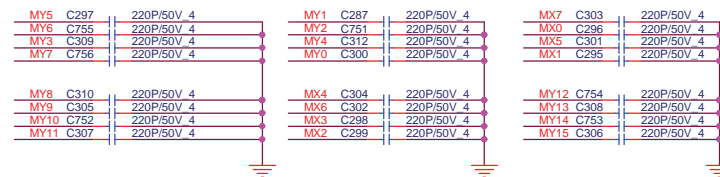
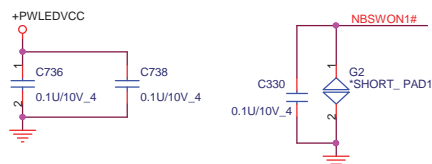


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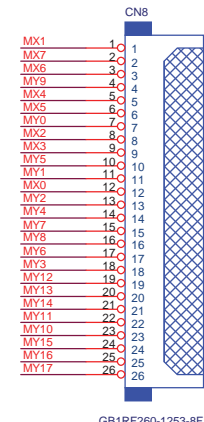
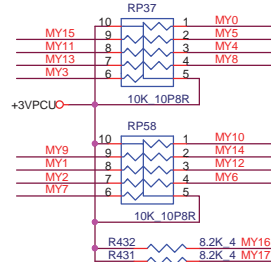
Size	Document Number	Rev
Custom	RTL8102EL/RJ45	1A
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POWER BUTTON CONNECT

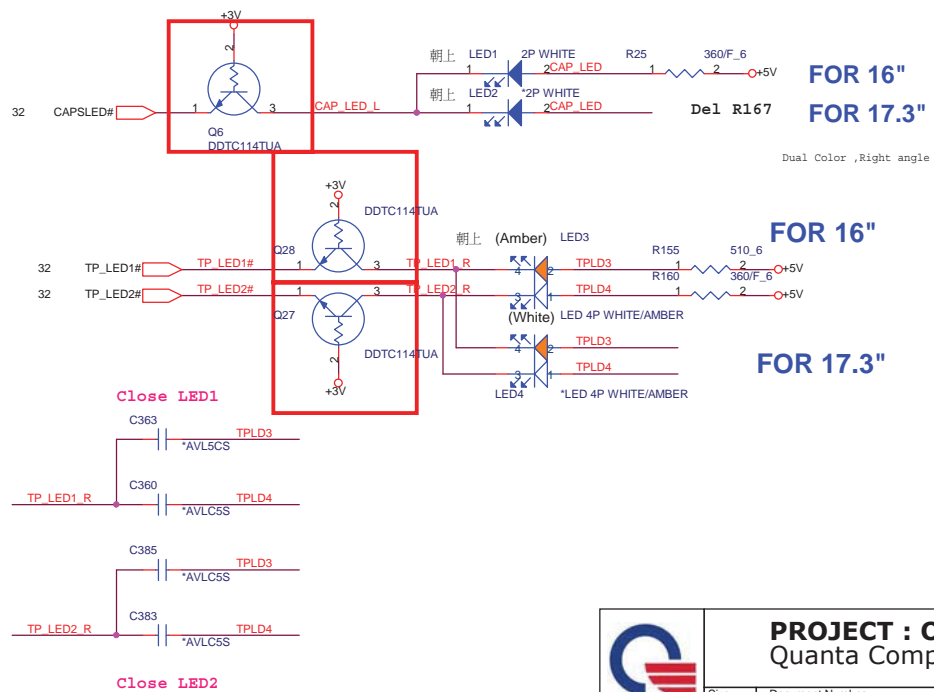
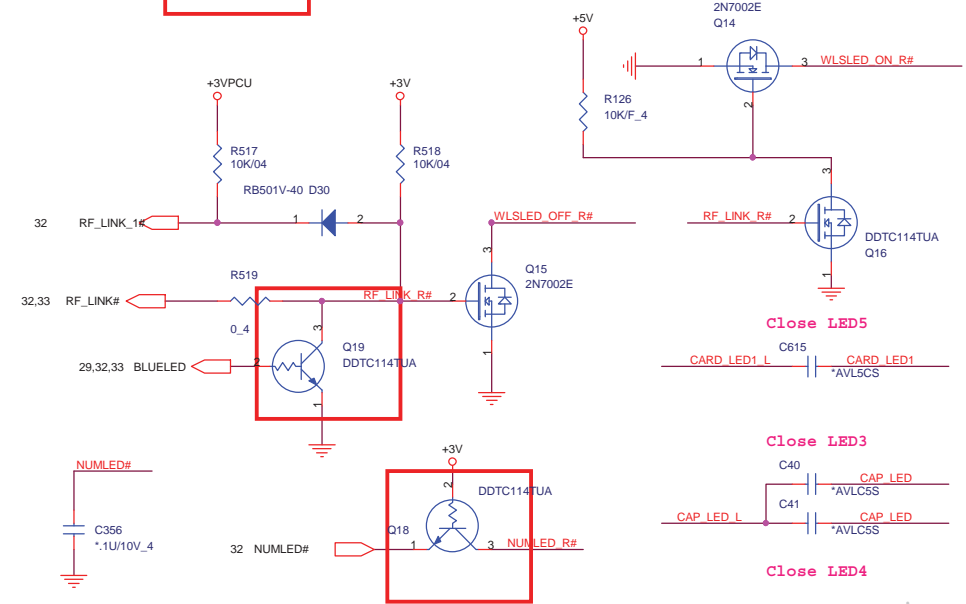
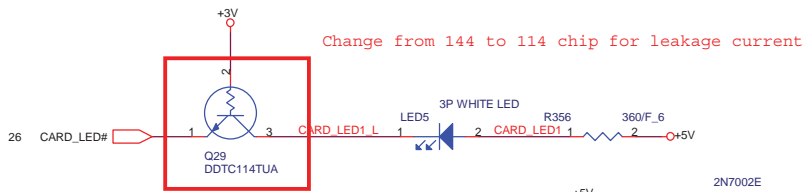
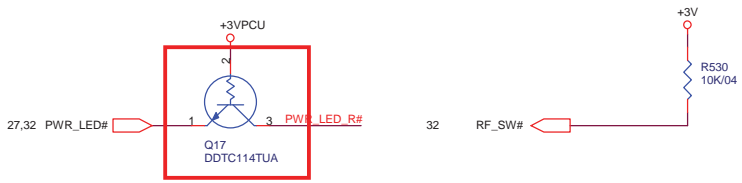
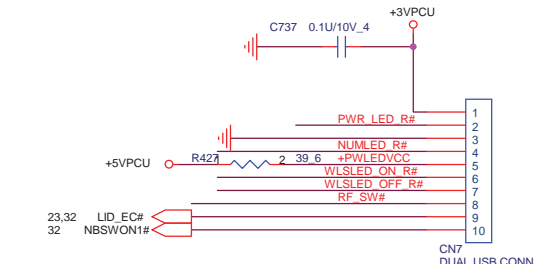
31



KEYBOARD PULL-UP



1. +3VPCU(LIDSWITCH PWR)
2. PWR_LED#
3. GND
4. NumLED
5. +5VPCU (PWRLED PWR)
6. WLSLED_ON#
7. WLSLED_OFF#
8. RF_SW#
9. LIDSWITCH
10. POWERON#

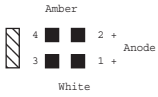


FOR 16"
FOR 17.3"

Dual Color ,Right angle

FOR 16"

FOR 17.3"



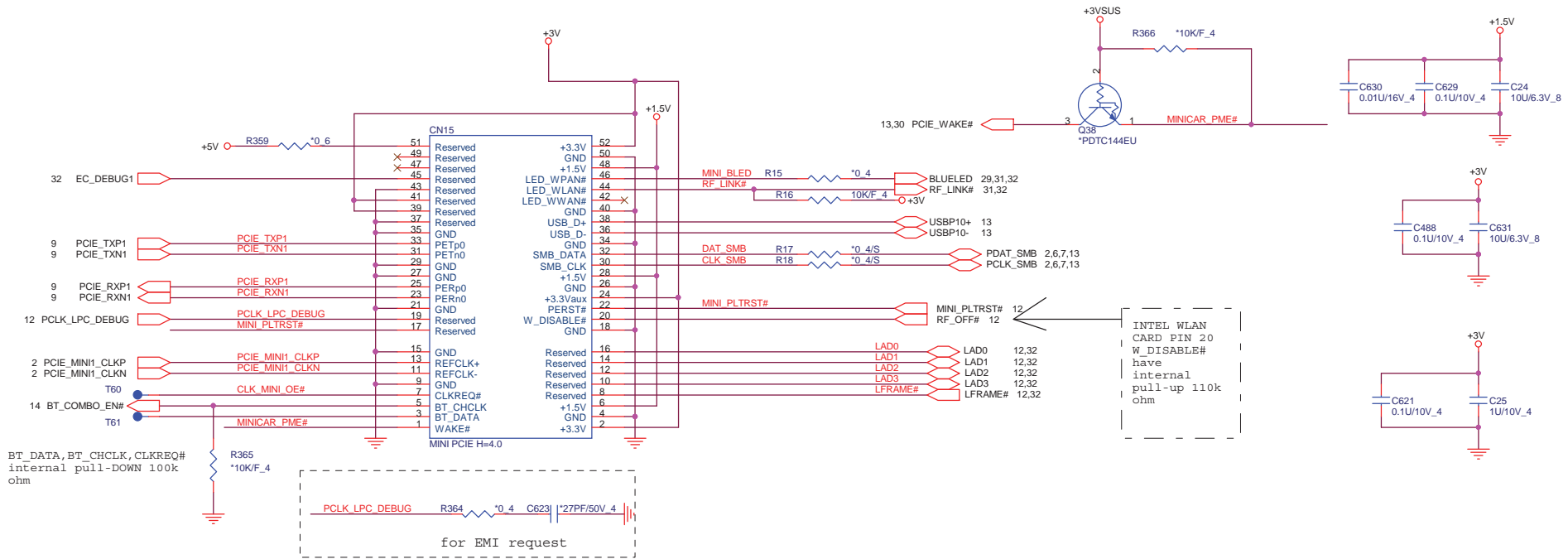
<http://hobi-elektronika.net>

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LED/KEYBOARD/SW_BOARD		
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Mini PCI-E Card 1 WLAN

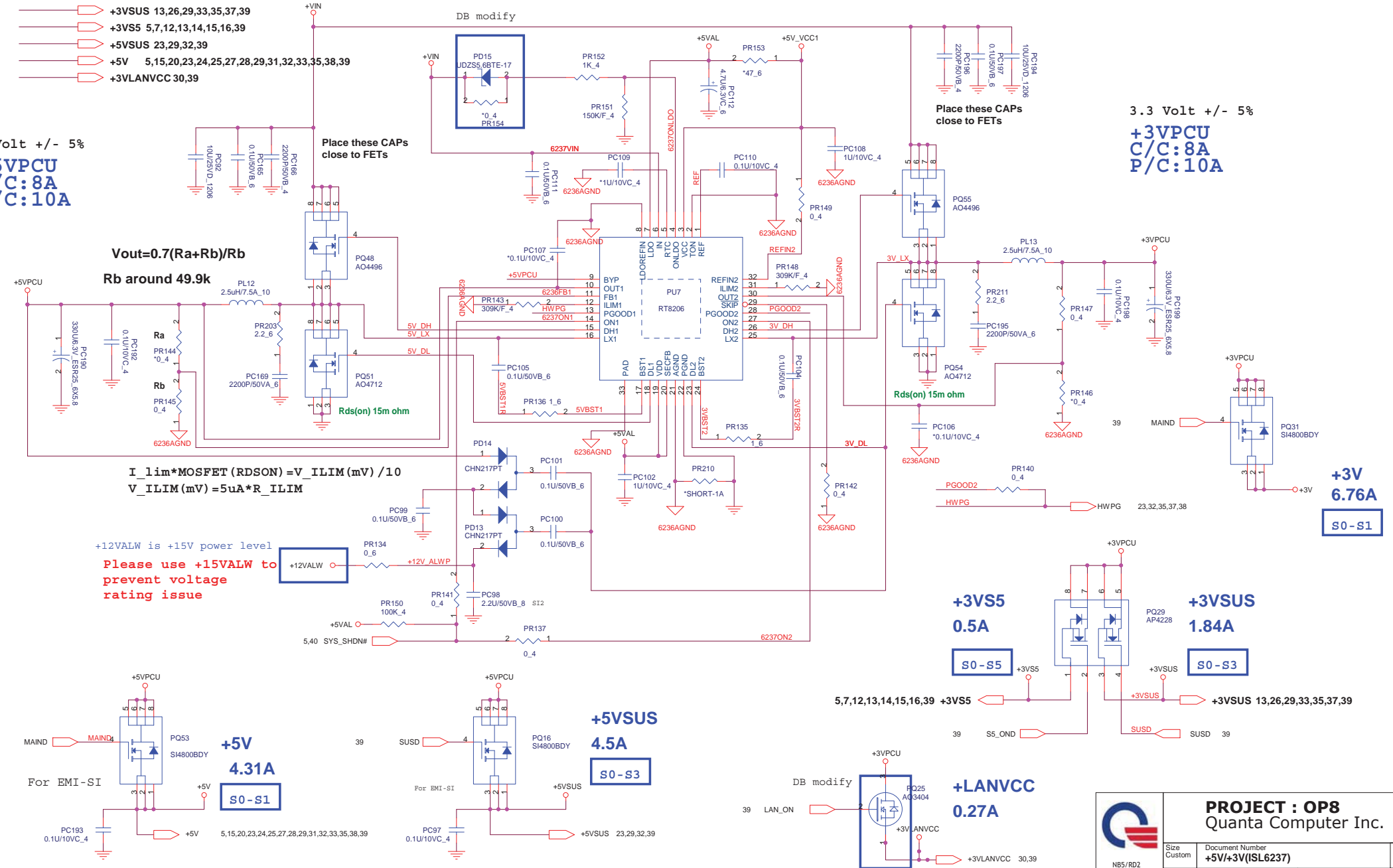
33



DC/DC +3VPCU/+ 5VPCU/ +12VALW

- +5VPCU 27,31,32,35,36,37,38
- +3VPCU 5,12,23,27,29,31,32,36,37,38,40
- +3VSUS 13,26,29,33,35,37,39
- +3VS5 5,7,12,13,14,15,16,39
- +5VSUS 23,29,32,39
- +5V 5,15,20,23,24,25,27,28,29,31,32,33,35,38,39
- +3VLAVCC 30,39

5 Volt +/- 5%
+5VPCU
C/C:8A
P/C:10A

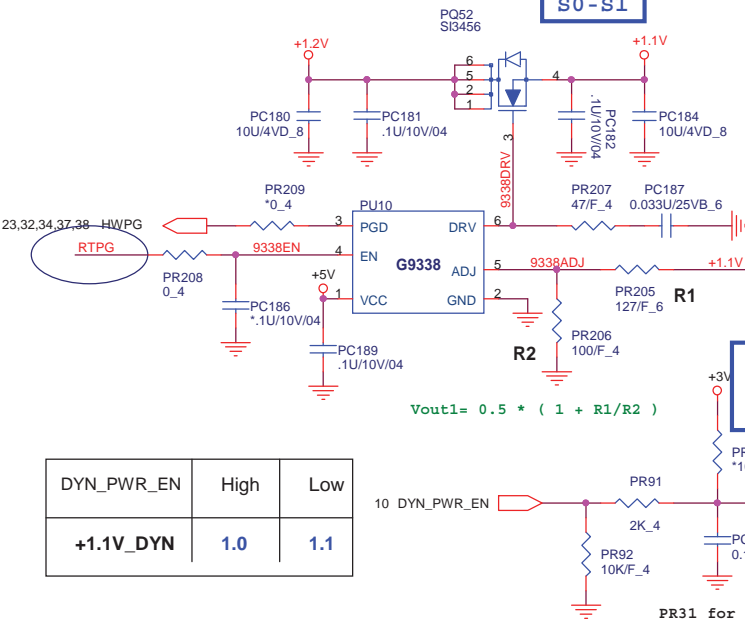


$$T_{on} = 3.85p \cdot R_{TON} \cdot V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} \cdot T_{ON})$$

reserved for pwr seq -- andrew

3.82A
S0-S1



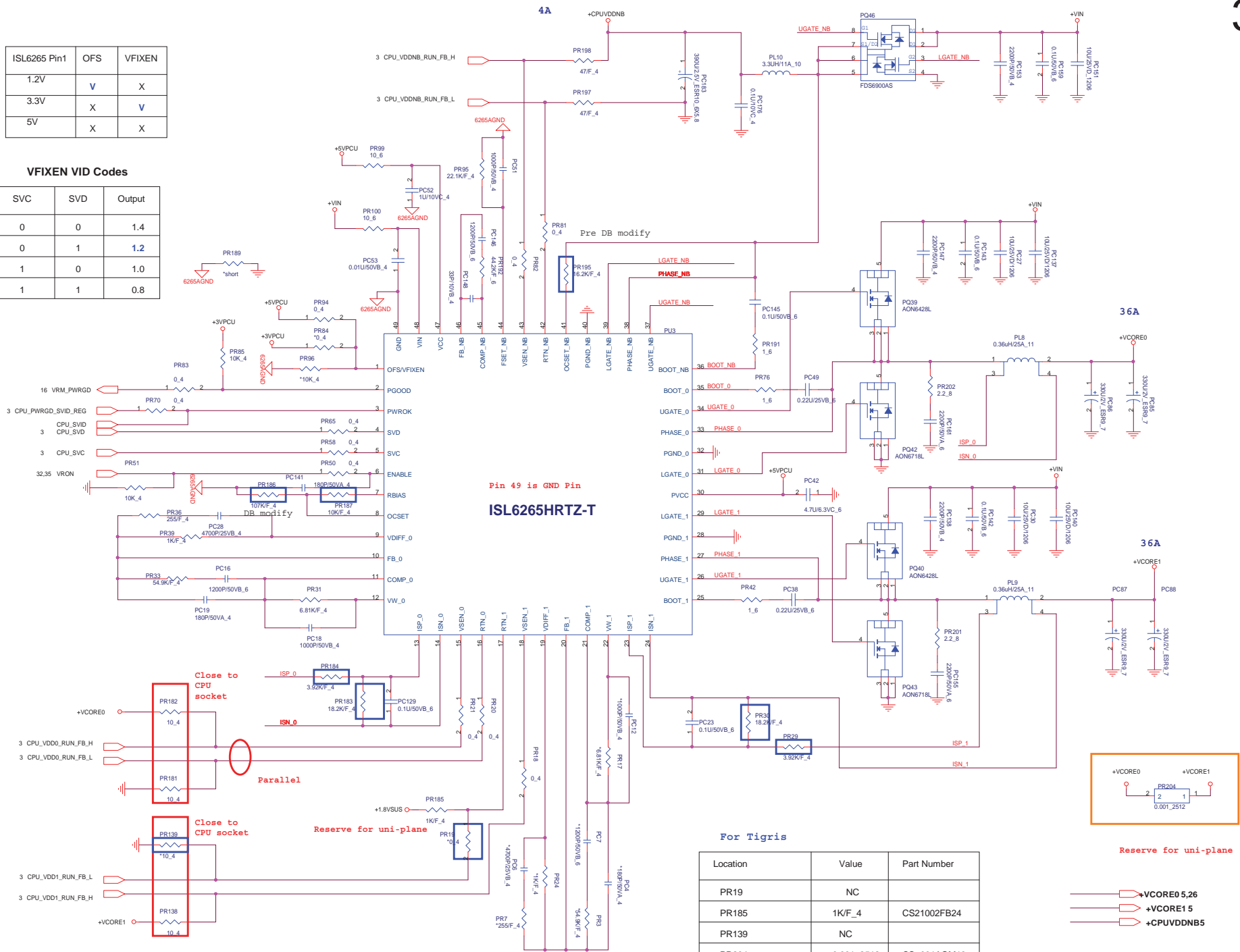
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Quanta Computer Inc.

Size B	Document Number +1.2V & +1.1V(RT8204)	Rev 1A
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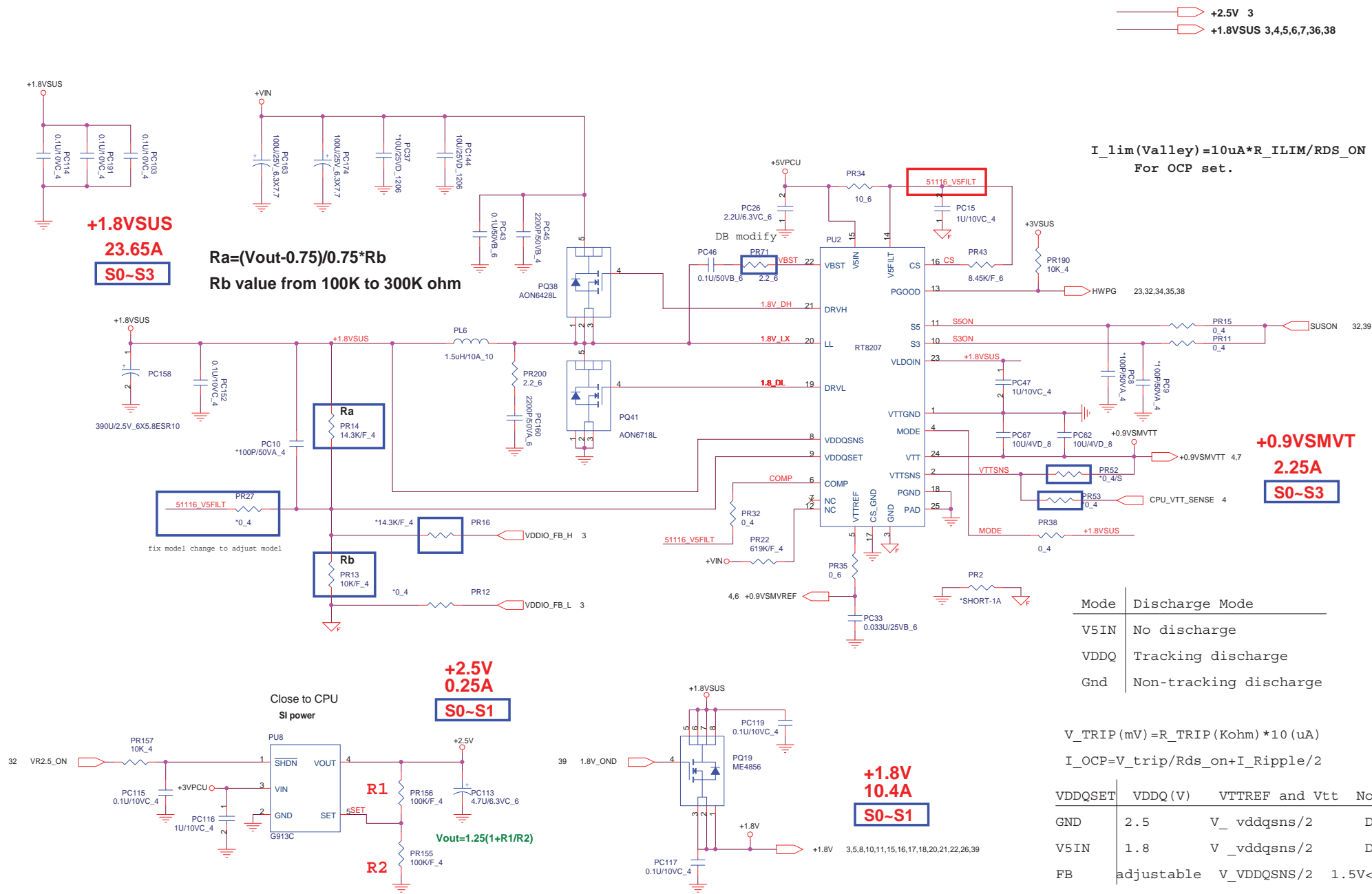
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



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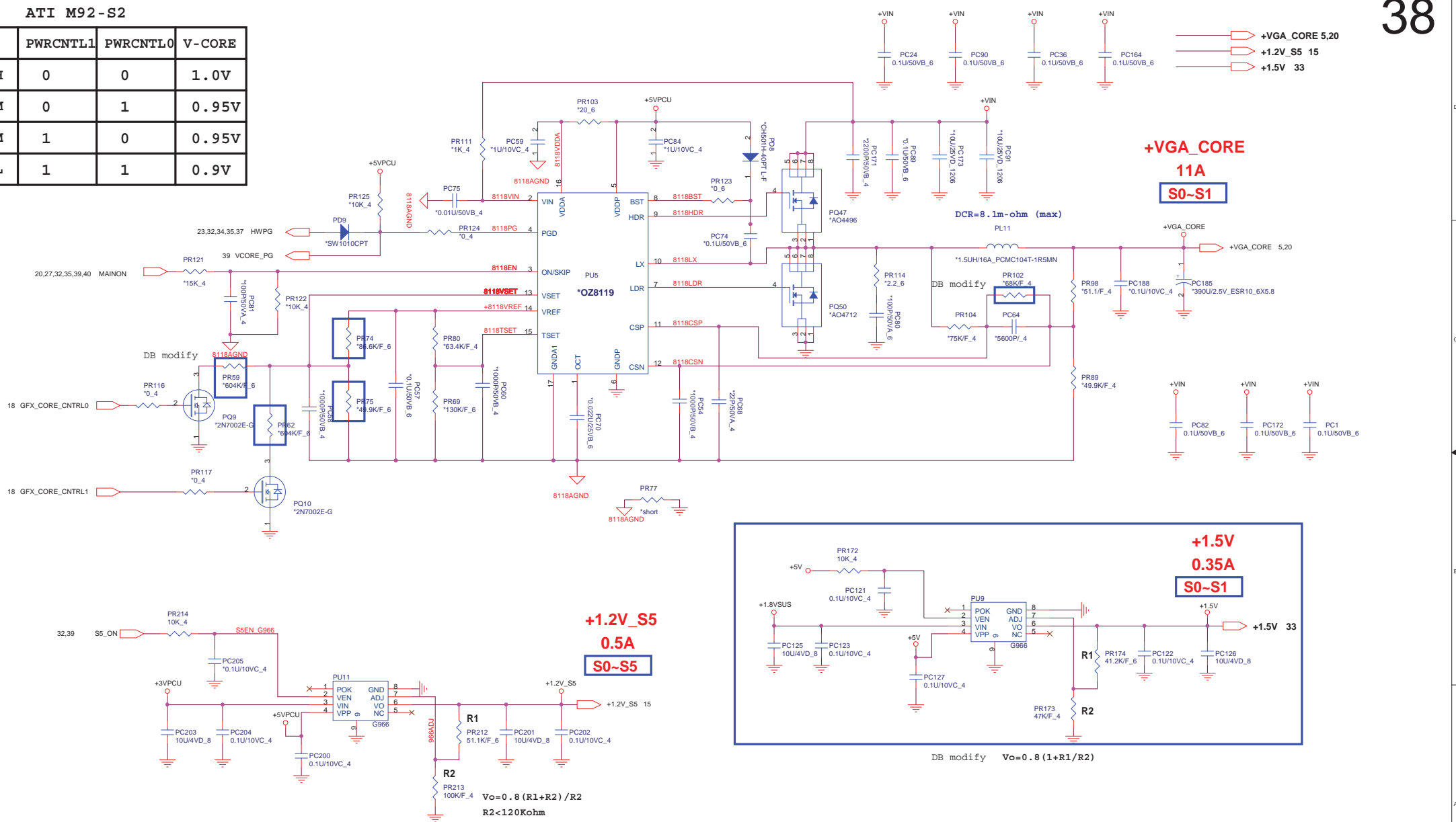


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Size Custom Document Number
1.8VSUS/DDR_VTER/+1.8V/2.5V Rev 1A
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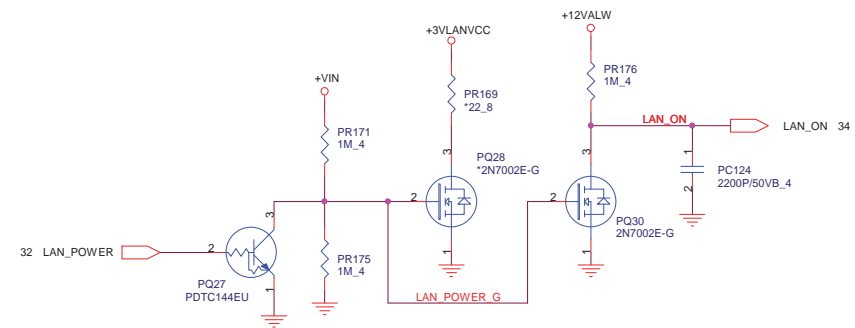
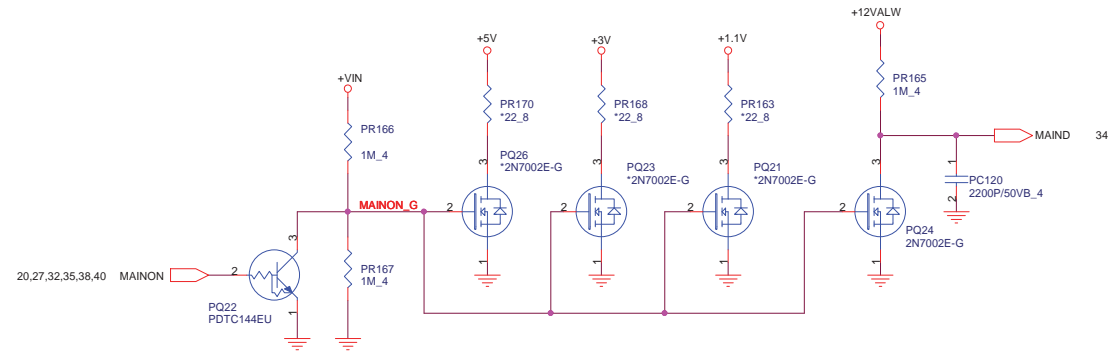
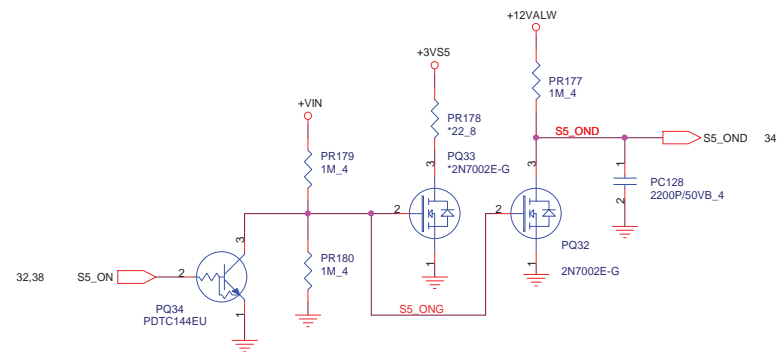
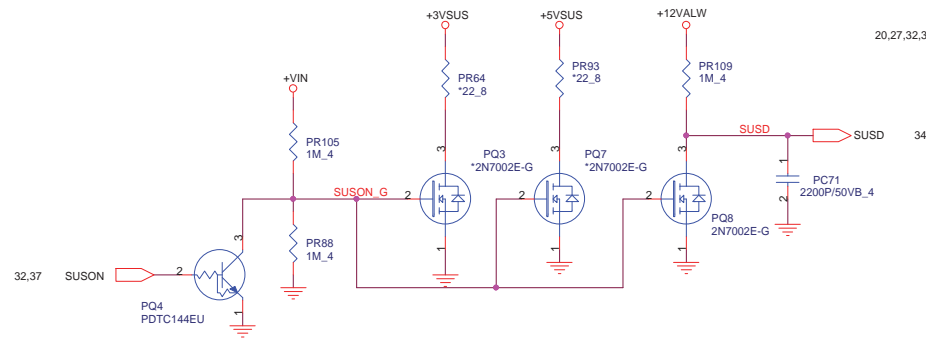
ATI M92-S2

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.0V
M	0	1	0.95V
M	1	0	0.95V
L	1	1	0.9V

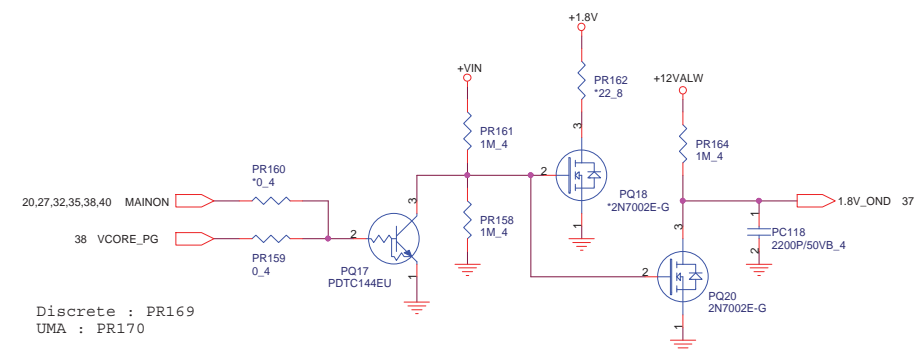


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Size Custom	Document Number VGA PWR OZ8118/1.2V_S5/+1.5	Rev 1A
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For Discrete Only



Discrete : PR169
UMA : PR170



NBS/RD2

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Size
Custom

Document Number
DISCHARGE

Rev
1A

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