First International Computer, Inc

Protable Computer Group HW Department

Board name : Mother Board Schematic

Project : KR2W_K8_ATI RS482M+SB450

Version : 0.1(ES)

Initial Date : 03.09.2005

Manager Sign by :

Drawing by : Audy Chou

Total confirm by :Adam Cho

LAN Circuit check by : Vivian Chen

Audio Circuit check by : Annie Wang

First International Computer, Inc.
3FL.,NO.300,Yang Guang St.,NeiHu
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Title	TITLE	
Size: C	Document Number: KR2W < AMD K8 + RS482M + SB450 >	Rev: 0.1
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1. Schematic Page Description :

KR2W Schematic Ver : 0.1

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD21	Mini PCI(Wireless LAN)
AD20	CardBus (CB1410)

PCIINT	CHIP
IRQA	VGA/LAN
IRQB	CardBus (CB1410)
IRQC	MiniPCI
IRQD	MiniPCI

BUSMASTER

REQ	CHIP
REQ0 / GNT0	Mini PCI(Wireless LAN)
REQ1 / GNT1	CardBus (CB1410)
REQ2 / GNT2	Mini PCI(Wireless LAN)
REQ3 / GNT3	——
REQ4 / GNT4	——

IRQ Channel	Desciption
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	Serial Port
IRQ5	AUDIO / VGA / USB
IRQ6	~~FLOPPY DISK~~
IRQ7	LPT
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	Cardbus
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	ECP
DMA2	~~FLOPPY DISK~~
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

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Title: Schematic Page Description

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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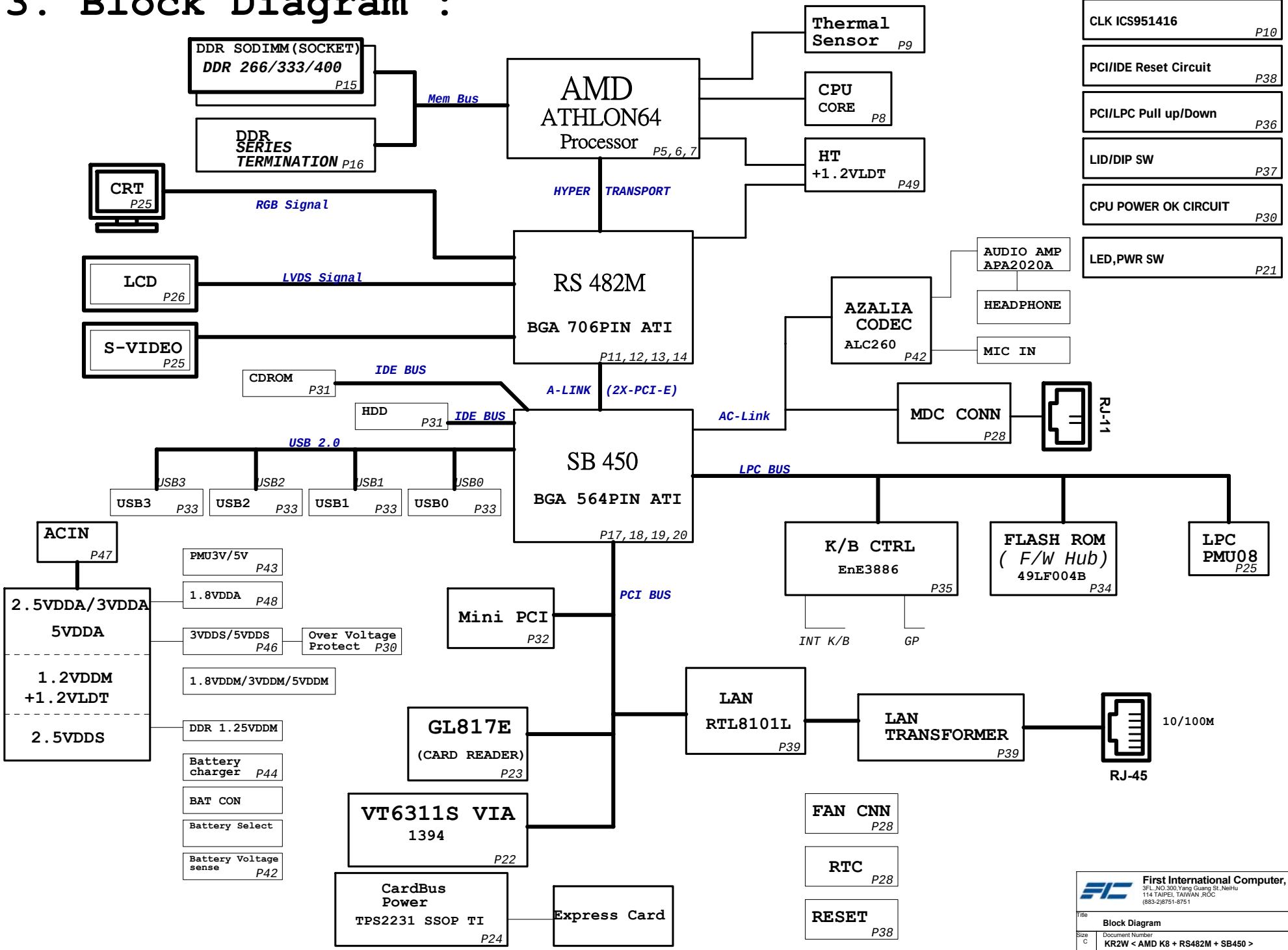
3. Block Diagram :



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Title: Block Diagram

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4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
2.5VDDA	2.5V always on power rail by DCON or PSUSC0
5VDDS	5.0V power rail
3VDDS	3.3V power rail
2.5VDDS	2.5V power rail
2.5VDDS_CPU	2.5V power rail for CPU&DDR
DDR_1.25VDDS	1.25V DDR Termination Voltage
12VDDM	12V switched power rail
5VDDM	5.0V switched power rail
3VDDM	3.3V switched power rail
2.5VDDM	2.5V switched power rail
1.5VDDM	1.5V power rail 0.8 ~ 1.55V
Vcore_CPU	Core Voltage for CPU
+1.2VLDT	VCC For CPU & NB Hyper Transport

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

0 = Active Low signal

Signal Conditioning

_D_ = Damped (by a resistor)
_Q_ = Isolated (by a Q-switch)
_L_ = Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1	TOP
Layer 2	GND
Layer 3	IN1/Mixer
Layer 4	IN2/Mixer
Layer 5	VCC
Layer 6	BOTTON

POWER RAIL	DESTINATION	VOLTAGE	S0 CURRENT
VCORE_CPU	K8	0.8~1.55V	42A
+1.2VLDT	K8	+1.2V	??A
2.5VCCA	K8 PLL	2.5V	??A
1.5VDDM	NB CORE & PLL	1.5V	??A
1.25VDDS	DDR RAM TERMINAL	1.25V	0.0769A
2.5VDDS_CPU	CPU & DDR RAM		1.046A (Idle) 1.692A (Run 3DMark)
2.5VDDM	SB CORE & USBPLL & MII LVDS	2.5V	??A
2.5VDDS	SB USB & MII (SUS)	2.5V	??A
2.5VDDA	SB WAKE UP (SUS)	2.5V	??A
		1.5V	0.0675A
3VDDM	NB VGA	3.3V	0.528A
	ENE 1410		0.13A
	MiniPCI		
	FWH BIOS		
	LPC KBC		0.0308A (Idle)
	AC97 CODEC		0.0461A (Idle)
	CLK GEN		0.36A
3VDDS	ENE 1410	3.3V	
	VT6103L		0.36A
	MiniPCI		
	PCMCIA VCCA		
3VDDA	SB (SUS)	3.3V	0.165A
5VDDM	AMP2020		0.0615A (Idle) 0.338A (Run)
	CDROM		0.0461A (Idle) 0.677~0.8A (Run)
	HDD		0.0461A (Idle) 0.492A (Run)
	INT KB/ INT MS		
	INVERTER		0.0615A (Idle) 0.569A (Run)
5VDDS	PCMCIA VCCA		
5VDDA	SWITCHING POWER VCC		10UA
PMU3V	PMU08		0.0615A
PMU5V	ASIC_C0		0.0615A

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Title: ANNOTATIONS
Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1
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ClawHammer HT Interface

200 mils

LAYOUT: Place HT bypass caps on topside near unconnected Clawhammer HT Link

LAYOUT: Route 2.5VCCA approx. 50mil wide and 500mils long.(Reference to ground)

LAYOUT: Route differentially with 10/10/5/10/10

LAYOUT: Route differentially with 20/8/5/8/20

FROM RS482M

TO RS482M

CN25A

FOXCONN_SOCKET754

CN25C

FOXCONN_SOCKET754

Close to SOCKET754

TO CLAWHAMMER < 1"

FROM CLOCK GEN

CPUCLK& CPUCLK0 Shall be placed as close to process <1".
For 5 mils Trace width for differential pair of CPUCLK.
CPUCLK& CPUCLK0 Shall 20 mils clearance to other.

Source from VLDT

AMD recommended(Item 1-23)

AMD recommended(Item 1-21)

0218 MODIFY

HT BUS General Routing Rules:

1. HT BUS is easy to route,and uses minmal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 2700 mils(max).
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.

SIGNAL / WSPAC=15mil / CADIN_H, CADIN_L / WDP=5mil / 5mil

SIGNAL / WSPAC=15mil / CADOUT_H, CADOUT_L / WDP=5mil / 5mil

SIGNAL / WSPAC=15mil / H_CLKIP/H_CTLIP, H_CLKIN/H_CTLIN / WDP=5mil / 5mil

SIGNAL / WSPAC=15mil / H_CLKOP/H_CTLOP, H_CLKON/H_CTLON / WDP=5mil / 5mil

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Title: K8_Claw Hammer (1/3)

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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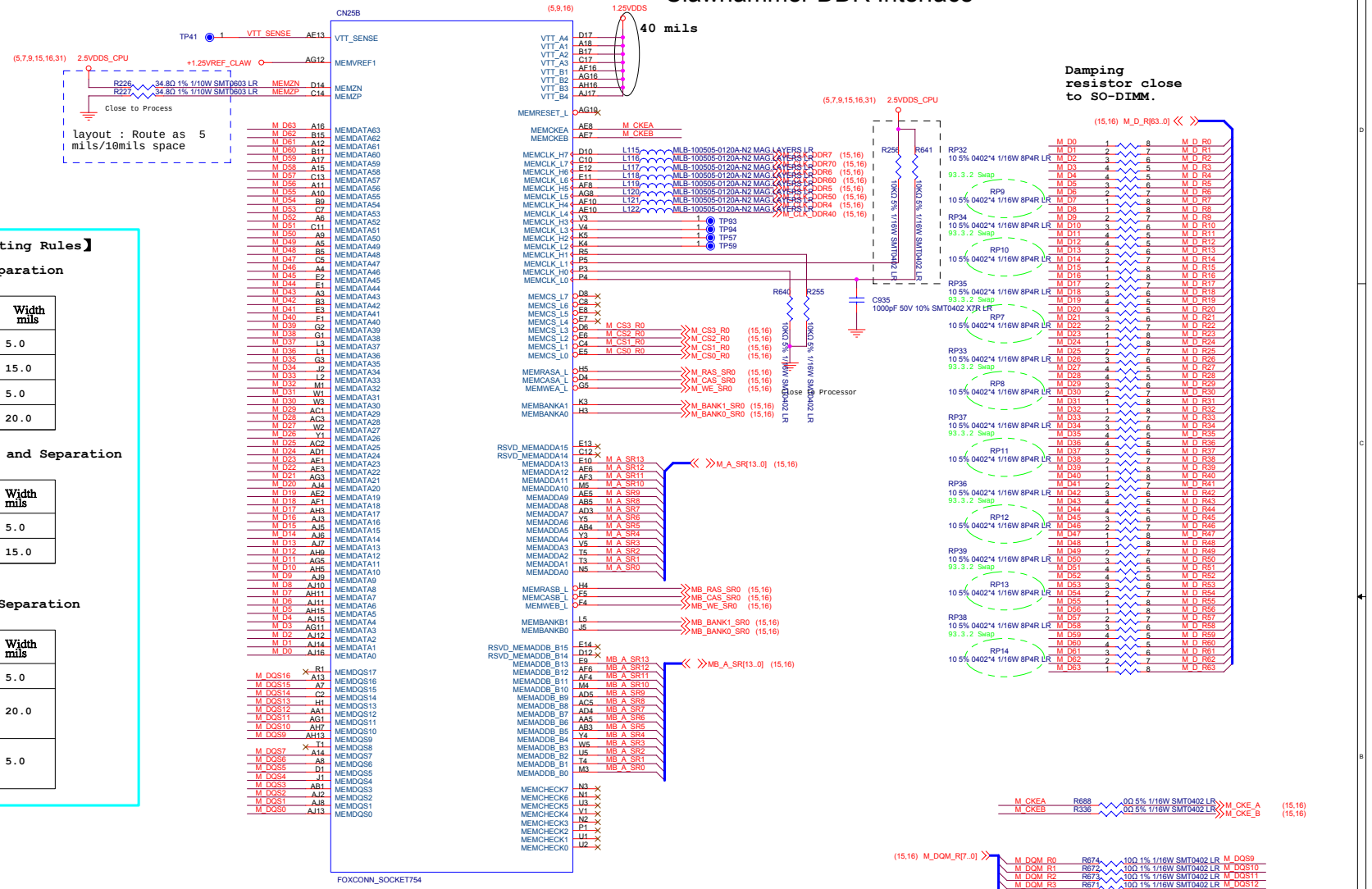
LAYOUT: Place on the bottom of the board.

Clawhammer DDR Interface



【DDR Memory General Routing Rules】

Data Bus Trace Width and Separation (Refer to Vss)

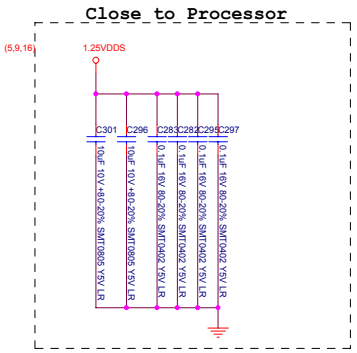
Parameter	Definition	Width mils
WDQ	MEMDQ/MEMDM Width	5.0
WDQ-space	MEMDQ/MEMDM Spacing	15.0
WDQS	MEMDQS Width	5.0
WDQA-space	MEMDQS Spacing	20.0

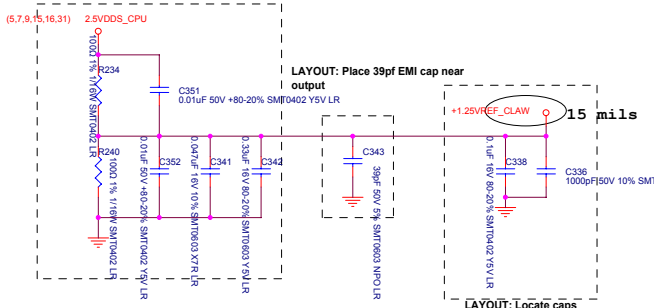
Address/Command Trace Width and Separation (Refer to Vdd)

Parameter	Definition	Width mils
WADD	Address/Command Width	5.0
WADD-space	Address/Command Space	15.0

MEMCLK H/L Trace Width and Separation (Refer to Vdd)

Parameter	Definition	Width mils
WCK	MEMCLK Width	5.0
WCK-space	MEMCLK Spacing for non matched differential pairs	20.0
WDP-space	MEMCLK Spacing for differential pairs	5.0





LAYOUT: Place on the bottom of the board.

Company	First International Computer, Inc.
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Phone	(883-2)8751-8751
Title	K8_Claw Hammer (2/3)
Size	C
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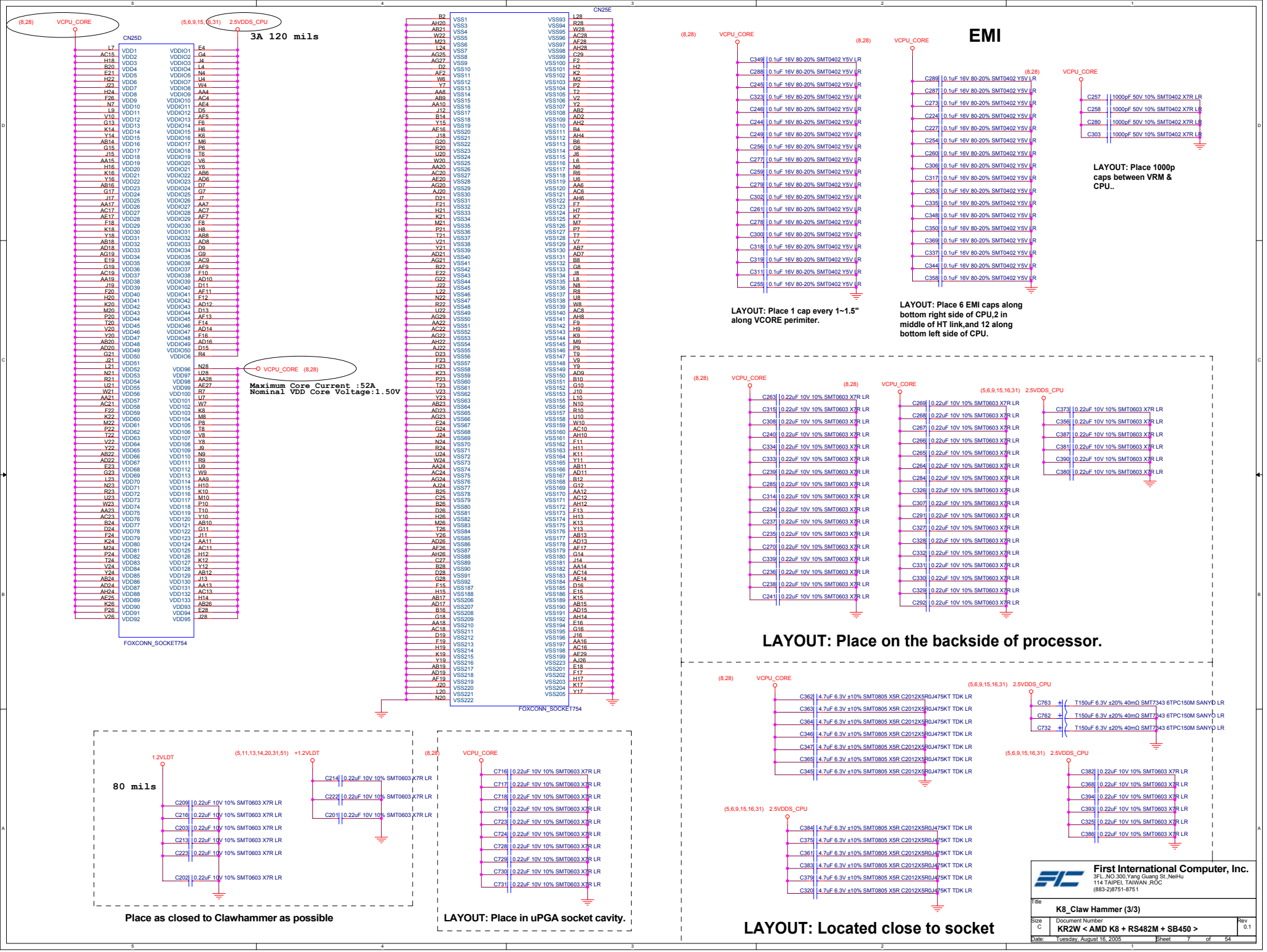
(8,28)
VCPU_CORE
(5,6,9,15,16,31)
2.5VDDS_CPU
3A 120 mils
CN25D
FOXCONN_SOCKET754
Maximum Core Current :52A
Nominal VDD Core Voltage:1.50V
CN25E
FOXCONN_SOCKET754
EMI
LAYOUT: Place 1 cap every 1~1.5" along VCORE perimiter.
LAYOUT: Place 6 EMI caps along bottom right side of CPU,2 in middle of HT link,and 12 along bottom left side of CPU.
LAYOUT: Place 1000p caps between VRM & CPU..
LAYOUT: Place on the backside of processor.
80 mils
1.2VLDT
(5,11,13,14,20,31,51)
+1.2VLDT
Place as closed to Clawhammer as possible
LAYOUT: Place in uPGA socket cavity.
LAYOUT: Located close to socket
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Title
K8_Claw Hammer (3/3)
Size C
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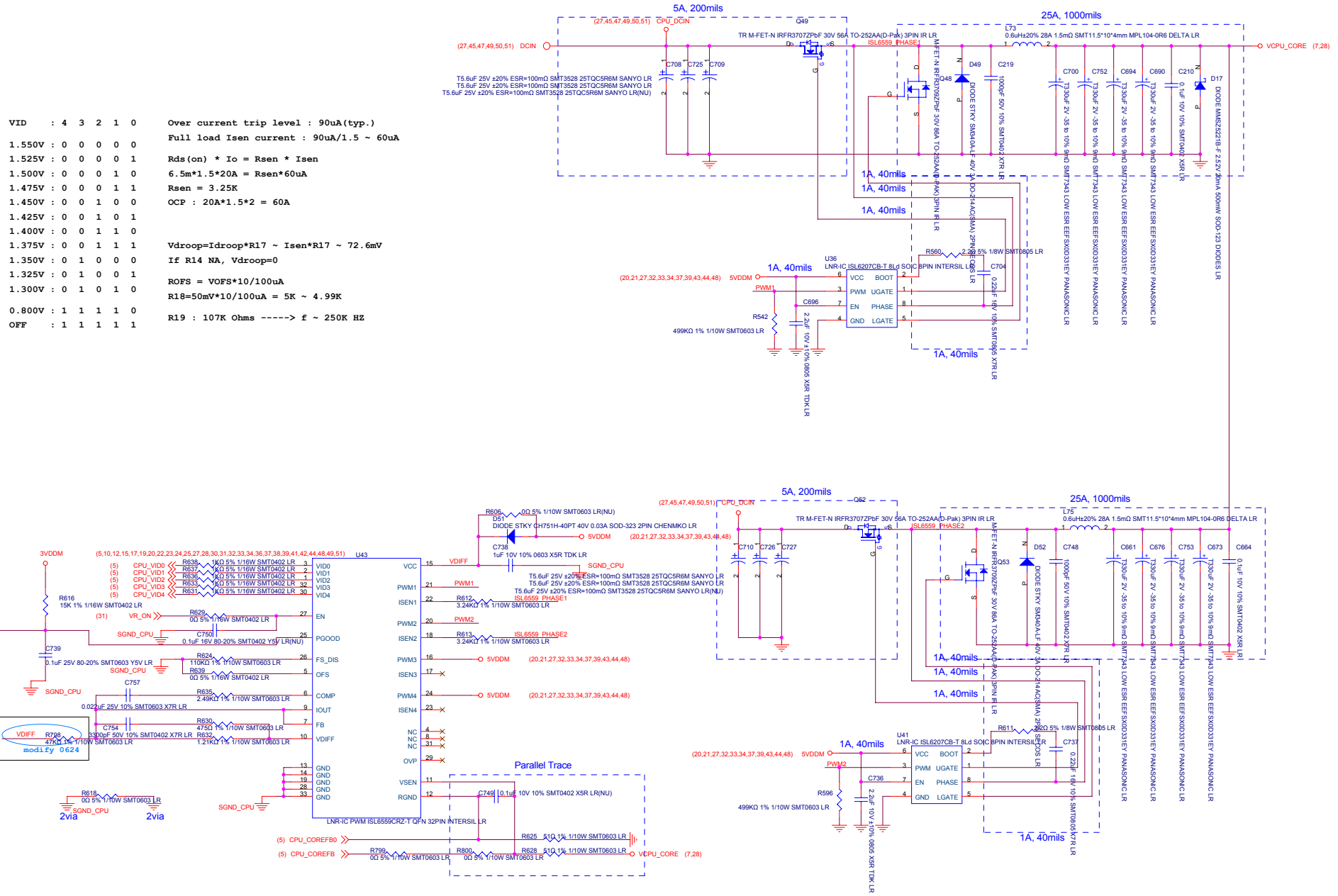
VID : 4 3 2 1 0
1.550V : 0 0 0 0 0
1.525V : 0 0 0 0 1
1.500V : 0 0 0 1 0
1.475V : 0 0 0 1 1
1.450V : 0 0 1 0 0
1.425V : 0 0 1 0 1
1.400V : 0 0 1 1 0
1.375V : 0 0 1 1 1
1.350V : 0 1 0 0 0
1.325V : 0 1 0 0 1
1.300V : 0 1 0 1 0
0.800V : 1 1 1 1 0
OFF : 1 1 1 1 1
Over current trip level : 90uA(typ.)
Full load Isen current : 90uA/1.5 ~ 60uA
Rds(on) * Io = Rsen * Isen
6.5m*1.5*20A = Rsen*60uA
Rsen = 3.25K
OCP : 20A*1.5*2 = 60A
Vdroop=Idroop*R17 ~ Isen*R17 ~ 72.6mV
If R14 NA, Vdroop=0
ROFS = VOFS*10/100uA
R18=50mV*10/100uA = 5K ~ 4.99K
R19 : 107K Ohms -----> f ~ 250K HZ
5A, 200mils
25A, 1000mils
1A, 40mils
CPU_DCIN
DCIN
VCPU_CORE
ISL6559_PHASE1
ISL6559_PHASE2
TR M-FET-N IRFR3707ZPbF 30V 56A TO-252AA(D-Pak) 3PIN IR LR
M-FET-N IRFR3702PbF 30V 86A TO-252AA(D-PAK) 3PIN IR LR
DIODE STKY SM340A-LF 40V 3A DO-214AC(SMA) 2PIN CHENMKO LR
DIODE MMSZ5221B-F 2.52V 20mA 500mW SOD-123 DIODES LR
T5.6uF 25V ±20% ESR=100mΩ SMT3528 25TQC5R6M SANYO LR
T5.6uF 25V ±20% ESR=100mΩ SMT3528 25TQC5R6M SANYO LR(NU)
T330uF 2V -35 to 10% 9mΩ SMT7343 LOW ESR EEFSX0331EY PANASONIC LR
0.1uF 10V 10% SMT0402 X5R LR
0.22uF 16V 10% SMT0805 X7R LR
2.2uF 10V 10% 0805 X5R TDK LR
499KΩ 1% 1/10W SMT0603 LR
U36
U41
LNR-IC ISL6207CB-T 8Ld SOIC 8PIN INTERSIL LR
VCC
BOOT
PWM
UGATE
EN
PHASE
GND
LGATE
5VDDM
PWM1
PWM2
U43
LNR-IC PWM ISL6559CRZ-T QFN 32PIN INTERSIL LR
VID0
VID1
VID2
VID3
VID4
PGOOD
FS_DIS
OFS
COMP
IOUT
FB
VDIFF
ISEN1
ISEN2
ISEN3
ISEN4
OVP
VSEN
RGND
Parallel Trace
modify 0624
2via
SGND_CPU
3VDDM
PM_VGATE
VR_ON
CPU_COREFB0
CPU_COREFB
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Title
CPU V-CORE (25W)
Size C
Document Number
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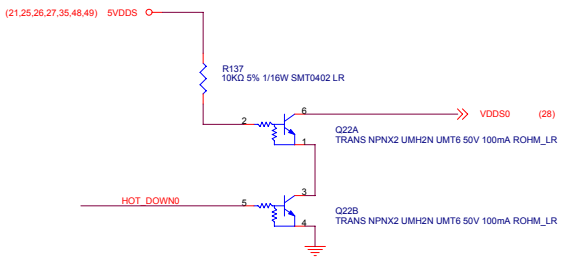
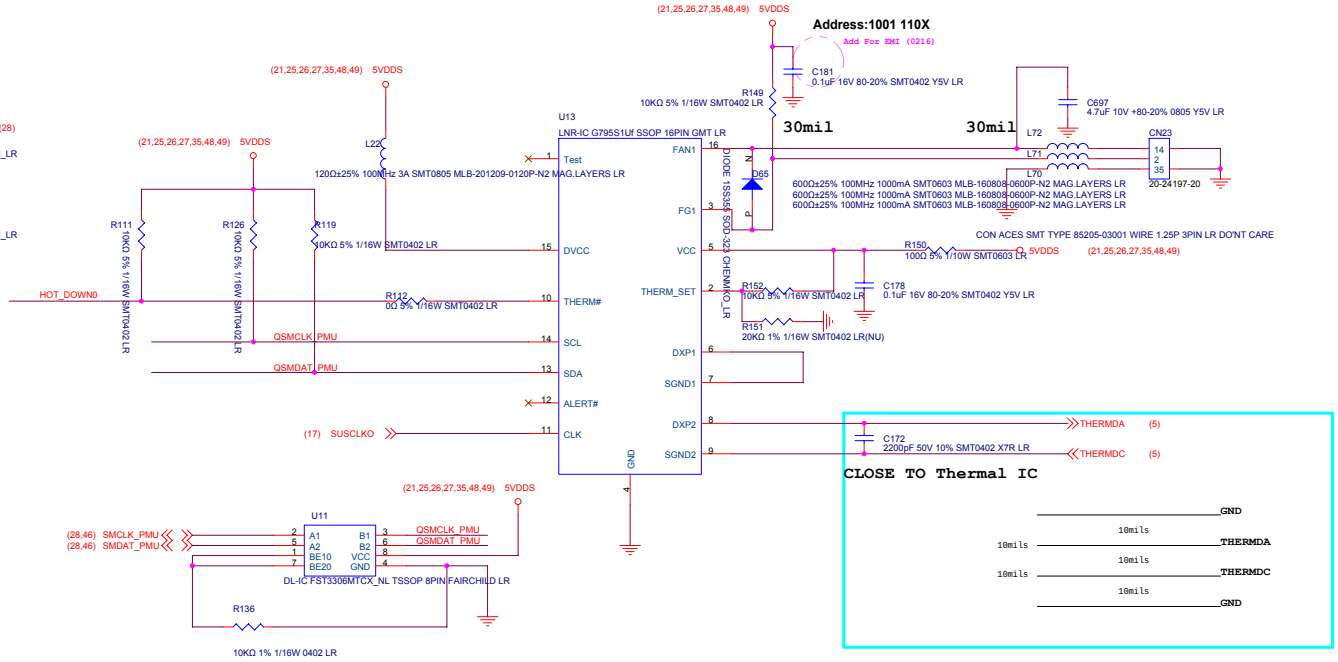
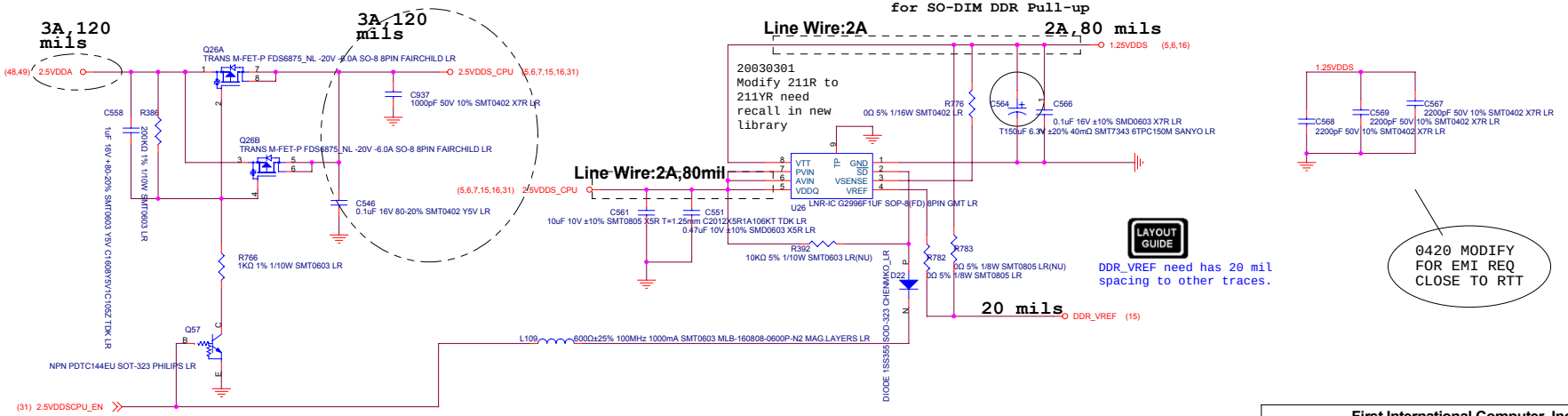
SYSTEM POWER OVP



THERMAL SENSOR/FAN



DDR VTT 1.25V



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Title: Thermal / DRAM POWER

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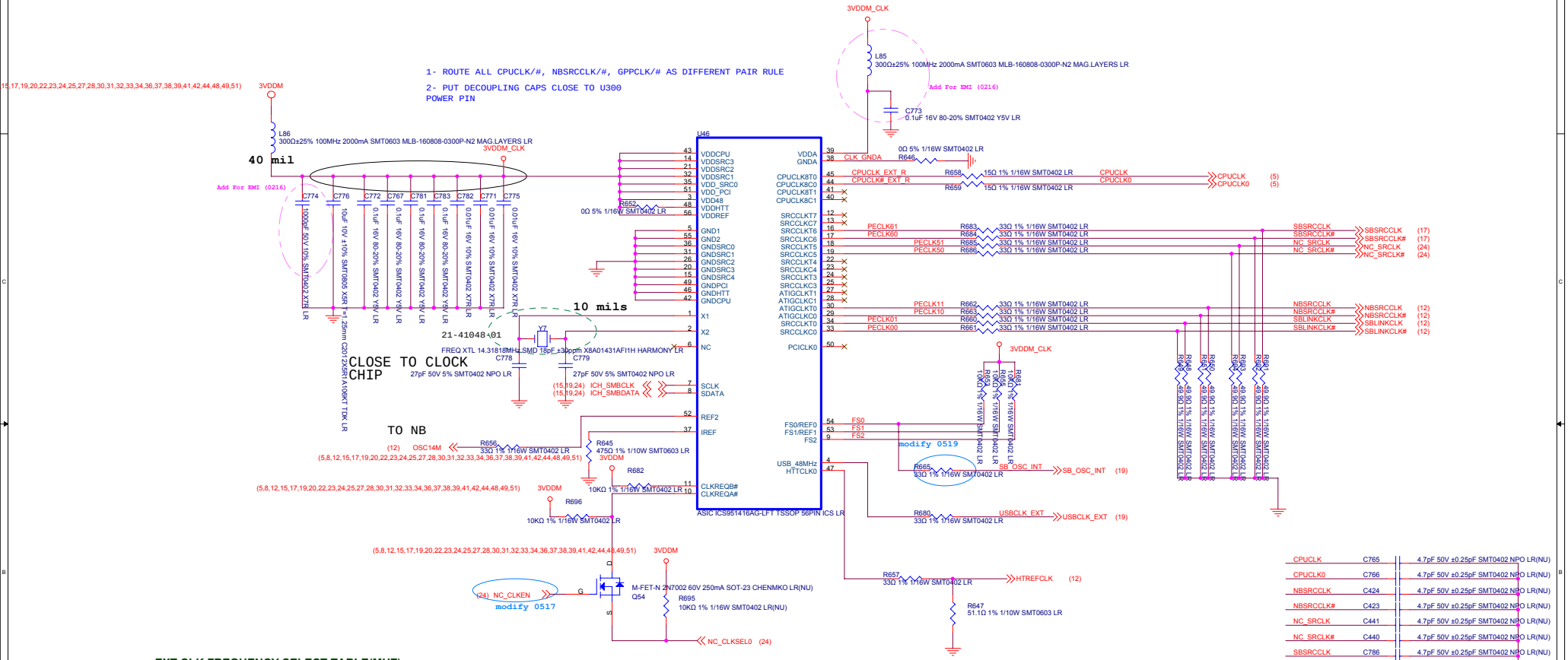

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

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Title: CLOCK GEN (ICS951412)

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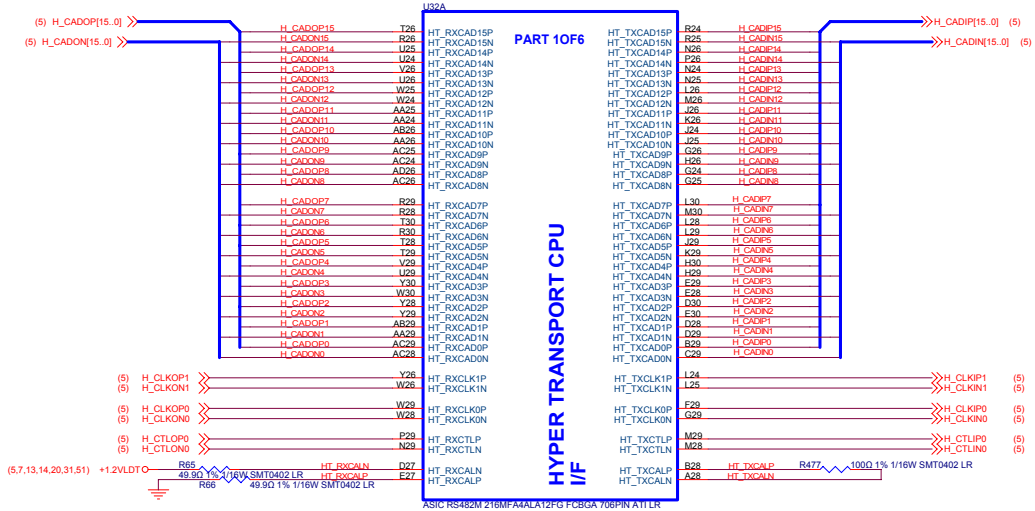

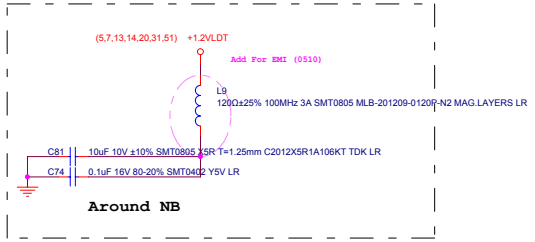

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Title: RS482M Host (1/4)

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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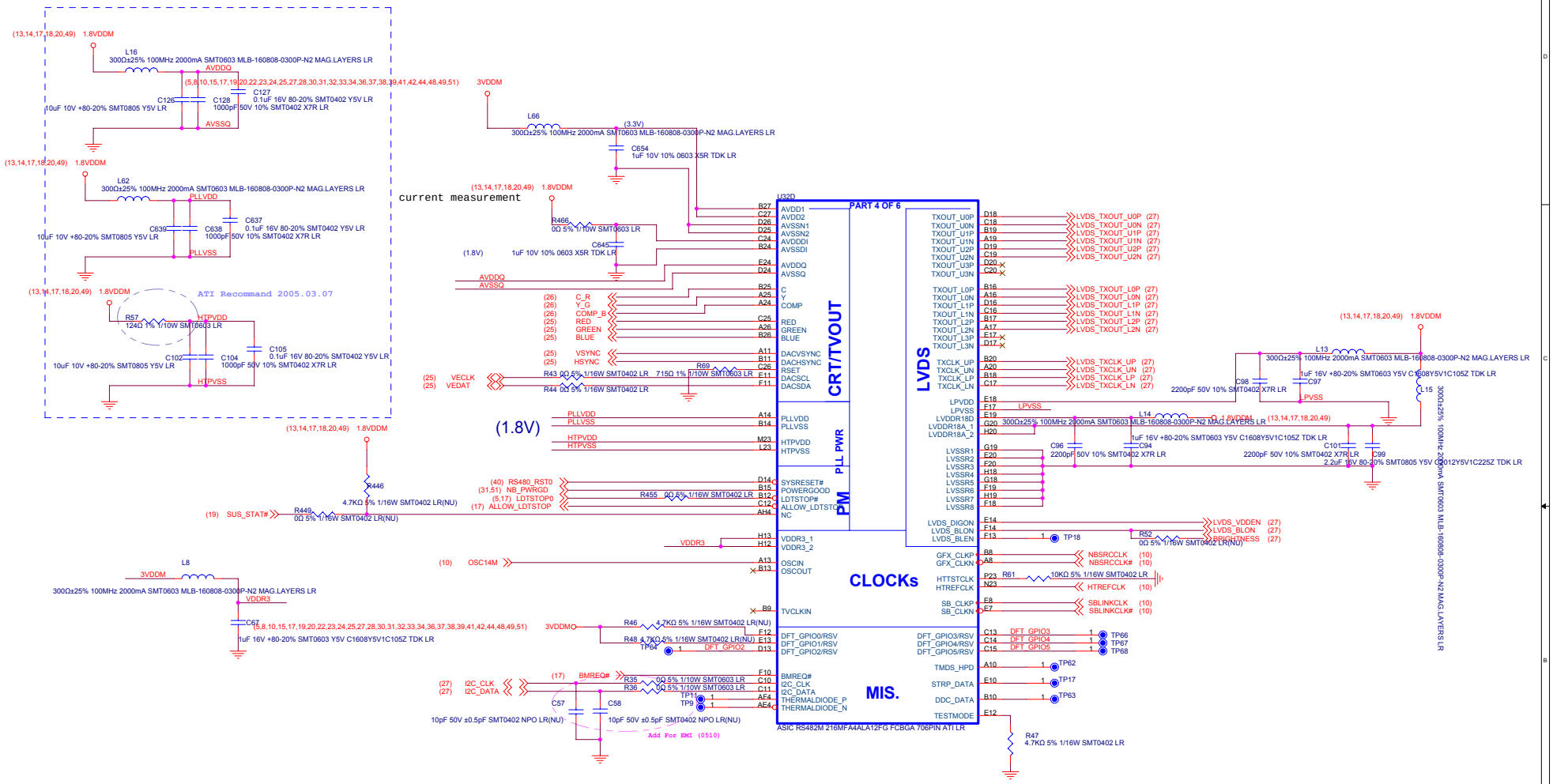

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Title	RS482MPCI(E)/AGP (2/4)		
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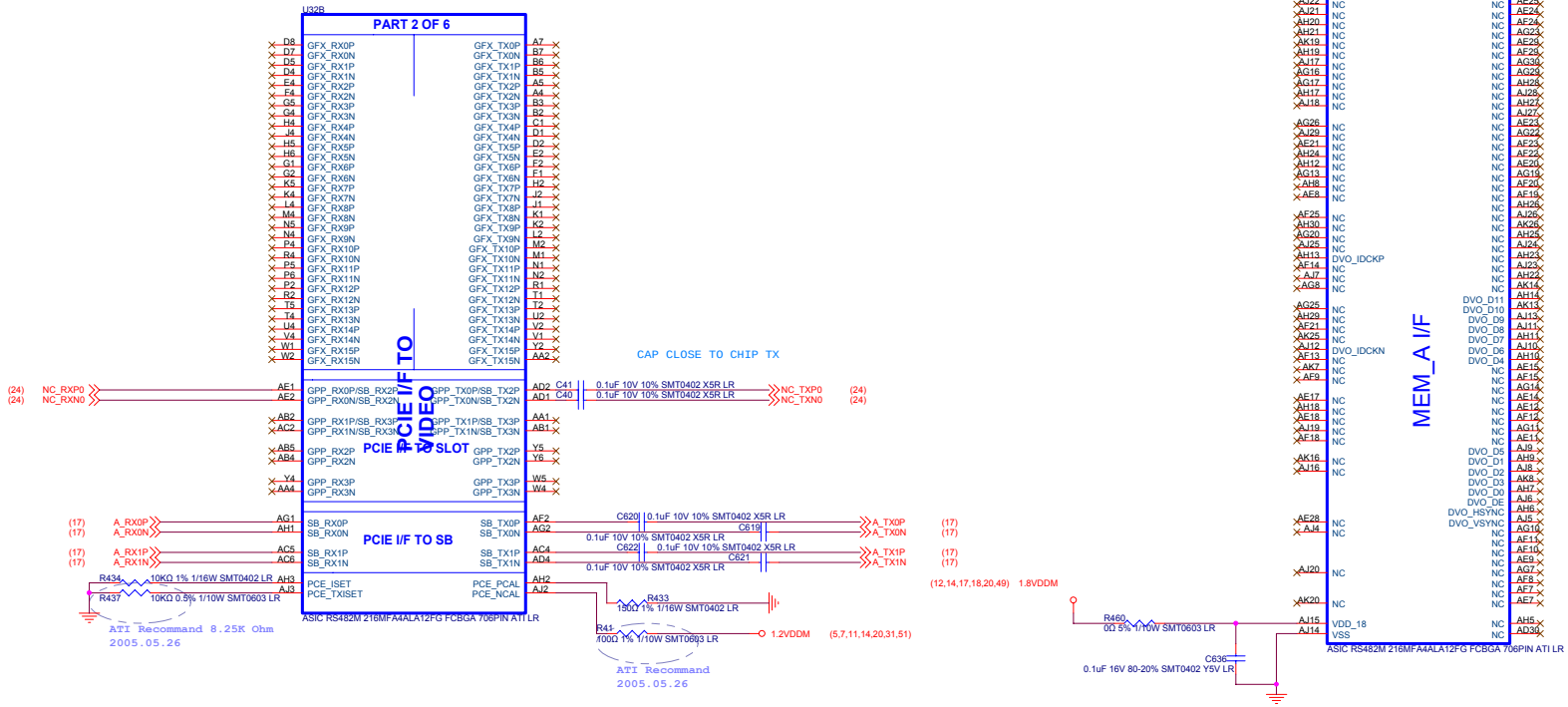

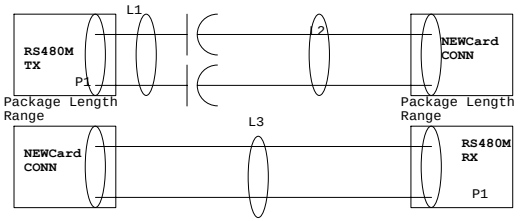

L1	L2	L3	Cap
Min 0.25" Max 14.75"	Max 14.75" - L1	Min 0.25" Max 15"	75nF ~200nF +/-20% 0402 or 0603

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Title: **RS482M A-LINK (3/4)**

Size	Document Number	Rev
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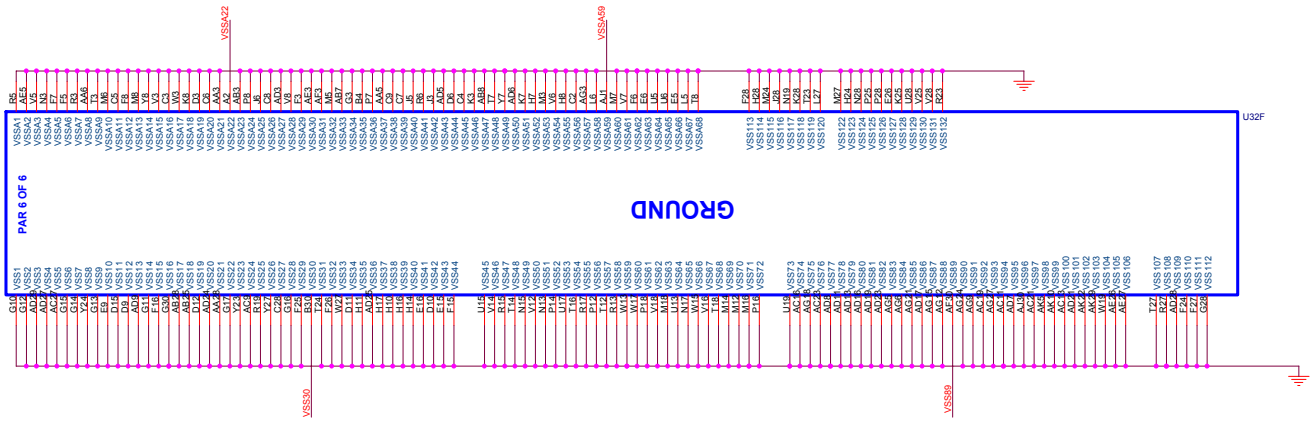
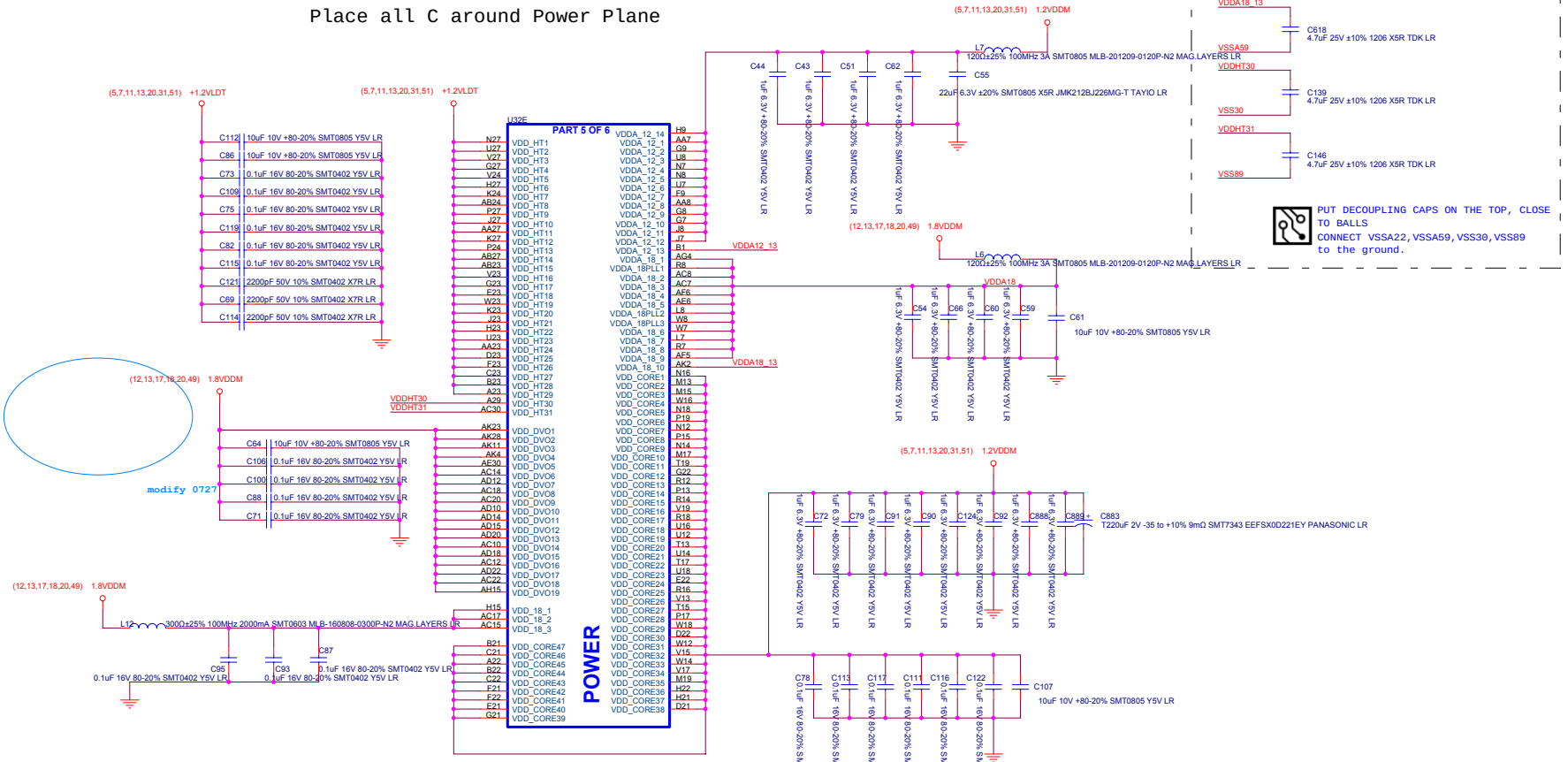
NB RS480 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR, VDDRCK	ON	ON	ON	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



Place all C around Power Plane



Place all C around Power Plane

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Title: **RS482M POWER&GRAND(4/4)**

Size	Document Number	Rev
C	KR2W < AMD K8 + RS482M + SB450 >	0.1

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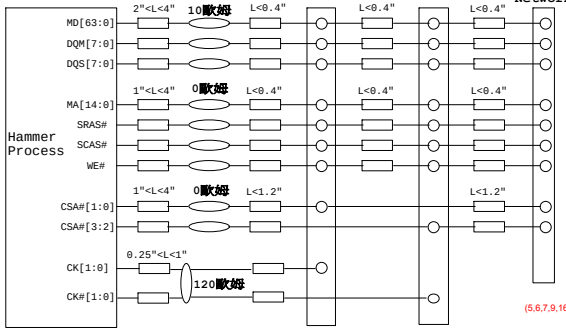
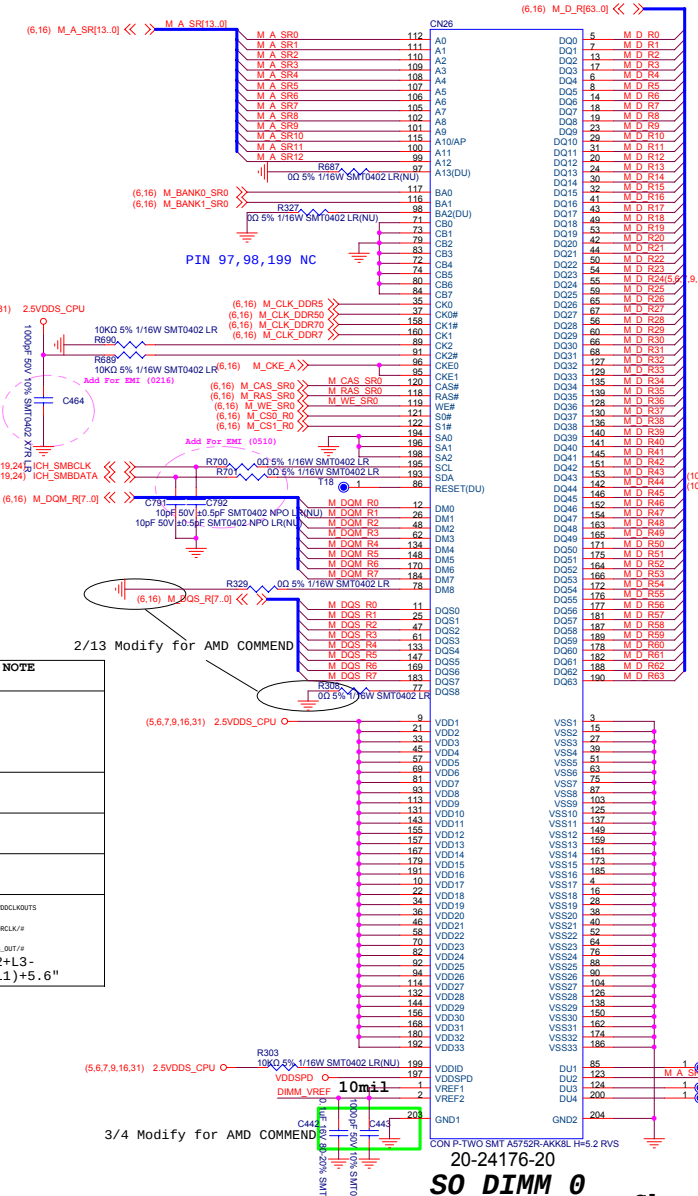
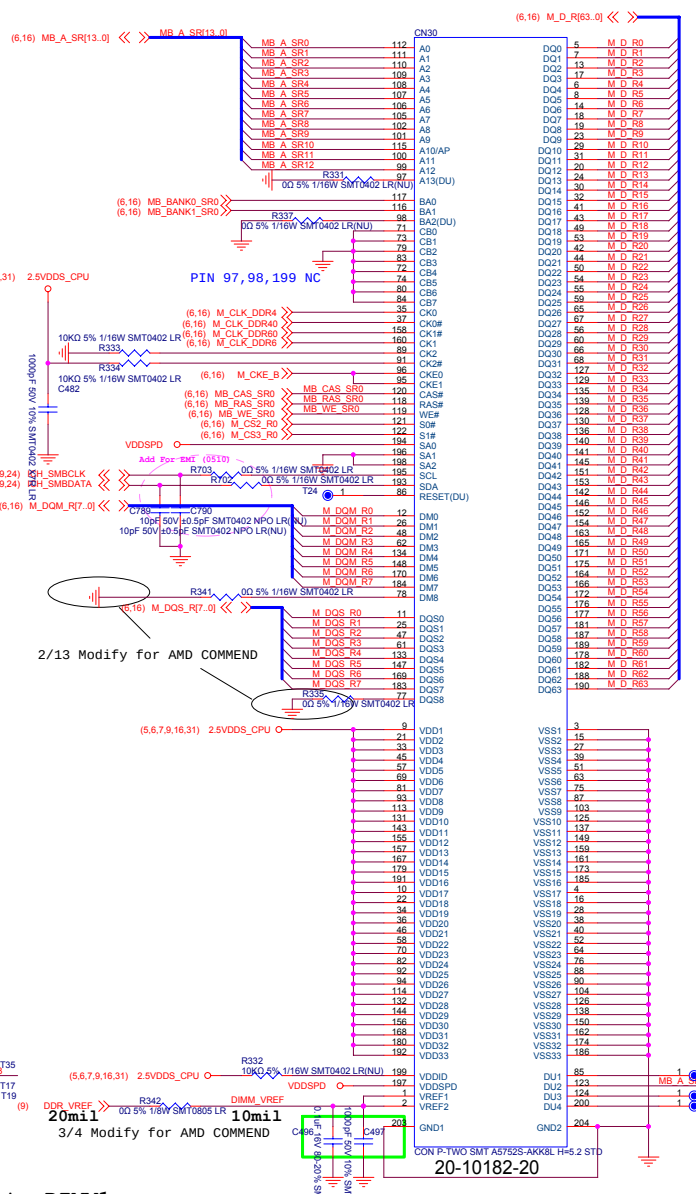
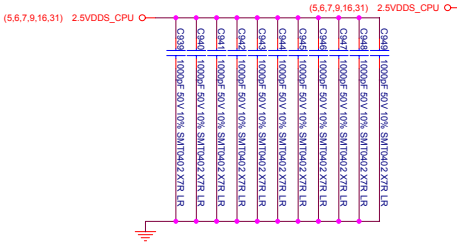


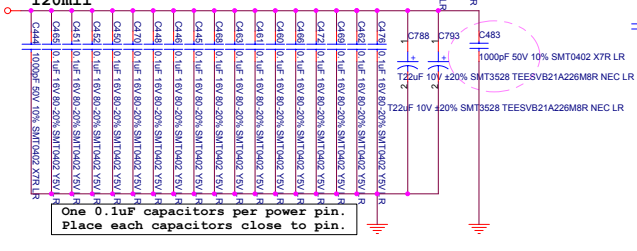
SIGNAL GROUP	DATA SIGNALS	STROBE SIGNALS	Length Mismatch
MD Group 0	MD[7:0],DQM0	DQS0	±25mils
MD Group 1	MD[15:8],DQM1	DQS1	±25mils
MD Group 2	MD[23:16],DQM2	DQS2	±25mils
MD Group 3	MD[31:24],DQM3	DQS3	±25mils
MD Group 4	MD[39:32],DQM4	DQS4	±25mils
MD Group 5	MD[47:40],DQM5	DQS5	±25mils
MD Group 6	MD[55:48],DQM6	DQS6	±25mils
MD Group 7	MD[63:56],DQM7	DQS7	±25mils
MA(& Control)	MA[14:0],CAS#,RAS#,WE#		
CS(Chip Select)	CSA#[5:0]		
CKE	CKE[5:0]		
Clocks	FWDSDCLKOUT,DDRCLK[8:0]/DDRCLK#[8:0] ,FB_OUT/FB_OUT#		

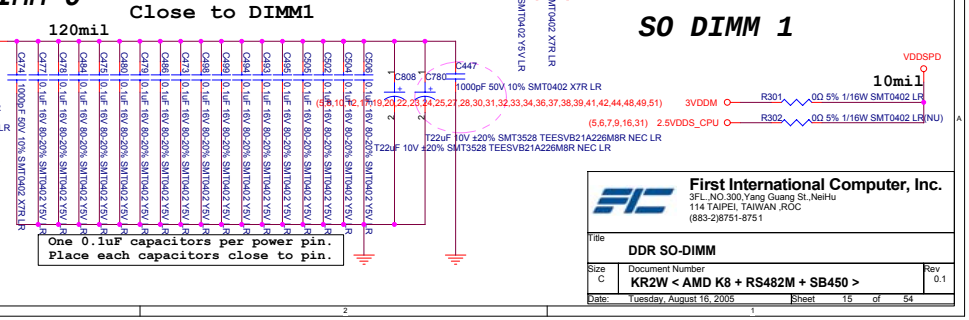
SIGNAL GROUP	WIDTH:SPACE	TRACE LENGTH	TRACE LENGTH MATCHING	NOTE
MD Group[7:0]	1:3 Data:Strobe 1:3 Data:Other 1:4 M_DQS:Other	1"<L1<3.5" L1+L2=1.5~5.0" (Avg~3")	<100mil mismatch within group. <2 inch mismatch between group.	
MA(& Control)	1:3 MA:MA 1:3 MA:Other	1"<L<4"		
CS(Chip Select)	1:3 CS:Other	1"<L<4"		
CKE	1:3 CKE:Other	14"<Lcke1<20" Lcke2<2"		
Clocks	1:1 CLK:CLK# 1:3 CLK#:Other	L2~6" L3~4" L4~12"		L2=$L_{FWDCLKOUTS}$ L3=$L_{DDRCLK/\#}$ L4=$L_{FB\_OUT/\#}$ L4=L2+L3-Avg(L1)+5.6"











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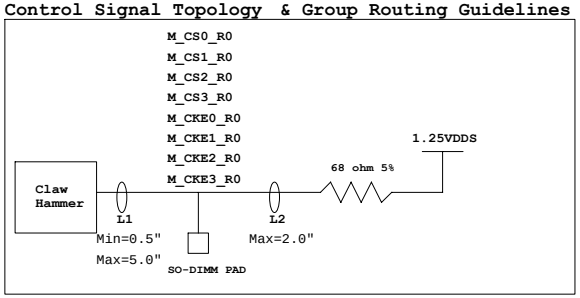
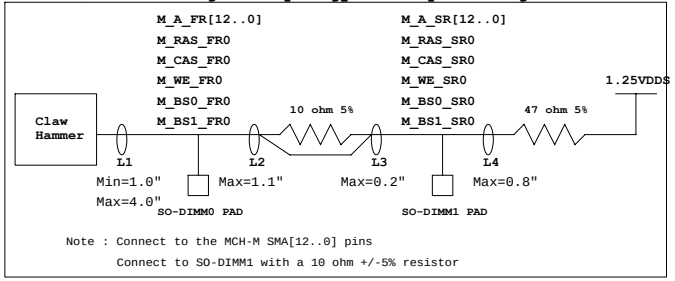
Title	DDR SO-DIMM	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 15 of 54	

Control Signal Topology & Group Routing Guidelines

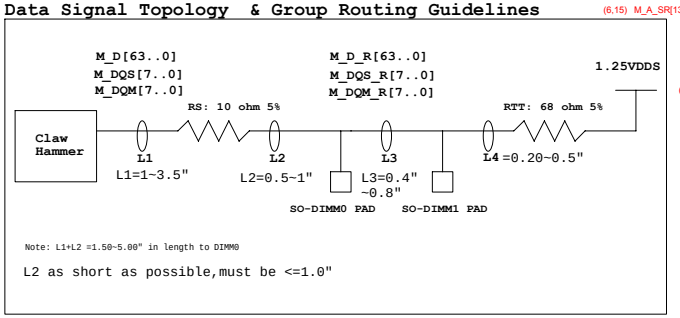


Address/Command Signal Topology & Group Routing Guidelines



Note : Connect to the MCH-M SMA[12..0] pins
Connect to SO-DIMM1 with a 10 ohm +/-5% resistor

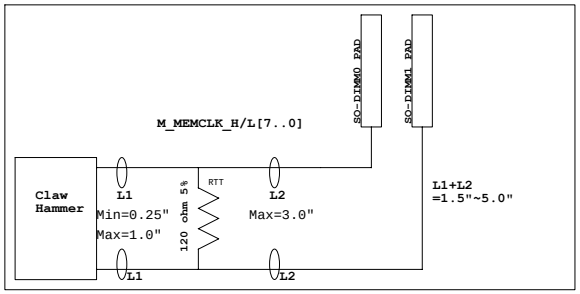
Data Signal Topology & Group Routing Guidelines

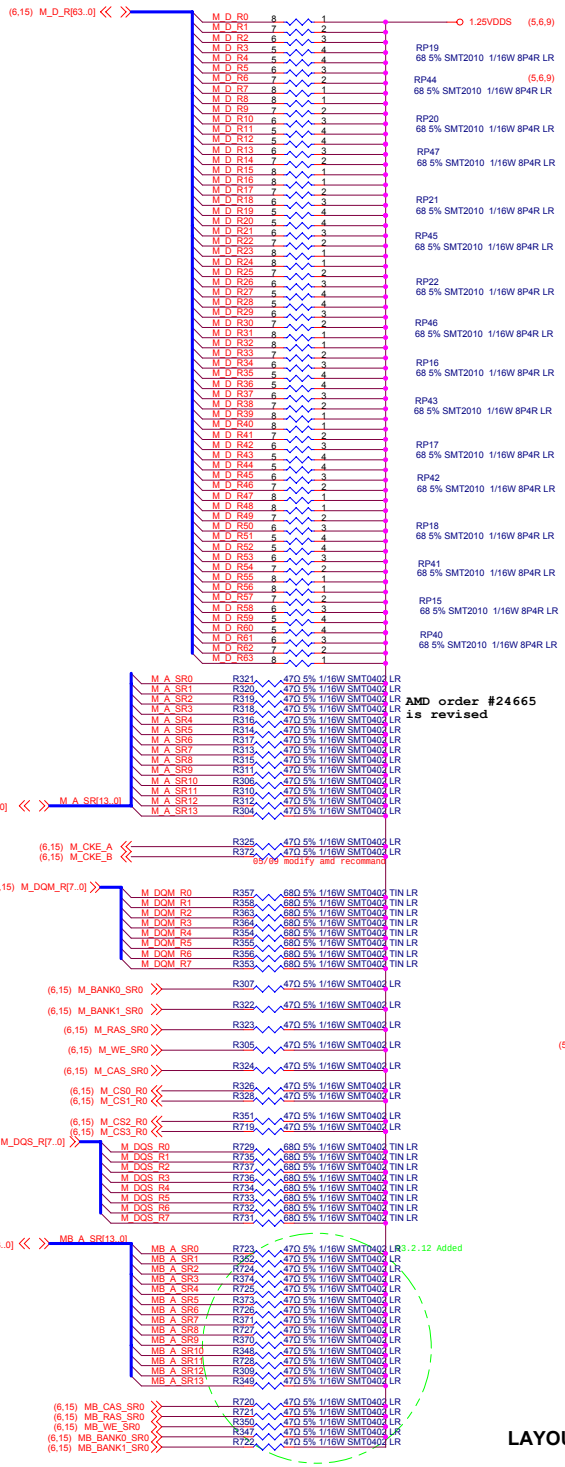


Note: L1+L2 =1.50~5.00" in length to DIMM0

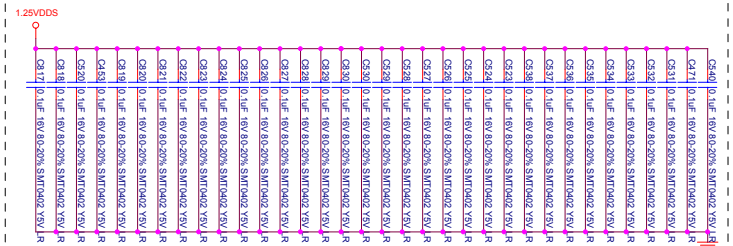
L2 as short as possible,must be <=1.0"

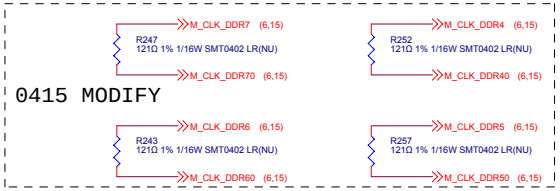
MEMCLK_H/L[7..0] & Group Routing Guidelines

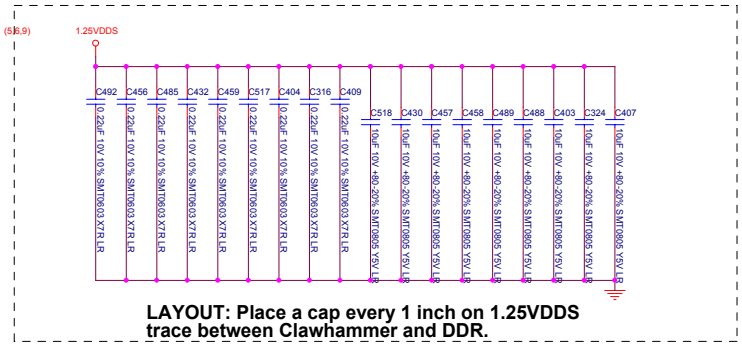




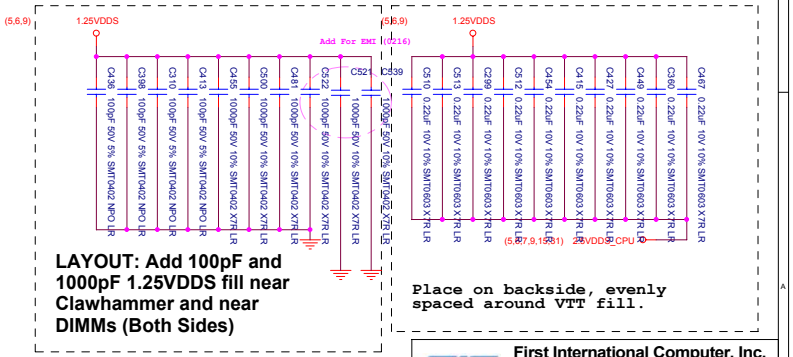
LAYOUT: Place alternating caps to GND and +2.5VDDS in a single line along 1.25VDDS island.







LAYOUT: Place a cap every 1 inch on 1.25VDDS trace between Clawhammer and DDR.



LAYOUT: Add 100pF and 1000pF 1.25VDDS fill near Clawhammer and near DIMMs (Both Sides)

Place on backside, evenly spaced around VTT fill.

LAYOUT: RTT 120 Ω near to process.
Min=0.25" Max= 1.0"

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Title	DDR PULL UP	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 16 of 54	

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB)
SHOULD BE AS SHORT AS POSSIBLE

SB450 SB
Part 1 of 4

ASIC IXP450 SB450 218S4PASAT2G BGA 564PIN ATI LR

STRAP CLK2~8

STRAP

STRAP

ACPWRON

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz XTAL MODE DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USE INT. PLL48 DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz OSC MODE	USB PHY PWRDOWN ENABLE	USE EXT. 48MHz	14MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM DEFAULT L,L = FWH ROM

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Title: SB450 PCI(E)/LPC (1/4)

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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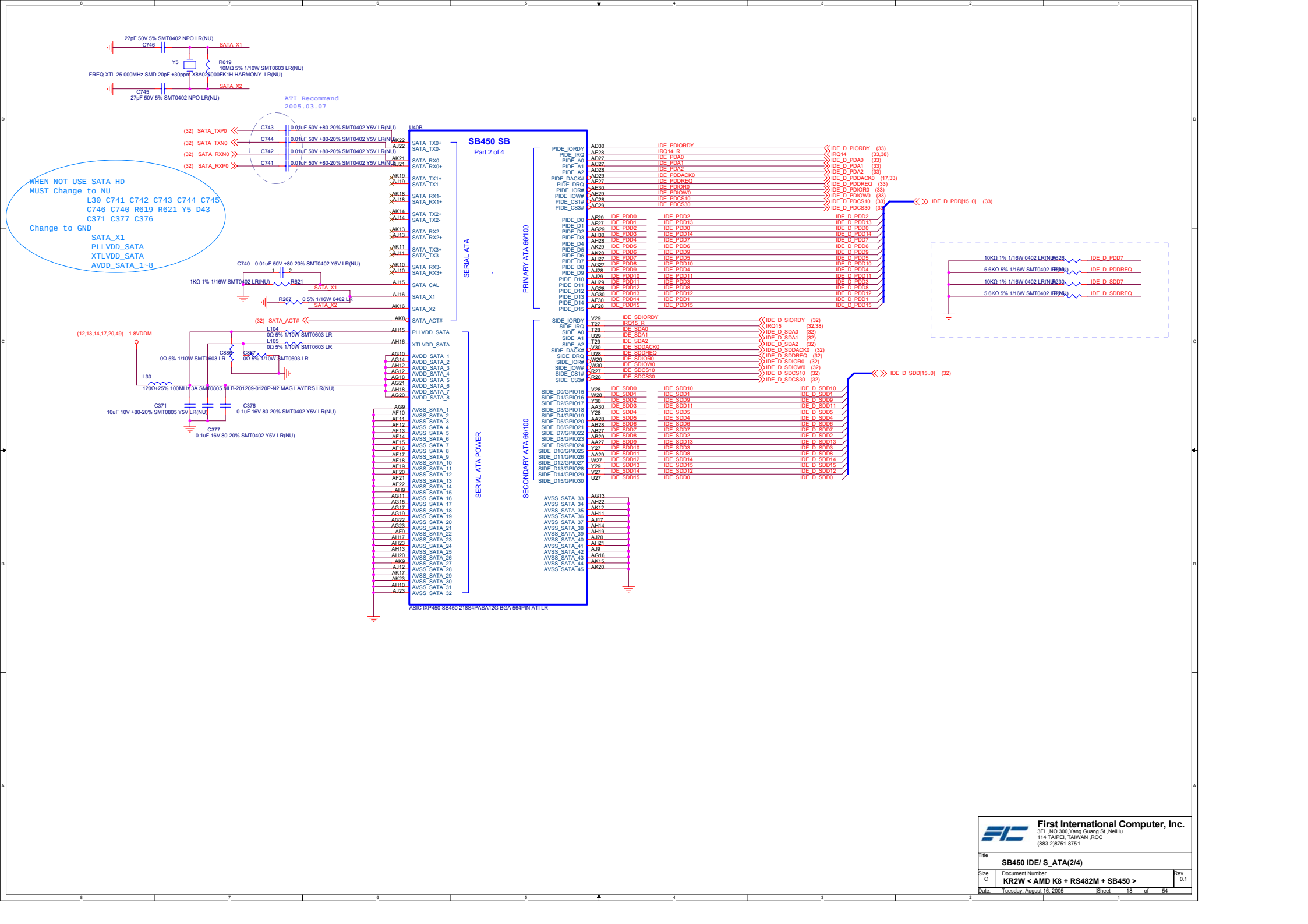
27pF 50V 5% SMT0402 NPO LR(NU)
C746
SATA_X1
Y5
R619
10MΩ 5% 1/10W SMT0603 LR(NU)
FREQ XTL 25.000MHz SMD 20pF ±30ppm X8A025000FK1H HARMONY_LR(NU)
SATA_X2
C745
27pF 50V 5% SMT0402 NPO LR(NU)
ATI Recommand
2005.03.07
WHEN NOT USE SATA HD
MUST Change to NU
L30 C741 C742 C743 C744 C745
C746 C740 R619 R621 Y5 D43
C371 C377 C376
Change to GND
SATA_X1
PLLVDD_SATA
XTLVDD_SATA
AVDD_SATA_1~8
U40B
SB450 SB
Part 2 of 4
SERIAL ATA
PRIMARY ATA 66/100
SECONDARY ATA 66/100
SERIAL ATA POWER
ASIC IXP450 SB450 218S4PASA12G BGA 564PIN ATI LR
IDE_D_PDD[15..0] (33)
IDE_D_SDD[15..0] (32)
10KΩ 1% 1/16W 0402 LR(NU)
5.6KΩ 5% 1/16W SMT0402 LR(NU)
10KΩ 1% 1/16W 0402 LR(NU)
5.6KΩ 5% 1/16W SMT0402 LR(NU)
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Title
SB450 IDE/ S_ATA(2/4)
Size C
Document Number
KR2W < AMD K8 + RS482M + SB450 >
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Date: Tuesday, August 16, 2005
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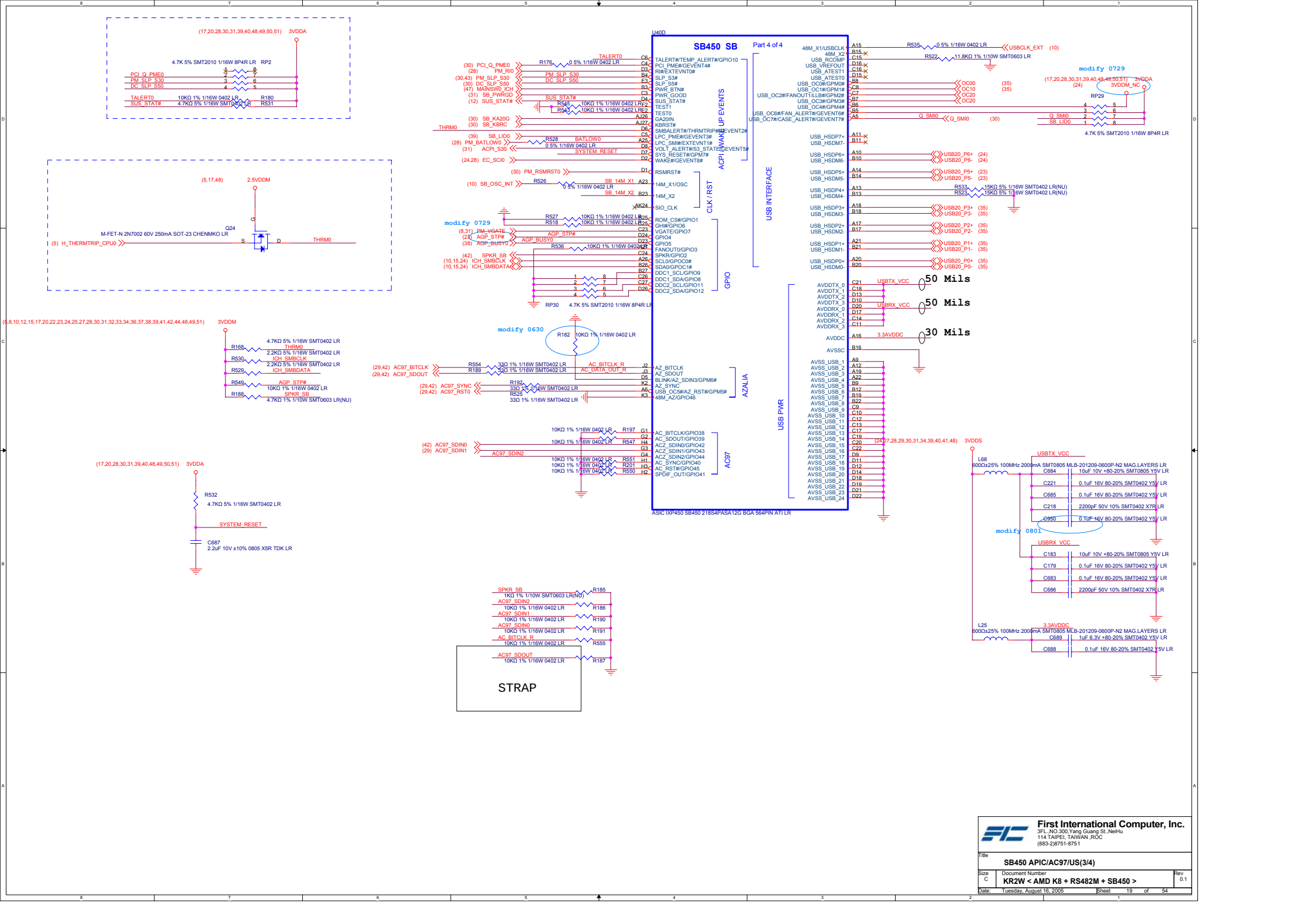
SB450 SB
Part 4 of 4
U40D
ASIC IXP450 SB450 218S4PASA12G BGA 564PIN ATI LR
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
AZALIA
AC97
USB INTERFACE
USB PWR
modify 0729
modify 0630
modify 0801
4.7K 5% SMT2010 1/16W 8P4R LR
RP30
RP29
M-FET-N 2N7002 60V 250mA SOT-23 CHENMKO LR
STRAP
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SB450 APIC/AC97/US(3/4)
KR2W < AMD K8 + RS482M + SB450 >
Tuesday, August 16, 2005
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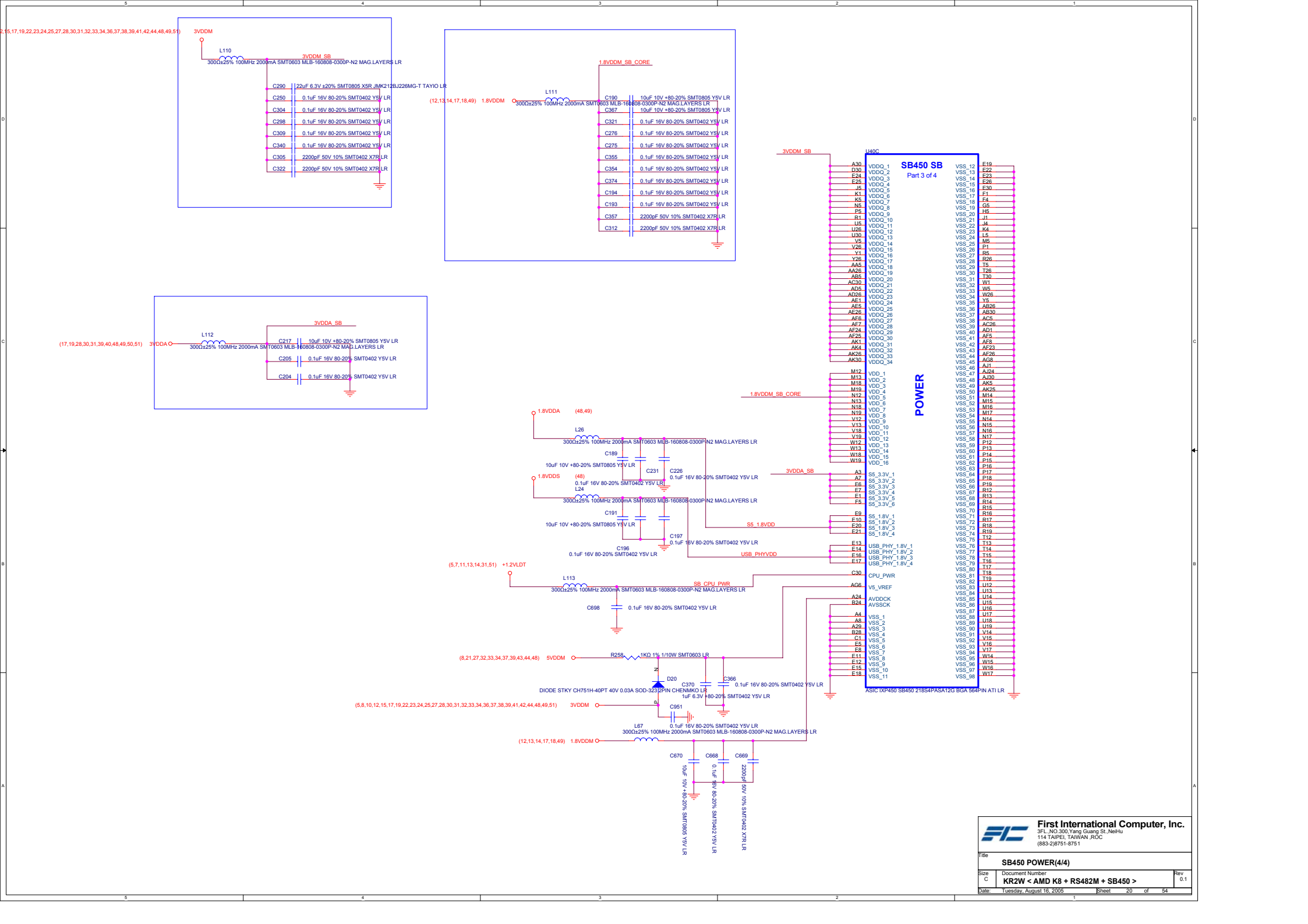
3VDDM
L110
3VDDM_SB
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
C290 22uF 6.3V ±20% SMT0805 X5R JMK212BJ226MG-T TAYIO LR
C250 0.1uF 16V 80-20% SMT0402 Y5V LR
C304 0.1uF 16V 80-20% SMT0402 Y5V LR
C298 0.1uF 16V 80-20% SMT0402 Y5V LR
C309 0.1uF 16V 80-20% SMT0402 Y5V LR
C340 0.1uF 16V 80-20% SMT0402 Y5V LR
C305 2200pF 50V 10% SMT0402 X7R LR
C322 2200pF 50V 10% SMT0402 X7R LR
1.8VDDM_SB_CORE
L111
(12,13,14,17,18,49) 1.8VDDM
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
C190 10uF 10V +80-20% SMT0805 Y5V LR
C367 10uF 10V +80-20% SMT0805 Y5V LR
C321 0.1uF 16V 80-20% SMT0402 Y5V LR
C276 0.1uF 16V 80-20% SMT0402 Y5V LR
C275 0.1uF 16V 80-20% SMT0402 Y5V LR
C355 0.1uF 16V 80-20% SMT0402 Y5V LR
C354 0.1uF 16V 80-20% SMT0402 Y5V LR
C374 0.1uF 16V 80-20% SMT0402 Y5V LR
C194 0.1uF 16V 80-20% SMT0402 Y5V LR
C193 0.1uF 16V 80-20% SMT0402 Y5V LR
C357 2200pF 50V 10% SMT0402 X7R LR
C312 2200pF 50V 10% SMT0402 X7R LR
3VDDM_SB
U40C
SB450 SB
Part 3 of 4
POWER
ASIC IXP450 SB450 218S4PASA12G BGA 564PIN ATI LR
L112
(17,19,28,30,31,39,40,48,49,50,51) 3VDDA
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
C217 10uF 10V +80-20% SMT0805 Y5V LR
C205 0.1uF 16V 80-20% SMT0402 Y5V LR
C204 0.1uF 16V 80-20% SMT0402 Y5V LR
1.8VDDA (48,49)
L26
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
C189
10uF 10V +80-20% SMT0805 Y5V LR
C231
C226 0.1uF 16V 80-20% SMT0402 Y5V LR
1.8VDDS (48)
0.1uF 16V 80-20% SMT0402 Y5V LR
L24
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
C191
10uF 10V +80-20% SMT0805 Y5V LR
C197 0.1uF 16V 80-20% SMT0402 Y5V LR
C196 0.1uF 16V 80-20% SMT0402 Y5V LR
S5_1.8VDD
USB_PHYVDD
(5,7,11,13,14,31,51) +1.2VLDT
L113
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
SB_CPU_PWR
C698 0.1uF 16V 80-20% SMT0402 Y5V LR
(8,21,27,32,33,34,37,39,43,44,48) 5VDDM
R258 1KΩ 1% 1/10W SMT0603 LR
D20
DIODE STKY CH751H-40PT 40V 0.03A SOD-323 2PIN CHENMKO LR
C370 1uF 6.3V +80-20% SMT0402 Y5V LR
C366 0.1uF 16V 80-20% SMT0402 Y5V LR
(5,8,10,12,15,17,19,22,23,24,25,27,28,30,31,32,33,34,36,37,38,39,41,42,44,48,49,51) 3VDDM
C951
L67
0.1uF 16V 80-20% SMT0402 Y5V LR
300Ω±25% 100MHz 2000mA SMT0603 MLB-160808-0300P-N2 MAG.LAYERS LR
(12,13,14,17,18,49) 1.8VDDM
C670 10uF 10V +80-20% SMT0805 Y5V LR
C668 0.1uF 16V 80-20% SMT0402 Y5V LR
C669 2200pF 50V 10% SMT0402 X7R LR
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Title
SB450 POWER(4/4)
Size C
Document Number
KR2W < AMD K8 + RS482M + SB450 >
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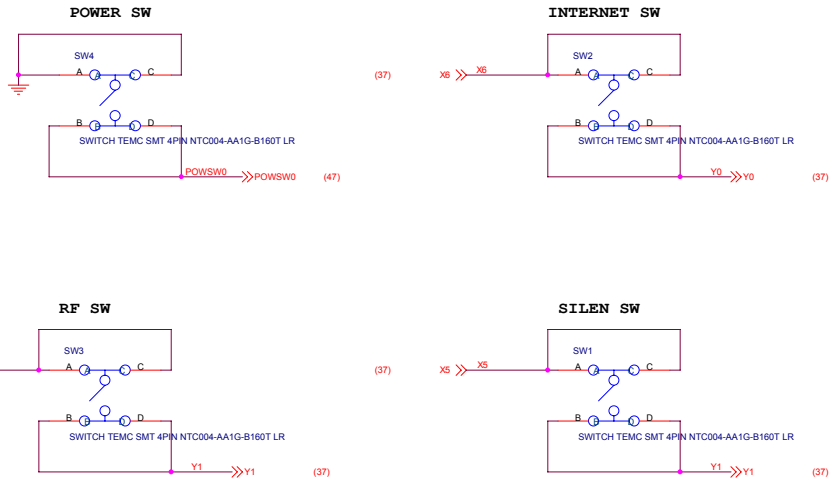
Switch



LED indicator control logic

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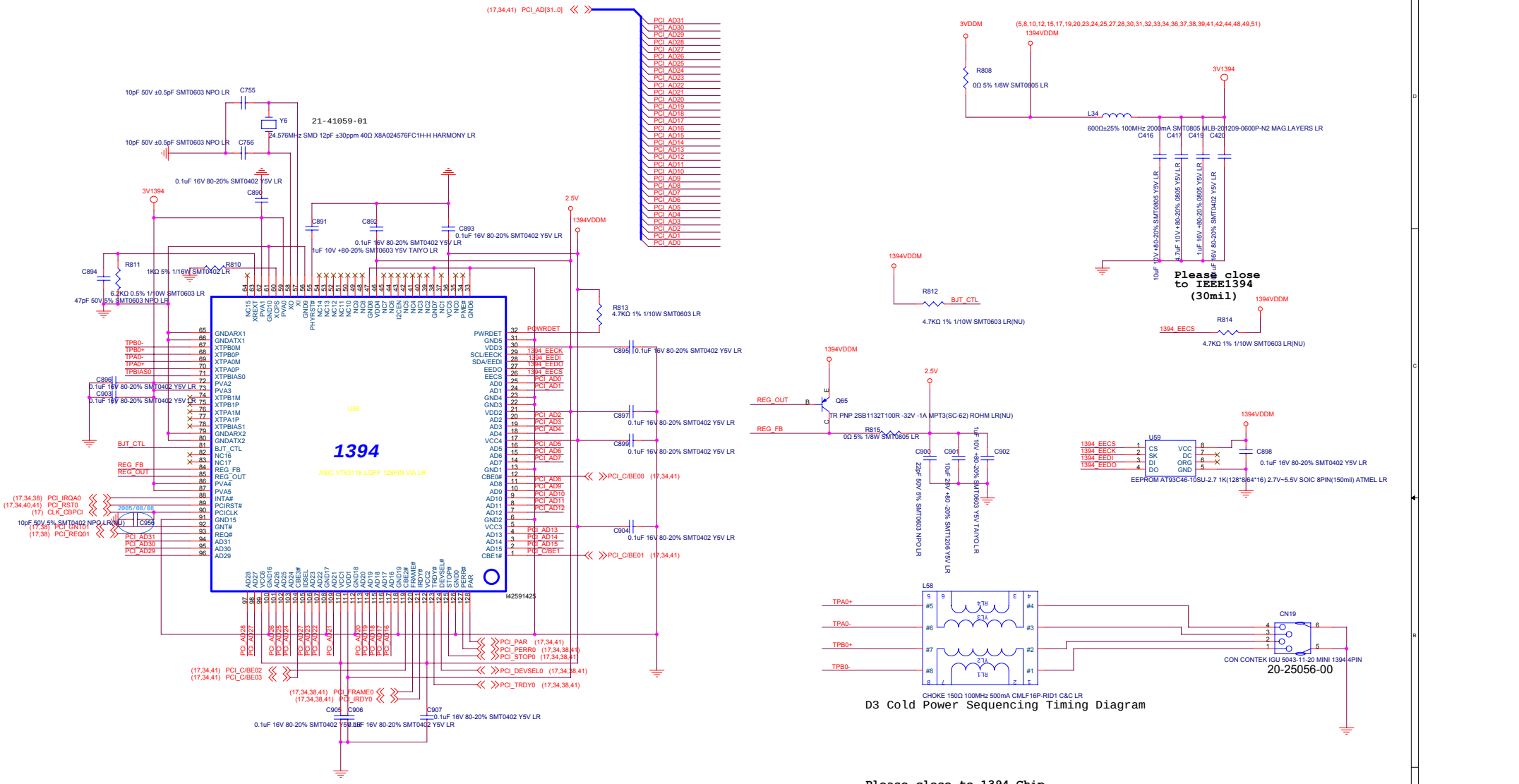
Title	LED / PWR SW	
Size: C	Document Number: KR2W < AMD K8 + RS482M + SB450 >	Rev: 0.1
Date: Tuesday, August 16, 2005	Sheet 21 of 54	



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3FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (883-2)8751-8751			
Title	VIA VT6311S(1394)		
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >		Rev 0.1
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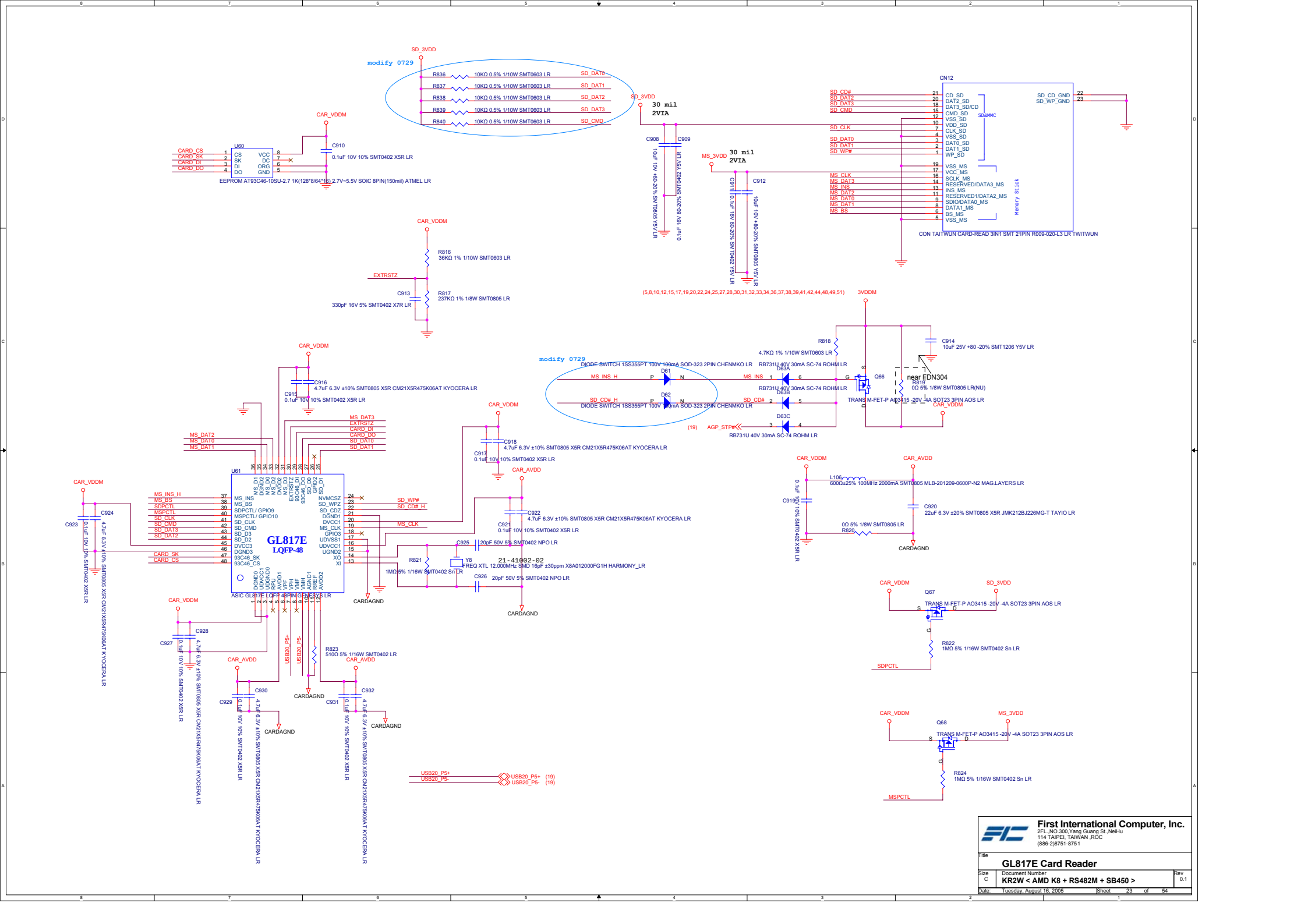

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Title: **GL817E Card Reader**

Size	Document Number	Rev
C	KR2W < AMD K8 + RS482M + SB450 >	0.1

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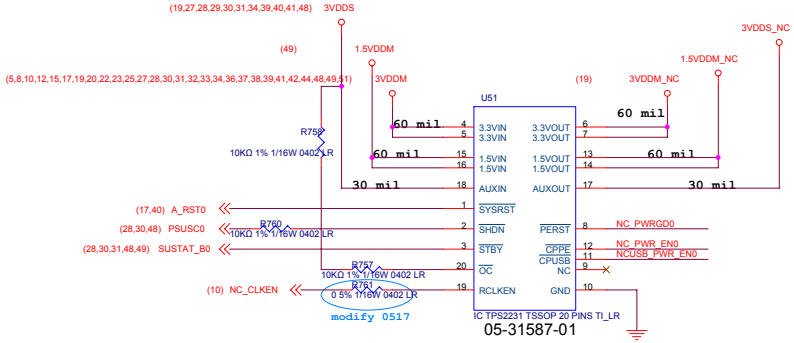

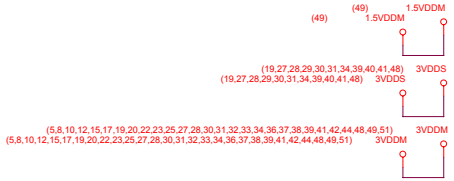

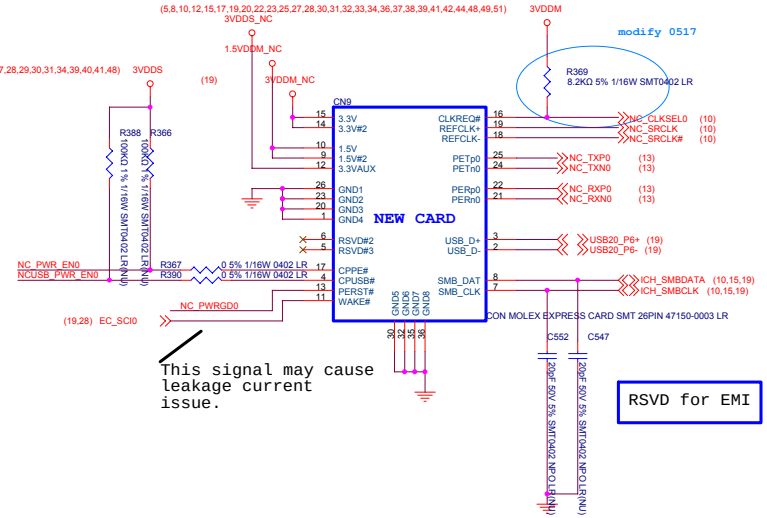

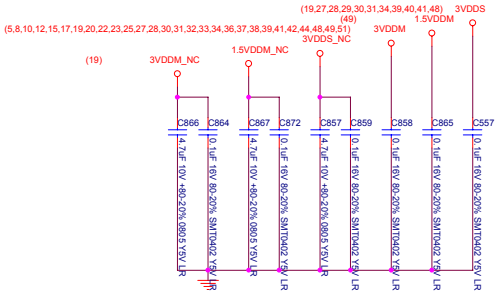

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Title: **AMD K8 + RS480M + SB400**

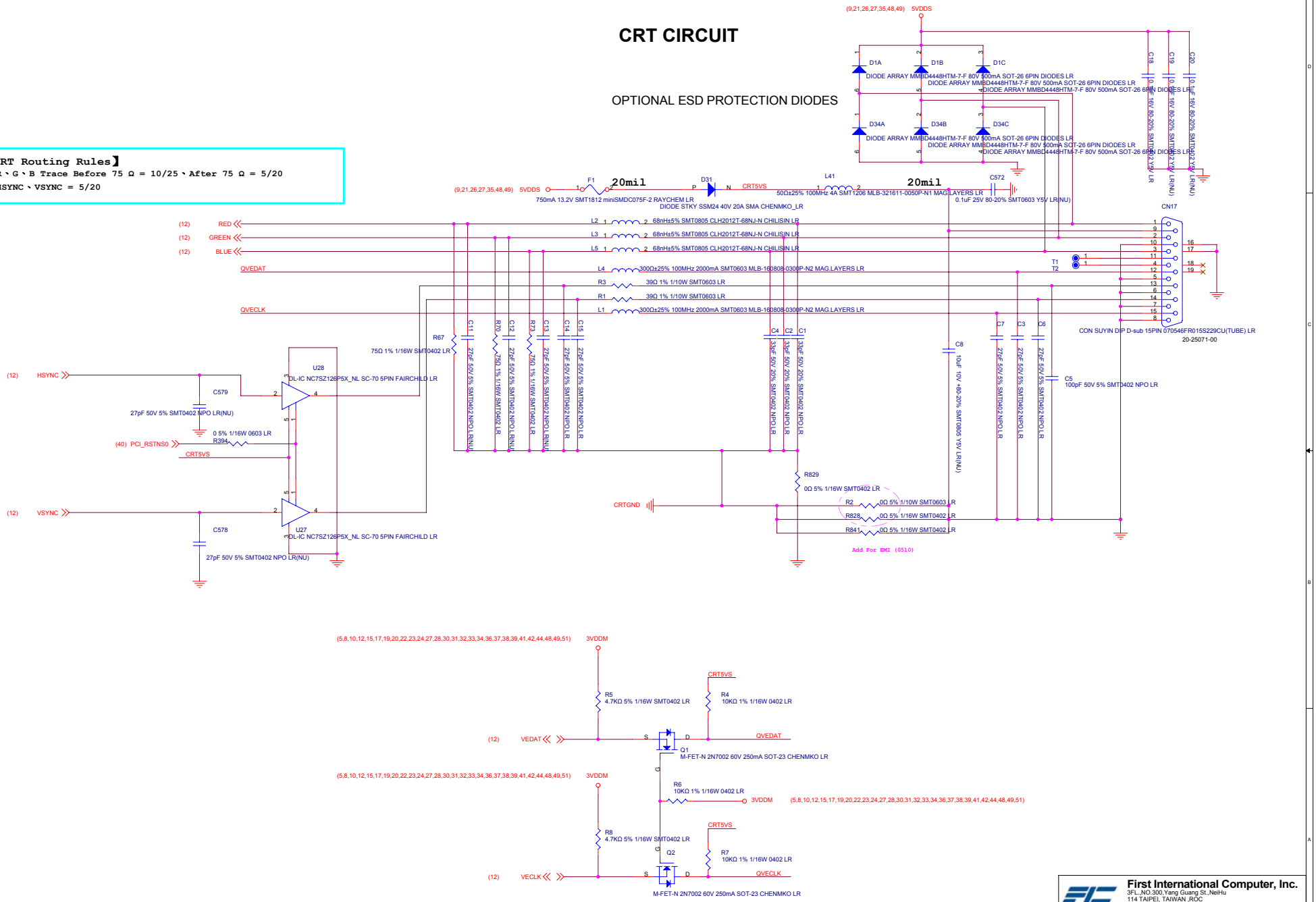
Size	Document Number	Rev
C	KR2W < AMD K8 + RS482M + SB450 >	0.1

Date: Tuesday, August 16, 2005 Sheet 24 of 54

CRT CIRCUIT

OPTIONAL ESD PROTECTION DIODES

【CRT Routing Rules】
1. R、G、B Trace Before 75 Ω = 10/25、After 75 Ω = 5/20
2. HSYNC、VSYNC = 5/20



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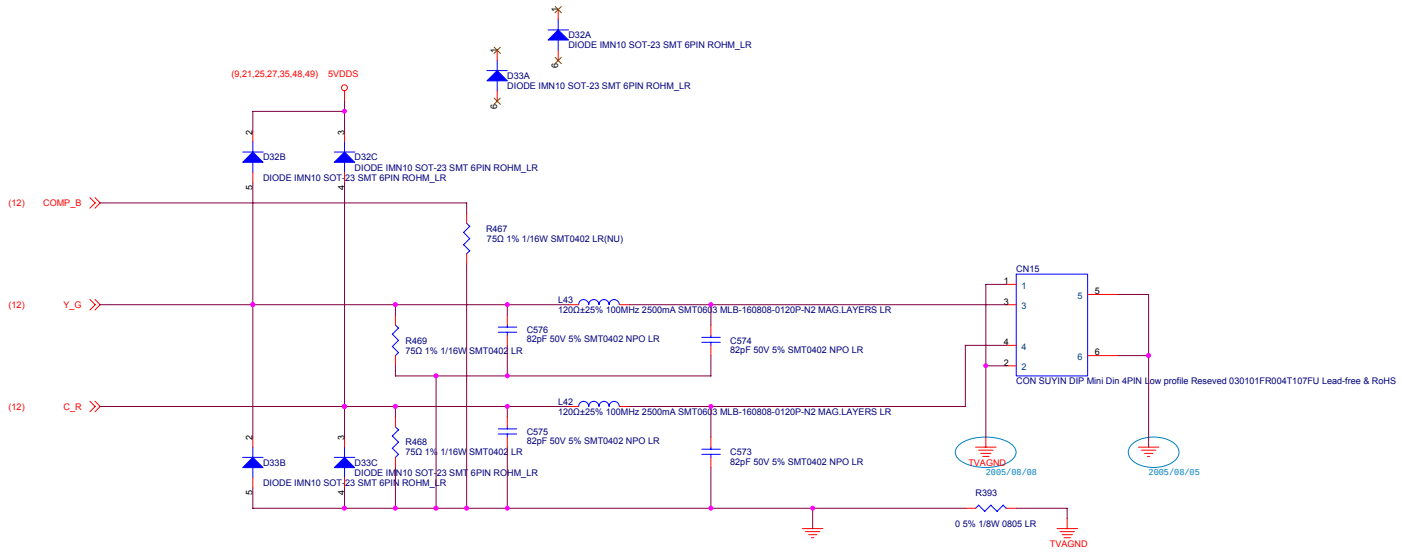
Title	CRT Port	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 25 of 54	

TV OUT CIRCUIT



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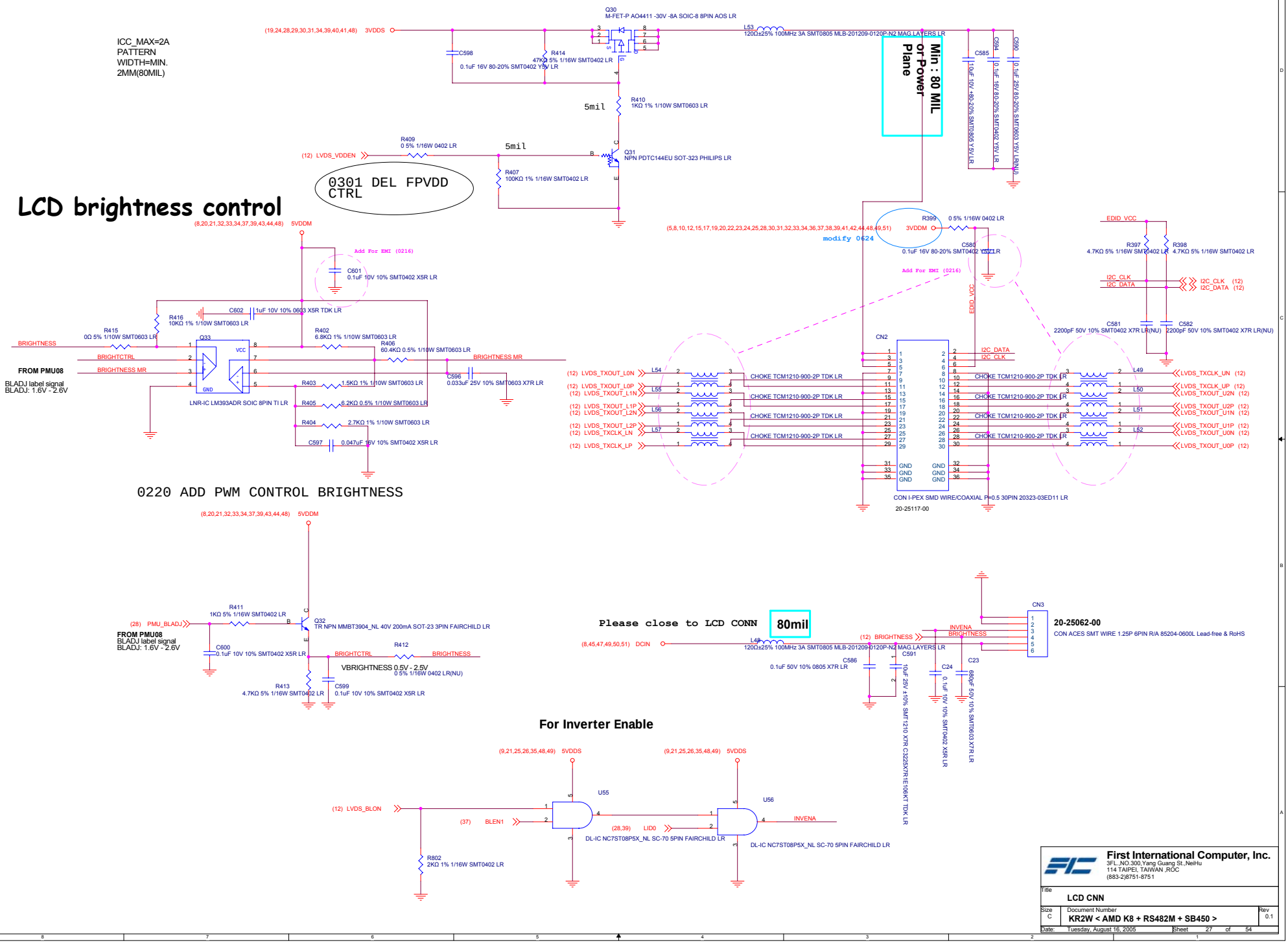
Title	**TV Port**	
Size: C	Document Number: **KR2W < AMD K8 + RS482M + SB450 >**	Rev: 0.1
Date: Tuesday, August 16, 2005	Sheet 26 of 54	

LCD brightness control



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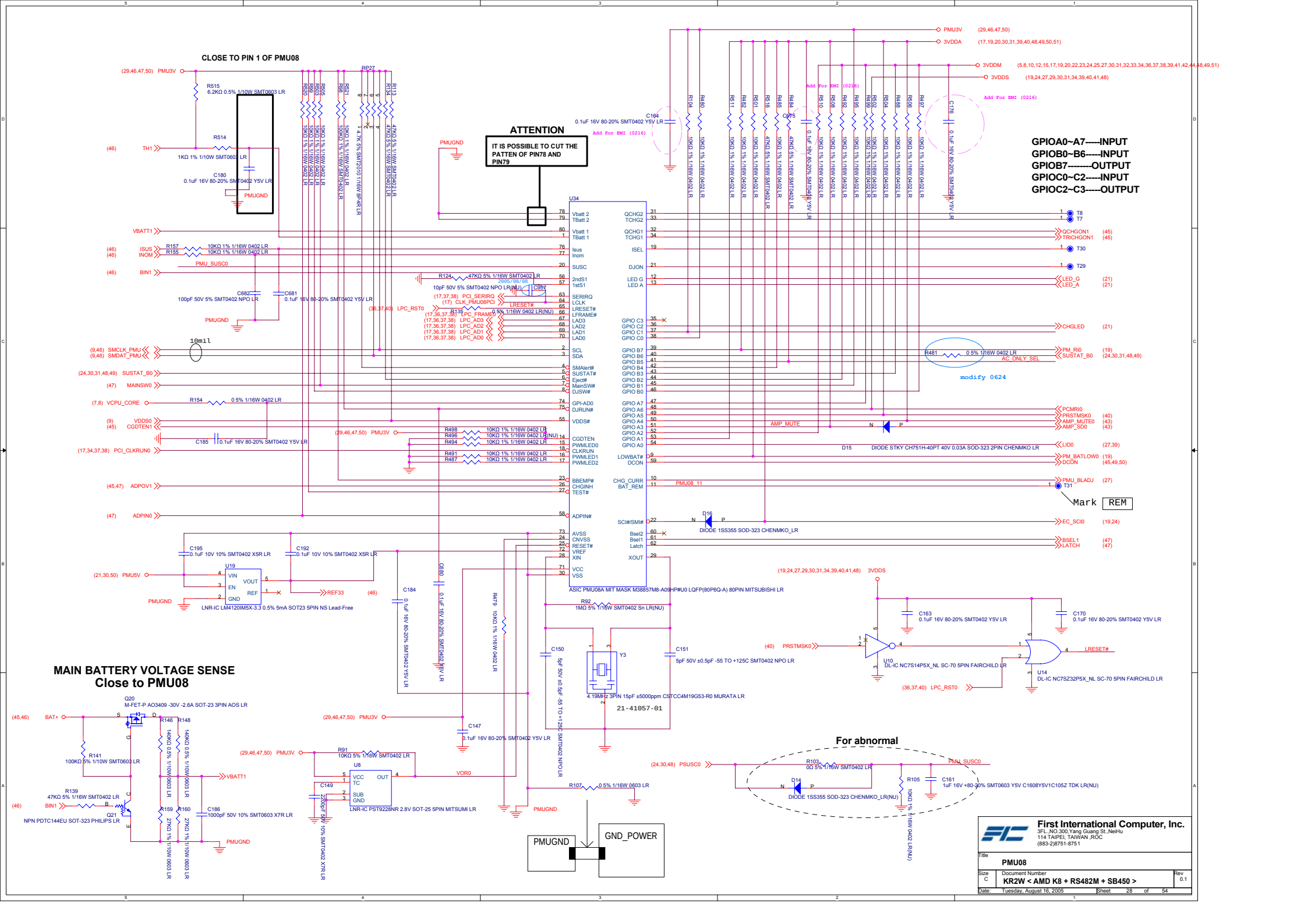
Title: LCD CNN

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

Date: Tuesday, August 16, 2005 | Sheet 27 of 54


CLOSE TO PIN 1 OF PMU08
ATTENTION
IT IS POSSIBLE TO CUT THE PATTEN OF PIN78 AND PIN79
GPIOA0~A7-----INPUT
GPIOB0~B6-----INPUT
GPIOB7--------OUTPUT
GPIOC0~C2-----INPUT
GPIOC2~C3-----OUTPUT
U34
ASIC PMU08A MIT MASK M38857M8-A09HP#U0 LQFP(80P6Q-A) 80PIN MITSUBISHI LR
MAIN BATTERY VOLTAGE SENSE
Close to PMU08
For abnormal
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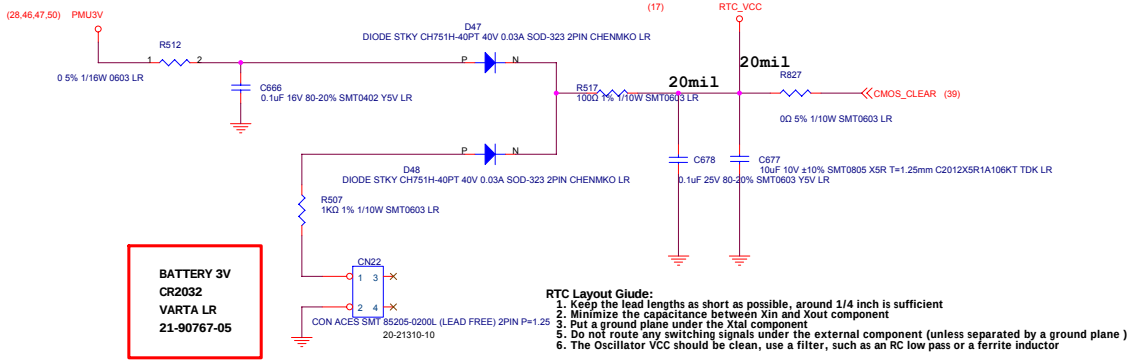
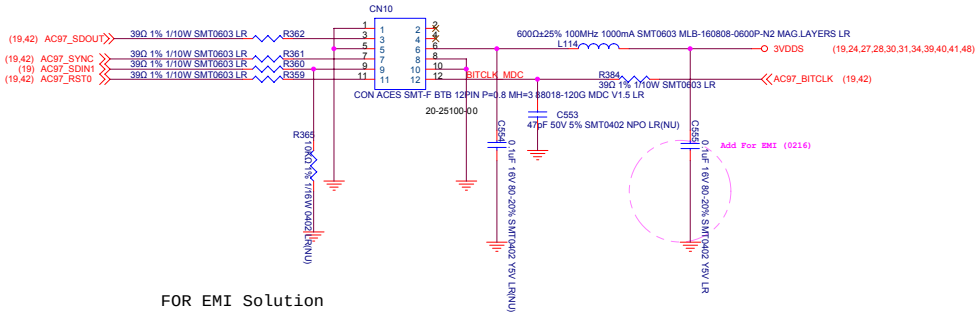
PMU08
KR2W < AMD K8 + RS482M + SB450 >
Rev 0.1
Tuesday, August 16, 2005
Sheet 28 of 54

RTC Discharge Circuit



MDC CNN



FOR EMI Solution

Close

CON ACES 1.25mm WTB SMT R/A 88266-02001 gold flash 2 PIN H=1.9mm LR
20-24461-10

CON ACES 1.25mm WTB SMT R/A 88266-02001 gold flash 2 PIN H=1.9mm LR
20-24461-10

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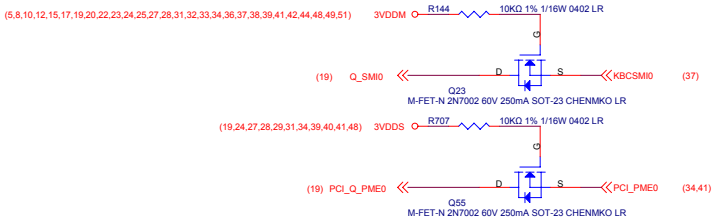
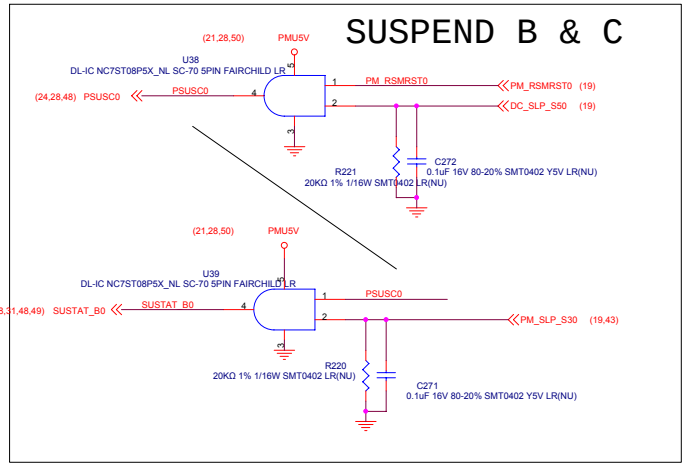
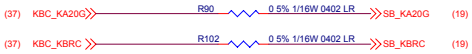
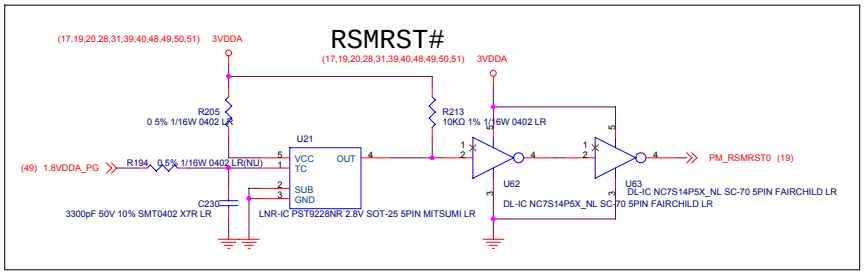
Title	RTC/ MDC CNN	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 29 of 54	







RESUME RESET



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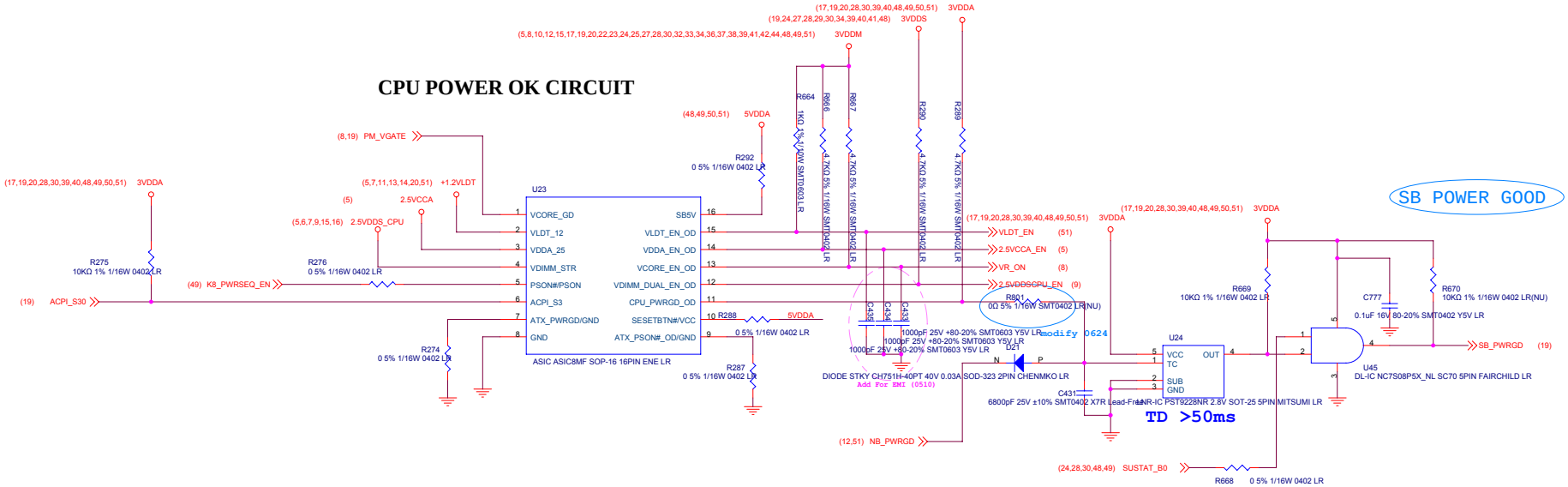
3FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (883-2)8751-8751		
Title	ASIC-C0	
Size: C	Document Number: KR2W < AMD K8 + RS482M + SB450 >	Rev: 0.1
Date: Tuesday, August 16, 2005	Sheet 30 of 54	

CPU POWER OK CIRCUIT



First International Computer, Inc.
3FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(883-2)8751-8751

Title	CPU PWR OK / SYSTEM OVP	
Size: C	Document Number: KR2W < AMD K8 + RS482M + SB450 >	Rev: 0.1
Date: Tuesday, August 16, 2005	Sheet 31 of 54	

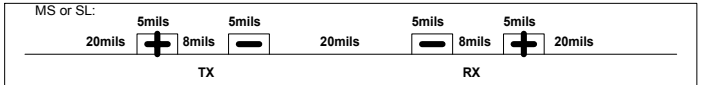
HDD I/F

NOTE

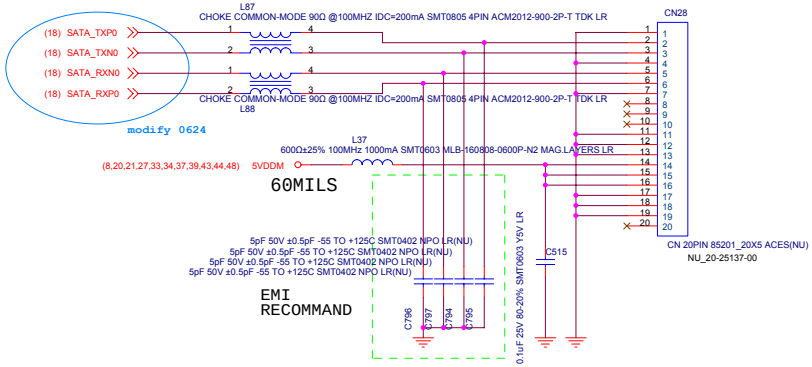
SATA differential stripline 20:4:8:4:20
SATA differential mircostripline 20:5:8:5:20
請包GROUND

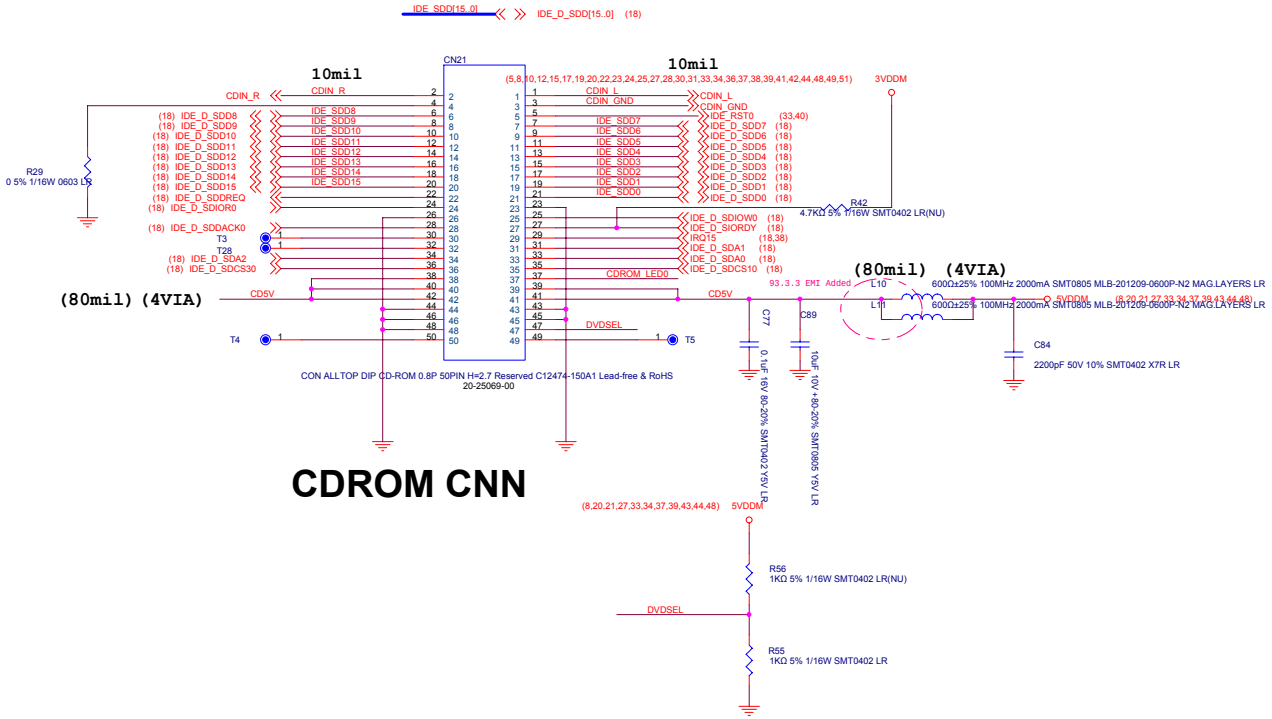
SATA Layout Note:

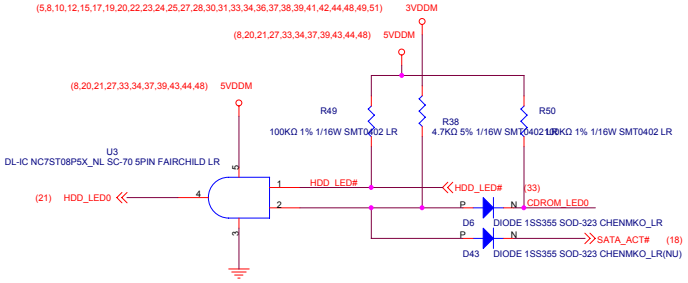
MS or SL:



* Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
* TX/RX trace length < 2 inchs.
* TX+/- need matching trace ±10 mils length.
* RX+/- need matching trace ±10 mils length.
* SATA Pair to Pair Trace matching trace ±10 mils length.







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Title: SATA HD / CD-ROM CNN

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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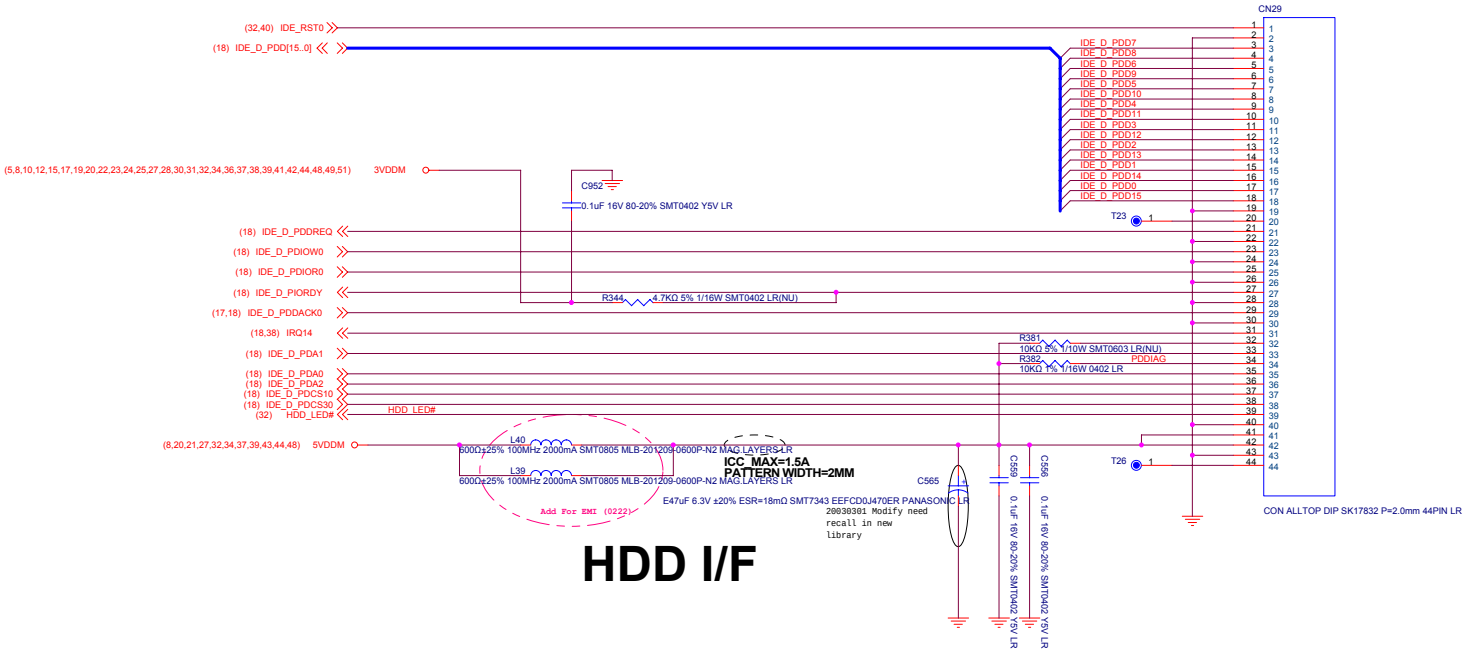
PATA-HDD CNN



HDD I/F

IDE Signals (microstrip)

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	7
IDE_SDD[15:0]	8	5	7
IDE_PDA0-2	8	5	7
IDE_SDA0-2	8	5	7
IDE_PDCS 10-30#	8	5	7
IDE_PDDREQ	8	5	7
IDE_SDDREQ	8	5	7
IDE_PDIOW#	8	5	7
IDE_PATADET	8	5	7
IDE_SATADET	8	5	7
IDE_PDDACK#	8	5	7
IDE_SDDACK#	8	5	7

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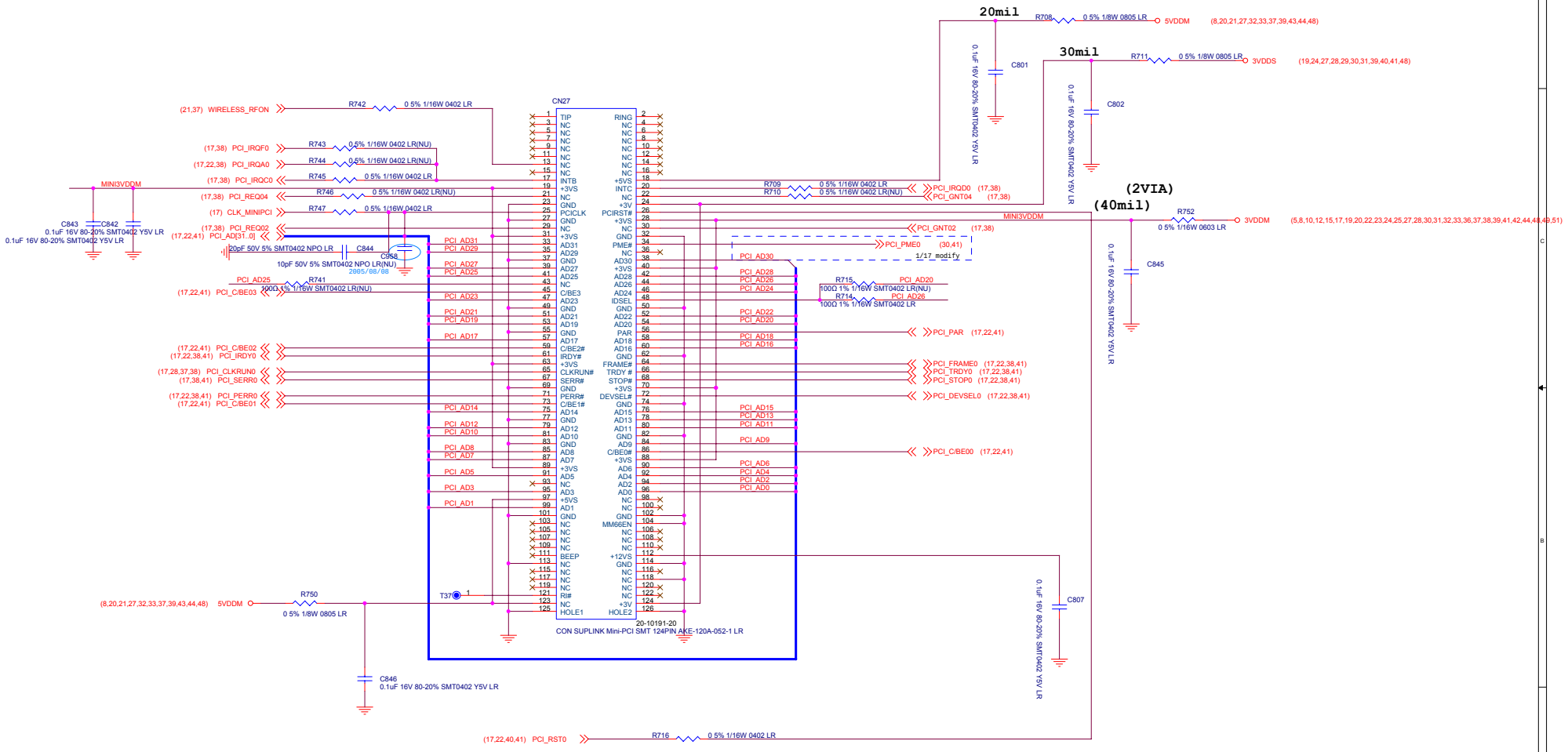
Title: PATA HD FPC-CNN

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

Date: Tuesday, August 16, 2005 | Sheet 33 of 54

TYPE III MODEM / LAN CONNECTOR



Company	First International Computer, Inc.
Address	3FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC
Phone	(883-2)8751-8751
Title	Calexico MINI PCI
Size	C
Document Number	KR2W < AMD K8 + RS482M + SB450 >
Rev	0.1
Date	Tuesday, August 16, 2005
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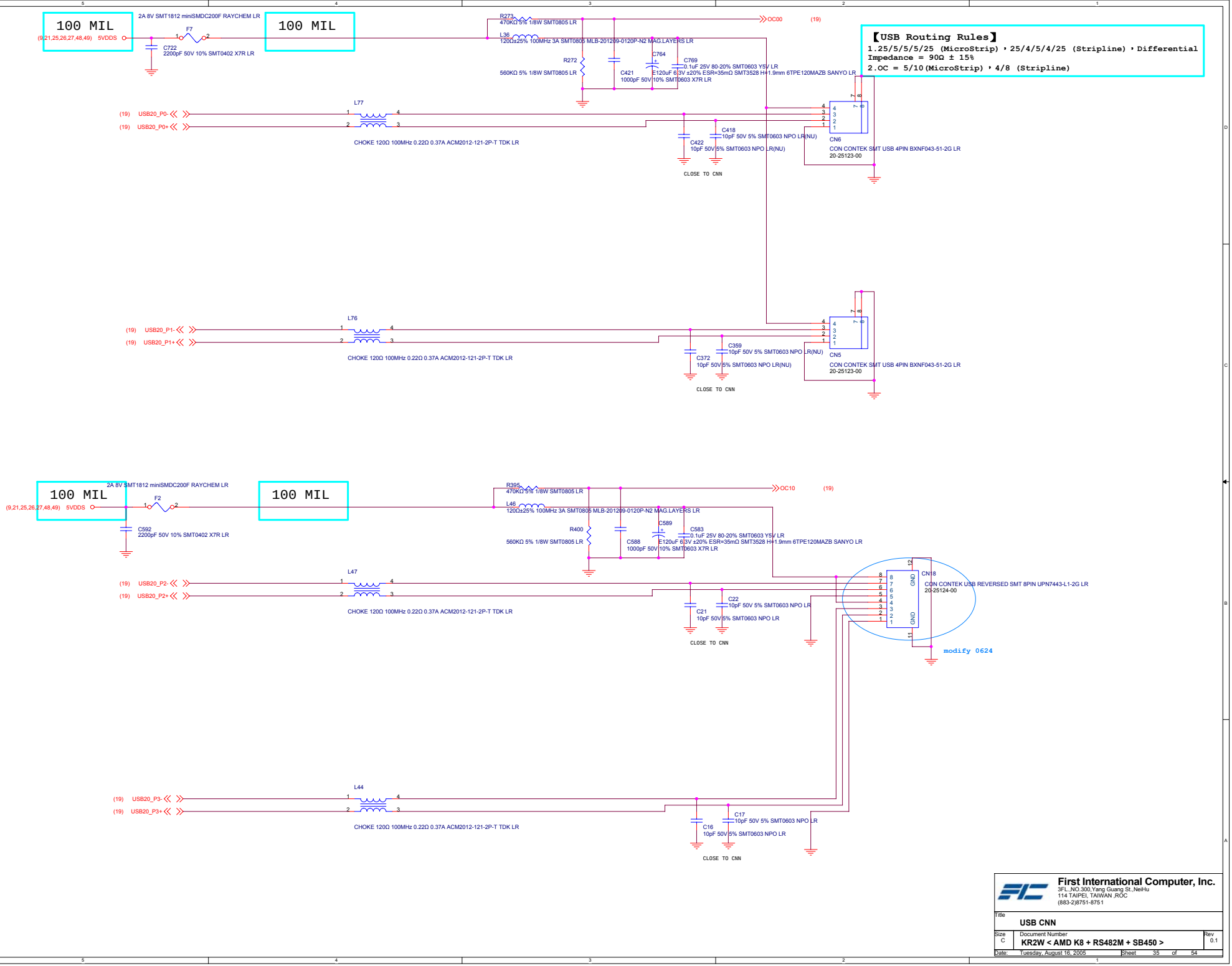

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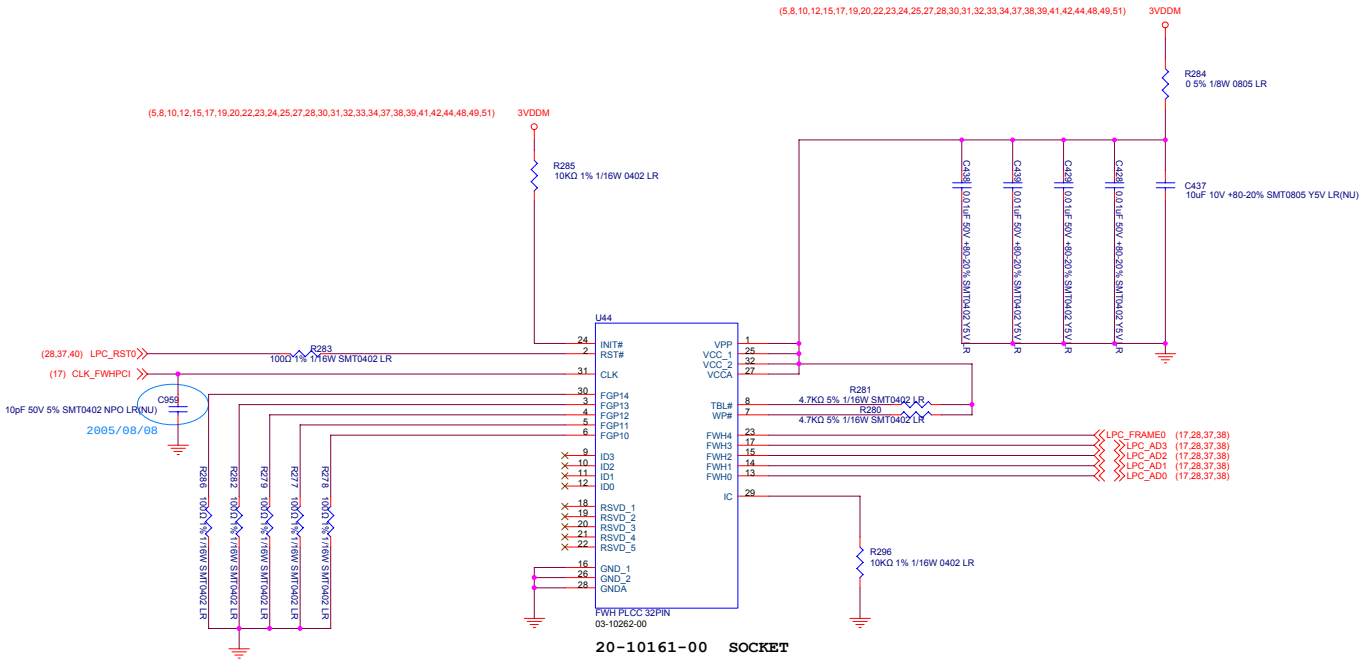
Title	USB CNN	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 35 of 54	



20-10161-00 SOCKET

03-10262-00 EEPROM SST49LF004B-33-4C-NHE 4Mbit(512K*8)

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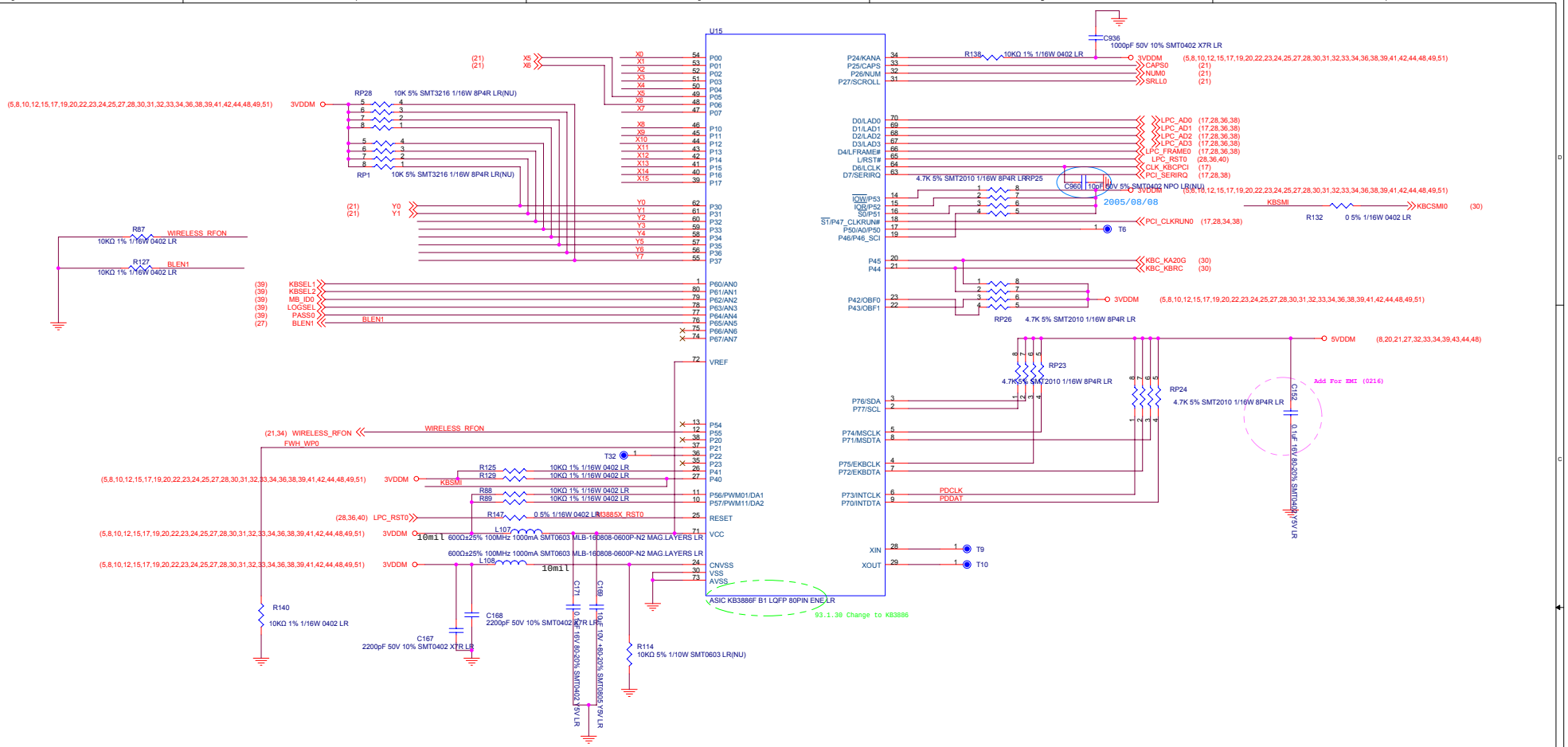
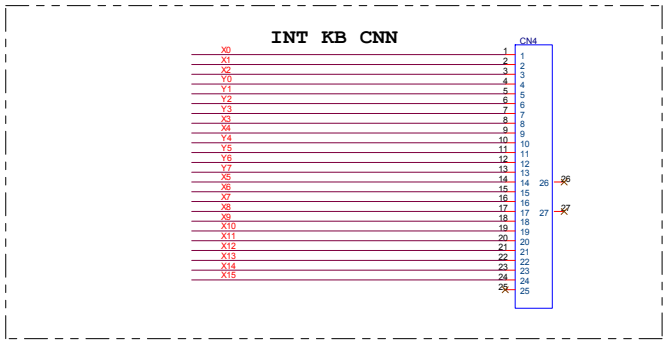
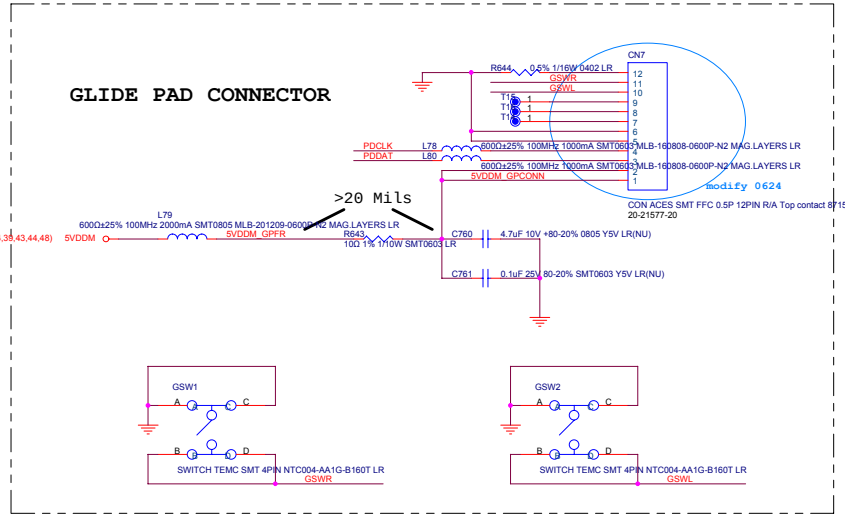
Title	FirmWare Hub	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 36 of 54	







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Title	LPC KBC (M3886)	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
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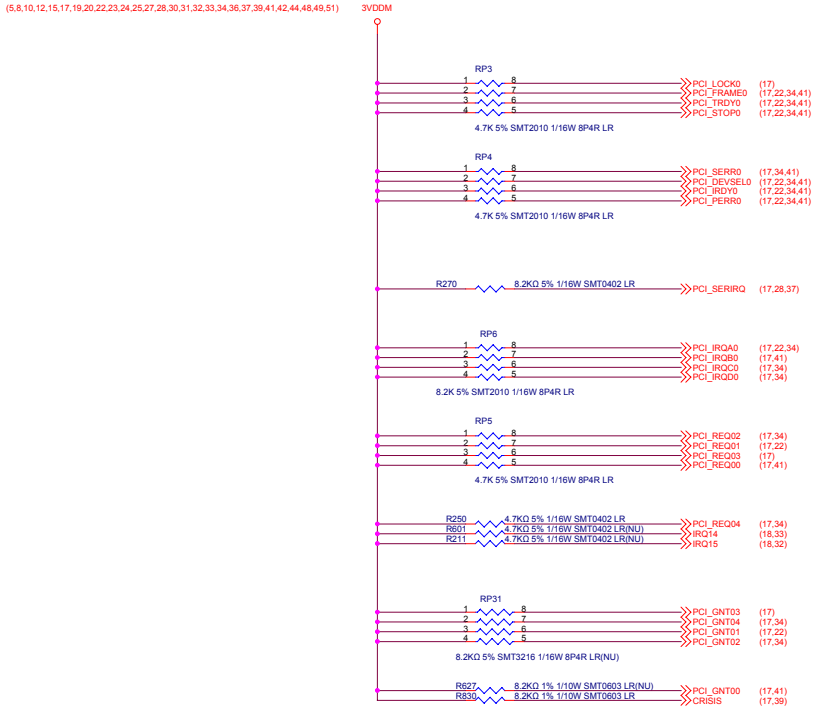
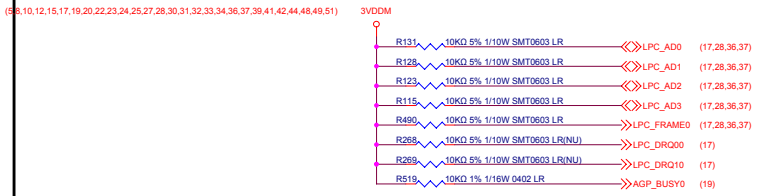
PCI Pull Up/Down

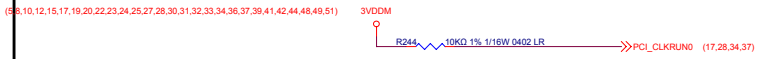


LPC Pull Up

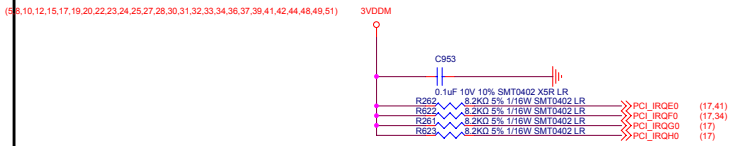


PCI PMU Pull Up

PME PULL HI 3VDDA



GPIO Pull Up



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(883-2)8751-8751

Title	PCI/LPC Pullup/Down	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
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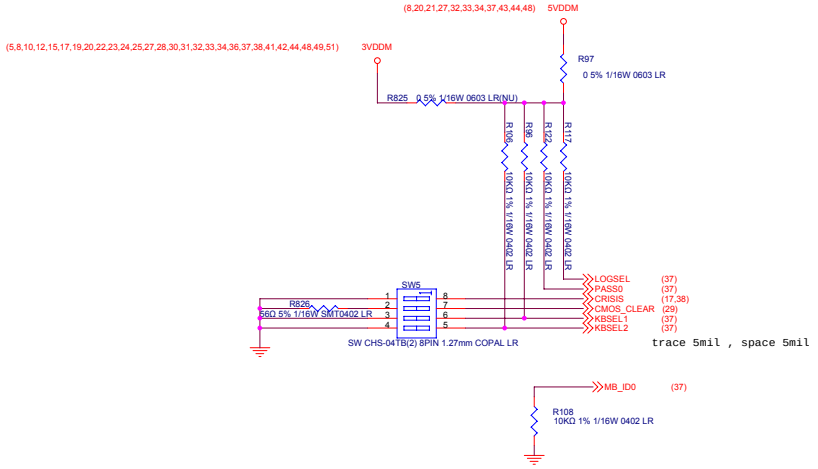
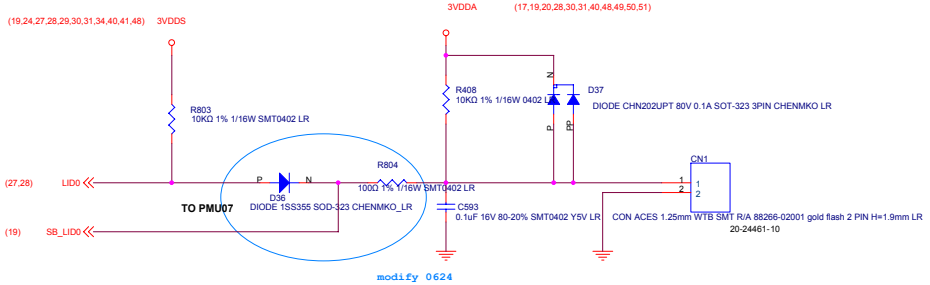
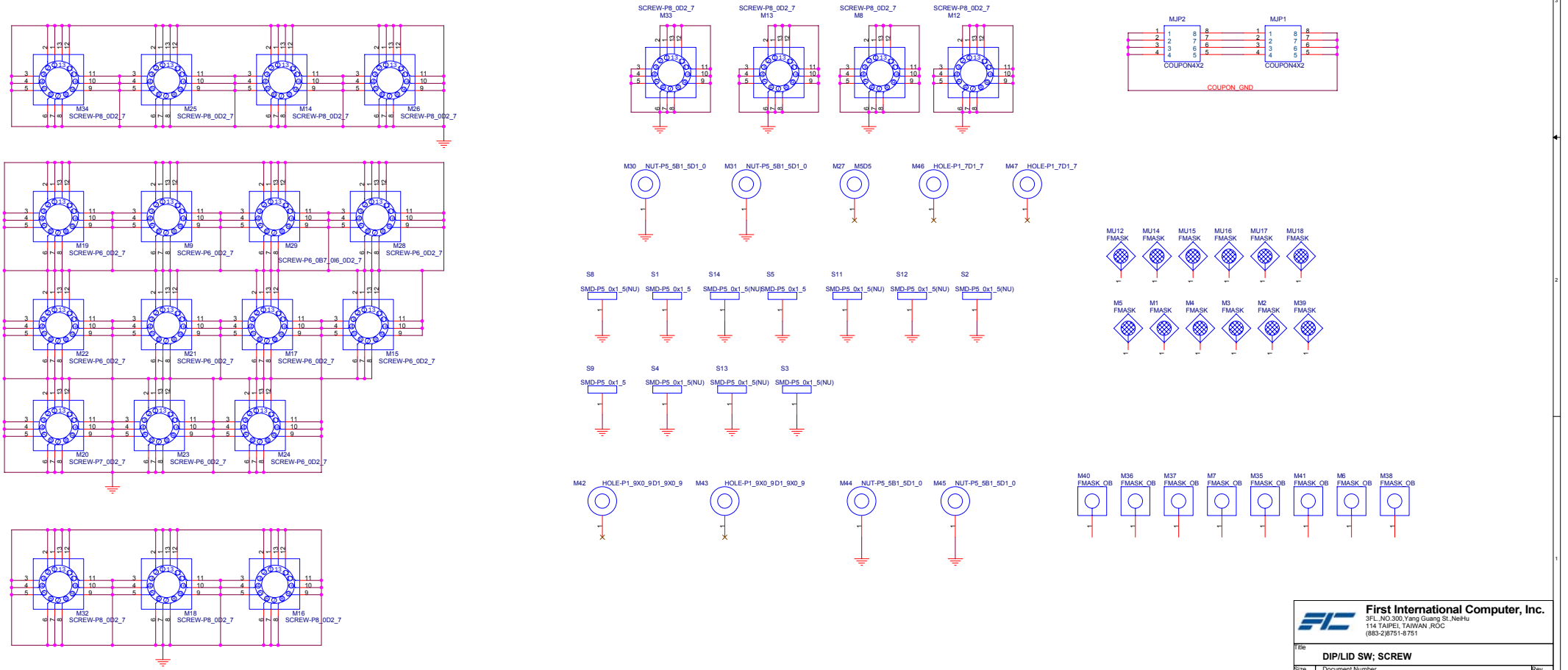
DIP SWITCH



LID Switch





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Title	DIP/LID SW; SCREW	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
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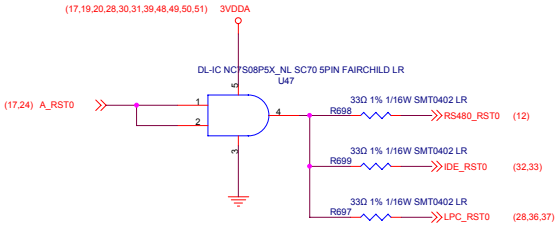
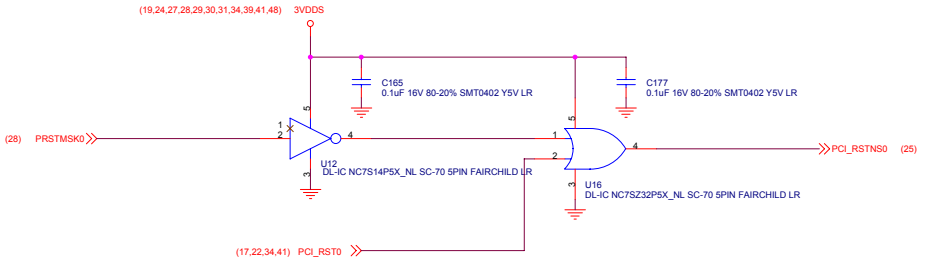
PCI RESET & PCI NON RESET





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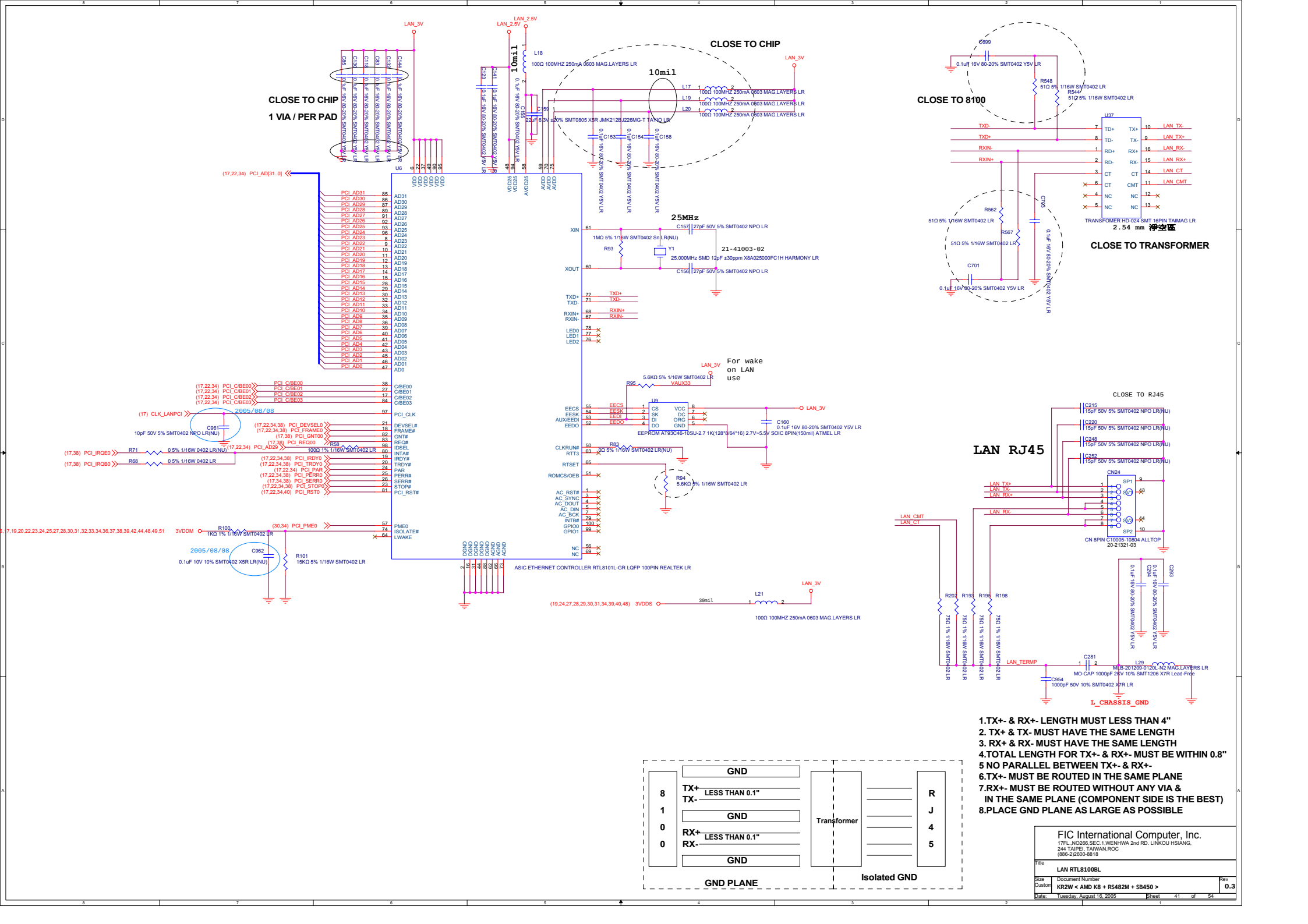
3FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (883-2)8751-8751		
Title: PCI/IDE Reset Circuit		
Size: C	Document Number: KR2W < AMD K8 + RS482M + SB450 >	Rev: 0.1
Date: Tuesday, August 16, 2005	Sheet 40 of 54	


CLOSE TO CHIP
1 VIA / PER PAD
CLOSE TO CHIP
10mil
CLOSE TO 8100
CLOSE TO TRANSFORMER
25MHz
21-41003-02
For wake on LAN use
CLOSE TO RJ45
LAN RJ45
ASIC ETHERNET CONTROLLER RTL8101L-GR LQFP 100PIN REALTEK LR
EEPROM AT93C46-10SU-2.7 1K(128*8/64*16) 2.7V~5.5V SOIC 8PIN(150mil) ATMEL LR
TRANSFORMER HD-024 SMT 16PIN TAIMAG LR
CN 8PIN C10005-10804 ALLTOP 20-21321-03
MO-CAP 1000pF 2KV 10% SMT1206 X7R Lead-Free
1.TX+- & RX+- LENGTH MUST LESS THAN 4"
2. TX+ & TX- MUST HAVE THE SAME LENGTH
3. RX+ & RX- MUST HAVE THE SAME LENGTH
4.TOTAL LENGTH FOR TX+- & RX+- MUST BE WITHIN 0.8"
5 NO PARALLEL BETWEEN TX+- & RX+-
6.TX+- MUST BE ROUTED IN THE SAME PLANE
7.RX+- MUST BE ROUTED WITHOUT ANY VIA &
IN THE SAME PLANE (COMPONENT SIDE IS THE BEST)
8.PLACE GND PLANE AS LARGE AS POSSIBLE
GND
TX+
TX-
LESS THAN 0.1"
RX+
RX-
Transformer
GND PLANE
Isolated GND
FIC International Computer, Inc.
17FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818
LAN RTL8100BL
KR2W < AMD K8 + RS482M + SB450 >
0.3
Tuesday, August 16, 2005
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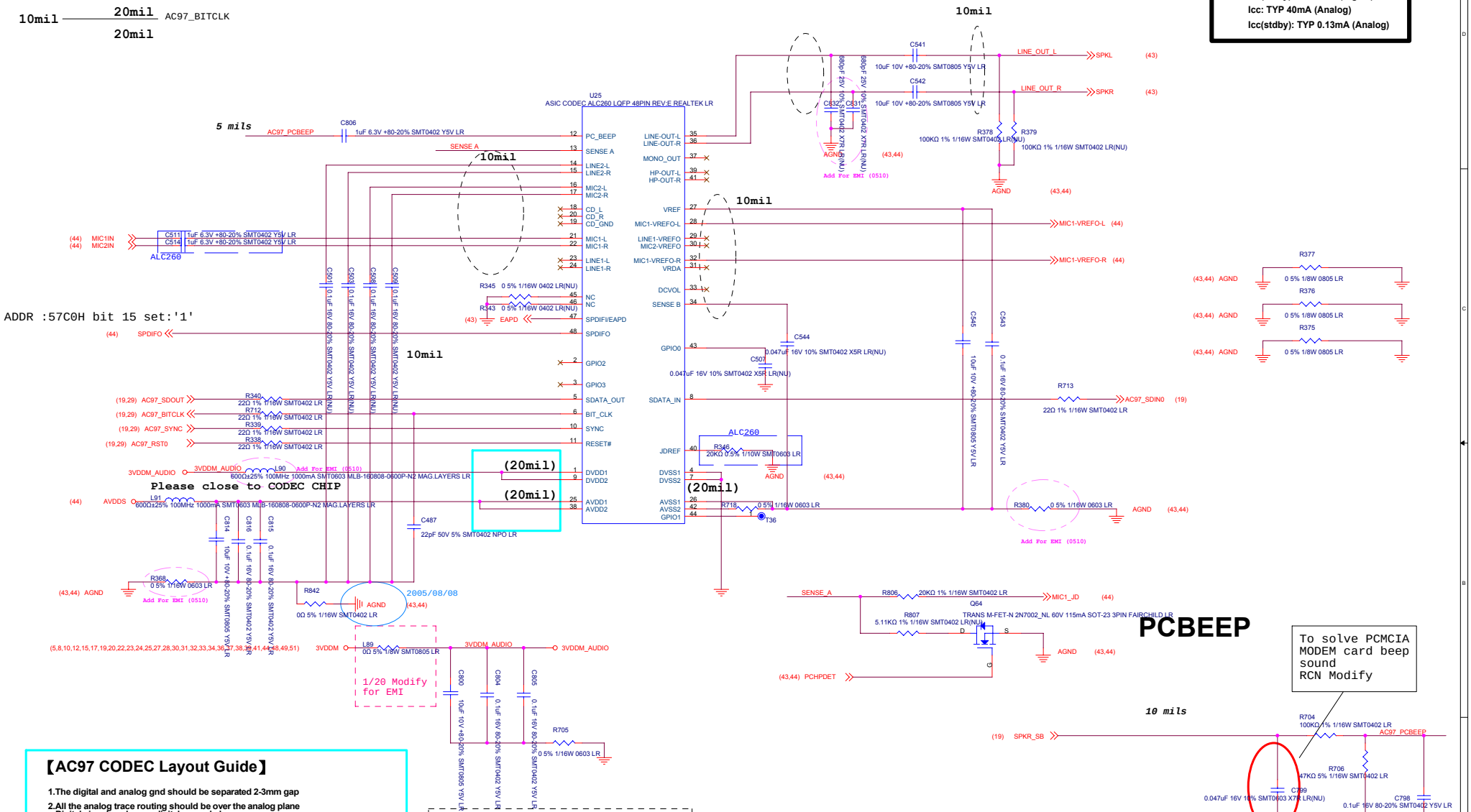
5mil 10mil AC97_PCBEEP 10mil

5mil 20mil 14MCLK_AC97 20mil

10mil 20mil AC97_BITCLK 20mil

AC97 CODEC Power Consumption:
Power Dissipation: TYP 330mW
Icc: TYP 40mA (Digital)
Icc(stdby): TYP 0mA (Digital)
Icc: TYP 40mA (Analog)
Icc(stdby): TYP 0.13mA (Analog)



【AC97 CODEC Layout Guide】

1. The digital and analog gnd should be separated 2-3mm gap
2. All the analog trace routing should be over the analog plane Digital signals only over digital ground plane
3. The analog and digital planes should electrically shorted at one place
4. All supply high frequency decoulping ,reference high freguency decoulp and filter caps must be routed on the same layer as the codec
5. Analog I/O routing should be kept a short as possible
6. Use of ground plane fill and the copper fill should be shorted to the analog ground plane
7. The AC-link signal should be as short as possible and should be shielding with ground
8. AC-link clock signal should have a series resistor close to the codec
9. Locate analog section away from high speed digital circuits
10. Place smallest bypass capacitor closest to IC pin
11. Use metal film resistors and NPO capacitors in analog path

LFE 20mil 20mil 10mil

LINE_OUT_L 20mil 20mil 10mil
LINE_OUT_R 20mil 20mil 10mil

CD_GND 10mil 10mil
CD_L 10mil 10mil
CD_GND 20mil
CD_R 10mil 10mil
CD_GND 10mil 10mil

First International Computer, Inc.
3FL.,NO.300,Yang Guang St.,NeiHu
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Title: AUDIO CODEC(ALC260)

Size	Document Number	Rev
C	KR2W < AMD K8 + RS482M + SB450 >	0.1

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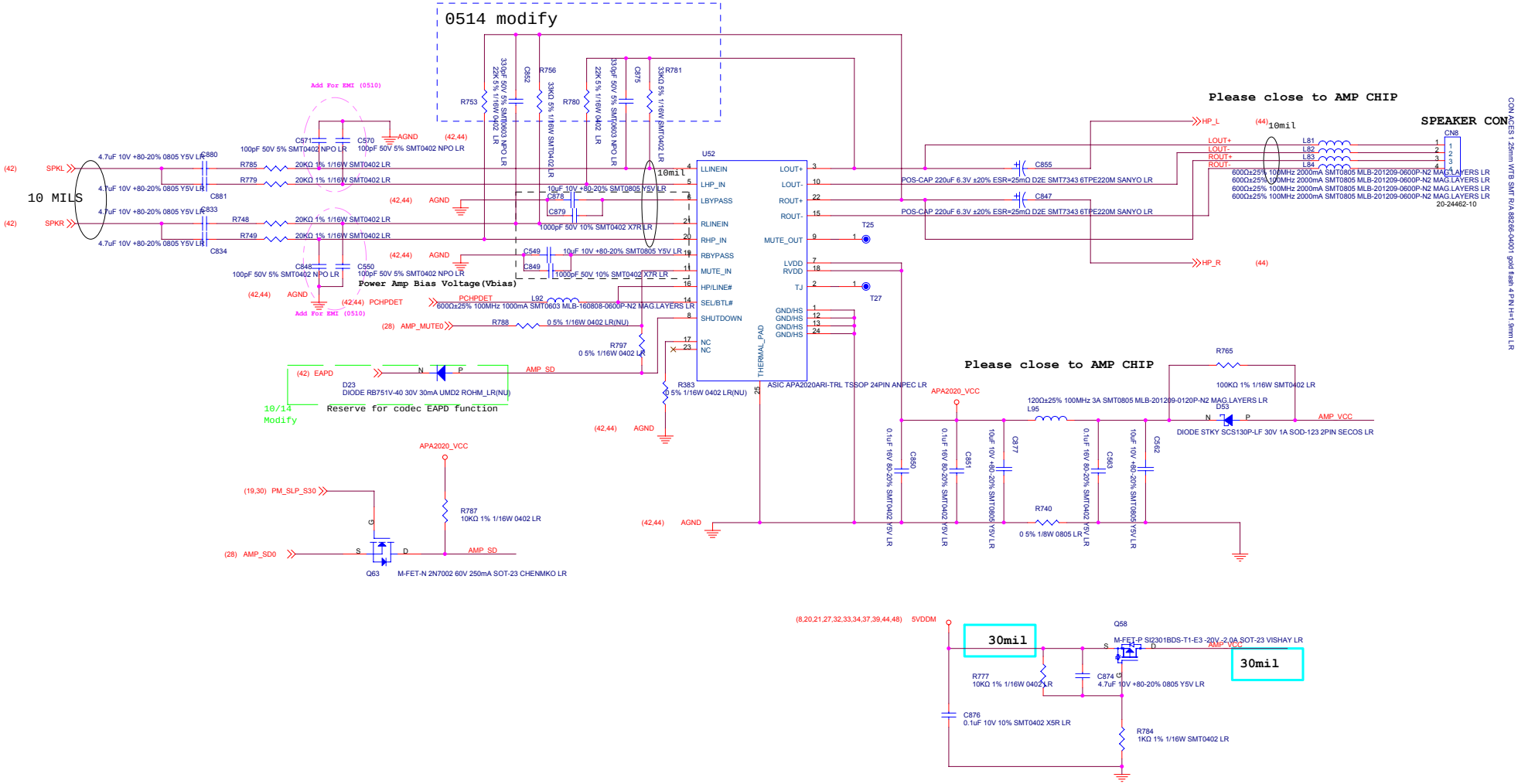

Company	First International Computer, Inc.
Address	3FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC
Phone	(883-2)8751-8751
Title	AUDIO AMP & SPEAKER
Size	C
Document Number	KR2W < AMD K8 + RS482M + SB450 >
Rev	0.1
Date	Tuesday, August 16, 2005
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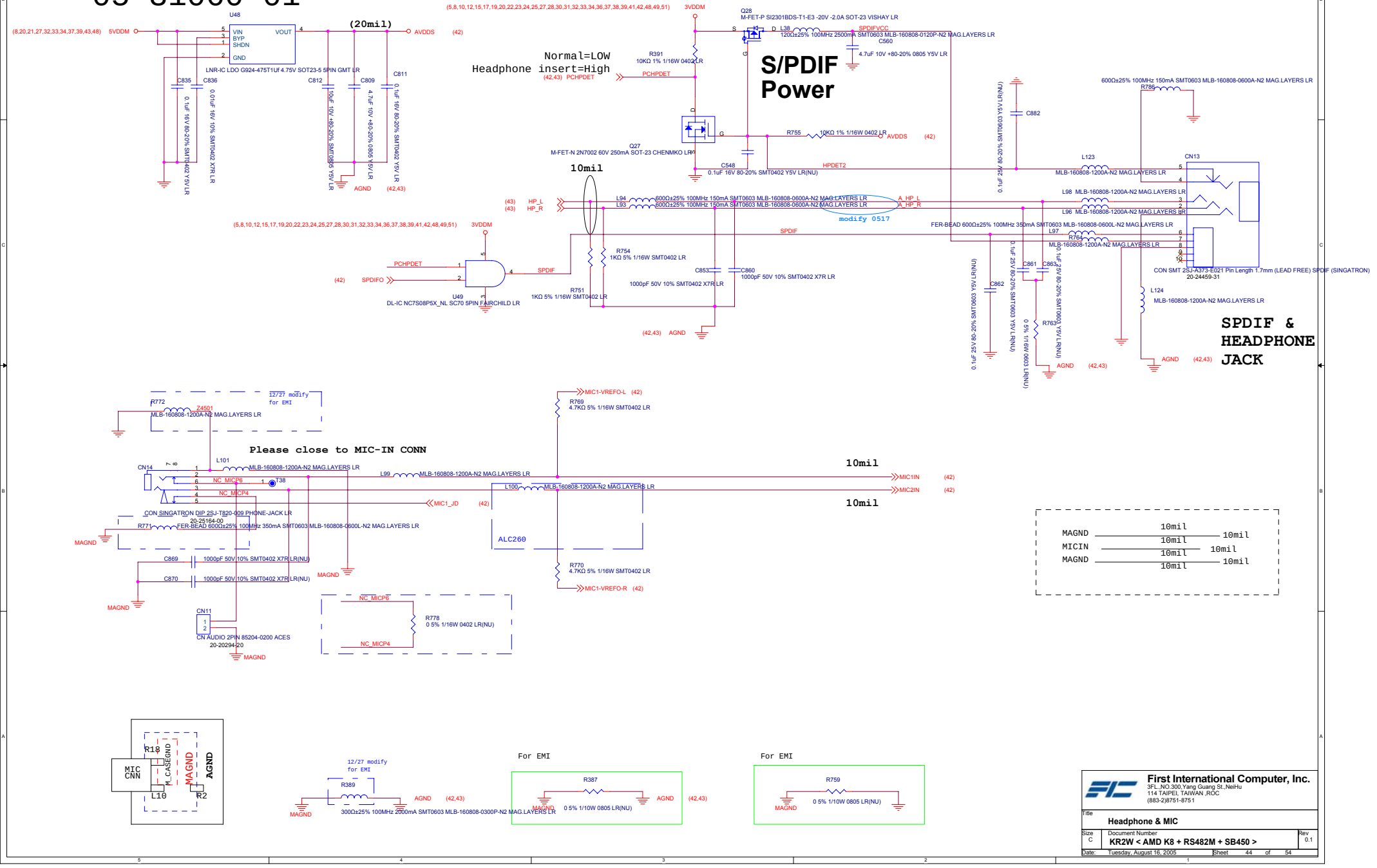
05-31060-01



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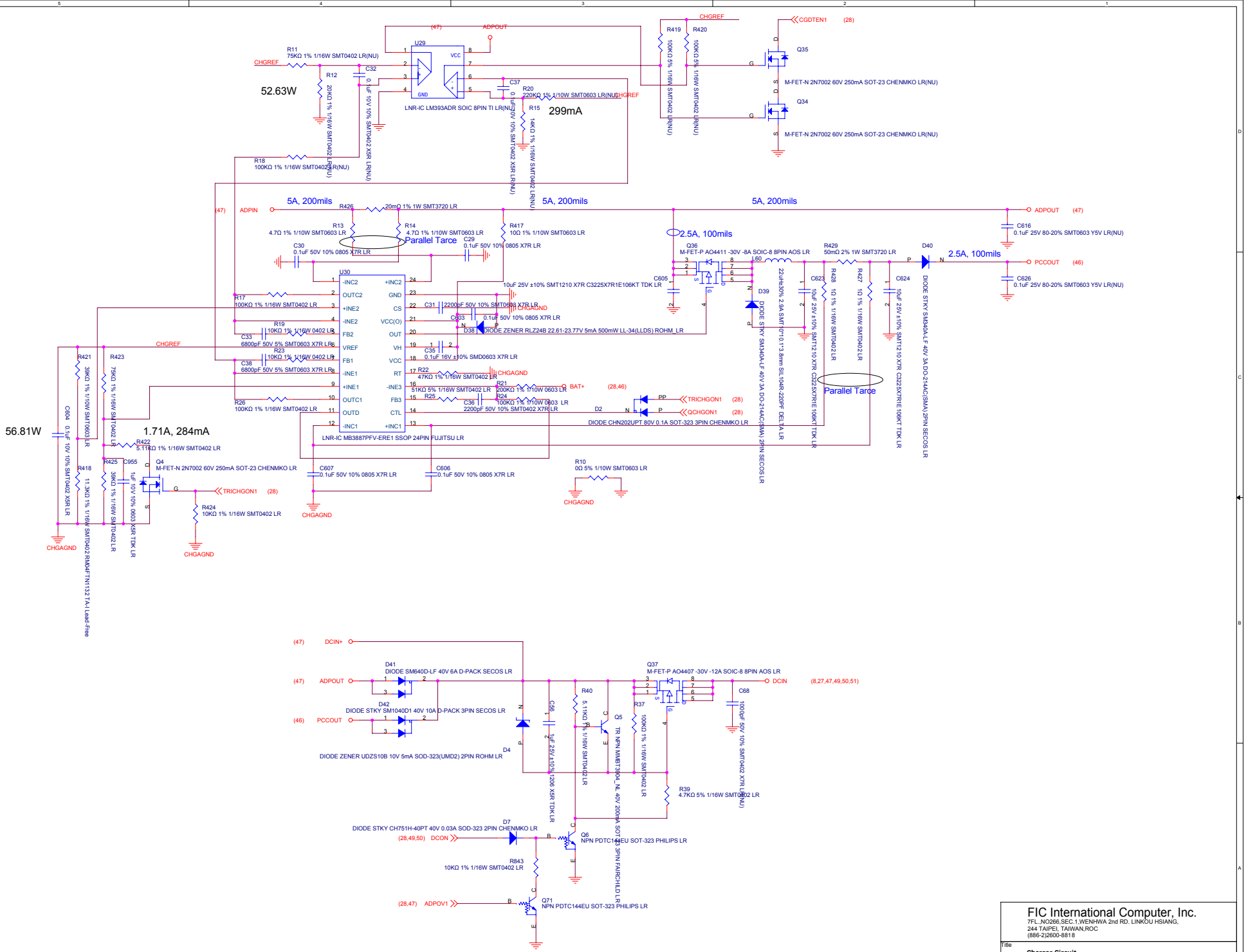
Title	Headphone & MIC	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 44 of 54	



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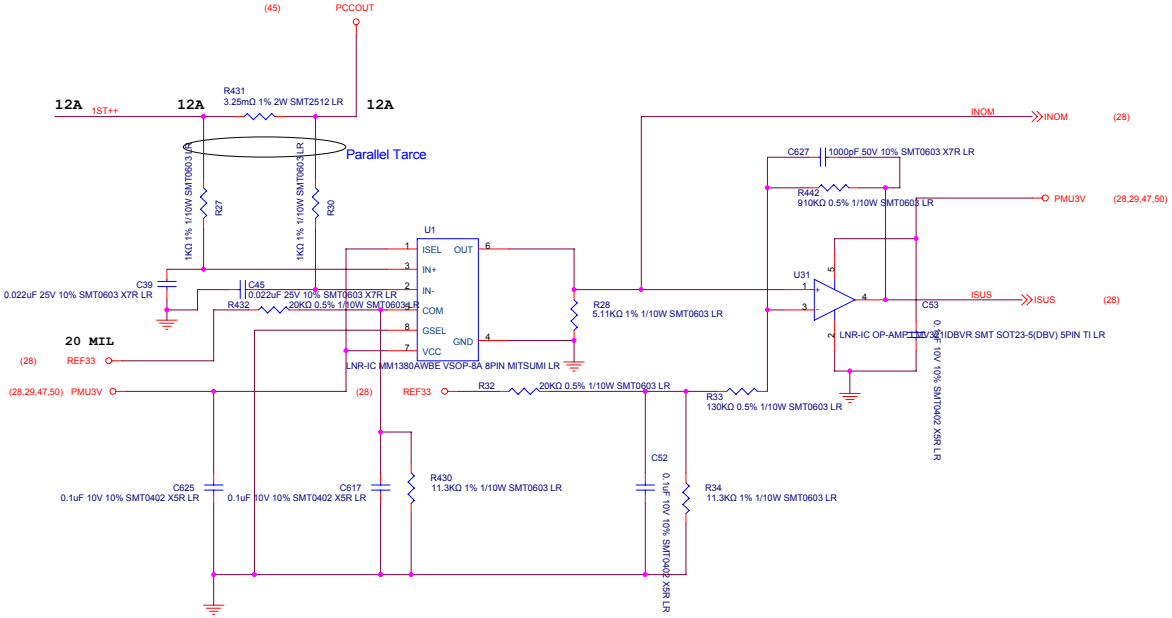
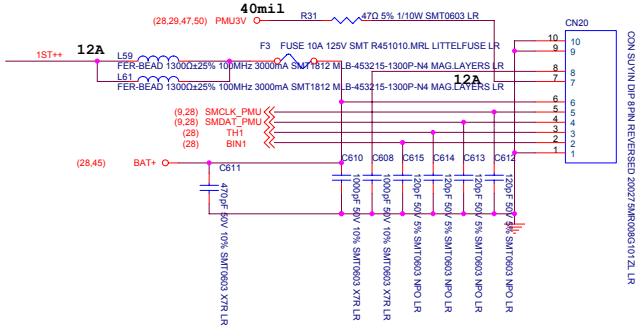
7FL.,NO266,SEC.1,WENHWA 2nd RD. LINKOU HSIANG,
244 TAIPEI, TAIWAN,ROC
(886-2)2600-8818

Title	Charger Circuit	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 45 of 54	

CHR Board BATTERY IN





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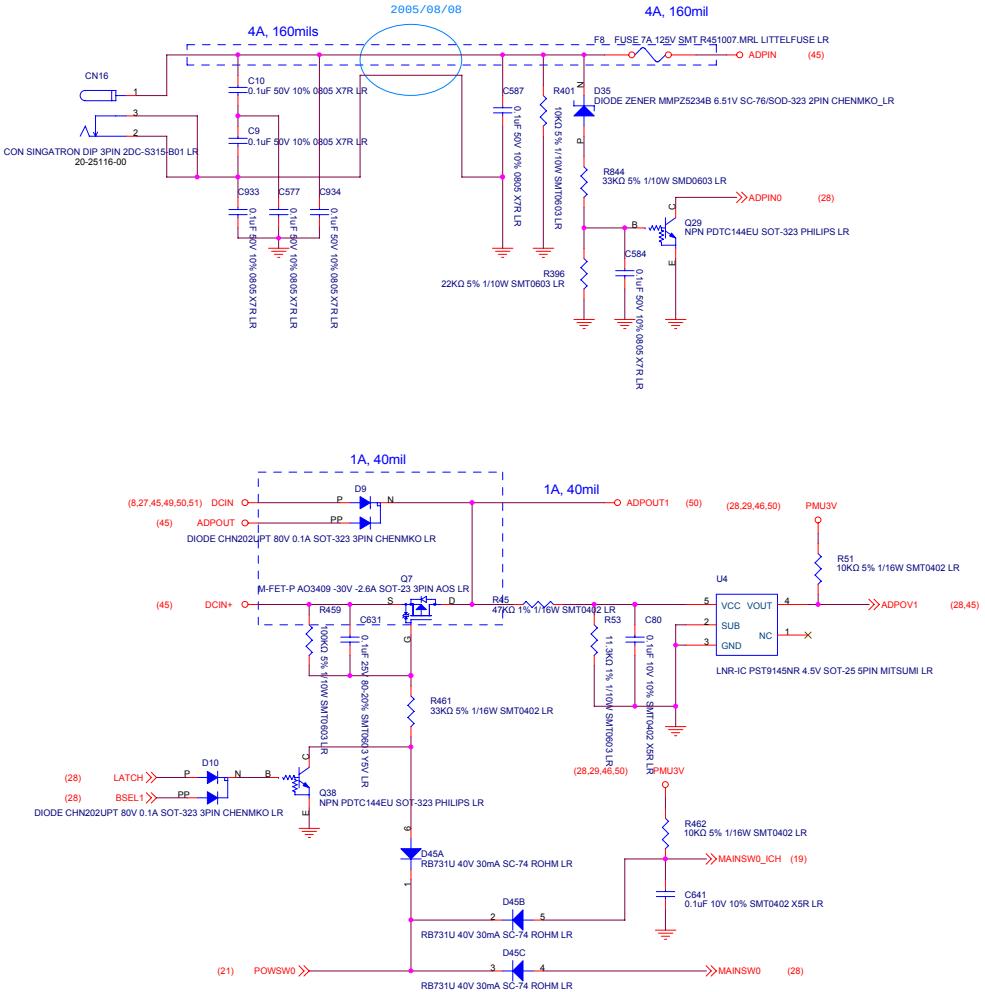
Title	Battery Voltage Sense	
Size C	Document Number KR2W < AMD K8 + RS482M + SB450 >	Rev 0.1
Date: Tuesday, August 16, 2005	Sheet 46 of 54	



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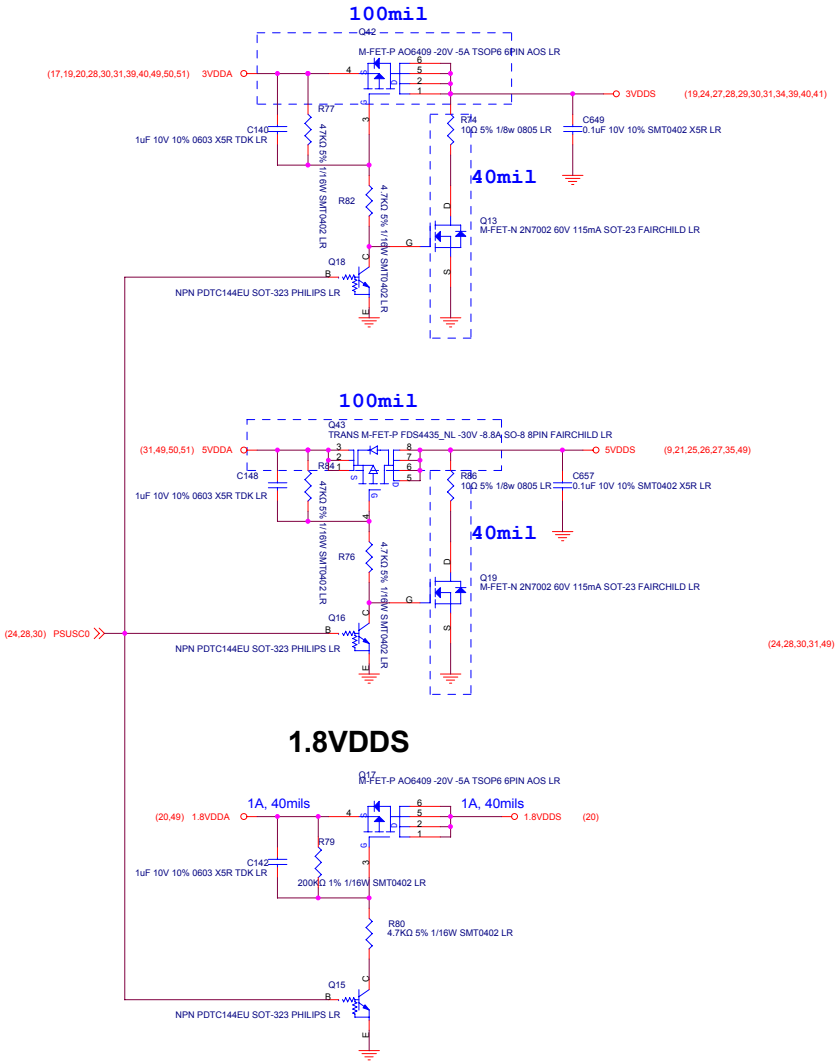
Title: **PMU3V / PMU5V**

Size	Document Number	Rev
C	KR2W < AMD K8 + RS482M + SB450 >	0.1

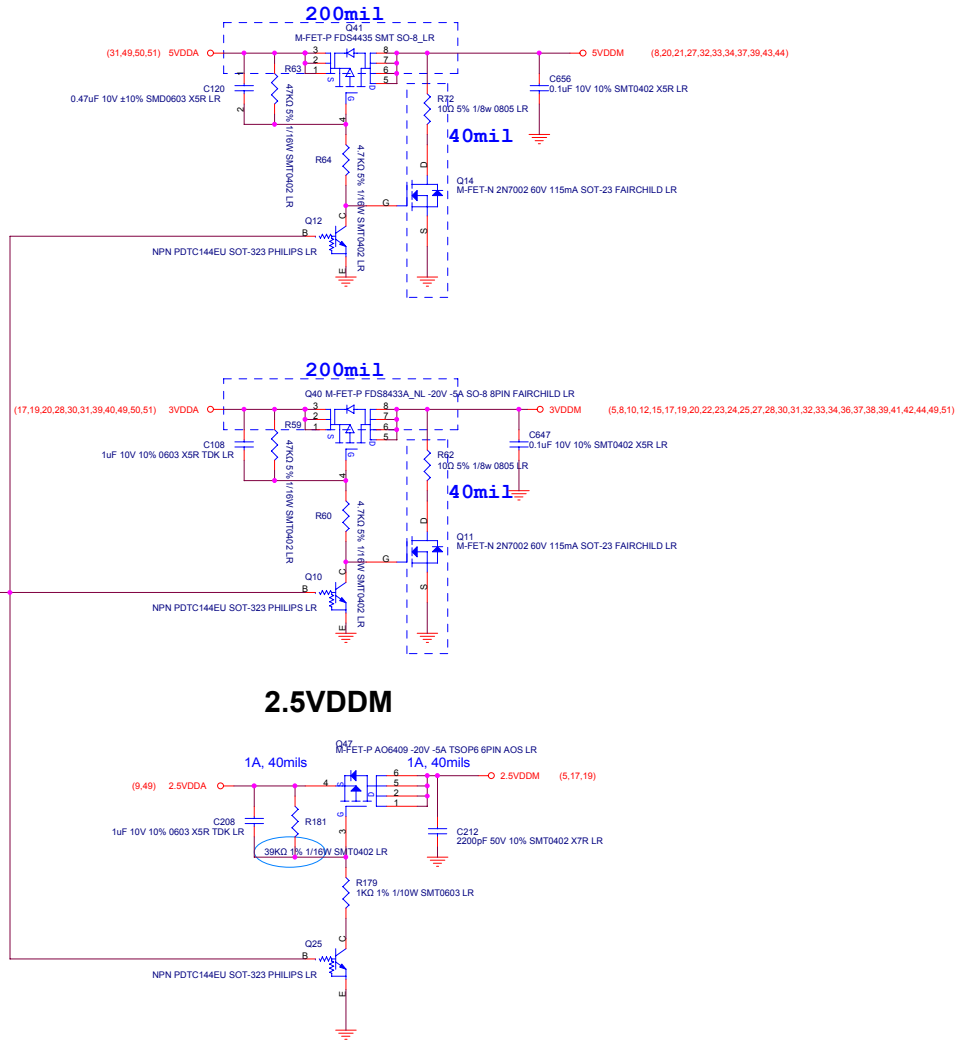
Date: Tuesday, August 16, 2005 Sheet 47 of 54

3VDDS/5VDDS



1.8VDDS

3VDDM/5VDDM



2.5VDDM

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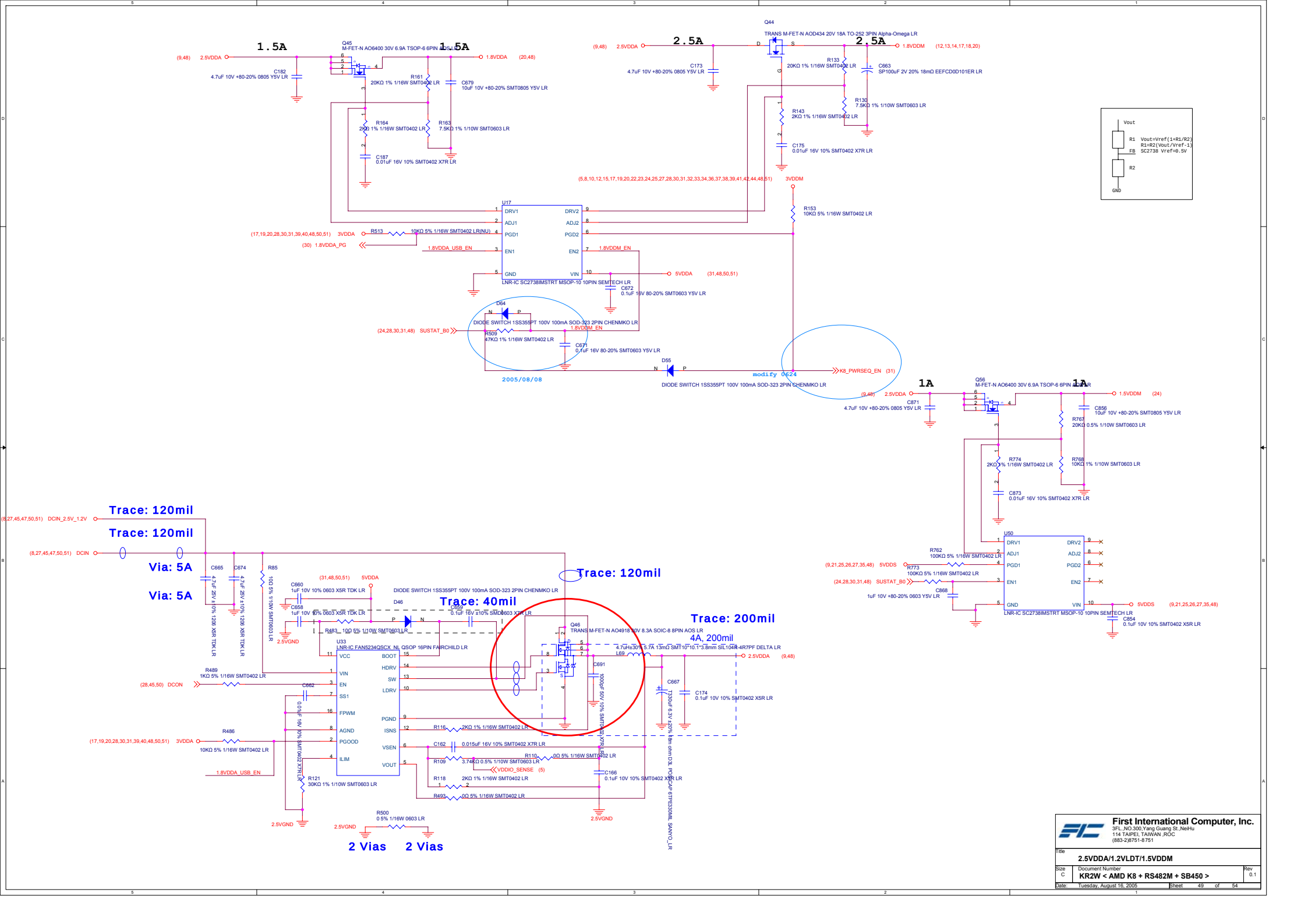
Title	3V, 5V, 2.5VDDS/M
Size C	Document Number: KR2W < AMD K8 + RS482M + SB450 >
Rev	0.1
Date:	Tuesday, August 16, 2005
Sheet	48 of 54


1.5A
Q45
M-FET-N AO6400 30V 6.9A TSOP-6 6PIN ALPHA&OMEGA LR
(9,48) 2.5VDDA
1.8VDDA (20,48)
C182
4.7uF 10V +80-20% 0805 Y5V LR
R161
20KΩ 1% 1/16W SMT0402 LR
C679
10uF 10V +80-20% SMT0805 Y5V LR
R164
2KΩ 1% 1/16W SMT0402 LR
R163
7.5KΩ 1% 1/10W SMT0603 LR
C187
0.01uF 16V 10% SMT0402 X7R LR
2.5A
Q44
TRANS M-FET-N AOD434 20V 18A TO-252 3PIN Alpha-Omega LR
(9,48) 2.5VDDA
1.8VDDM (12,13,14,17,18,20)
C173
4.7uF 10V +80-20% 0805 Y5V LR
R133
20KΩ 1% 1/16W SMT0402 LR
C663
SP100uF 2V 20% 18mΩ EEFCD0D101ER LR
R130
7.5KΩ 1% 1/10W SMT0603 LR
R143
2KΩ 1% 1/16W SMT0402 LR
C175
0.01uF 16V 10% SMT0402 X7R LR
Vout
R1 Vout=Vref(1+R1/R2)
FB R1=R2(Vout/Vref-1)
SC2738 Vref=0.5V
R2
GND
(5,8,10,12,15,17,19,20,22,23,24,25,27,28,30,31,32,33,34,36,37,38,39,41,42,44,48,51) 3VDDM
U17
DRV1
ADJ1
PGD1
EN1
GND
DRV2
ADJ2
PGD2
EN2
VIN
R153
10KΩ 5% 1/16W SMT0402 LR
(17,19,20,28,30,31,39,40,48,50,51) 3VDDA
R513
10KΩ 5% 1/16W SMT0402 LR(NU)
(30) 1.8VDDA_PG
1.8VDDA_USB_EN
1.8VDDM_EN
5VDDA (31,48,50,51)
LNR-IC SC2738IMSTRT MSOP-10 10PIN SEMTECH LR
C672
0.1uF 16V 80-20% SMT0603 Y5V LR
D64
DIODE SWITCH 1SS355PT 100V 100mA SOD-323 2PIN CHENMKO LR
(24,28,30,31,48) SUSTAT_B0
R509
47KΩ 1% 1/16W SMT0402 LR
C671
0.1uF 16V 80-20% SMT0603 Y5V LR
2005/08/08
D55
DIODE SWITCH 1SS355PT 100V 100mA SOD-323 2PIN CHENMKO LR
modify 0624
K8_PWRSEQ_EN (31)
1A
Q56
M-FET-N AO6400 30V 6.9A TSOP-6 6PIN ALPHA&OMEGA LR
(9,48) 2.5VDDA
1.5VDDM (24)
C871
4.7uF 10V +80-20% 0805 Y5V LR
C856
10uF 10V +80-20% SMT0805 Y5V LR
R767
20KΩ 0.5% 1/10W SMT0603 LR
R774
2KΩ 1% 1/16W SMT0402 LR
R768
10KΩ 1% 1/10W SMT0603 LR
C873
0.01uF 16V 10% SMT0402 X7R LR
U50
DRV1
ADJ1
PGD1
EN1
GND
DRV2
ADJ2
PGD2
EN2
VIN
R762
100KΩ 5% 1/16W SMT0402 LR
(9,21,25,26,27,35,48) 5VDDS
R773
100KΩ 5% 1/16W SMT0402 LR
(24,28,30,31,48) SUSTAT_B0
C868
1uF 10V +80-20% 0603 Y5V LR
LNR-IC SC2738IMSTRT MSOP-10 10PIN SEMTECH LR
C854
0.1uF 10V 10% SMT0402 X5R LR
Trace: 120mil
(8,27,45,47,50,51) DCIN_2.5V_1.2V
Trace: 120mil
(8,27,45,47,50,51) DCIN
Via: 5A
Via: 5A
C665
4.7uF 25V ±10% 1206 X5R TDK LR
C674
4.7uF 25V ±10% 1206 X5R TDK LR
R85
100 5% 1/10W SMT0603 LR
(31,48,50,51) 5VDDA
C660
1uF 10V 10% 0603 X5R TDK LR
C658
1uF 10V 10% 0603 X5R TDK LR
2.5VGND
D46
DIODE SWITCH 1SS355PT 100V 100mA SOD-323 2PIN CHENMKO LR
C659
0.1uF 16V ±10% SMD0603 X7R LR
R483 10Ω 5% 1/10W SMT0603 LR
Trace: 40mil
Trace: 120mil
Trace: 200mil
4A, 200mil
Q46
TRANS M-FET-N AO4918 30V 8.3A SOIC-8 8PIN AOS LR
4.7uH±30% 5.7A 13mΩ SMT10*10.1*3.8mm SIL1041R-4R7PF DELTA LR
L69
2.5VDDA (9,48)
C691
4700uF 20V 10% SMT0252 20R LR
C667
T330uF 6.3V 420% 18m ohm D3L POSCAP 6TPE330ML SANYO_LR
C174
0.1uF 10V 10% SMT0402 X5R LR
U33
LNR-IC FAN5234QSCX_NL QSOP 16PIN FAIRCHILD LR
VCC
VIN
EN
SS1
FPWM
AGND
PGOOD
ILIM
BOOT
HDRV
SW
LDRV
PGND
ISNS
VSEN
VOUT
R489
1KΩ 5% 1/16W SMT0402 LR
(28,45,50) DCON
C662
0.01uF 16V 10% SMT0402 X7R LR
R486
10KΩ 5% 1/16W SMT0402 LR
(17,19,20,28,30,31,39,40,48,50,51) 3VDDA
1.8VDDA_USB_EN
R121
30KΩ 1% 1/10W SMT0603 LR
R116
2KΩ 1% 1/16W SMT0402 LR
C162
0.015uF 16V 10% SMT0402 X7R LR
R109
3.74KΩ 0.5% 1/10W SMT0603 LR
R110
0Ω 5% 1/16W SMT0402 LR
VDDIO_SENSE (5)
R118
2KΩ 1% 1/16W SMT0402 LR
R493
0Ω 5% 1/16W SMT0402 LR
C166
0.1uF 10V 10% SMT0402 X5R LR
2.5VGND
R500
0 5% 1/16W 0603 LR
2 Vias
2 Vias
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Title
2.5VDDA/1.2VLDT/1.5VDDM
Size C
Document Number
KR2W < AMD K8 + RS482M + SB450 >
Rev 0.1
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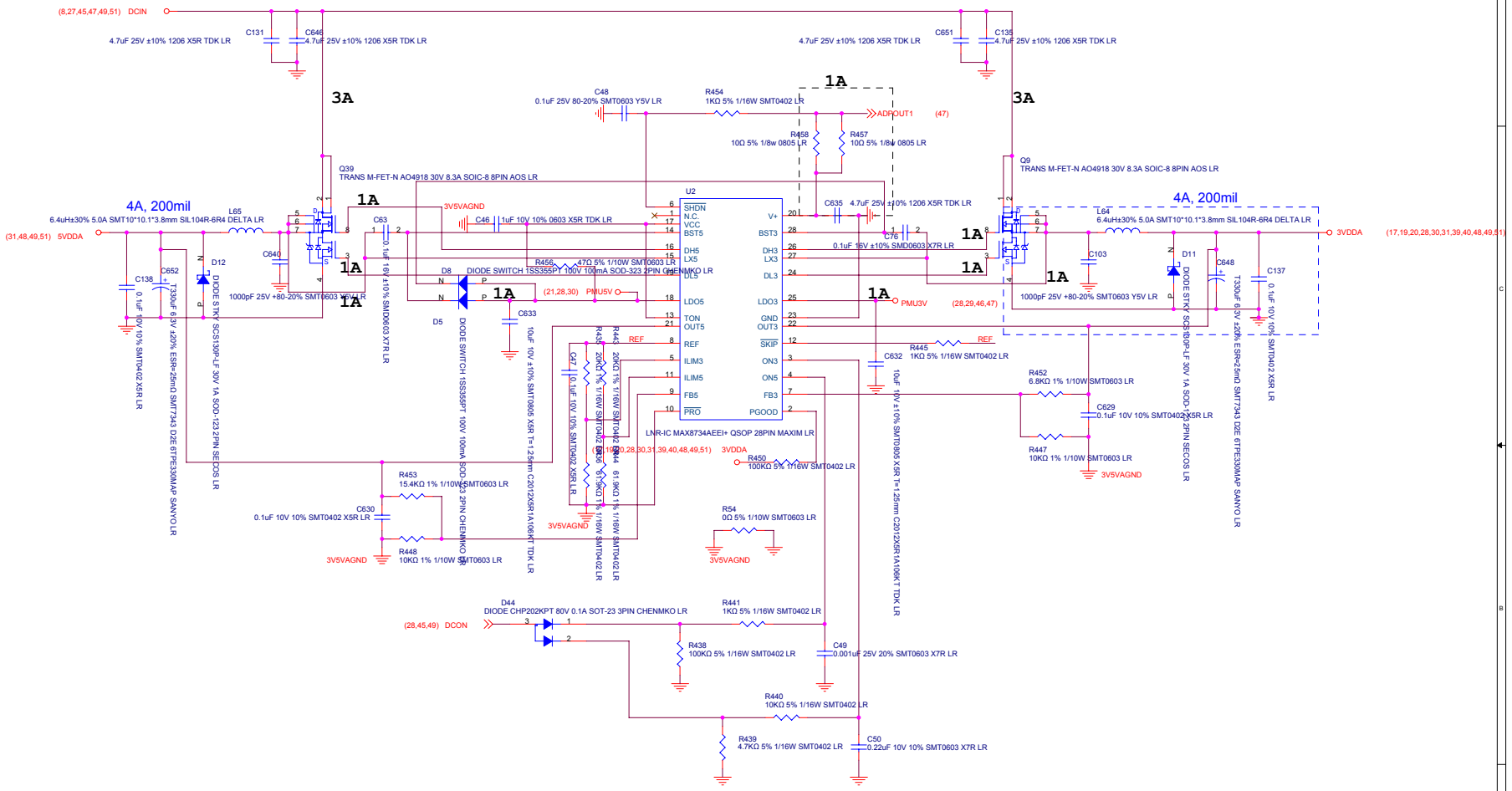

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Title	5VDDA/3VDDA	
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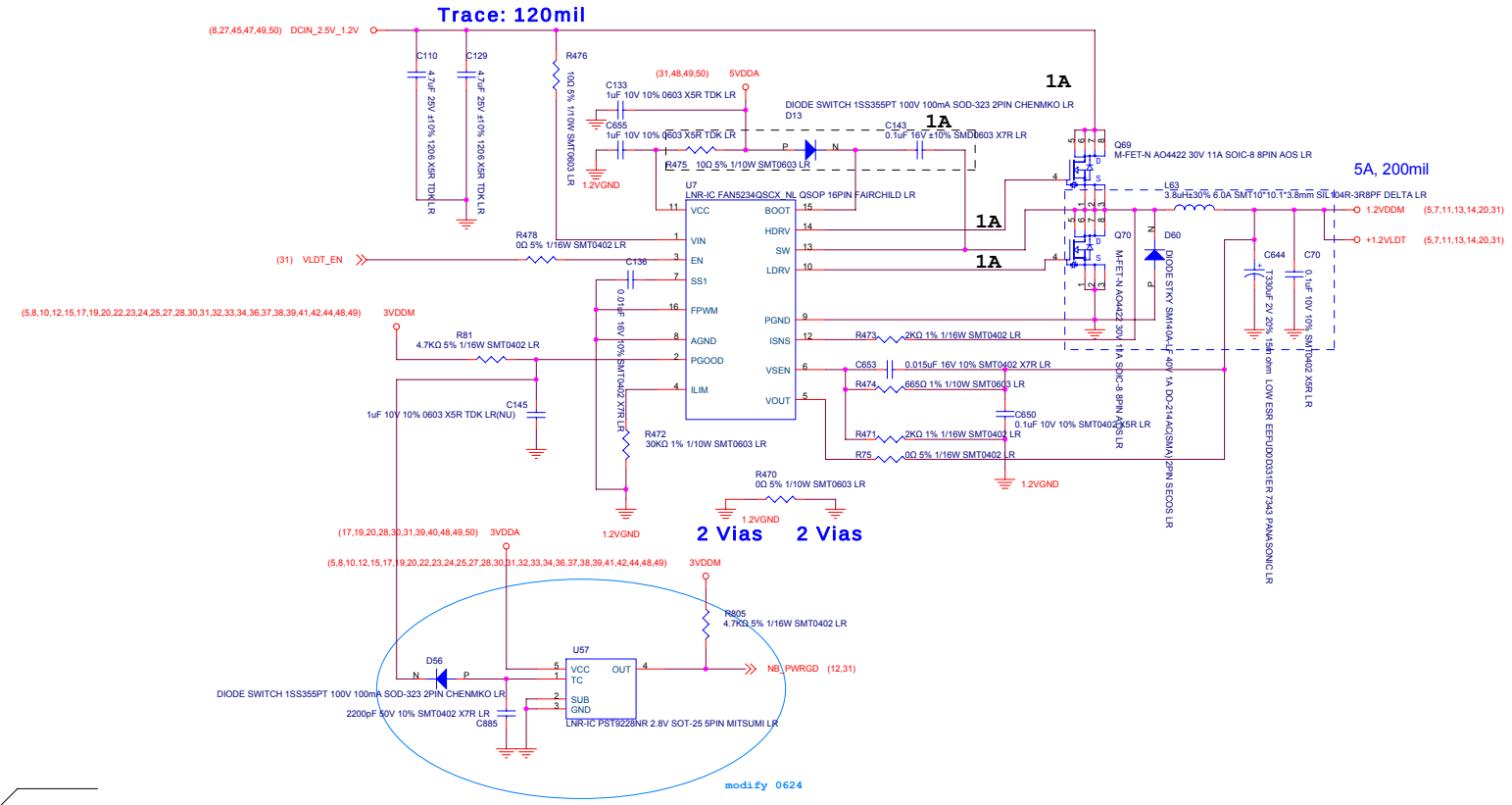
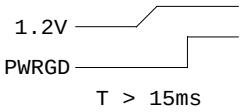
N.B. Core Power and Hypertransport Power





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Title: NB_CORE/HT POWER

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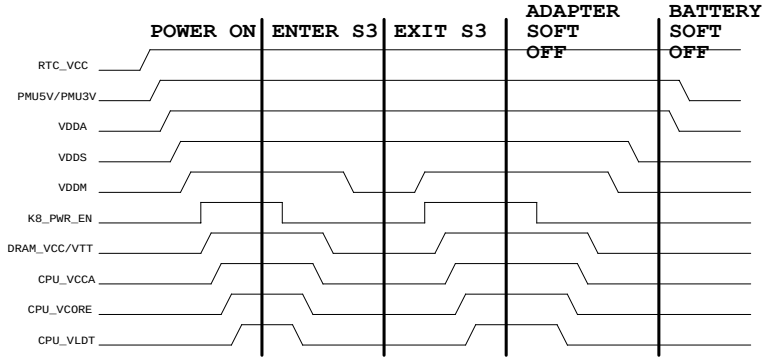
SYSTEM POWER SEQUENCE

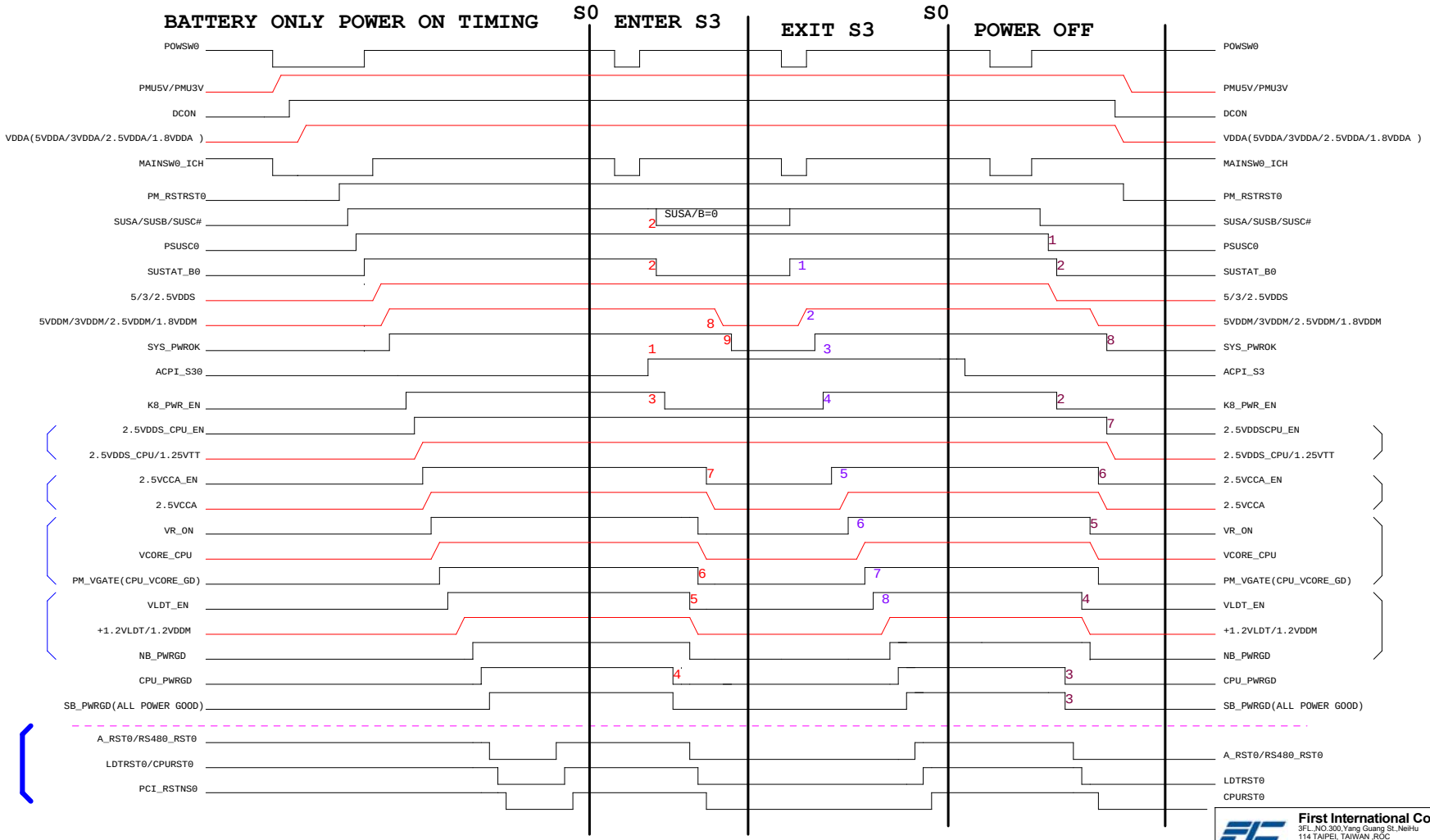
VCC USE

SIGNAL

STEP 1 2



BATTERY ONLY POWER ON TIMING



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Title: Timming

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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6.Schematic modify Item and History :

	BUG	ROOT CAUSE	SOLUTION	PHASE IN
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				

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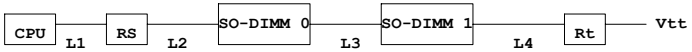
Title: Schematic History

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

Date: Tuesday, August 16, 2005 | Sheet 53 of 54

1 DDR SODIMM LAYOUT GUIDE

1. DATA GROUP TOPOLOGY



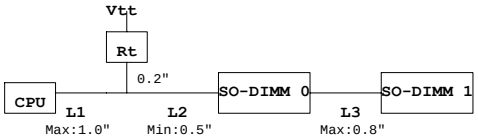
	L1	L2	L3	L4
Signals	1.0~3.00"	Max:1.0"	Max:0.8"	Max:1.5"

M_D[63..0]
M_DM[7..0]
M_DQS[7..0]

NOTE
L1 + L2 < CLK - 1"

GROUP A	GROUP B	GROUP C	NOTE
M_D[7..0]	M_DM0	M_DQS0	* Group A & Group B & Group C Mismatch must be within 25 mils (Total Length)
M_D[15..8]	M_DM1	M_DQS1	* The same Group must be routed in the same layer
M_D[23..16]	M_DM2	M_DQS2	
M_D[31..24]	M_DM3	M_DQS3	* M_DQS[16..0] 5mil trace , 20 mil space M_D[63..0],M_DM[7..0] 5mil trace , 15 mil space
M_D[39..32]	M_DM4	M_DQS4	
M_D[47..40]	M_DM5	M_DQS5	
M_D[55..48]	M_DM6	M_DQS6	
M_D[63..56]	M_DM7	M_DQS7	* M_DQS & M_CLK mismatch within 0.5"

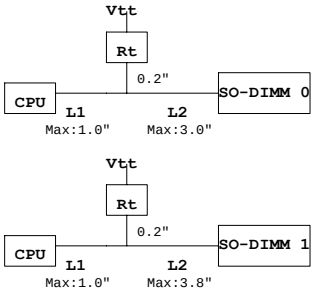
2. ADDRESS/COMMAND GROUP TOPOLOGY



Signals

M_A_SR[13..0]	**NOTE** **L1 + L2 < CLK - 1"**
MB_A_SR[13..0]	
M_BANK0_SR0 , M_BANK1_SR0	* Trace Width 5 mils , Spacing 15 mils
MB_BANK0_SR0 , MB_BANK1_SR0	
M_WE_SR0 , MB_WE_SR0	
M_CAS_SR0 , MB_CAS_SR0	
M_RAS_SR0 , MB_RAS_SR0	

3. ADDRESS/COMMAND GROUP 2 TOPOLOGY



Signals

M_CS0_R0	**NOTE** **L1 + L2 < CLK - 1"**
M_CS1_R0	* Trace Width 5 mils , Spacing 15 mils
M_CS2_R0	
M_CS3_R0	

2 Signal Layout Guide

Signal Group	Maxium Length	Trace Property Normal (Width : Space) Differential(S :W:S: W: S)
Hyper Transport Bus	8"	15:5:5:5:15
A_Link Bus	12"	20:5:8:5:20(MS) 20:4:8:4:20(SL)
LVDS BUS	3"	20:5:8:5:20(MS) 20:4:8:4:20(SL)
USB Data	8"	20:5:5:5:20(MS) 20:4:5:4:20(SL)
1394 Bus	8"	20:4:8:4:20(MS) 20:4:12:4:20(SL)
SATA Bus	8"	20:5:8:5:20(MS) 20:4:8:4:20(SL)
PCI / Card / LPC Bus	8"	5:7(MS) 4:6(SL)
IDE Bus	8"	5:7(MS) 4:6(SL)
Clock 66M/33M Hz	6"	5:20(MS) 4:20(SL)

* Differential Signal Layout Should Be The Same Length

For Example :

LVDS_TXCLK_LP & LVDS_TXCLK_LN
USB20_P0+ & USB20_P0-

Should Be The Same Length ASAP

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Title: LAYOUT DESIGN GUIDE

Size: C | Document Number: KR2W < AMD K8 + RS482M + SB450 > | Rev: 0.1

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