XPCAM Project

UNIC-CASS - Mock tapeout report

February 19, 2026

Contents

XPCAM Macro

1.1 Processing unit

The processing unit is a single n-bit content-addressable memory row.

1.1.1 Cell

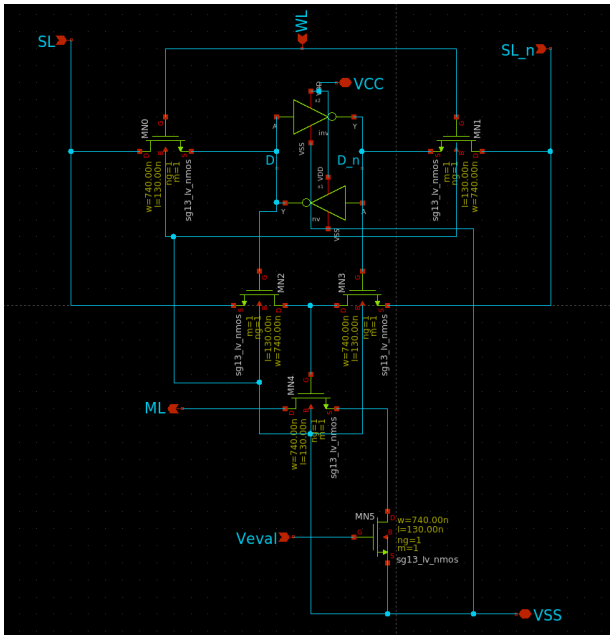

FIGURE 1.1
Cell schematic

1.1.2 Input/Output/Write Circuitry

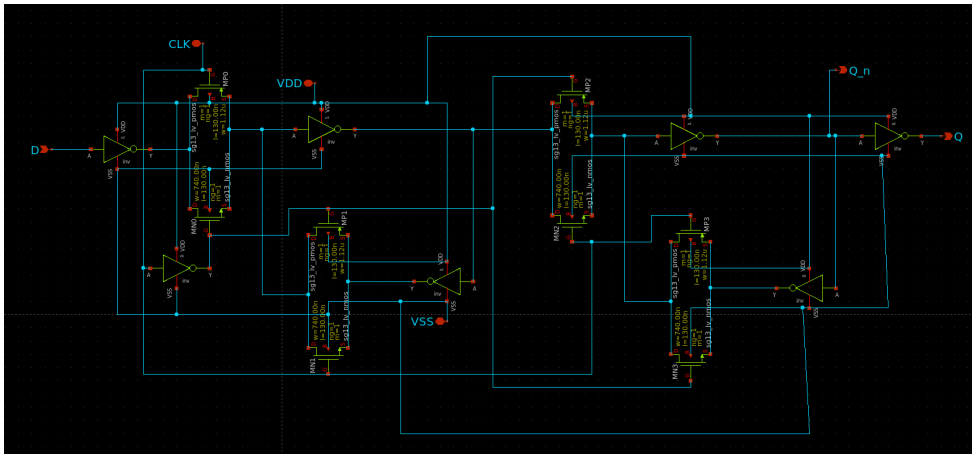

FIGURE 1.2
Schematic of Type-D Flip Flop for Input/output/write circuitry

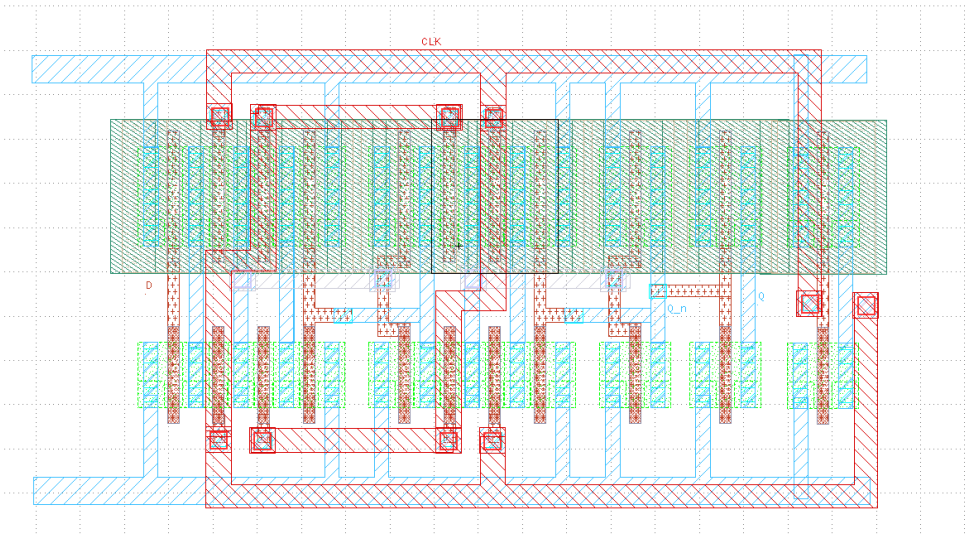

FIGURE 1.3
Layout of Type-D Flip Flop for Input/output/write circuitry

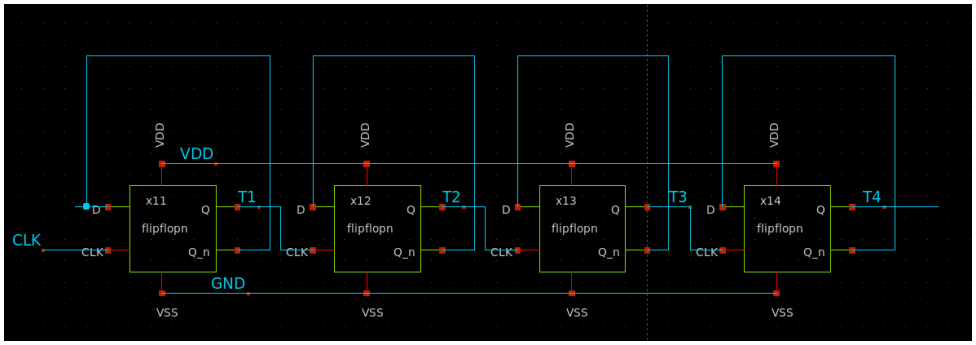

FIGURE 1.4
Schematic of 8 bit Counter

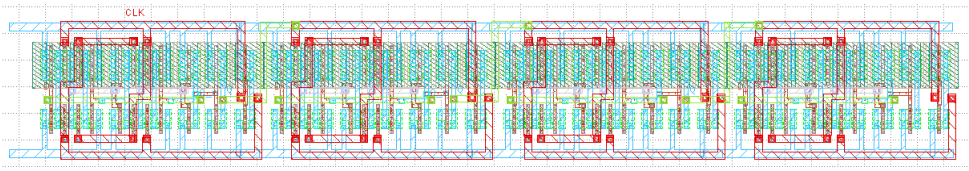

FIGURE 1.5
layout of 8 bit Counter

1.1.3 Sense amplifier

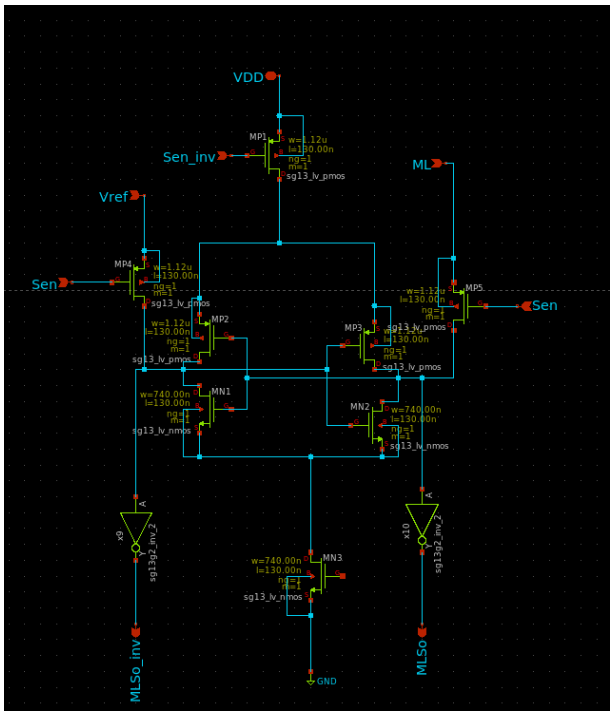

FIGURE 1.6
Sense amplifier circuit

1.2 Layout & Macro Information

1.2.1 XPCAM Pin Information

The pin information is shown below. Note: the 'rst', 'cen' pins could be optional.

Pin Name	Type	Description
VDD	Power	
VSS	Ground	
Veval	Analog	
Vref	Analog	reference voltage of SA
Vsample	Analog	move sample time
enpim	digital input	enable XNOR+POPCOUNT
sdin	digital input	Serial data in
wen	digital input	write enable
cen	digital input	clock enable (of registers)
rst	digital input	reset (of registers)
out	digital output	output

TABLE 1.1
Pin information

1.2.2 Layout Status

The layout was created from the provided analog pad ring wrapper. We worked in KLayout 0.30.01 with the IHP SG13G2 PDK installed and used the SG13_dev–IHP SG13G2 Pcells library to instantiate the devices. With these PCells, we built a simple bitcell-like structure and routed it at the layout level. This block was then inserted into the wrapper and connected to the analog_io1 pad as a frist "proof of concept". The goal was to verify that the basic flow from device creation to pad-ring connection works correctly for the mock tapeout.

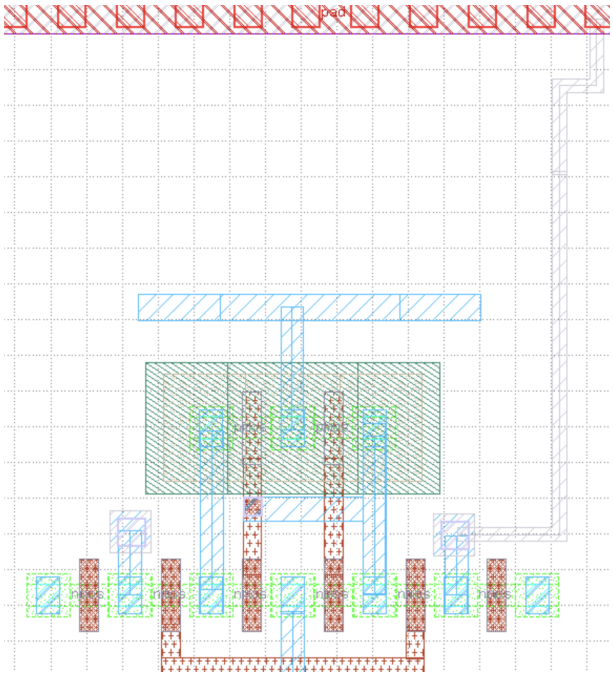

FIGURE 1.7
Layout (work in progress) of the cell using KLayout