

# **TEMA PROIECT BTME2**

**PROIECT NR. 2**

**BLAGA EDUARD GABRIEL**

**GRUPA 5413**

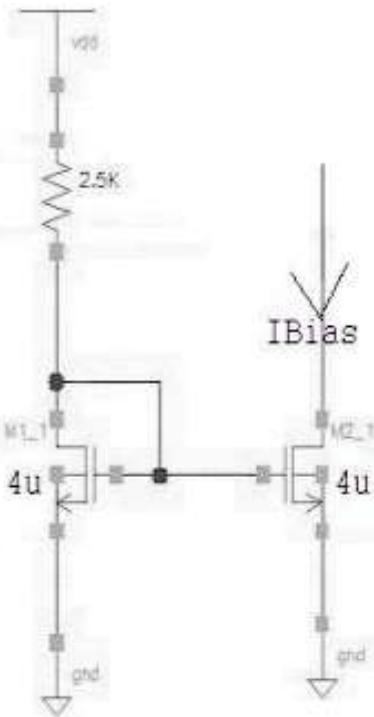
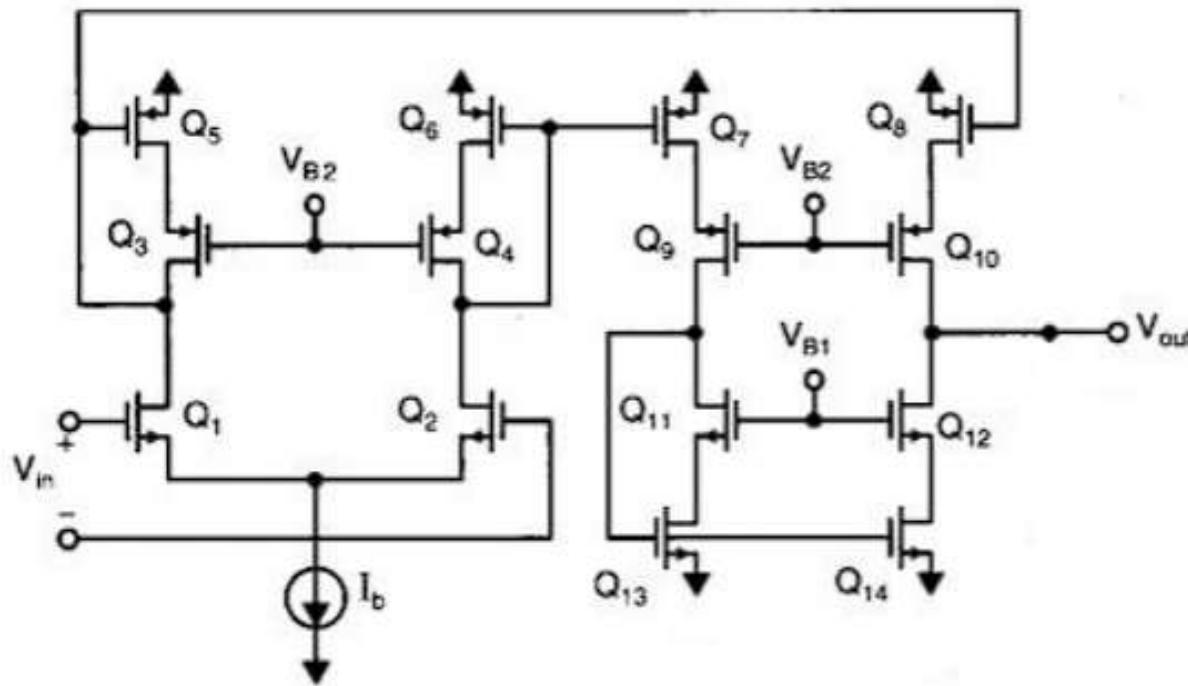
# CAPITOLUL 1 - SCHEMATIC

- STABILIREA GRUPARILOR TRANZISTOARELOR
- REALIZAREA MATCHINGULUI
- REALIZAREA SCHEMATICELOR

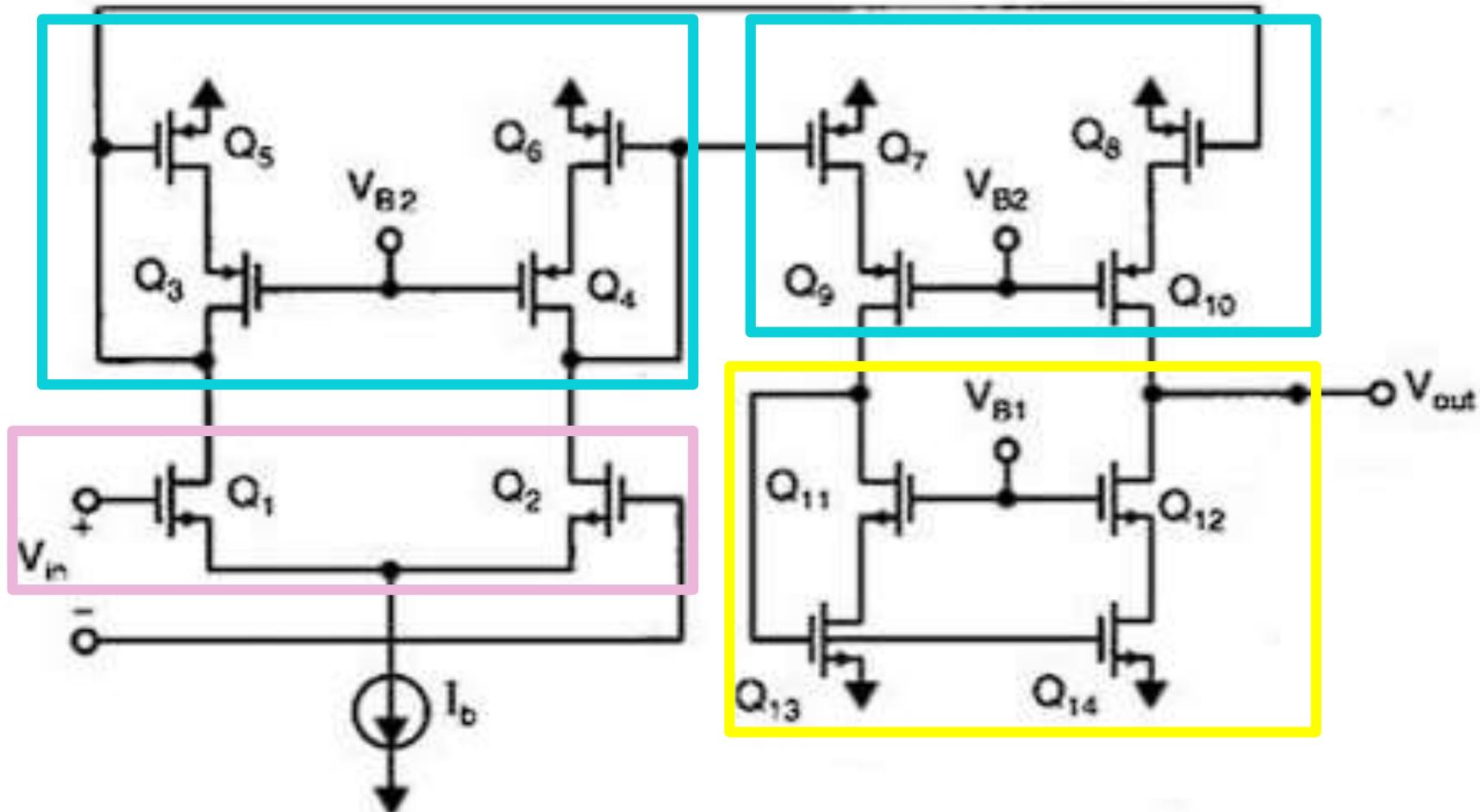
# SCHEMA CIRCUITULUI

## Proiect 2.

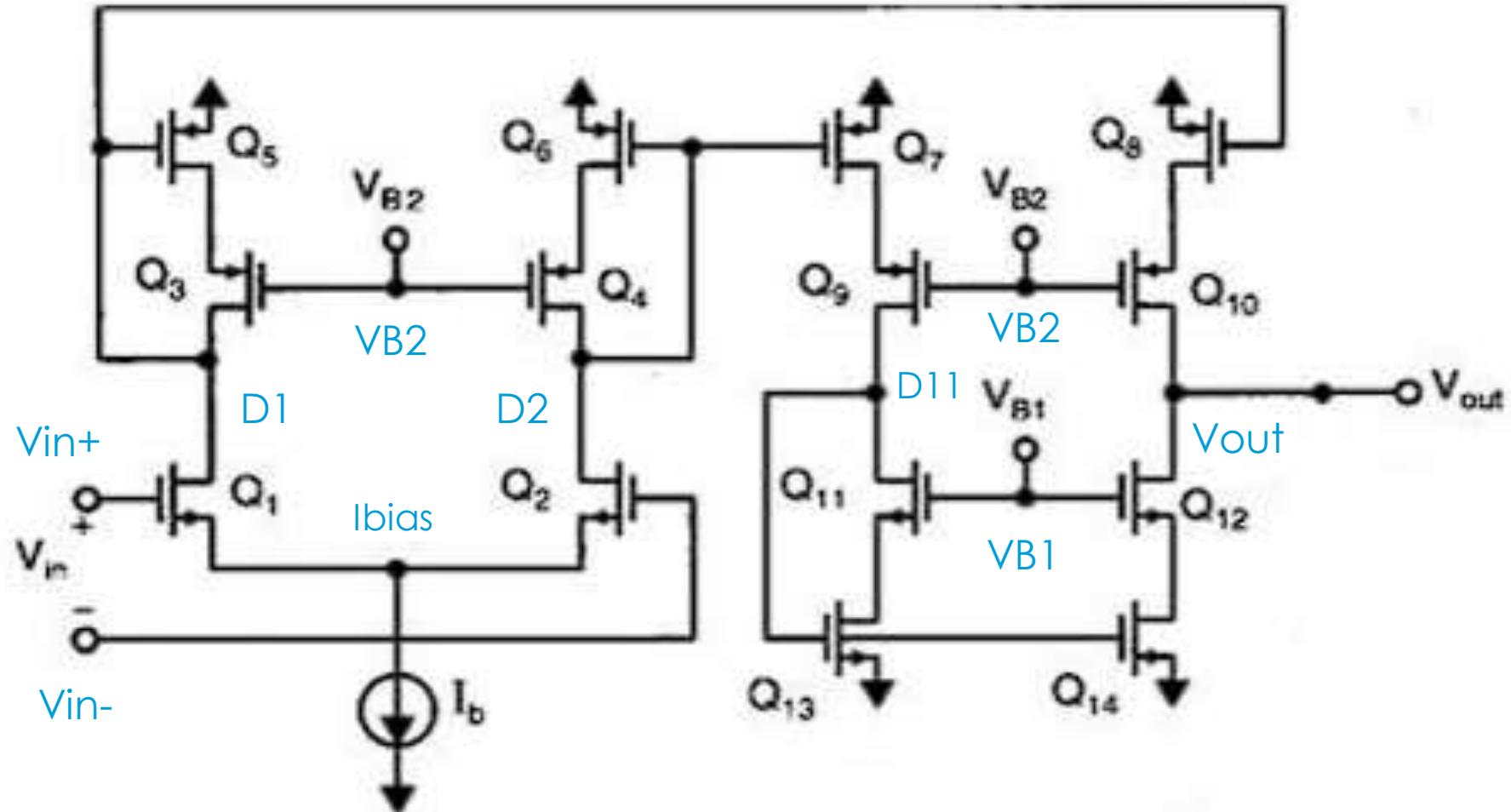
$L=0.9\mu$  și  $w_1=w_2=16\mu$ ,  $w_3=w_4=12\mu$   $w_5=w_6=w_7=w_8=10\mu$ ,  $w_9=w_{10}=8\mu$   $w_{11}=w_{12}=w_{13}=w_{14}=6\mu$   $I_{bias}$  ca în figură:



# STABILIREA GRUPARILOR



# CONEXIUNI INTERNE



# STABILIREA GRUPARILOR PENTRU LAYOUT

## 1. Bloc sarcina p

Blocul 1 format din Q3, Q4, Q5 si Q6 :  $12u + 12u + 10u + 10u = 44u$ ;  $+4Du(\text{Colturi}) +4Du(\text{interior}) = 52u$

Blocul 2 format din Q7, Q8, Q9 si Q10 :  $10u + 10u + 8u + 8u = 36u$ ;  $+4Du(\text{Colturi}) +4Du(\text{interior}) = 44u$

## 2. Etaj Diferential

Este format din Q1 si Q2 :  $16u + 16u = 32u$ ;  $+4Du(\text{Colturi}) = 36u$

## 3. Oglinda n

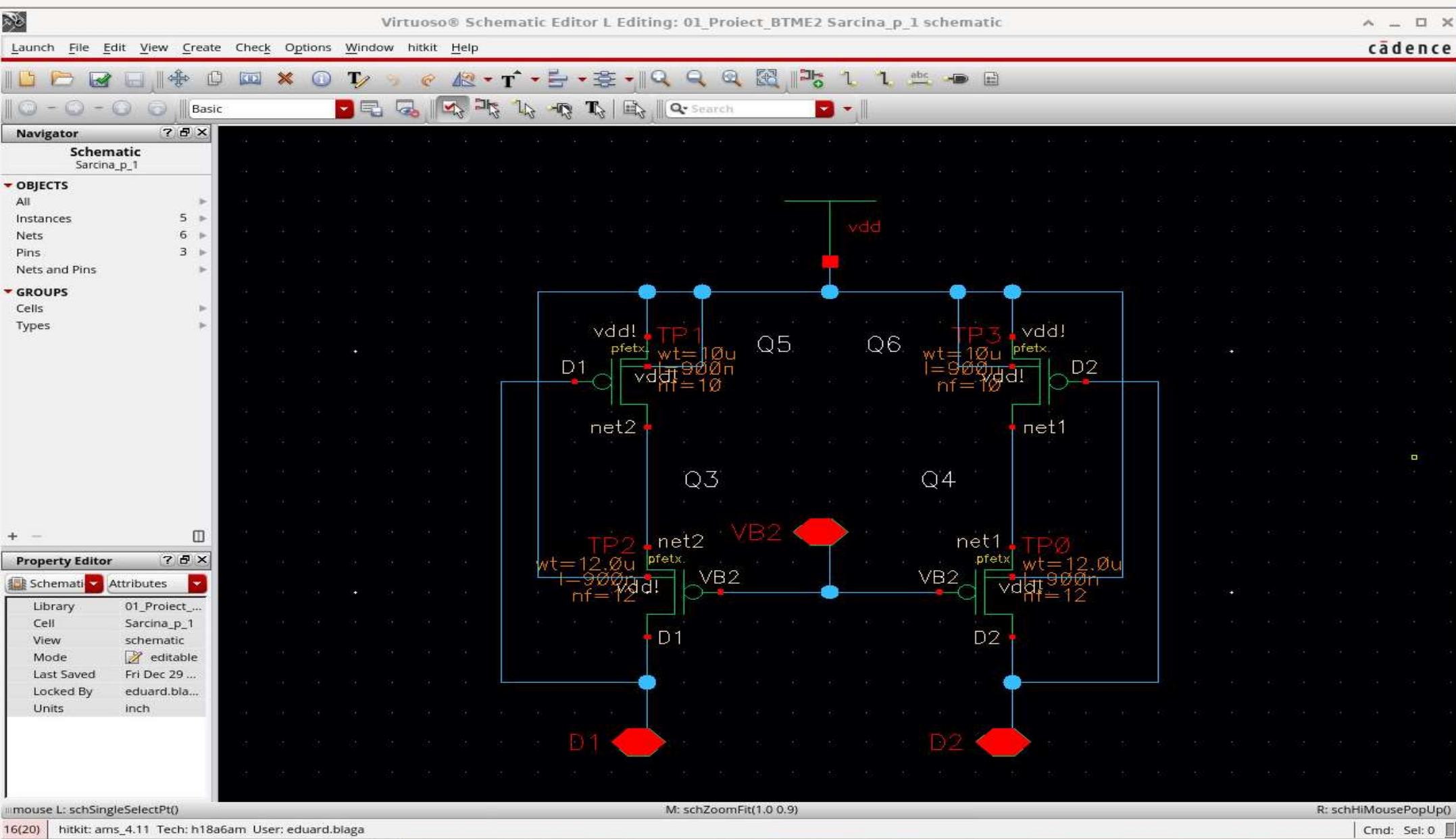
Este formata din Q11, Q12, Q13 si Q14 :  $6u + 6u + 6u + 6u = 24u$ ;  $+4Du(\text{Colturi}) +8Du(\text{Interior}) = 36u$

## 4. Sursa current Ibias

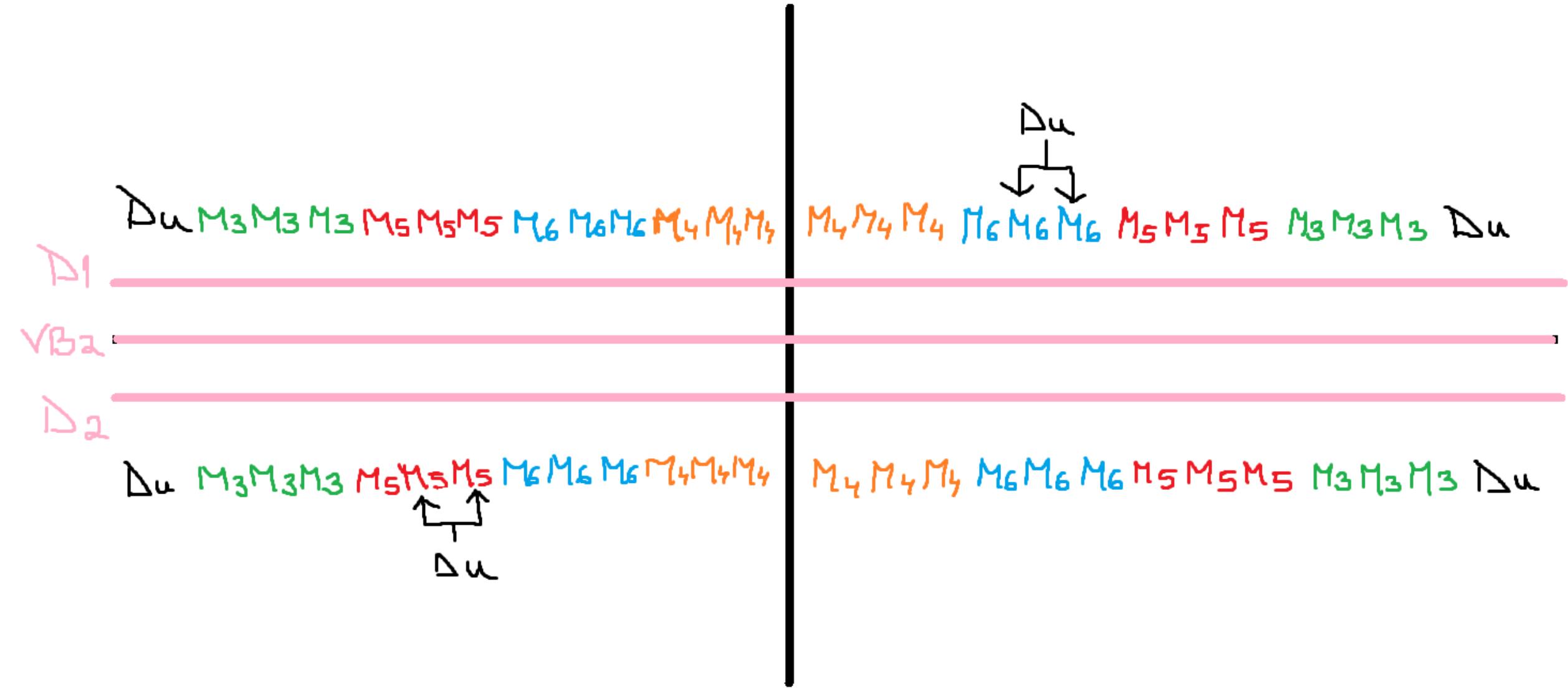
Este formata din M1 si M0 :  $4u + 4u = 8u$ ;  $+4Du(\text{Colturi}) = 12u$

# SARCINA P – BLOC 1 - SCHEMATIC

Fri 29 Dec, 15:27 Eduard-Gabriel BLAGA

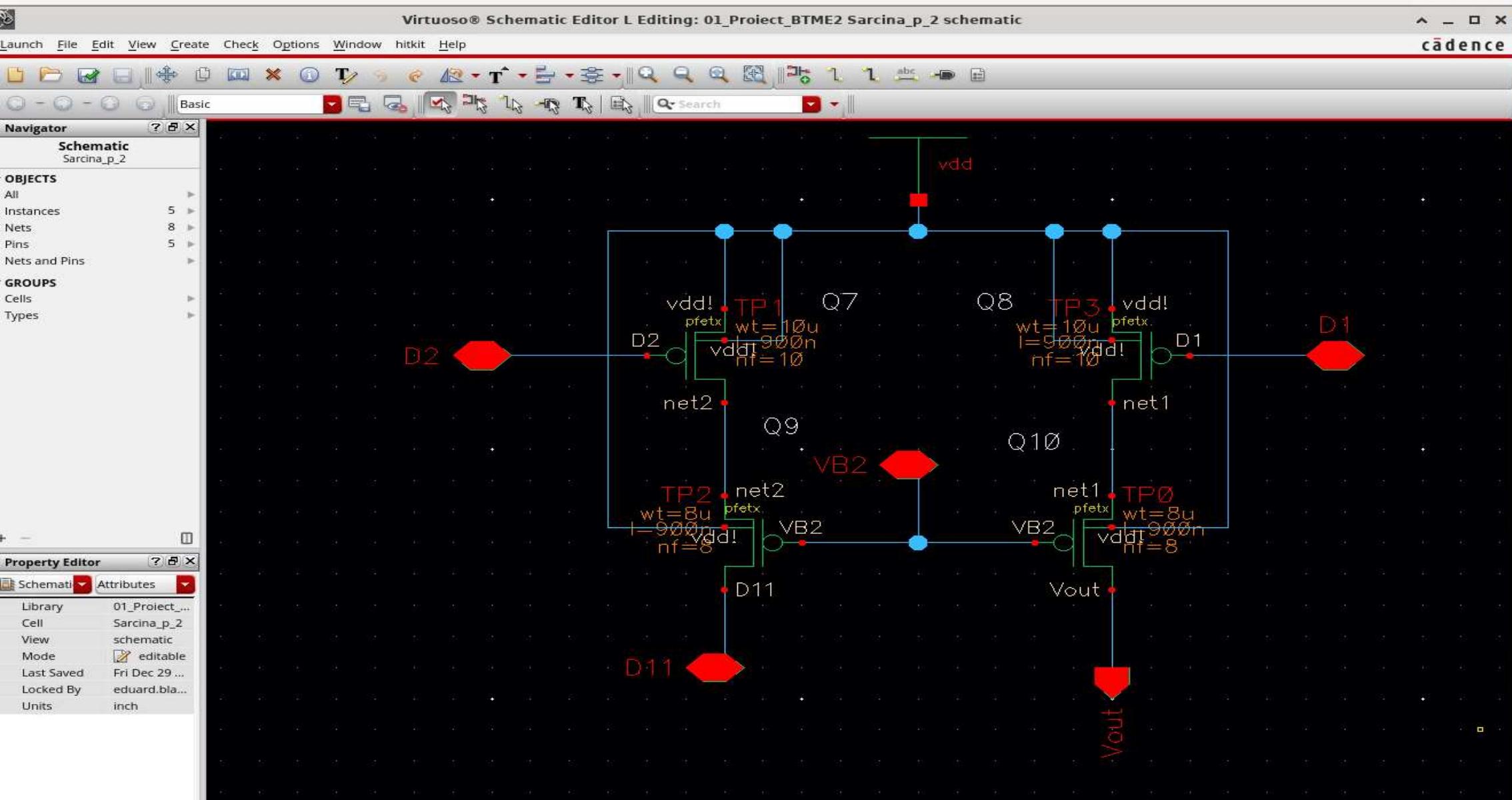


# MATCHING – SARCINA P – BLOC 1

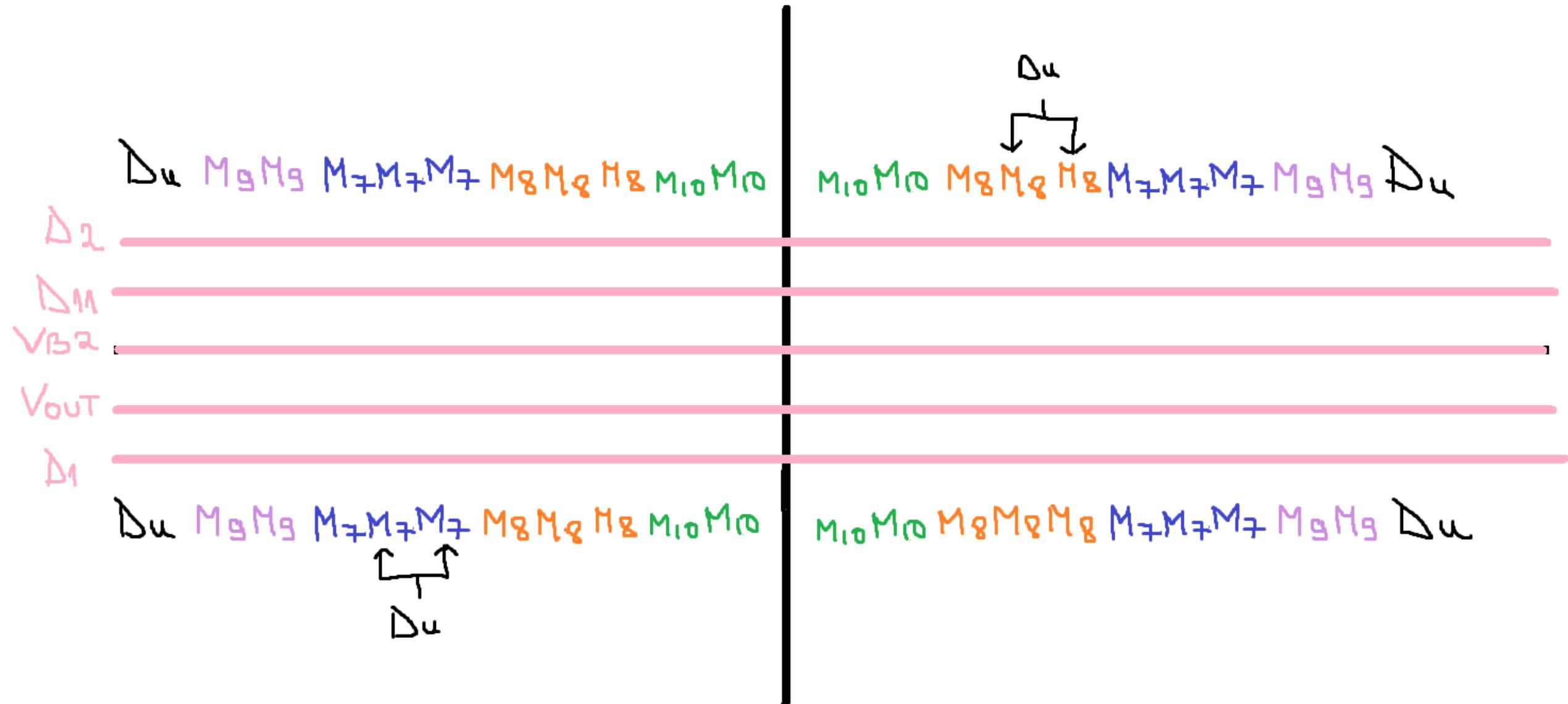


# SARCINA P – BLOC 2 - SCHEMATIC

Fri 29 Dec, 15:29 Eduard-Gabriel BLAGA

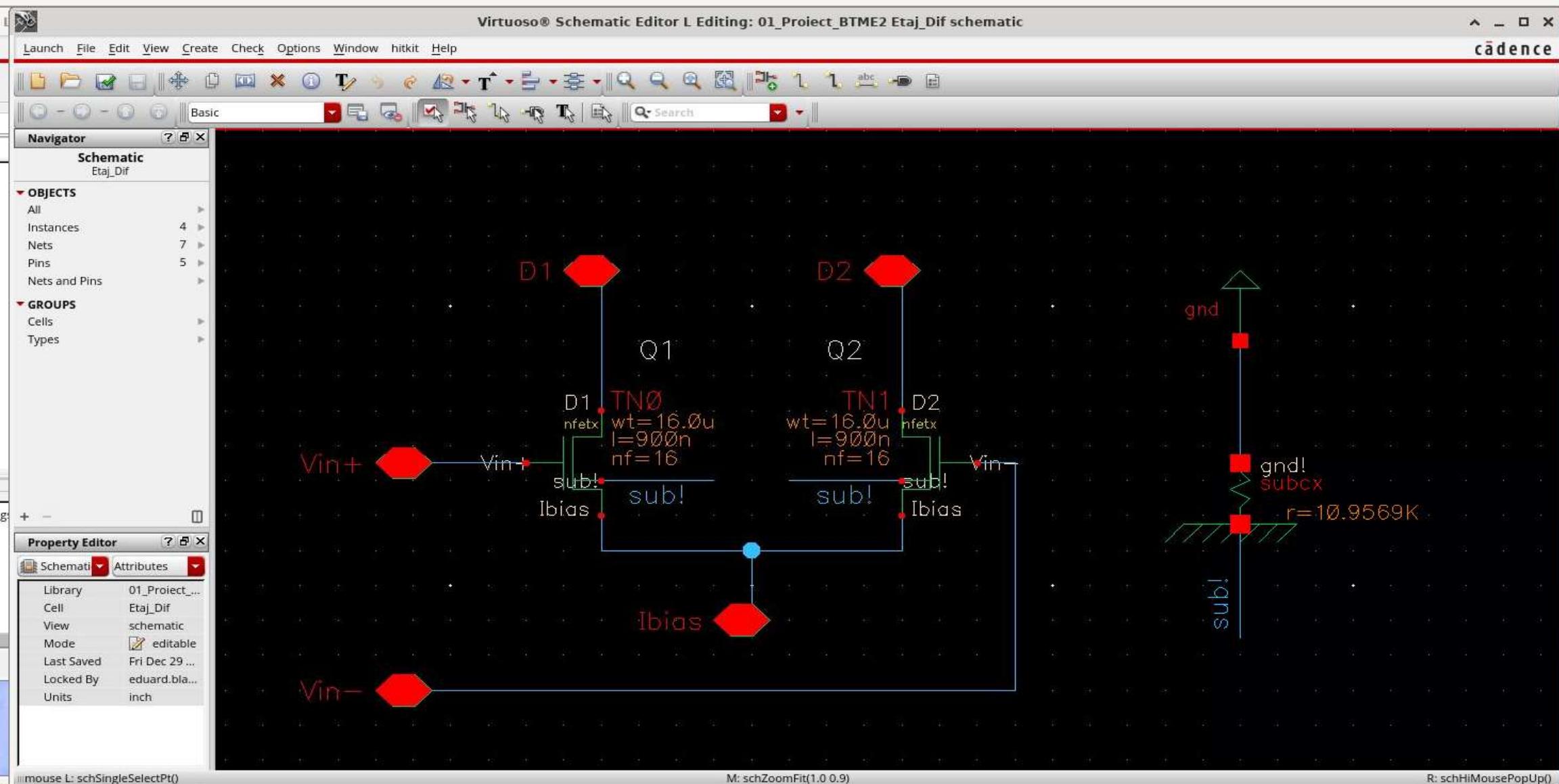


# MATCHING – SARCINA P – BLOC 2



# DIFERENTIAL - SCHEMATIC

Fri 29 Dec, 15:29 Eduard-Gabriel BLAGA

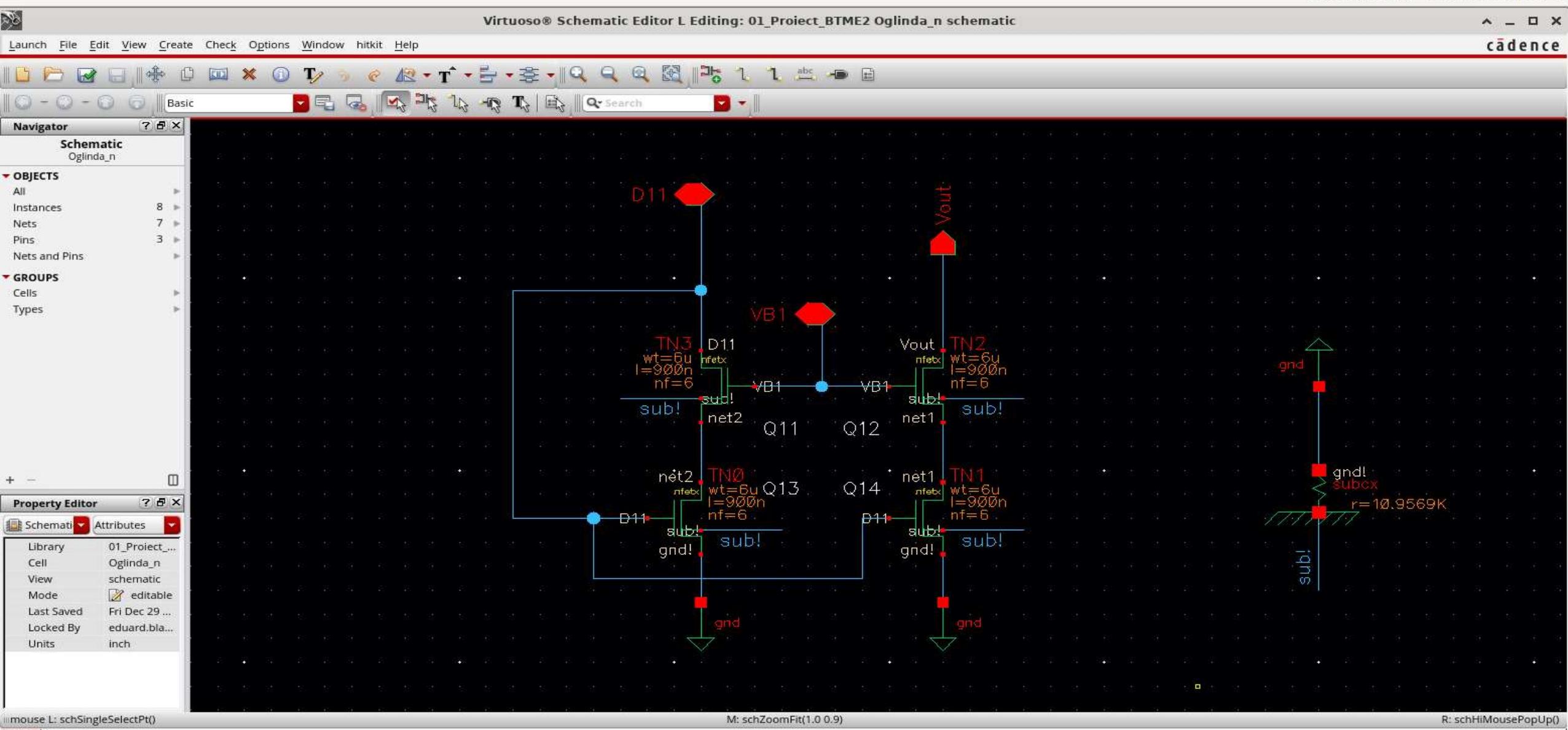


# MATCHING – DIFERENTIAL

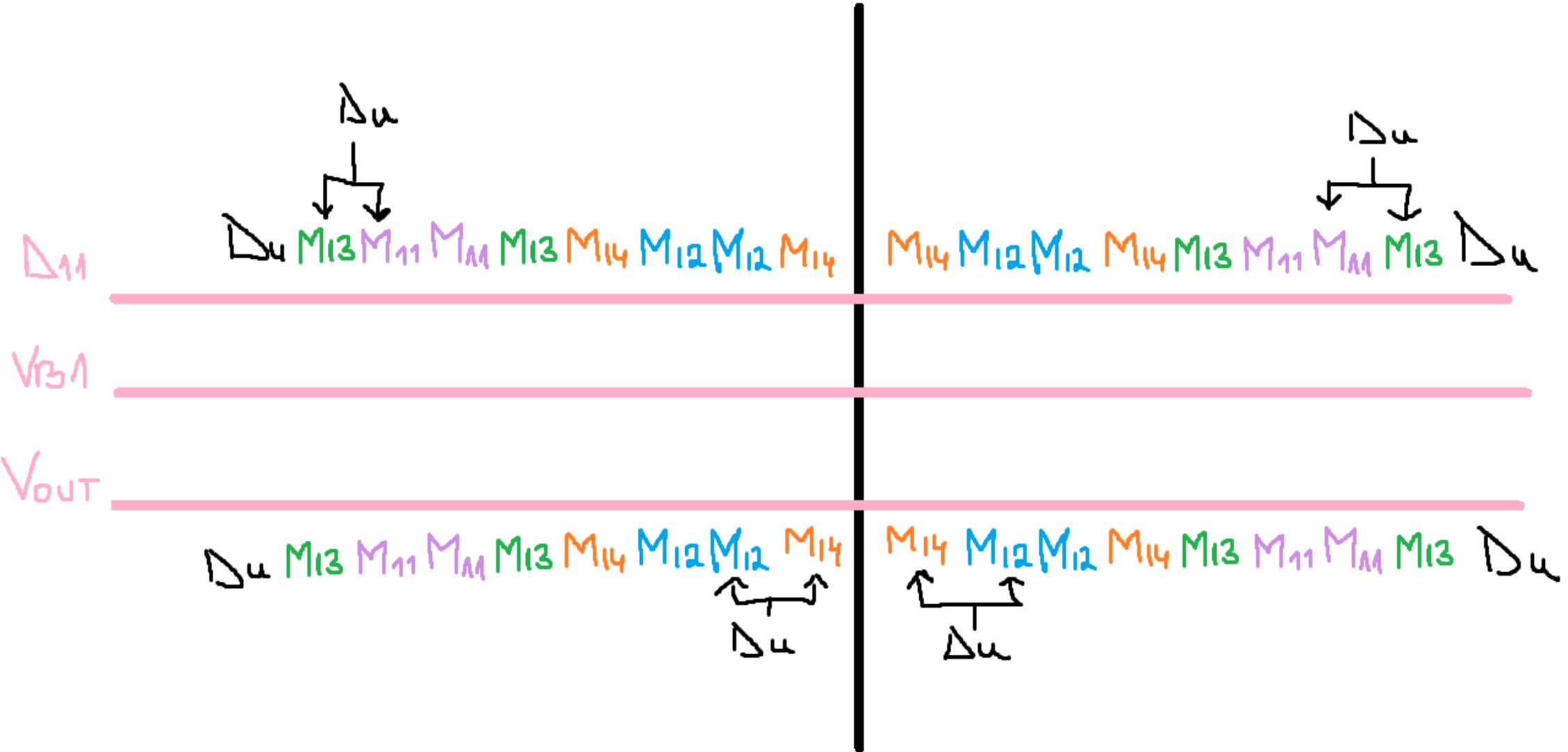


# OGLINDA N- SCHEMATIC

Fri 29 Dec, 15:30 Eduard-Gabriel BLAGA

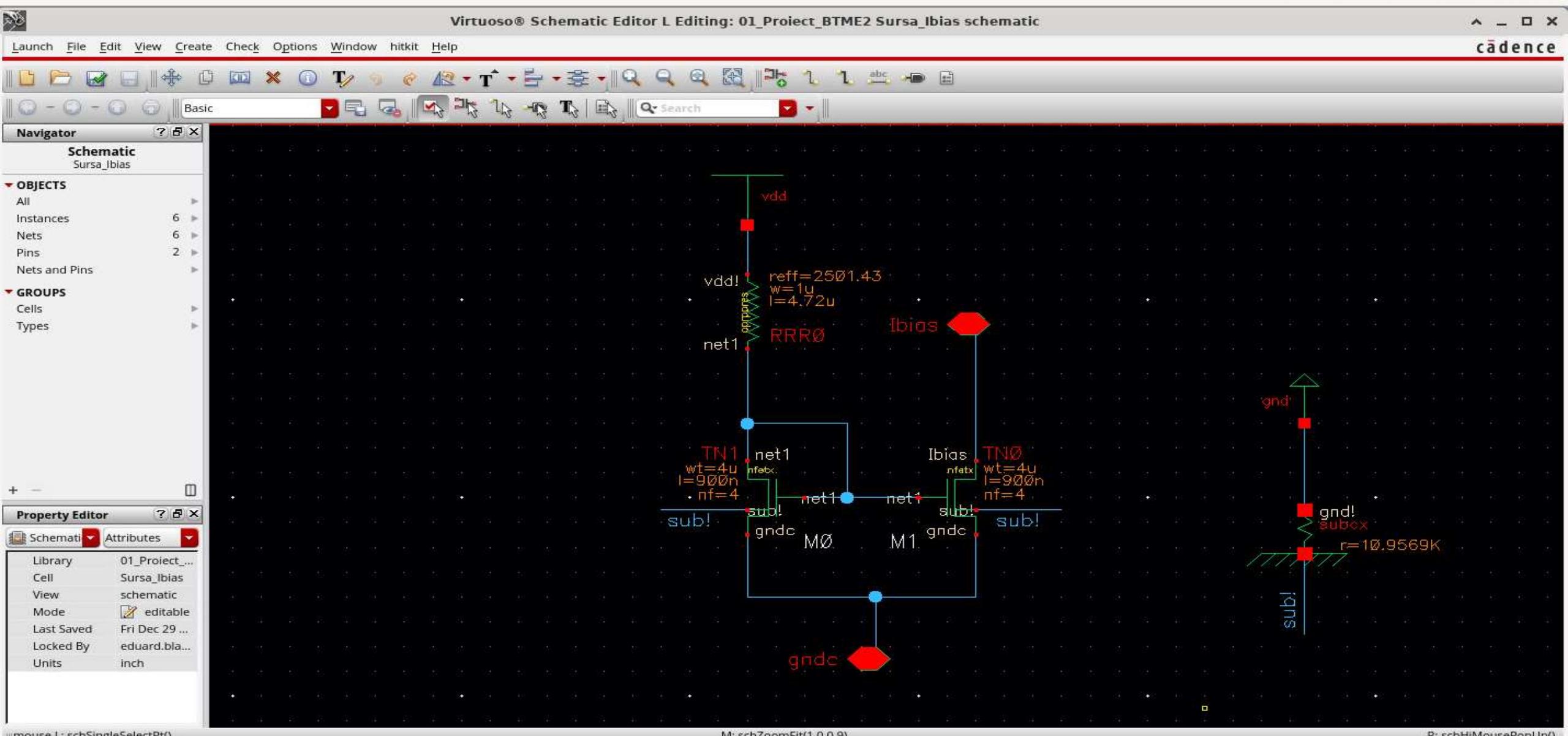


# MATCHING – OGLINDA N

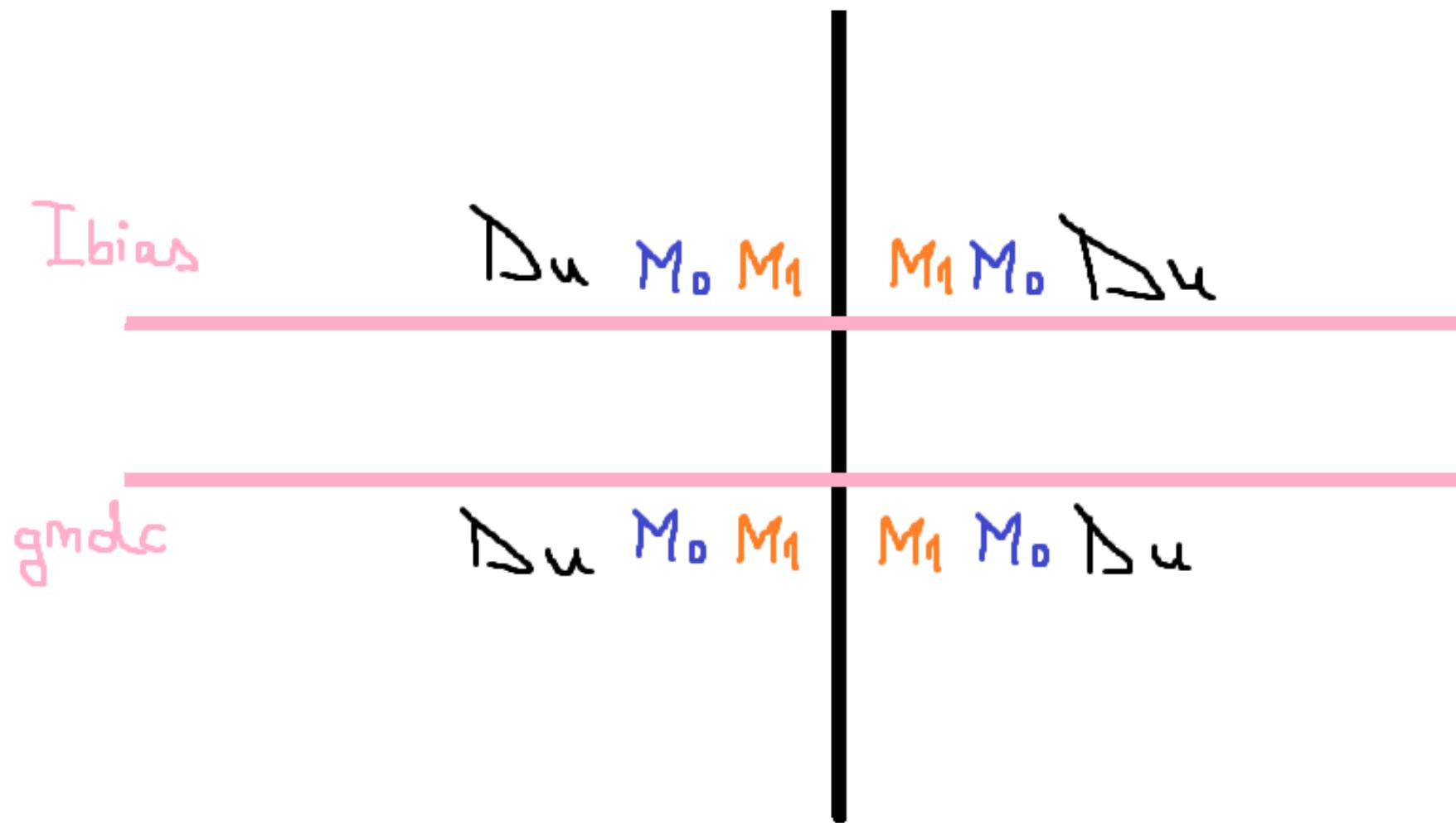


# SARCINA IBIAS - SCHEMATIC

Fri 29 Dec, 15:30 Eduard-Gabriel BLAGA



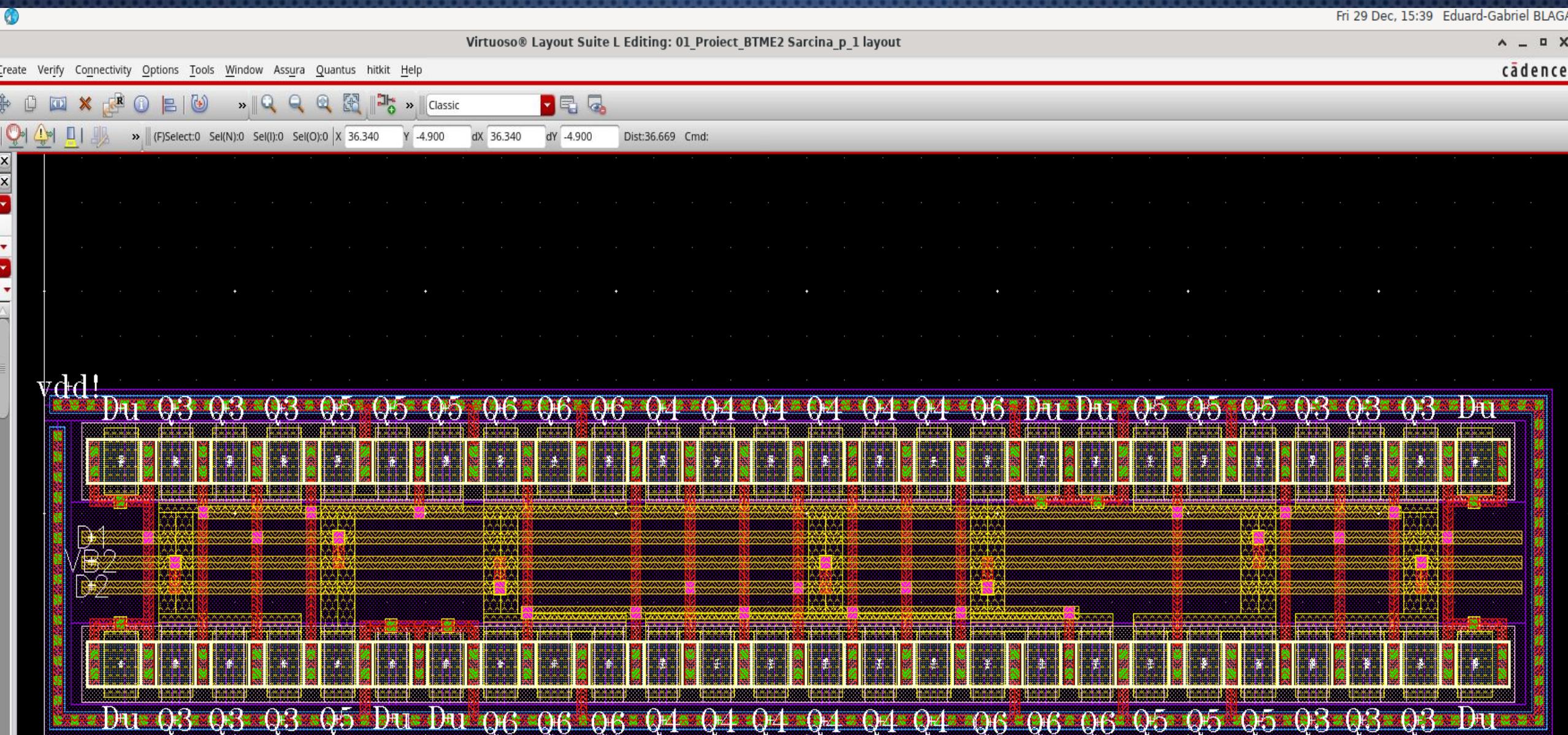
# MATCHING – SURSA IBIAS



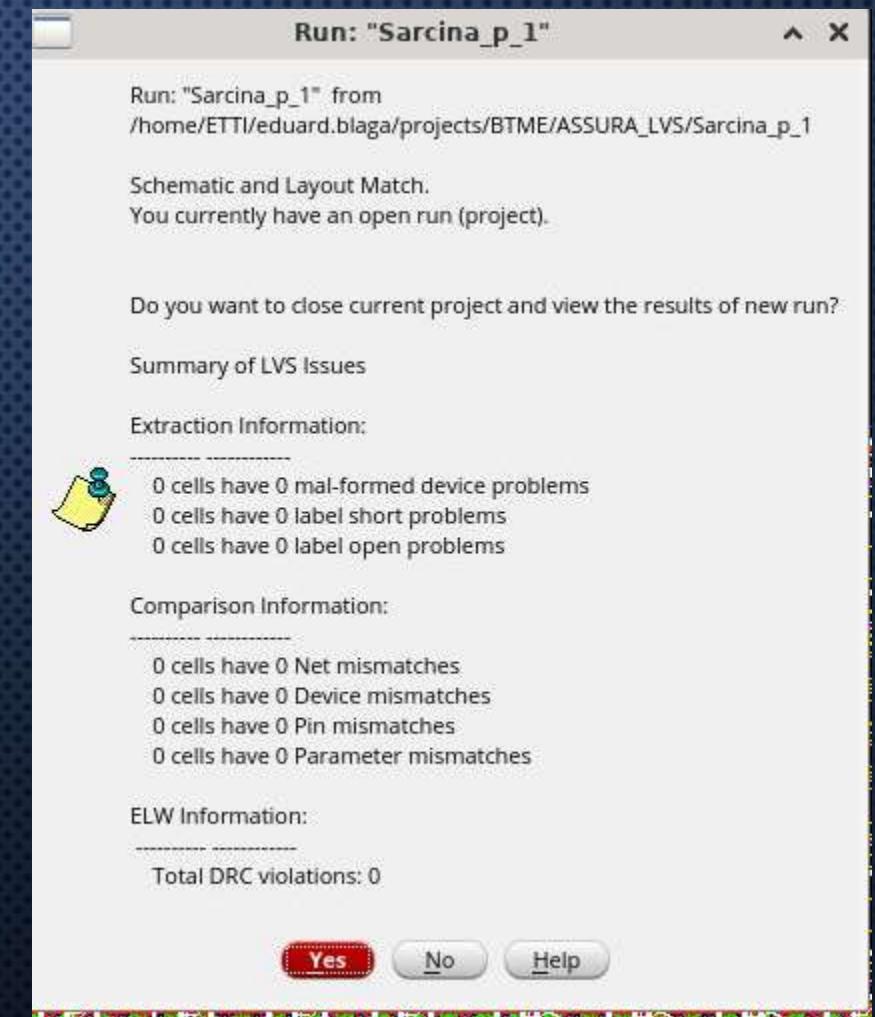
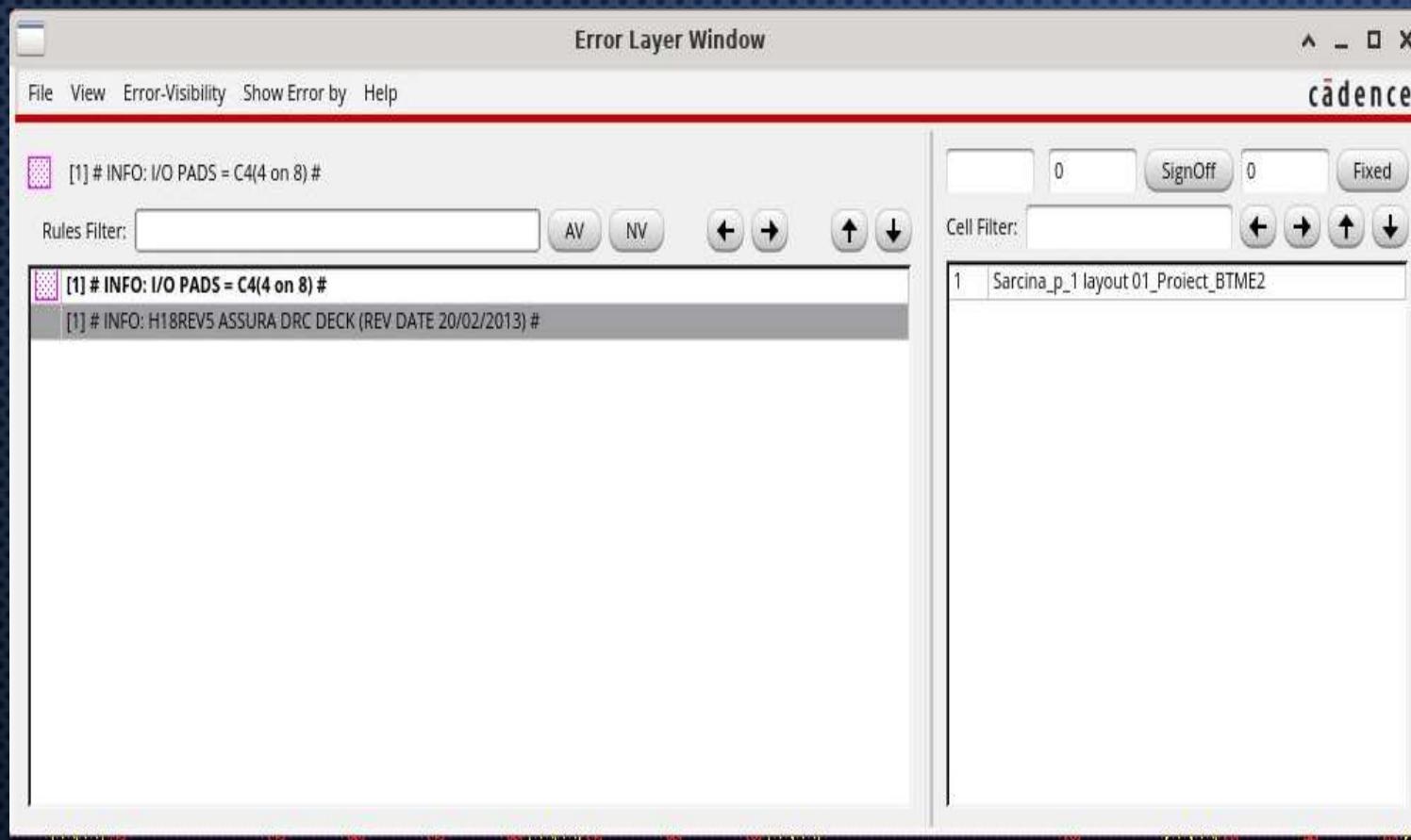
# CAPITOLUL 2

# LAYOUT

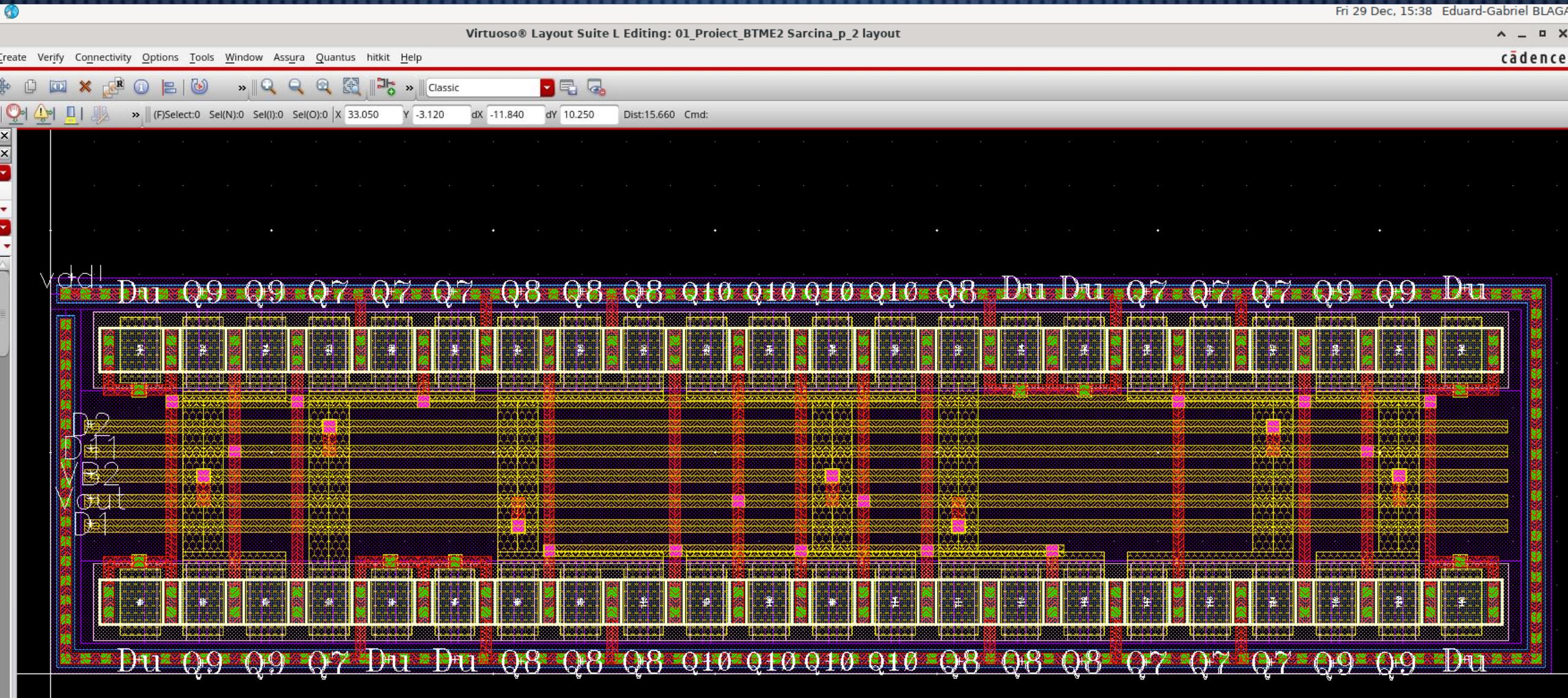
# SARCINA P – BLOC 1 - LAYOUT



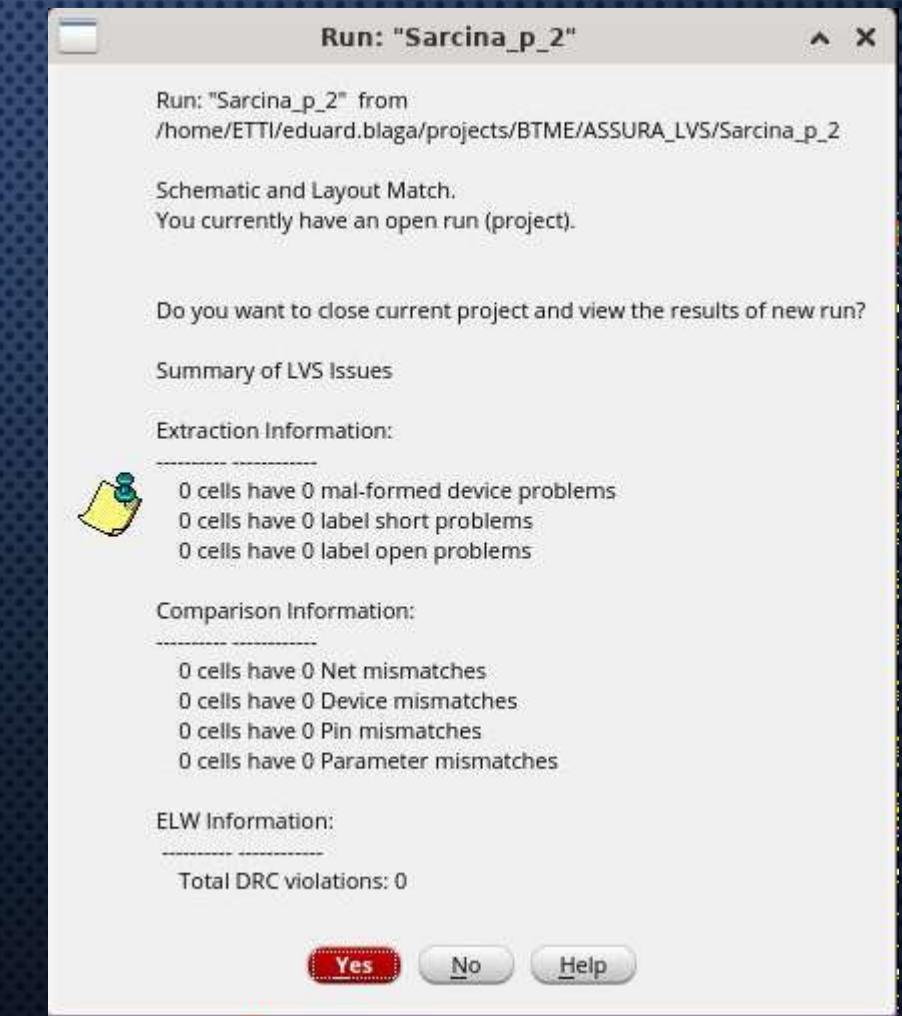
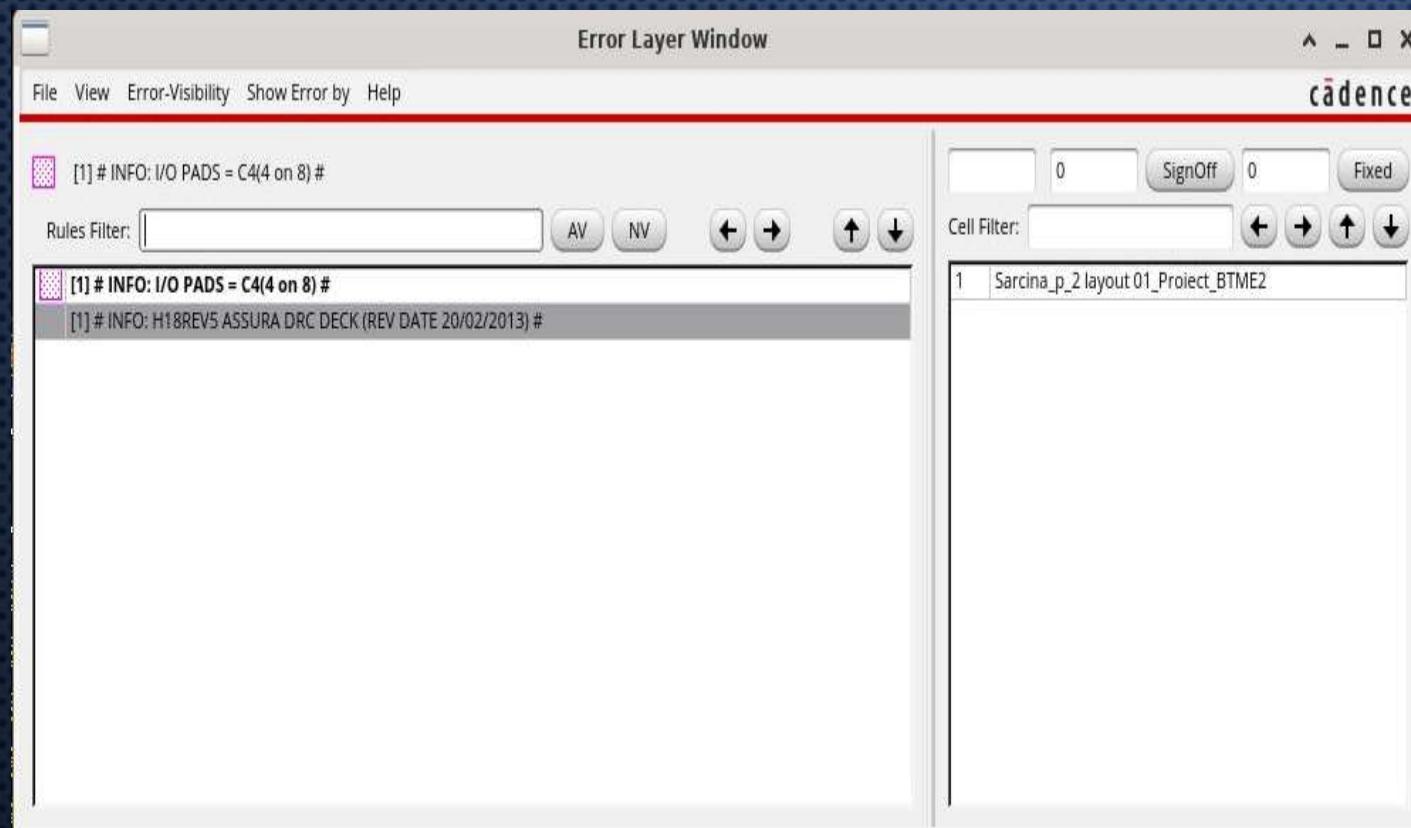
# VERIFICARE DRC SI LVS



# SARCINA P – BLOC 2 - LAYOUT

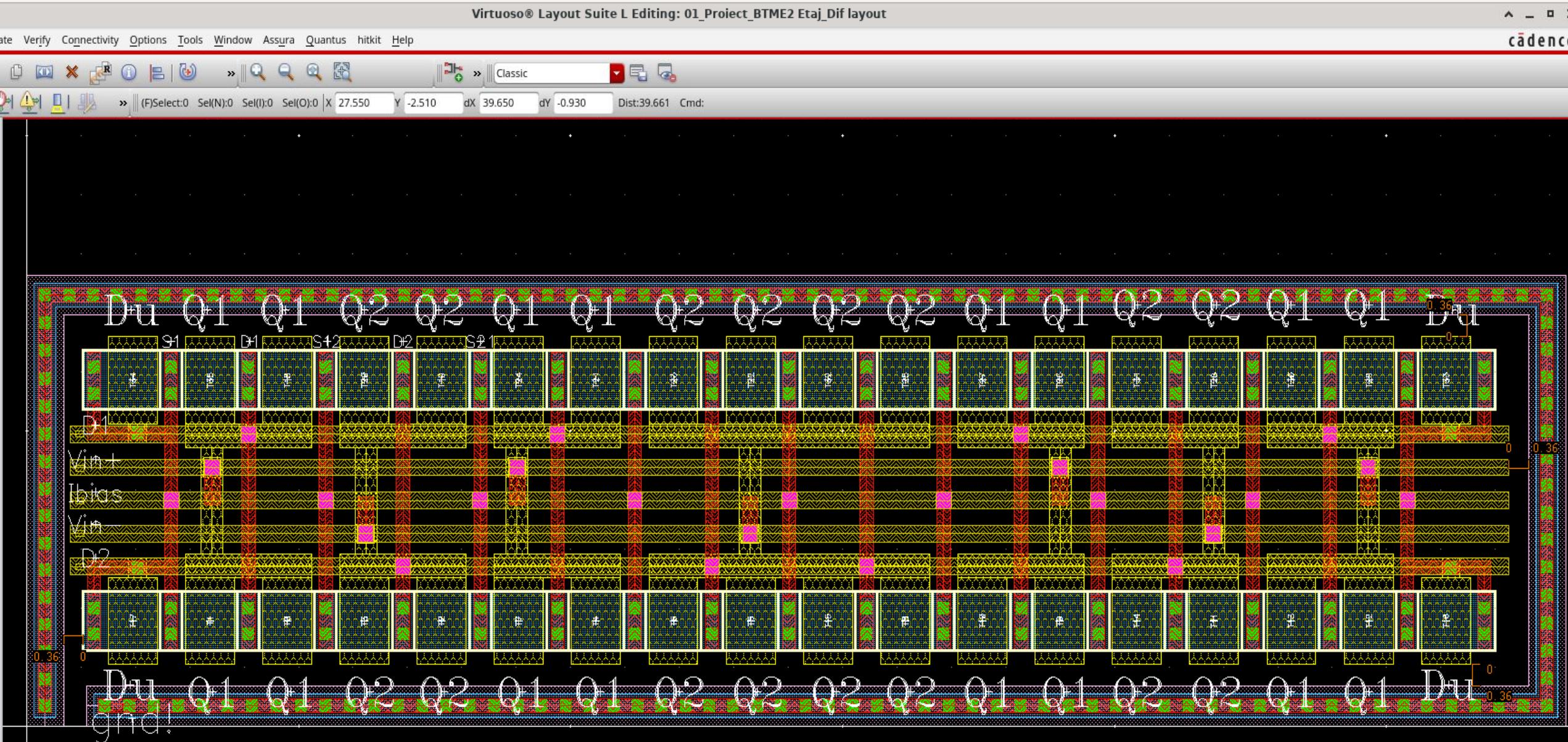


# VERIFICARE DRC SI LVS

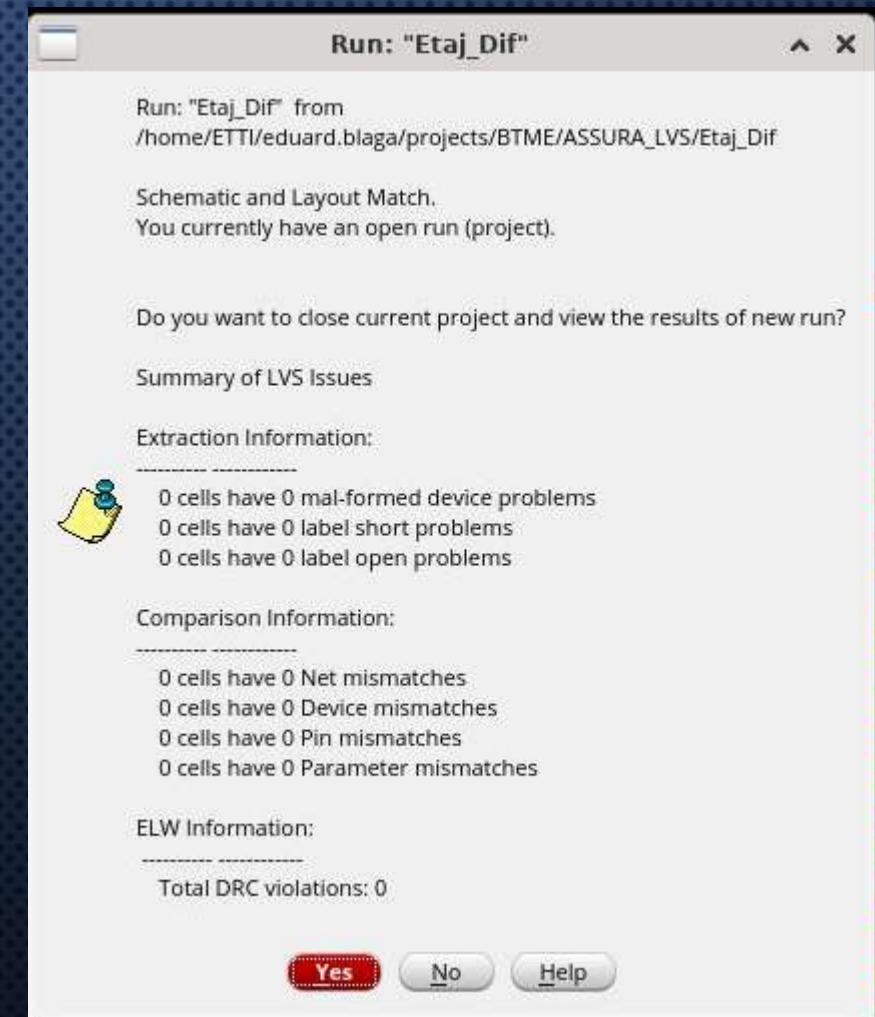
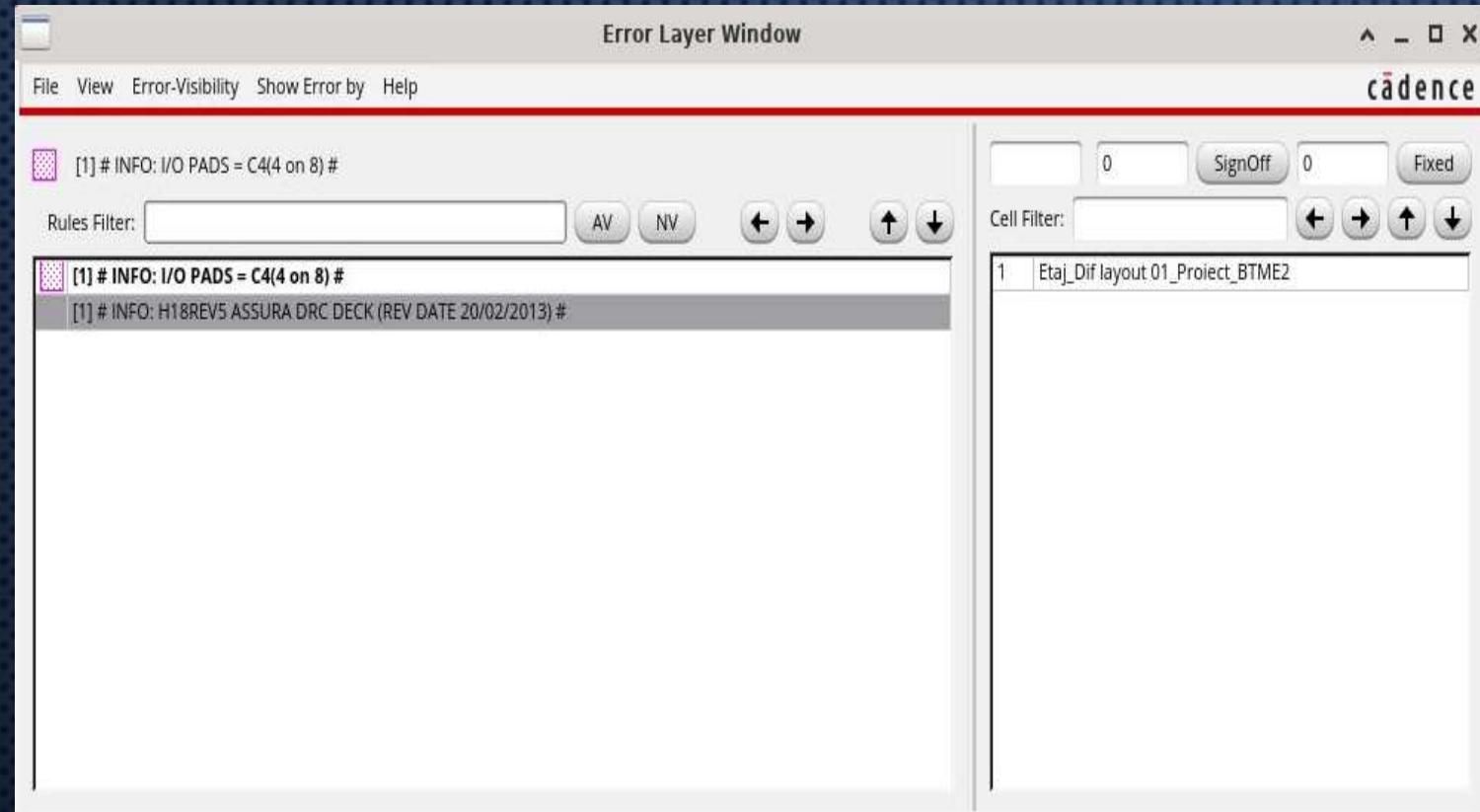


# DIFERENTIAL - LAYOUT

Fri 29 Dec, 15:42 Eduard-Gabriel BLAGA



# VERIFICARE DRC SI LVS



# OGLINDA N - LAYOUT

Fri 29 Dec, 15:45 Eduard-Gabriel BLAGA

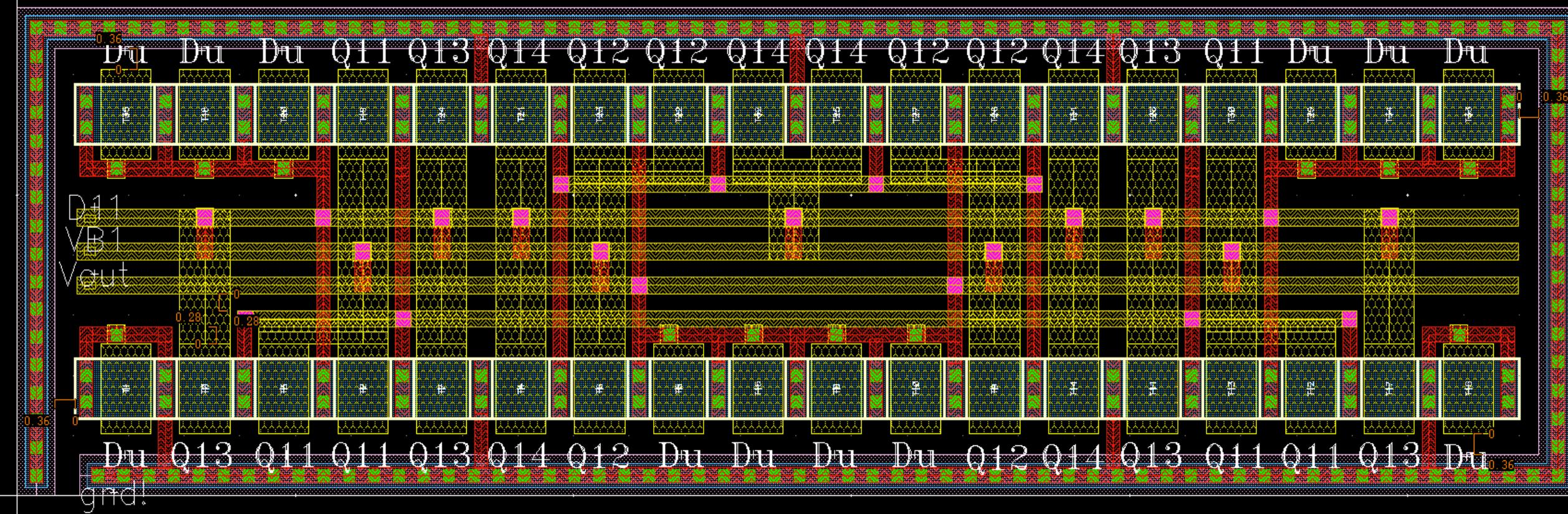
Virtuoso® Layout Suite L Editing: 01\_Project\_BTME2 Oglinda\_n layout



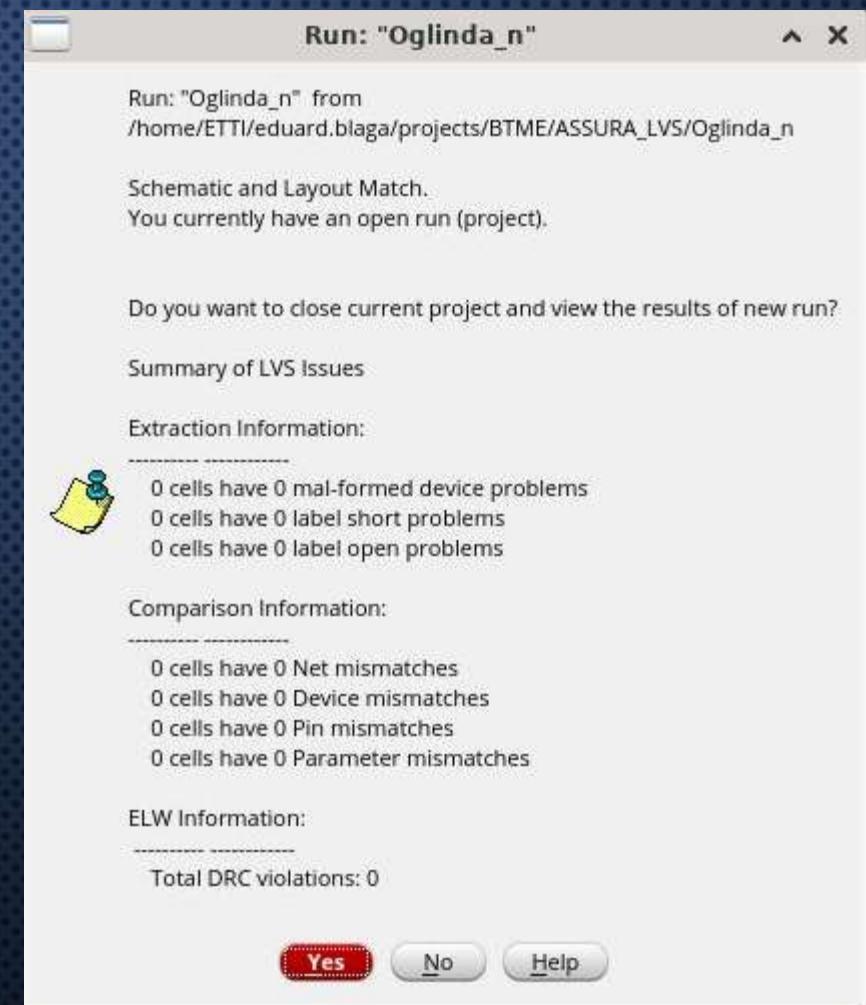
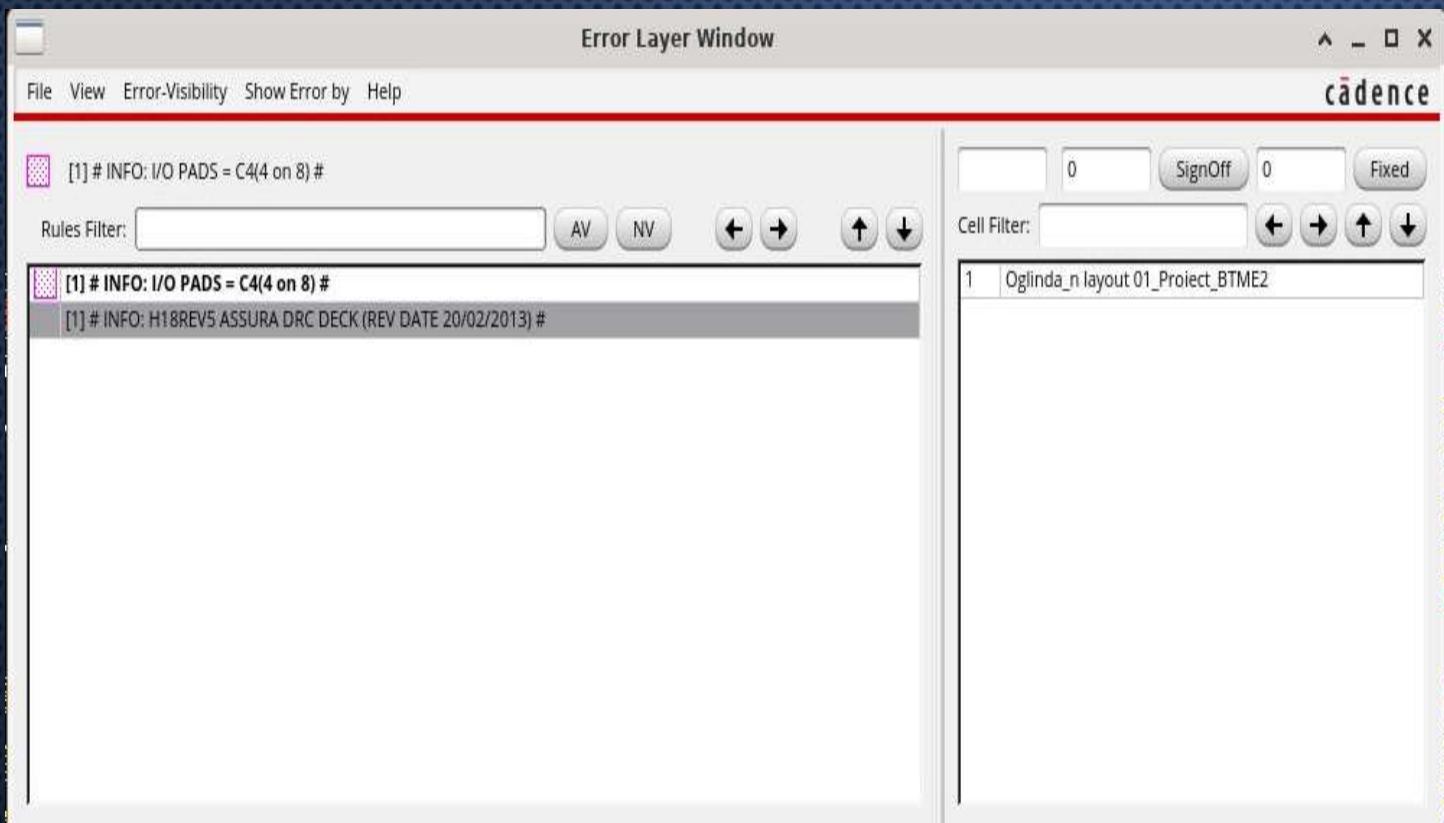
Verify Connectivity Options Tools Window Assura Quantus hitkit Help



(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 23.160 Y -2.250 dX 23.160 dY -2.250 Dist:23.269 Cmd:



# VERIFICARE DRC SI LVS



**Edit Object Properties**

Apply To: only current instance

Show: system user CDF

Browse Reset Instance Labels Display

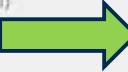
Property	Value	Display
Library Name	cmhv7sf	off
Cell Name	oprppres	value
View Name	symbol1	off
Instance Name	RRR0	off

Add Delete Modify

CDF Parameter

Value	Display
Specify res by geometry? <input checked="" type="checkbox"/>	off
Backplate <input type="button" value="sub"/>	off
Backplate node <input type="button" value="sub!"/>	off
Resistance (total) <input type="text" value="2501.43 Ohms"/>	off
Resistance <input type="text" value="833.8100000000001 Ohms"/>	off
Width <input type="text" value="1u M"/>	off
Length <input type="text" value="4.72u M"/>	off
Number of Series Bars <input type="text" value="3"/>	off
Parallel Bars <input type="text" value="1"/>	off
Multiplicity <input type="text" value="1"/>	off
Resistor Bar Spacing (microns) <input type="text" value="0.76"/>	off
Sub Resistance <input type="text" value="50 Ohms"/>	off
Temperature Delta <input type="text" value="0"/>	off
Subcircuit name <input type="text" value="oprppres"/>	off

OK Cancel Apply Defaults Previous Next Help




PENTRU A OBTINE UN LAYOUT MAI COMPACT IN CADRUL SURSEI IBIAS, AM INSERIAT 3 REZISTENTE OPRPPRES CONECTATE CU METAL M1. PENTRU A OBTINE ACEEASI VALOARE SI IN LAYOUTSI IN SCHEMATIC, MODIFICAM PARAMETRUL REZISTENTEI DIN SCHEMATIC CA IN IMAGINE. LA FINAL, IN PARTEA DE LAYOUT VA TREBUI SA UMPELEM SPATIUL GOL DINTRE REZISTENTE CU UN STRAT DE OP (DRW)

**Edit Instance Properties**

Attribute Connectivity Parameter Property ROD

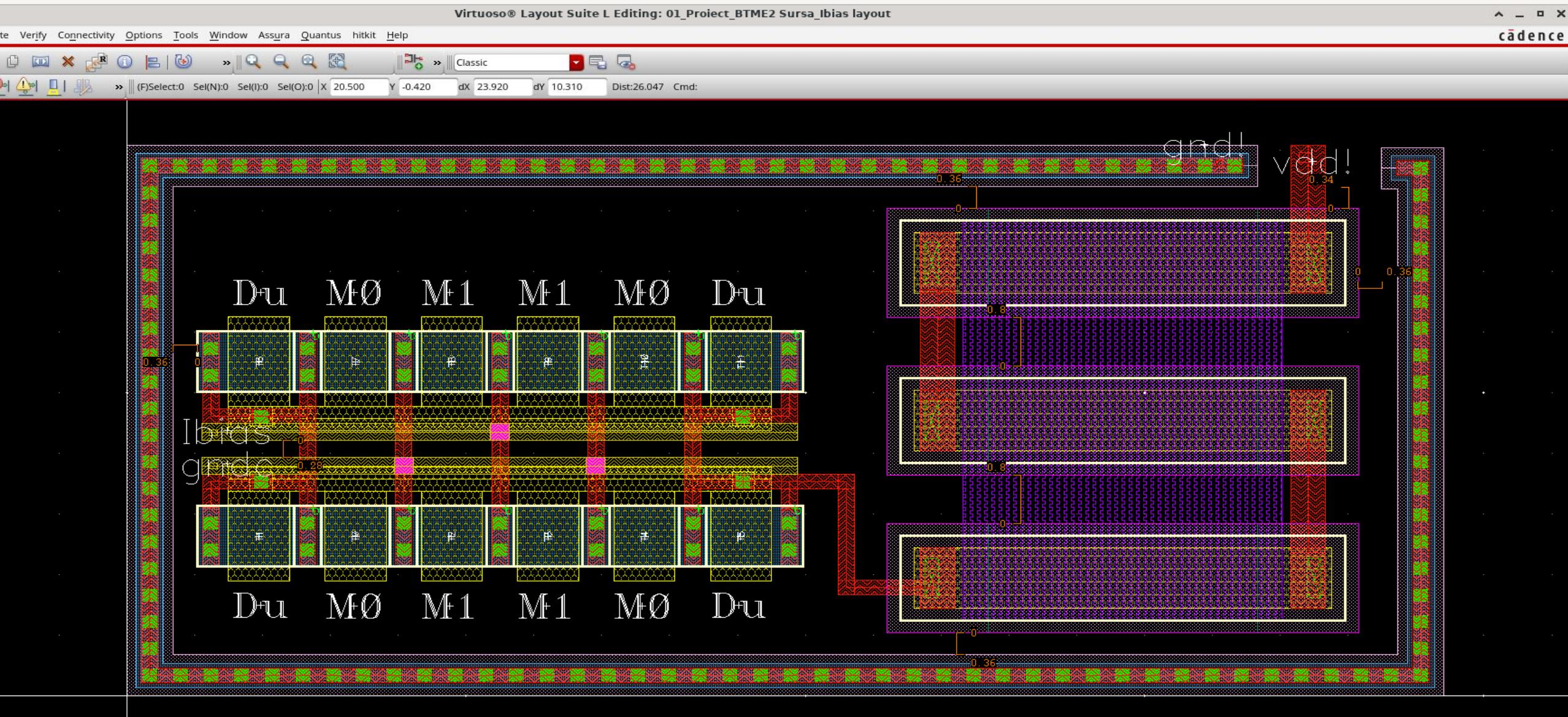
Specify res by geometry?	<input checked="" type="checkbox"/>
Backplate	<input type="button" value="sub"/>
Backplate node	<input type="button" value="sub!"/>
Resistance (total)	833.81
Resistance	833.8100000000001
Width	<input type="text" value="1u"/>
Length	<input type="text" value="4.72u"/>
Number of Series Bars	1
Parallel Bars	1
Multiplicity	1
Temperature Delta	0
Subcircuit name	oprppres

Display CDF Parameter Name

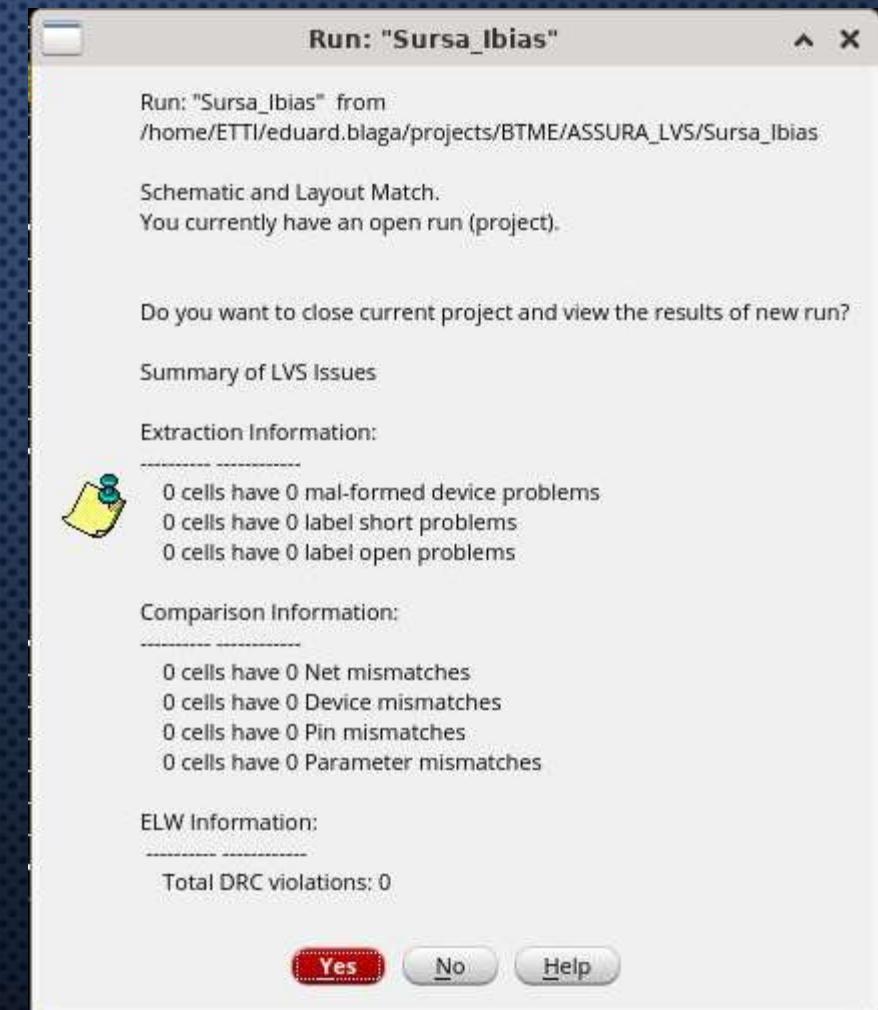
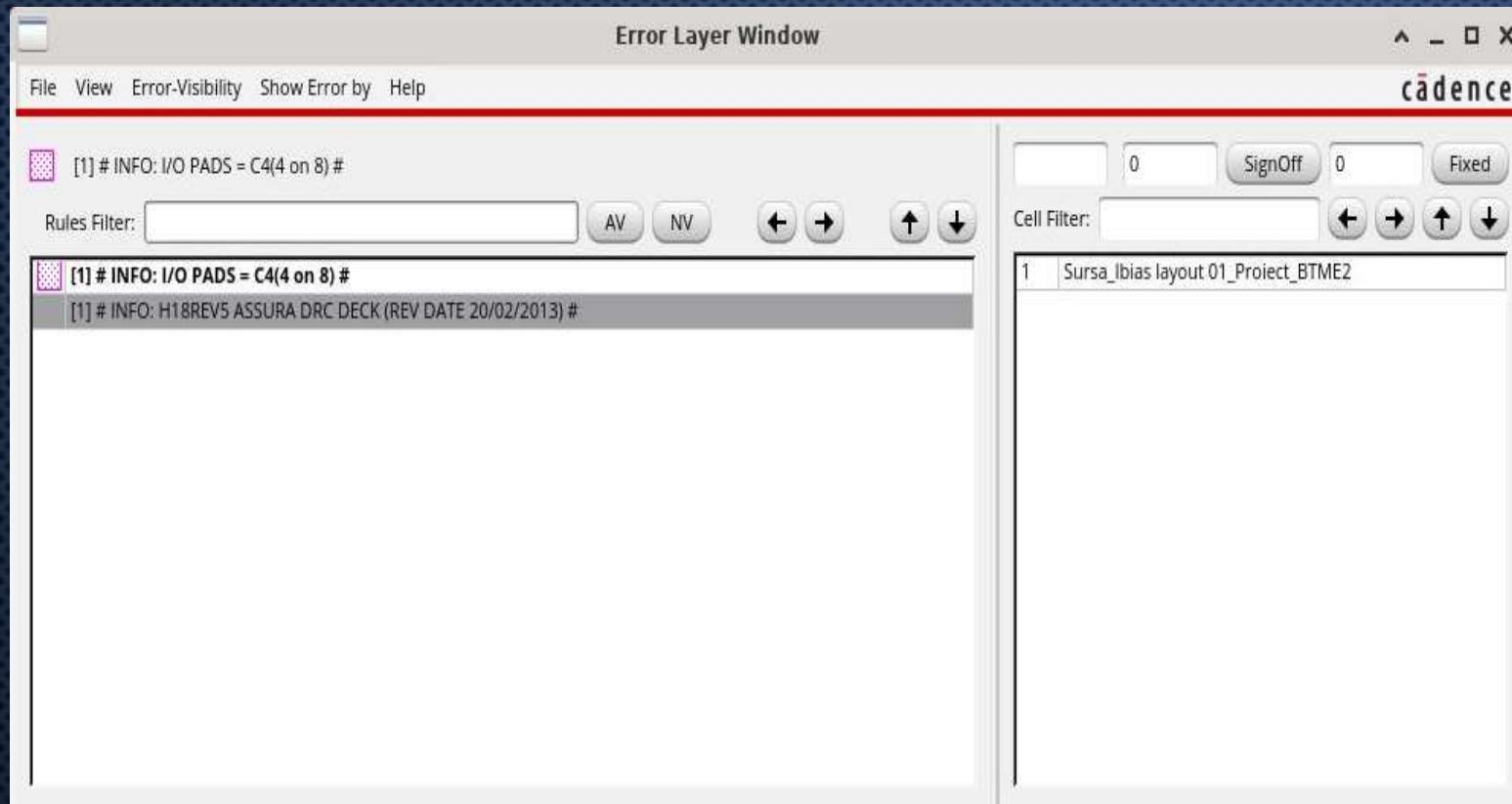
OK Cancel Apply Convert To Mosaic Help

# SURSA IBIAS - LAYOUT

Fri 29 Dec, 15:49 Eduard-Gabriel BLAGA



# VERIFICARE DRC SI LVS

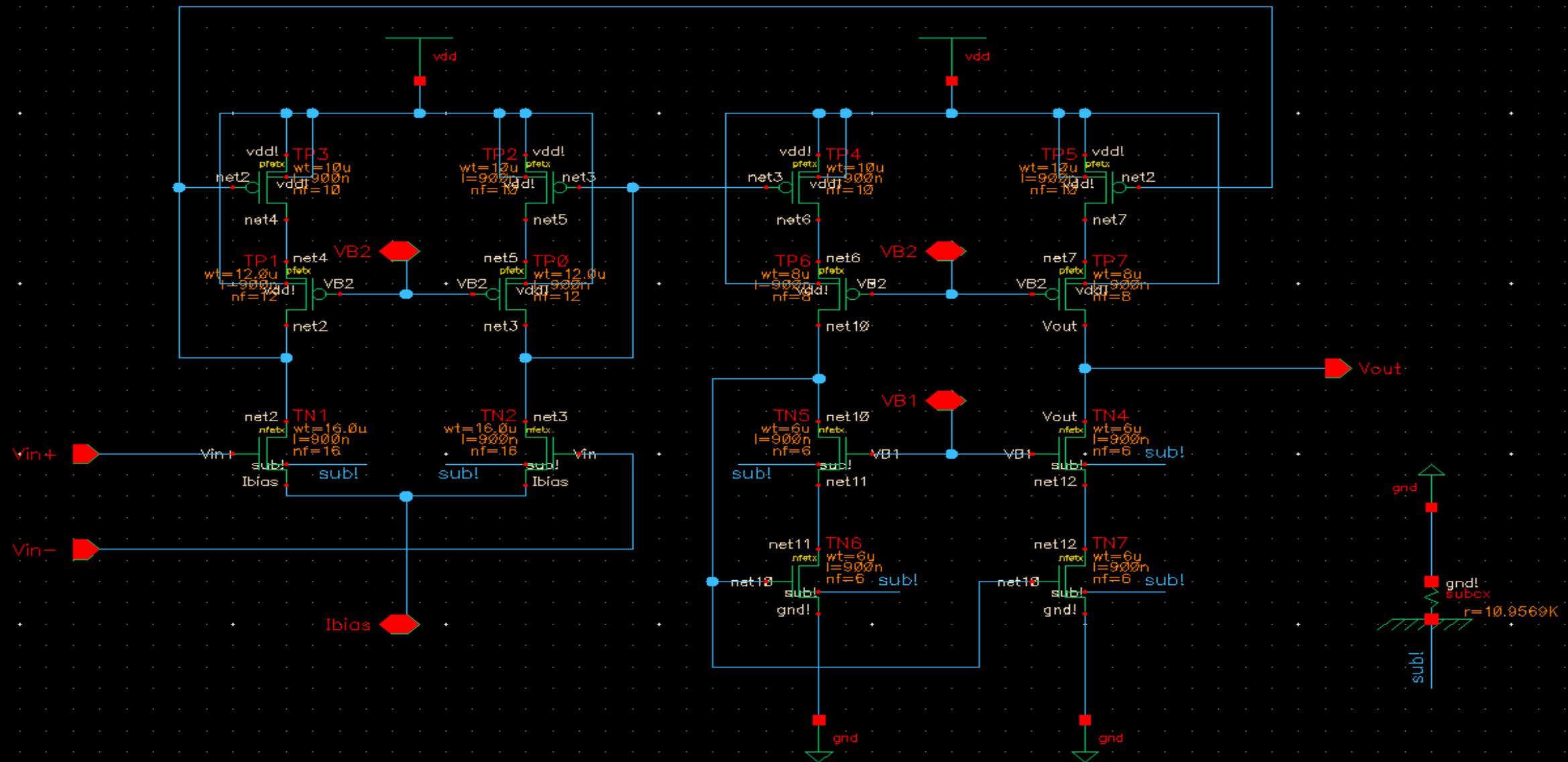




# **CAPITOLUL 3**

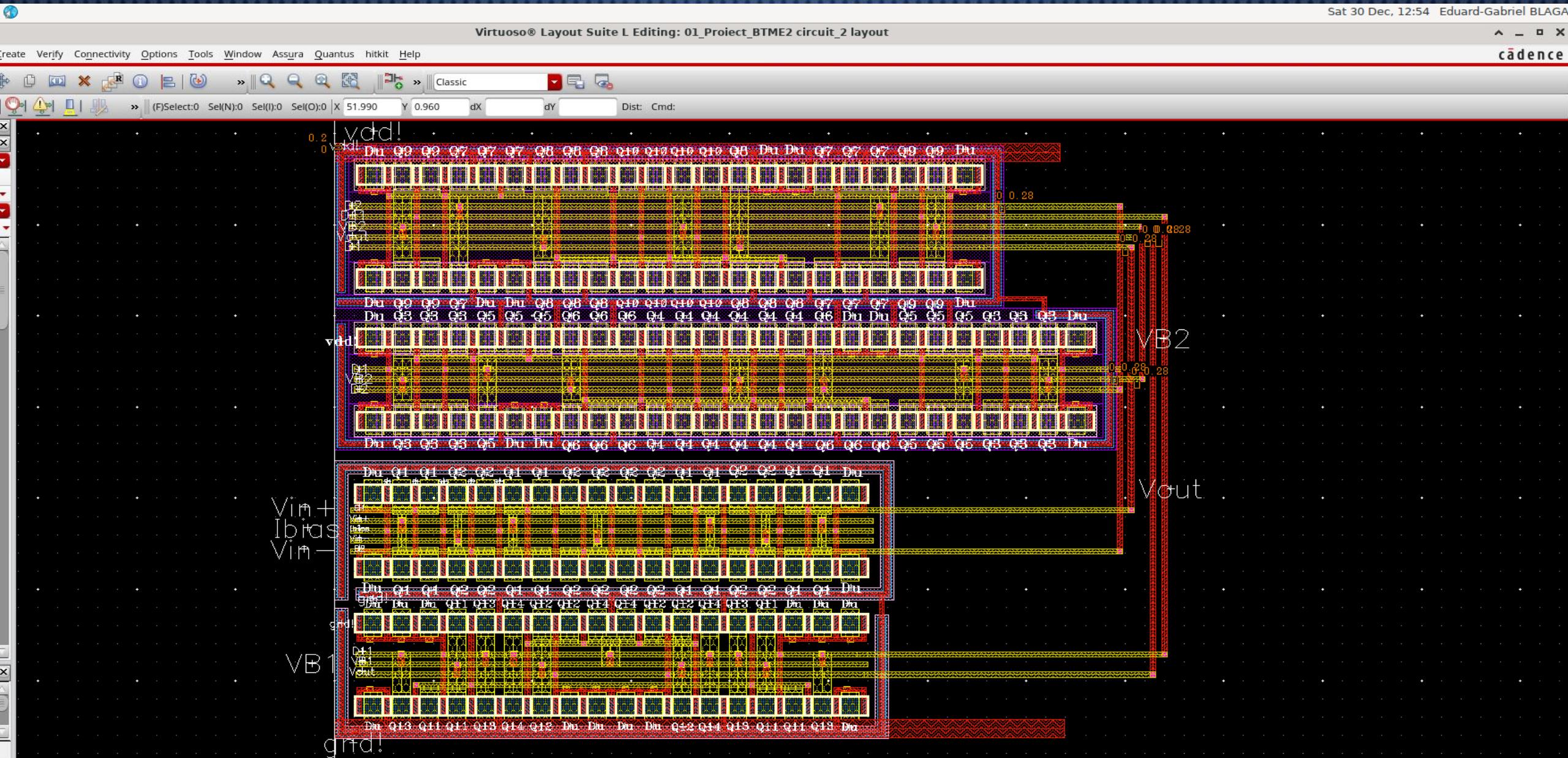
# **CIRCUITUL FINAL**

# SCHEMATICUL CIRCUITULUI

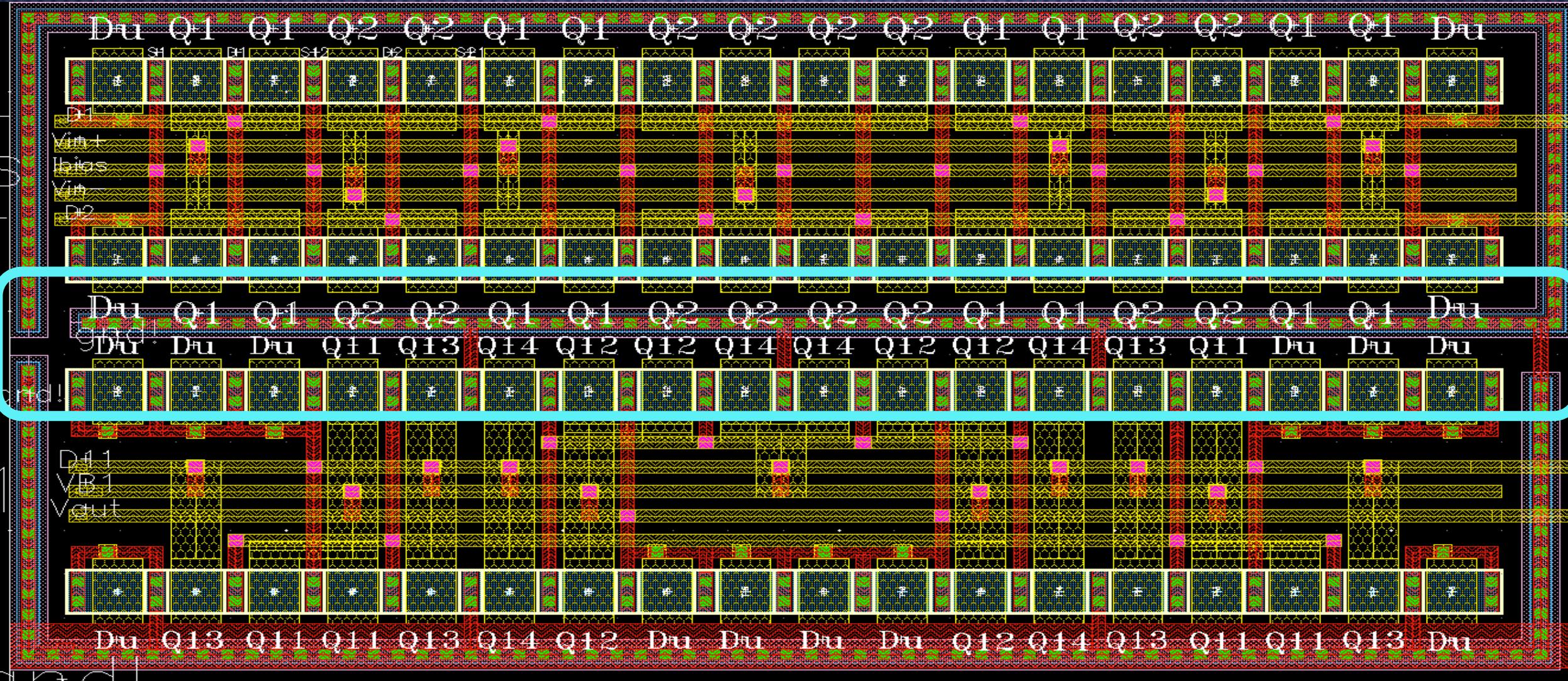


# LAYOUT-UL CIRCUITULUI

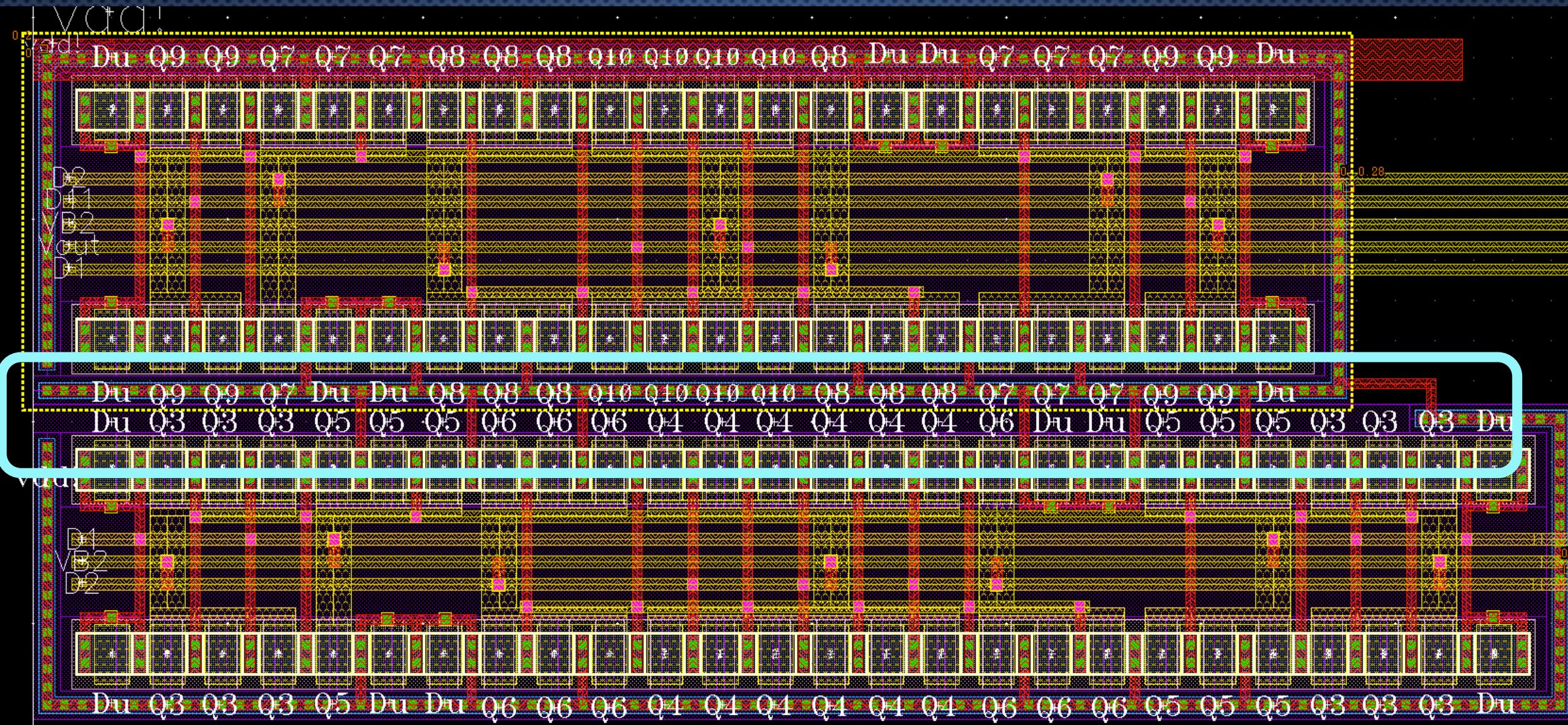
Sat 30 Dec, 12:54 Eduard-Gabriel BLAGA



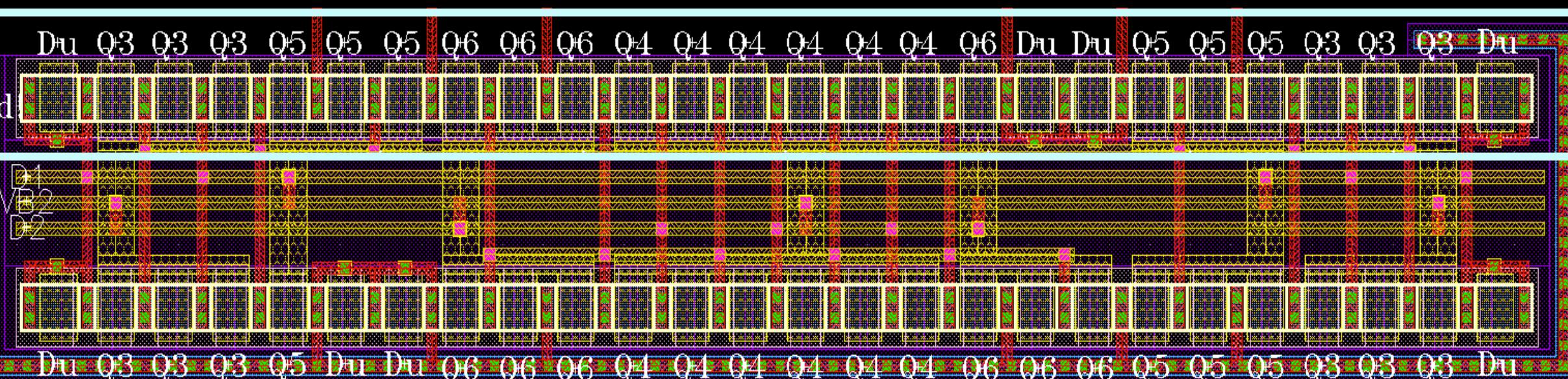
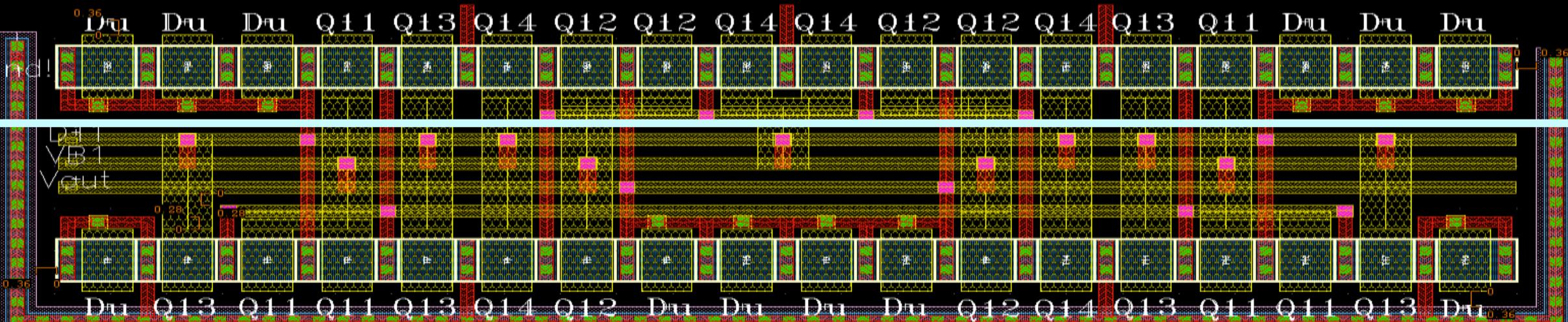
PENTRU CACIRCUITUL SA TREACA DE SIMULAREA LVS TREBUIE SA MODIFICAM LAYOUTURILE INITIALE IN CAZUL BLOCURILOR CU ACELEASI LINII DE GND SI VDD, ASTFEL INCAT SA LE INTERCONECTAM LA ACEEASI LINIE



PENTRU CACIRCUITUL SA NU DEA EROARE LA SIMULAREA LVS TREBUIE SA MODIFICAM LAYOUTURILE INITIALE IN CAZUL BLOCURILOR CU ACELEASI LINII DE GND SI VDD, ASTFEL INCAT SA LE INTERCONNECTAM LA ACEEASI LINIE



SURSELE CARE ERAU INITIAL CONECTATE LA LINIA DE GND LE VOM PRELUNGI CU ACEEASI DISTANTA ASTFEL INCAT SA VINE CONECTATE LA LINIA DE GND A URMATORULUI BLOC. ACEEASI ANALOGIE SE APLICA SI IN CADRUL BLOCURILOR CU VDD



# VERIFICARE DRC SI LVS

