TEMA PROIECT BTME2

PROIECT NR. 2

Blaga Eduard Gabriel

Grupa 5413

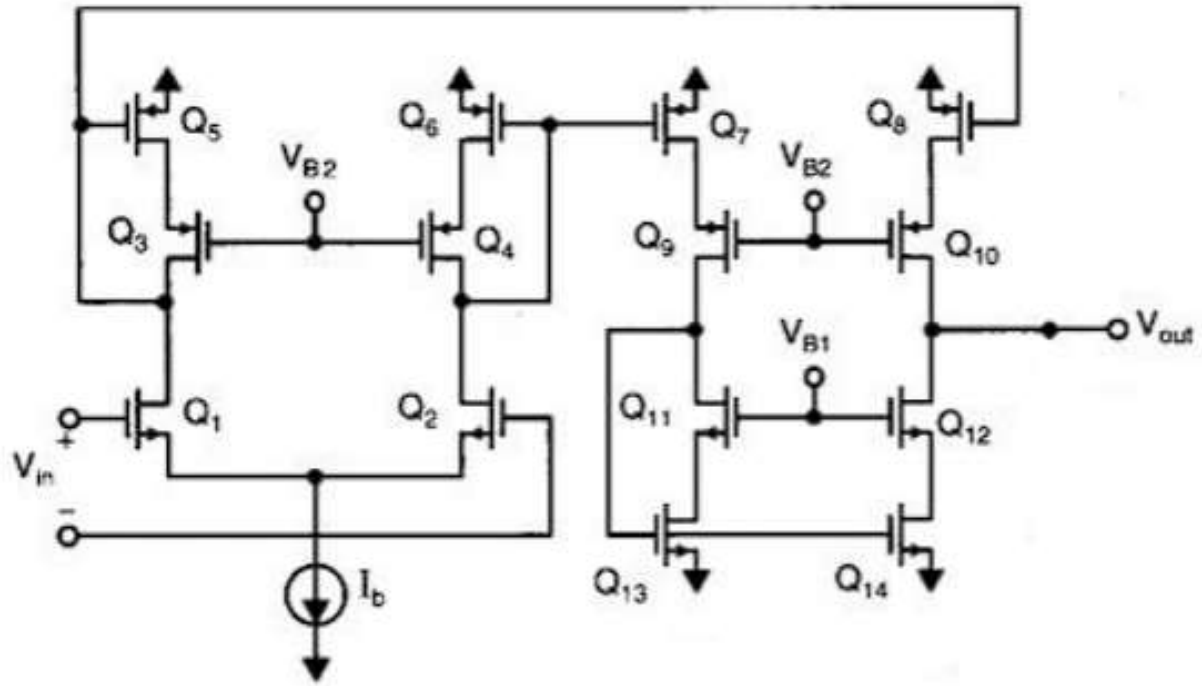
CAPITOLUL 1 - SCHEMATIC

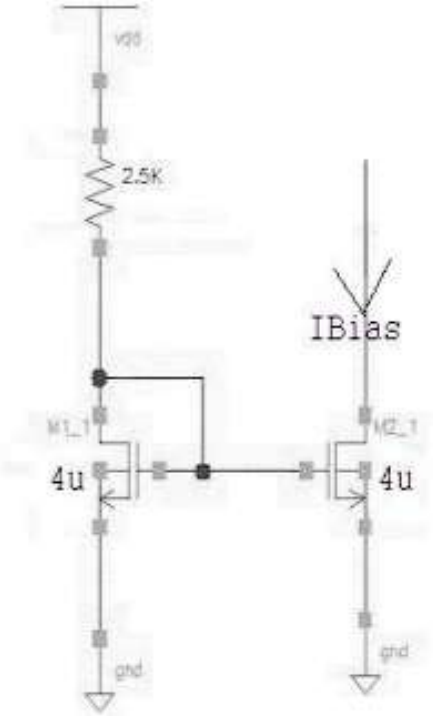
- Stabilirea gruparilor tranzistoarelor
- Realizarea matchingului
- Realizarea schematicelor

SCHEMA CIRCUITULUI

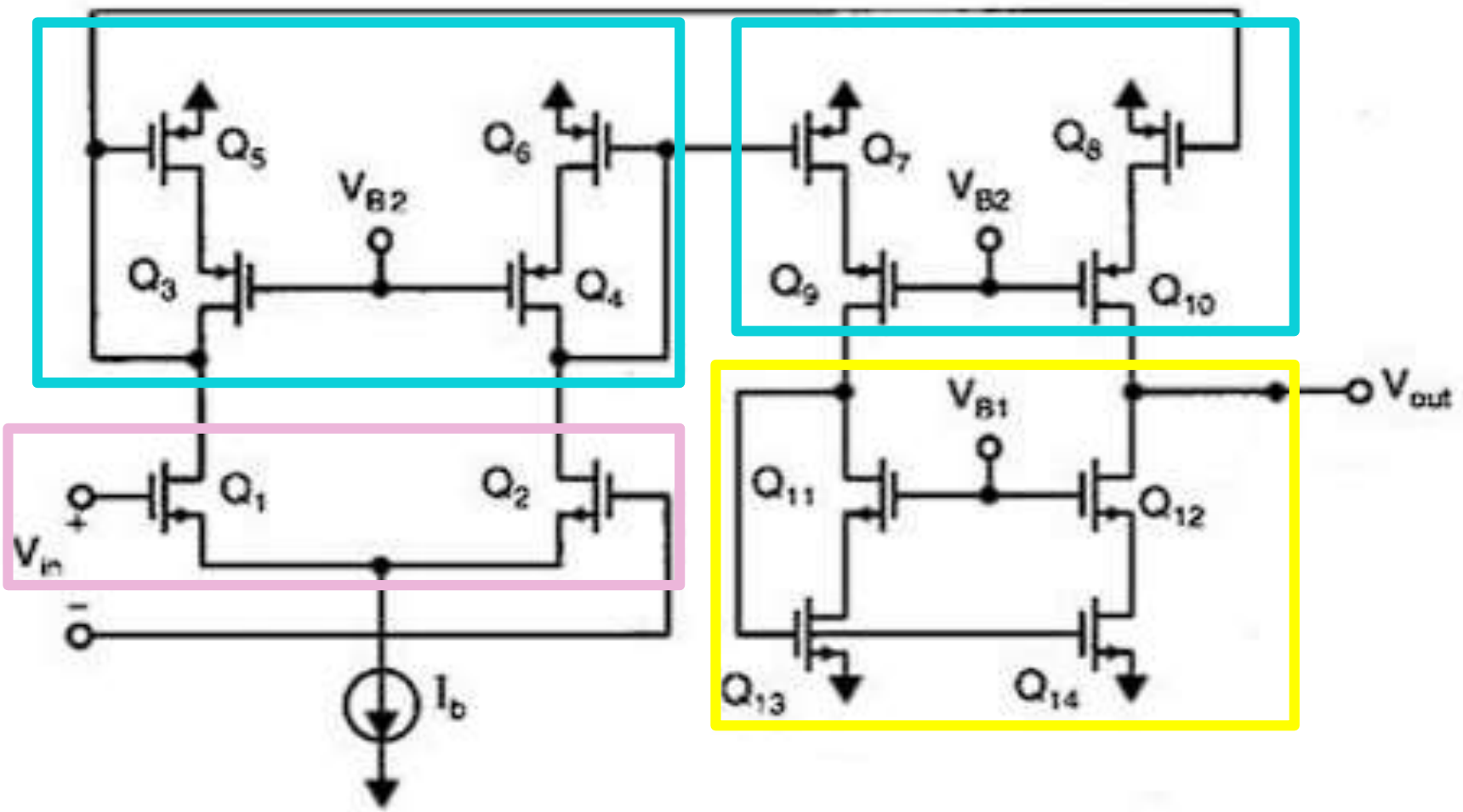
Proiect 2.

L=0.9u și w1=w2=16u , w3=w4= 12u w5=w6=w7=w8=10u, w9=w10=8u w11=w12=w13=w14=6u Ibias1 ca în figură:

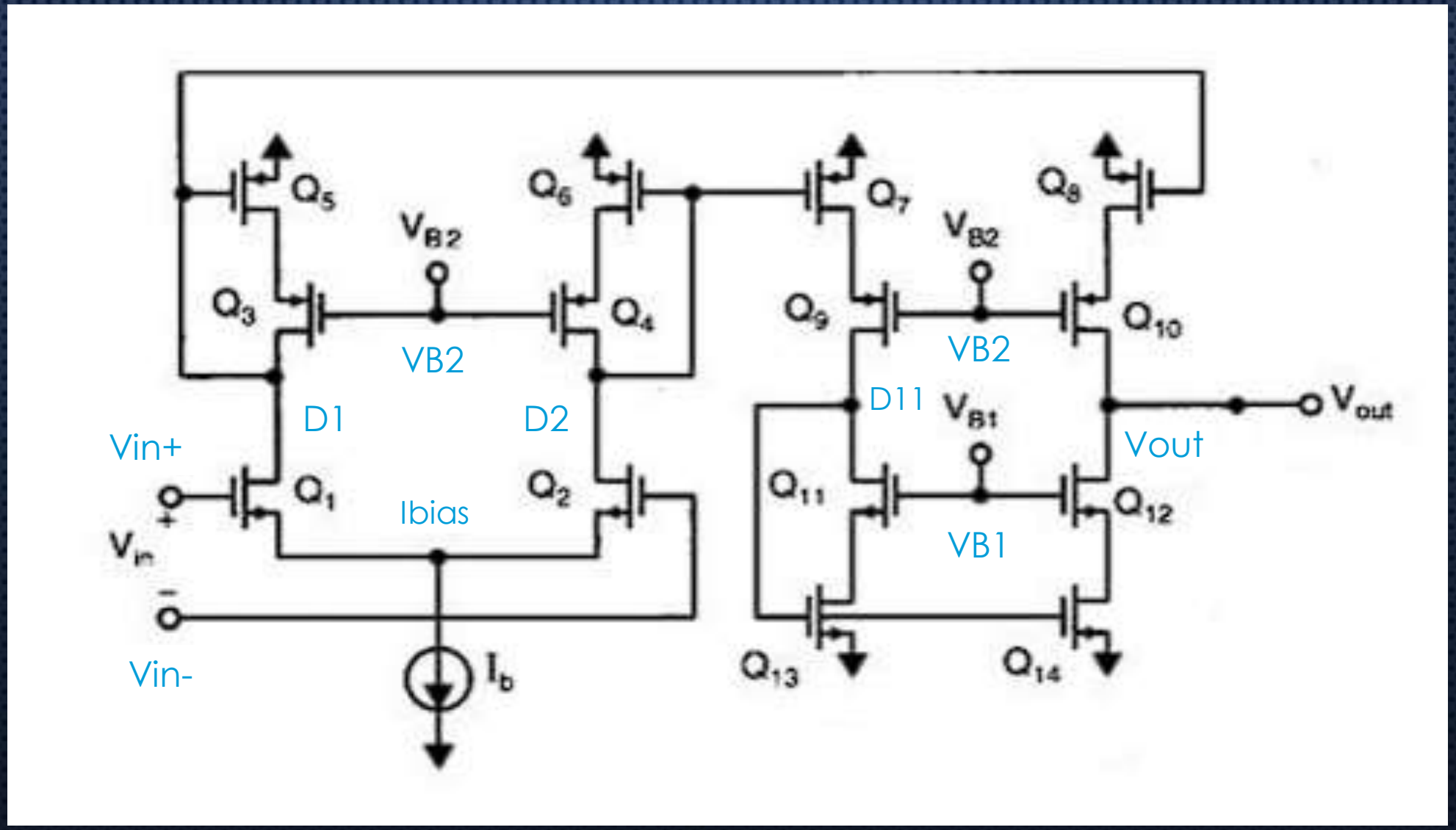




STABILIREA GRUPARILOR



CONEXIUNI INTERNE



STABILIREA GRUPARILOR PENTRU LAYOUT

1. Bloc sarcina p

   Blocul 1 format din Q3, Q4, Q5 si Q6 : 12u + 12u + 10u + 10u = 44u; +4Du(Colturi) +4Du(interior) = 52u
   Blocul 2 format din Q7, Q8, Q9 si Q10 : 10u + 10u + 8u + 8u = 36u ; +4Du(Colturi) +4Du(interior) = 44u

2. Etaj Diferential

   Este format din Q1 si Q2 : 16u + 16u =32u; +4Du(Colturi) = 36u

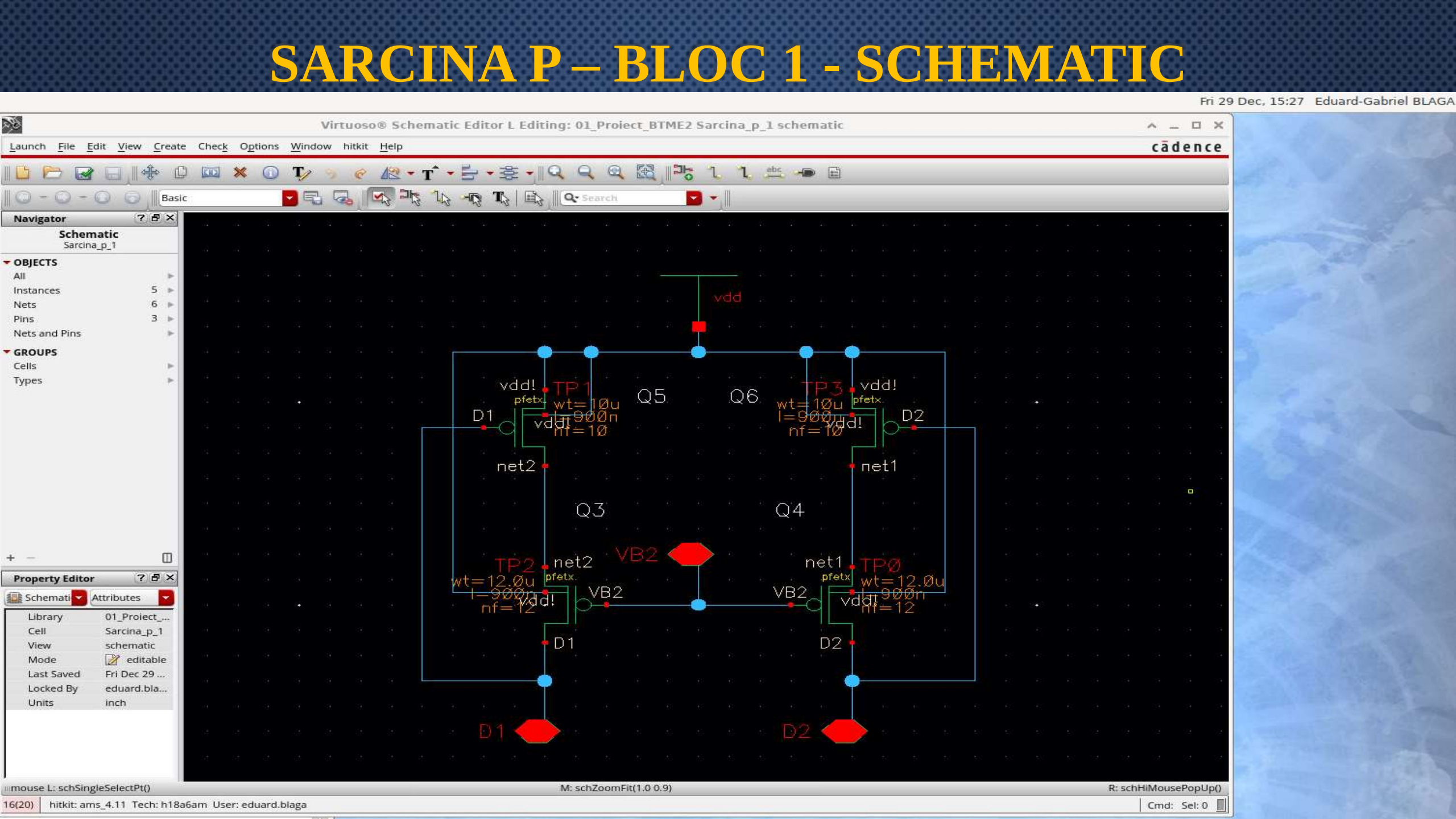
3. Oglinda n

   Este formata din Q11, Q12, Q13 si Q14 : 6u + 6u + 6u + 6u = 24u; +4Du(Colturi) +8Du(Interior) = 36u

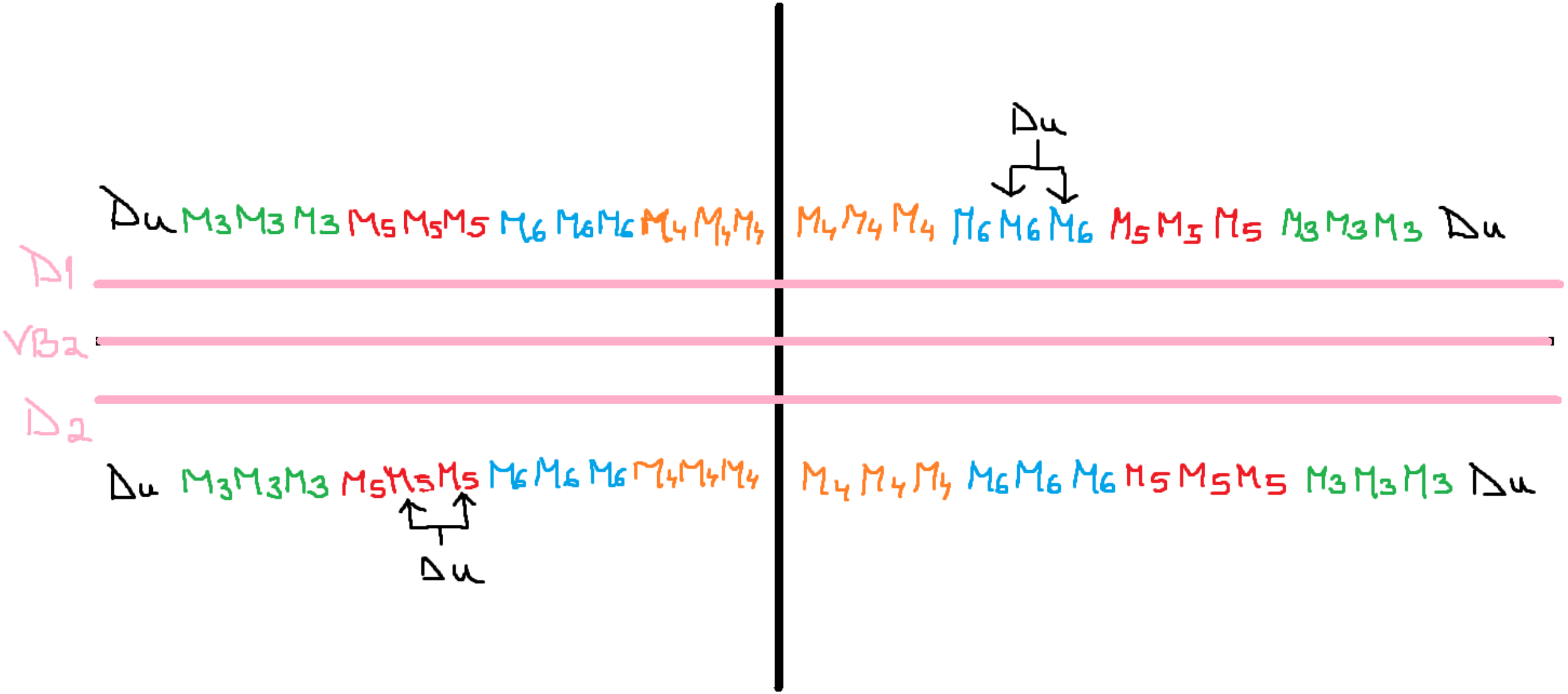
4. Sursa current Ibias

   Este formata din M1 si M0 : 4u + 4u = 8u; +4Du(Colturi) = 12u

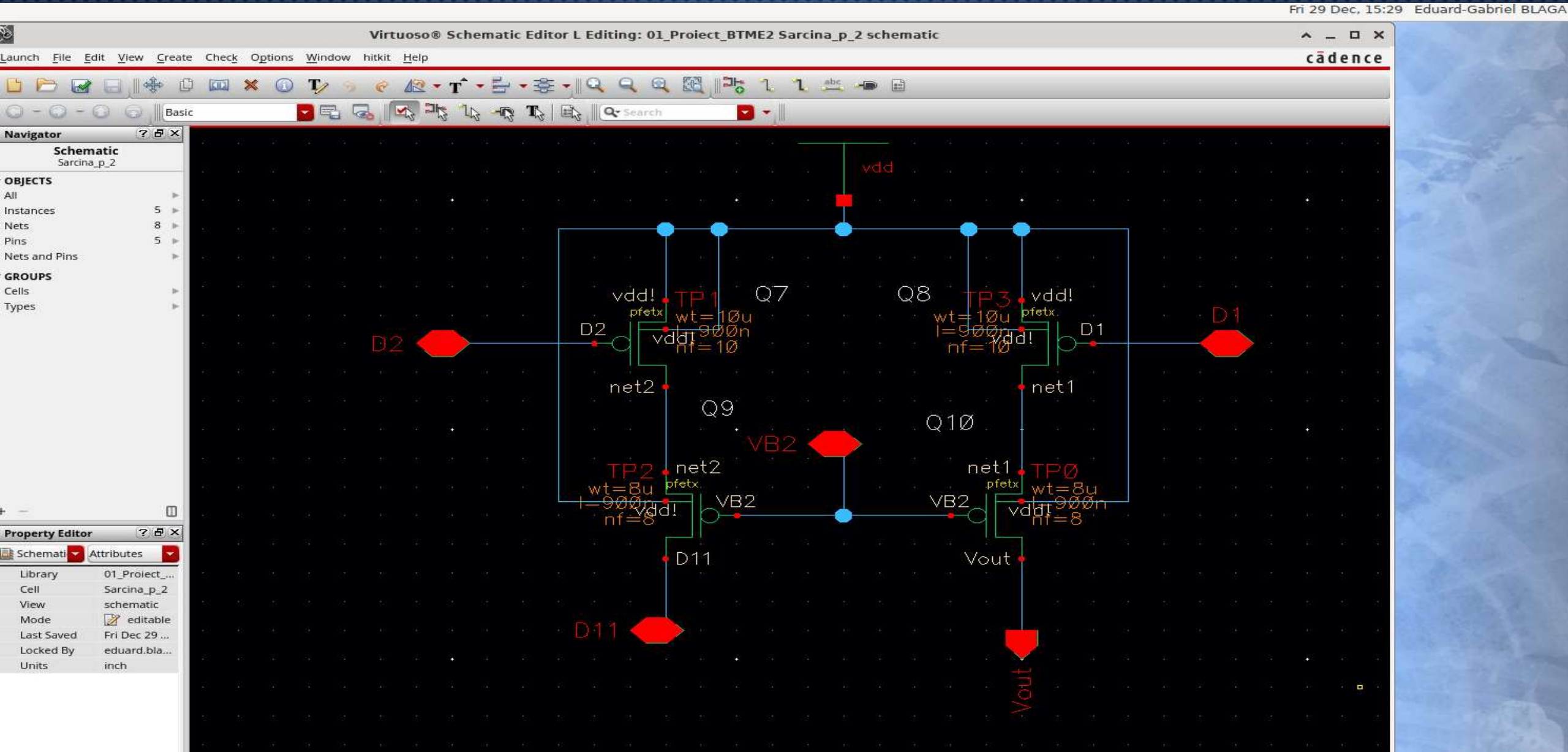
SARCINA P – BLOC 1 - SCHEMATIC



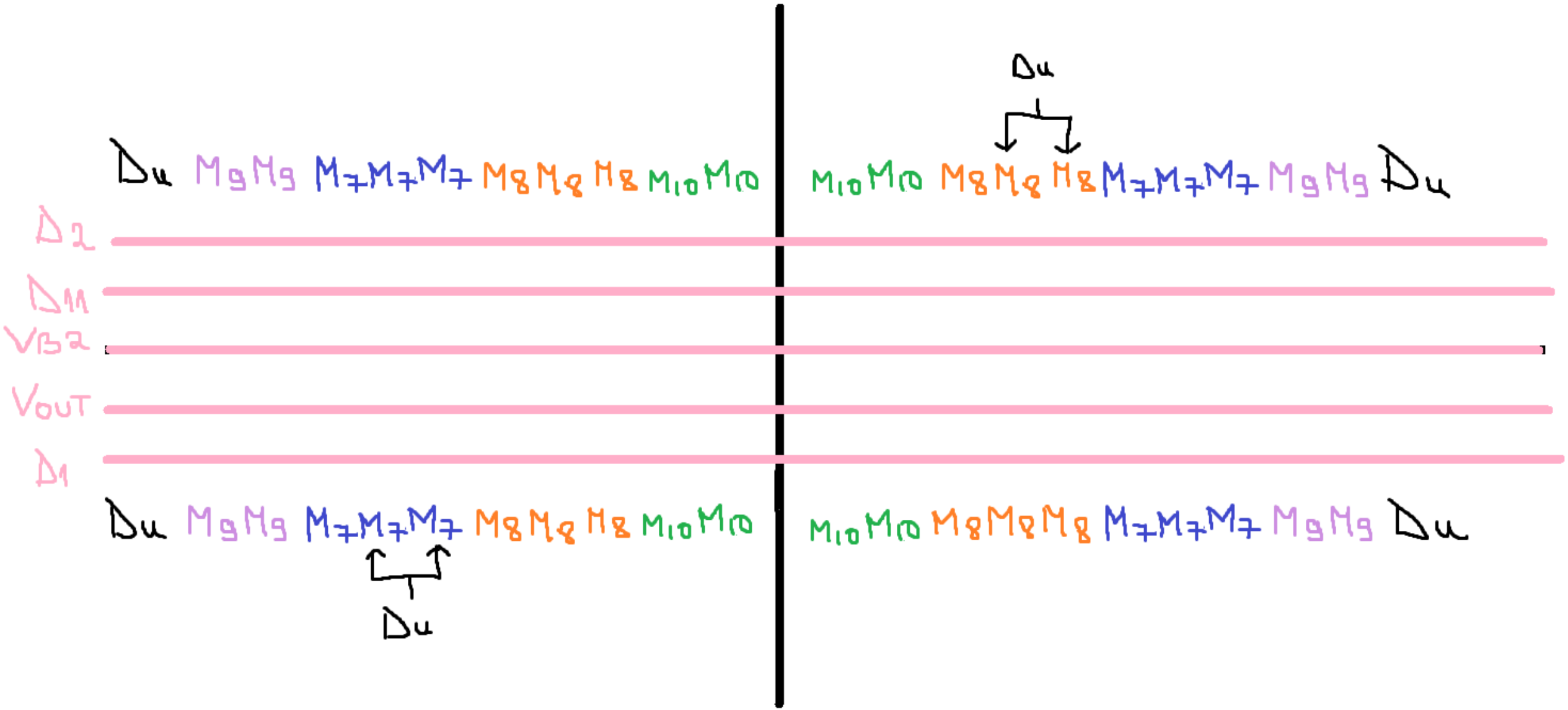
MATCHING – SARCINA P – BLOC 1



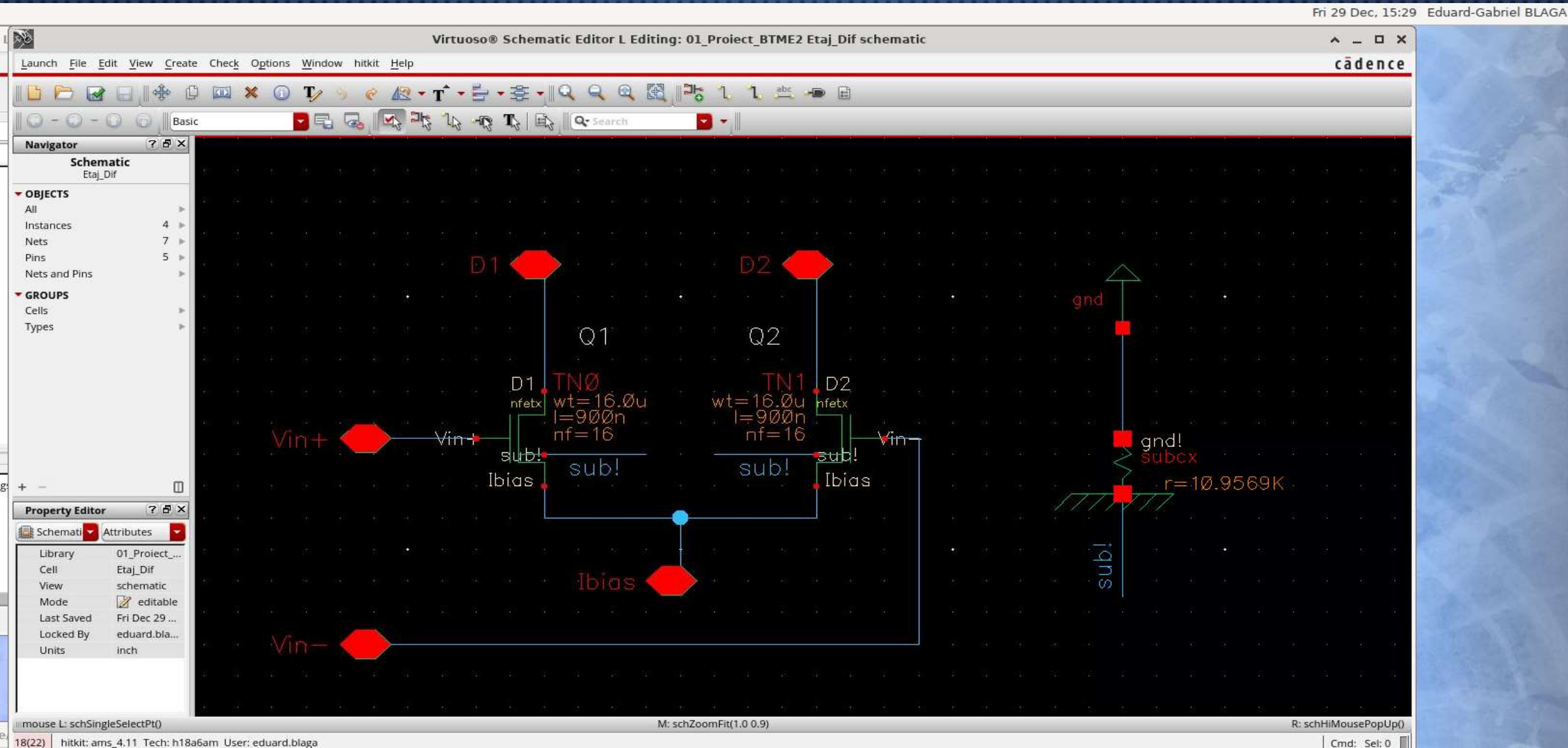
SARCINA P – BLOC 2 - SCHEMATIC



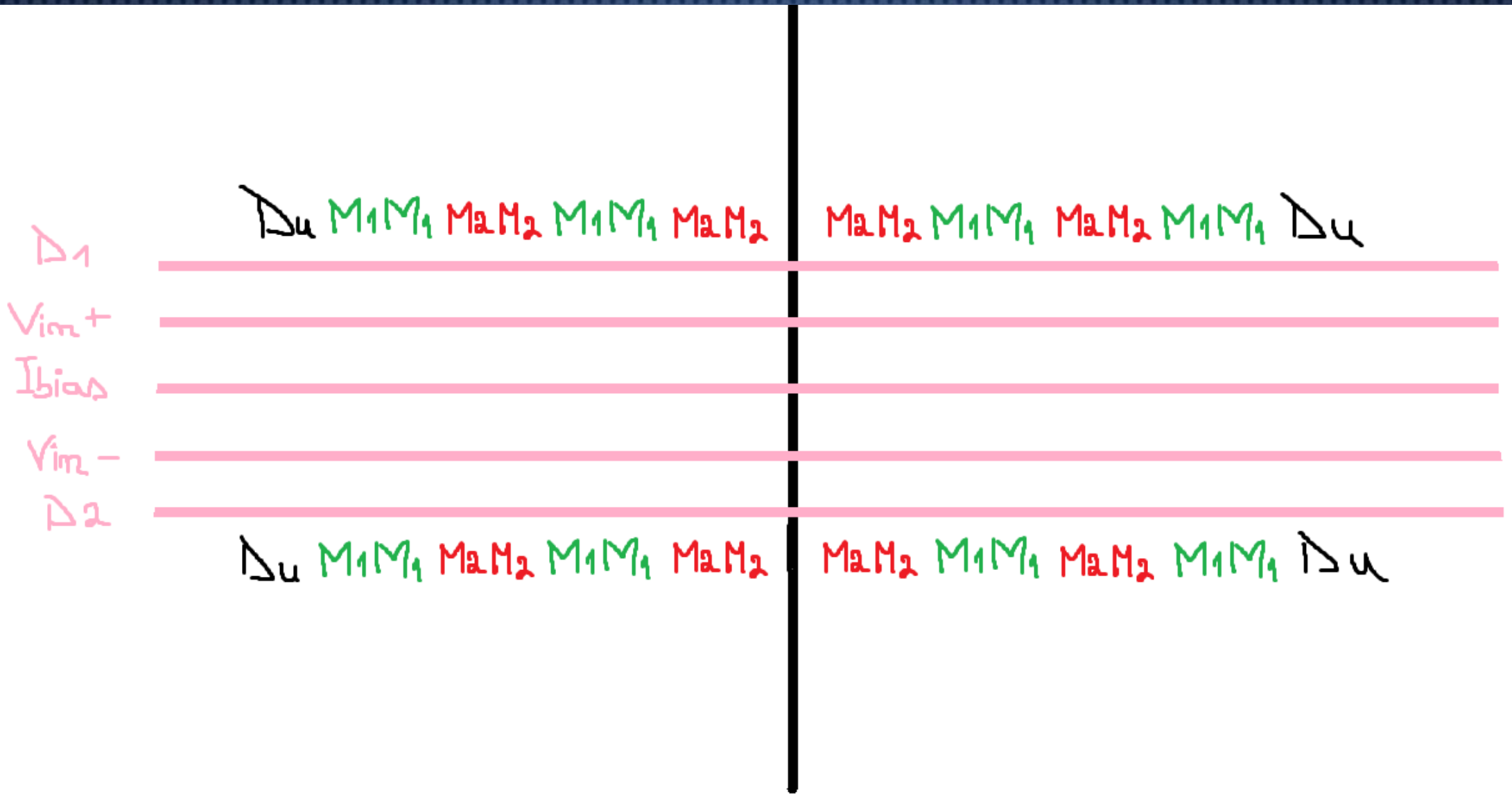
MATCHING – SARCINA P – BLOC 2



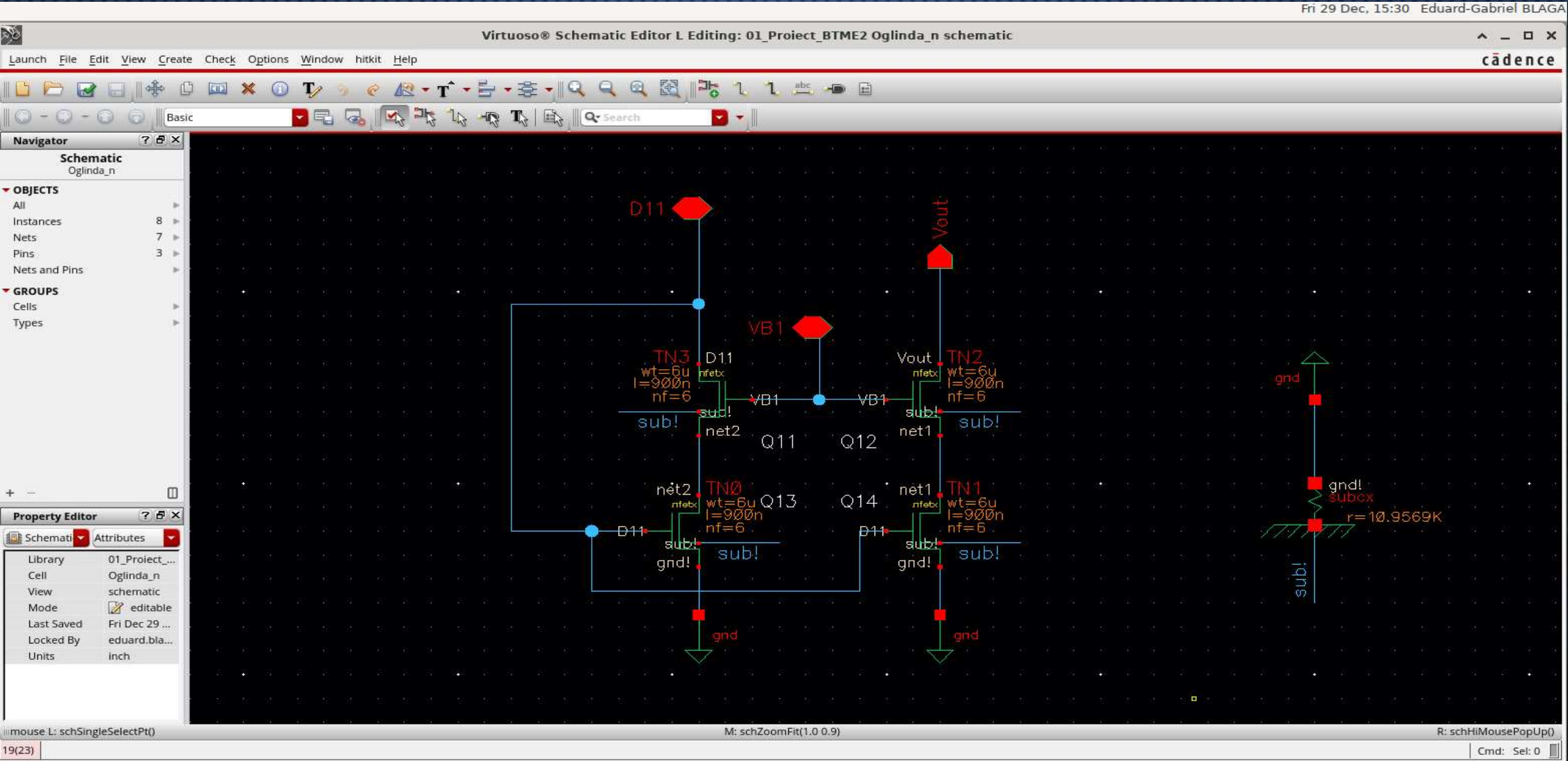
DIFERENTIAL - SCHEMATIC



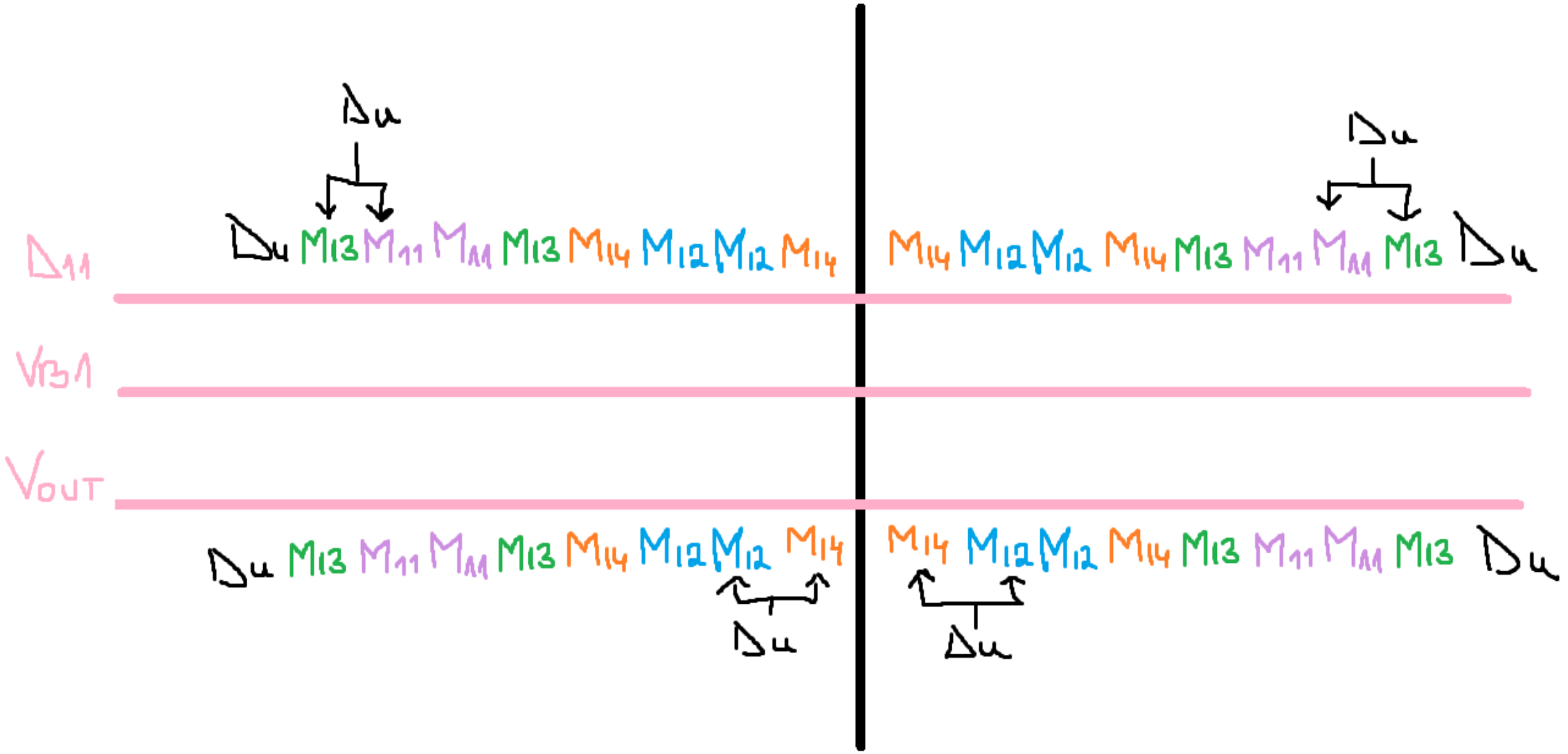
MATCHING – DIFERENTIAL



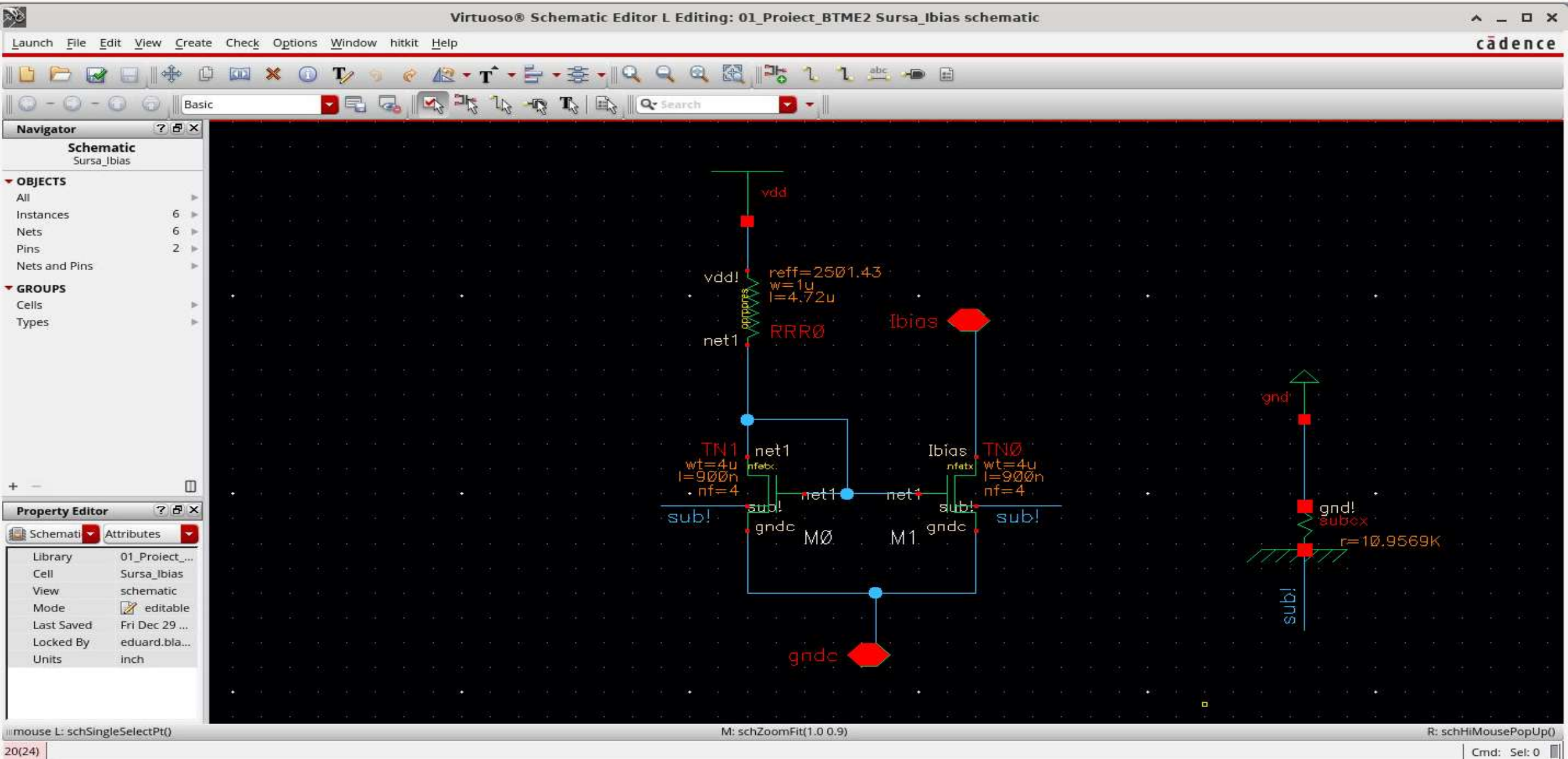
OGLINDA N- SCHEMATIC



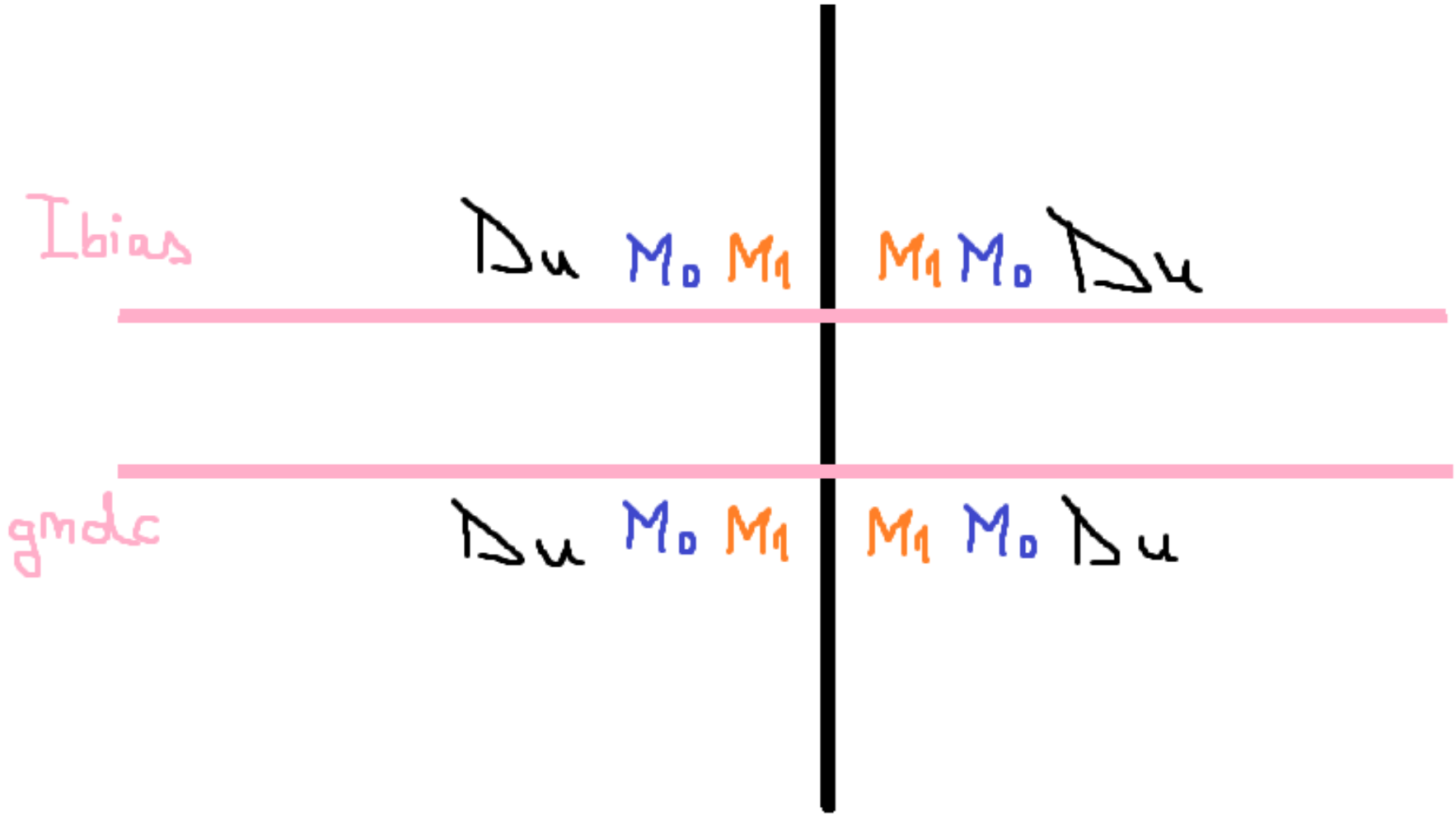
MATCHING – OGLINDA N



SARCINA IBIAS - SCHEMATIC

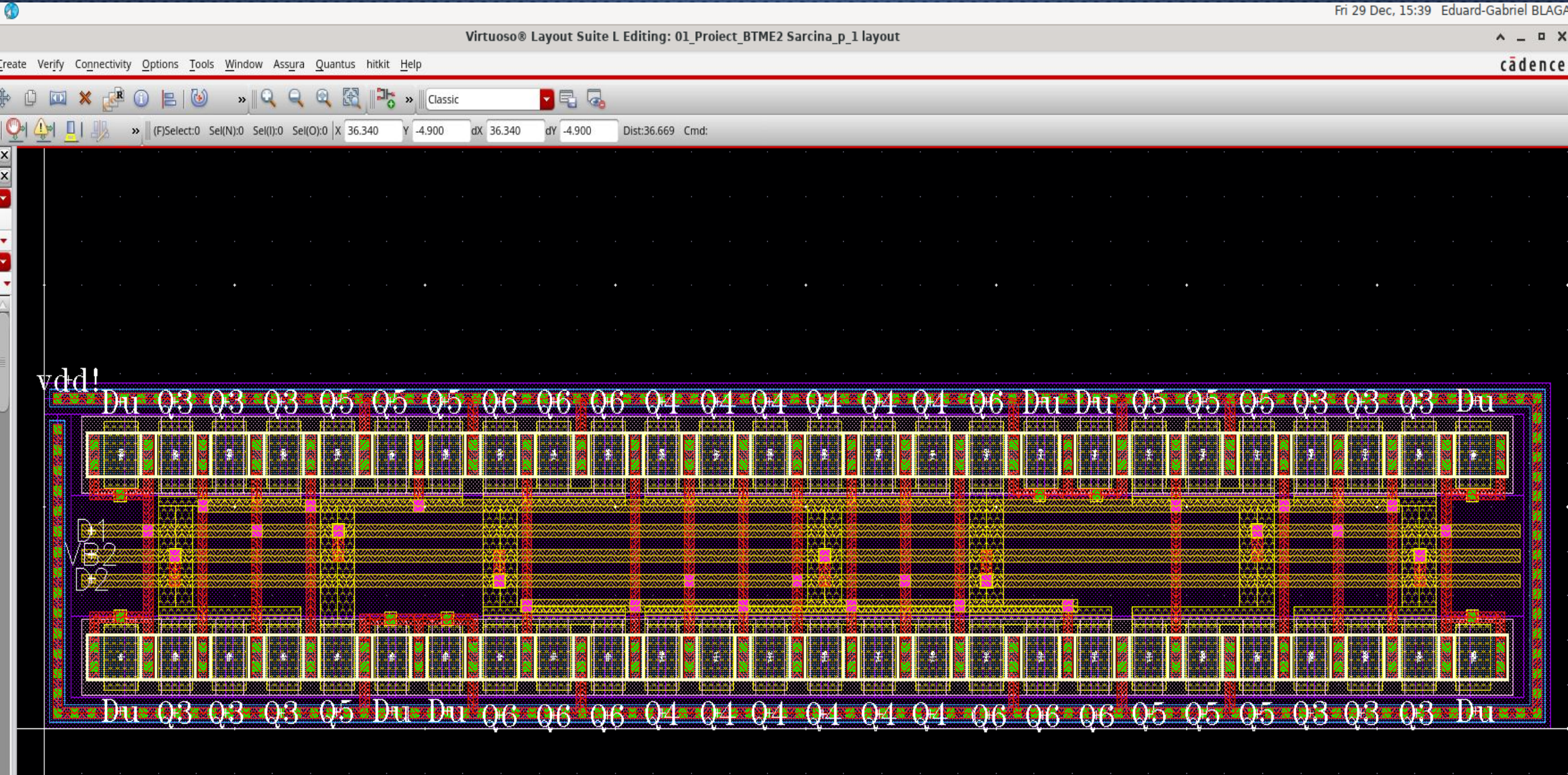


MATCHING – SURSA IBIAS

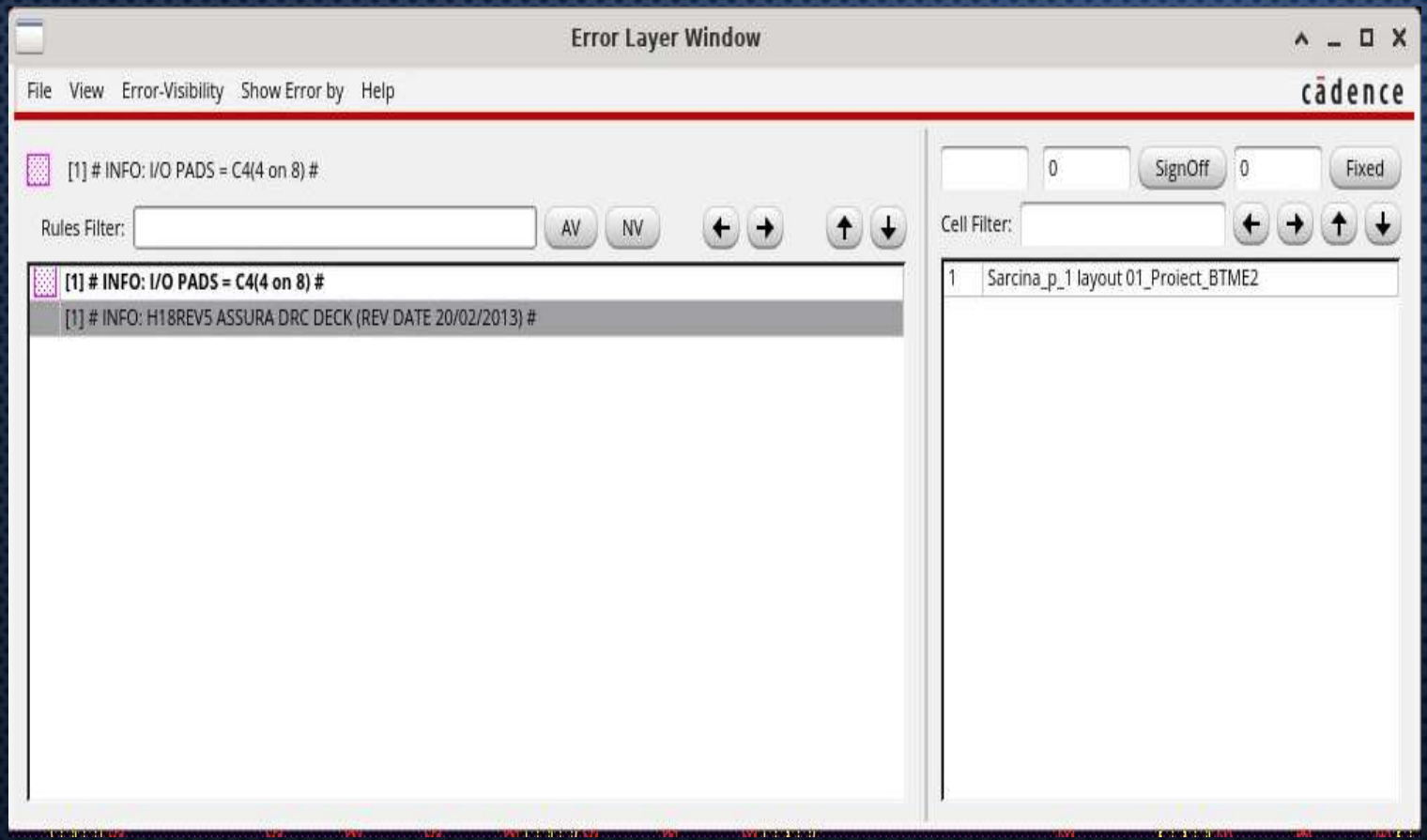


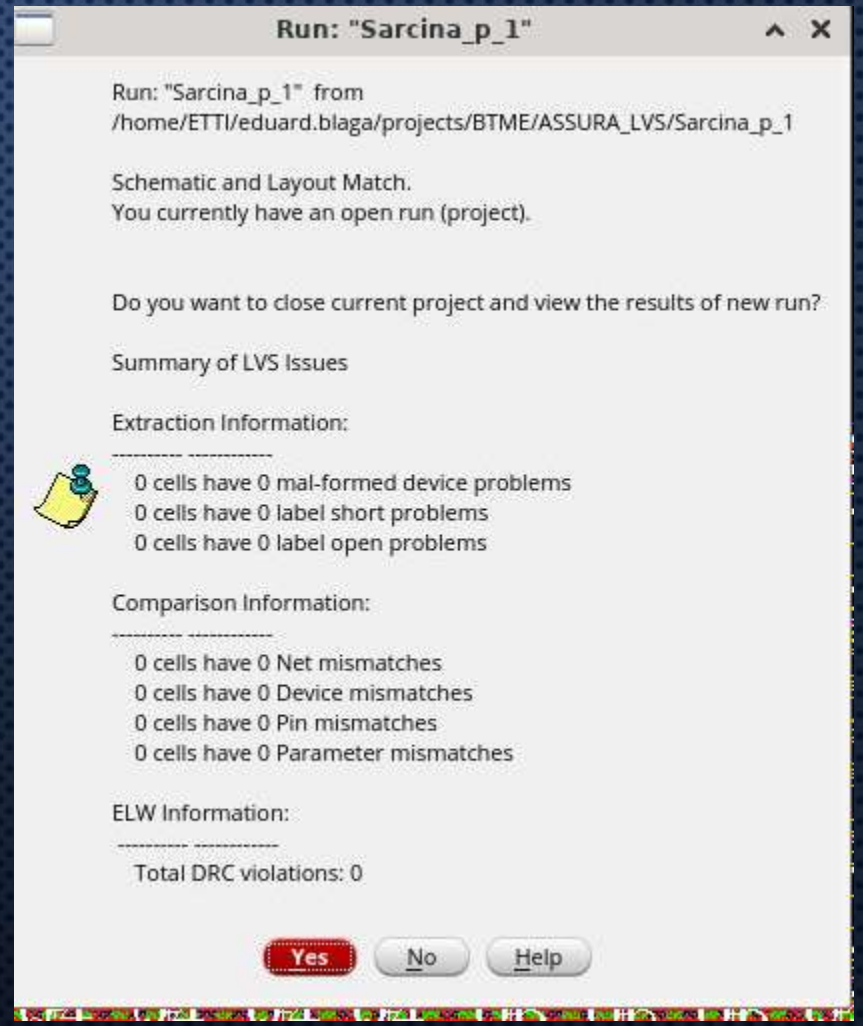
CAPITOLUL 2
LAYOUT

SARCINA P – BLOC 1 - LAYOUT

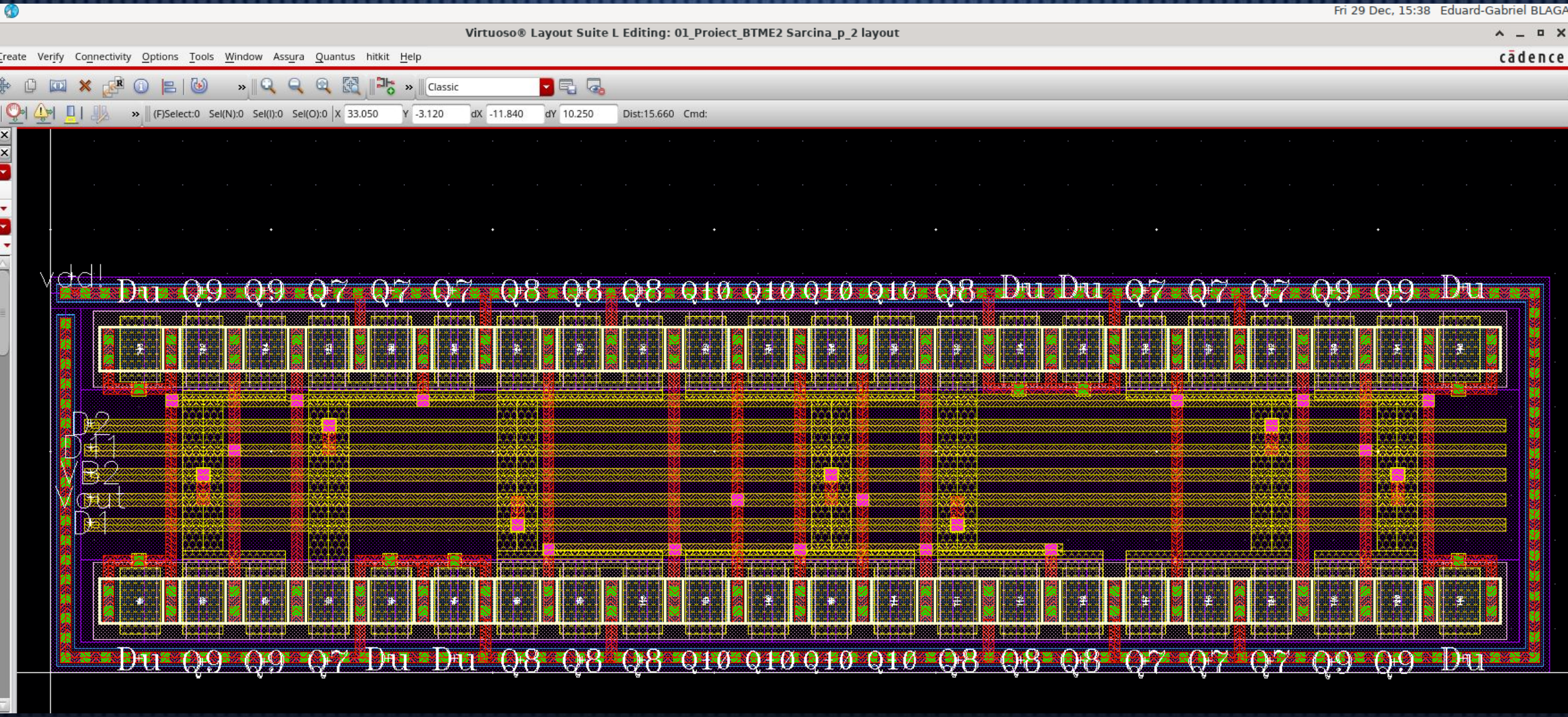


VERIFICARE DRC SI LVS





SARCINA P – BLOC 2 - LAYOUT



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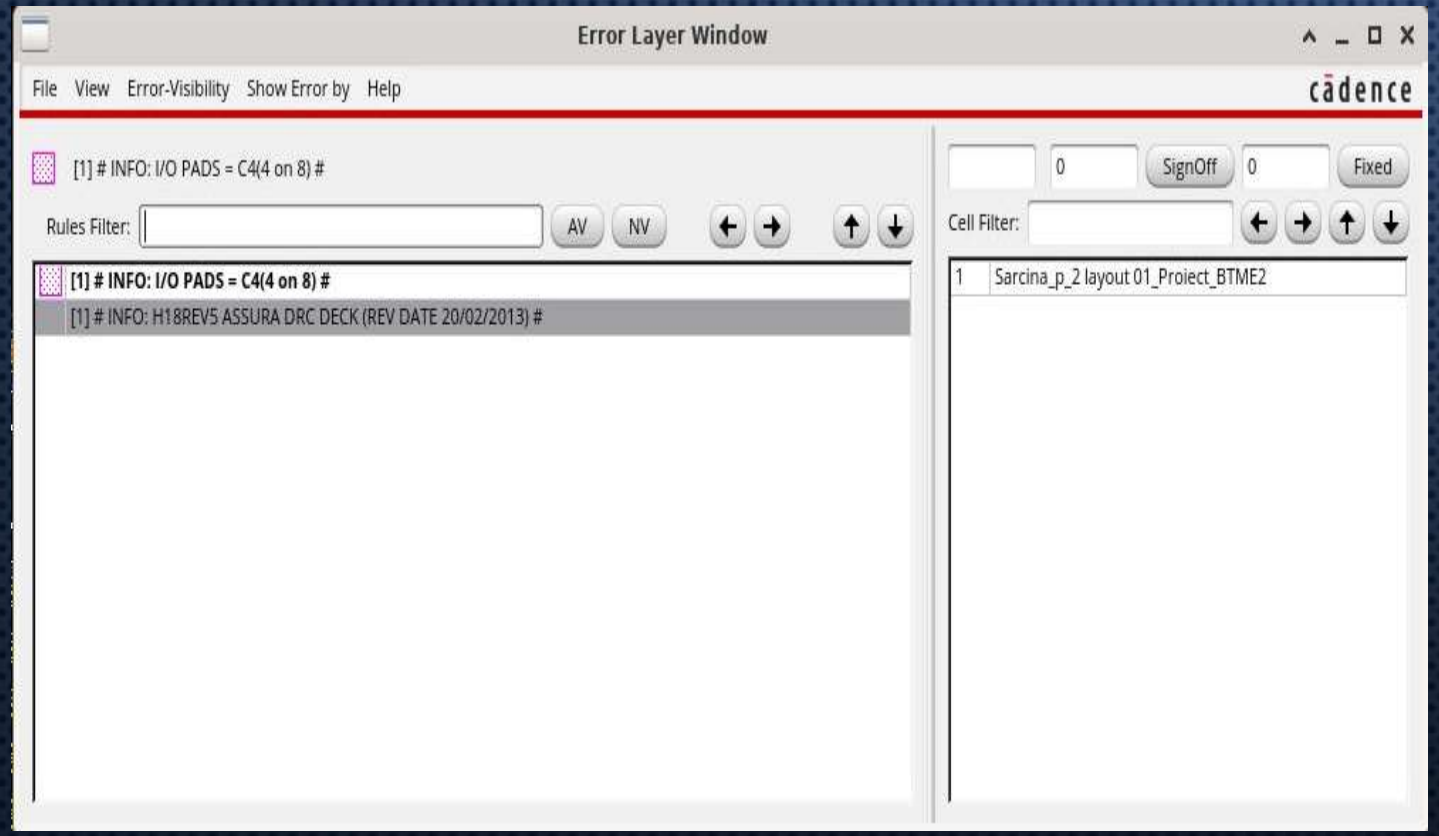
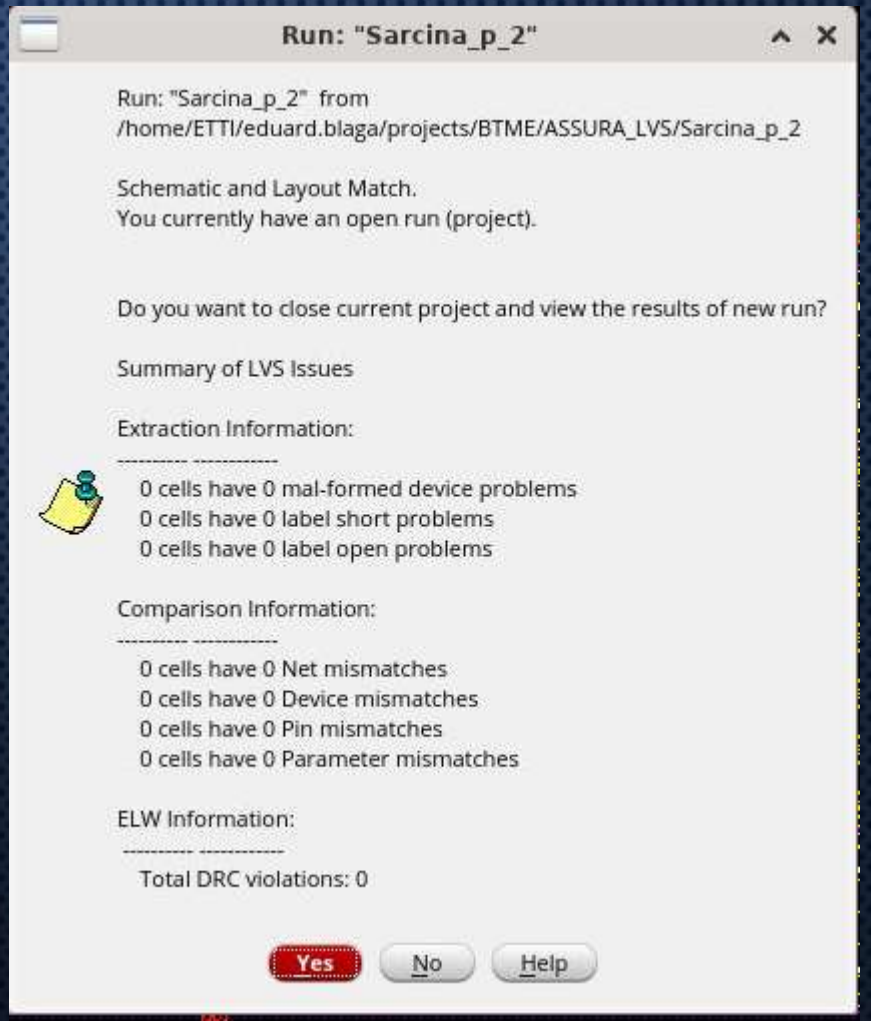
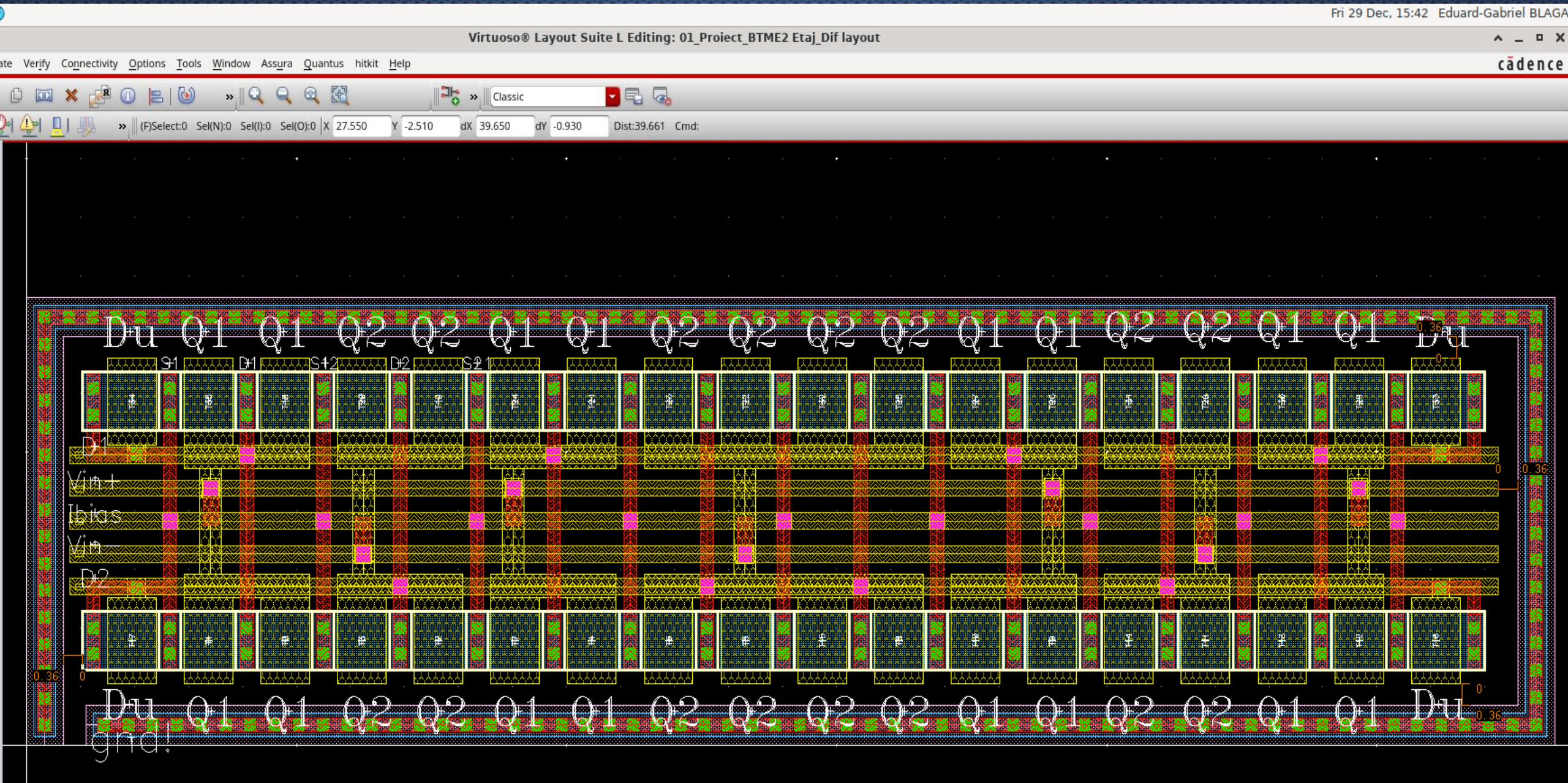




DIFERENTIAL - LAYOUT



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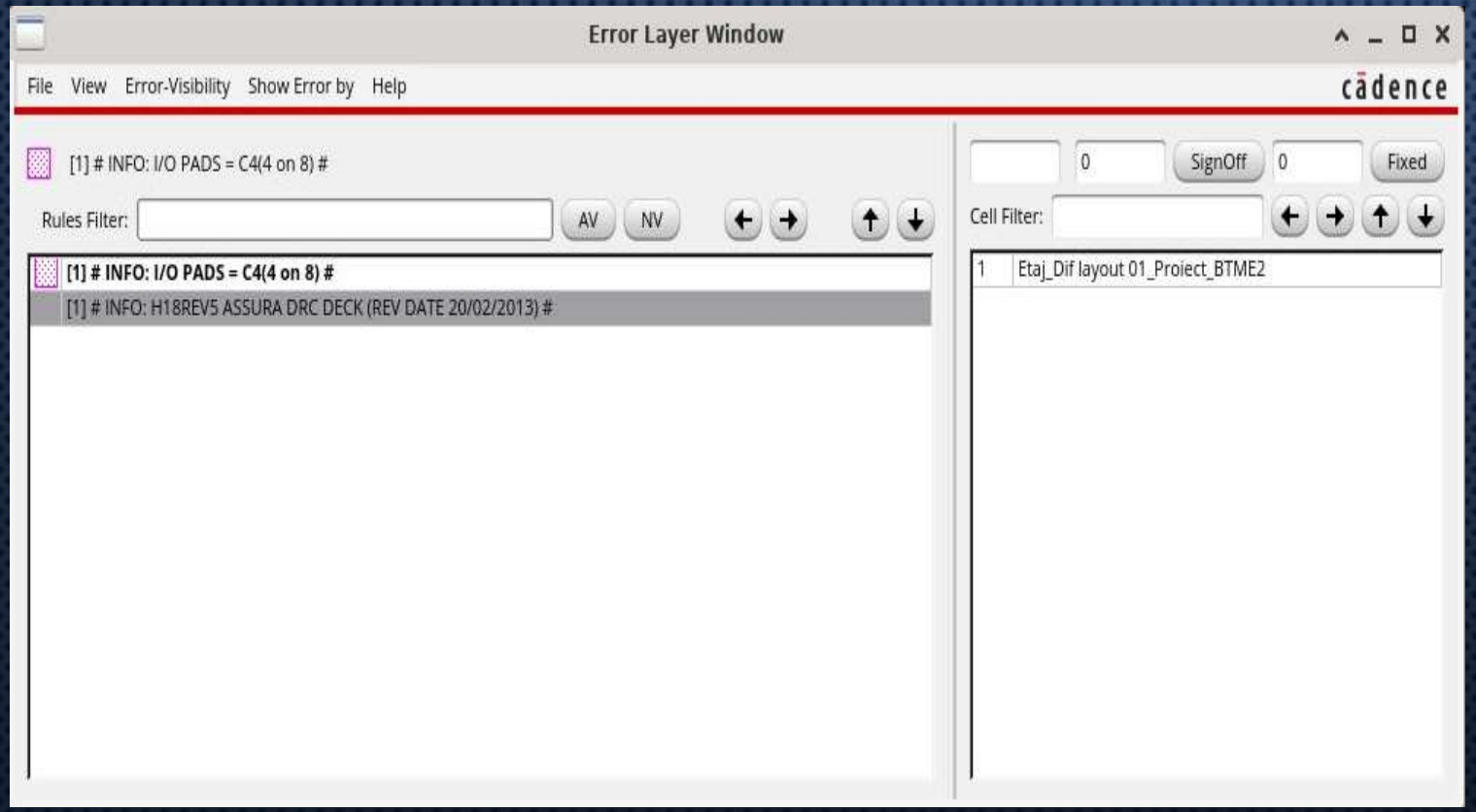
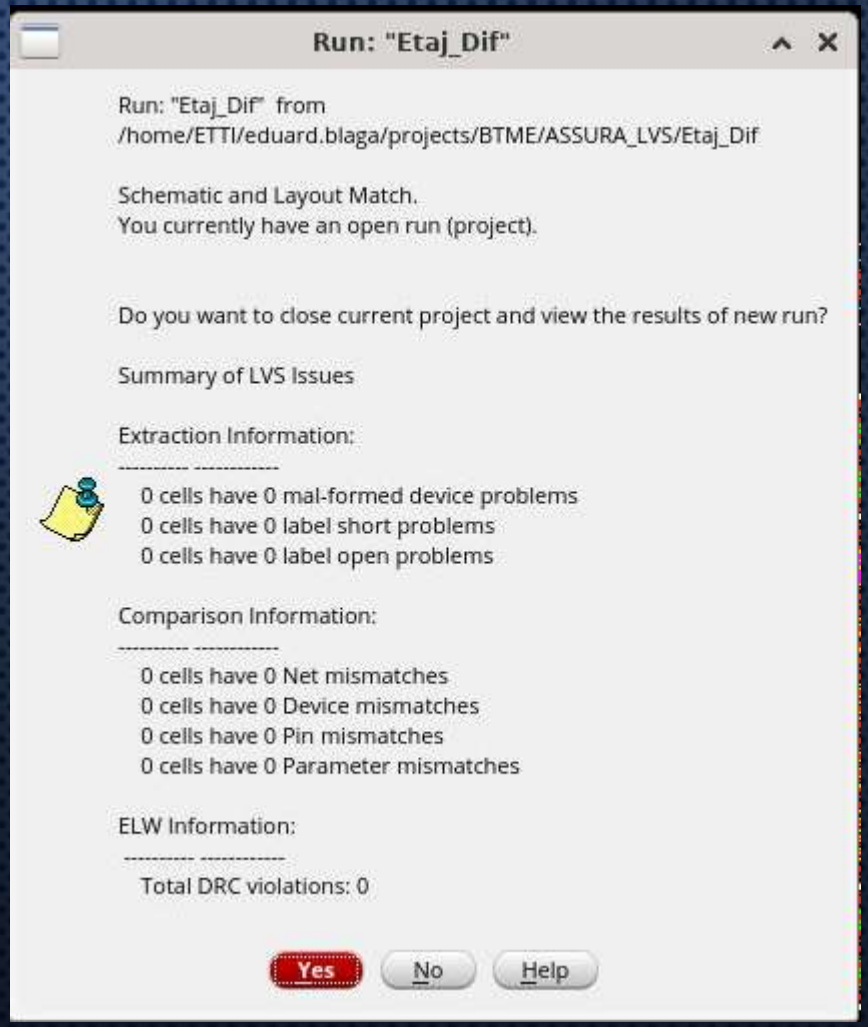
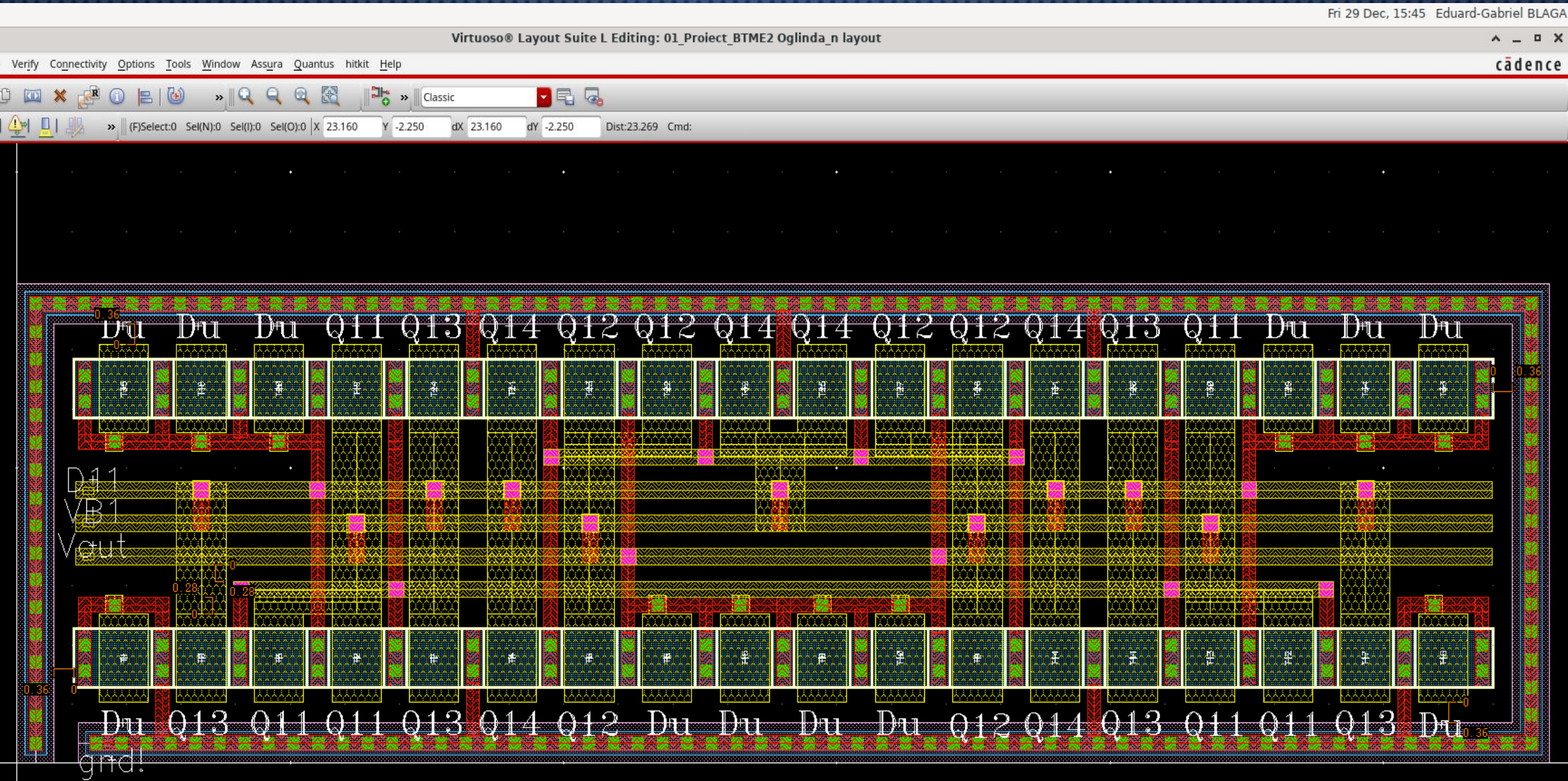




OGLINDA N - LAYOUT



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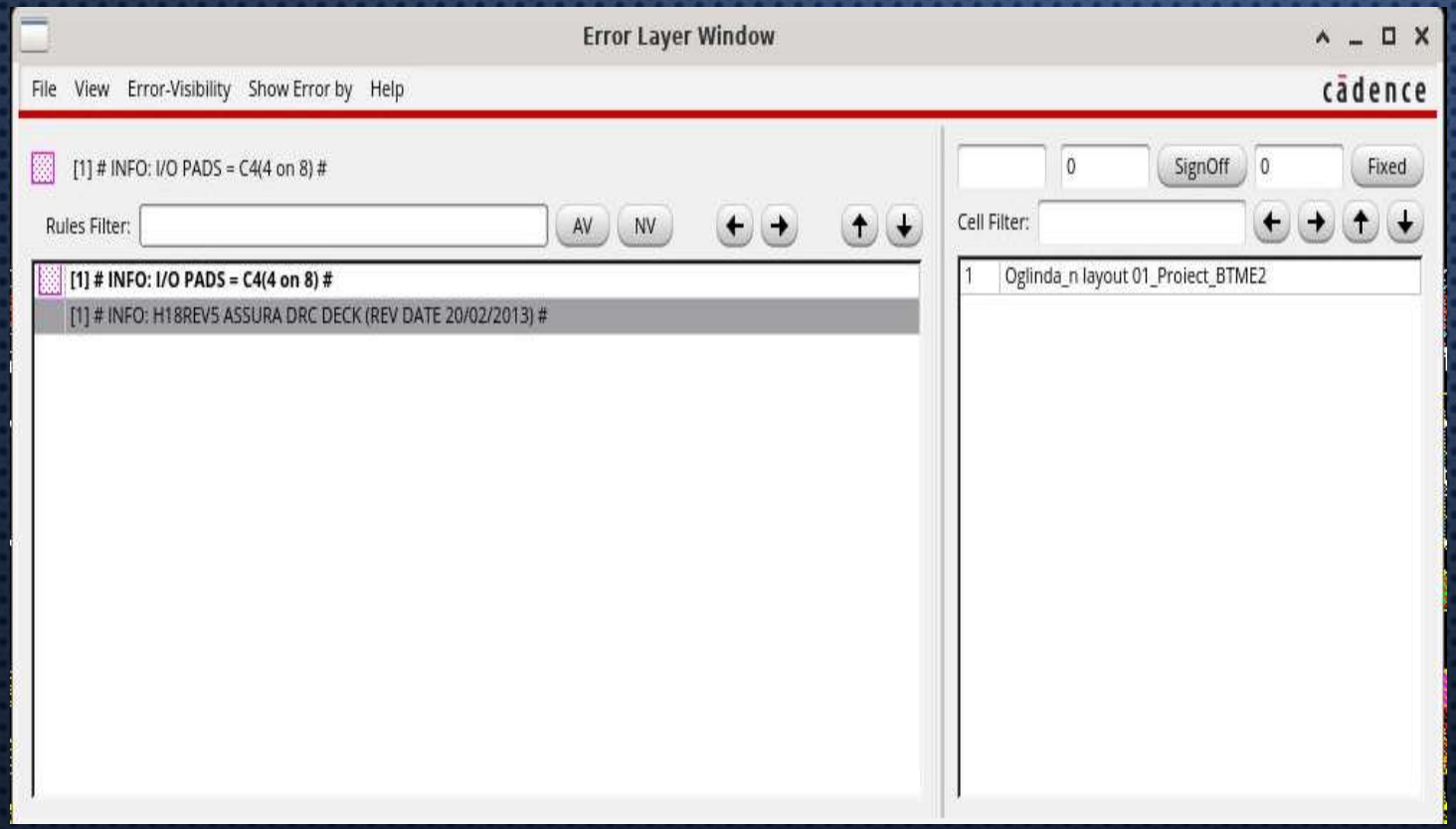
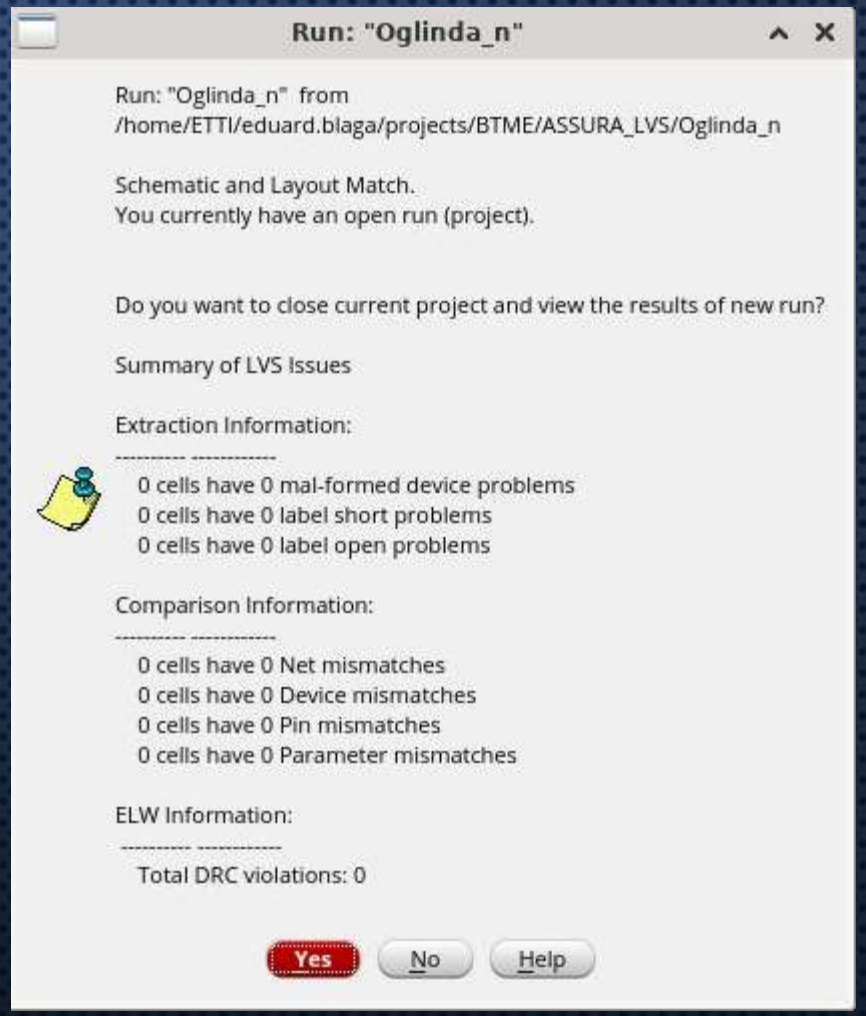
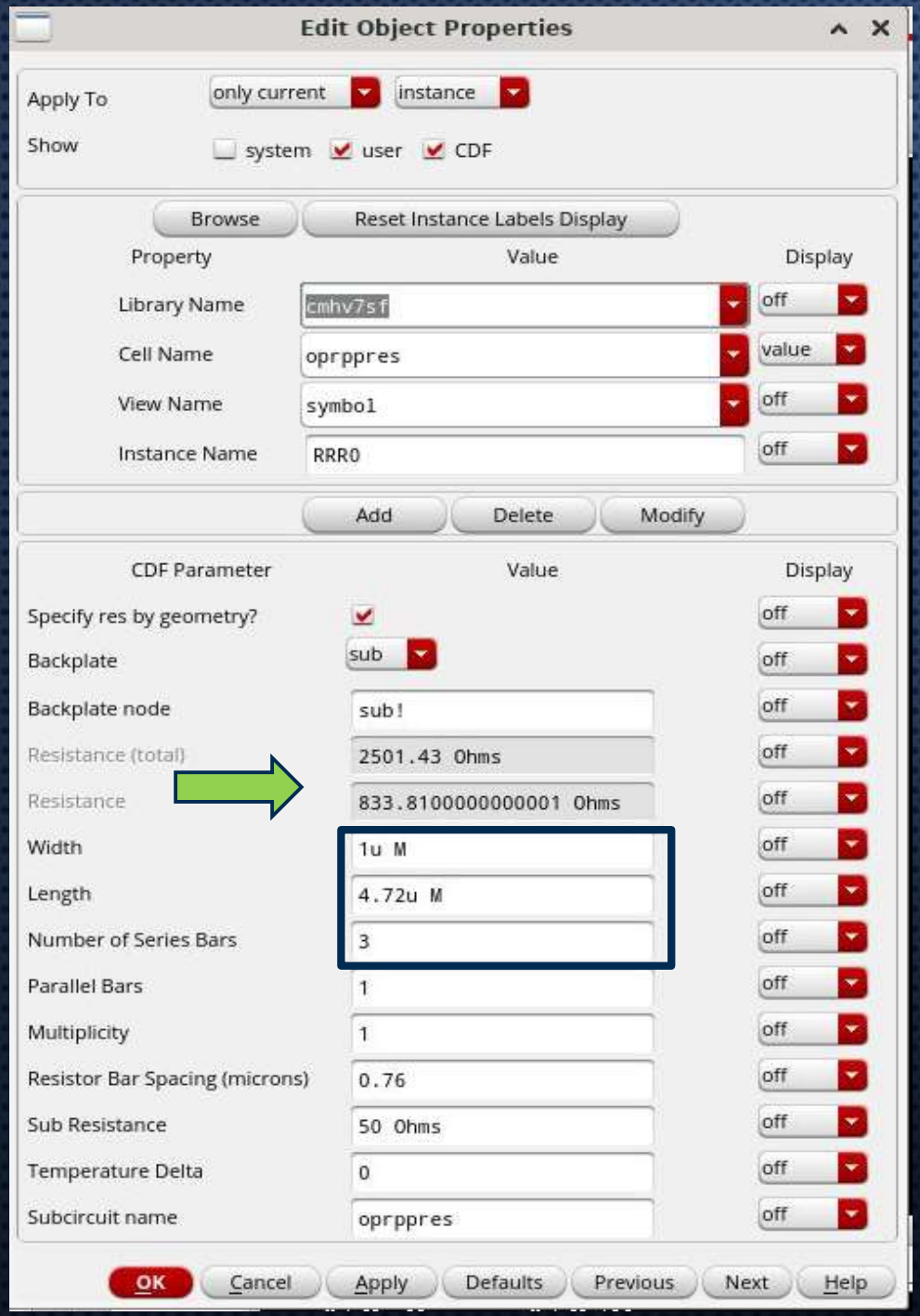
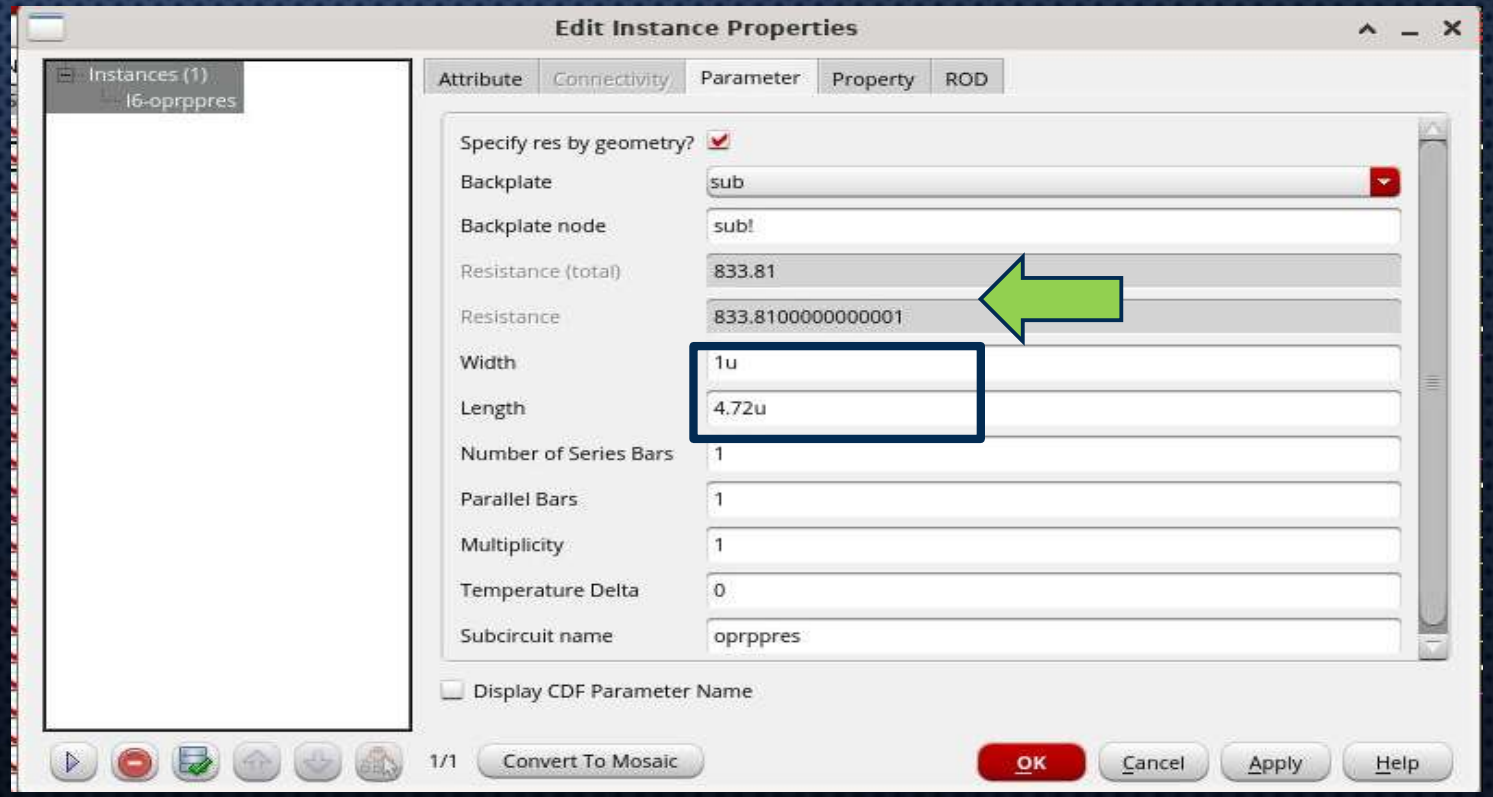


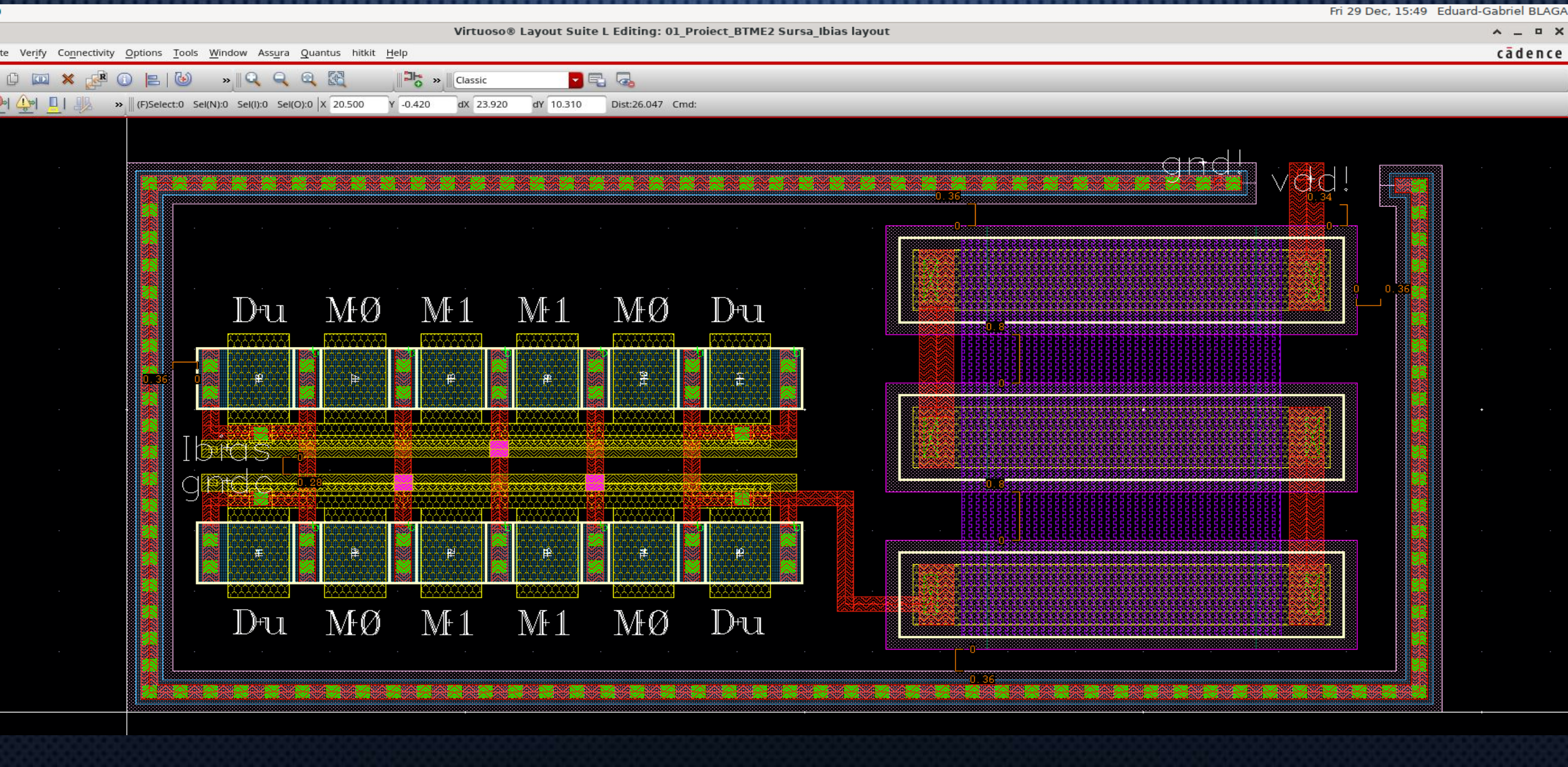


Pentru a obtine un layout mai compact in cadrul sursei IBIAS, am inseriat 3 rezistente oprppres conectate cu metal M1. Pentru a obtine aceeasi valoare si in layoutsi in schematic, modificam parametrul rezistentei din schematic ca in imagine. La final, in partea de layout va trebui sa umplem spatiul gol dintre rezistente cu un strat de OP (drw)

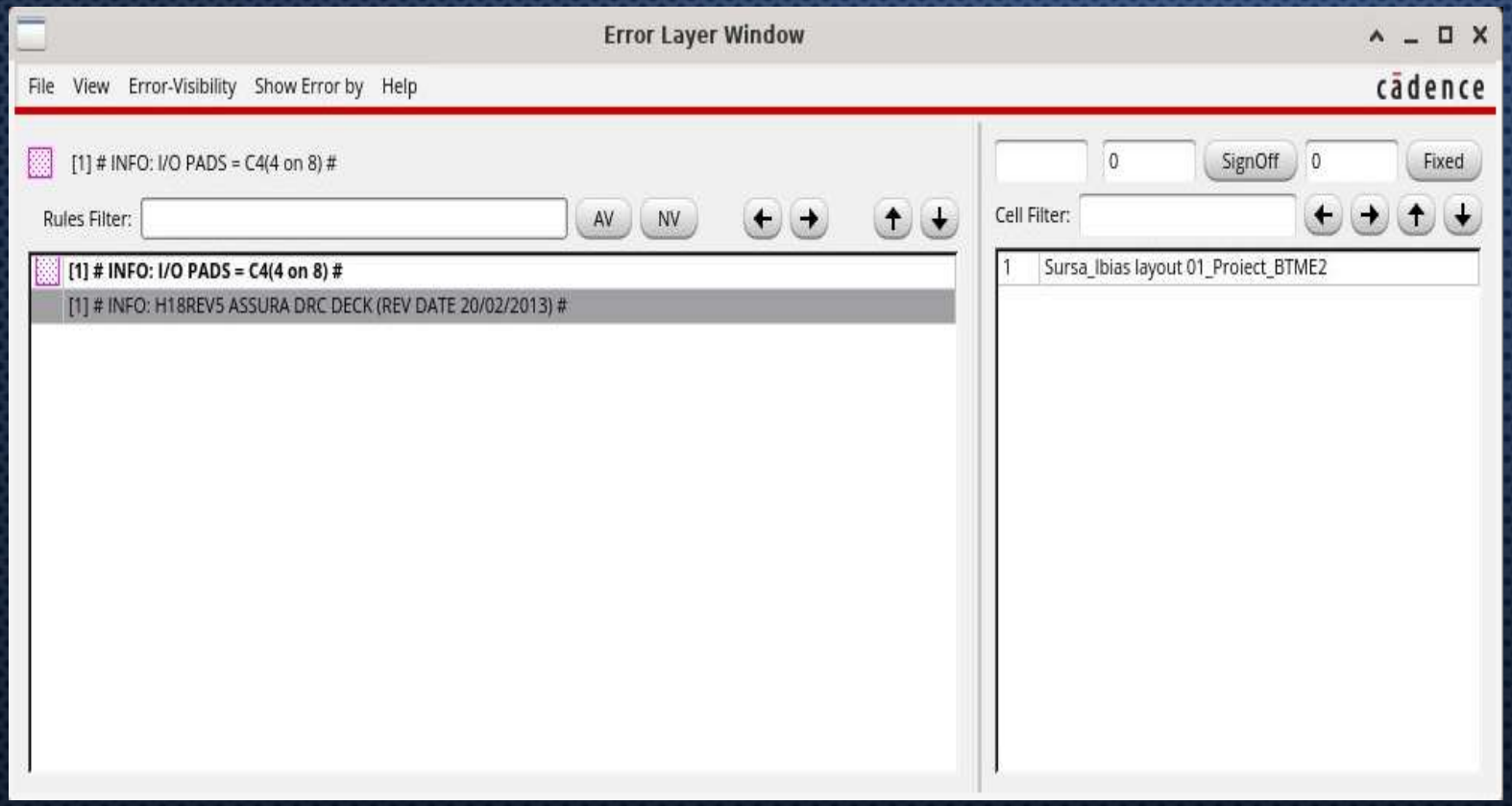




SURSA IBIAS - LAYOUT

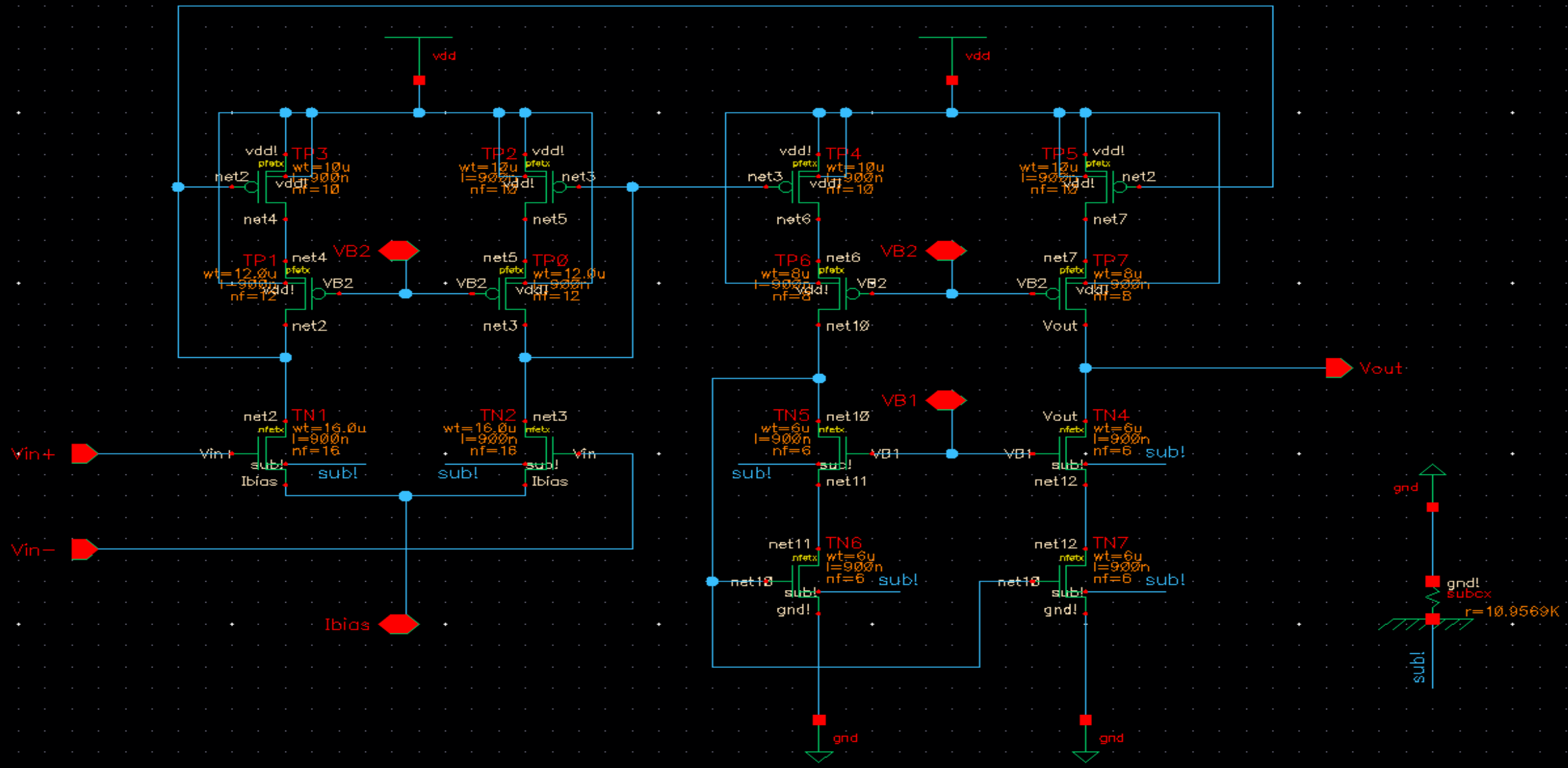


VERIFICARE DRC SI LVS

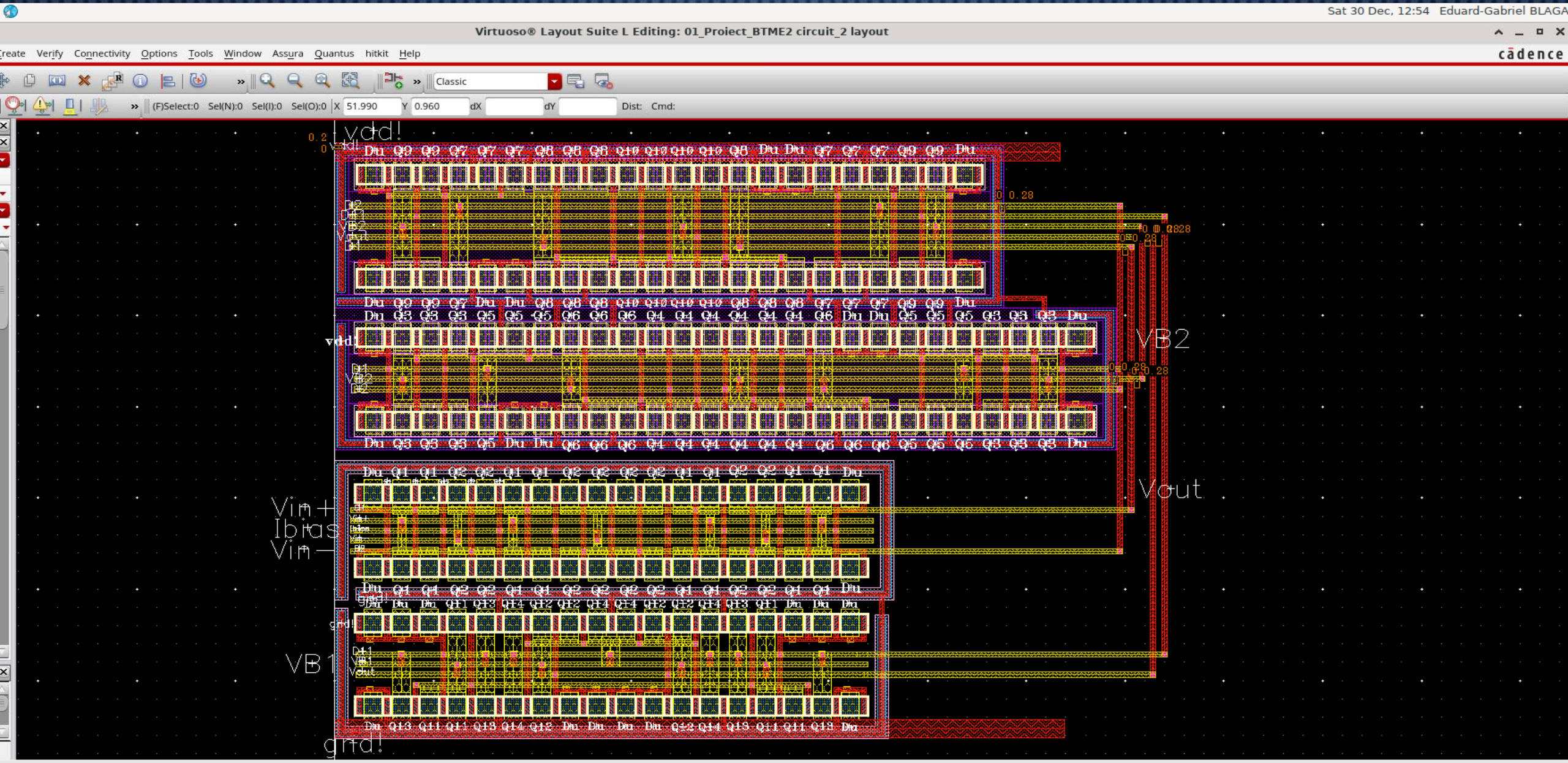


CAPITOLUL 3
CIRCUITUL FINAL

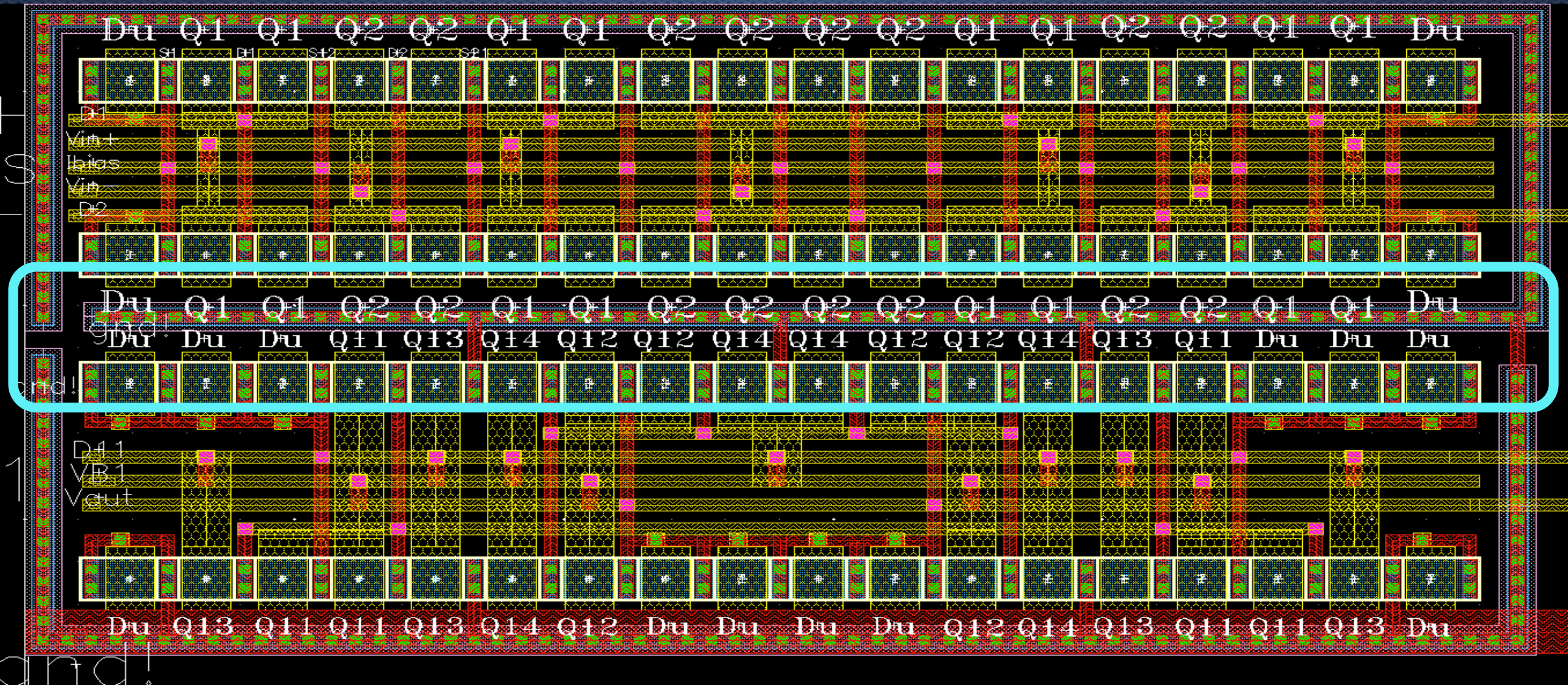
SCHEMATICUL CIRCUITULUI



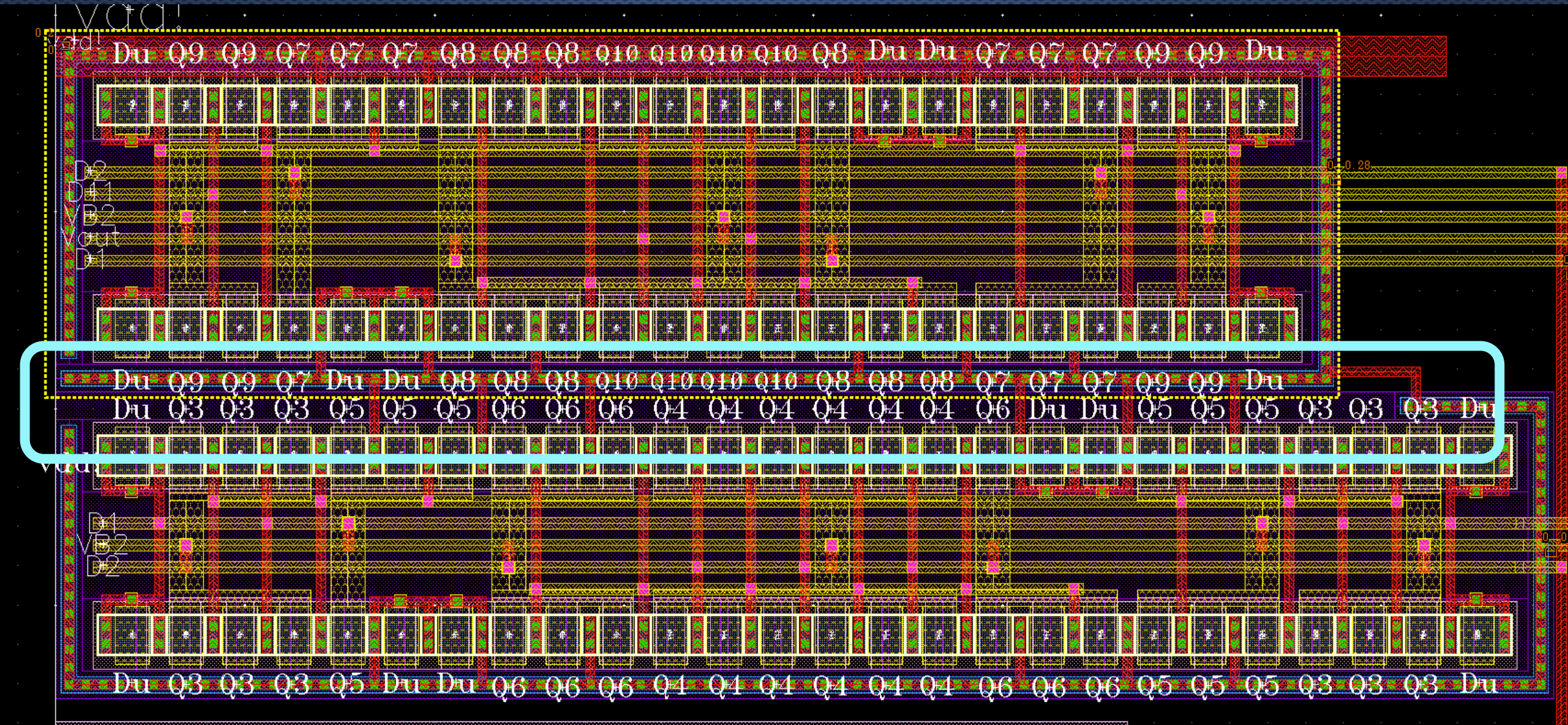
LAYOUT-UL CIRCUITULUI



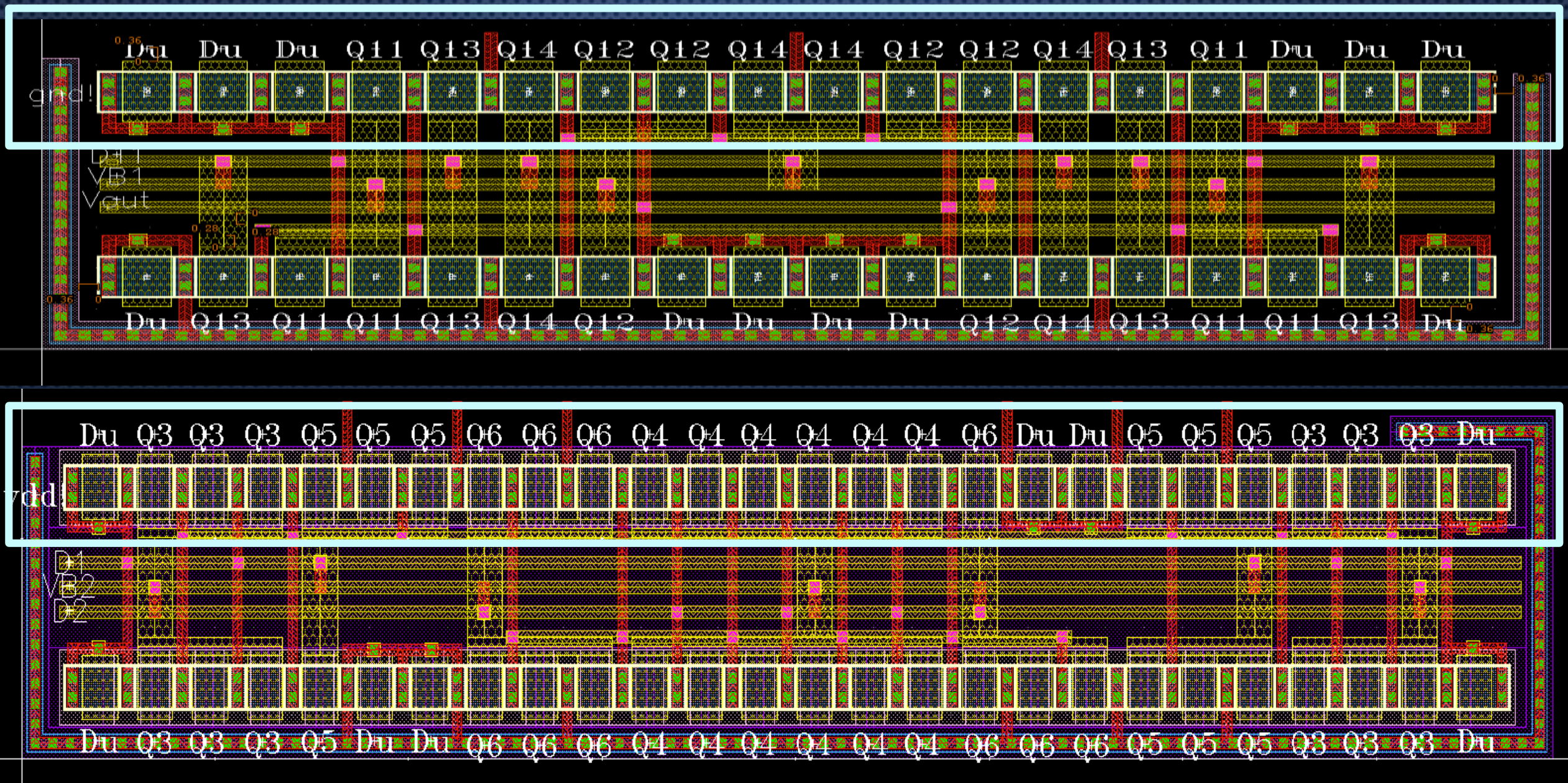
PENTRU CACIRCUITUL SA TREACA DE SIMULAREA LVS TREBUIE SA MODIFICAM LAYOUTURILE INITIALE IN CAZUL BLOCURILOR CU ACELEASI LINII DE GND SI VDD, ASTFEL INCAT SA LE INTERCONECTAM LA ACEEASI LINIE



PENTRU CACIRCUITUL SA NU DEA EROARE LA SIMULAREA LVS TREBUIE SA MODIFICAM LAYOUTURILE INITIALE IN CAZUL BLOCURILOR CU ACELEASI LINII DE GND SI VDD, ASTFEL INCAT SA LE INTERCONECTAM LA ACEEASI LINIE



SURSELE CARE ERAU INITIAL CONECTATE LA LINIA DE GND LE VOM PRELUNGI CU ACEEASI DISTANTA ASTFEL INCAT SA VINE CONECTATE LA LINIA DE GND A URMATORULUI BLOC. ACEEASI ANALOGIE SE APLICA SI IN CADRUL BLOCURILOR CU VDD



VERIFICARE DRC SI LVS