

Proiect BTME1 2023

Numarator binar asincron cu 13 stari cu bistabil D_v3

Student : Blaga Eduard Gabriel

Grupa : 5313

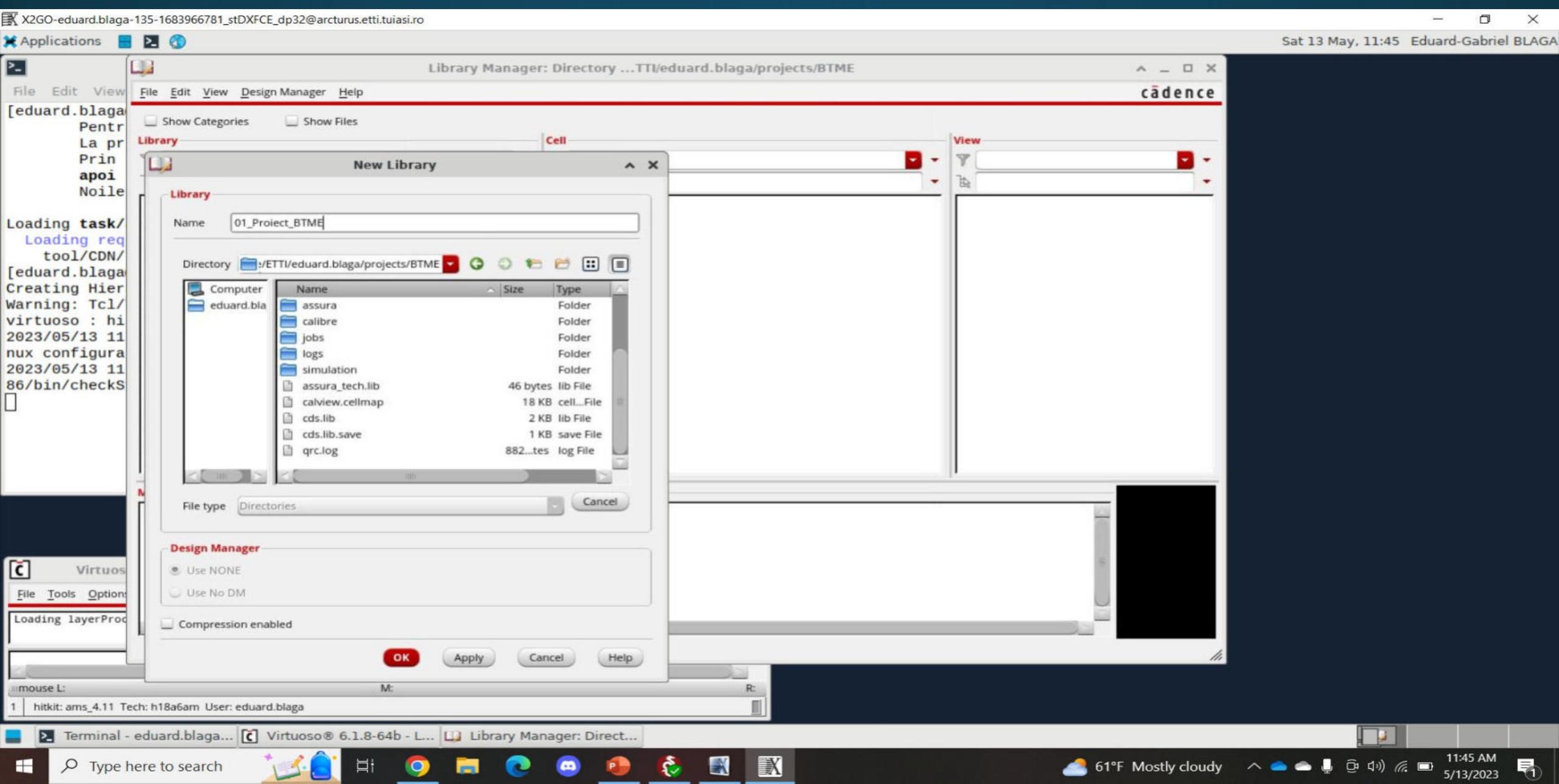
Tema Numarul : 13

Profesor indrumator
Asist. Dr. Ing. Nicolae
Patache

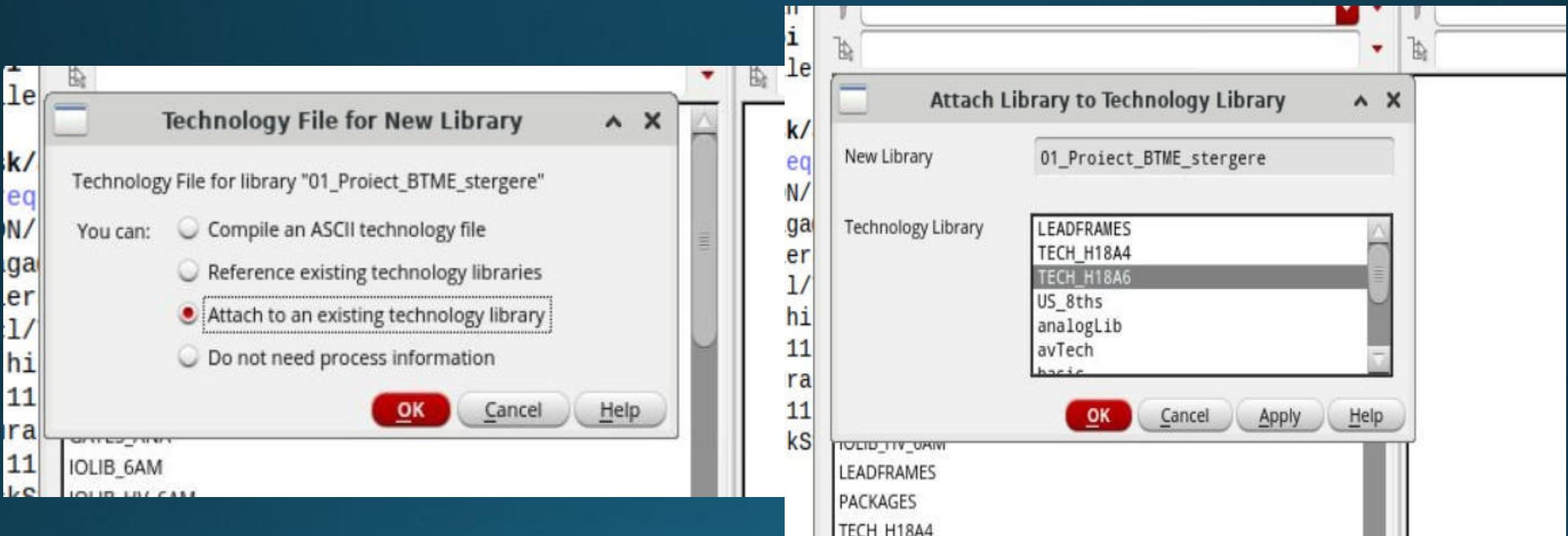
Cerinte

- ❖ **Etapa1 saptamana 11** - Sa se proiecteze portile logice necesare fiecarui tip de bistabil realizandu-se simularea si layout-ul aferent pornind de la tranzistoare NMOS cu $L=0.7\mu$ si $W=1\mu$ (se va determina W -ul pentru tranzistoarele PMOS astfel incat punctul de comutare sa fie la jumatea tensiunii de alimentare)
- ❖ **Etapa2 saptamana 12** - Sa se realizeze schema ierarhizata a numaratorului cu intrarile set, reset, clk si iesirile Q0, Q1, Q2, Q3, simularea si verificarea functionalitatii
- ❖ **Etapa3 saptamana 13** - Sa se realizeze layoutul numaratorului, cu arie minima si fara erori DRC sau LVS
- ❖ **Etapa4 saptamana 14** - Sa se realizeze o prezentare (.pptx) ce va contine prezentarea circuitului, rezultatele similarilor si detalii despre layout (mod de plasare, rutare si verificari)

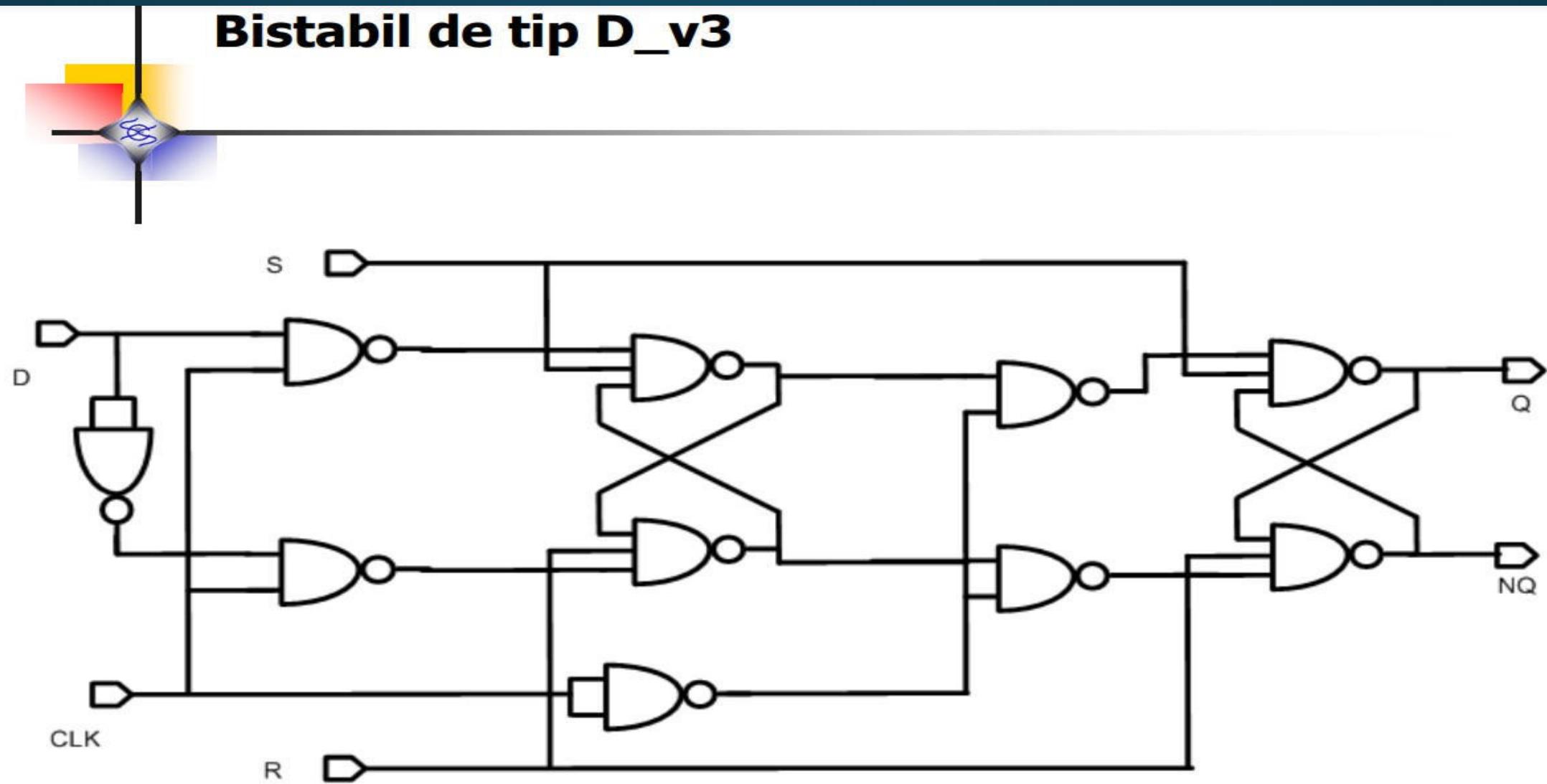
Se realizeaza o librarie noua in care vom lucra



Avem grija sa selectem tehnologia H18A6



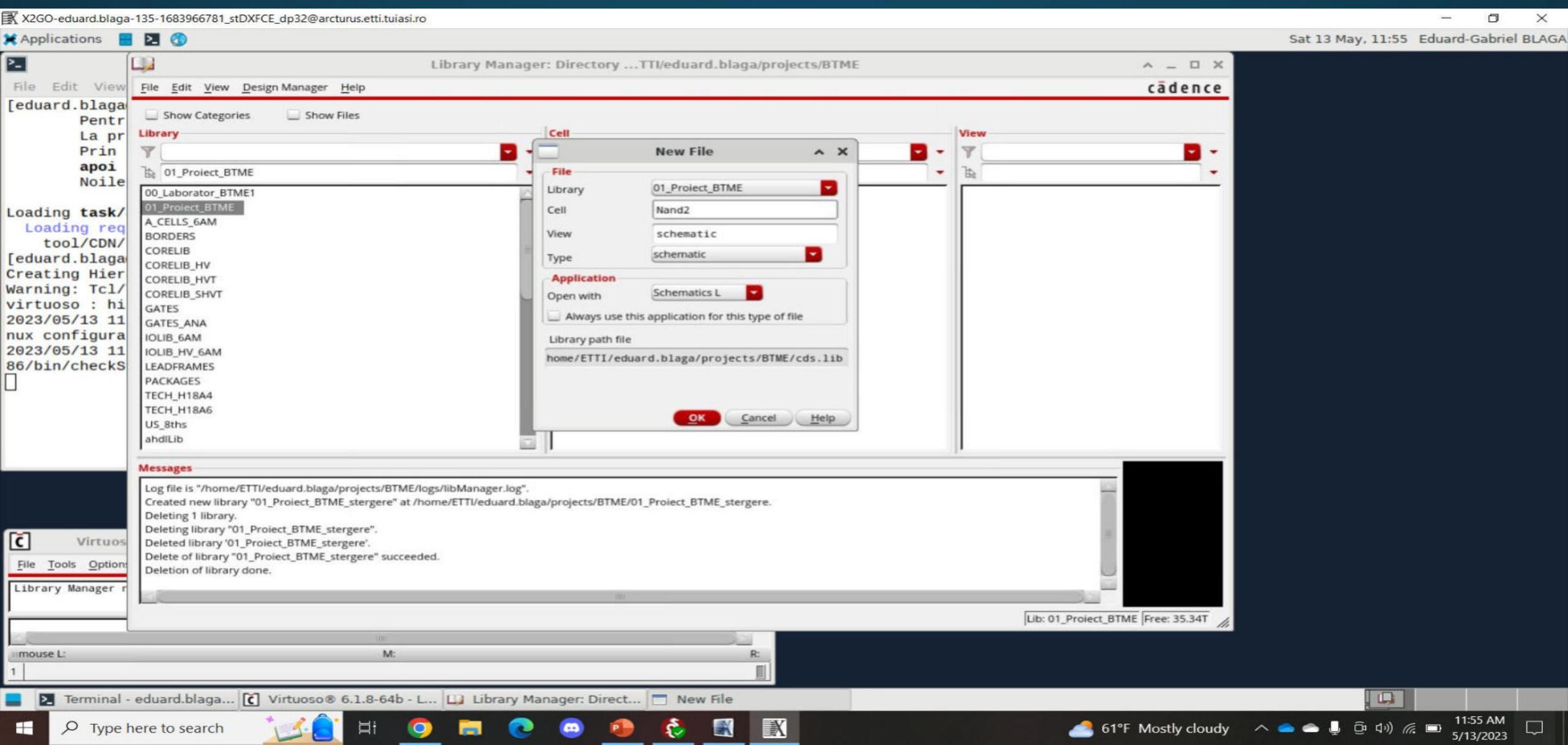
Schema bistabilului D_v3 necesar pentru construirea numaratorului



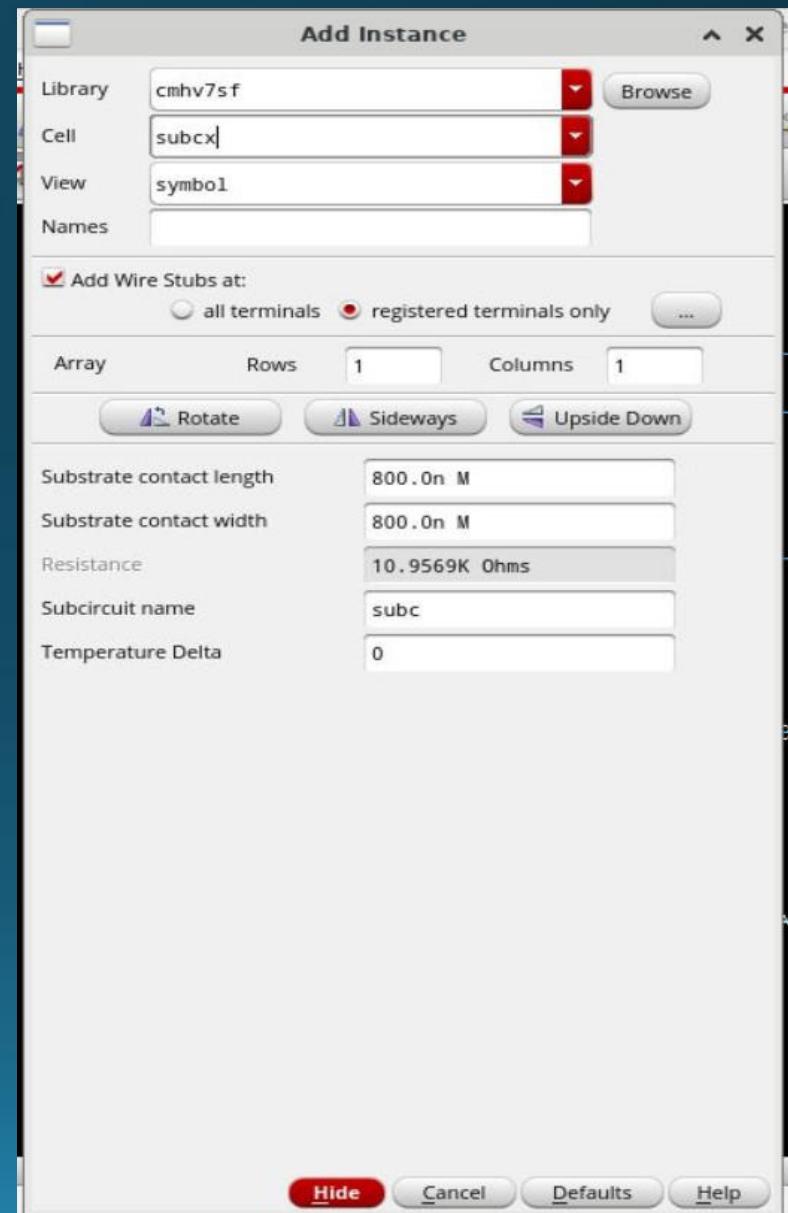
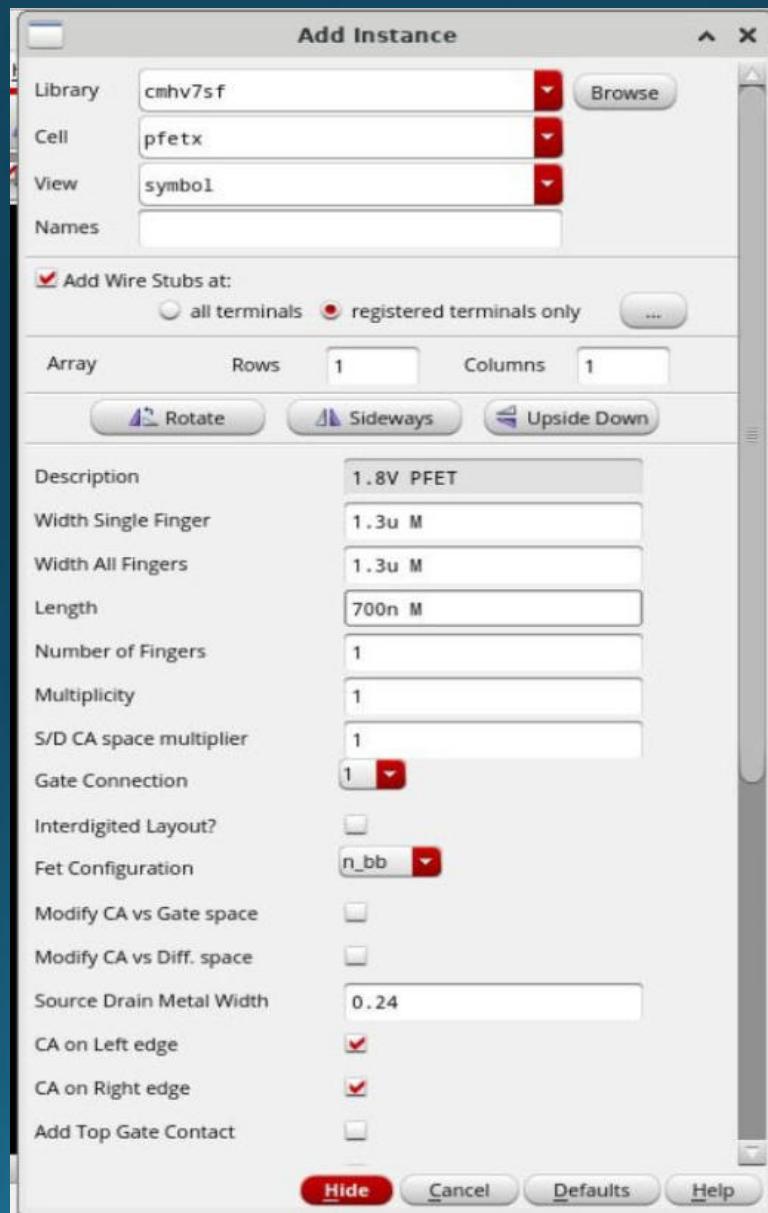
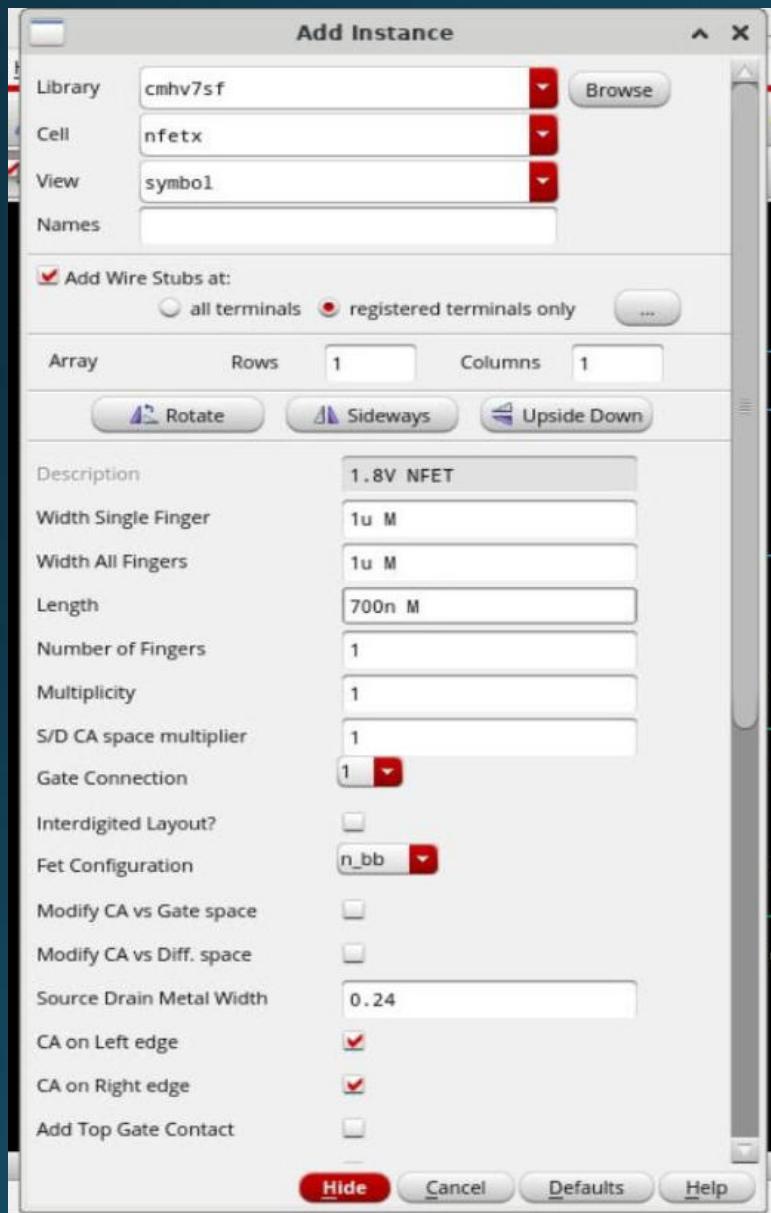


NAND 2

Se realizeaza un cell view de tip schematic pentru poarta nand 2

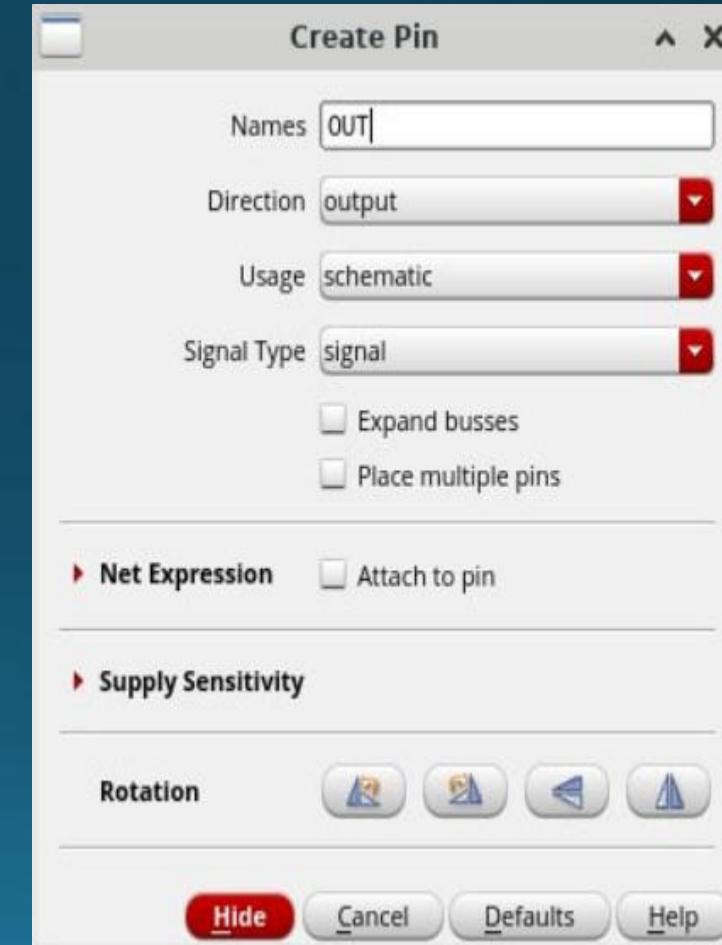
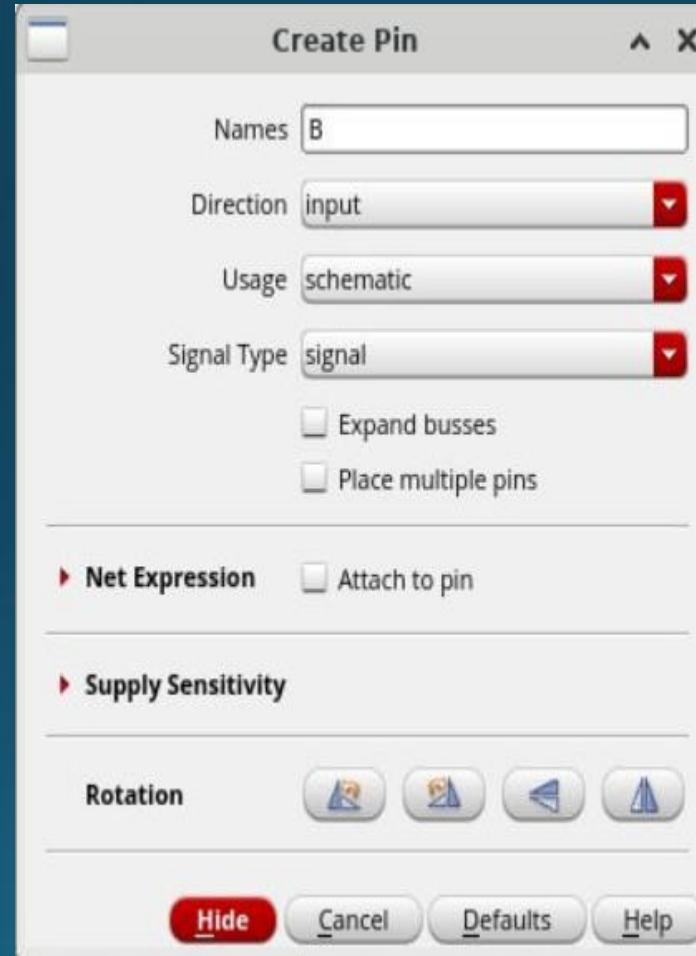
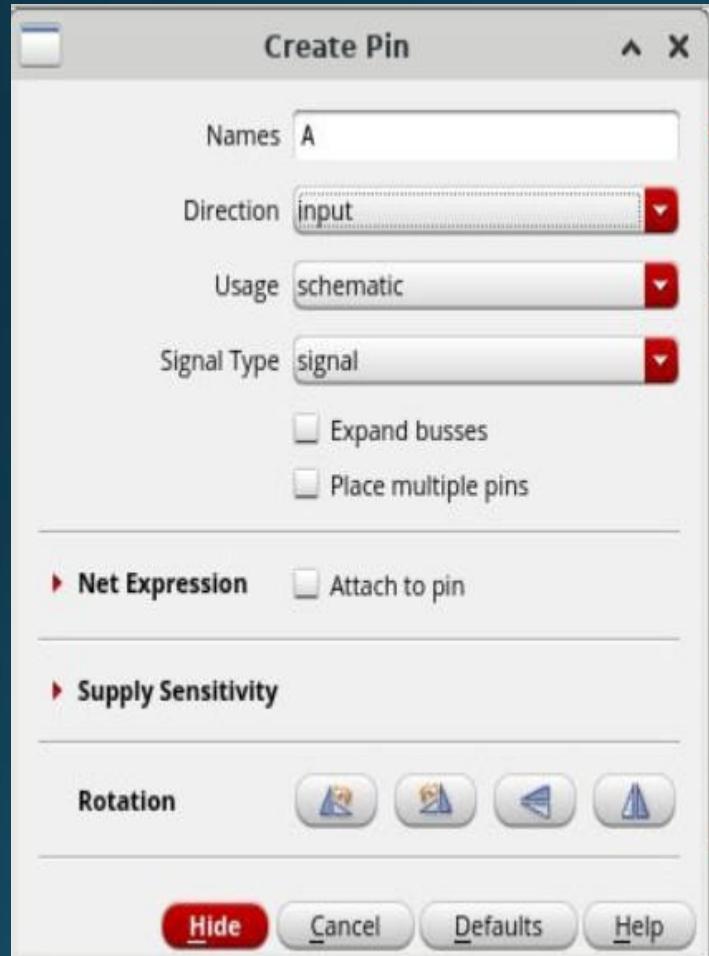


Ne folosim de tranzistoarele PMOS si NMOS din libraria tehnologica cu dimensiunile L si W exact ca in imagini (Create Instance)

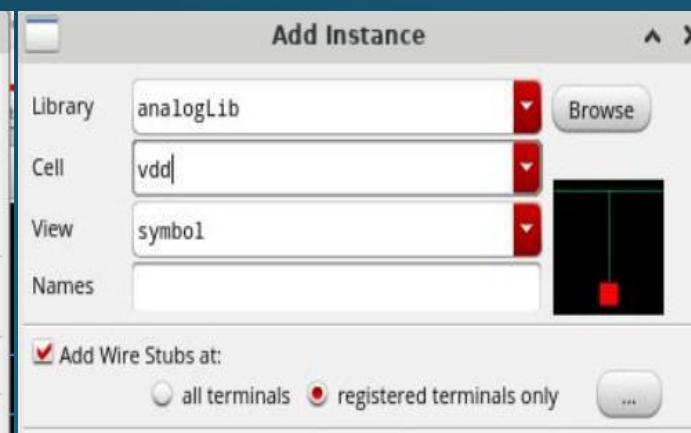
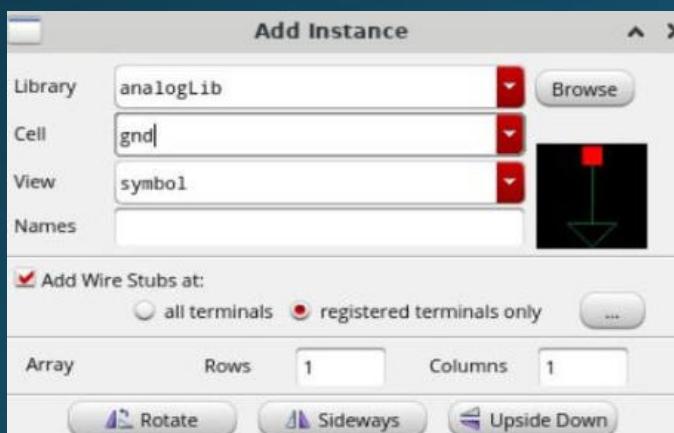
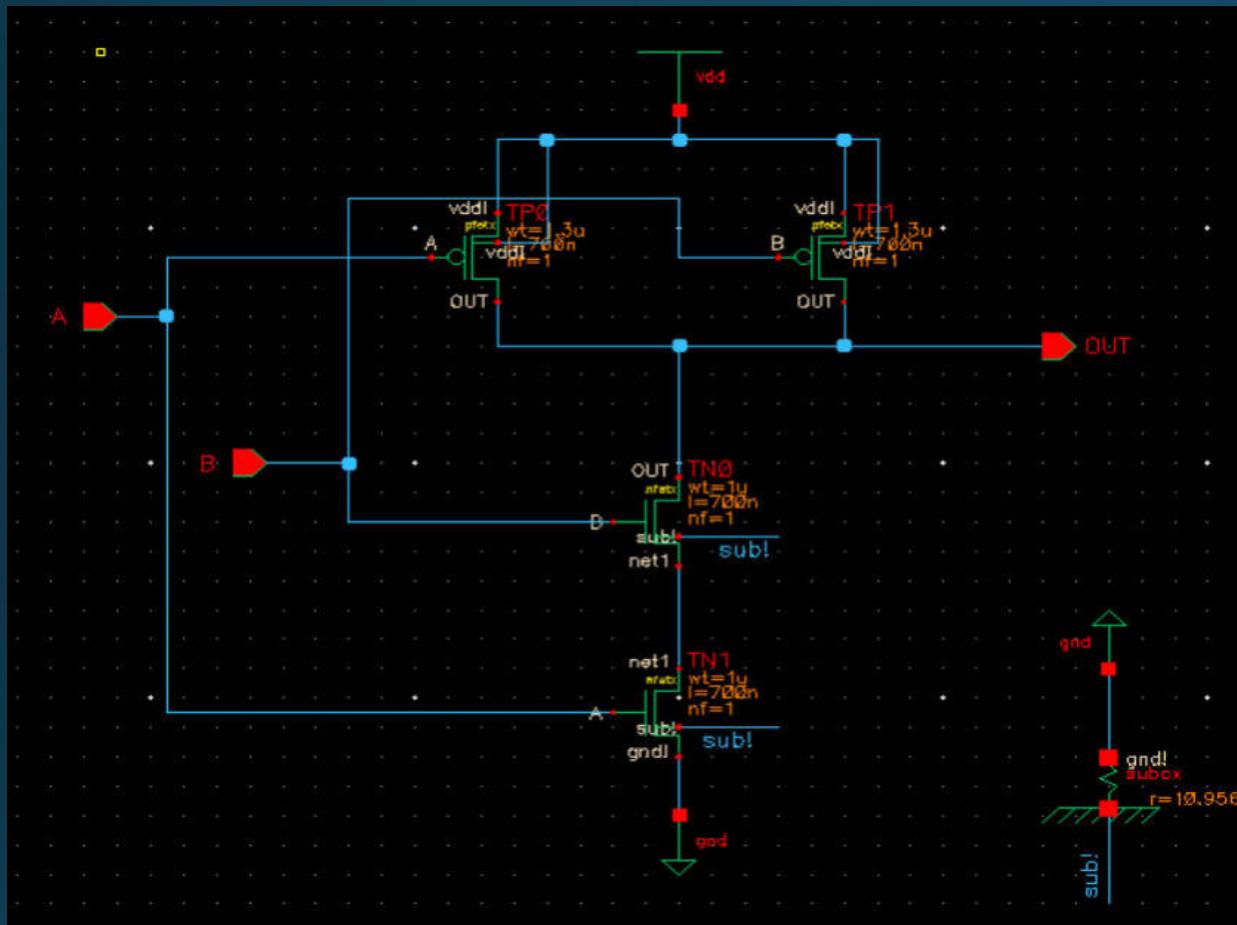


Crearea pinilor de iesire si de intrare

Create -> Pin

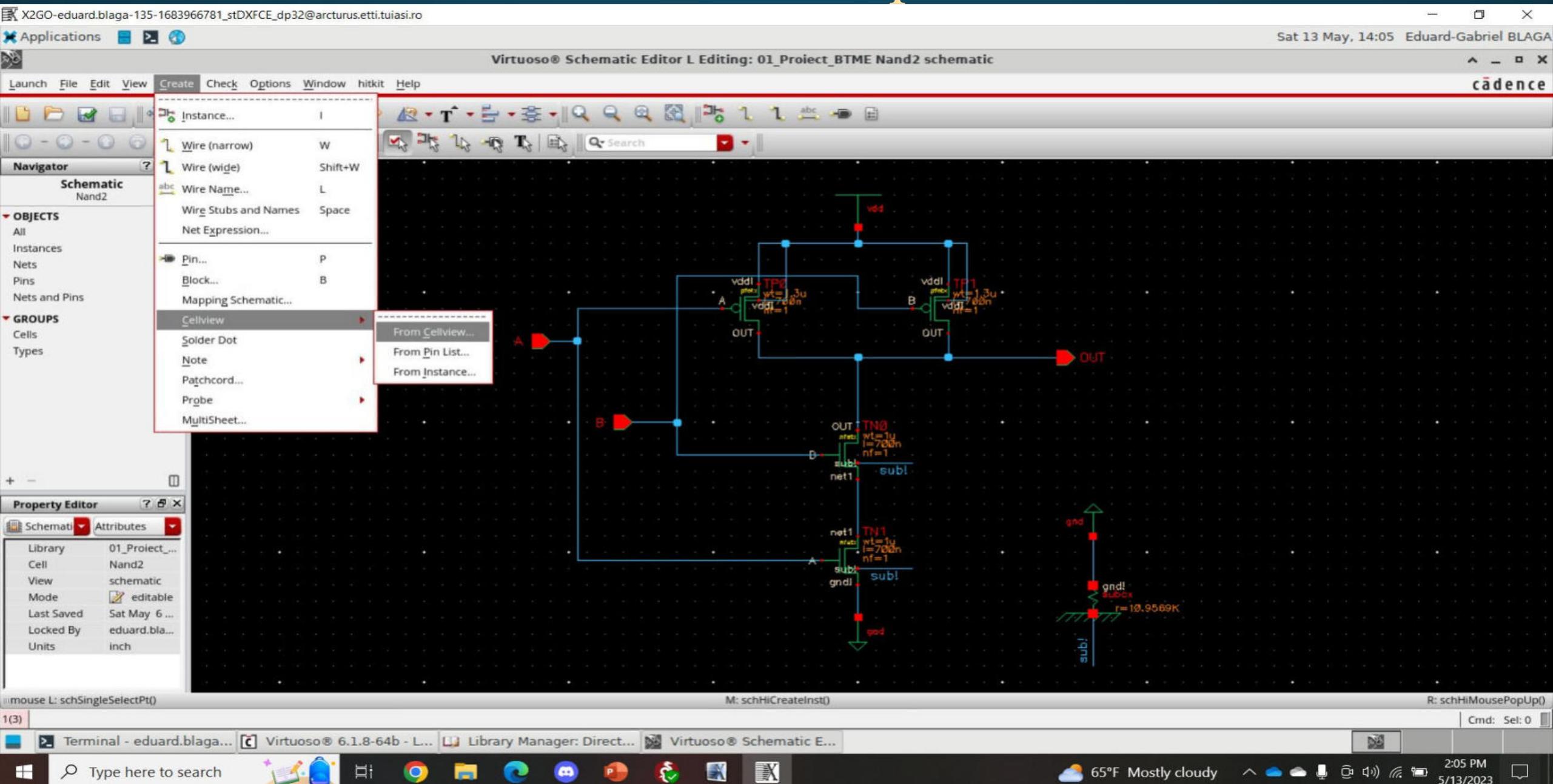


Intocmim schematicul



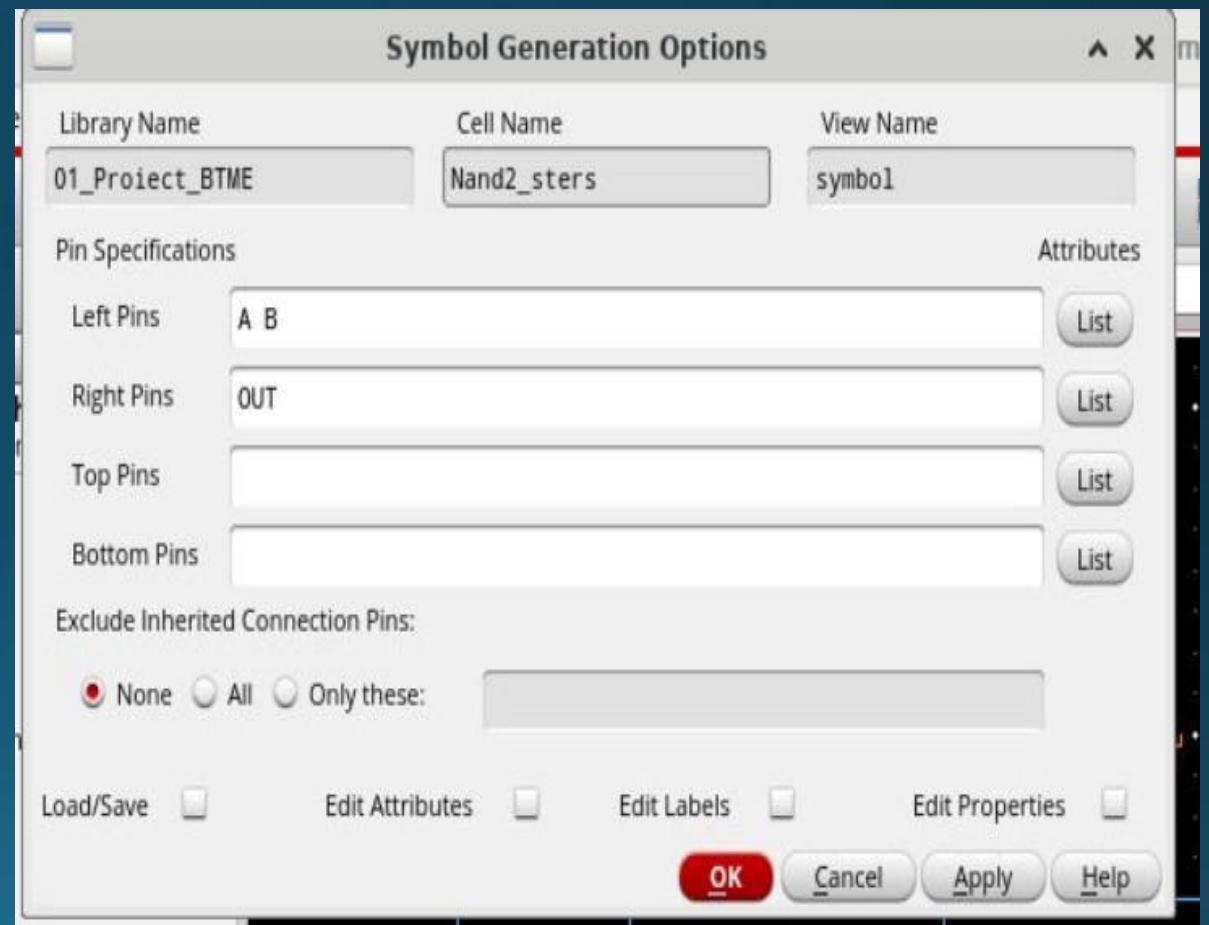
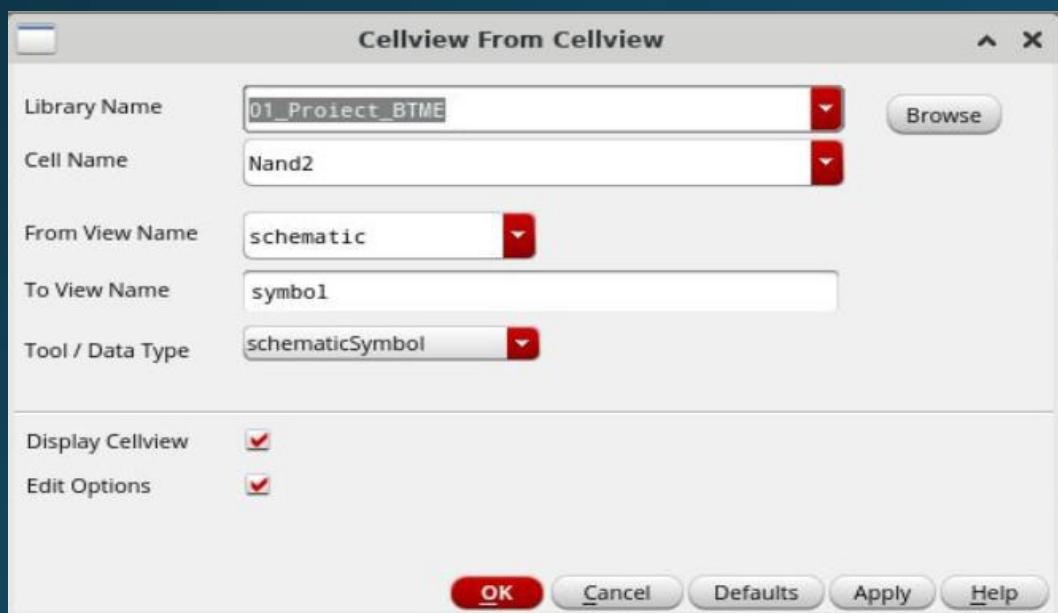
- Ne vom folosi de libraria analogLib pentru ground si sursa VDD.
- Pentru denumirea firului de la componenta subcx vom folosi comanda Create -> Wire name; dupa care vom copia firul (tasta C) si il vom plasa la fiecare substrat a tranzistoarelor NMOS ca in figura

Crearea simbolului portii nand

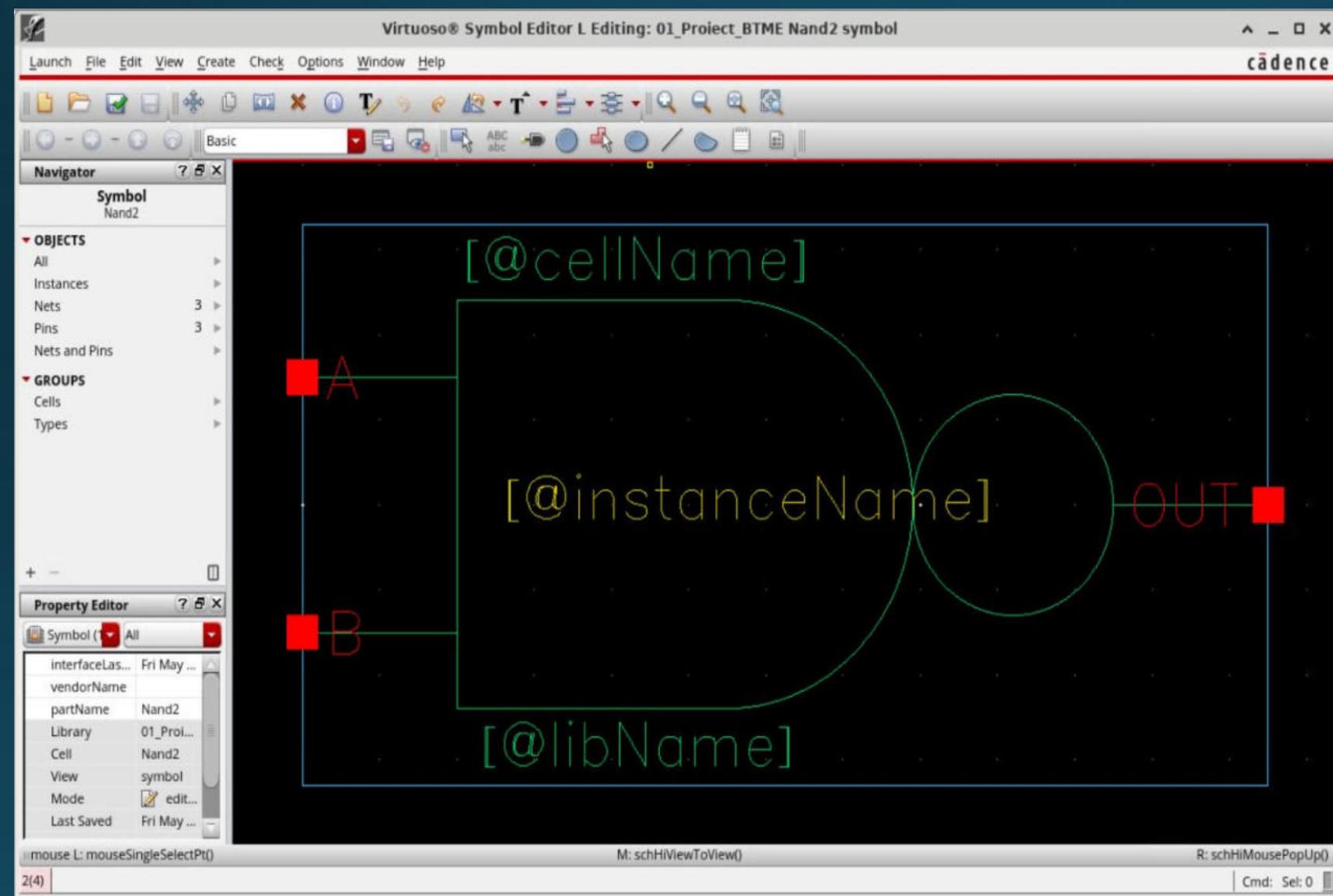


Crearea simbolului portii nand

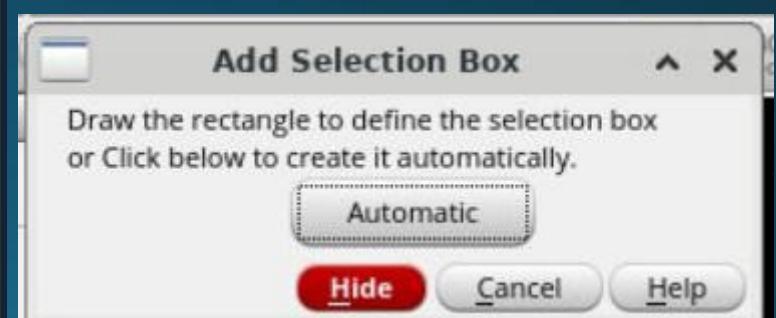
- Deoarece aveam creat deja un symbol pentru NAND2, am fost nevoie sa creez o replica a cell view-ului cu denumirea **Nand2_sters** pentru a putea arata ordinea de aranjare a pinilor



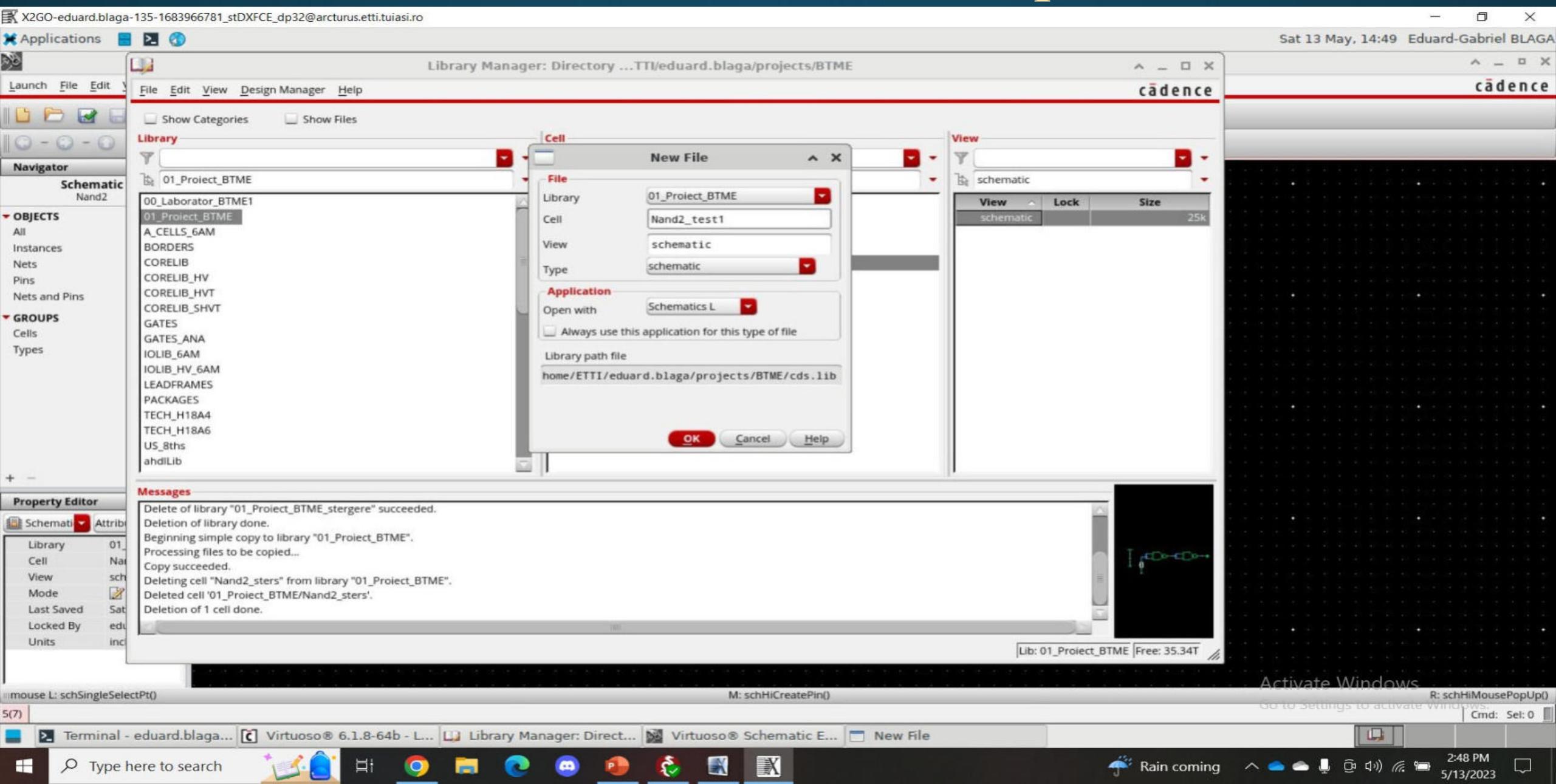
Realizam sibolul cu ajutorul comenzii Create -> Shape



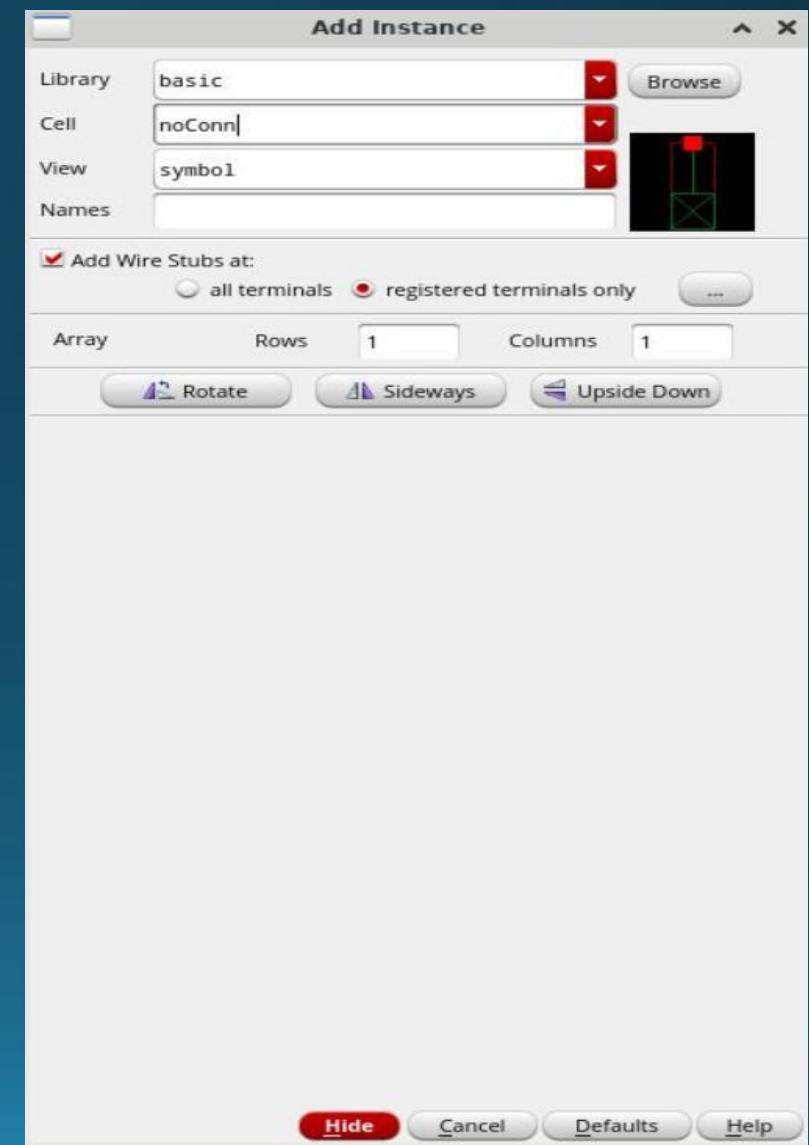
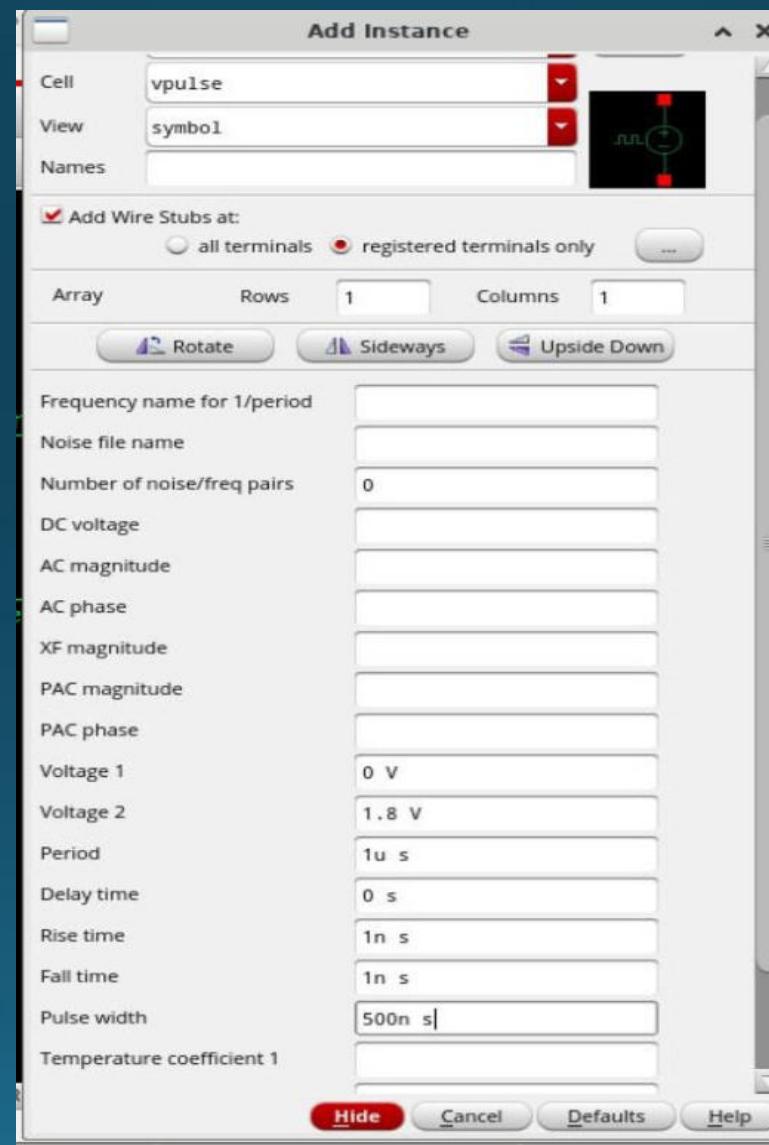
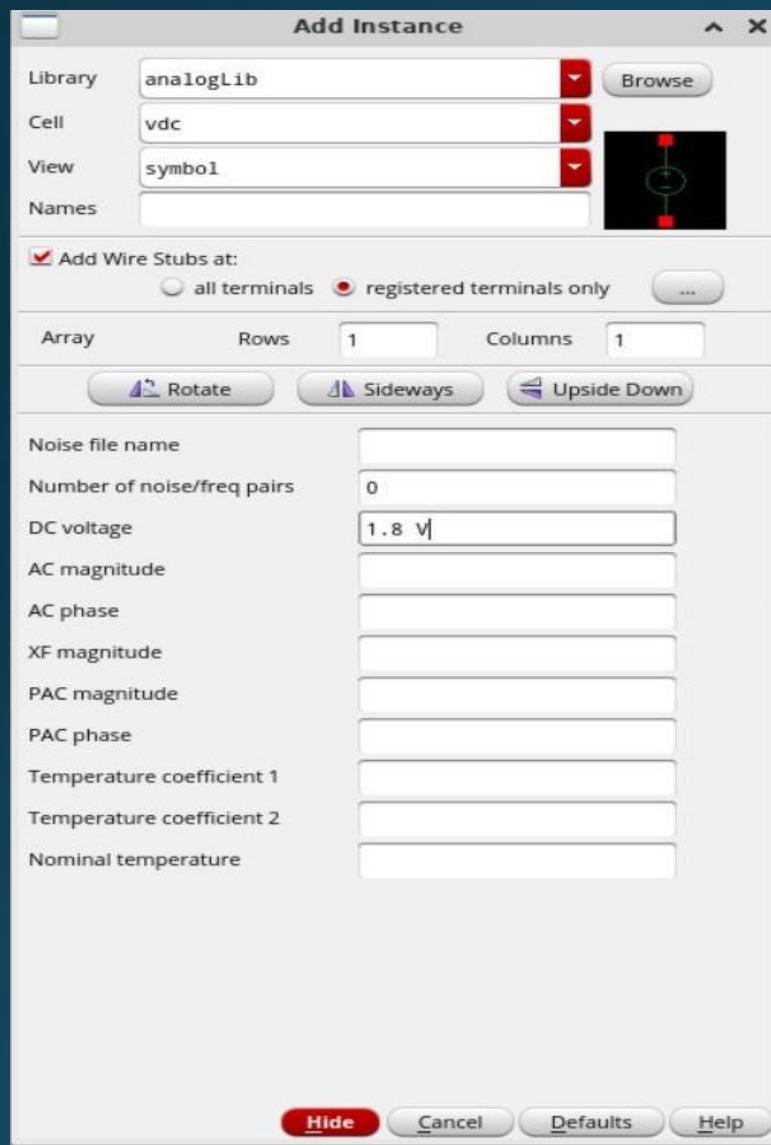
La final, urmam comanda Create -> Selection Box si apasam pe butonul Automatic



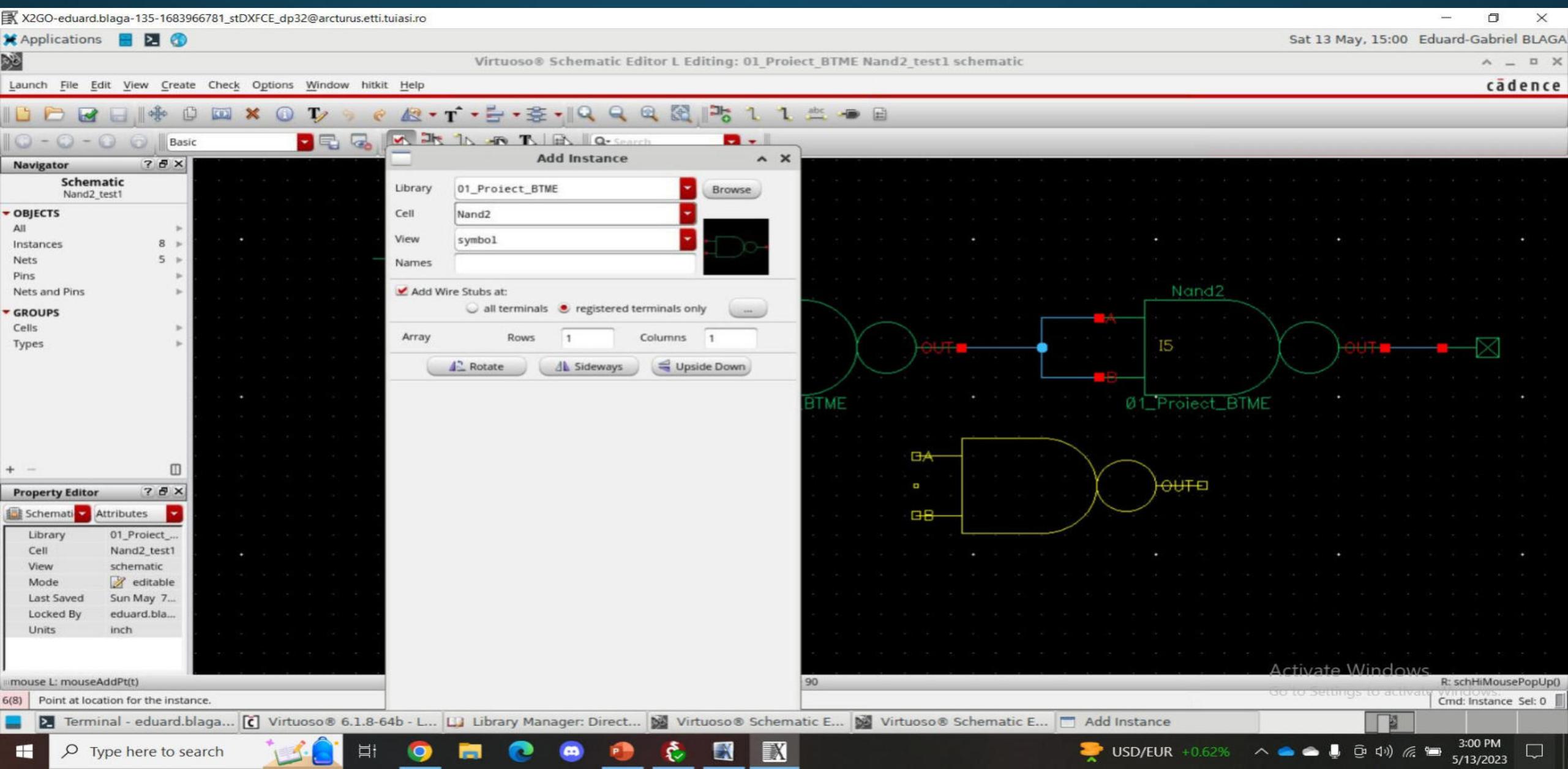
Se realizeaza un cell view de test pentru NAND



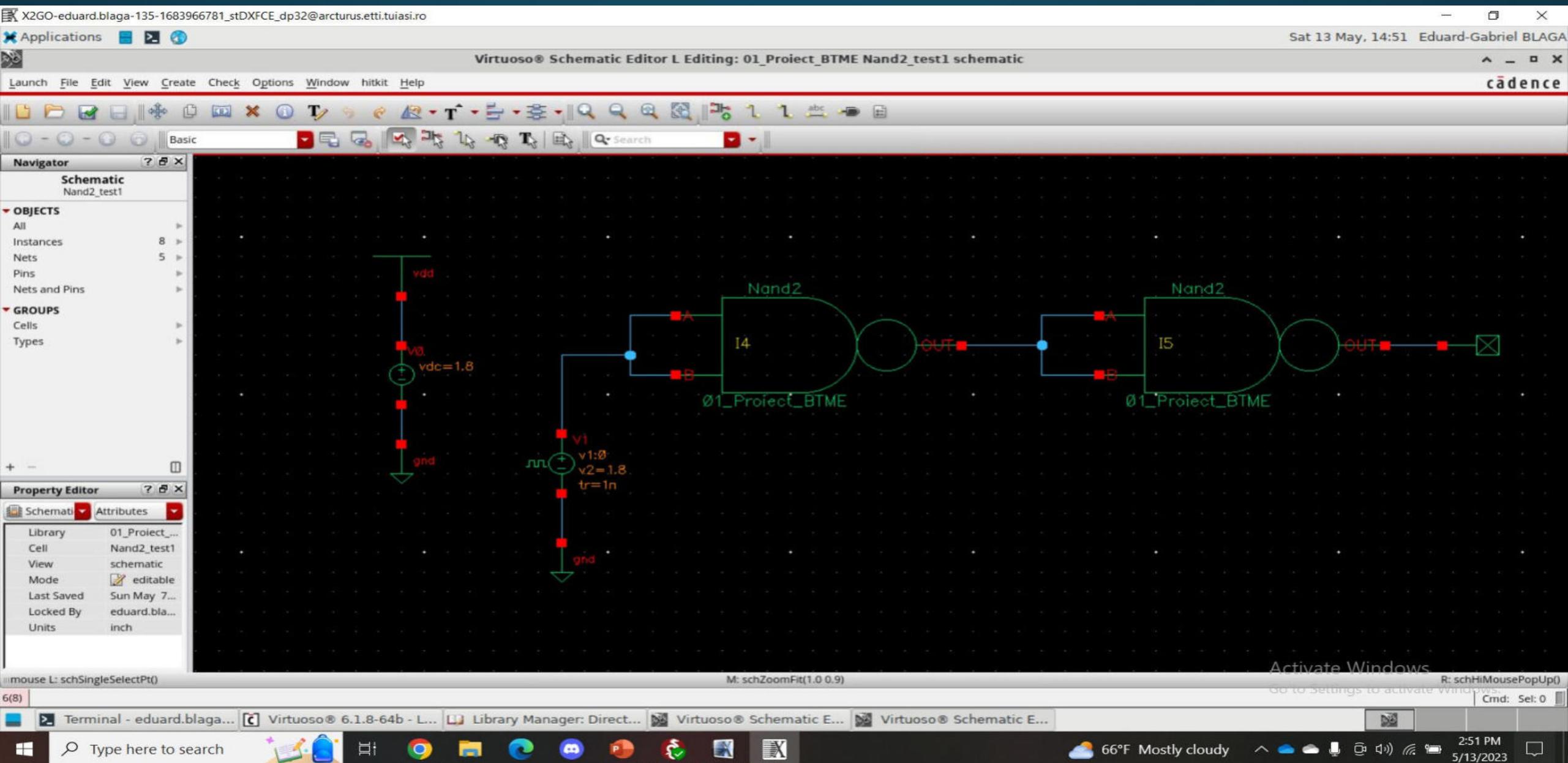
Extragem sursele Vdc si Vpulse din libraria analogLib cu urmatorii parametri si noConnect din libraria basic



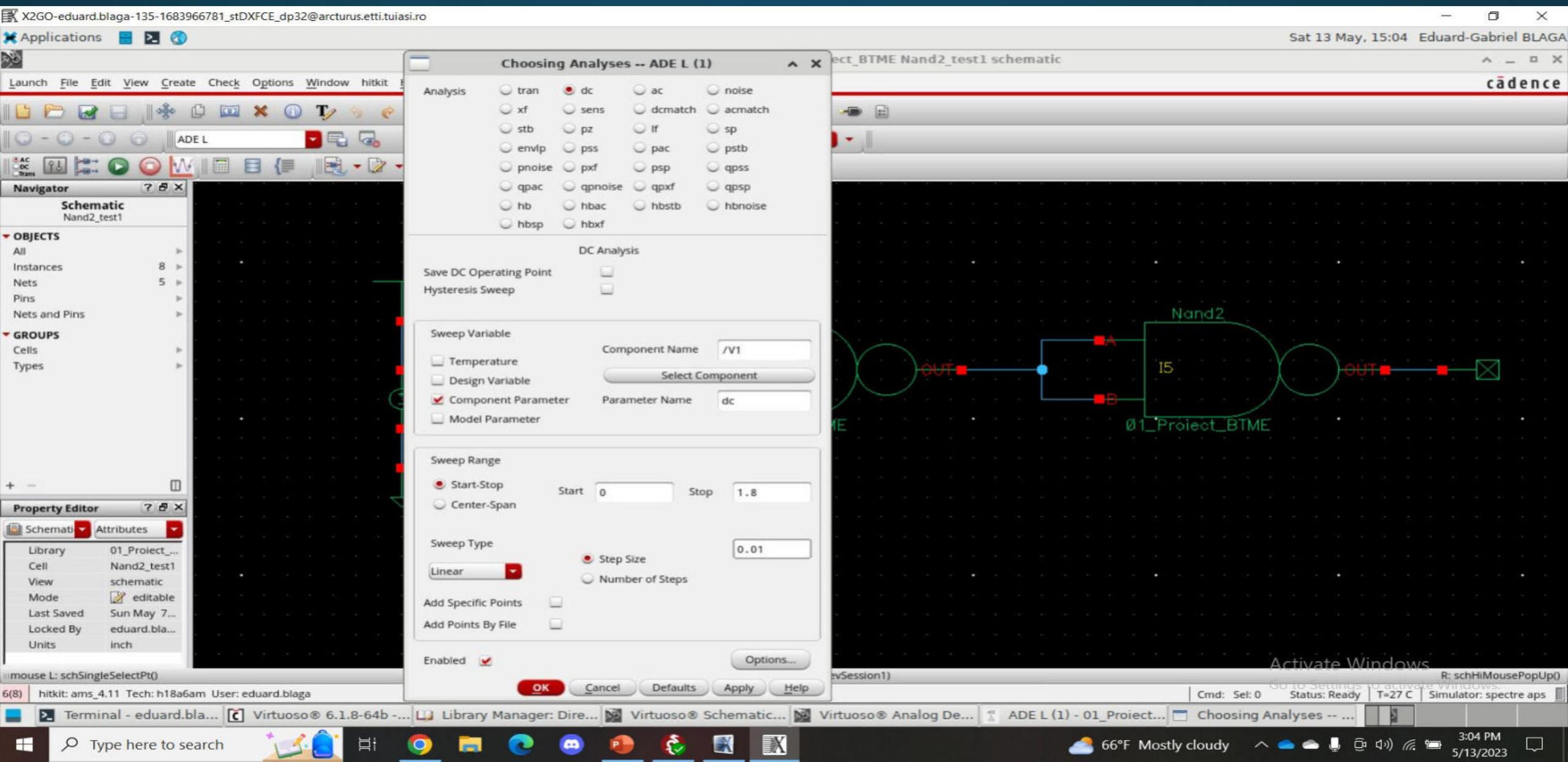
Se instantiaza NAND-ul creat cu view de tip simbol



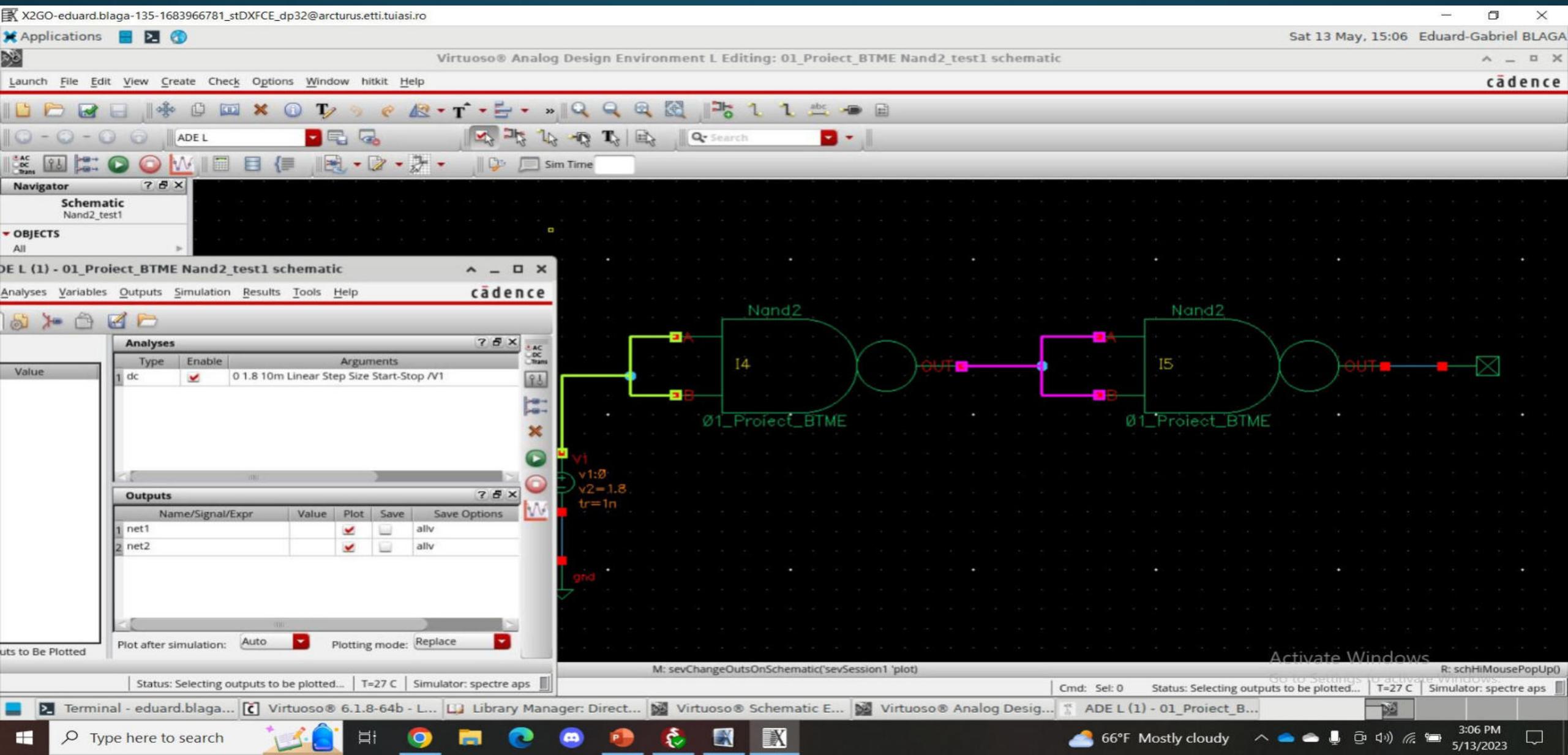
Se realizeaza schema de test



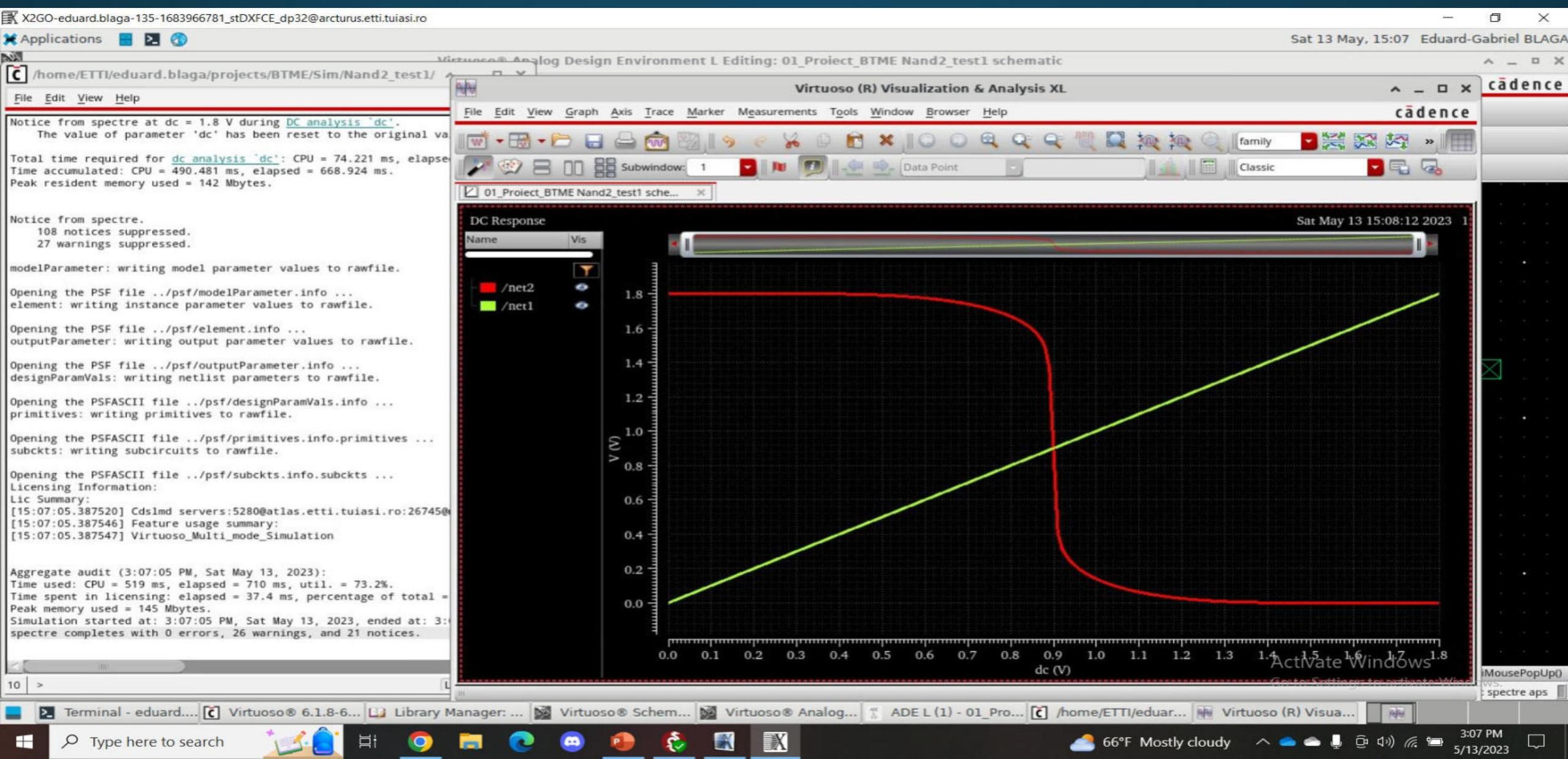
Se lanseaza ADE-L si se seteaza analiza DC



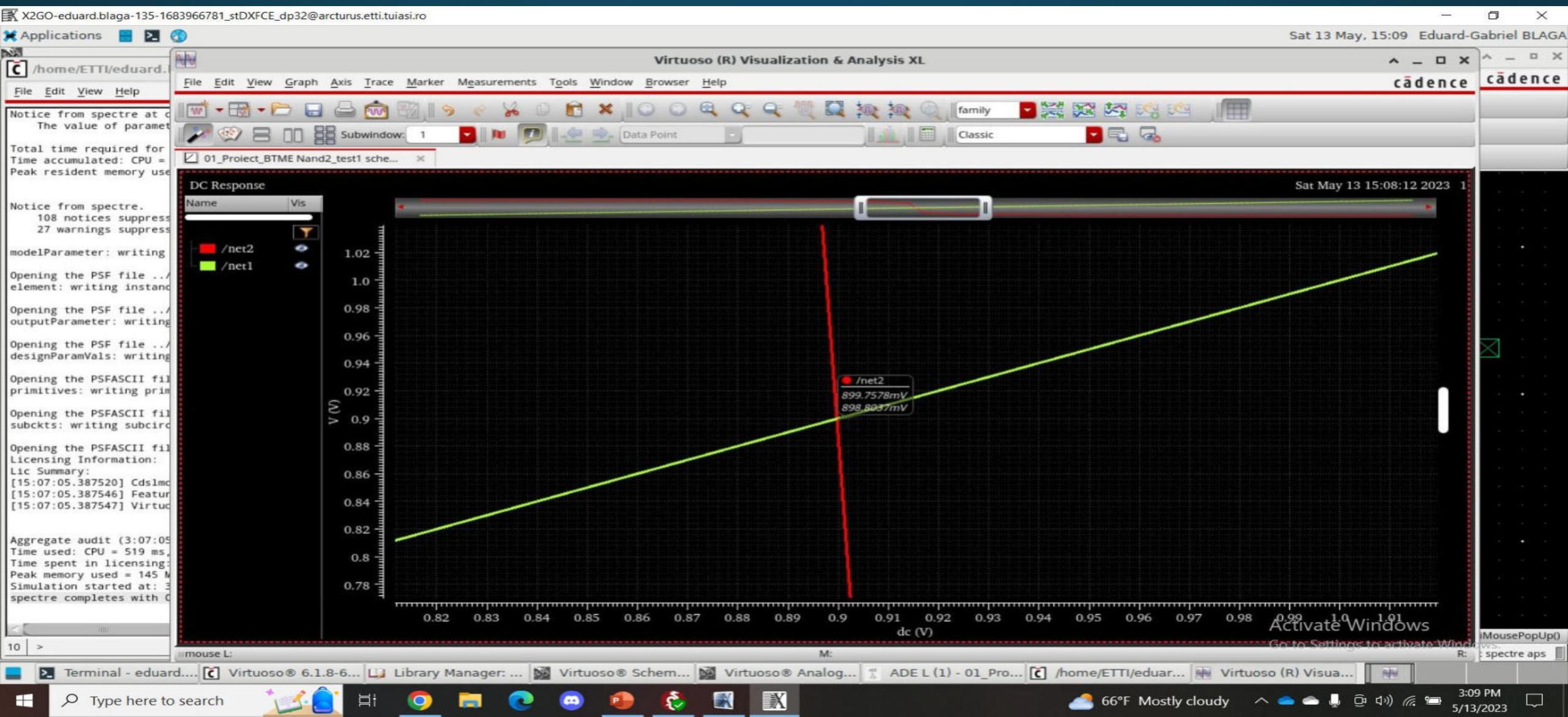
Selectie plot intrarea si iesirea primului NAND



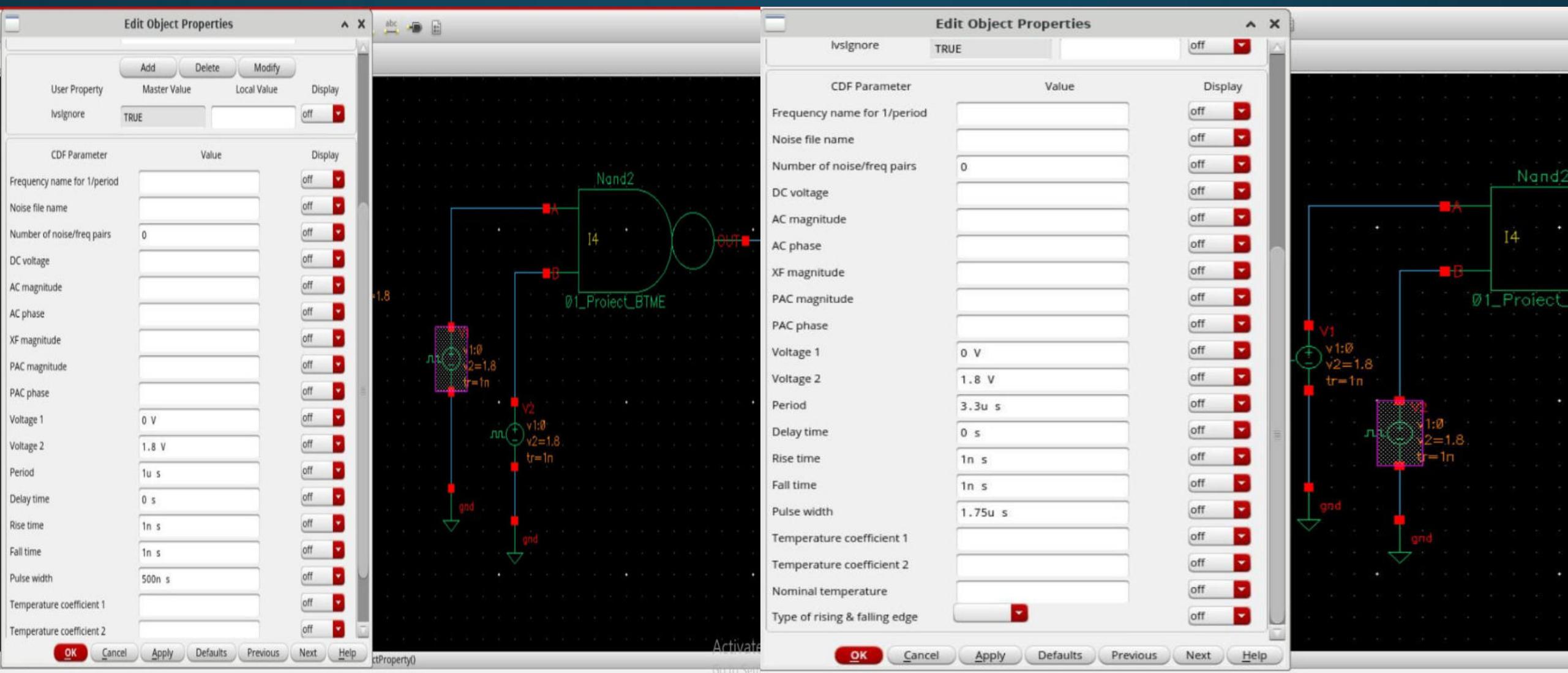
Realizarea simularii si plotarea caracteristicii de transfer



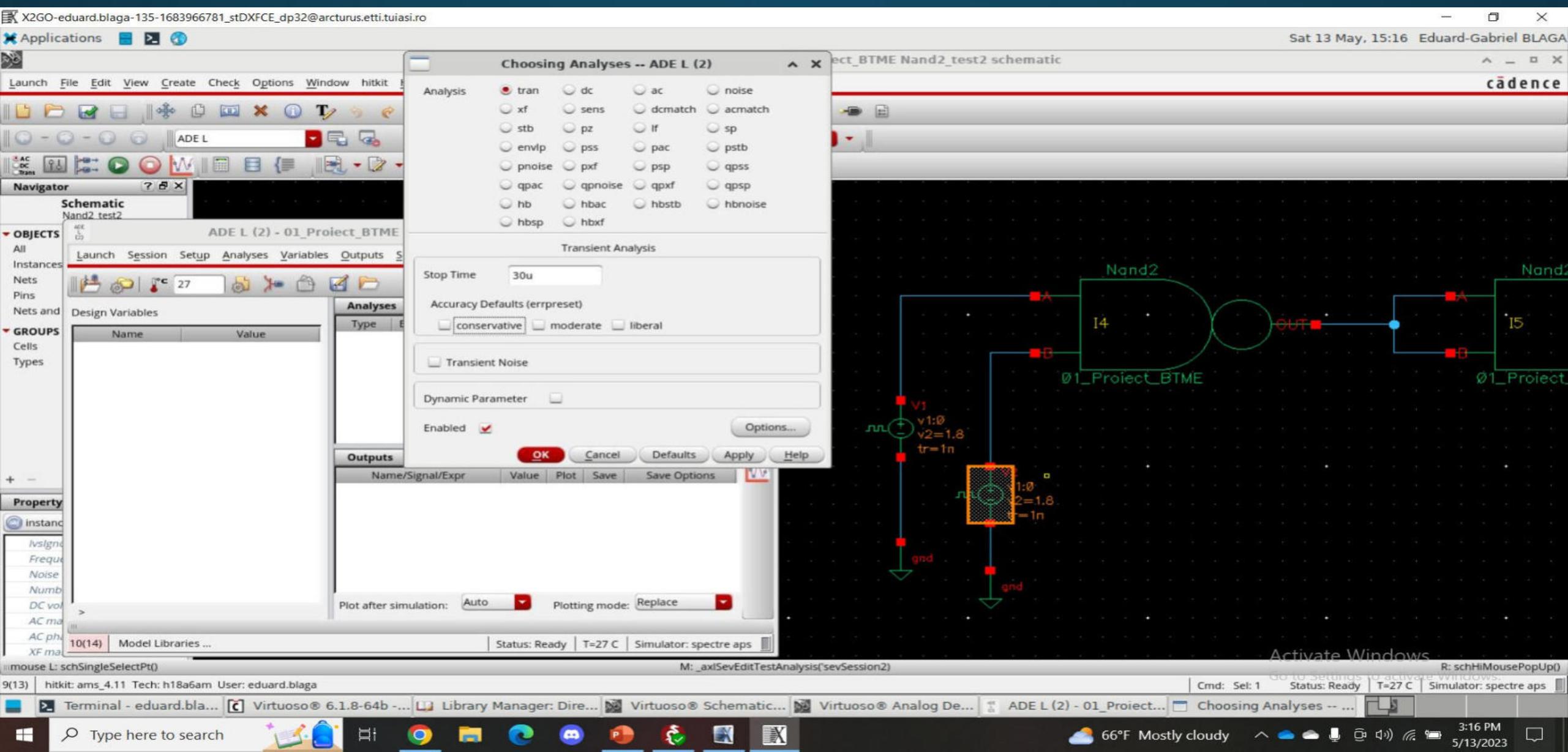
Zoom caracteristica de transfer si identificarea punctului de comutare care ar trebui sa fie la vdd/2 (900mV)



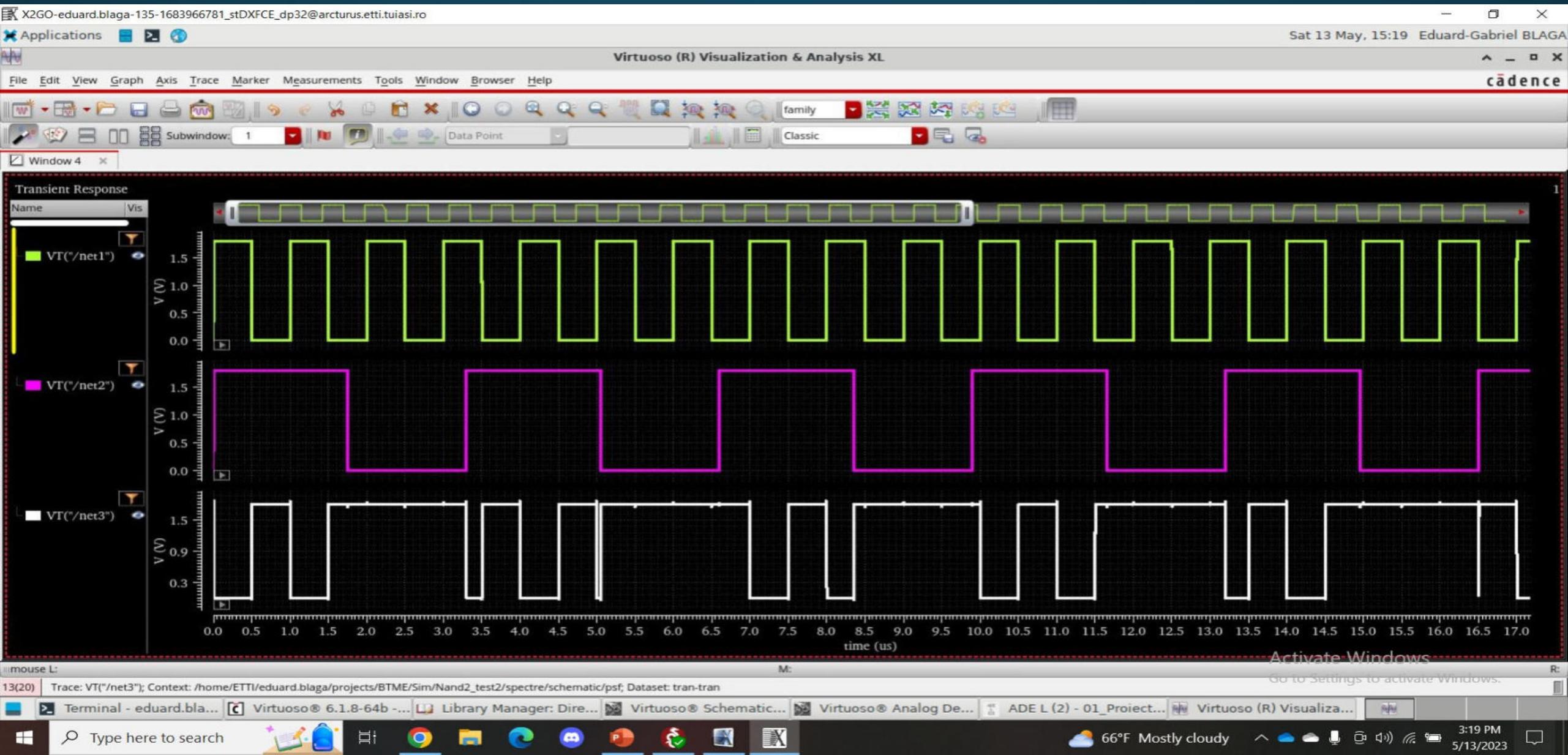
Pentru analiza tranzitorie se aplica pe intrari doua surse vpulse cu frecvențe diferite



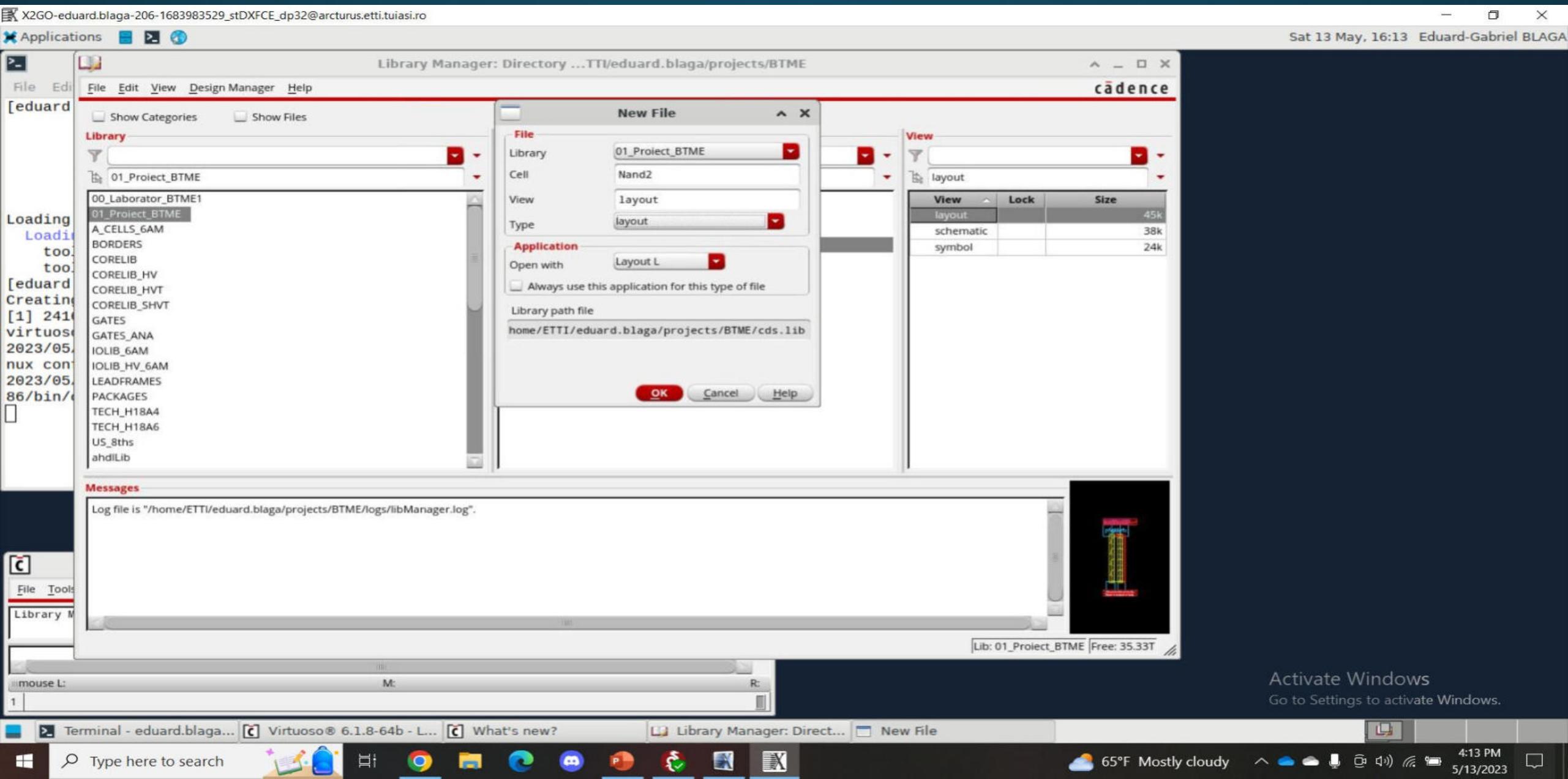
Se realizeaza o analiza tranzitorie



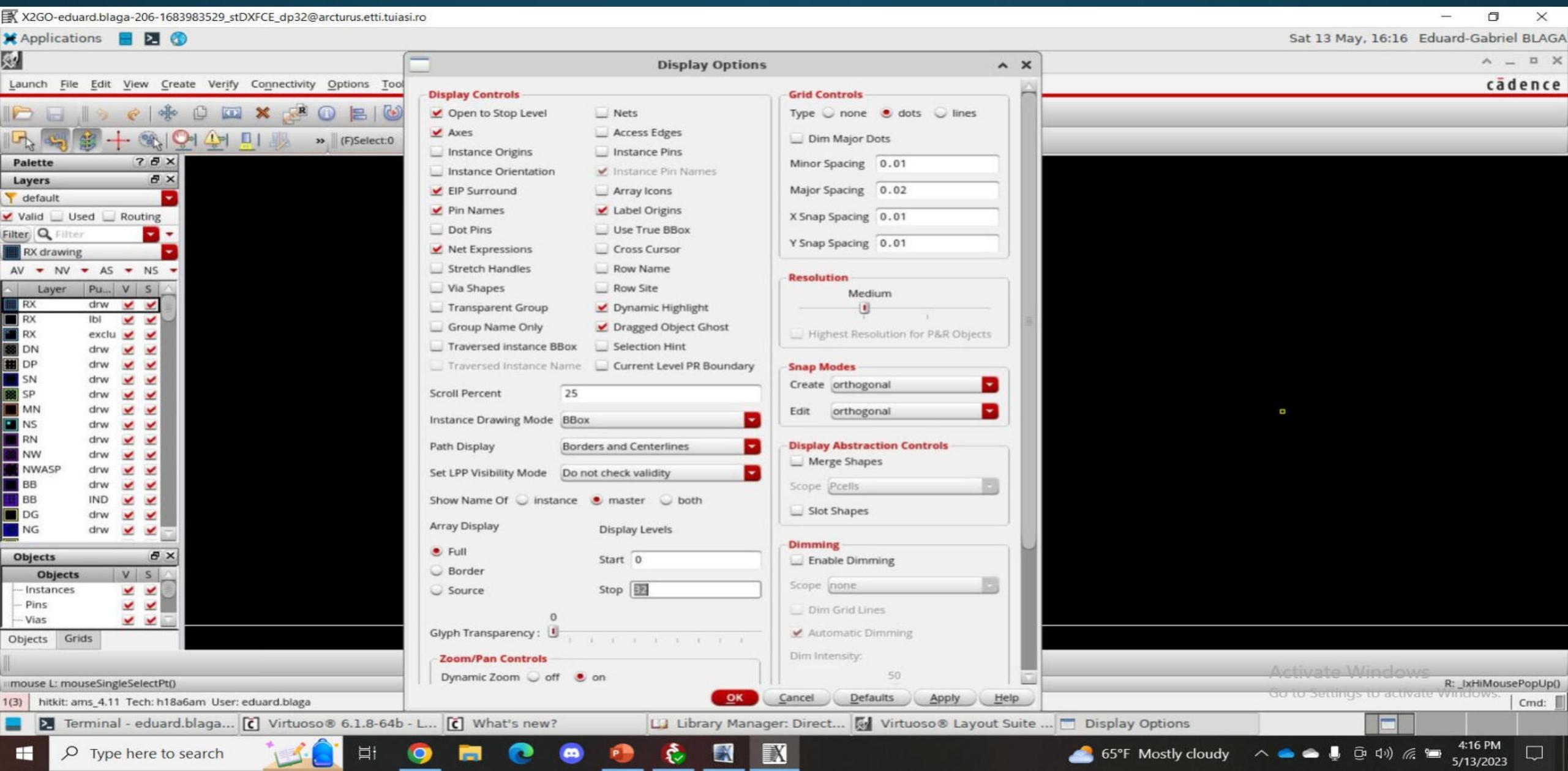
Se reface simularea si se ploteaza forma de unda in timp



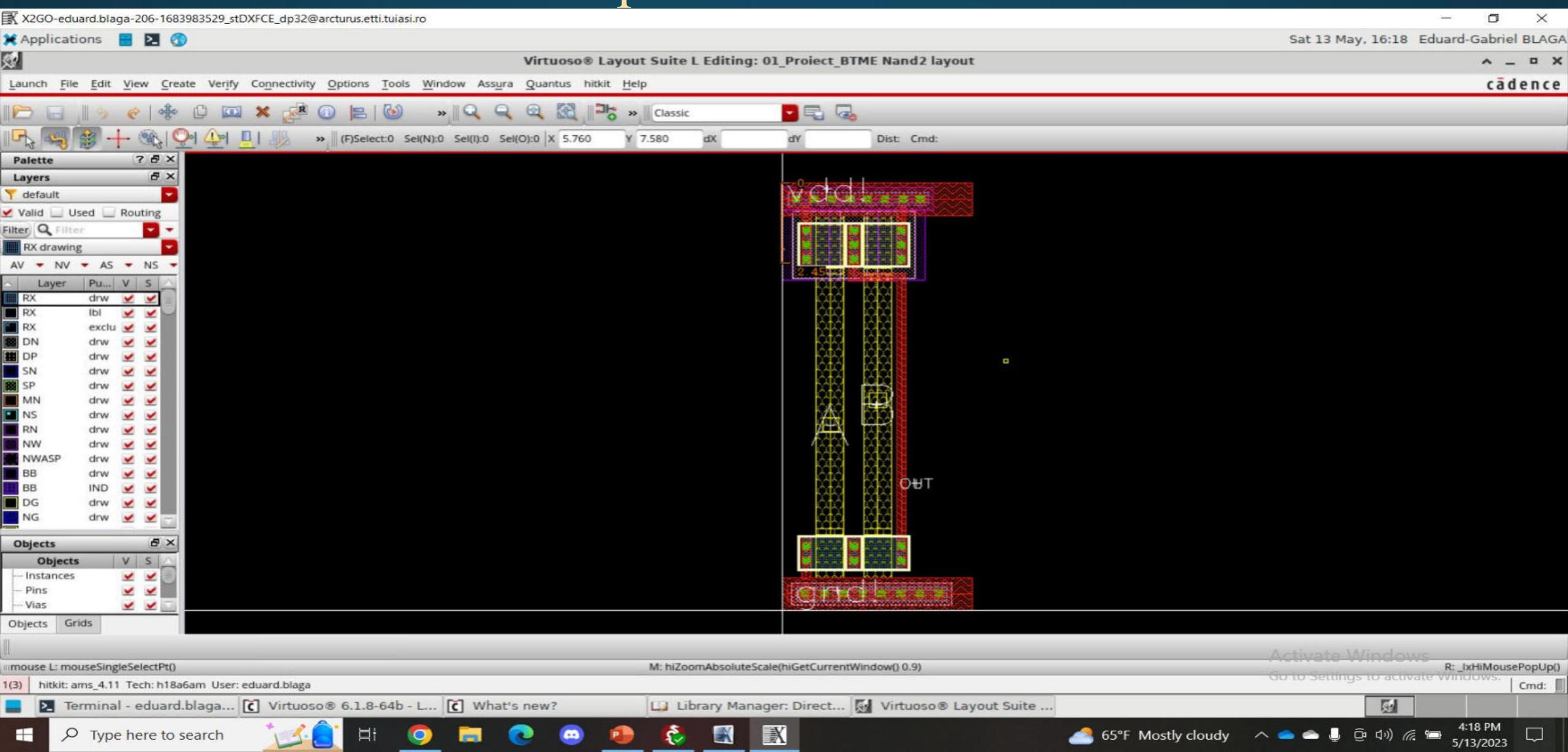
Se realizeaza un cell view de tip layout cu aceeasi denumire



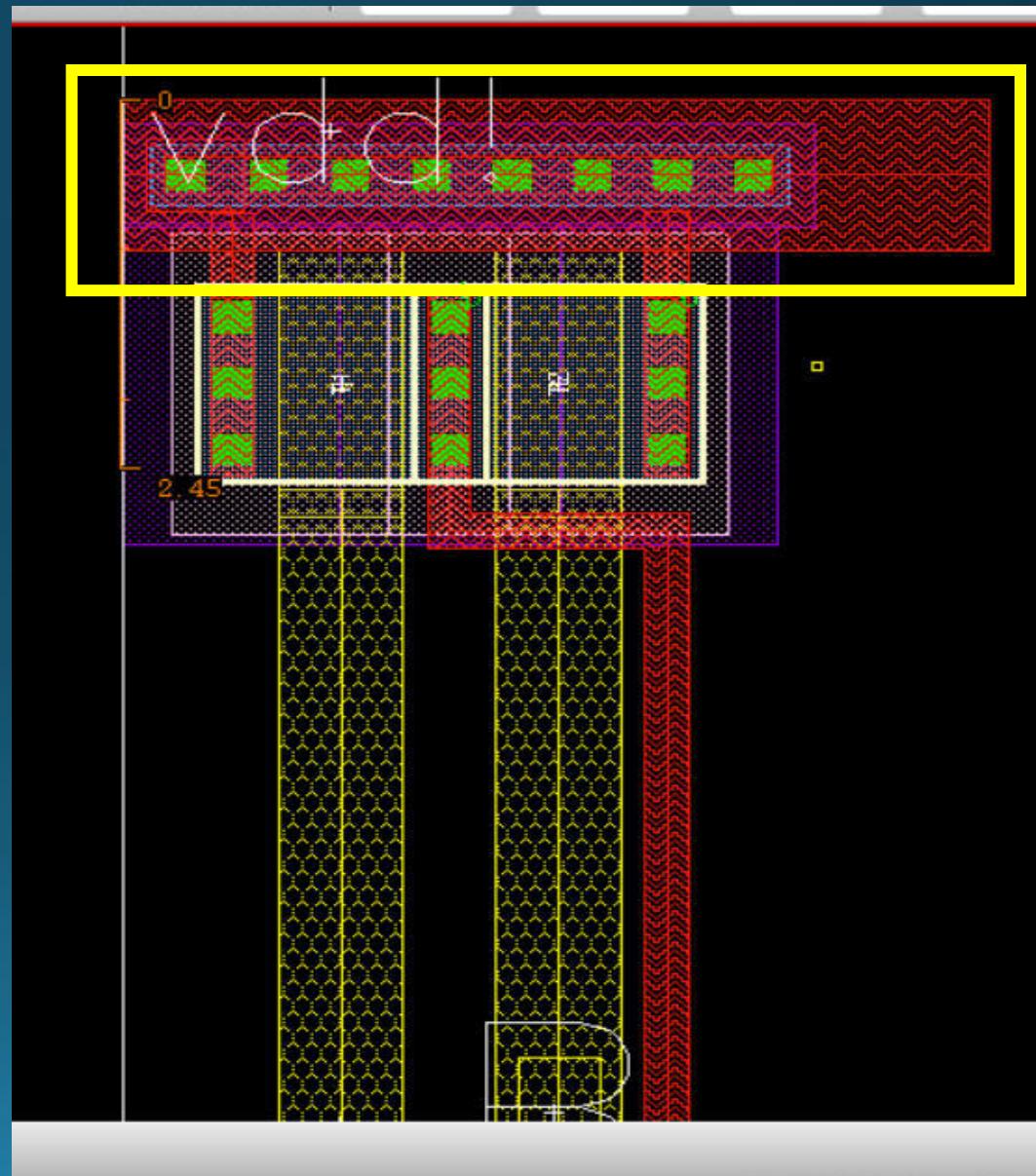
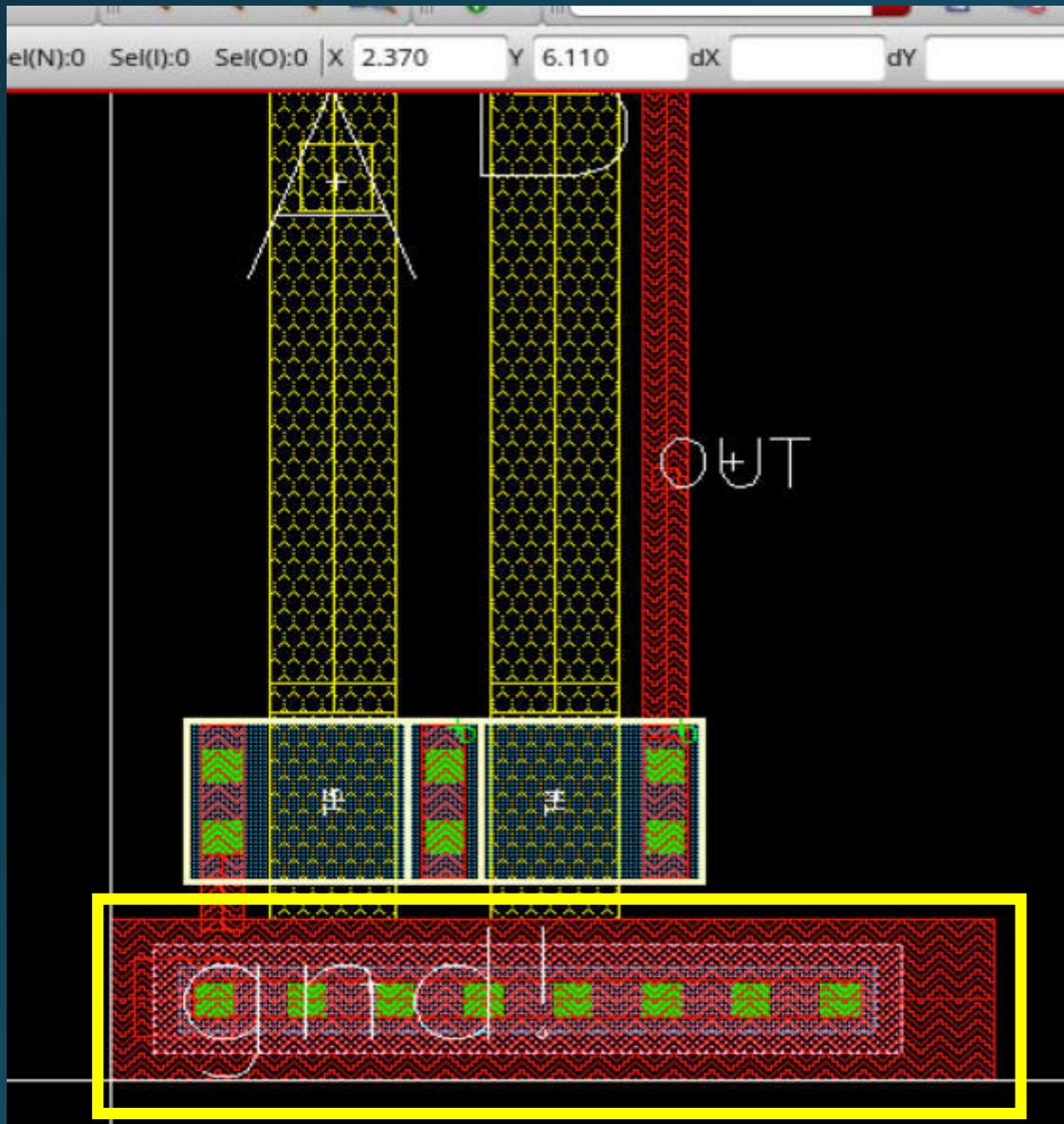
Configuram display-ul cu urmatoarele setari prin tasta E



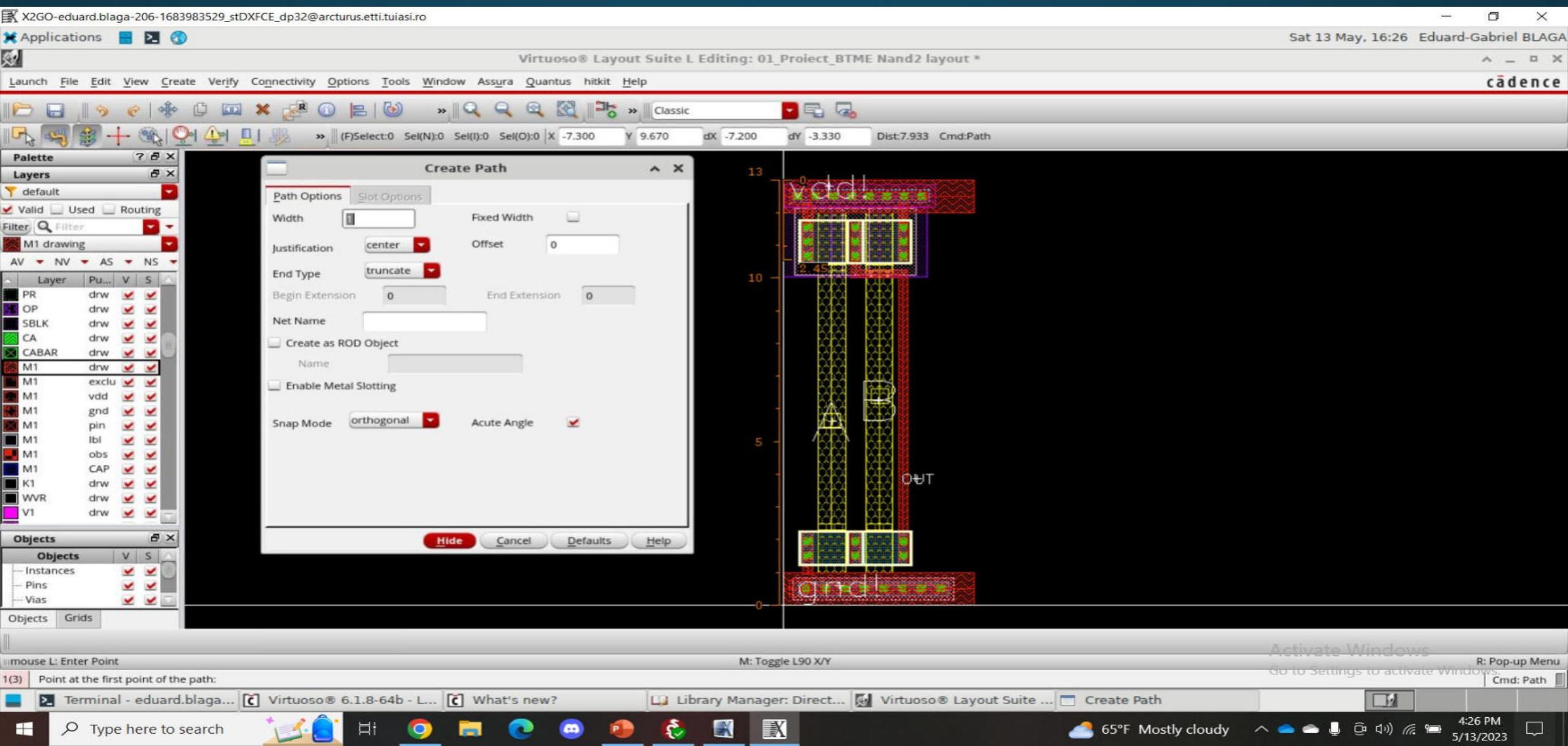
Avand deja layout-ul facut, voi explica direct pe schema pasii de urmat



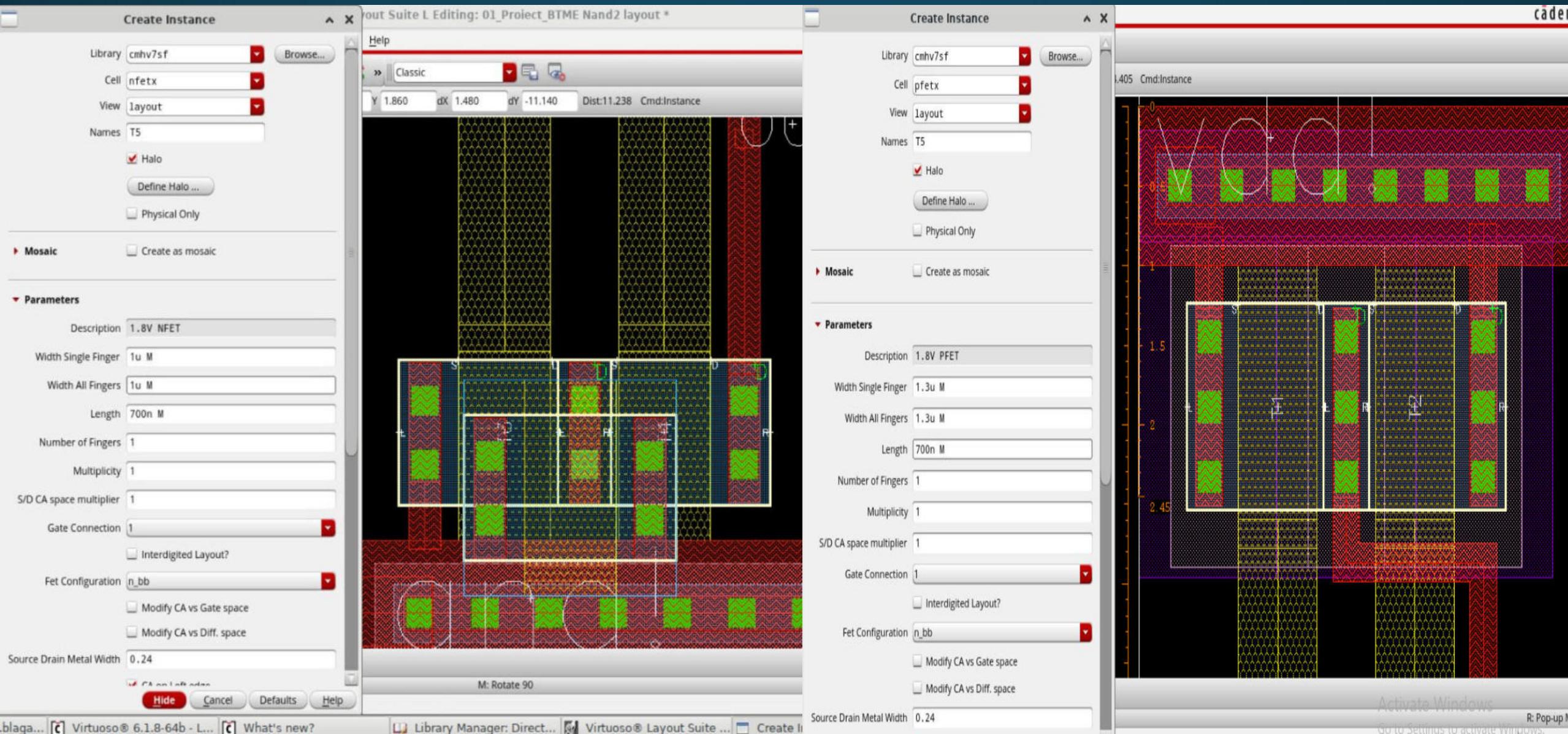
Se creeaza cu M1 un path cu dimensiune de 1u pentru alimentare si ground (prin comanda Create->Shape->Path)



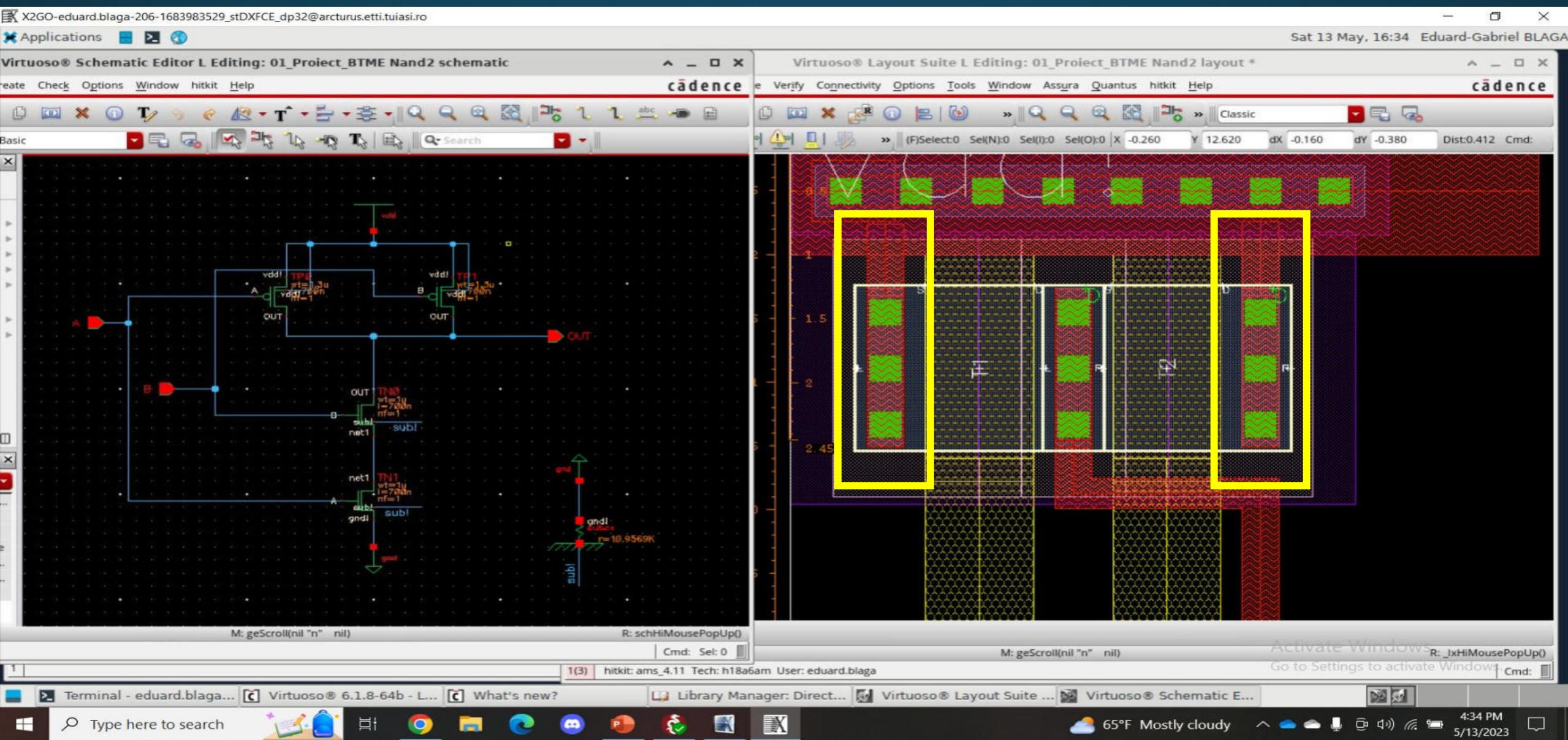
Cu tasta F3 se editeaza latimea path-ului



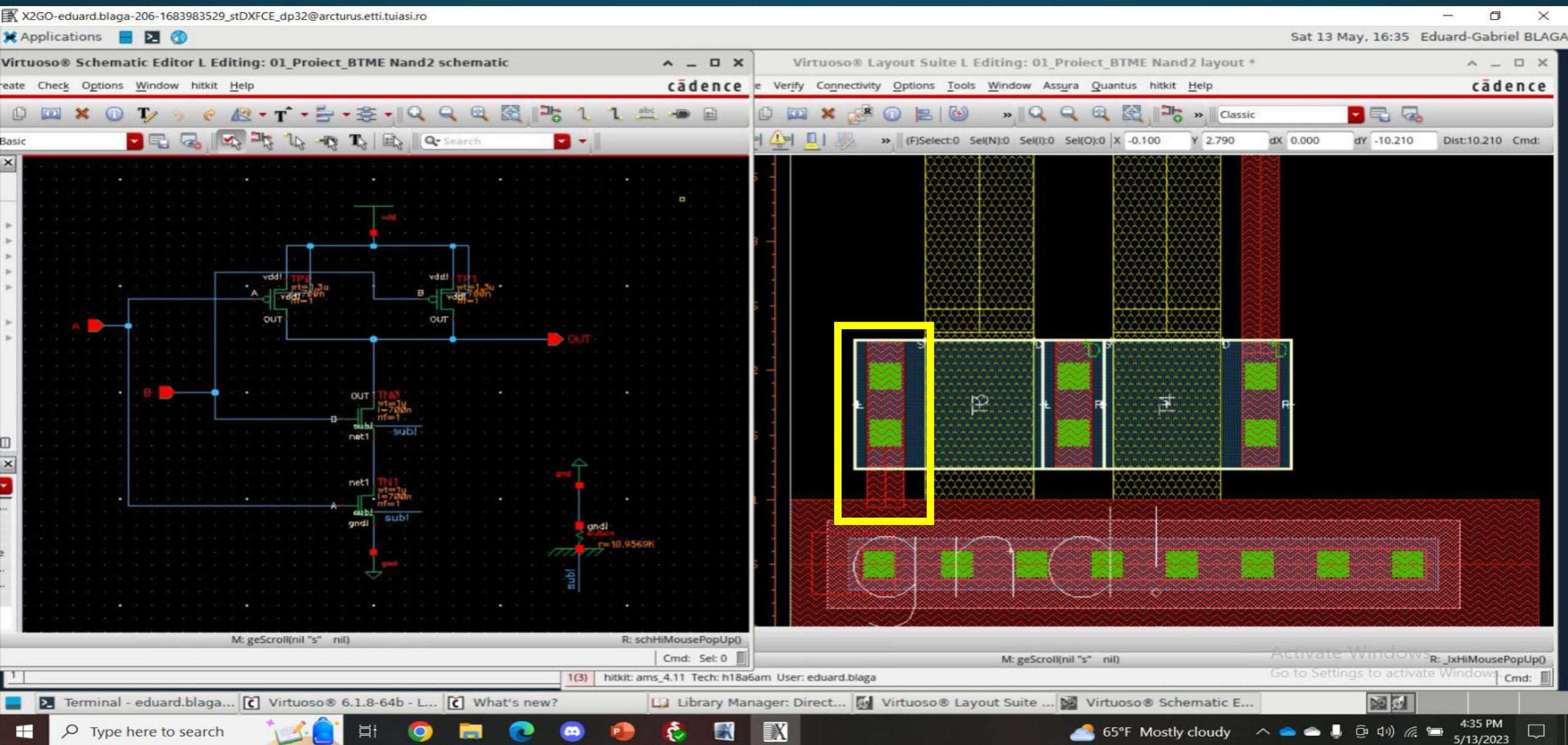
Se instantiaza 2 tranzistoare pfetx si nfetx cu aceleasi dimensiuni ca cele din schematic



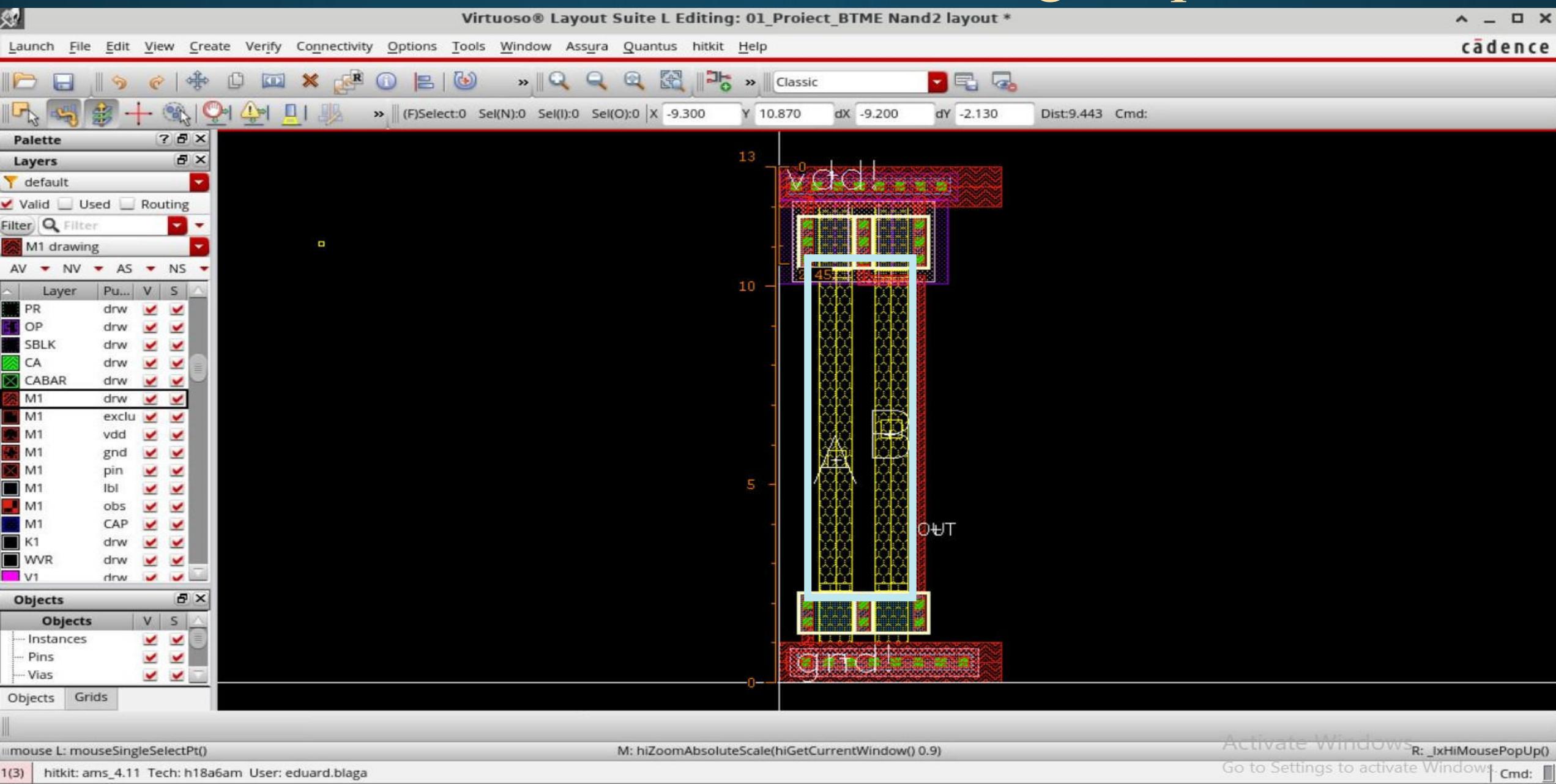
Se realizeaza conexiunile intre grile pe PC si conectarea surselor la vdd si gnd pe M1



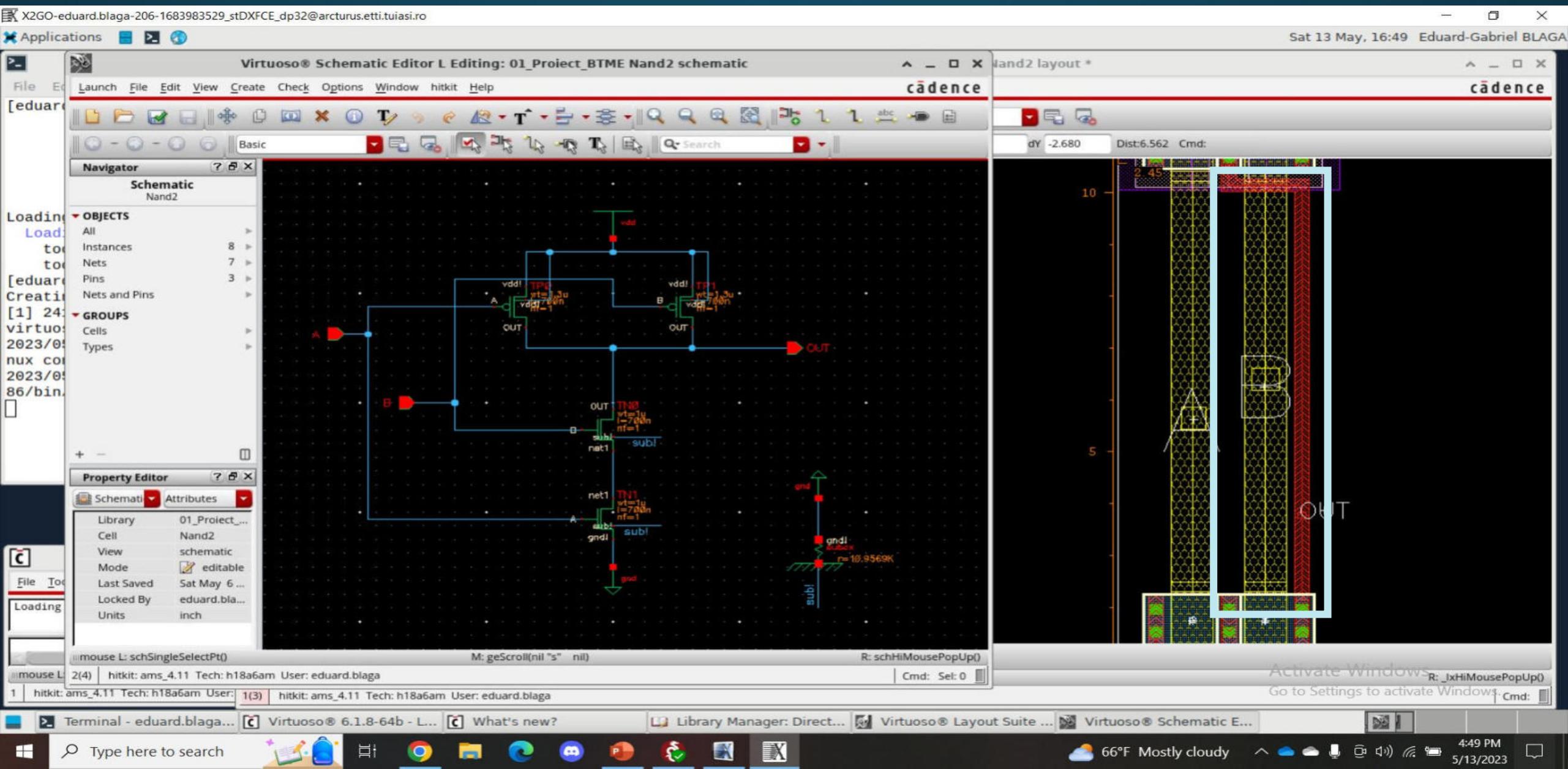
Se realizeaza conexiunile intre grile pe PC si conectarea surselor la vdd si gnd pe M1



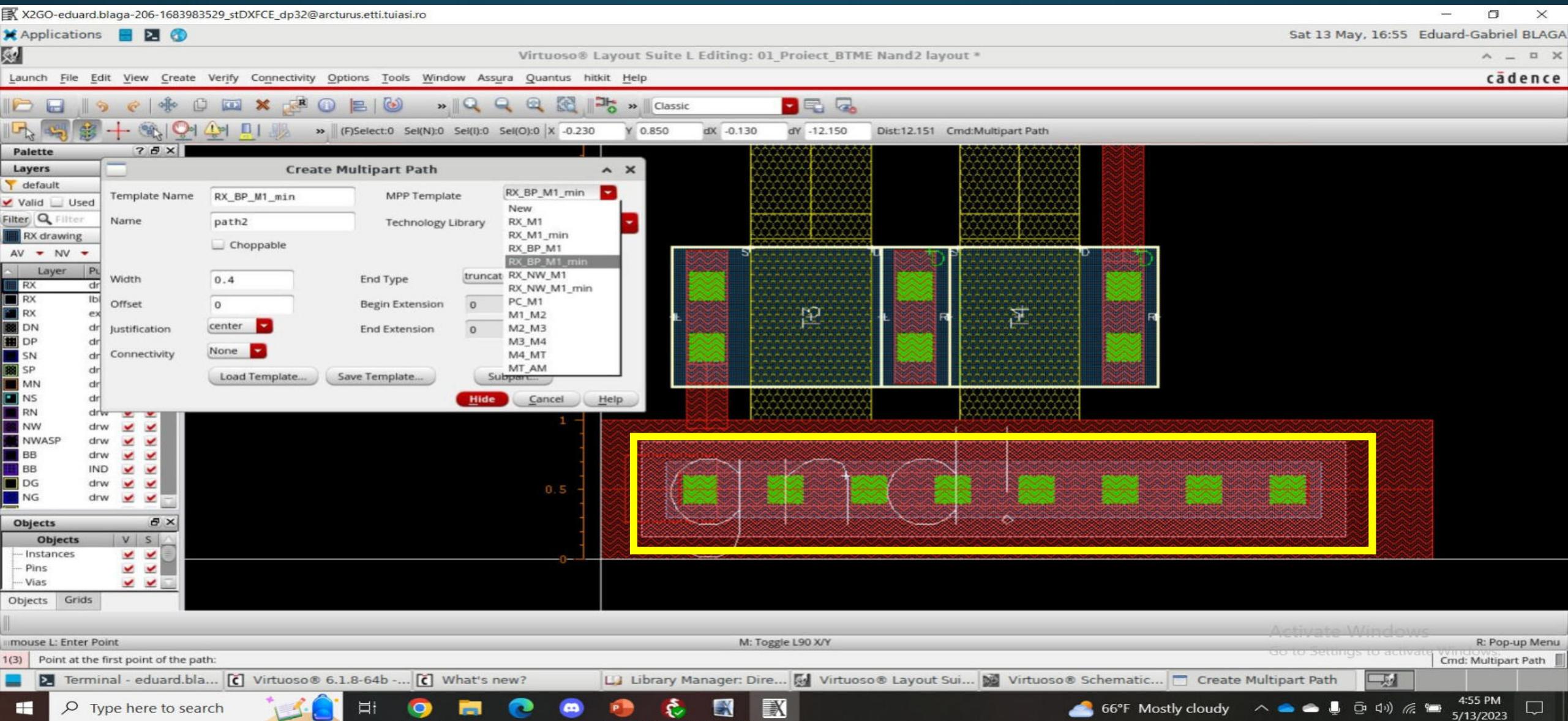
Se realizeaza conexiunile intre grile pe PC



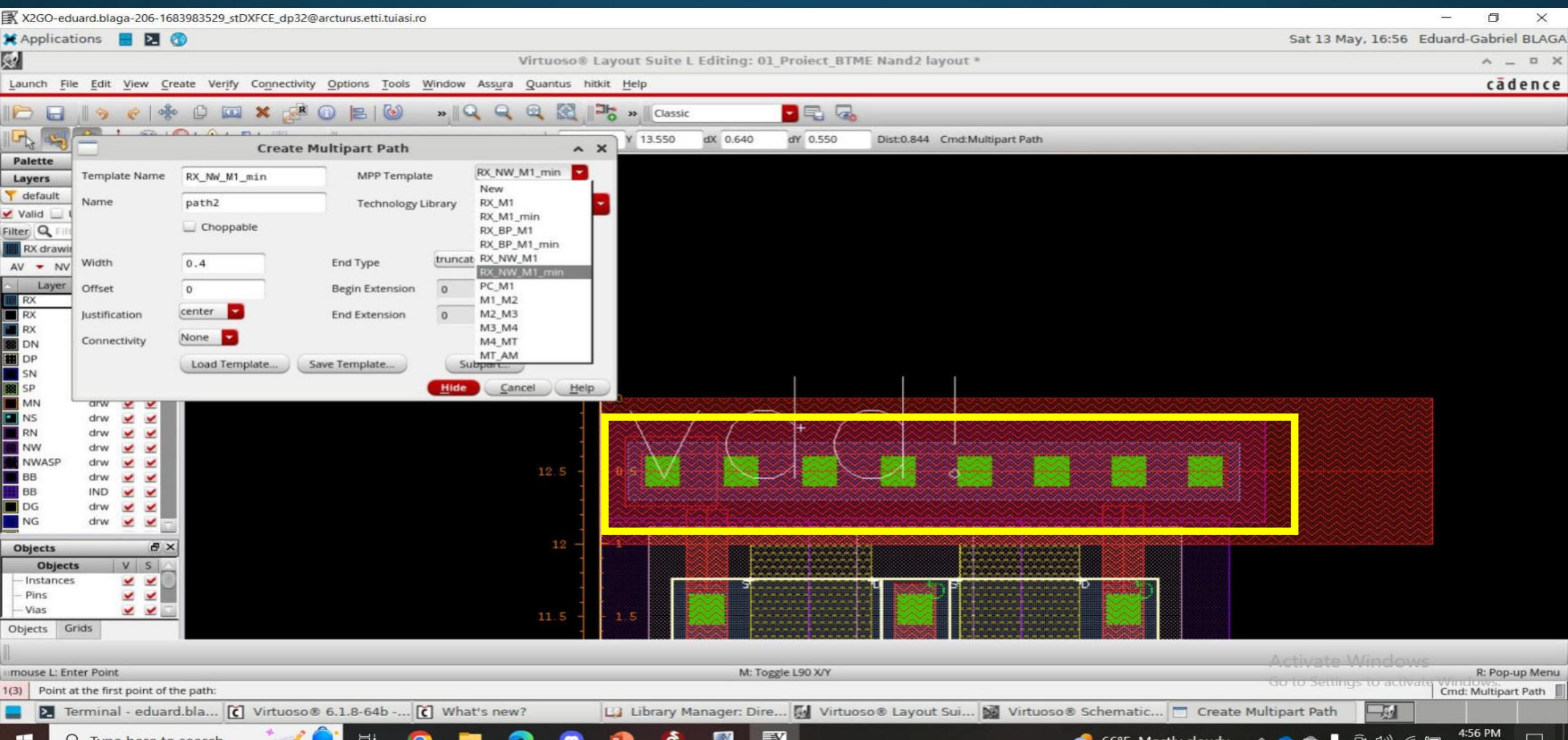
Se realizeaza conexiunile pentru iesirea portii pe M1 conectandu-se drenele tranzistoarelor pfetx cu drena tranzistorului nfetx



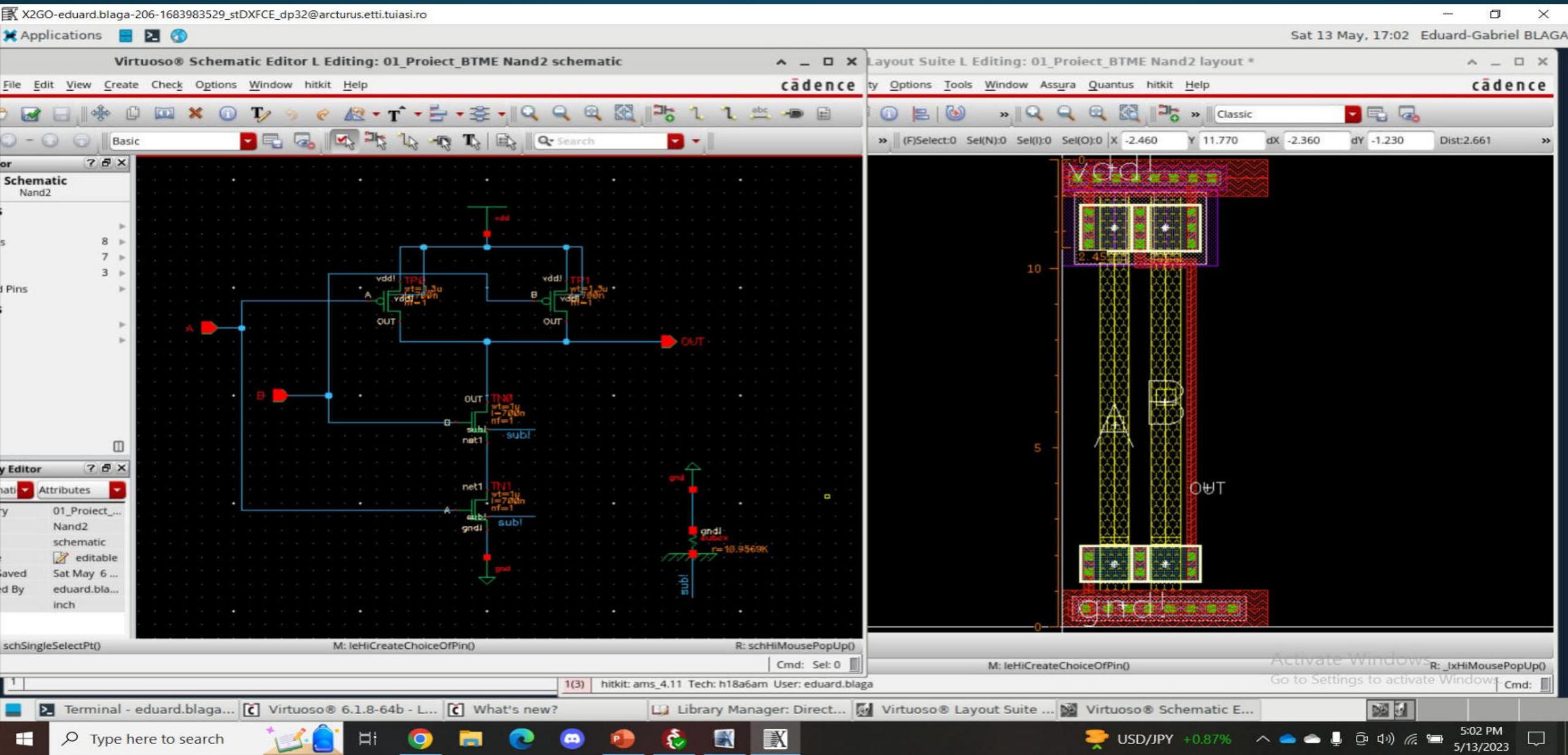
Se creeaza un MultipartPath -> F3 pentru activarea optiunilor -> se selecteaza MPP template RX_BP_M1_min si se pune pe linia de gnd



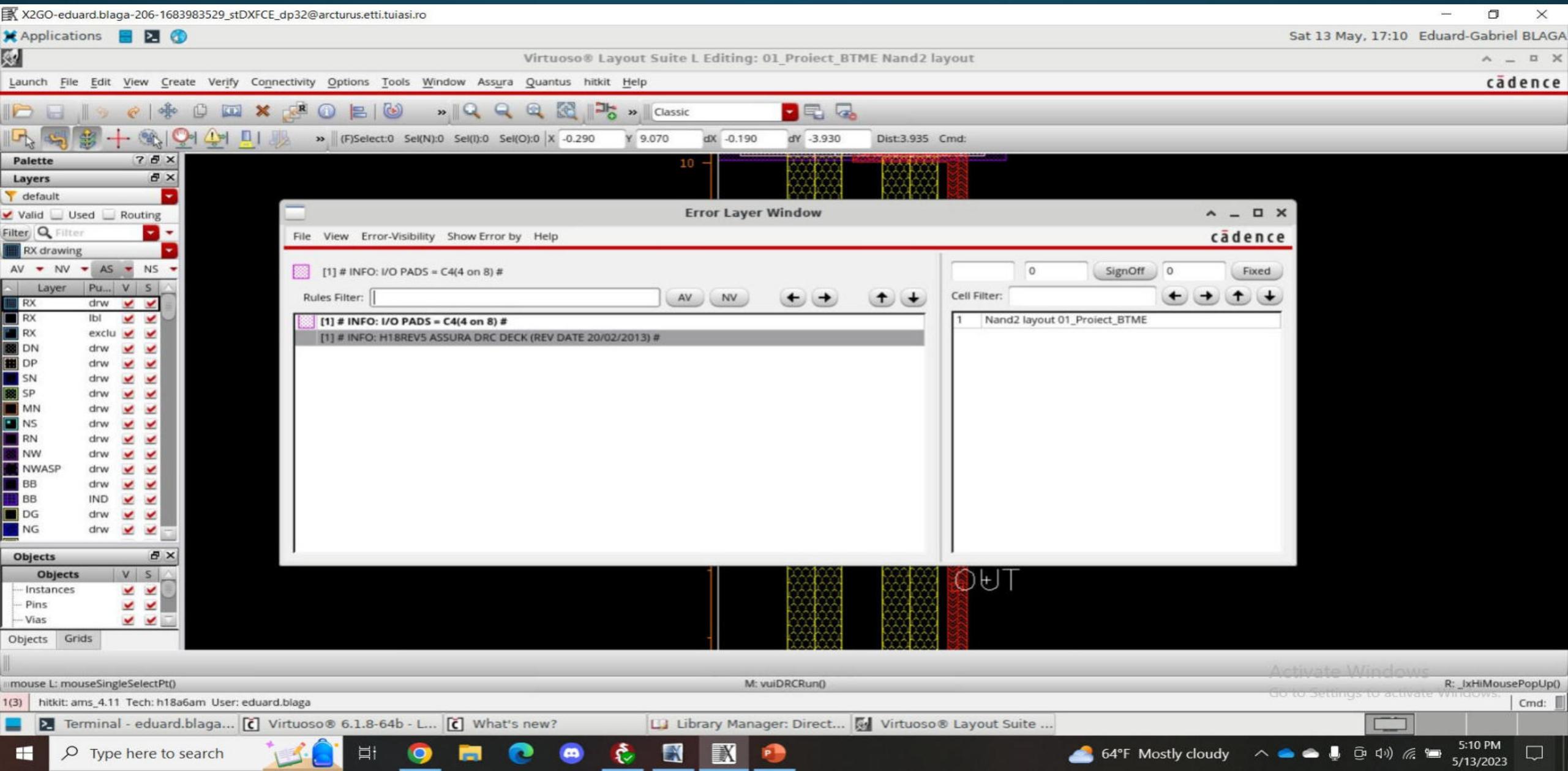
Identic se creaza un Multipart path pentru conexiunea Nwellului la vdd selectand selectand RX NW M1 min



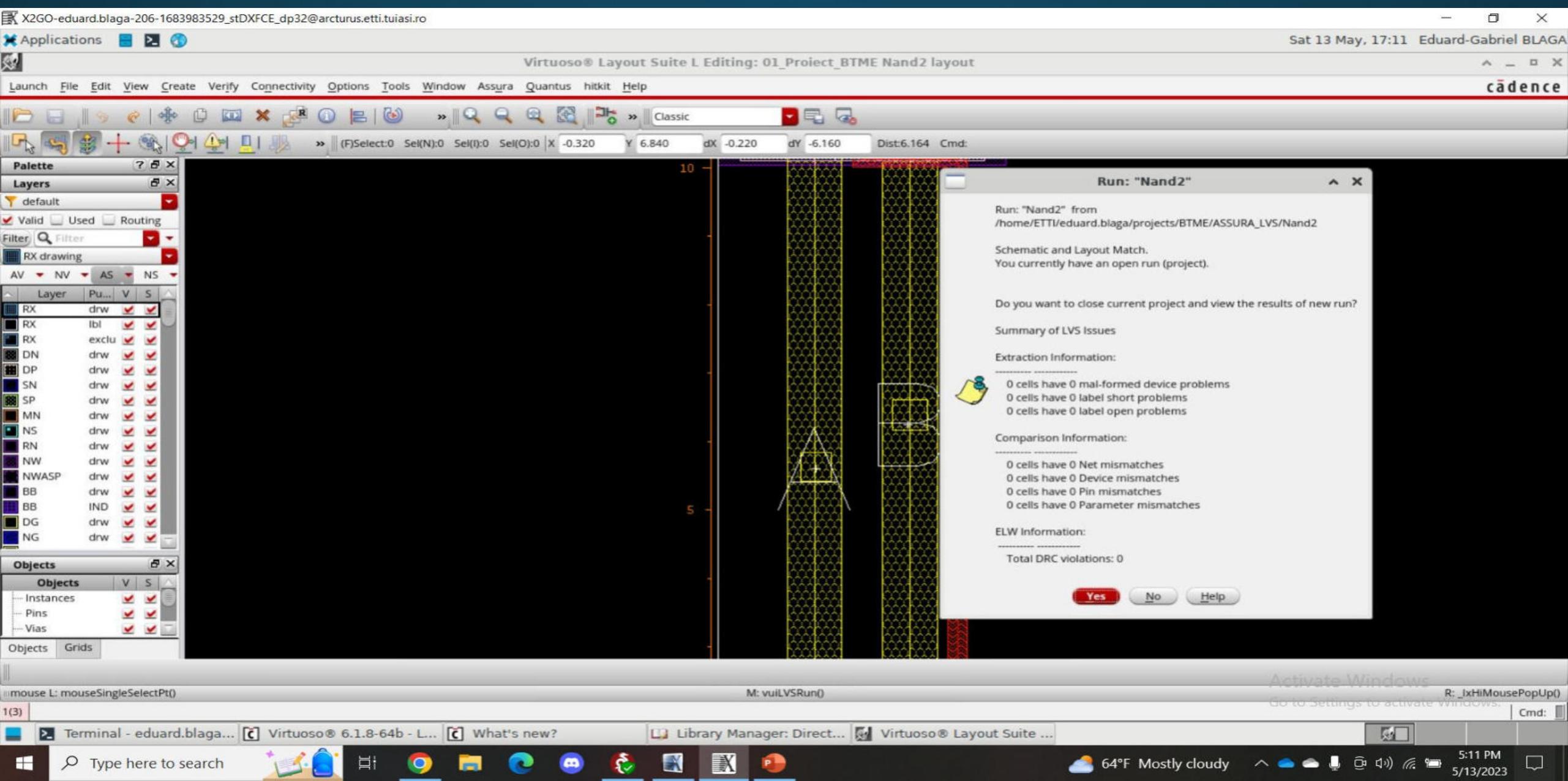
Se plaseaza pini de vdd! si gnd! de tip inputOutput apoi pinul OUT de tip Output pe M1 si pinii A si B de tip input pe PC



Se realizeaza verificarea DRC



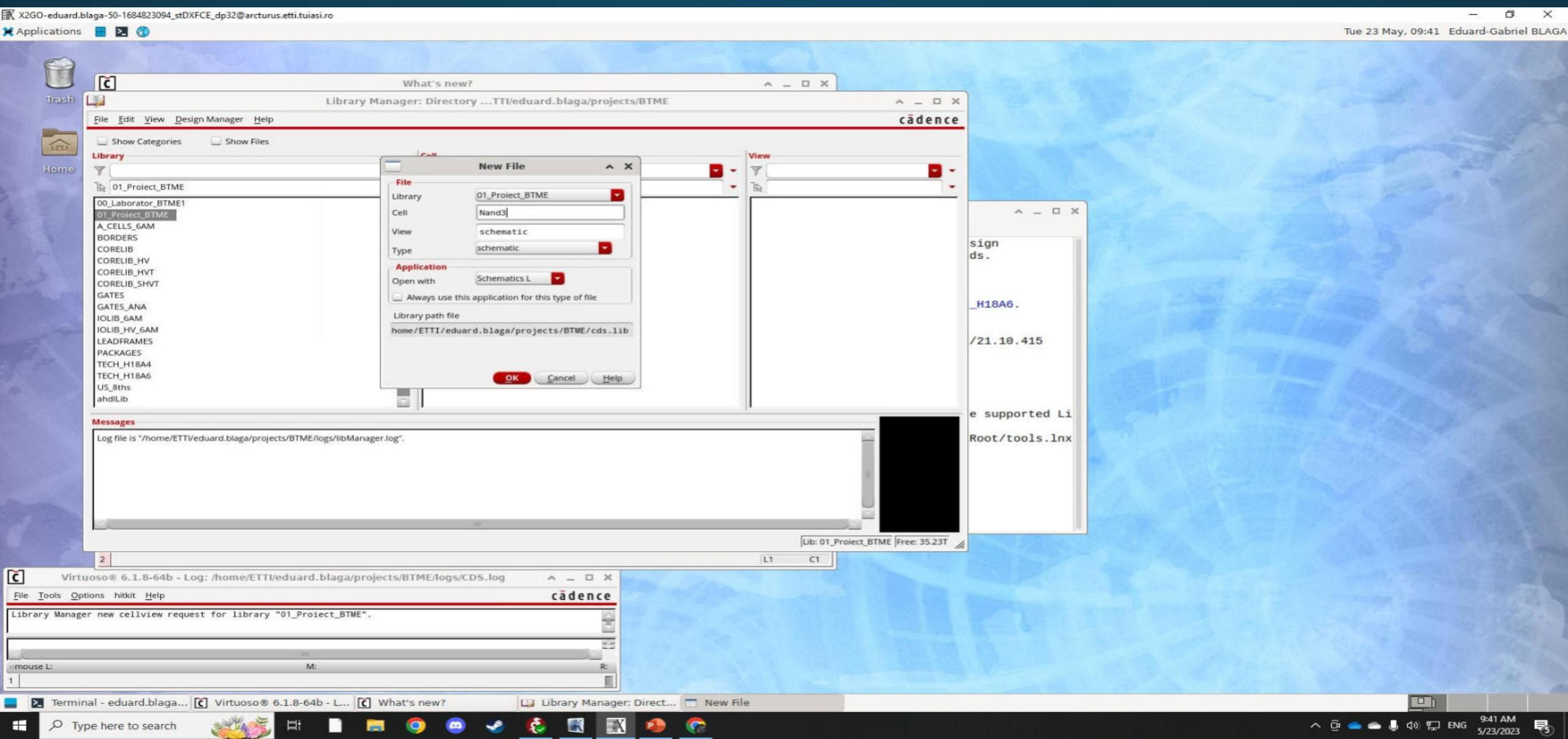
Se realizeaza verificarea LVS





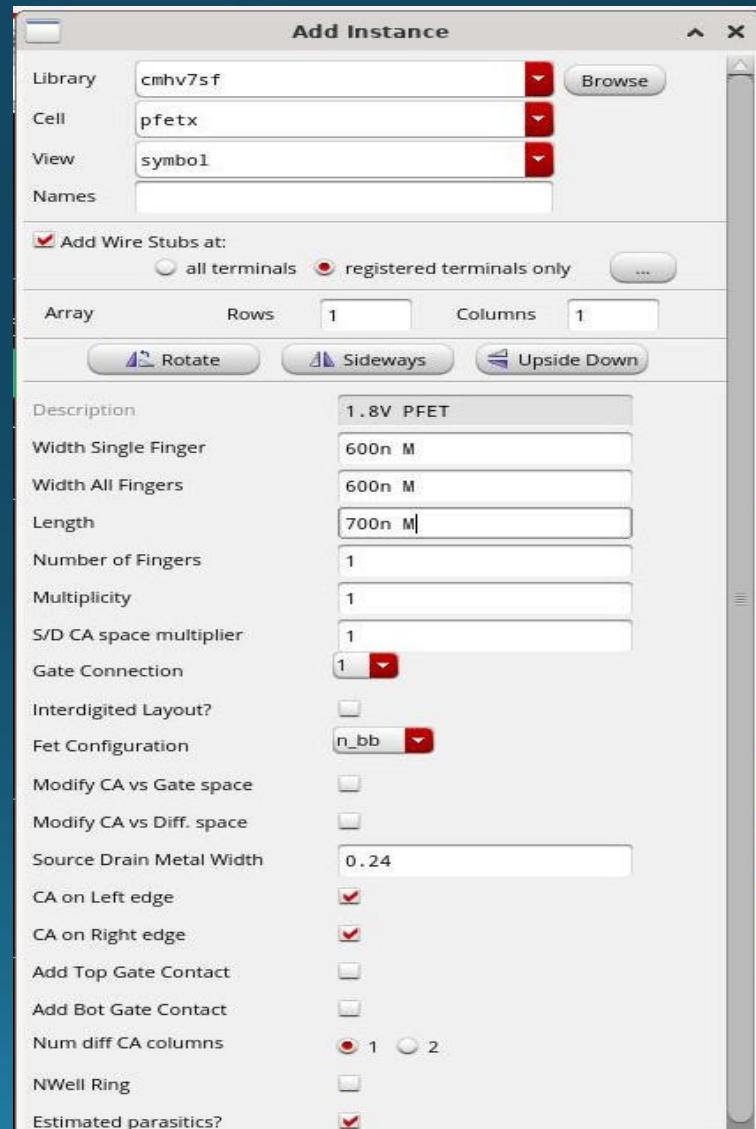
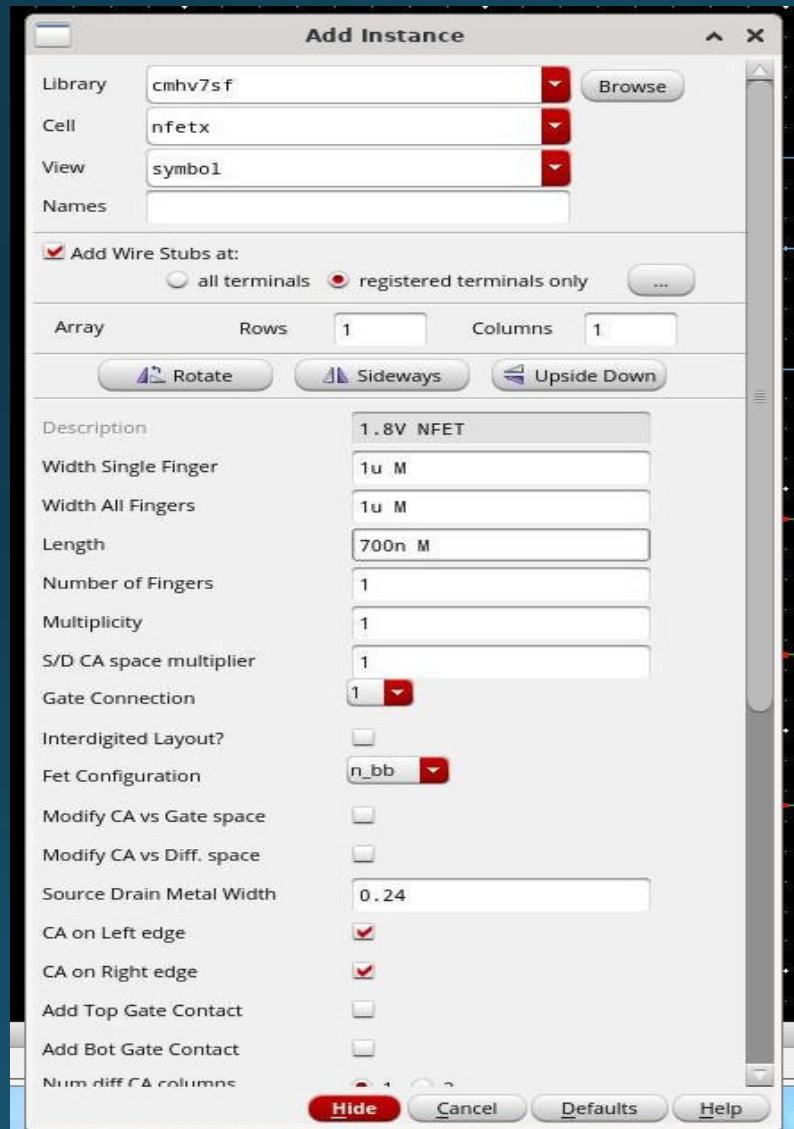
NAND 3

Se creeaza un nou cell view de tip schematic

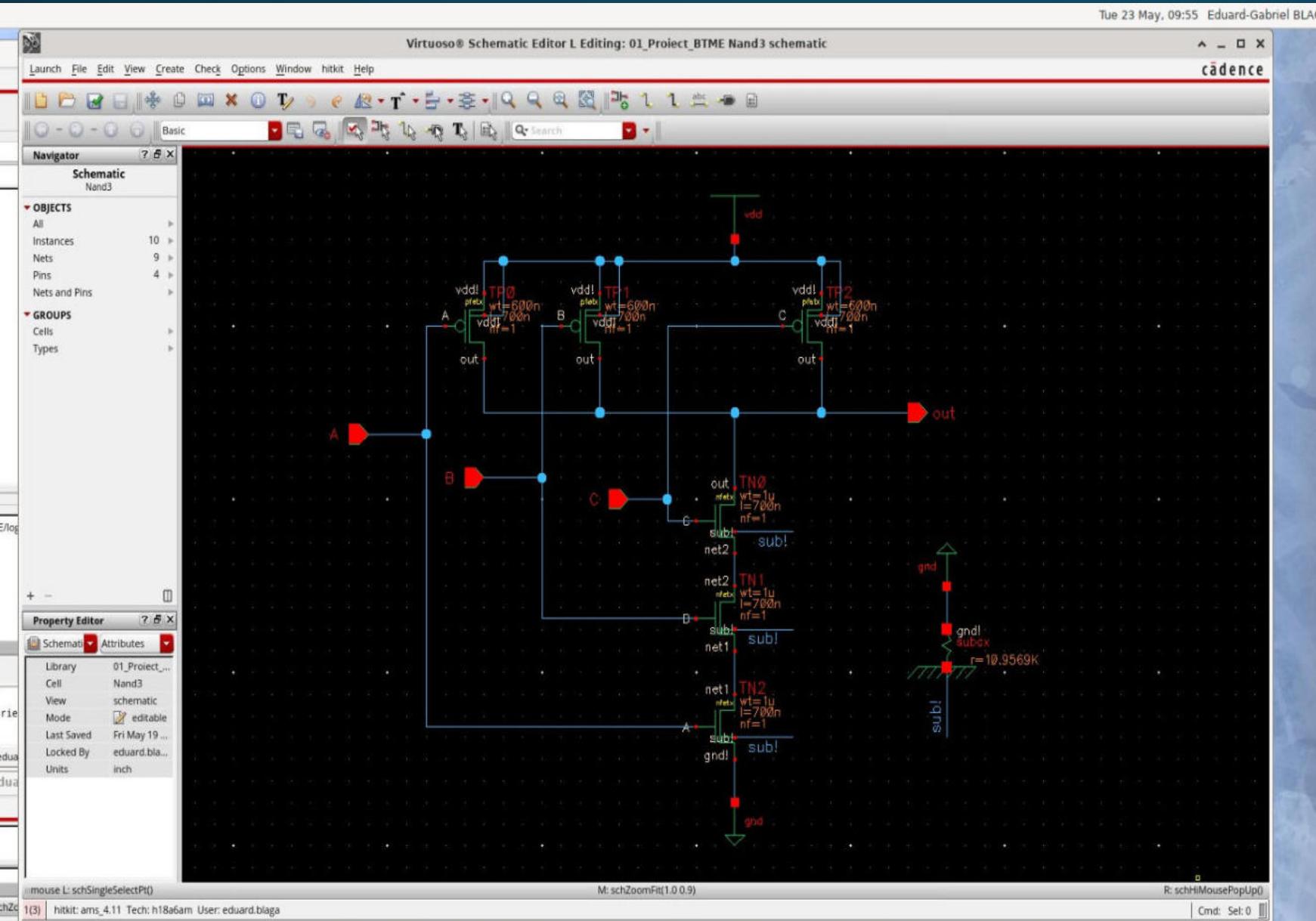


Pentru poarta Nand3 se respecta pasii anteriori pentru crearea Nand2,
dar cu mici modificari.

Prima modificare apare la dimensionarea tranzistoarelor

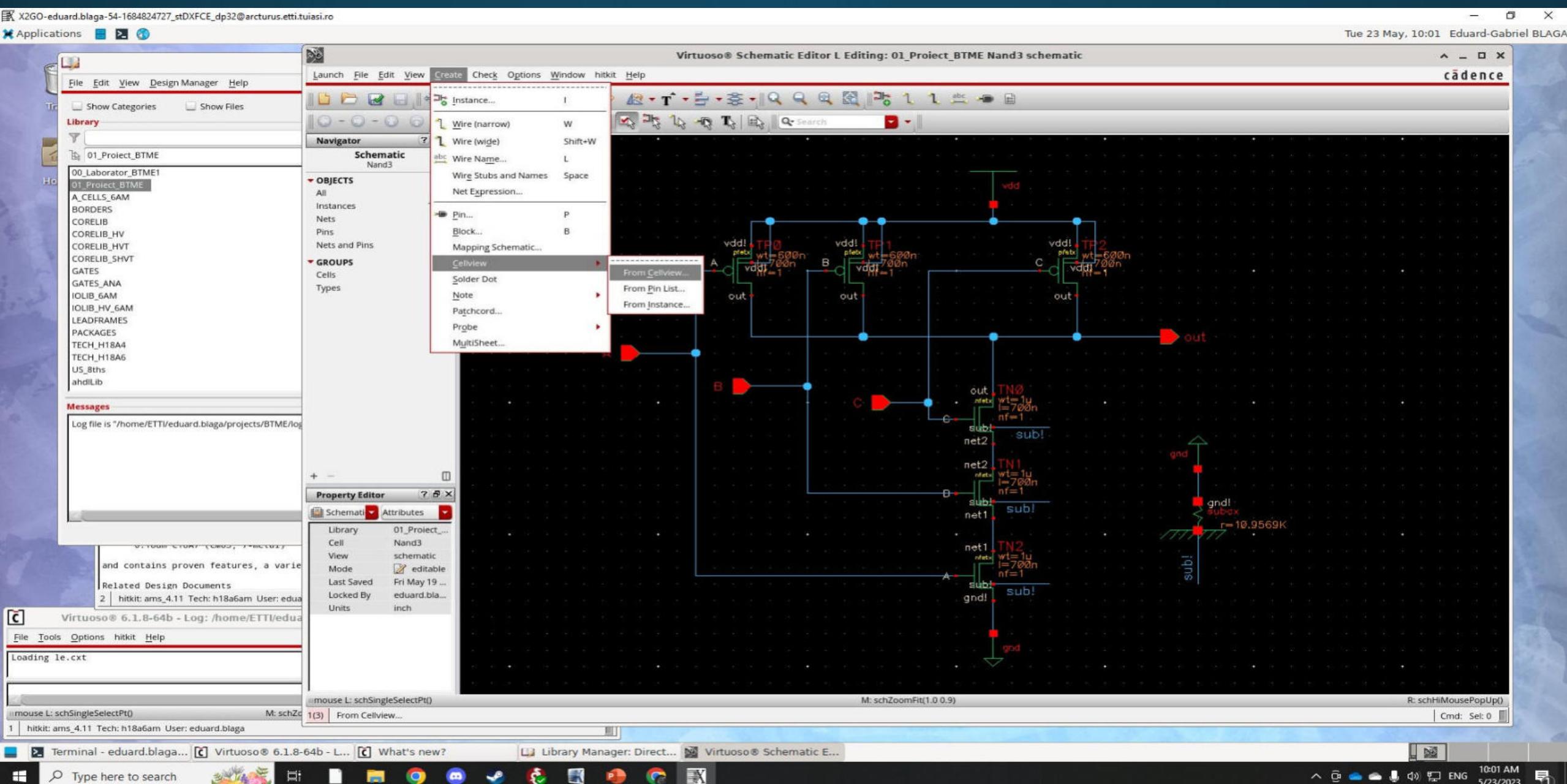


Intocmim schematicul

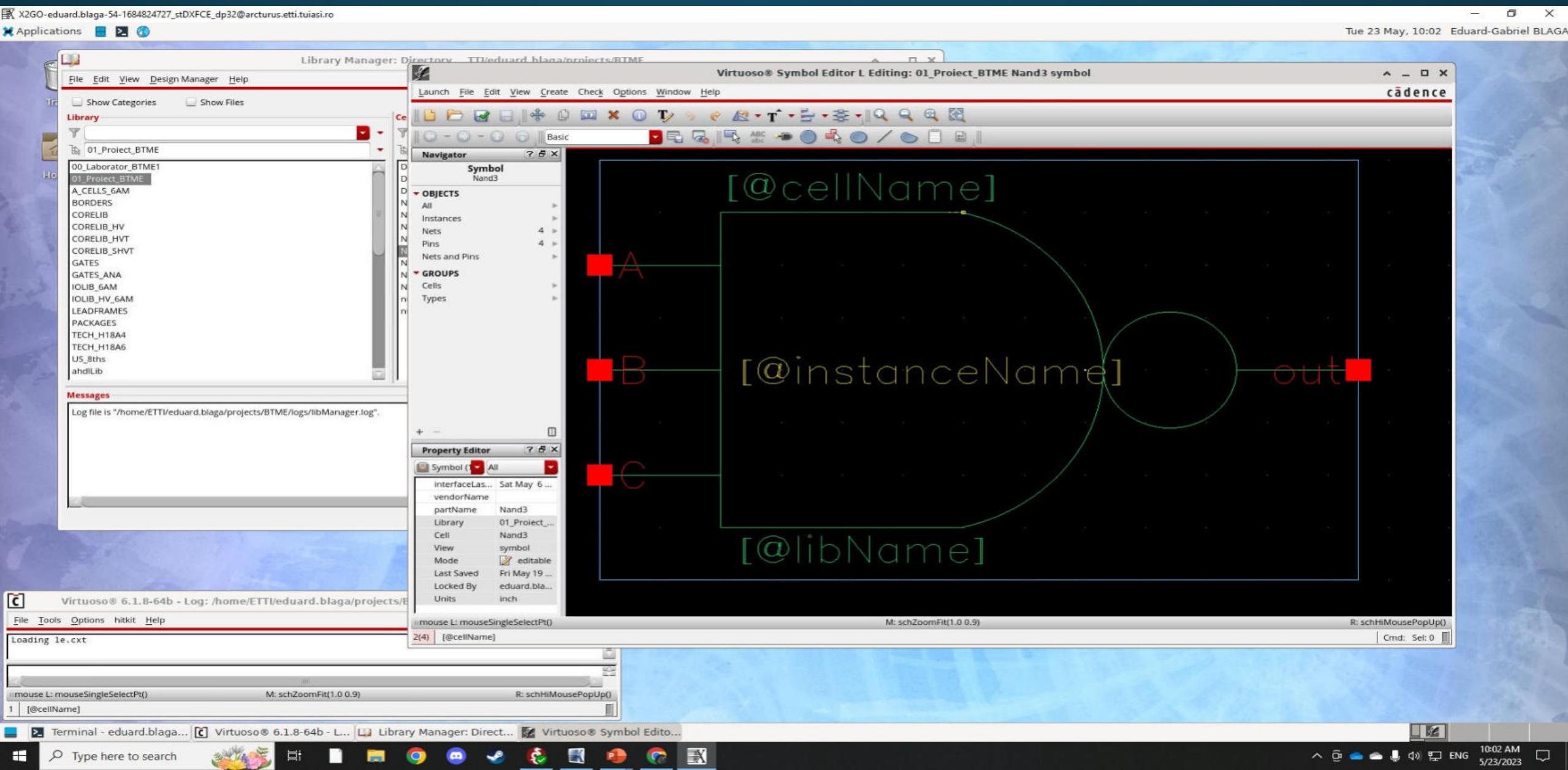


- Fata de Nand2, va mai trebui sa realizam un pin de tip Input cu denumirea C

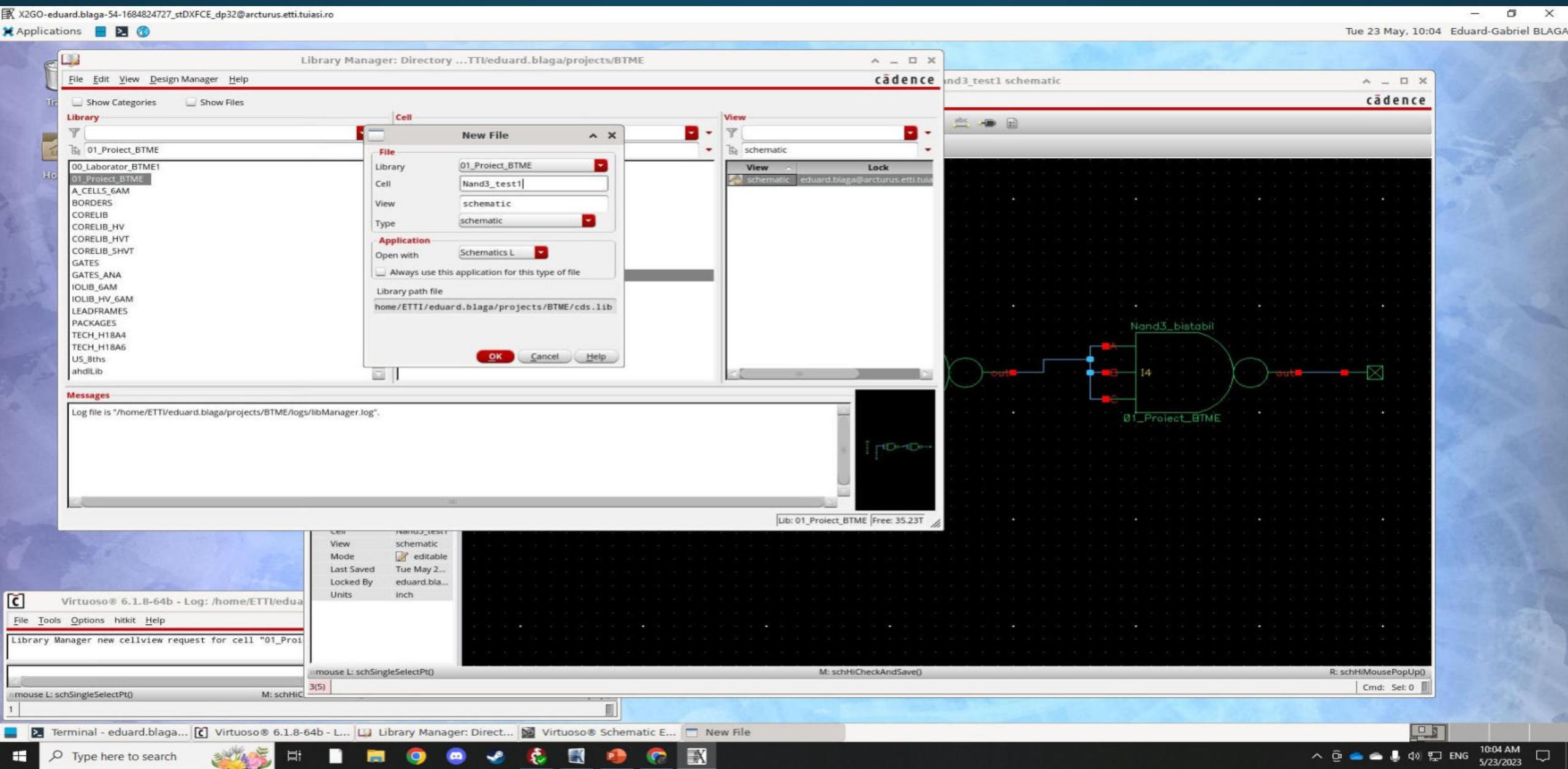
Crearea simbolului Nand3



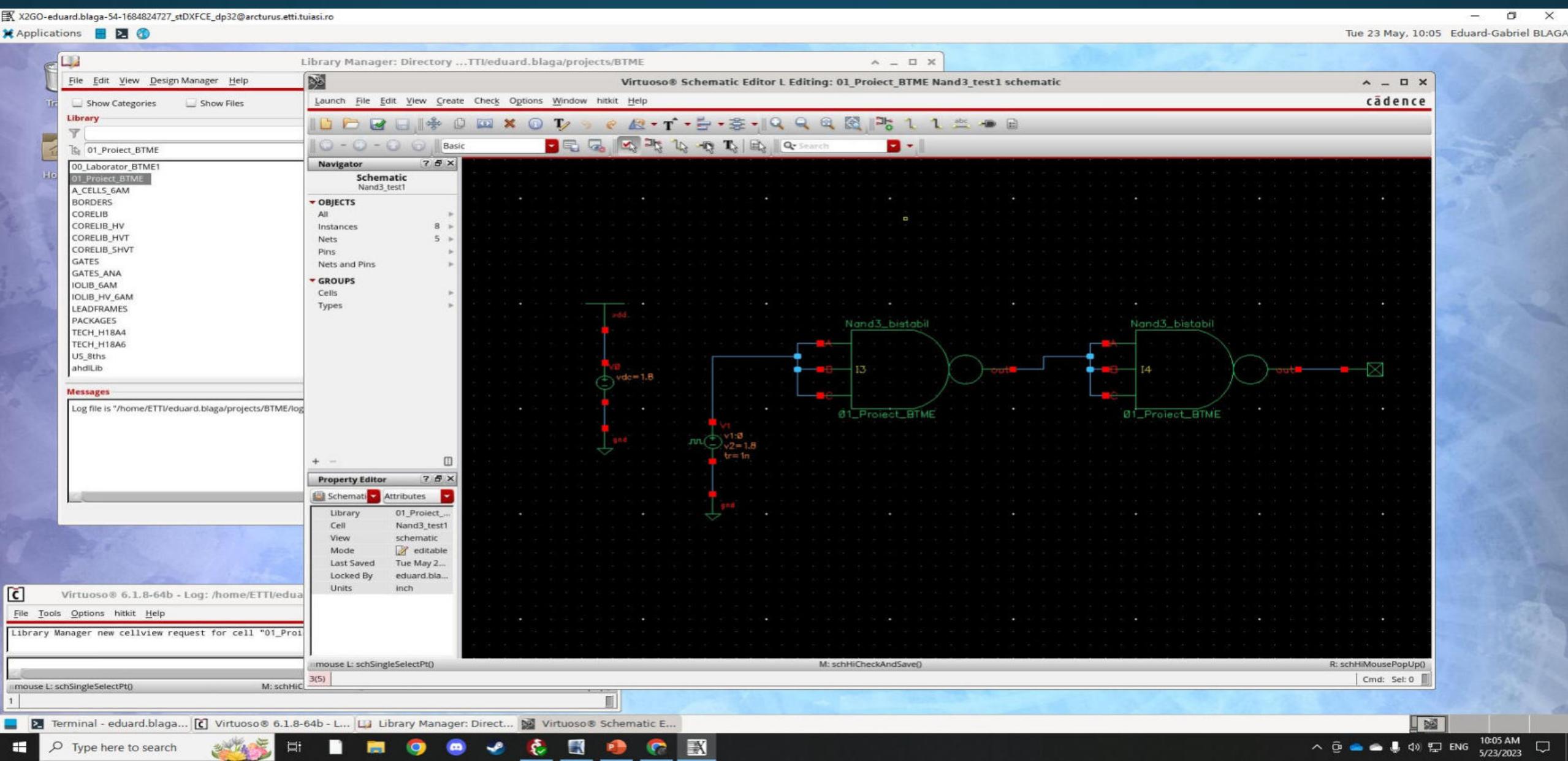
Realizam simbolul Nand3



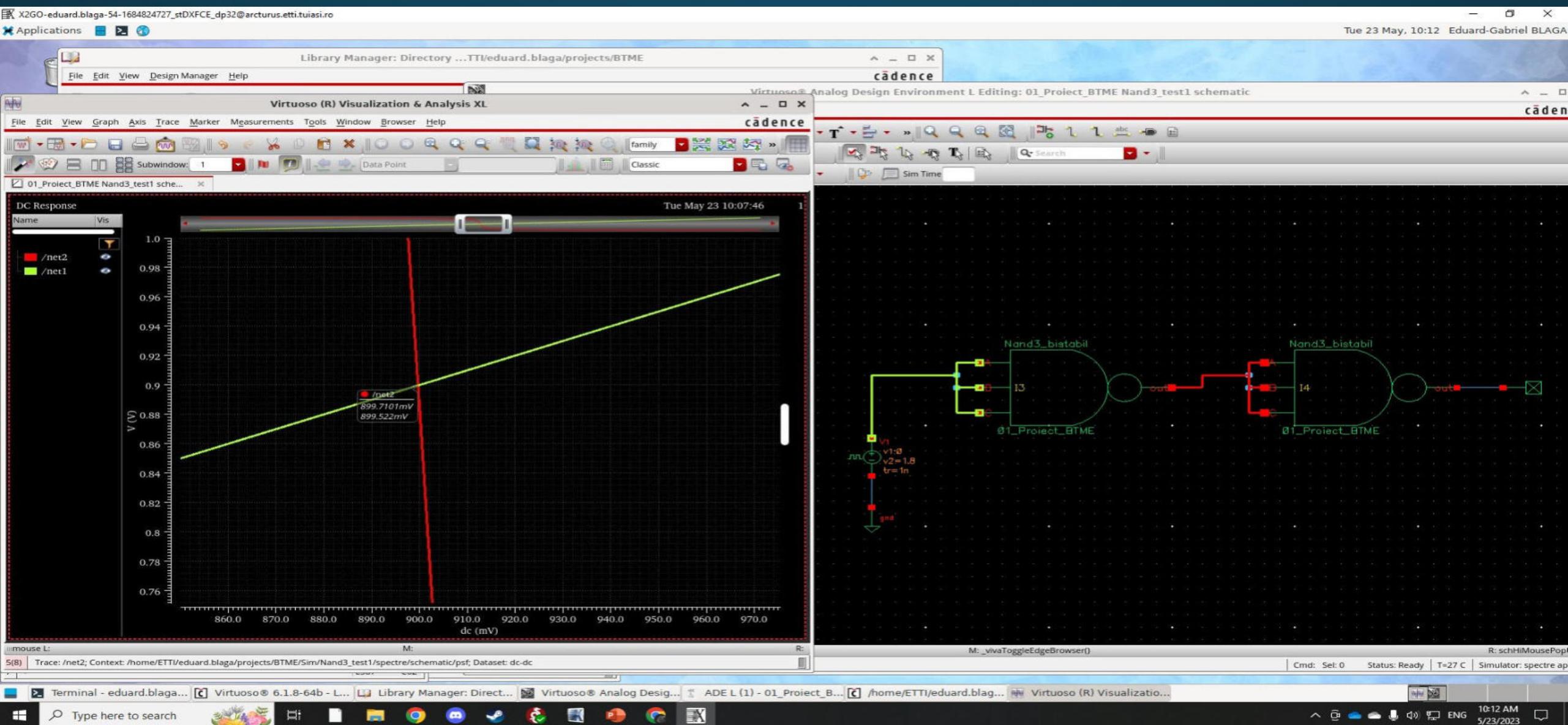
Se realizeaza un cell view pentru testarea portii Nand3



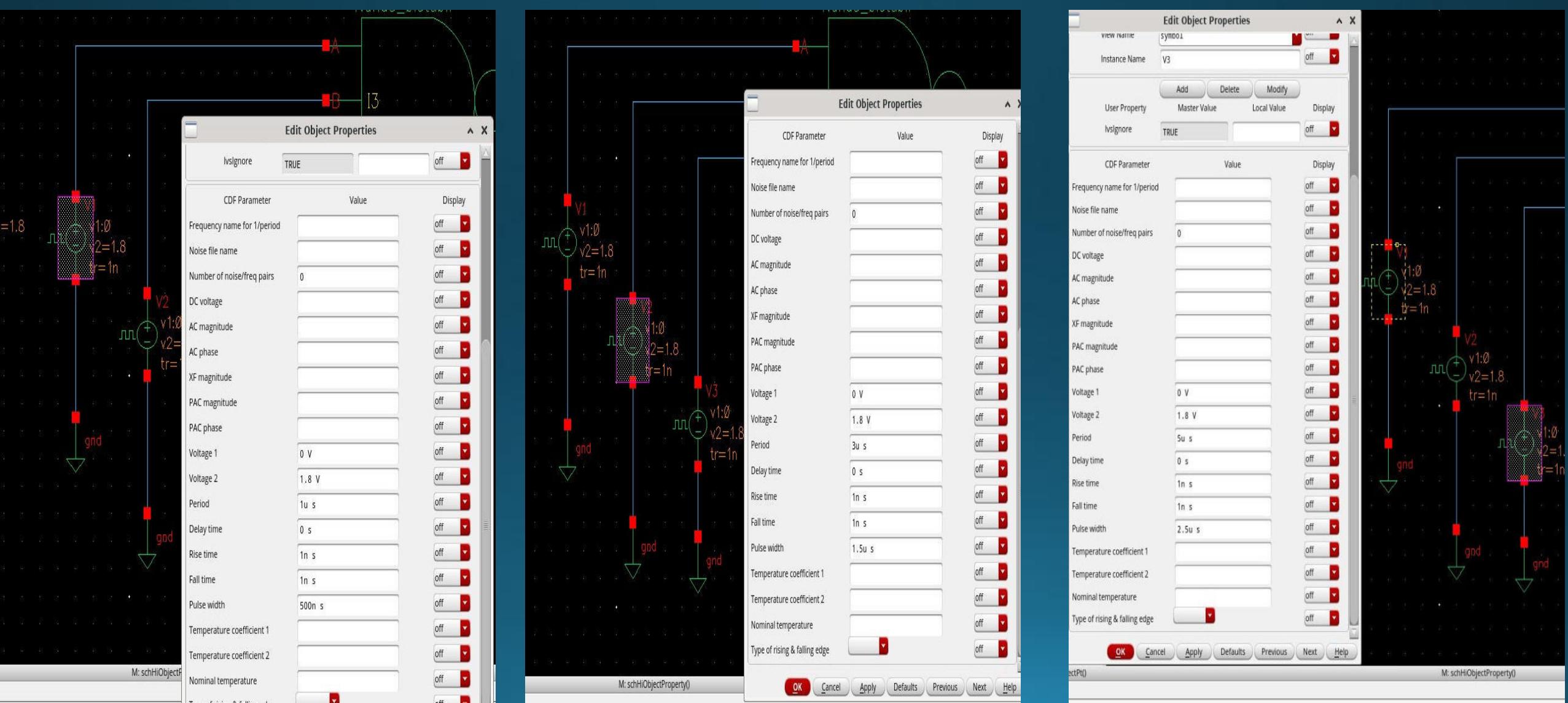
Se realizeaza schema de test



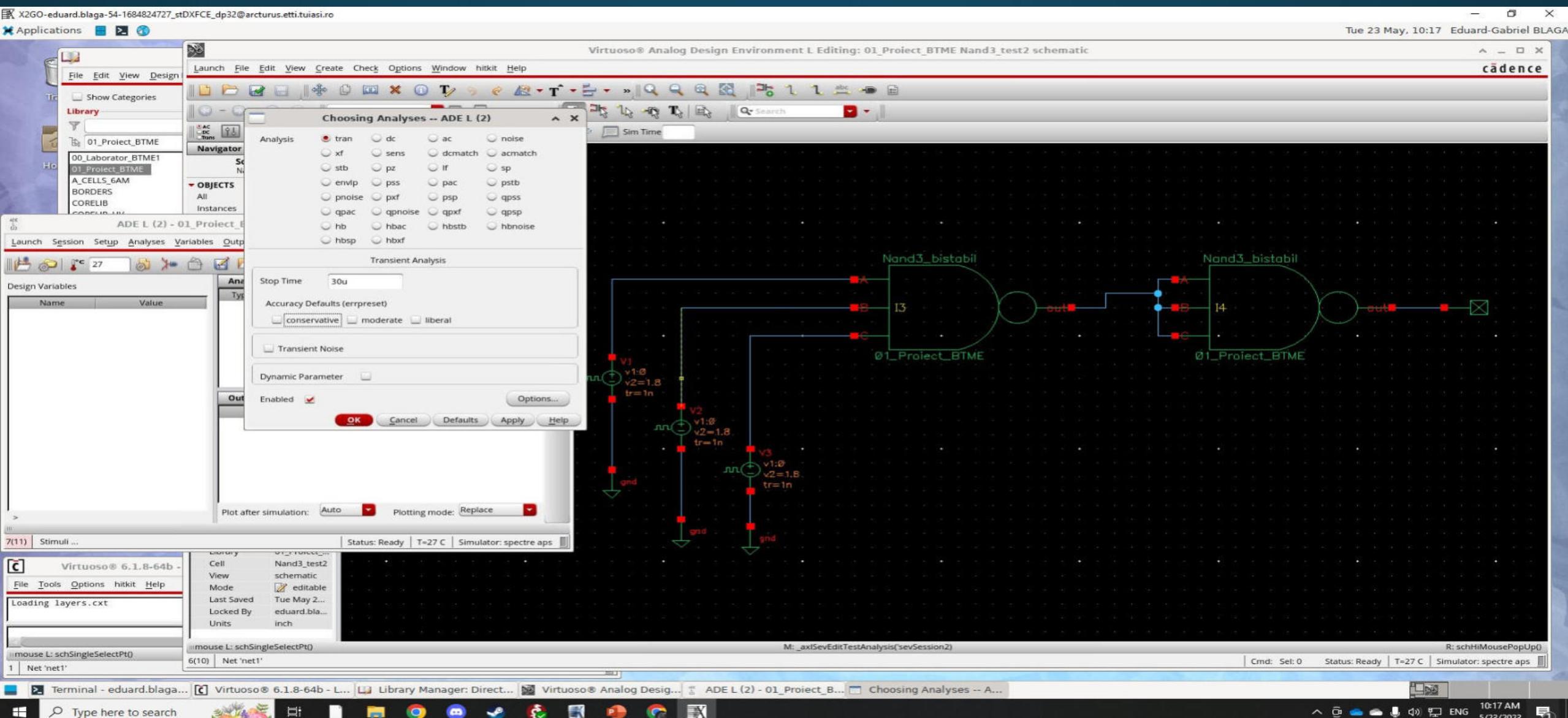
Se realizeaza o analiza DC si se identifica punctul de comutare care ar trebui sa fie la $V_{DD}/2$ (900mV)



Pentru analiza tranzitorie se aplica pe intrari trei surse vpulse cu diferite perioade



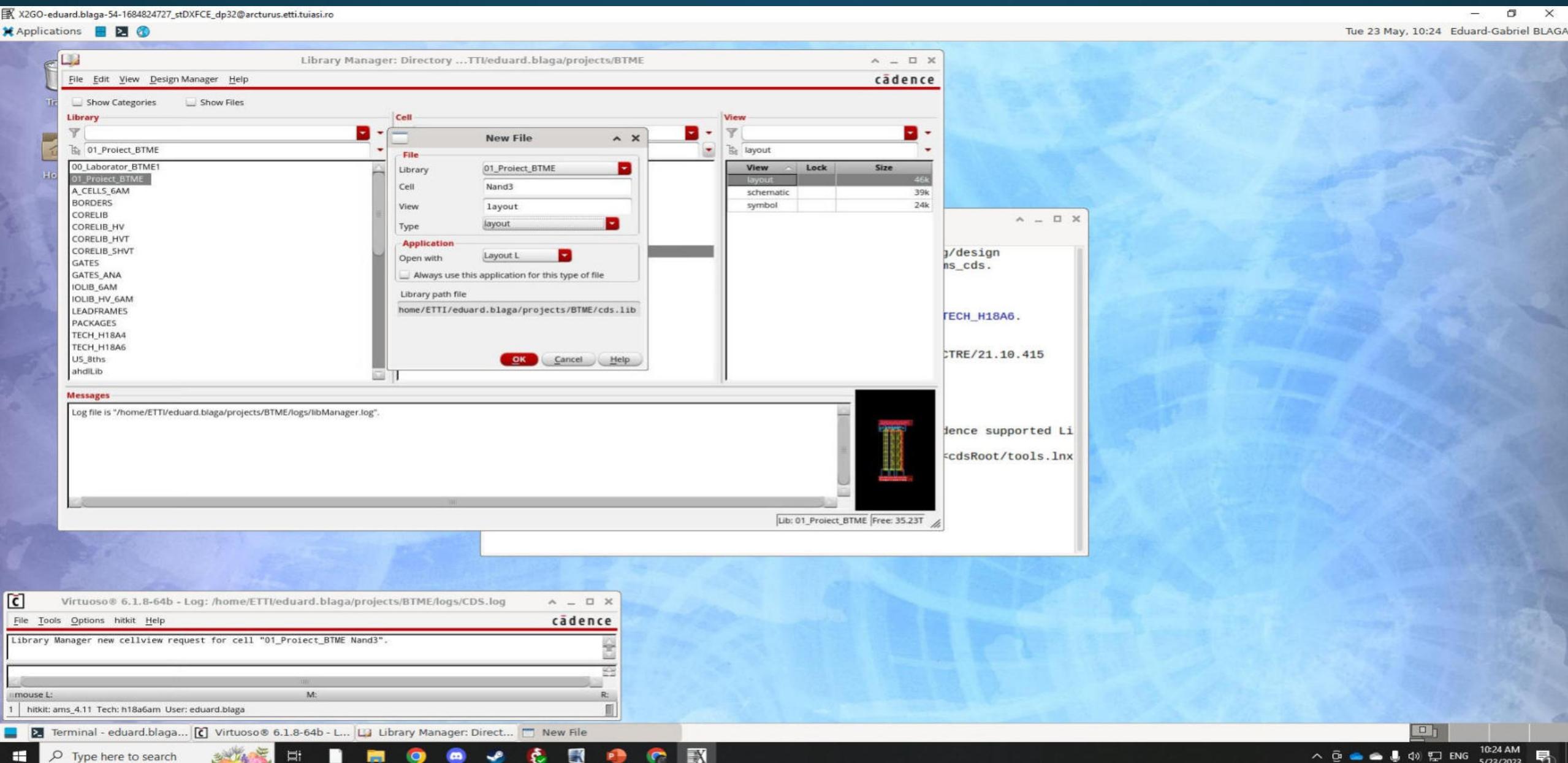
Se realizeaza o analiza tranzitorie



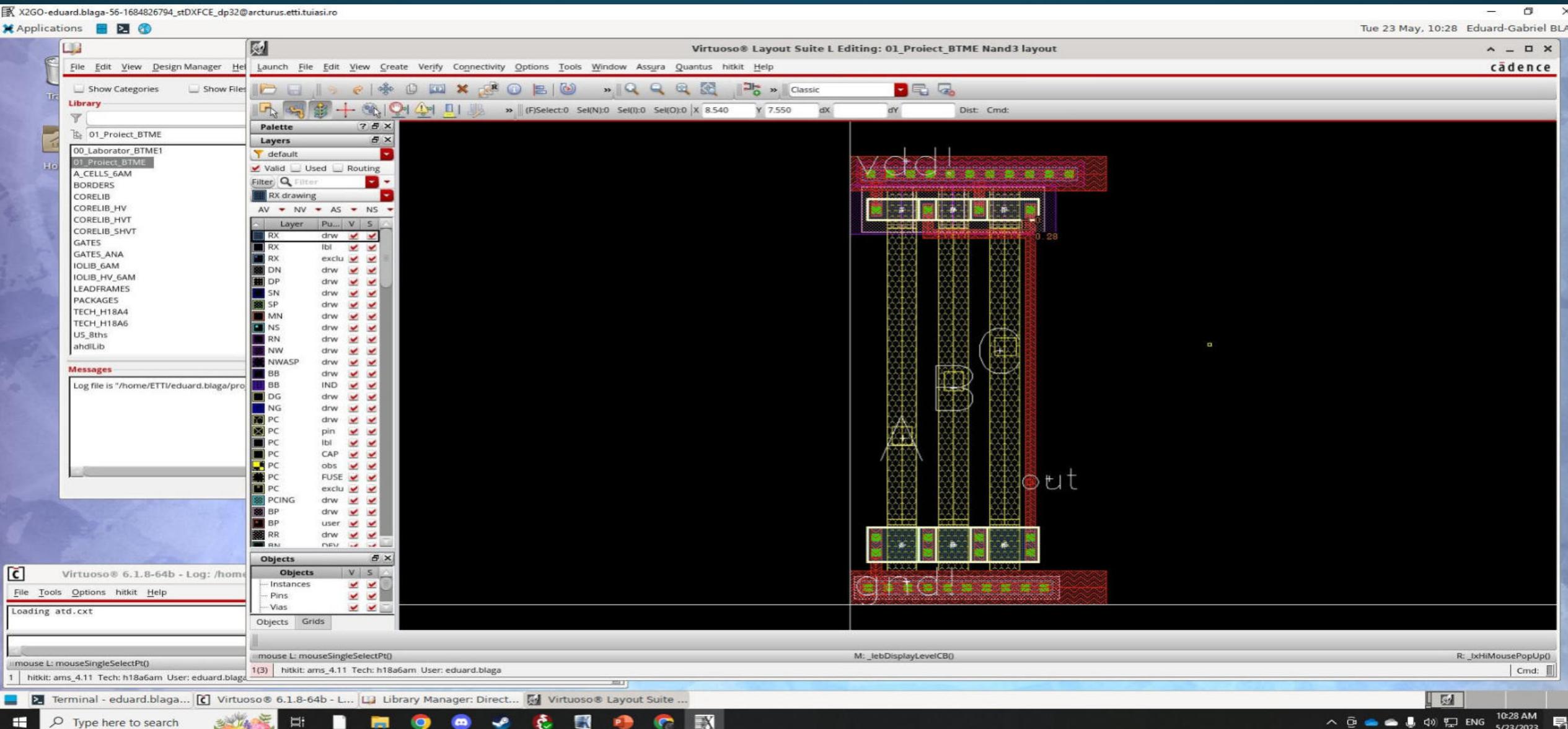
Se reface simularea si se ploteaza forma de unda in timp



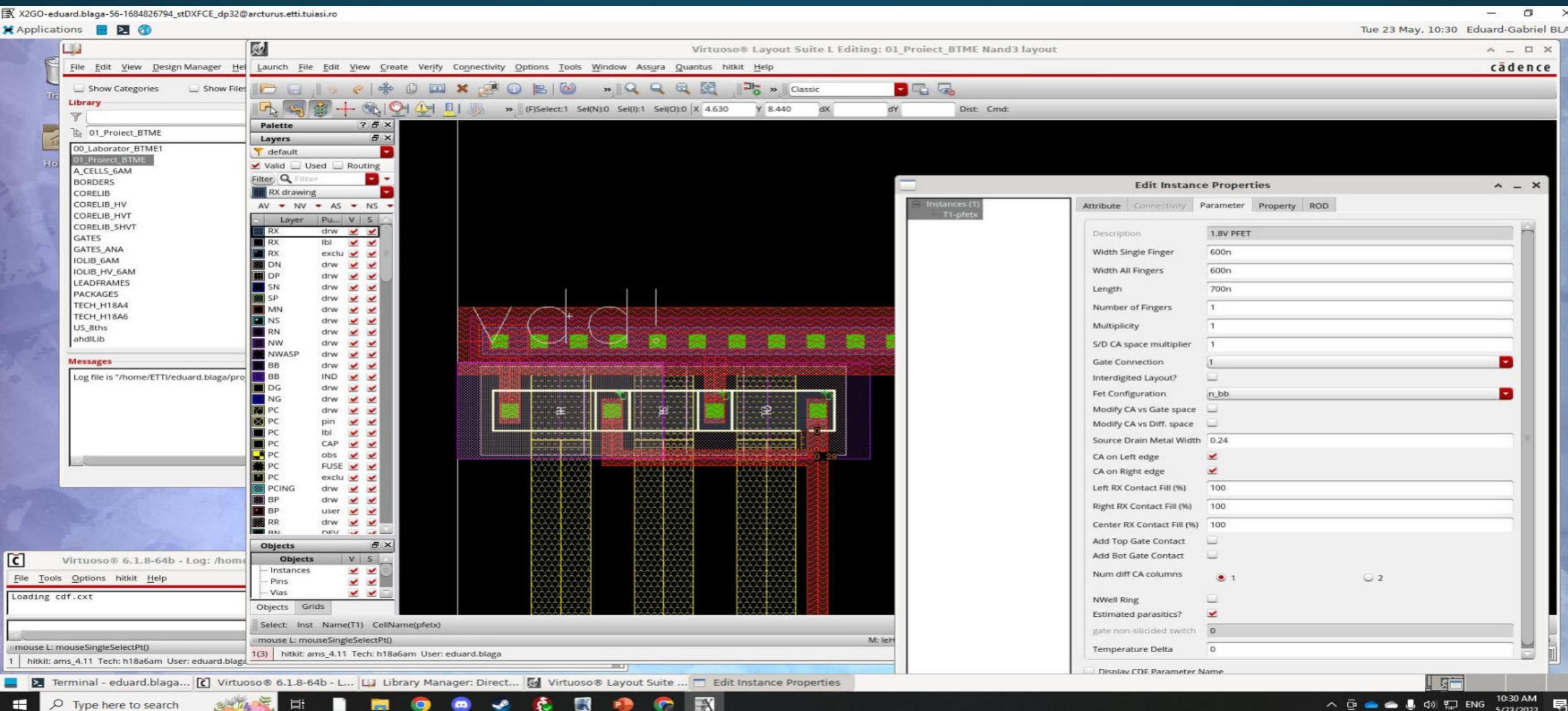
Se creeaza un cell view cu aceeasi denumire dar de tip layout



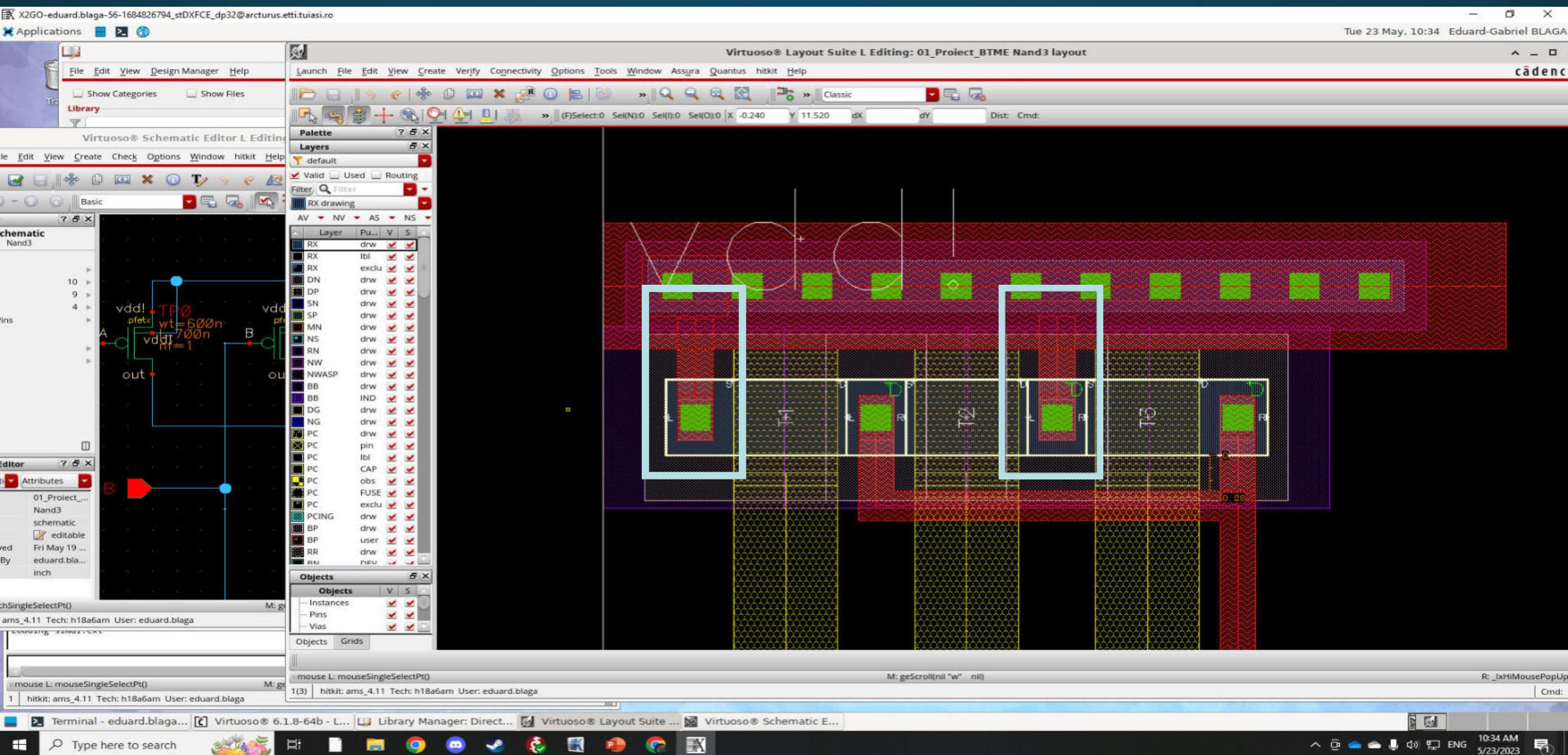
Se respecta pasii de creeare layout ca si pentru Nand2, cu mici modificari



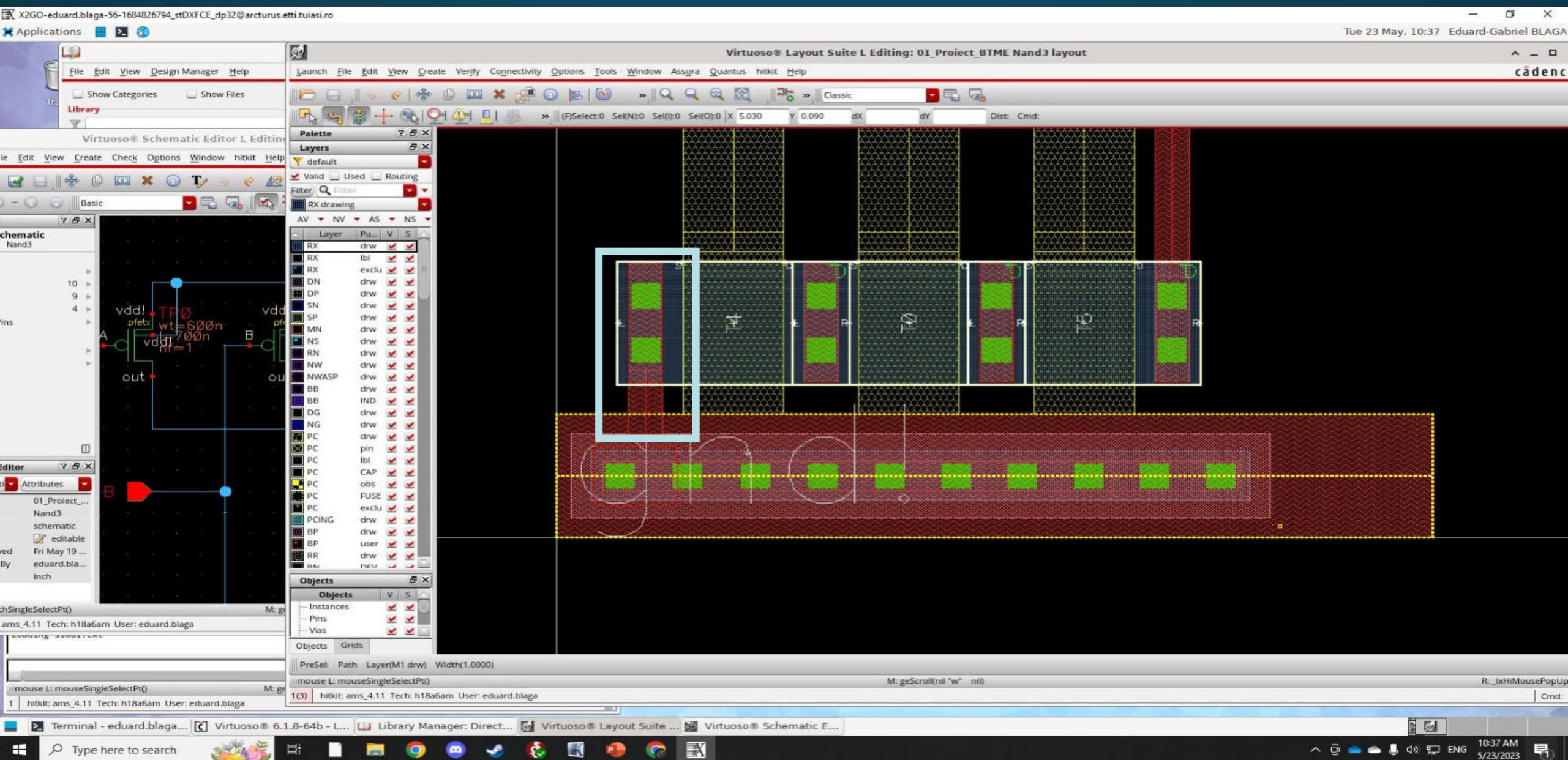
Dimensiunile tranzistoarelor pfetx sunt modificate corespunzator schematicului, cele nfetx raman la fel cu $L=0.7\mu$ si $W=1\mu$



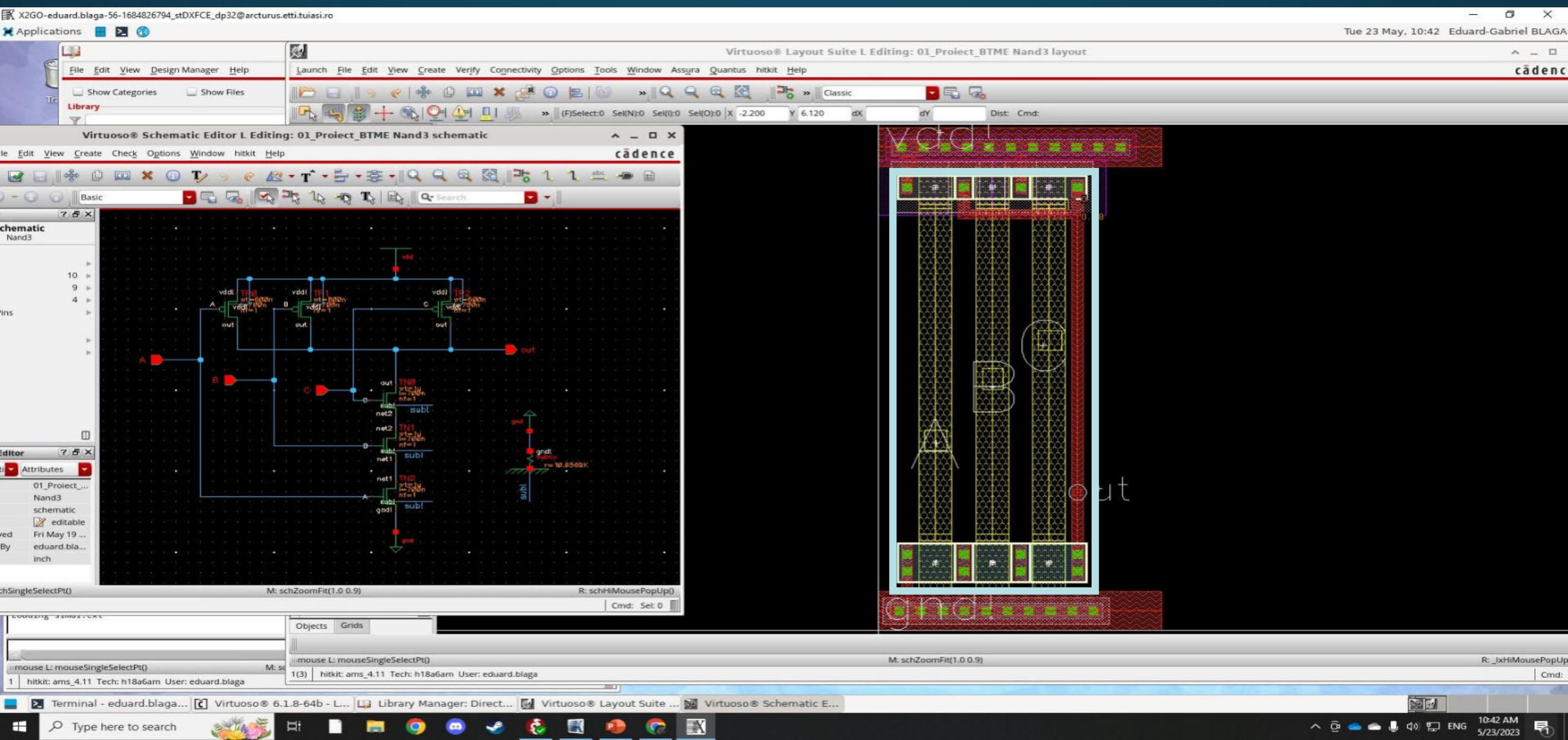
Sursele se conecteaza la vdd si ground



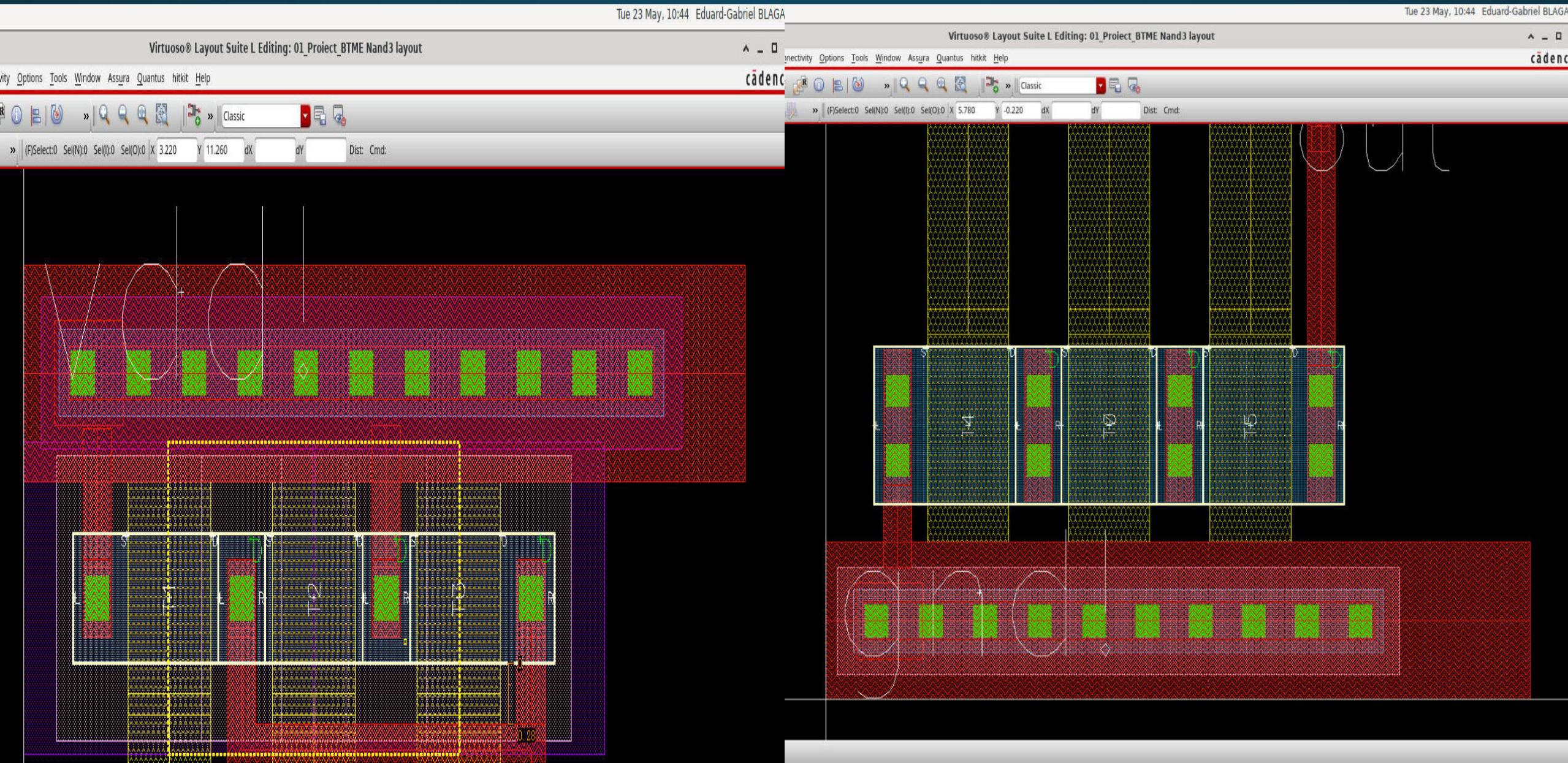
Sursele se conecteaza la vdd si ground



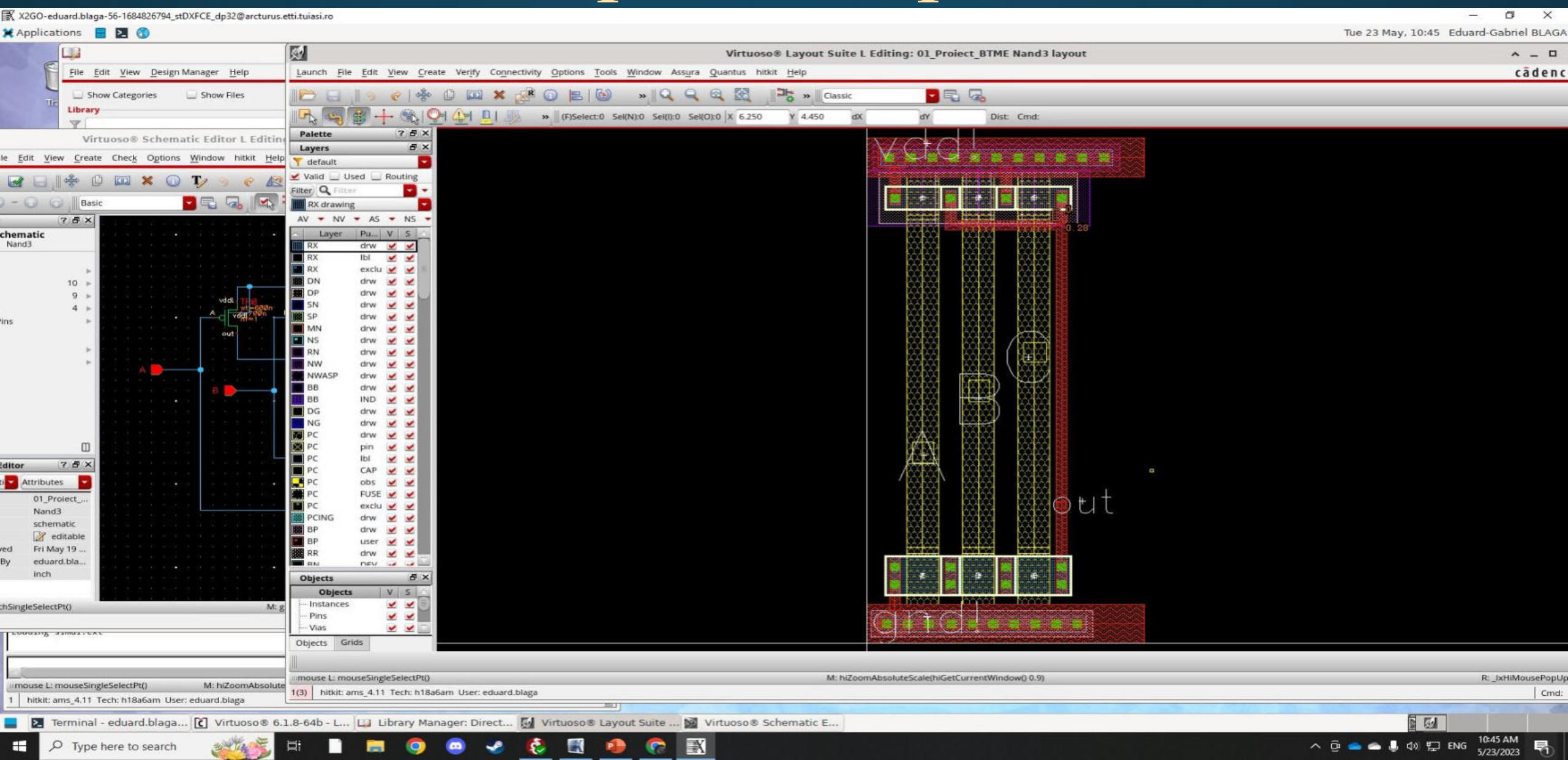
Se realizeaza conexiunile intre grille pe PC si iesirea portii pe M1 prin legatura drenelor tranzistoarelor



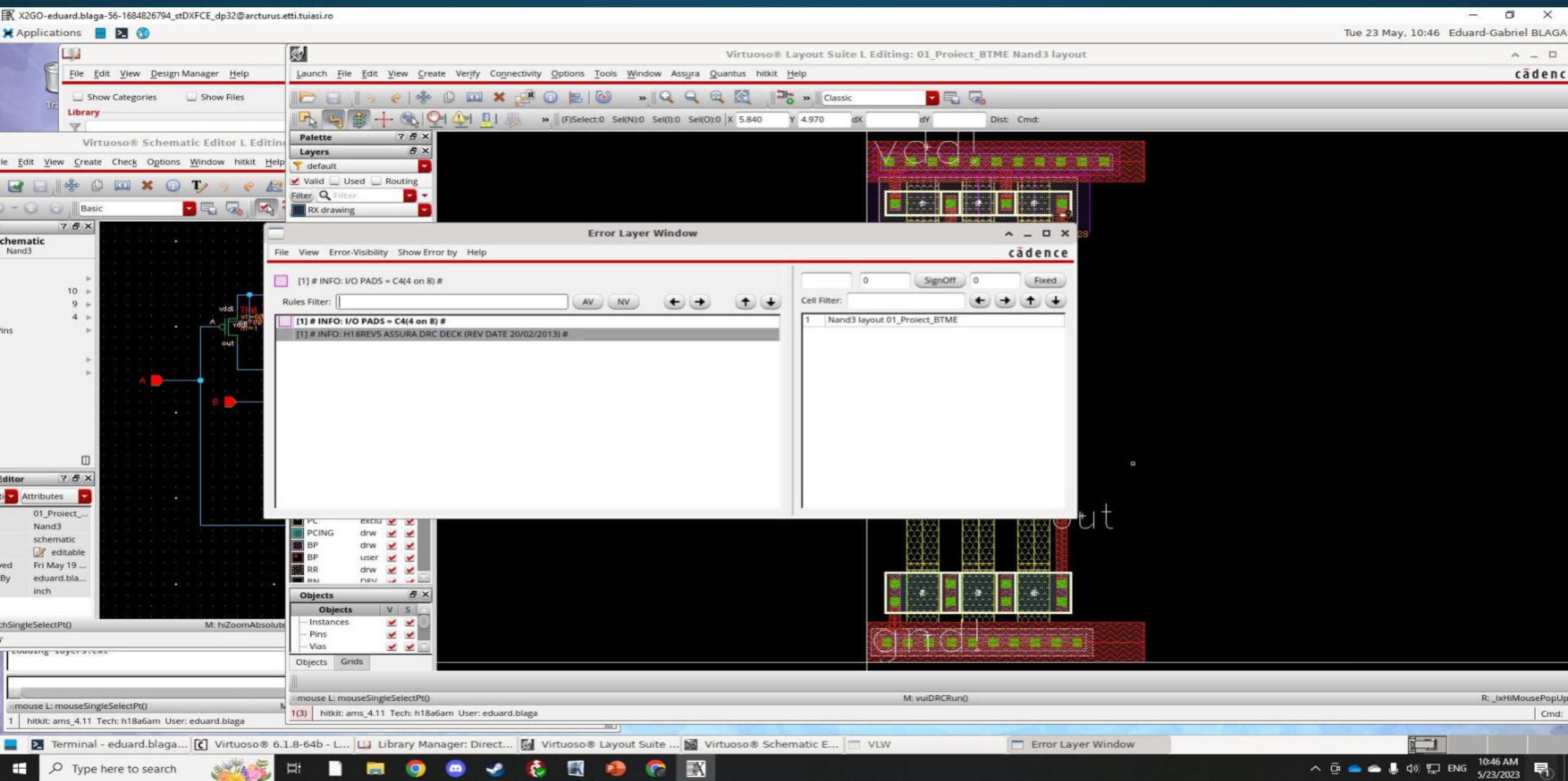
Se traseaza MultiPart Path-urile pentru liniile de gnd si vdd



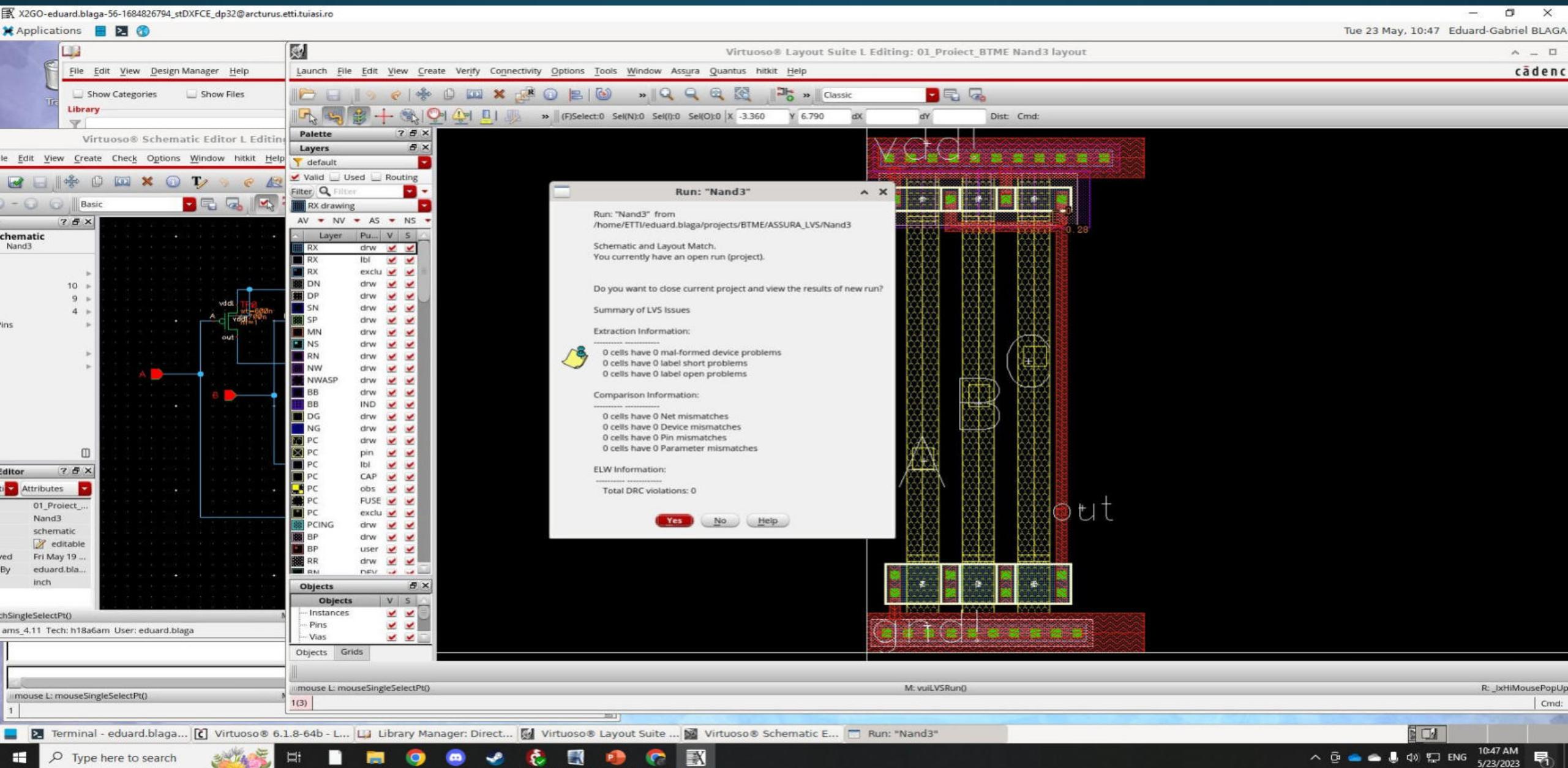
Se plaseaza pinii



Se realizeaza verificarea DRC

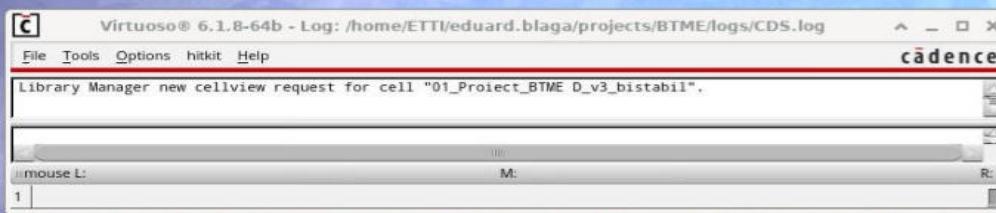
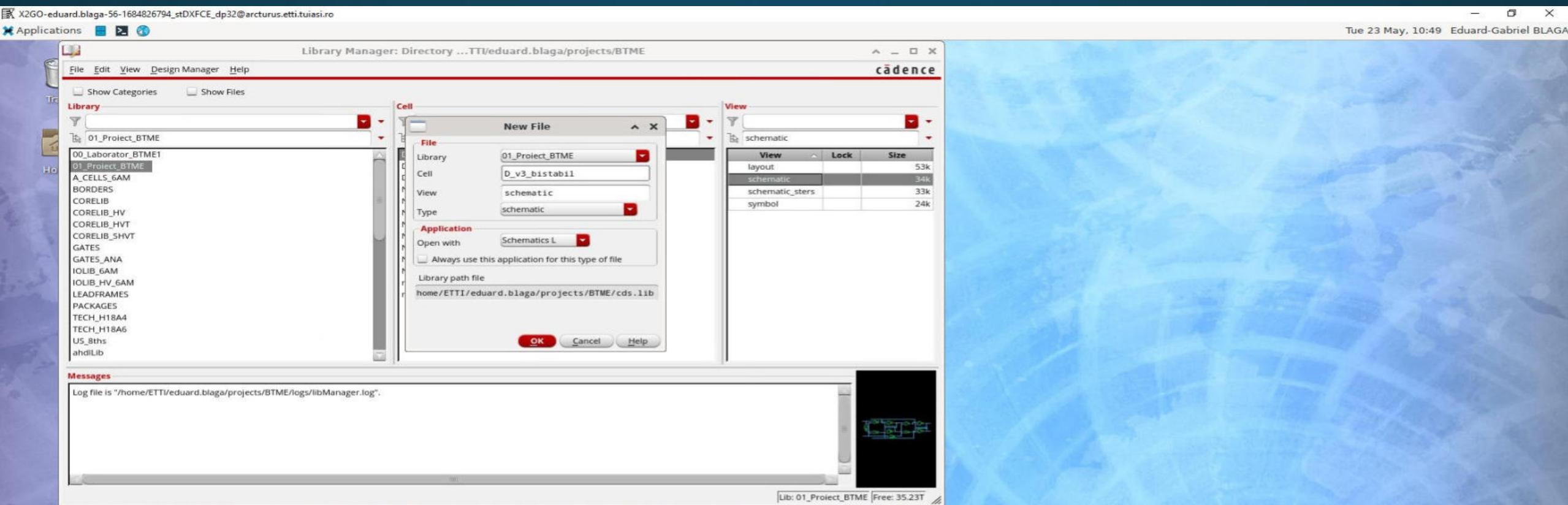


Se realizeaza verificarea LVS



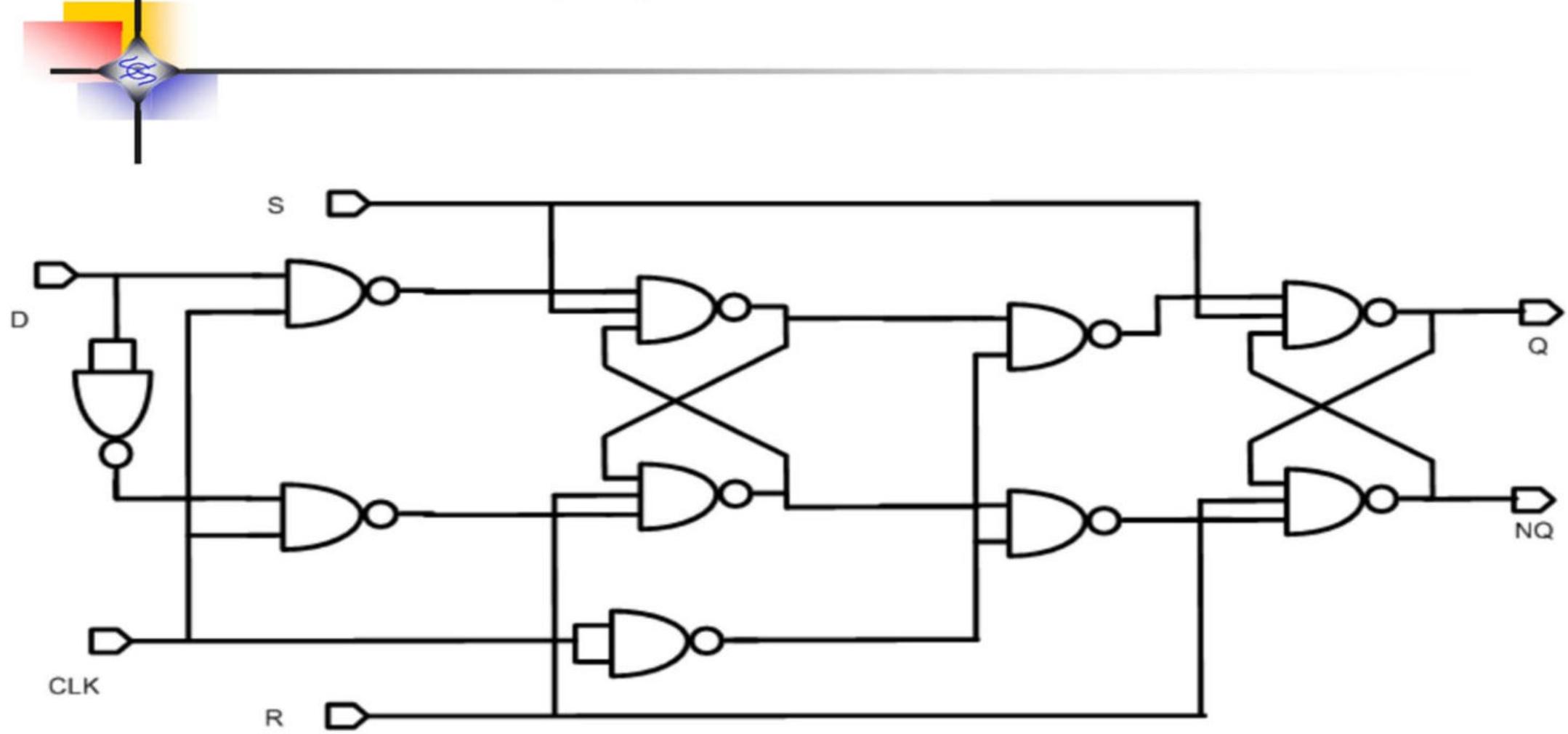
Bistabil D_v3

Se creeaza un cell view de tip schematic

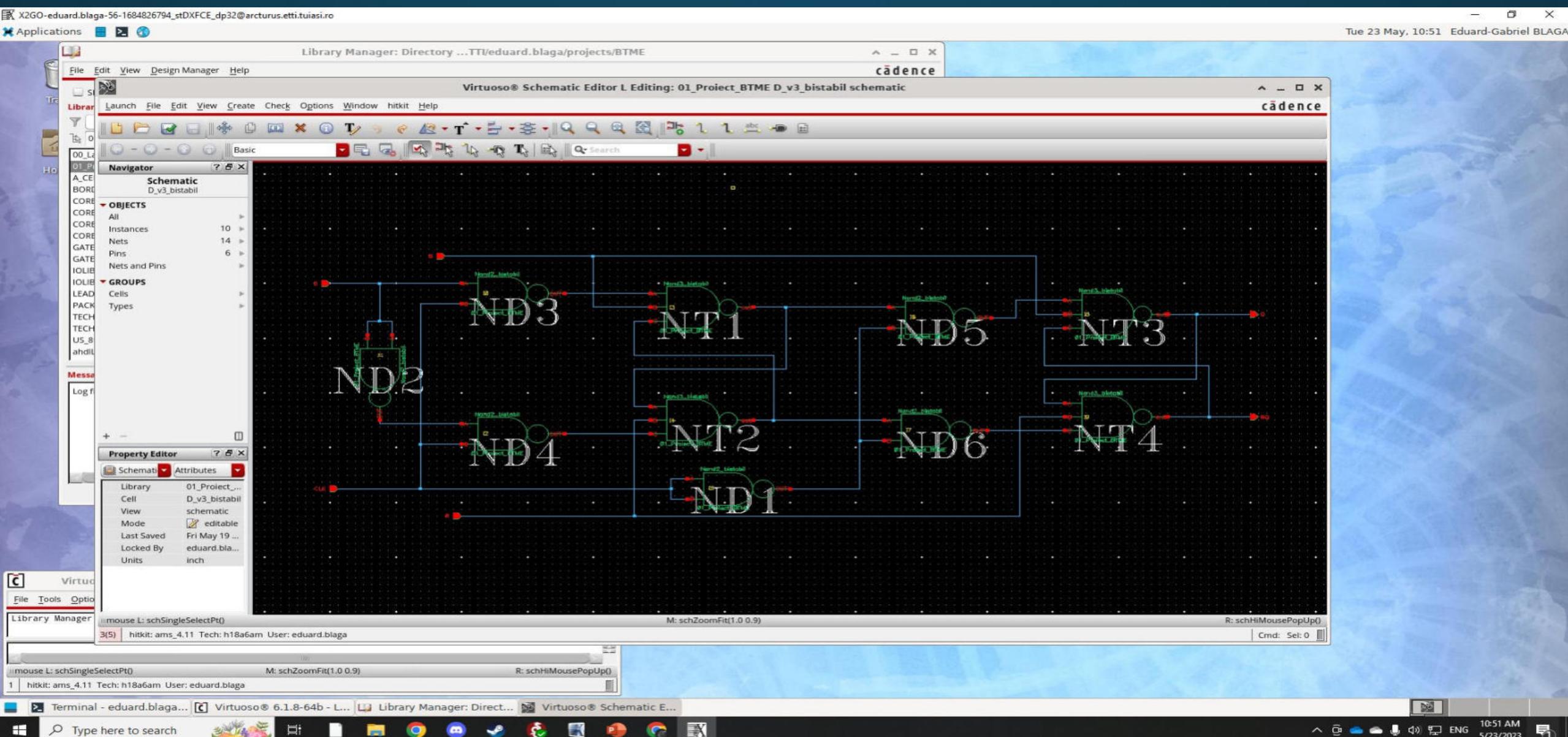


Bistabilul D_V3

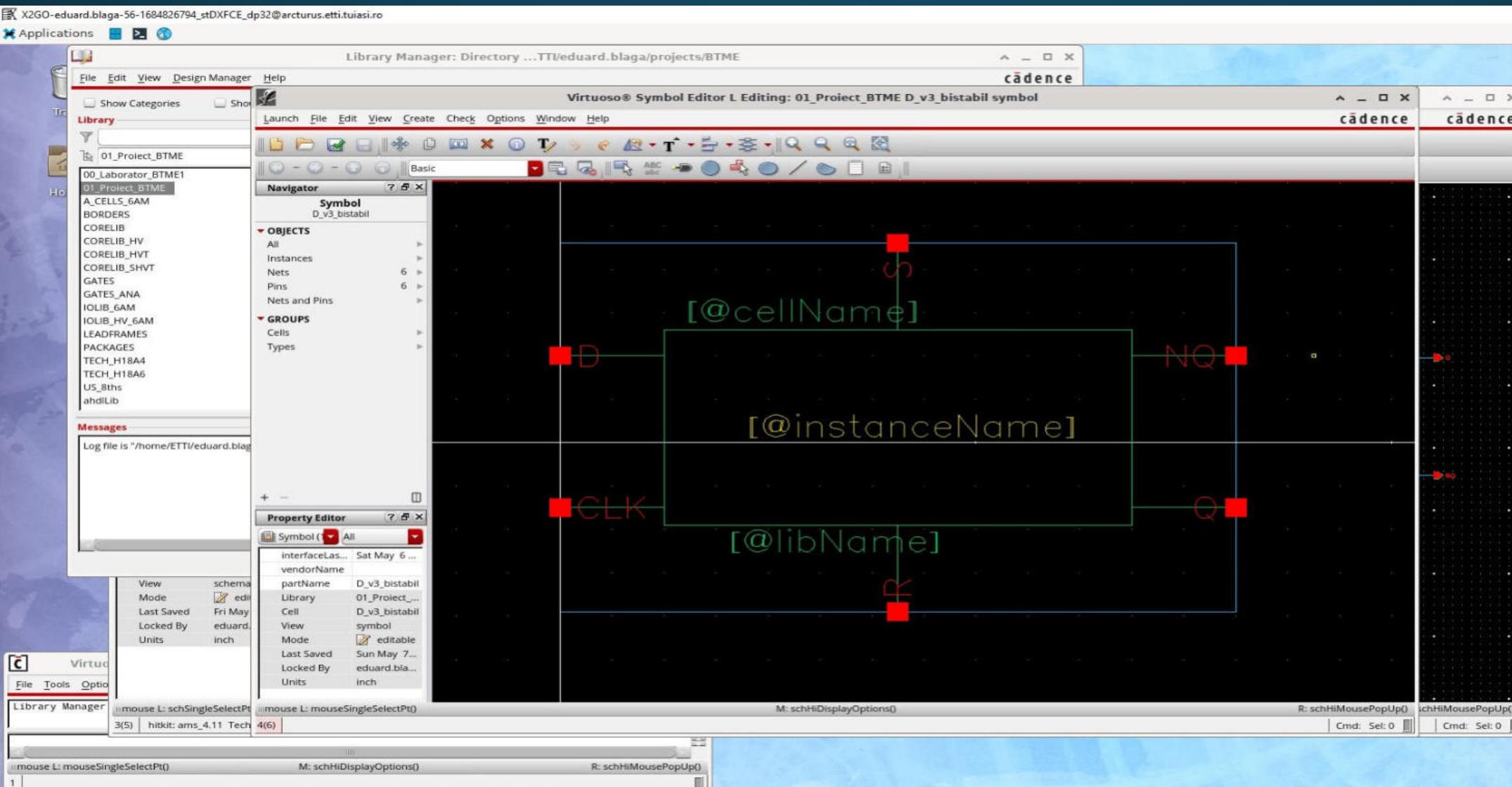
Bistabil de tip D_v3



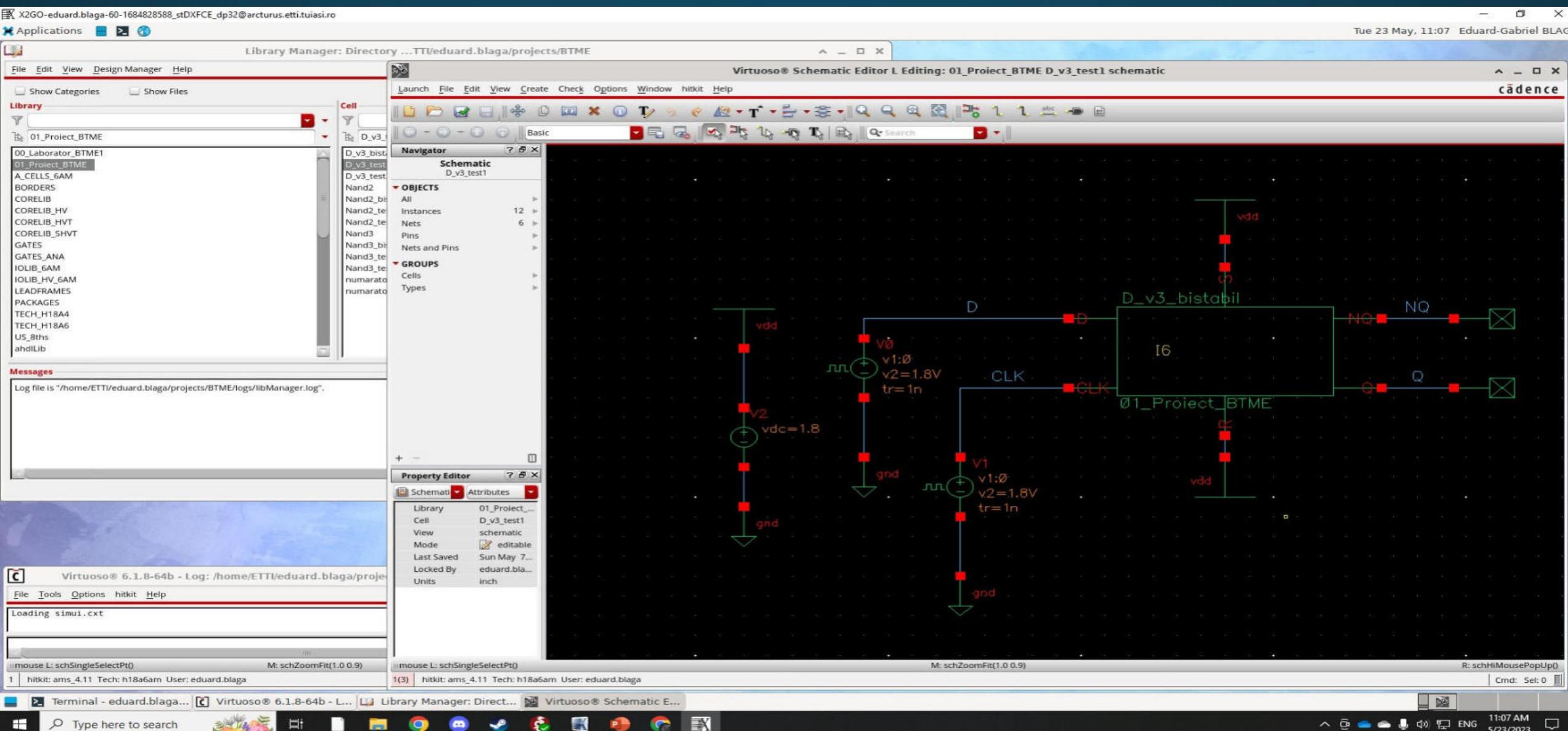
Se realizeaza schema bistabilului D_v3



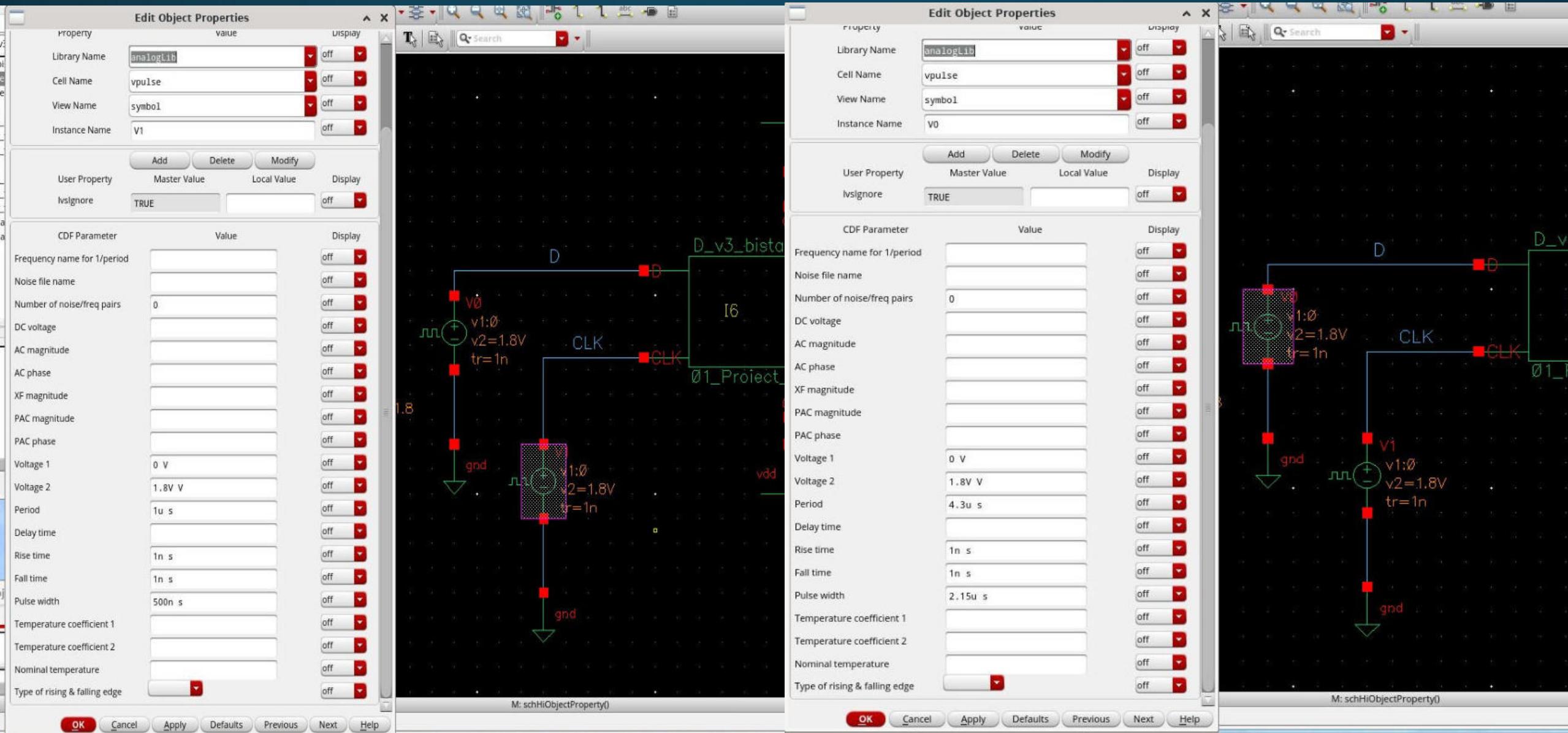
Intocmin simbolul bistabilului



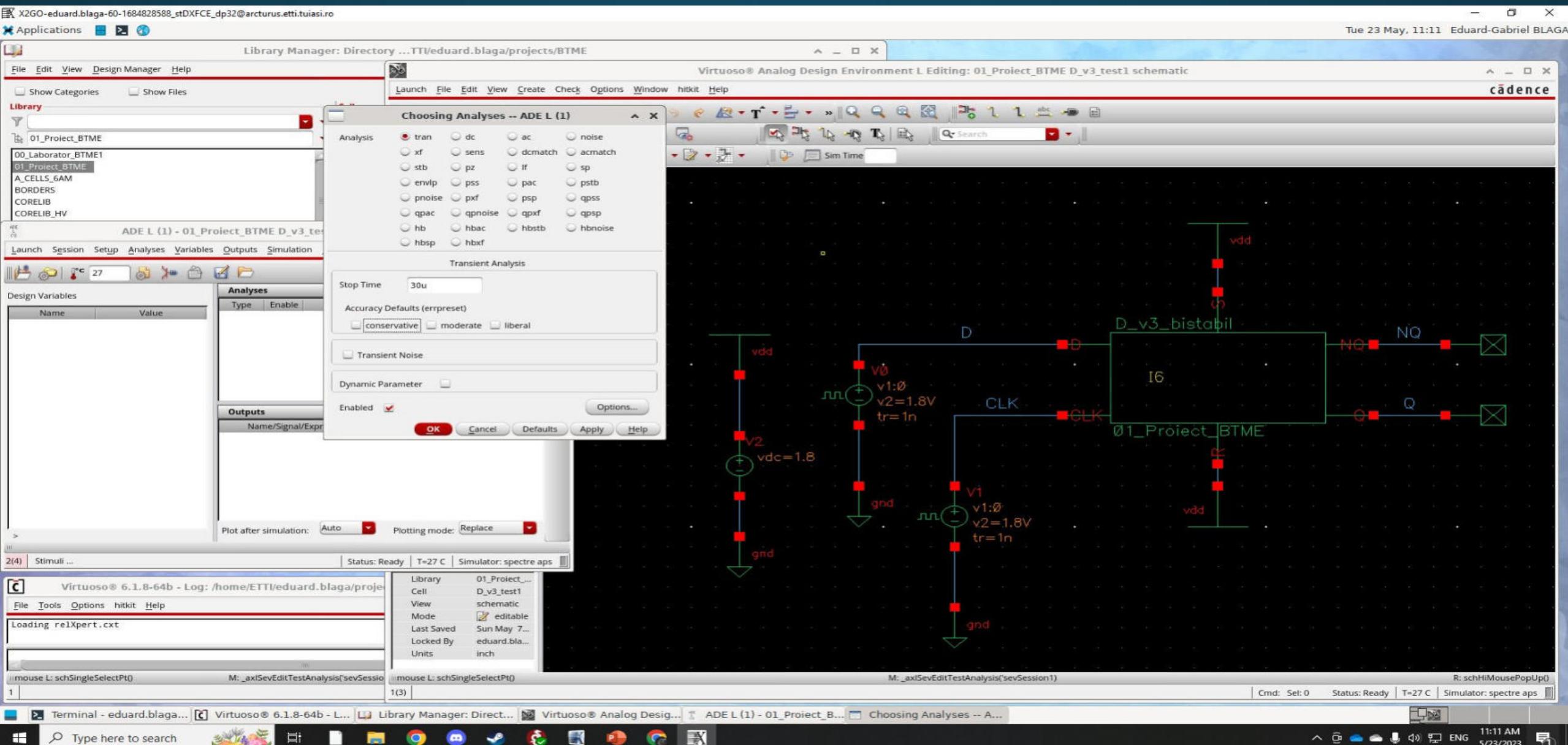
Construim o schema de test pentru a verifica functionarea bistabilului nostru



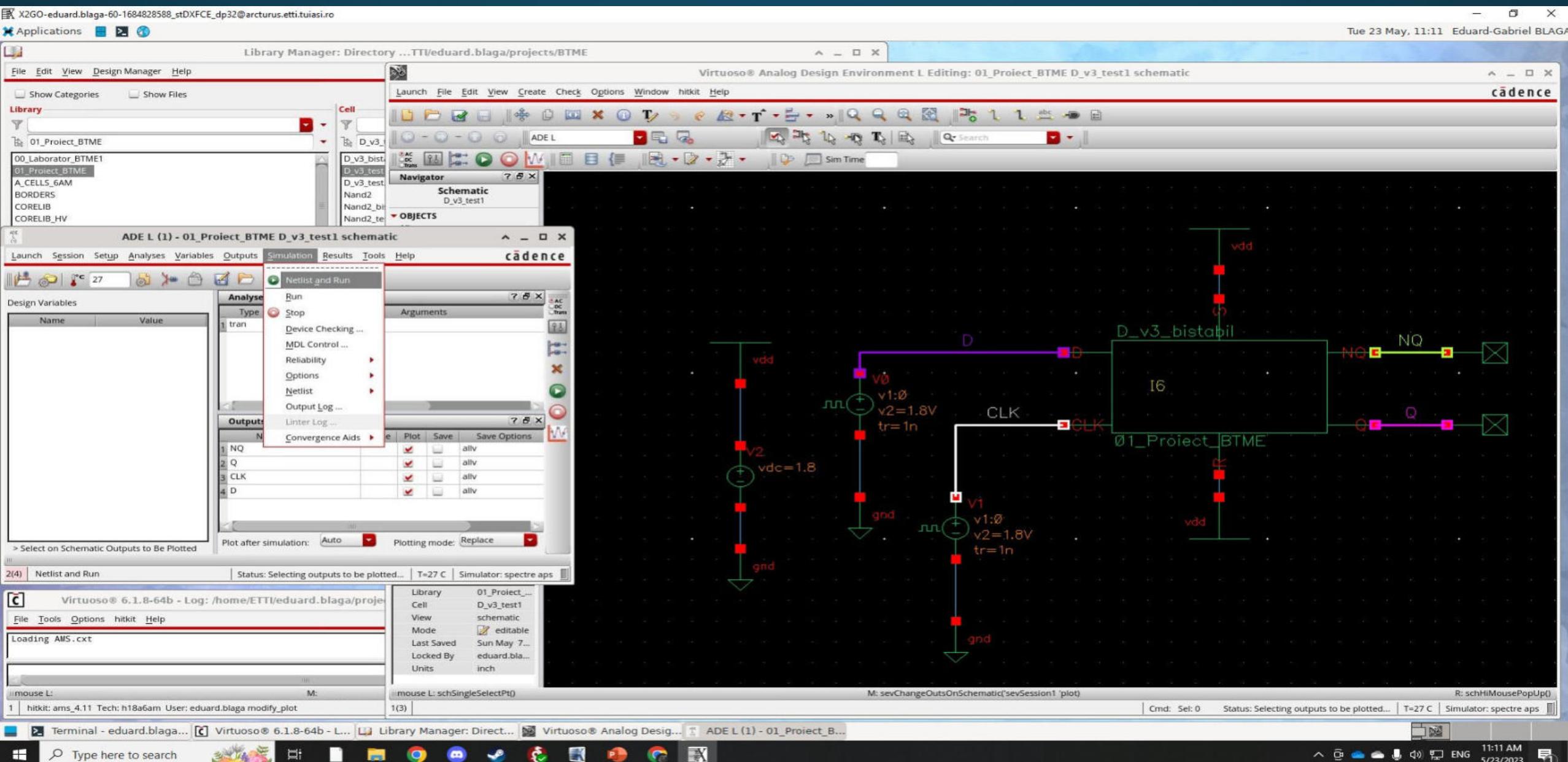
Setam parametrii surselor Vpulse



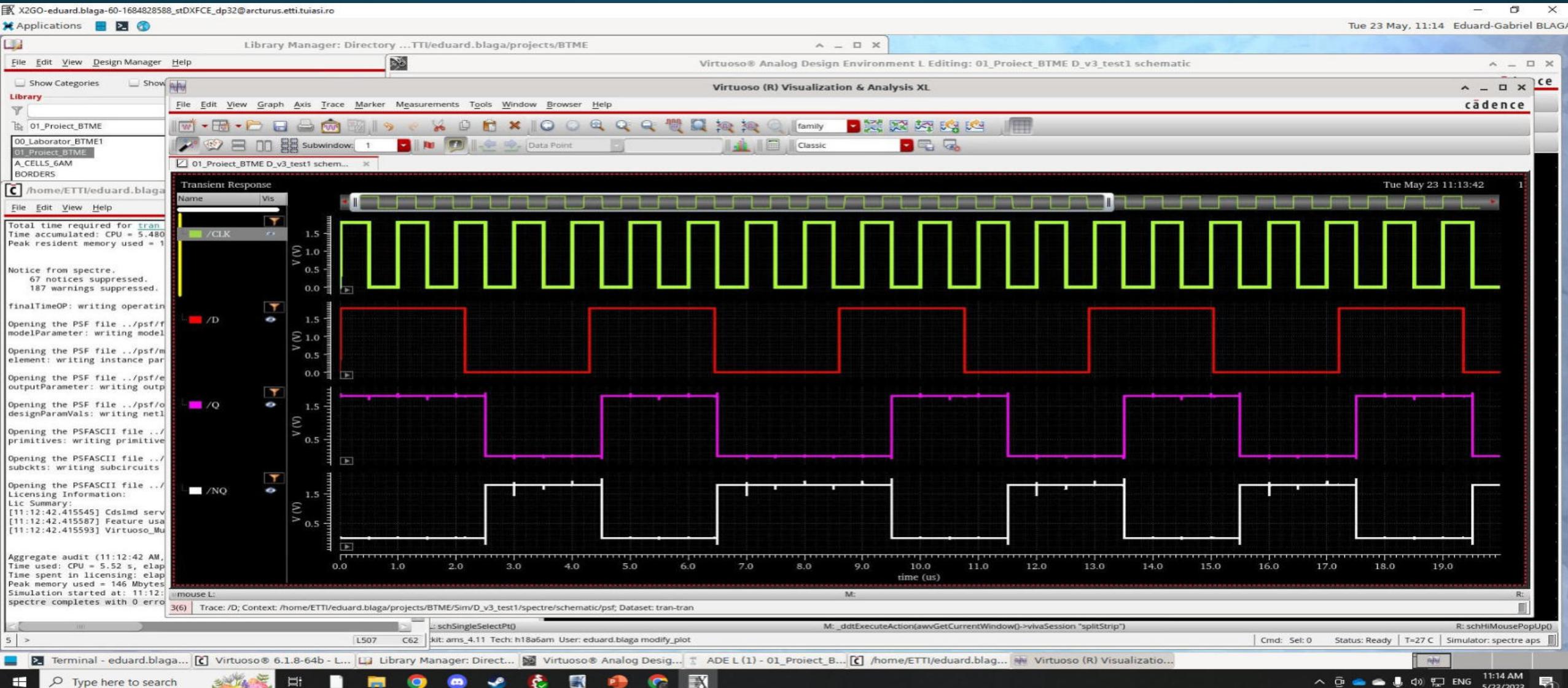
Efectuam o analiza tranzitorie



Efectuam o analiza tranzitorie



Observam rezultatele obtinute si vedem ca la fiecare front negativ de ceas iesirea Q corespunde cu intrarea D

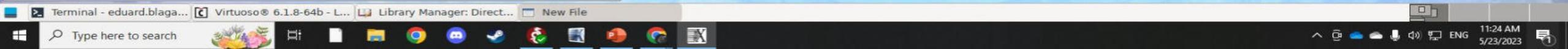
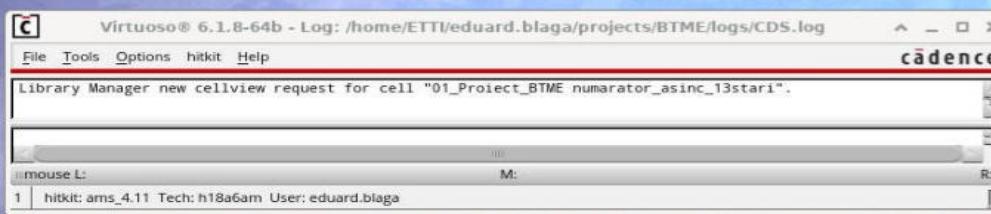
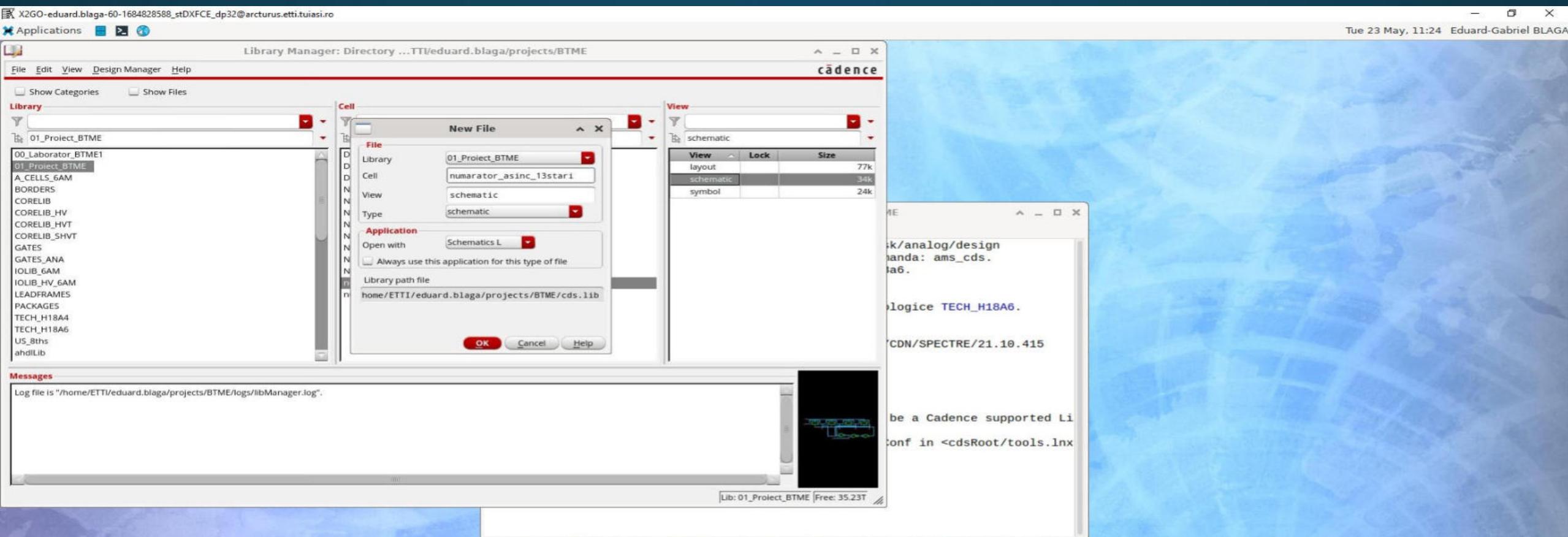


Refacem simularea dar conectam resetul la ground si vedem ca iesirea Q va sta doar in 0

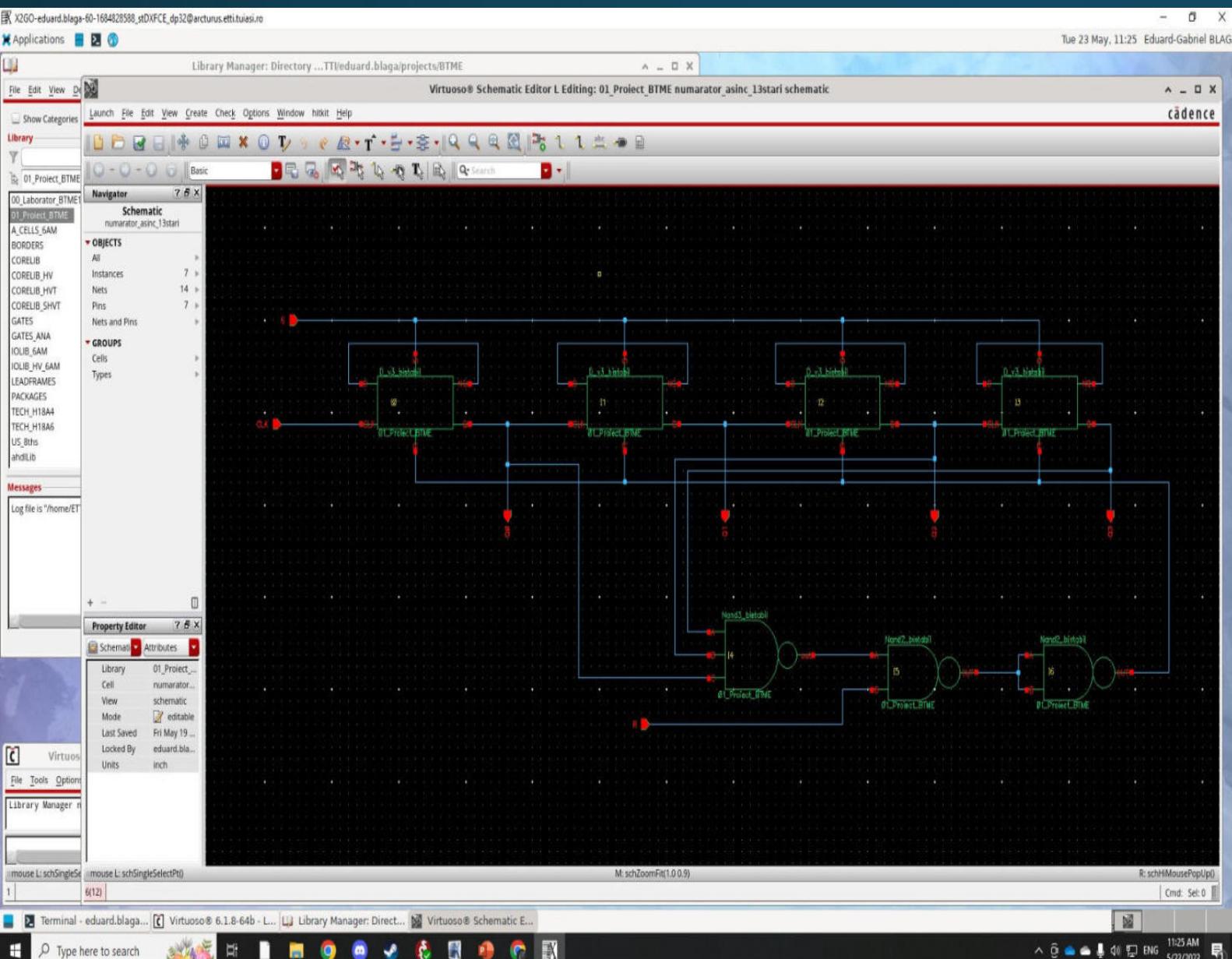


Numarator binar asincron cu 13 stari

Se creeaza un cell view de tip schematic pentru numarator

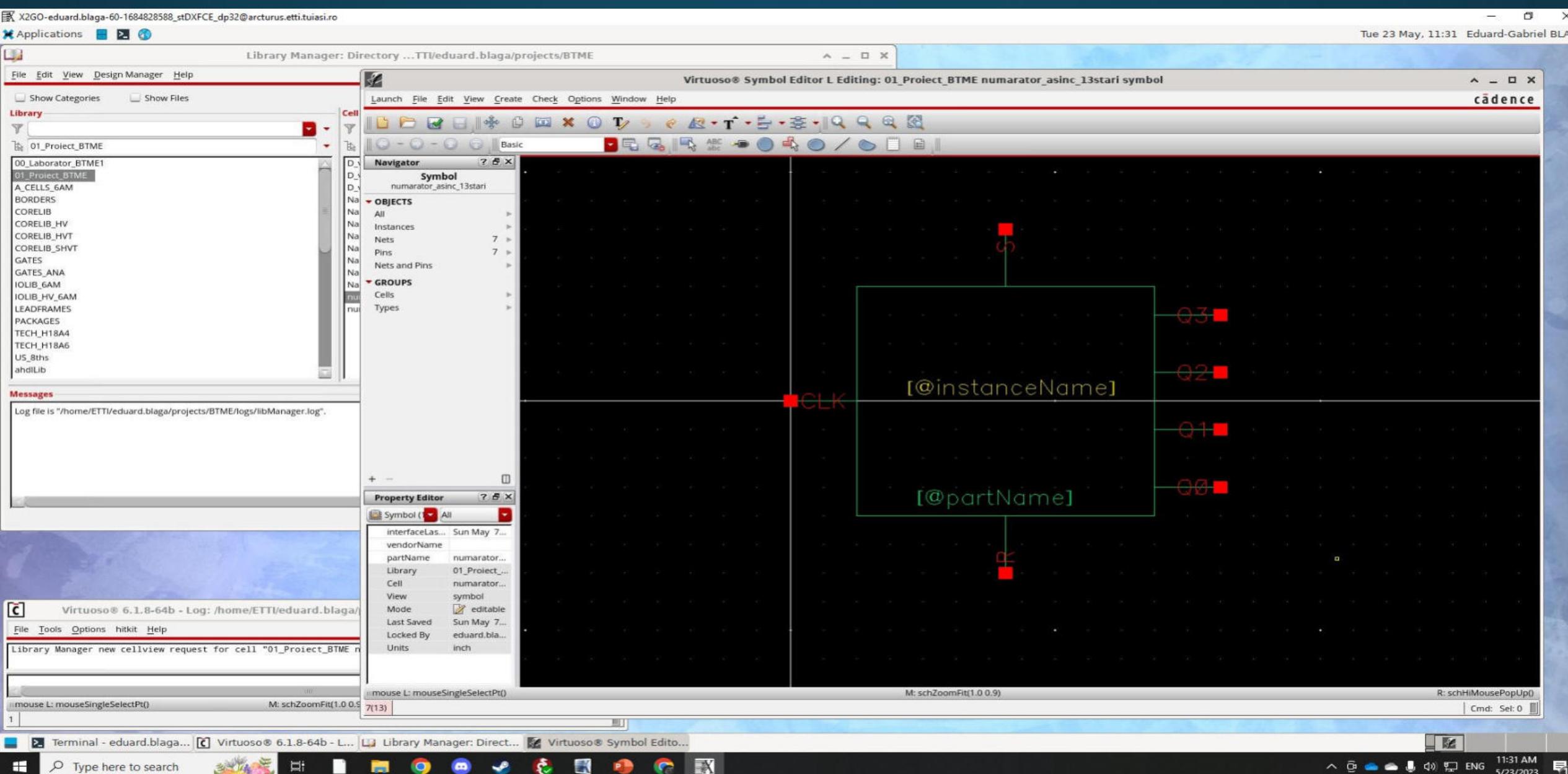


Se realizeaza schema numaratorului binar cu 13 stari

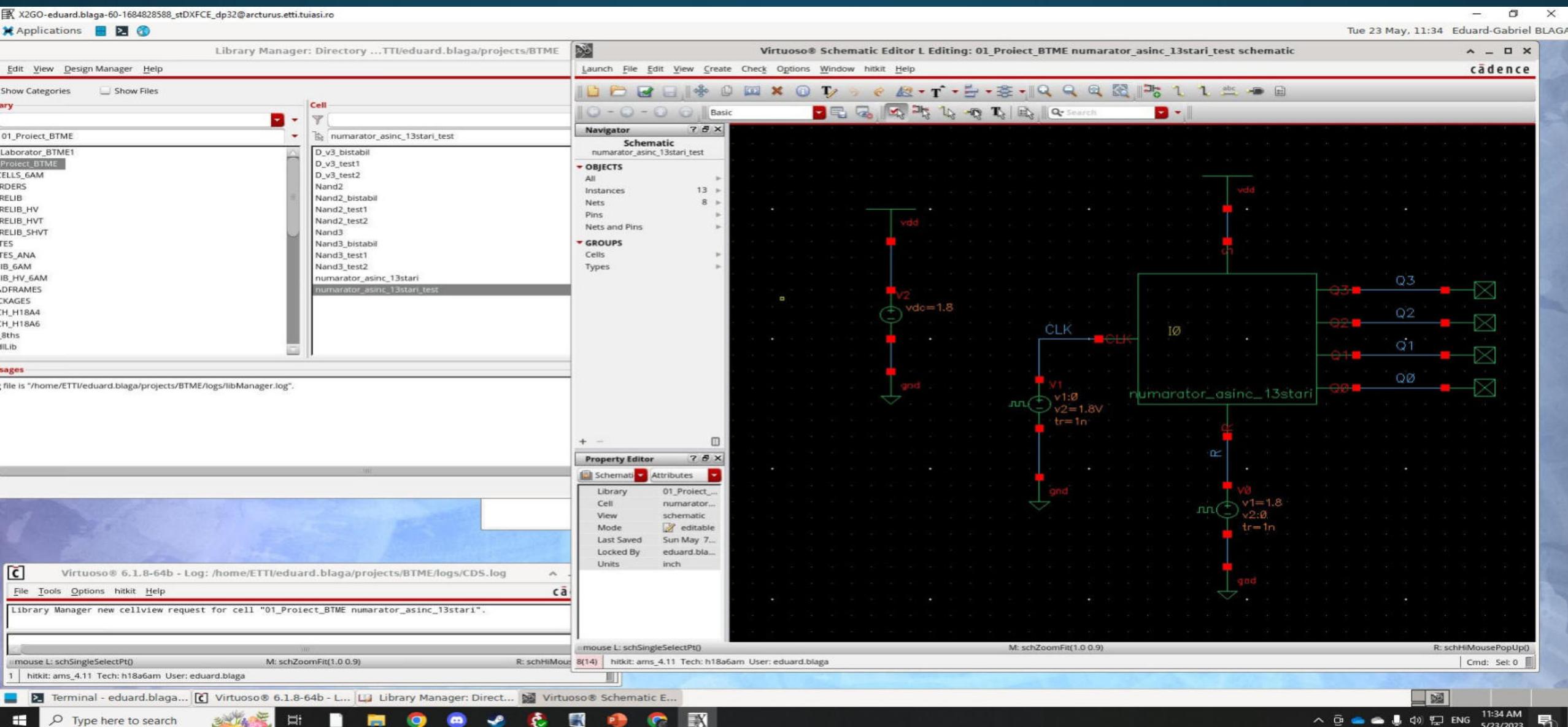


- Pentru a fi numarator cu 13 stari, acesta trebuie sa ajunga de la starea 0 pana la starea 12, iar la starea 13 sa se reseteze. Starea 13 in binar este 1101. Asta inseamna ca va trebui sa conectam o poarta Nand3 la iesirile care sunt 1 logic, mai exact Q3, Q2 si Q0. De asemenea, am adaugat un Reset extern ca sa putem reseta numaratorul oricand avem nevoie

Intocmin simbolul numaratorului



Construim o schema de test pentru a verifica functionarea numaratorului



Setam parametrii surselor Vpulse

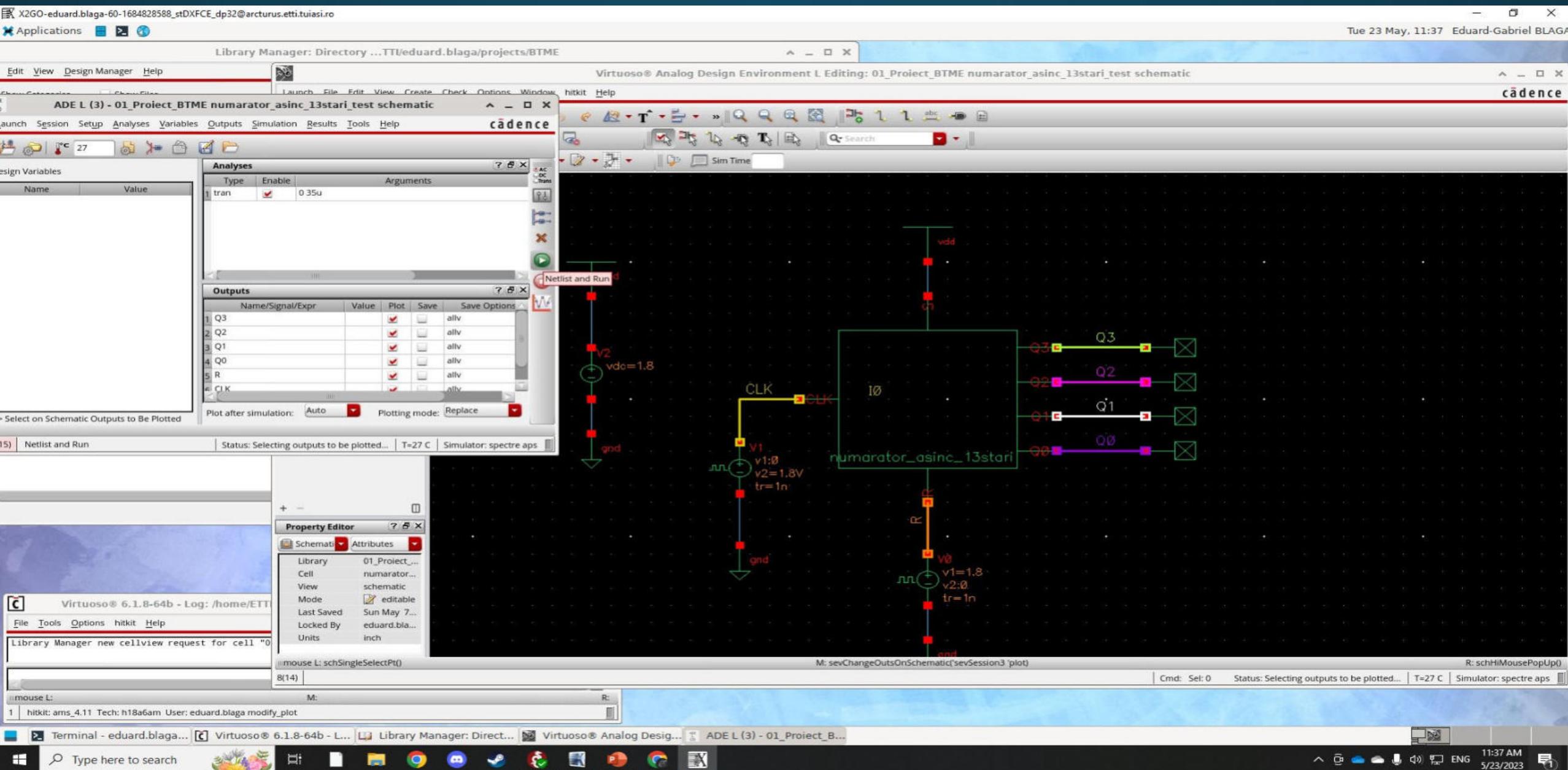
Edit Object Properties

Library Name	analogLib
Cell Name	vpulse
View Name	symbol
Instance Name	V1
User Property	Add Delete Modify
IvsIgnore	TRUE
CDF Parameter	Value
Frequency name for 1/period	
Noise file name	
Number of noise/freq pairs	0
DC voltage	
AC magnitude	
AC phase	
XF magnitude	
PAC magnitude	
PAC phase	
Voltage 1	0 V
Voltage 2	1.8V V
Period	1u s
Delay time	
Rise time	1n s
Fall time	1n s
Pulse width	500n s
Temperature coefficient 1	
Temperature coefficient 2	
Nominal temperature	
Type of rising & falling edge	

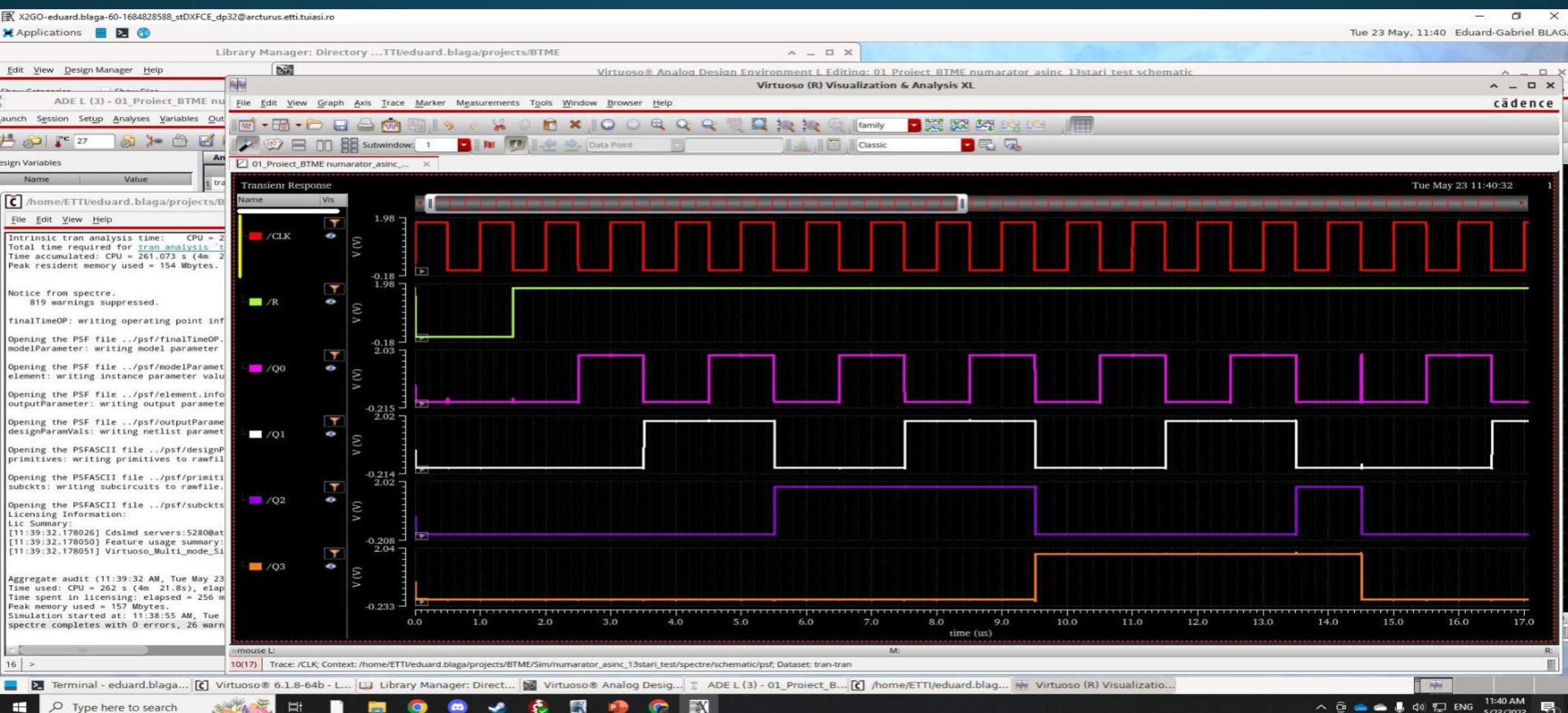
Edit Object Properties

Library Name	analogLib
Cell Name	vpulse
View Name	symbol
Instance Name	V0
User Property	Add Delete Modify
IvsIgnore	TRUE
CDF Parameter	Value
Frequency name for 1/period	
Noise file name	
Number of noise/freq pairs	0
DC voltage	
AC magnitude	
AC phase	
XF magnitude	
PAC magnitude	
PAC phase	
Voltage 1	1.8 V
Voltage 2	0 V
Period	1 s
Delay time	
Rise time	1n s
Fall time	1n s
Pulse width	1.5u s
Temperature coefficient 1	
Temperature coefficient 2	
Nominal temperature	
Type of rising & falling edge	

Efectuam o analiza tranzitorie

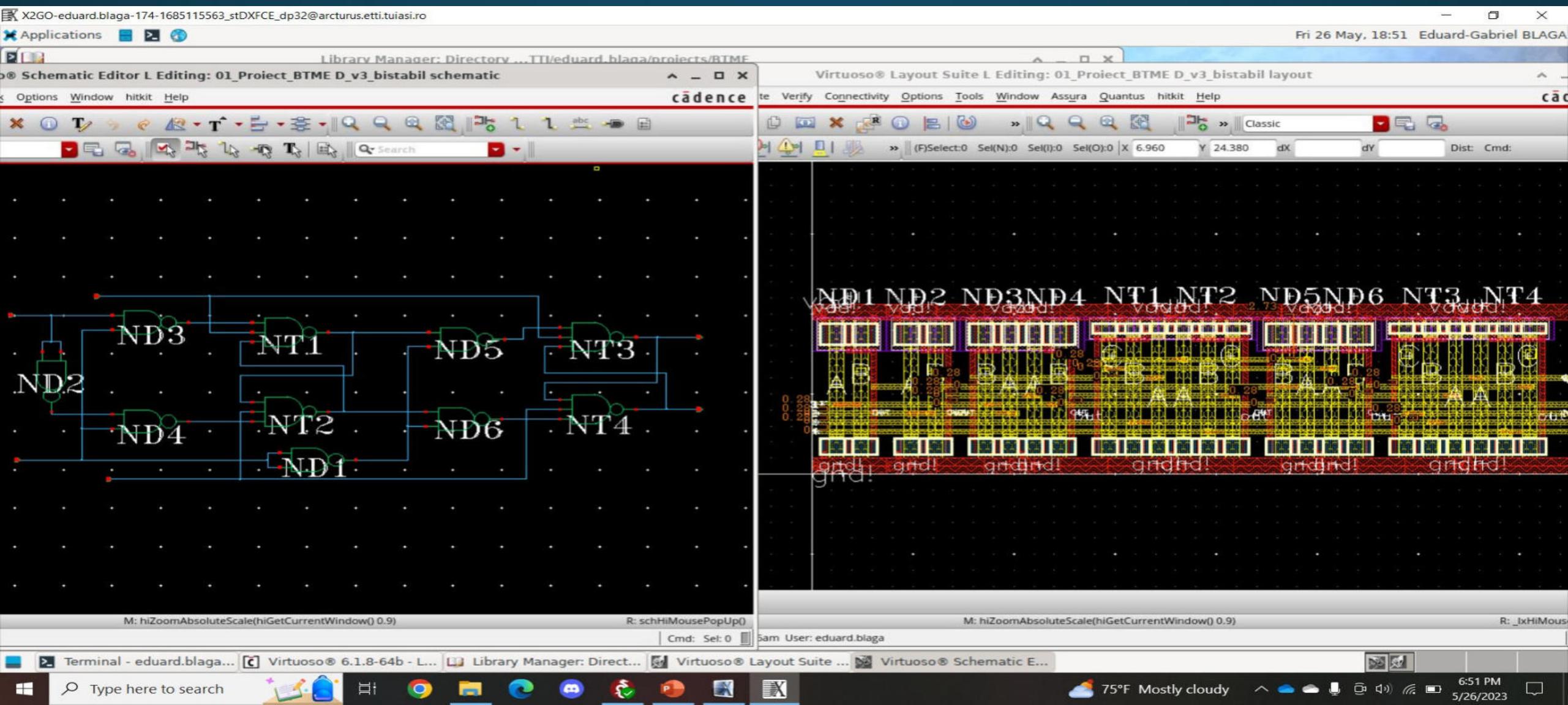


Numaratorul numara pana la starea 12, iar la starea 13 isi da Reset si o ia de la capat

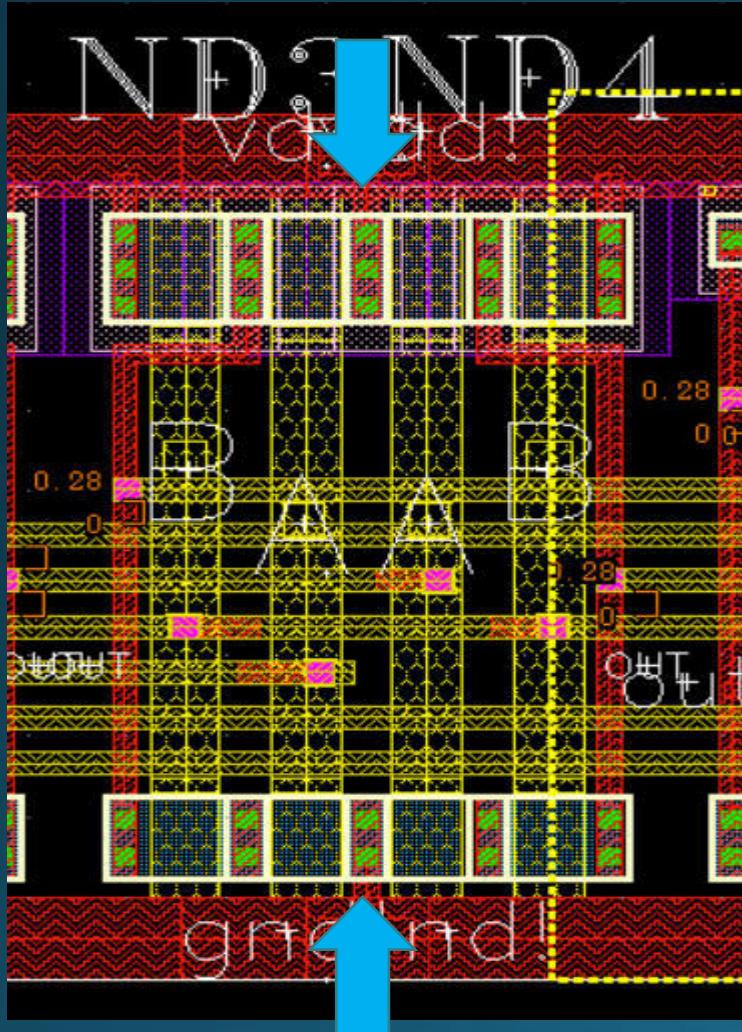


Layout Bistabil

Specific schematului, vom instantia toate portile de care avem nevoie si le vom lega intre ele la nivelul N-Well-urilor tranzistoarelor PMOS

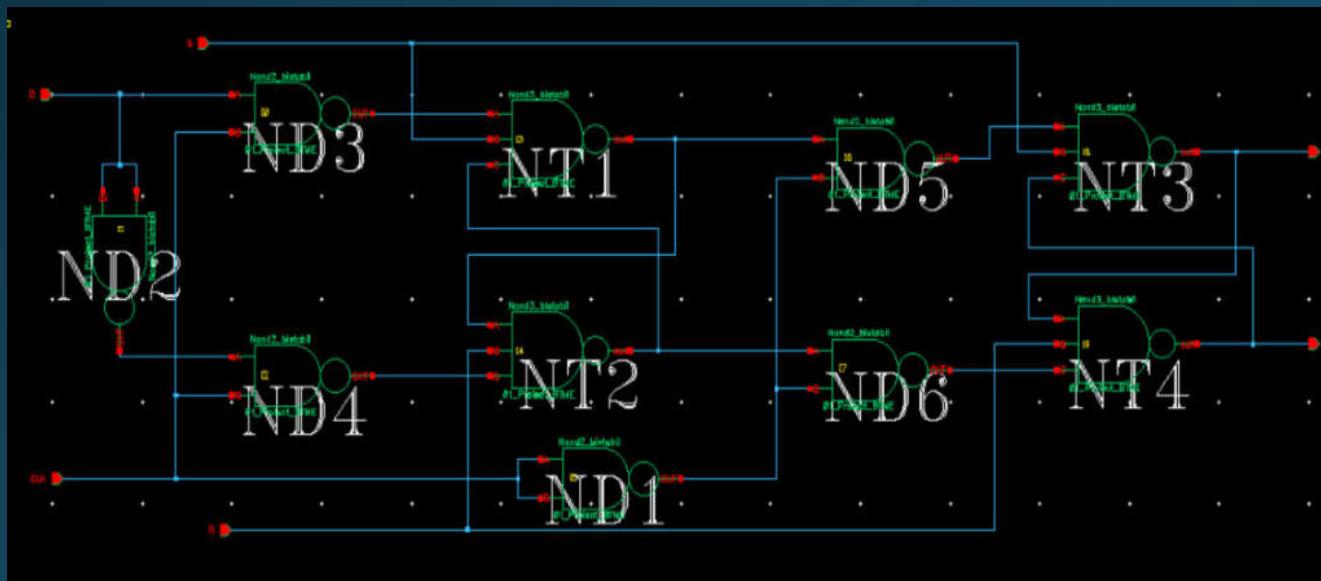
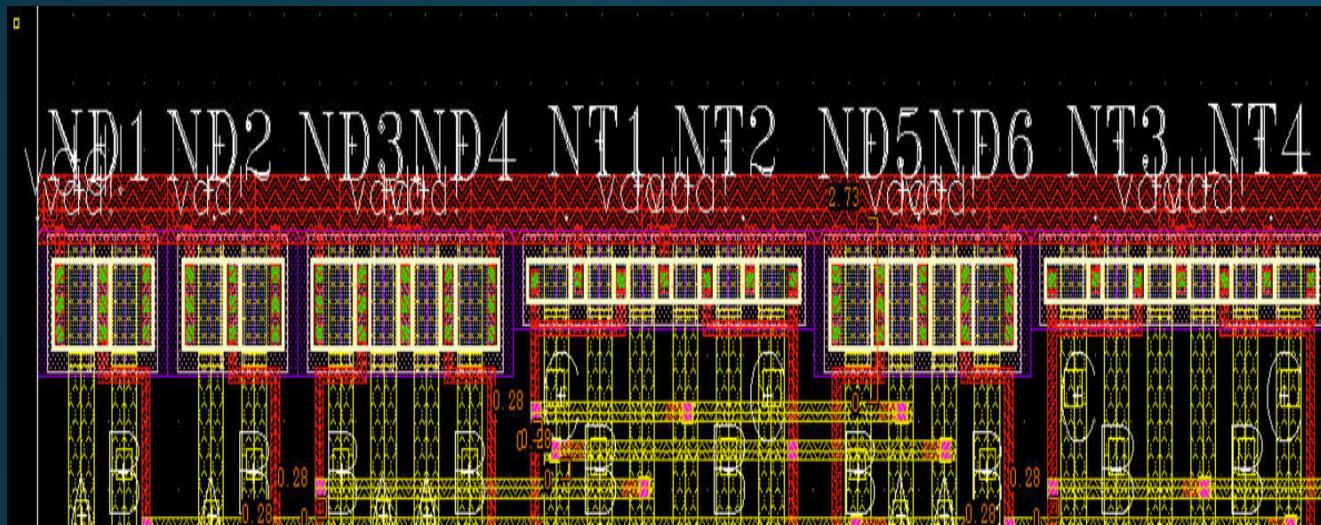


Mentiuni

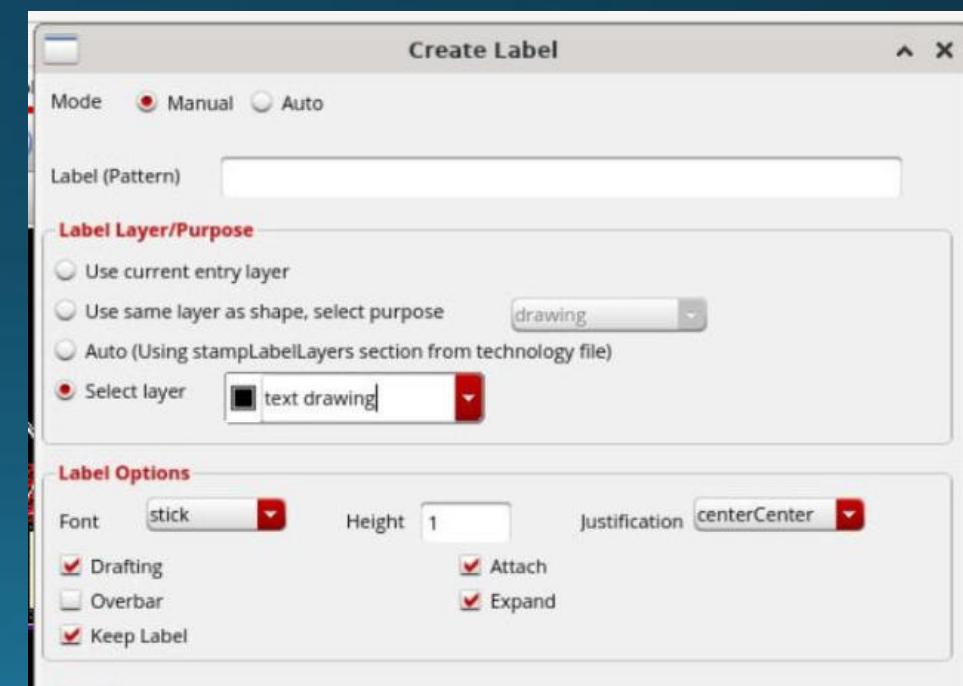


- Prima data este nevoie sa modificam portile create anterior prin stergerea contactelor de la vdd si ground. Putem grupa 2 porti nand intr-o schema ca cea prezenta pe slide printr-o tehnica numita **ABUTMENT**, adica se suprapun contactele tranzistoarelor spre vdd si gnd;
- Pasii pentru realizarea schemei : se instantiaza o poarta nand 2 sau 3 -> copy (si cu F3 selectam sideways) -> suprapunem contactele tranzistoarelor;
- Putem folosi aceasta metoda pentru a folosi cat mai putin spatiu de lucru.

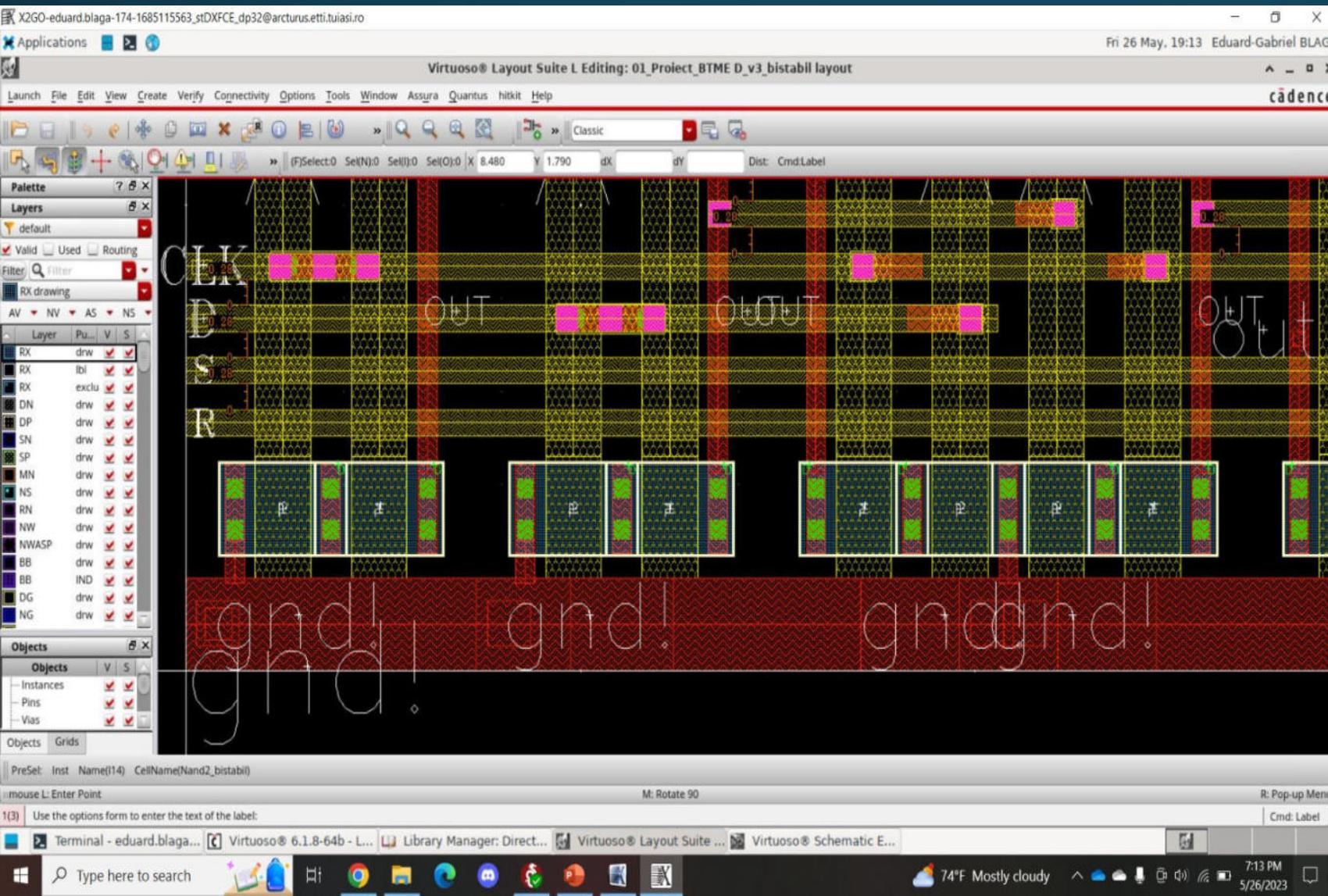
Denumim cu Create Label toate portile astfel incat sa corespunda cu schematicul



- Avem grija sa selectam un layer de tip text drawing

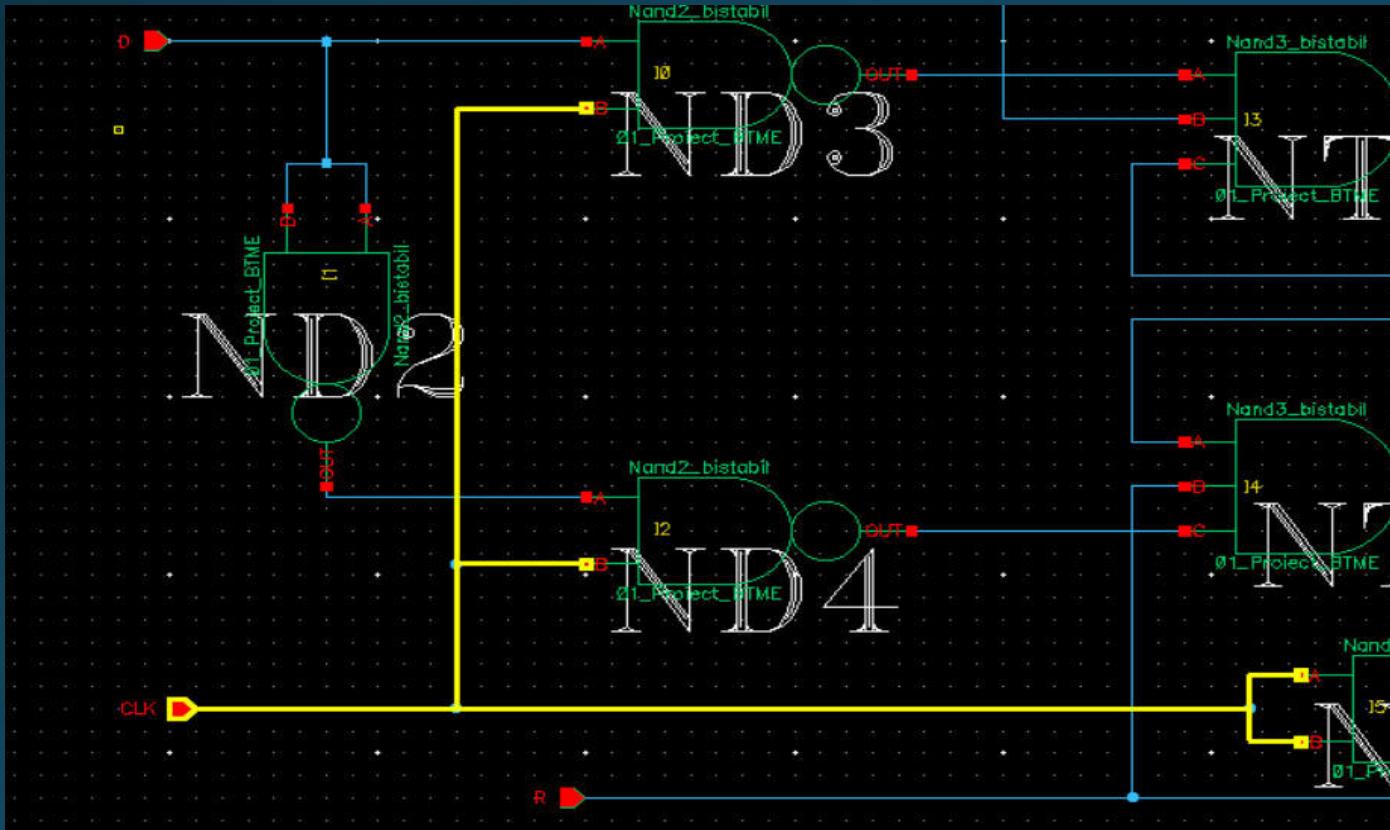
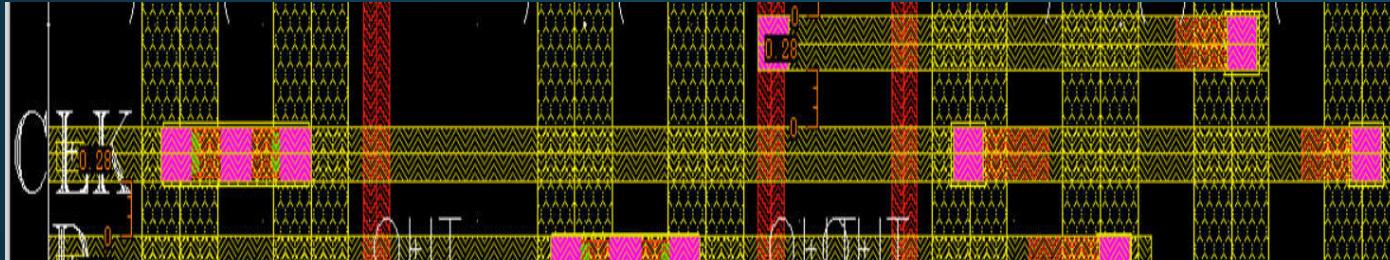


Intocmim cu layer de M2 traseele pentru Reset, Set, Clock si D, si tot cu layer de M2 vom crea si pinii specifici acestora



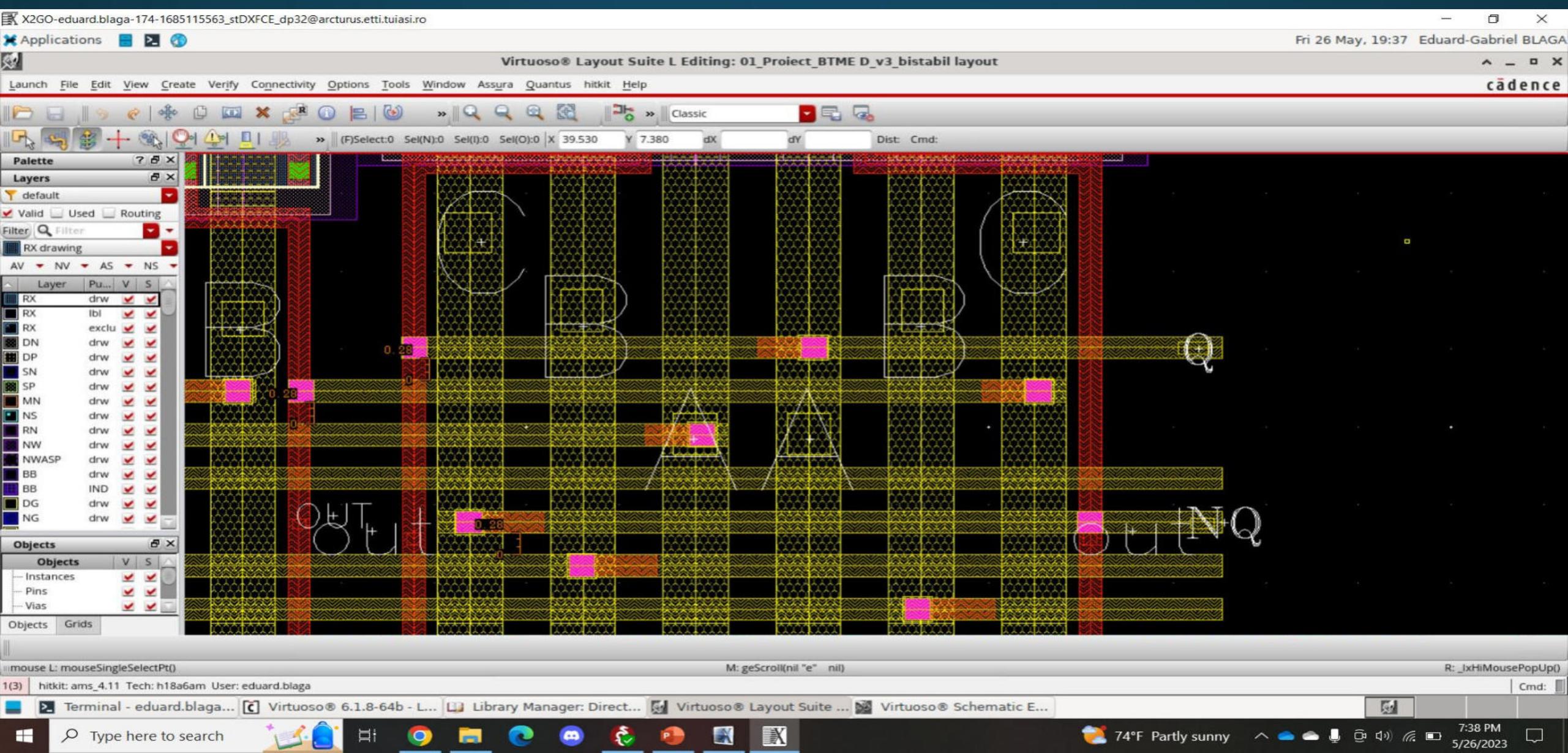
- Vom incepe trasarea la distanta de 0.28 fata de sursa tranzistoarelor NMOS de M1
- De asemenea, trebuie sa pastram aceasta distanta si intre layerele de M2
- In momentul in care vom realiza legaturile si observam ca lungimea traseului este mai mare decat ne trebuie, il putem scurta corespunzator, exceptie fac Setul, Resetul si Clockul

Copiem schematicul, iar cu fiecare legatura pe care o face in layout, se va sterge corespunzator legatura din schematic pentru a ne fi mai usor la urmarirea si realizarea corecta a legaturilor

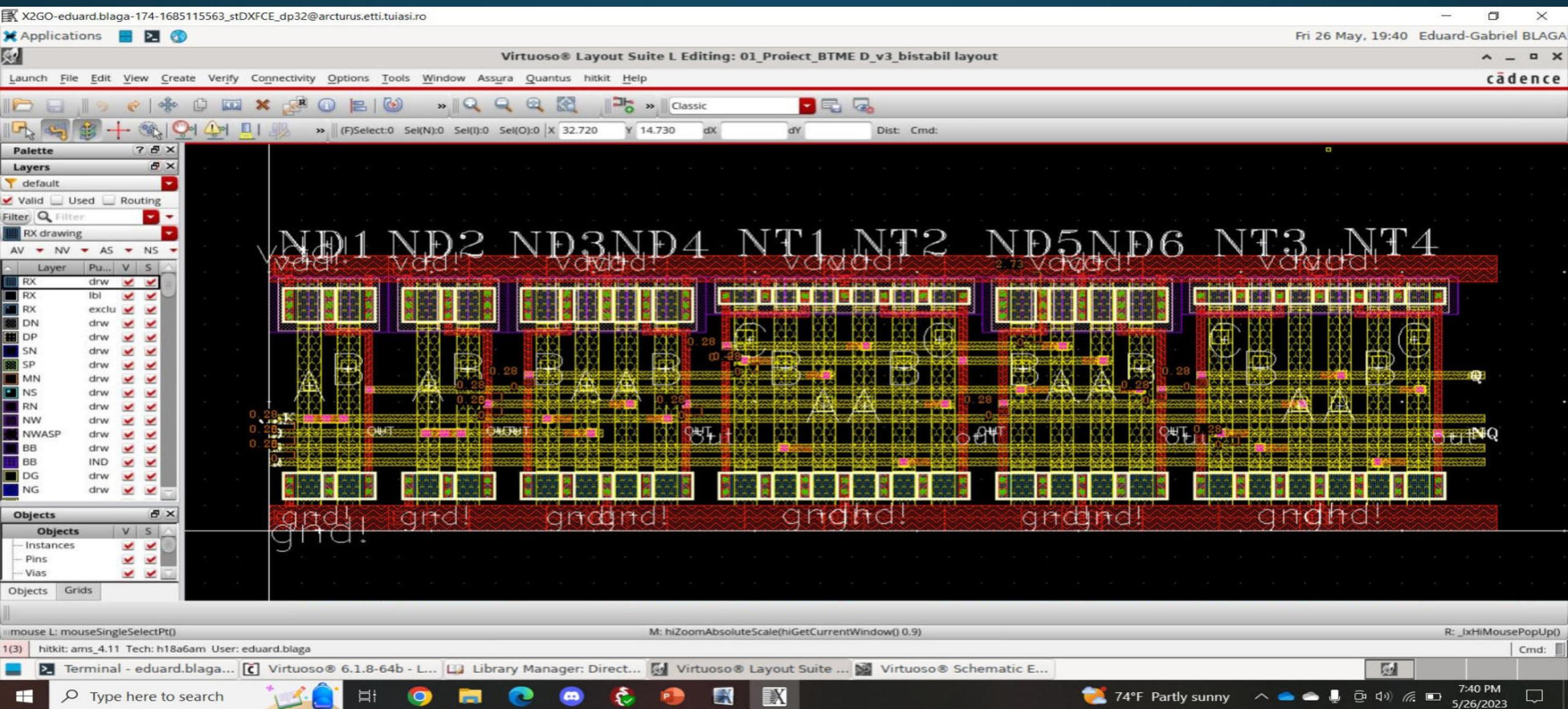


- Pentru realizarea legaturilor se folosesc VIA (tasta O)
- Pentru legaturi de PC-M2, folosim VIA de tip stack de la Pc la M2, si vom plasa un path de 0.28 de M1 conform regulii de plasare a contactelor
- Pentru legaturi de M1-M2, folosim Via de tip single

Realizam si traseele si pinii de iesire pentru Q si Q negat, cu specificatia ca iesirea NQ sa fie pe acelasi rand cu intrarea D (ne va ajuta ulterior la numarator)



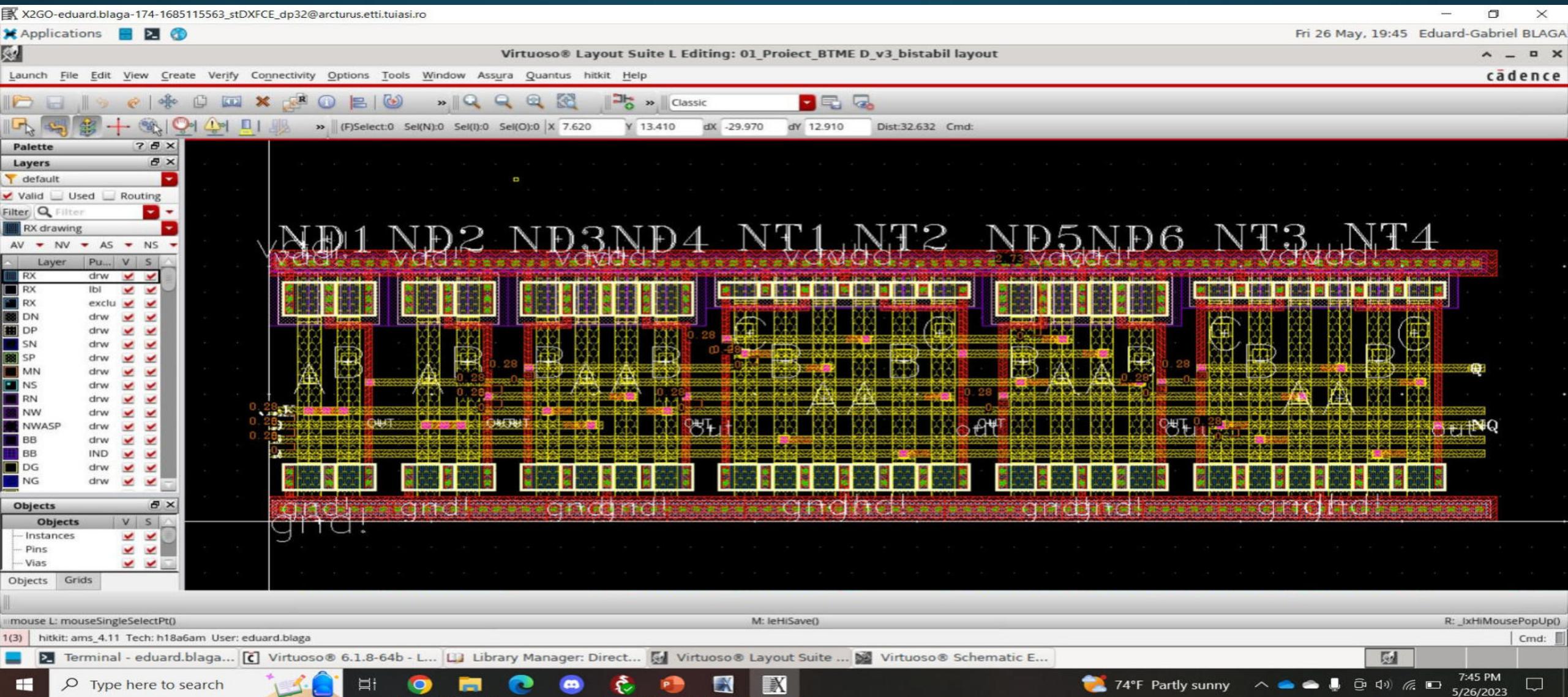
Continuam procesul pana cand parcurgem tot schematicul si nu ne mai raman legaturi de facut



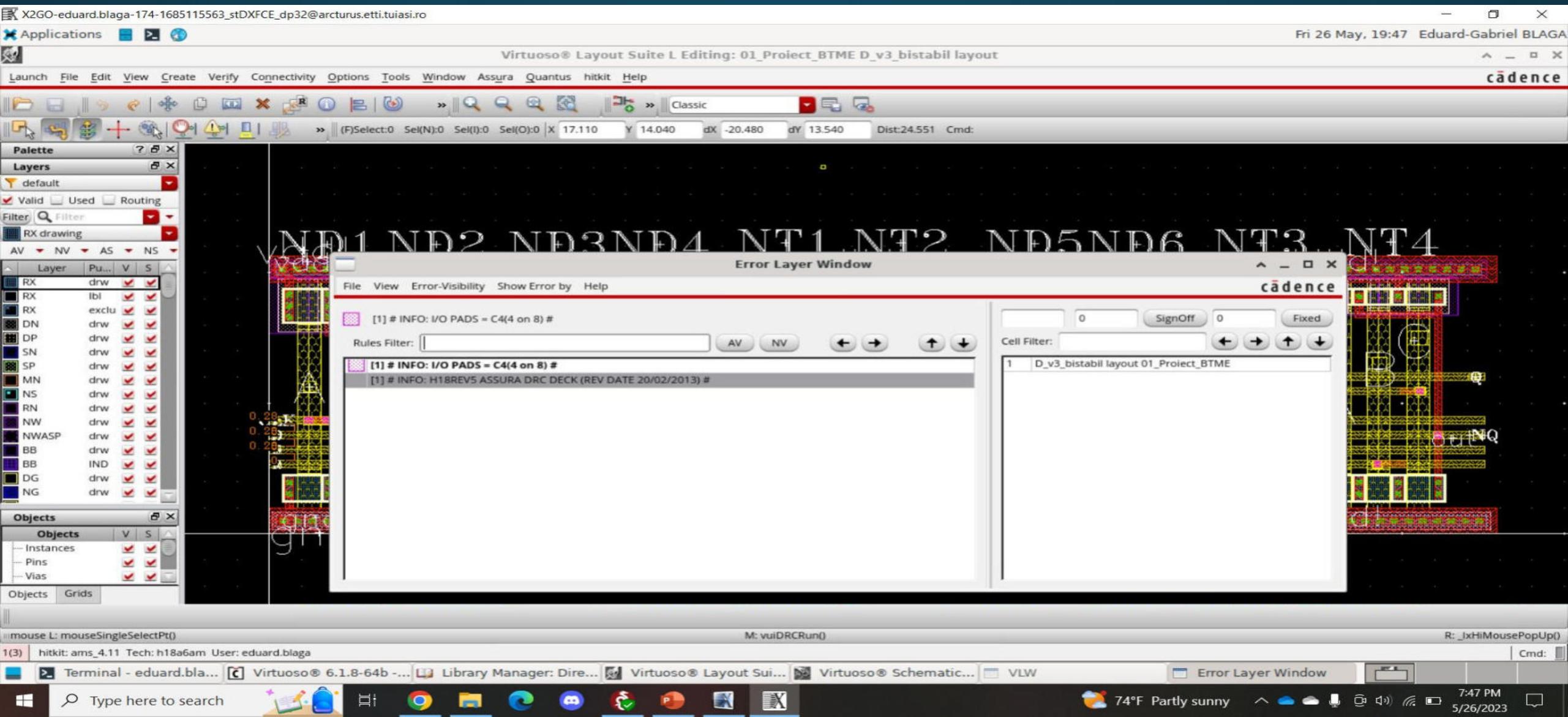
Mentiuni

- Dupa terminarea bistabilului, trebuie sa facem astfel incat sa acoperim o arie minima de folosinta
- Vom calula de la cea mai de top legatura facuta cu M2 pana la iesirea M1 a portii Nand2, si vom scadea 0.28
- Intram in layout-ul portilor Nand2 si Nand3 si cu Stratch micsoram poarta cu valoarea rezultata in urma scaderii. Astfel vom obtine aria minima a bistabilului

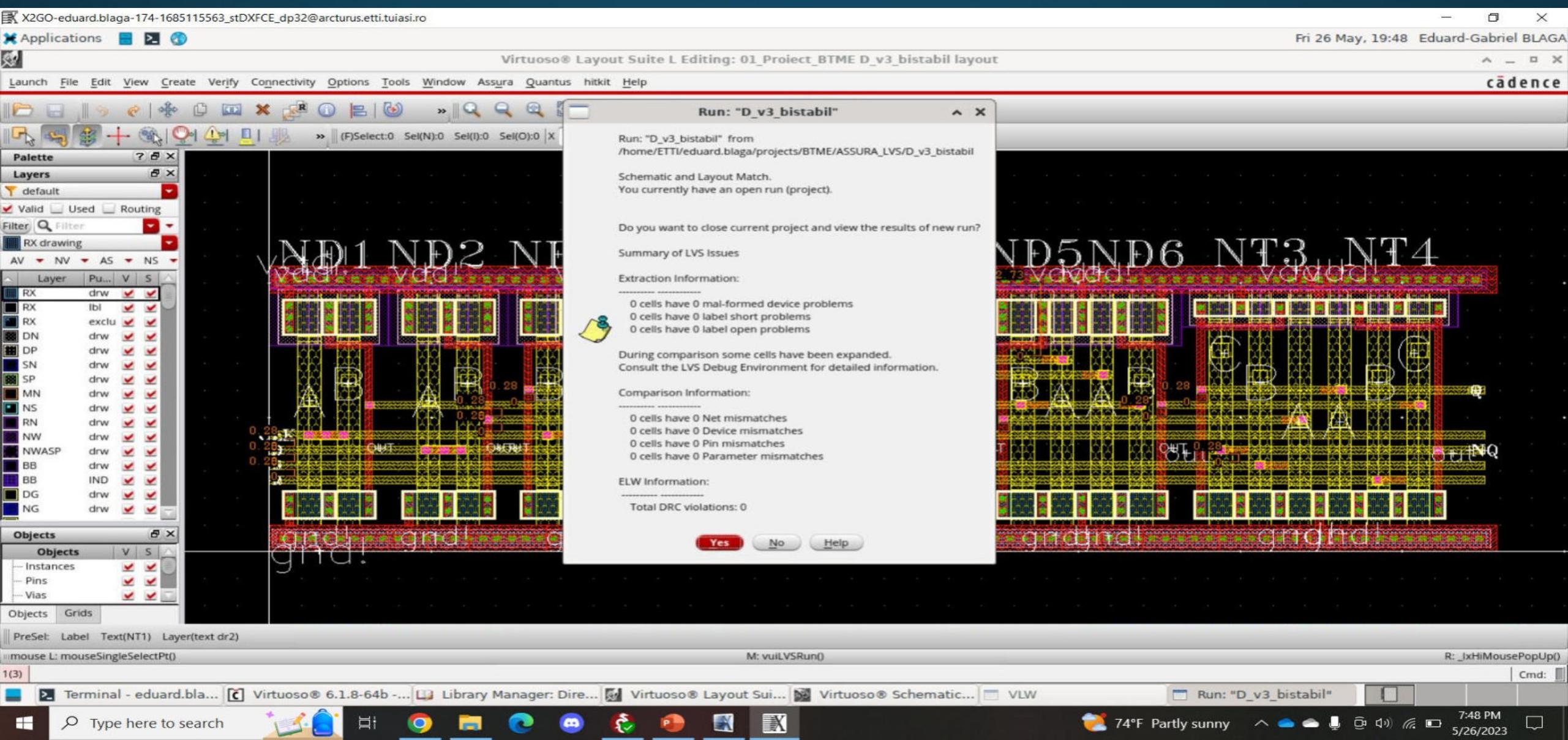
Plasam MultiPart Path pentru liniile de vdd si gnd si
pinii aferenti de tip InputOutput cu M1



Realizam analiza DRC

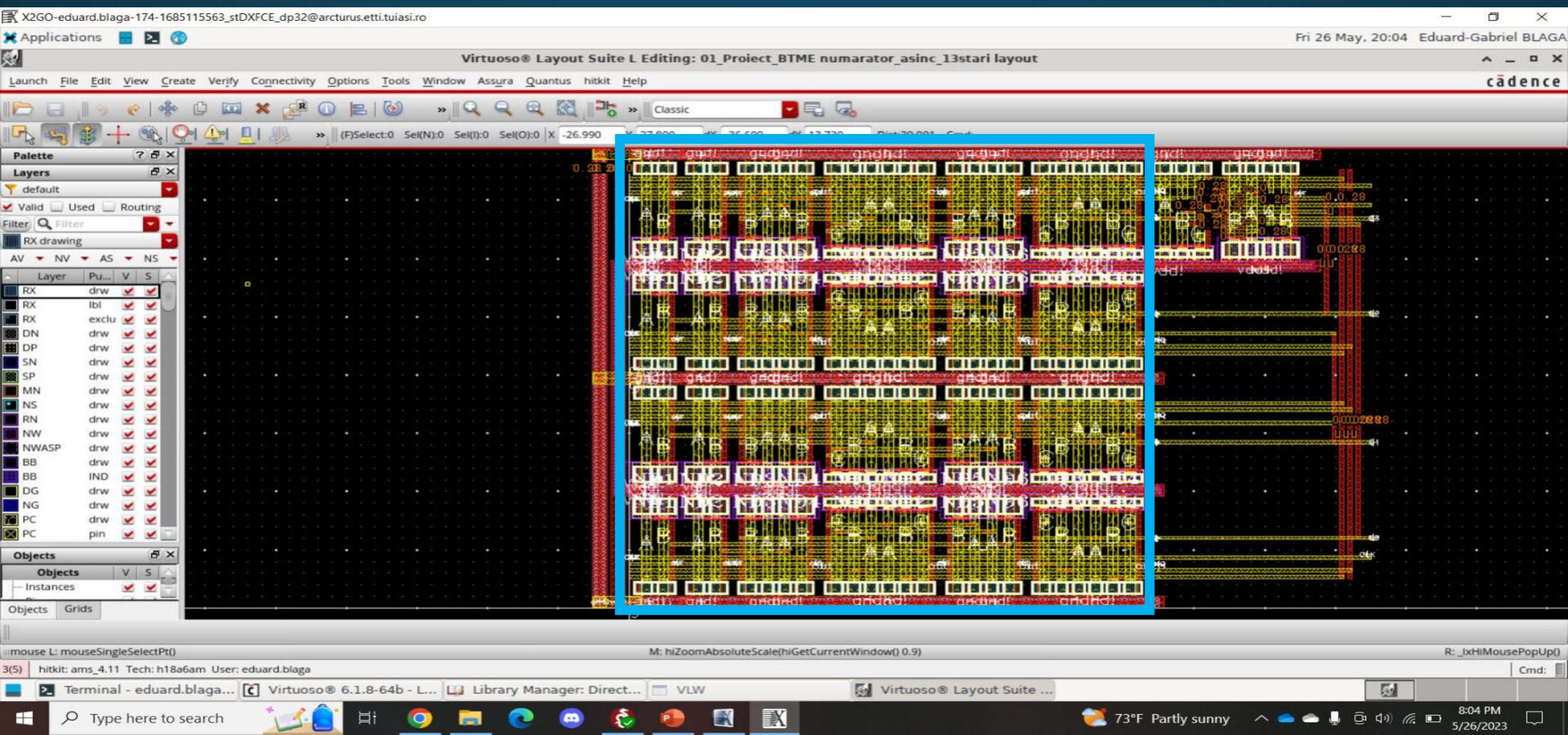


Realizam analiza LVS

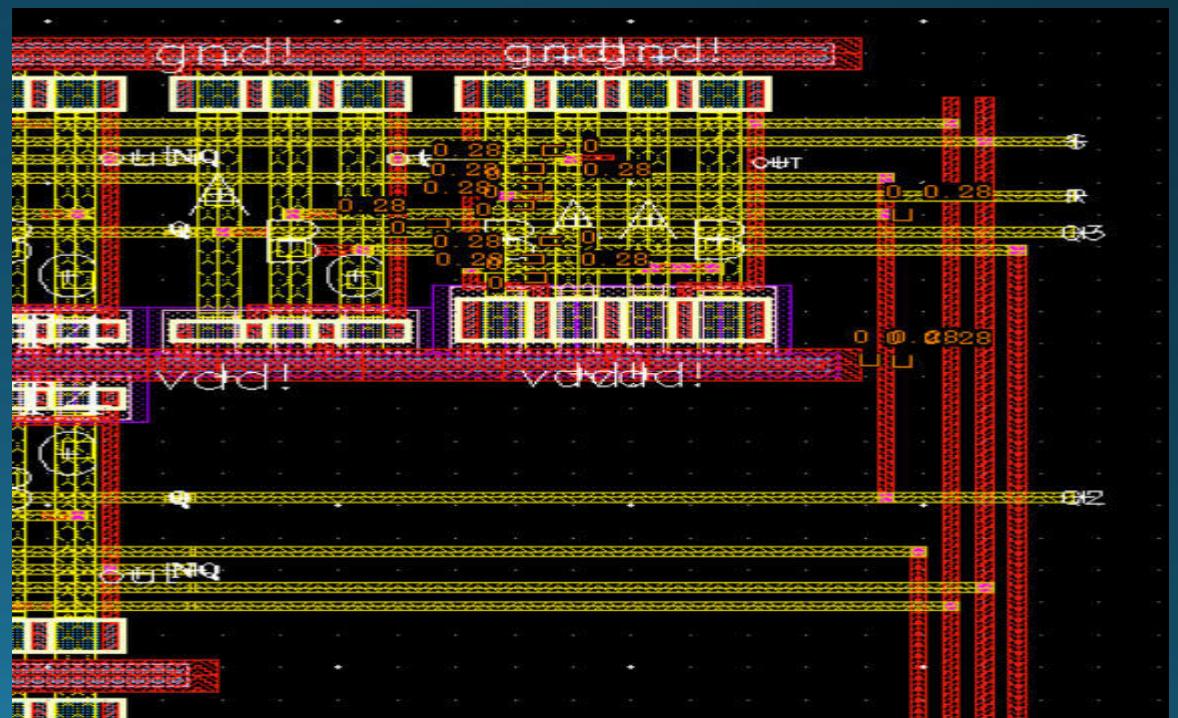
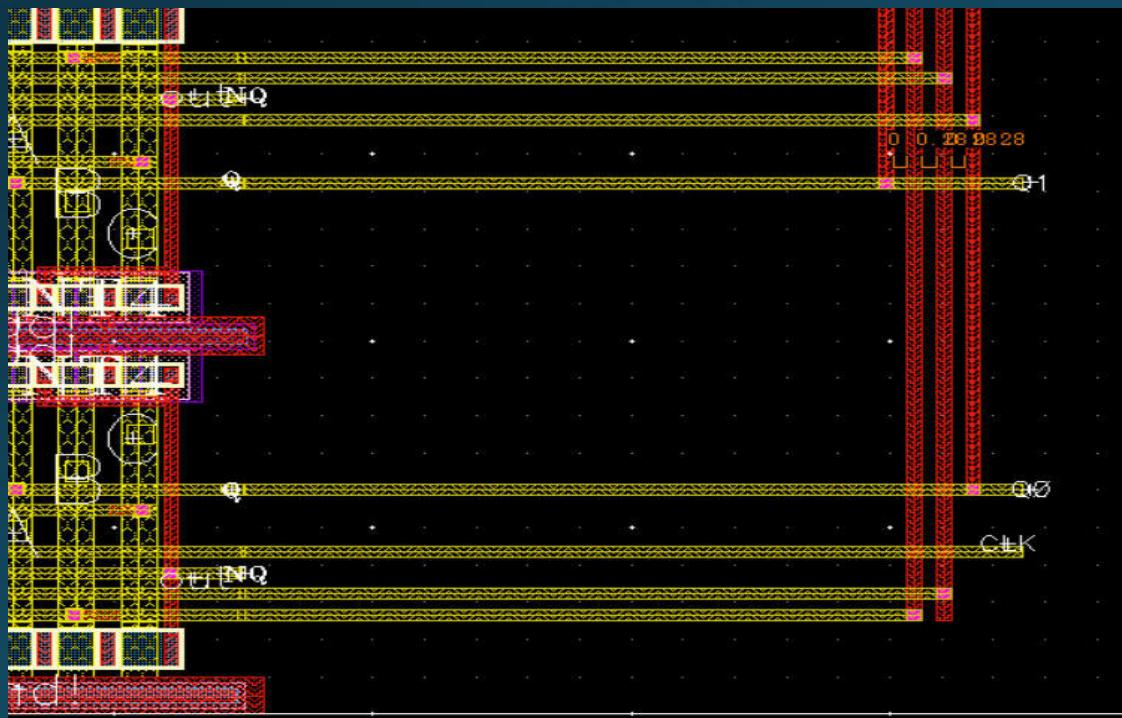
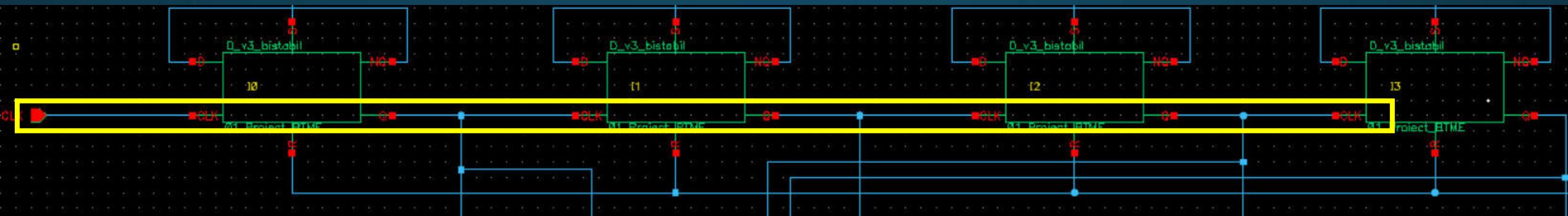


Layout Numarator

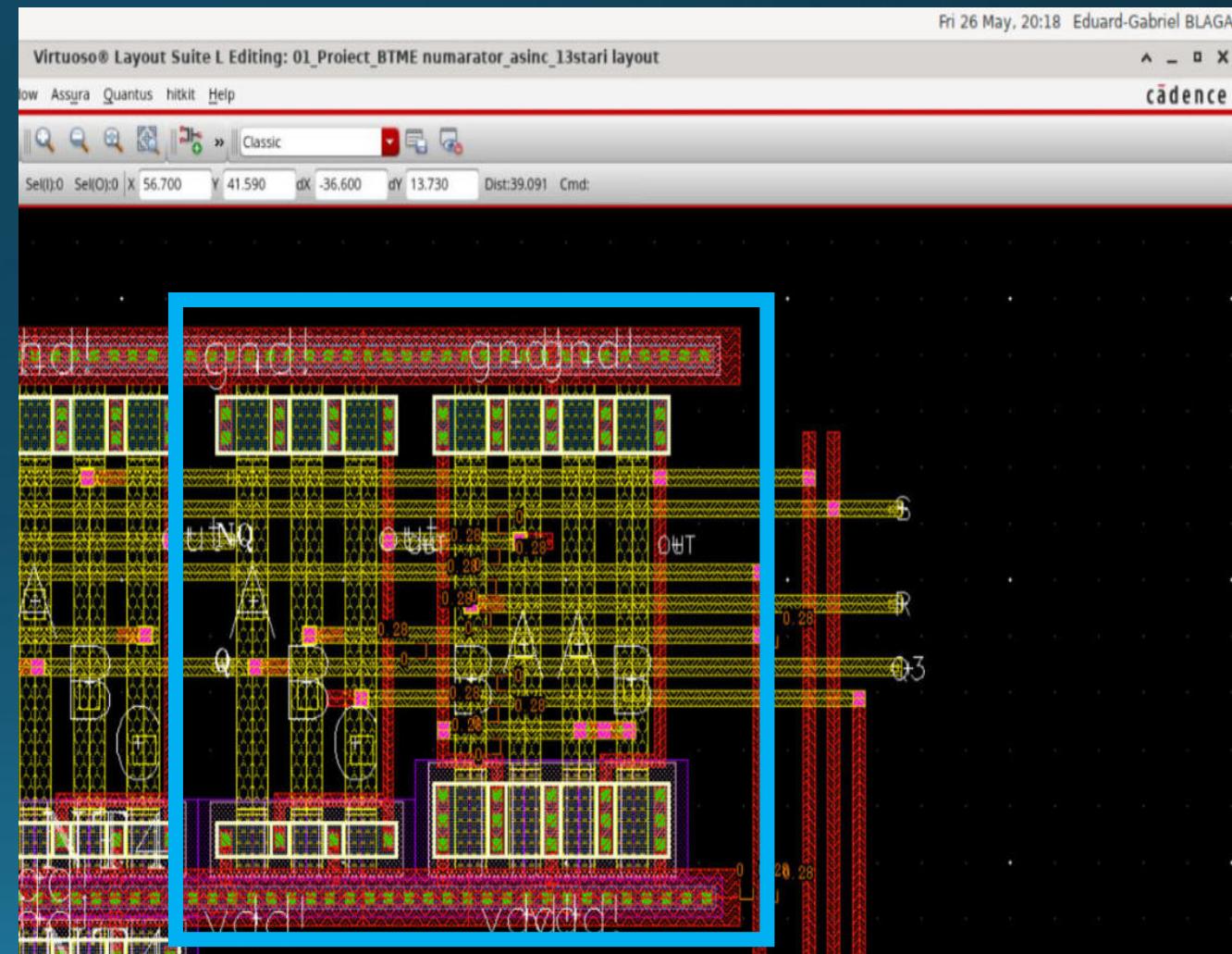
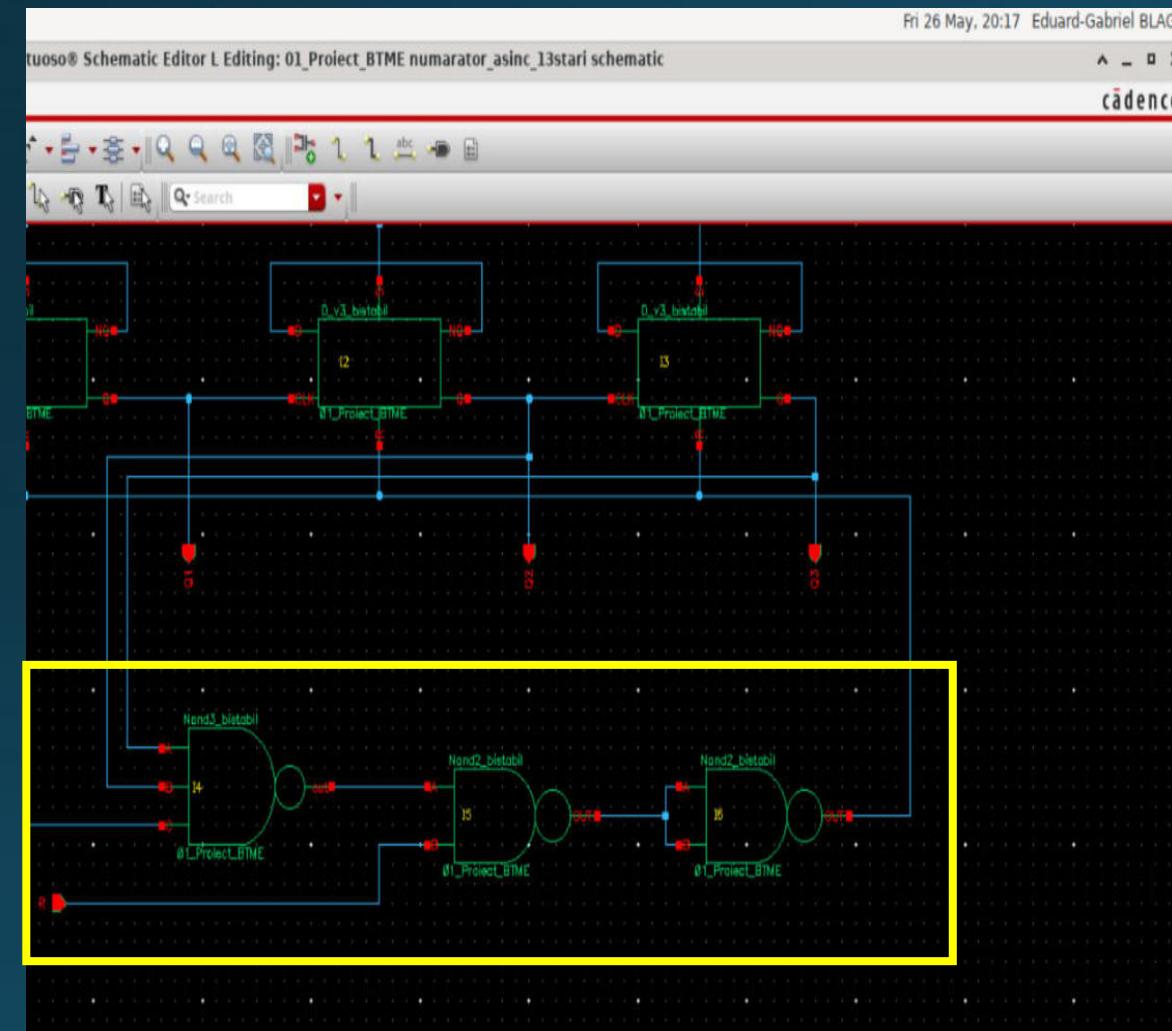
Se instantiaza bistabilul, il copiem pe verticala in oglinda si suprapunem vdd-urile. Dupa care mai copiem o data intreaga schema si suprapunem ground-urile



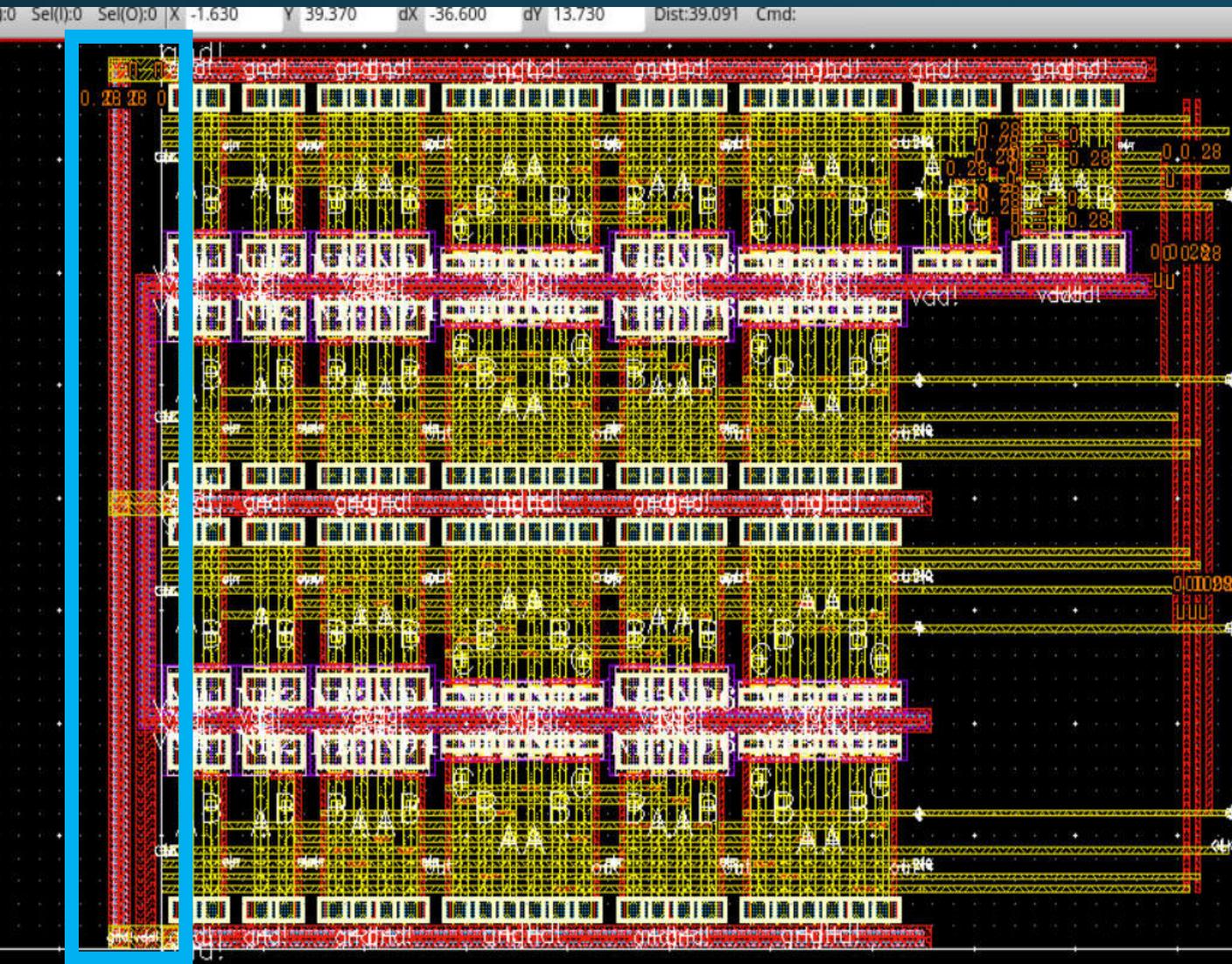
Specific schematicului, vom face legaturile dintre iesirile bistabilelor anterioare si intrarea de clock a bistabilului urmator



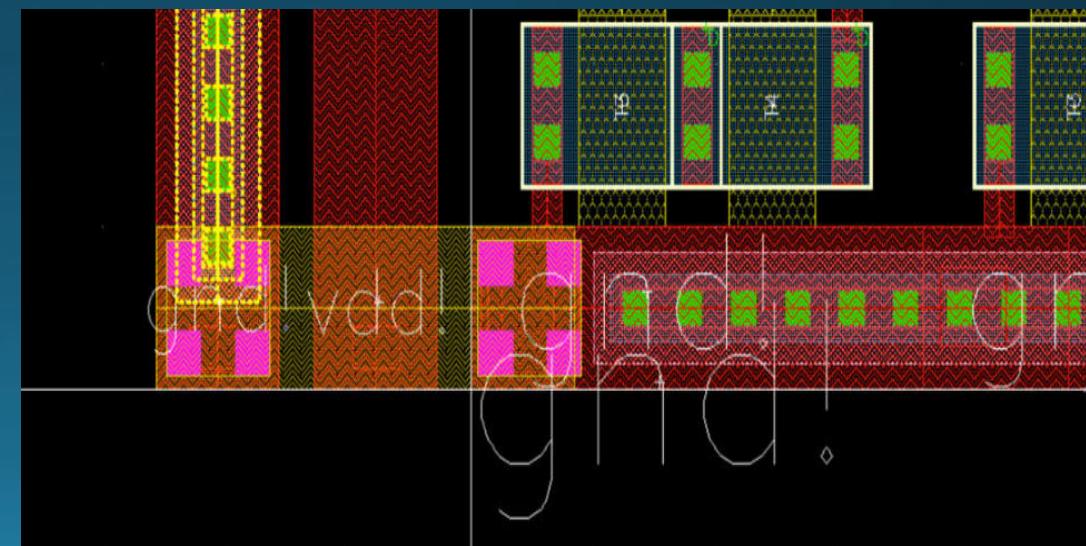
Cu Stratch se prelungesc conexiunile facute mai la dreapta si se instantiaza cele 3 porti nand necesare, urmand sa se faca conexiunile in aceeasi maniera ca la bistabil



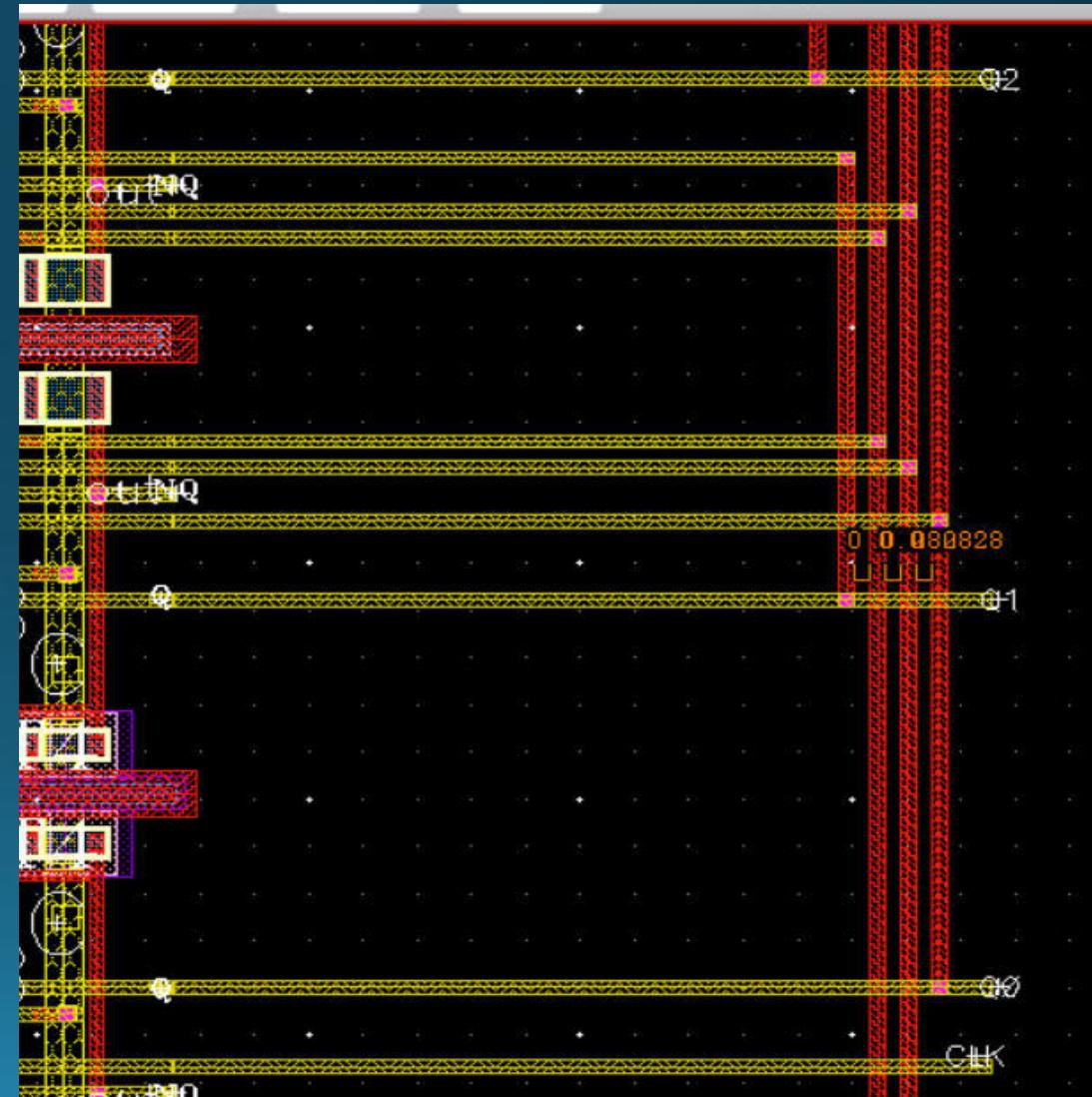
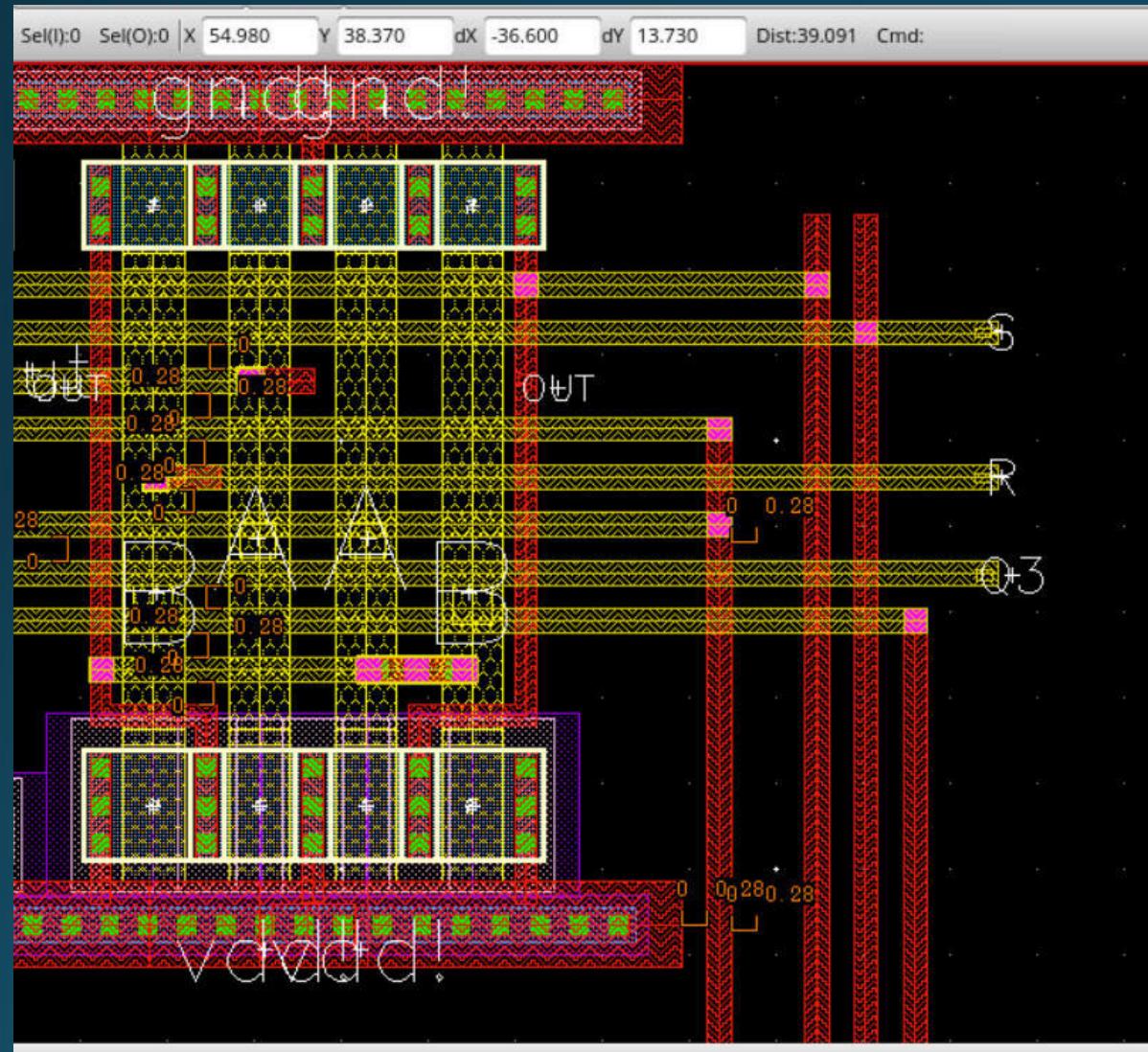
In partea stanga se creeaza linii de vdd si ground cu M1 cu pinii aferenti de tip InputOutput



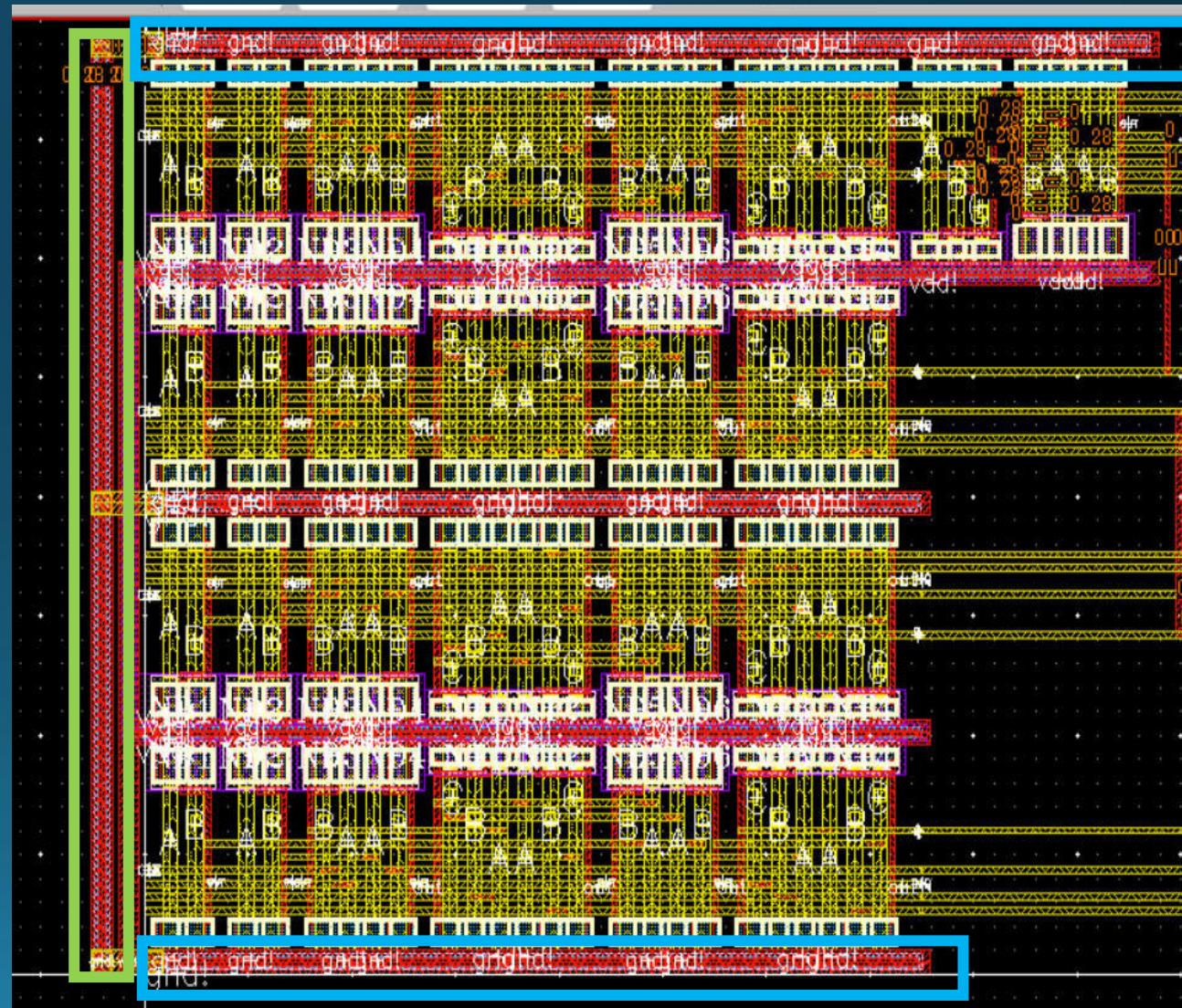
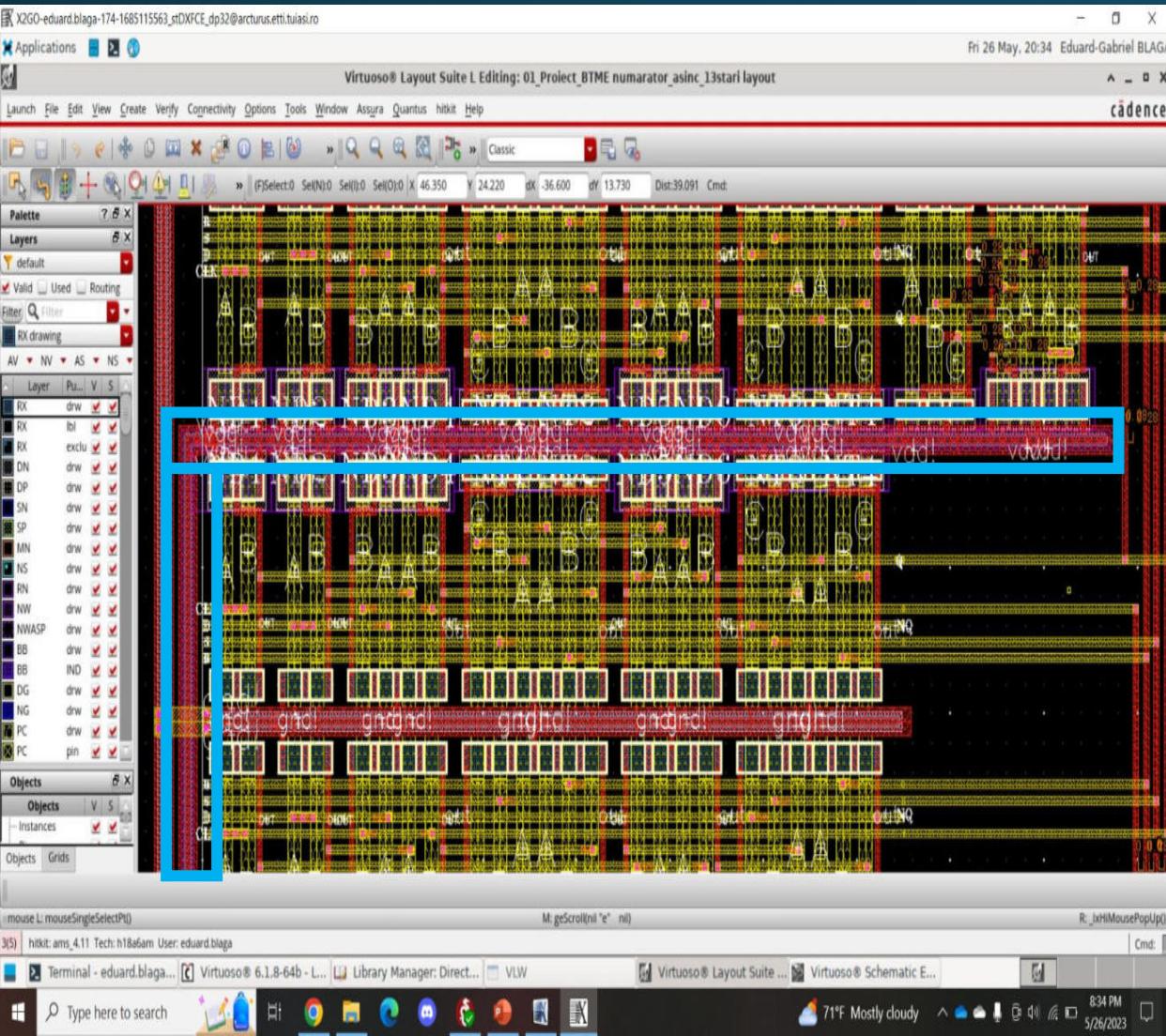
- Legatura dintre linia de ground de la bistabil si cea creeata recent se face cu o punte de M2, conectat cu VIA de tip M1-M2 2x2



Se realizeaza conexiunile de R si S care sunt commune pentru toate bistabilele si se realizeaza iesirile numaratorului, Setul, Resetul si Clockul



Se sterg din layout-ul bistabilului Multipart Path-urile si se creeaza altele noi in layout-ul numaratorului impreuna cu pinii gnd! si vdd!



Se realizeaza analizele DRC si LVS

