Test plan

DUT: Parameterizable adder.

Objectives: Verify the adder's behavior under various stimuli and determine the design's limit values.

RTL Description: The adder has two inputs, a and b, and a single output. The data bus width is configured pre-synthesis through the WIDTH parameter.

Test Cases:

Test Case 1: Basic Addition without Overflow

Assign 10 different values to a and b within a specified range that prevents overflow.

A value	B value	Expected result	Simulation result	Overflow

Test Case 2: Zero in the Inputs

Test the case where both inputs, a and b, have a value of zero.

A value	B value	Expected result	Simulation result	Overflow
0	**0**	**0**		

Test Case 3: Middle Values

Assign the middle value to both a and b so that the result is the maximum value minus 1.

A value	B value	Expected result	Simulation result	Overflow
7	**7**	**14**		

Test Case 4: Limit Values

Test the case where both inputs have the maximum possible value.

A value	B value	Expected result	Simulation result	Overflow
15	**15**	**14**		

Test Case 5: Addition of Even Numbers

Assign 10 even values to a and b to verify that the results are also even.

A value	B value	Expected result	Simulation result	Overflow

Test Case 6: Addition of Odd Numbers

Assign 10 odd values to a and b to verify that the results are even.

A value	B value	Expected result	Simulation result	Overflow

Test Case 7: Sum of Even a and Odd b

Assign 10 even values to a and 10 odd values to b to verify that the results are odd.

A value	B value	Expected result	Simulation result	Overflow

Test Case 8: Sum of Odd a and Even b

Assign 10 odd values to a and 10 even values to b to verify that the results are odd.

A value	B value	Expected result	Simulation result	Overflow