SERTECH LABS
580 Pleasant Street
Watertown, MA 02172
(617) 924-9280

# TSC311/312/313
## Flip Flops
- Master/Slave RST
- Dual J-K Edge Triggered
- Dual J-K Master/Slave

## Features

311

- NOT EDGE-SENSITIVE
- DIRECT SET AND RESET INPUTS
- SIX DATA INPUTS
- SEPARATE CLOCK INPUTS ALLOW TWO-PHASE OPERATION

312/313

- CAN BE SET OR RESET WITH CLOCK HIGH OR LOW
- CLOCK INPUTS ARE ONLY 1 UNIT LOAD
- J-K OR S-R OPERATION (313 J-K MASTER/SLAVE)
- FAST—5 MHz TYPICAL TOGGLE RATE
- EDGE-SENSITIVE OPERATION (ON 312)
- NON-EDGE SENSITIVE OPERATION (ON 313)

## General Descriptions

311

The 311 is a clocked master/slave flip-flop that can operate in set-reset or J-K modes. Applications flexibility is increased by three data inputs to each side of the master flip-flop and by two clock inputs. It provides three S-R inputs, or two J-K inputs, and operates single-phase or two-phase.

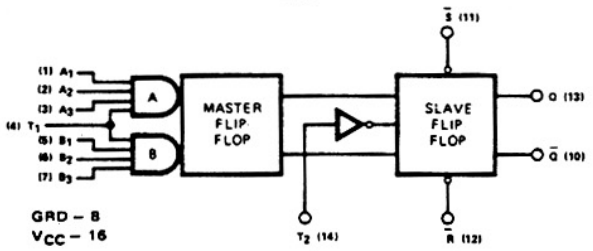
312/313

The 312/313 provides two fast, edge-triggered flip-flops in a single package. Separate logic inputs allow them to be used independently as J-K or set-reset flip-flops. Clock inputs present only 1 unit load.

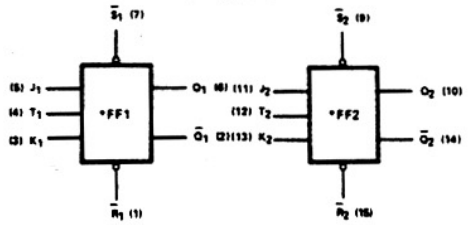
For use in new designs, the non-edge sensitive 313 is recommended.

## Logic Diagrams

311




312/313




On 313 FF1 and FF2 are master/slave flip-flops.

## Truth Tables

J-K MODE

| J | K | $Q^{n+1}$ |
|---|---|---|
| L | L | $Q^n$ |
| L | H | L |
| H | L | H |
| H | H | $\overline{Q}^n$ |

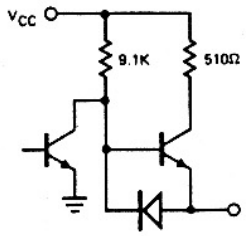
S-R MODE

| $\overline{S}$ | $\overline{R}$ | Q |
|---|---|---|
| H | H | X |
| H | L | L |
| L | H | H |
| L | L | H |

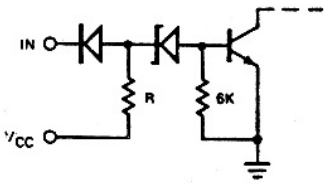
X = Indeterminate state

## Equivalent Circuits

TYPICAL OUTPUT




TYPICAL INPUT




R = 8.2K ON A, B, $\overline{S}$, $\overline{R}$, $T_2$
R = 4.1K ON $T_1$.

## Specifications

311

| $I_{CC}$ (WORST-CASE) | 18 mA @ 13V, 25 mA @ 16V | | | |
|---|---|---|---|---|
| $t_{PD}$ I/O FUNCTION FOR $t_{PD}$ | 820 ns T–Q+ | 610 ns T–Q– | 400 ns $\overline{R}$–$\overline{Q}$+ | 250 ns $\overline{R}$–$\overline{Q}$– |

TYPICAL TOGGLE RATE is 2 MHz

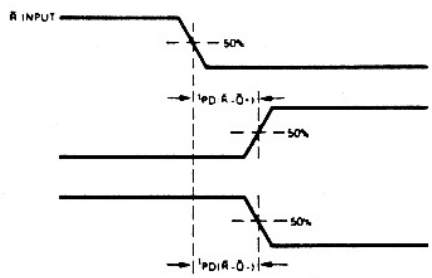
312,313

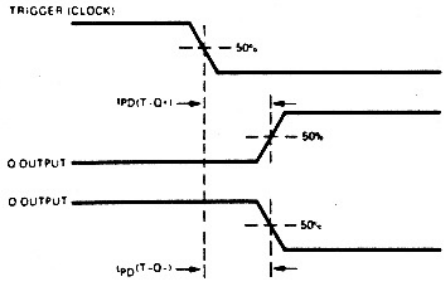
| $I_{CC}$ (WORST-CASE) | 30 mA @13V, 40 mA @16V | | | |
|---|---|---|---|---|
| $t_{PD}$ I/O FUNCTION FOR $t_{PD}$ | 300 ns T–Q+ | 230 ns T–Q– | 600 ns $\overline{R}$–$\overline{Q}$+ | 320 ns $\overline{R}$–Q– |

TYPICAL TOGGLE RATE IS 5 MHz

NOTE:
$I_{CC}$ is tested at $V_{CC}$ +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. $t_{PD}$ is guaranteed at $V_{CC}$ ±1V and across the applicable temp range with the output loaded with 6 unit loads.
**See page 12 for electrical summary data.**

## Switching Time Waveforms




NOTE:
J and K are tied to $V_{CC}$.

## Loading Tables

311

| PINS | FUNCTION | LOADING |
|---|---|---|
| A,B | Data inputs | 1 UL |
| $T_1$ | Clock input | 2 UL |
| $T_2$ | Clock input | 1 UL |
| $\overline{S}$,$\overline{R}$ | Direct $\overline{S}$-$\overline{R}$ inputs | 1 UL |
| Q,$\overline{Q}$ | Outputs | 6 UL |

312

| PINS | FUNCTION | LOADING |
|---|---|---|
| J,K | J-K inputs | 1 UL |
| T | Clock inputs | 1 UL |
| $\overline{S}$,$\overline{R}$ | Direct $\overline{S}$-$\overline{R}$ inputs | 2 UL |
| Q,$\overline{Q}$ | Outputs | 5 UL |

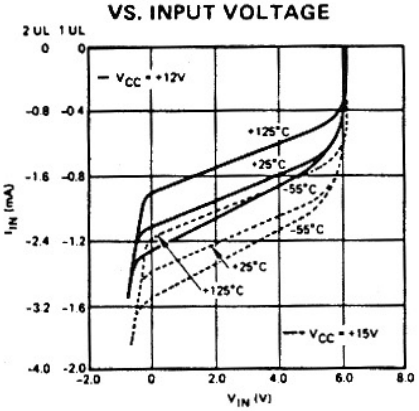
## Loading Tables (contd.)

313

| PINS | FUNCTION | LOADING |
|---|---|---|
| J,K | Data inputs | 1 UL |
| T | Clock input | 1 UL |
| $\overline{R},\overline{S}$ | Direct Set/Reset Inputs | 2 UL |
| Q,$\overline{Q}$ | Outputs | 5 UL |

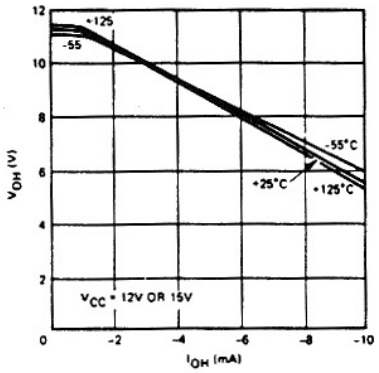
## Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

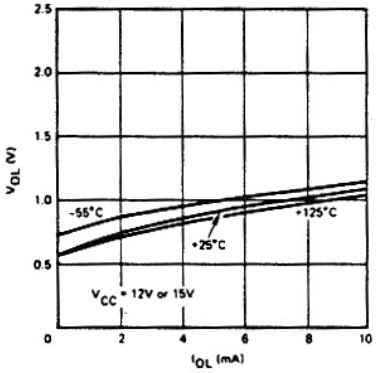



OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH




OUTPUT LOW




## Typical Applications

### 311

AND gates A and B form the set and reset inputs of the master flip-flop. The slave has direct set and reset inputs that operate active low (for example, the $\overline{R}$ input is switched low while the clock is high to reset the flip-flop). Also, input $T_2$ has a built-in inverter to inhibit data transfer from the master to the slave when the clock is high. The $T_1$ and $T_2$ thresholds are offset as shown on the single-phase timing diagram, to ensure proper inhibition of the master and slave in the single-phase mode.

Since there are three sets of master inputs, two J and K inputs are available in the J-K connection. In either the set-reset or J-K modes, single-phase operation is obtained by connecting $T_1$ to $T_2$, or two-phase operation by applying out-of-phase clocks to $T_1$ and $T_2$.

### 312

The 312 triggers on the falling edge of the clock pulse, which must fall faster than 3V/microsecond for proper operation. Direct set and reset may be accomplished at any time, with the clock either high or low.

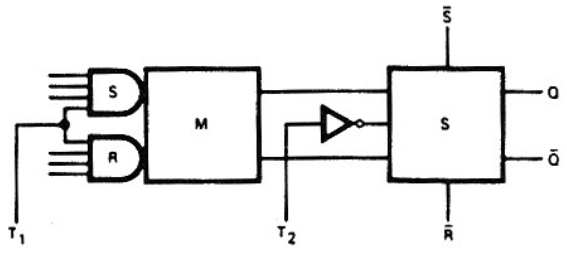
### 313

The 313 was developed to give the HiNIL logic designer the most flexible dual flip-flop package possible. The 313 is capable of J-K Master/Slave or S-R operation with set and reset inputs.

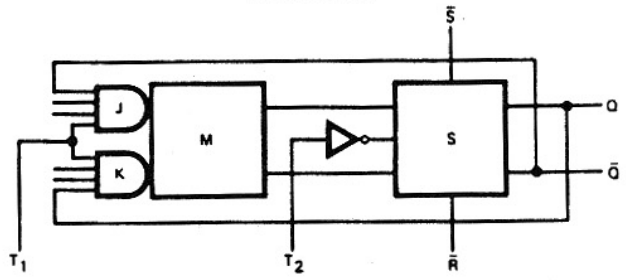
The timing diagram shown on page 28 indicates the operation sequence for J-K Master/Slave operation. The positive going edge of the clock pulse inhibits the slave and enables data transfer

311 CONFIGURATION

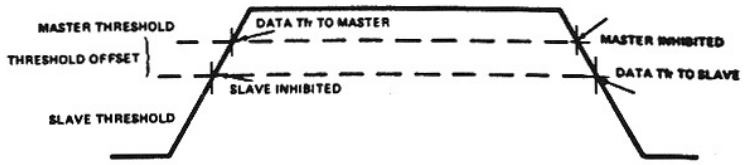
SET–RESET MODE




J-K MODE



## Typical Applications (contd.)




to the master (Master/Slave thresholds are offset to ensure proper inhibition and enable). The falling edge inhibits the master and allows data transfer to the slave.

Direct set or reset may be accomplished at any time, with the clock pulse either high or low.

For reliable operation the following 313 timing recommendations should be followed. They apply across both the applicable temp range and $V_{CC}$ spread.

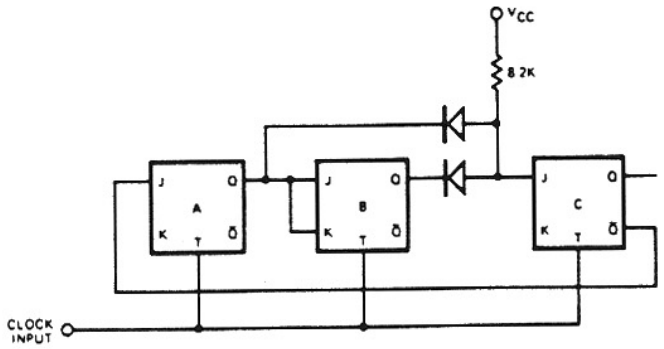
| | |
|---|---|
| Clock Pulse Width (CP) | 300 nsec min. |
| J-K Input Setup Time | $\geqslant$ CP |
| J-K Input Release Time | 0 nsec min. |
| $\overline{S}$ or $\overline{R}$ Pulse Width | 300 nsec min. |
| Clock Rise and Fall Time | N/A |

Due to the master/slave action of the 313, data must be present during the entire time the clock is high to ensure proper data transfer to the output.

NOTE:
Because of the high noise immunity of the 312/313, it can be used in a variety of counter configurations with inexpensive diodes replacing the external gating normally required. Use IN4148 or similar high-voltage diodes or the diodes in a 331 gate expander.

### 312, 313 CONFIGURATIONS

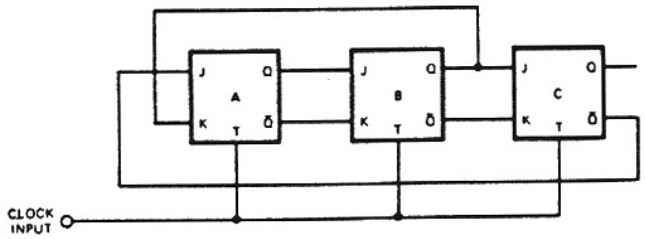
#### SYNCHRONOUS MOD 5, BINARY CODED OUTPUT




**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 0 | 0 | 0 |

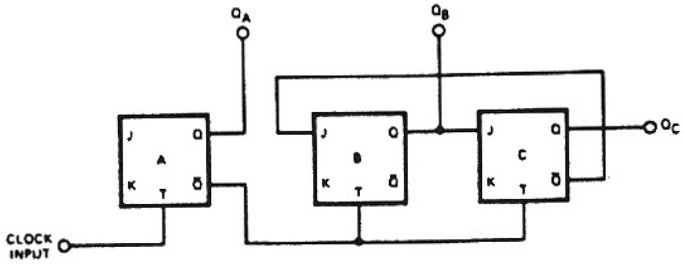
#### SYNCHRONOUS MOD 5, SHIFT MODE




**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 1 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 |
| 5 | 0 | 0 | 0 |

#### MOD 6, BINARY CODED OUTPUT

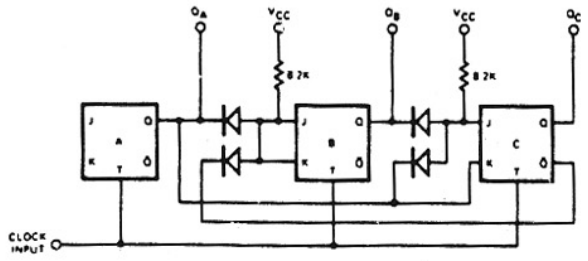



**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 |
| 6 | 0 | 0 | 0 |

## Typical Applications (contd.)

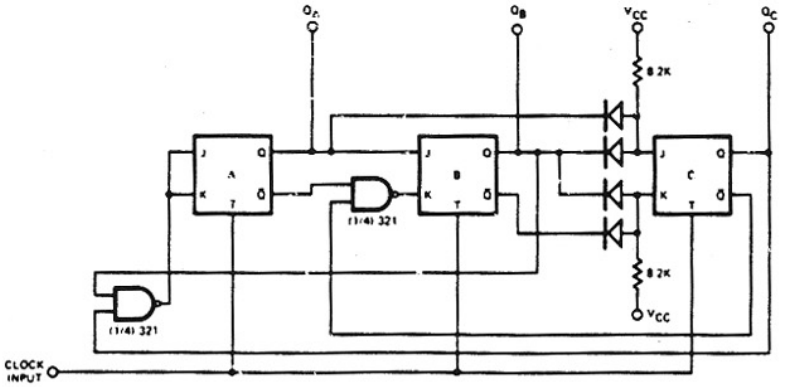
### SYNCHRONOUS MOD 6, BINARY CODED OUTPUT




**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 |
| 6 | 0 | 0 | 0 |

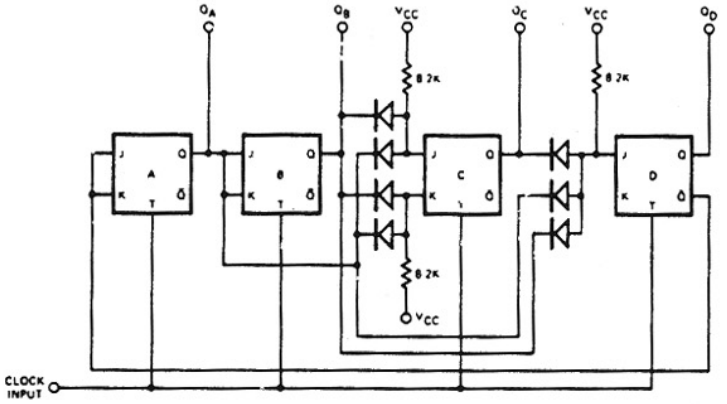
### SYNCHRONOUS MOD 7, BINARY CODED OUTPUT




**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 |
| 3 | 1 | 1 | 0 |
| 4 | 0 | 0 | 1 |
| 5 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 |

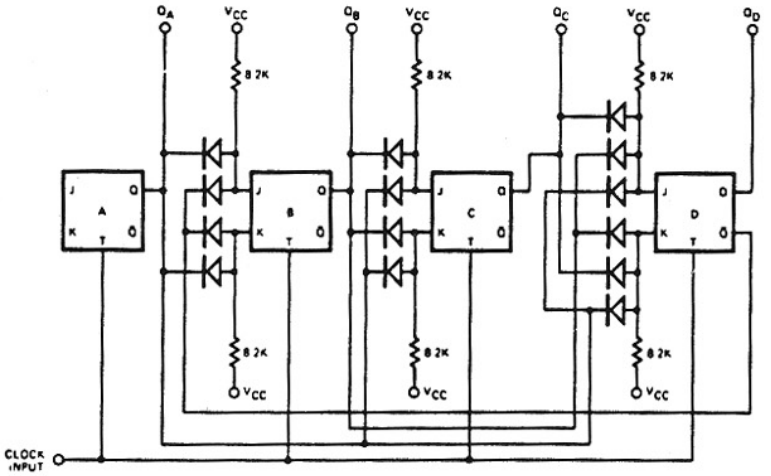
### SYNCHRONOUS MOD 9, BINARY CODED OUTPUT




**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 0 | 0 | 0 | 0 |

### SYNCHRONOUS BCD DECADE COUNTER




**TRUTH TABLE**

| T | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 1 | 0 | 0 |
| 4 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 1 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 0 | 0 | 0 | 0 |