chapter III: BPSK and QPSK modulation and demodulation with Simulink

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Chapter III: Phase Shift Keying modulation and demodulation

III-1 Introduction

Phase-shift keying (PSK) is a digital modulation process which conveys data by changing (modulating) the phase of a reference signal (the carrier wave). The modulation occurs by varying the sine and cosine inputs at a precise time. It is widely used for wireless LANs, RFID and Bluetooth communication.

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. PSK uses a finite number of phases; each assigned a unique pattern of binary digits. Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator, which is designed specifically for the symbol-set used by the modulator, determines the phase of the received signal and maps it back to the symbol it represents, thus recovering the original data. This requires the receiver to be able to compare the phase of the received signal to a reference signal – such a system is termed coherent (and referred to as CPSK).

III-2 Bipolar Phase Shift Keying modulation and demodulation (BPSK)

III-2- Introduction:

In phase shift keying (PSK), the phase of a carrier is changed according to the modulating waveform which is a digital signal. In BPSK, the transmitted signal is a sinusoid of fixed amplitude. It has one fixed phase when the data is at one level and when the data is at the other level, phase is different by 180 degree. A Binary Phase Shift Keying (BPSK) signal can be defined as

$$BPSK(t) = A_0 \times \sin\left(2\pi f_0 \bullet t + \begin{cases} 0 \text{ if } m(t) = '1' \\ \pi \text{ if } m(t) = '0' \end{cases}\right)$$

Where m(t) is the binary information, and the BPSK signal is presented in figure III-1.

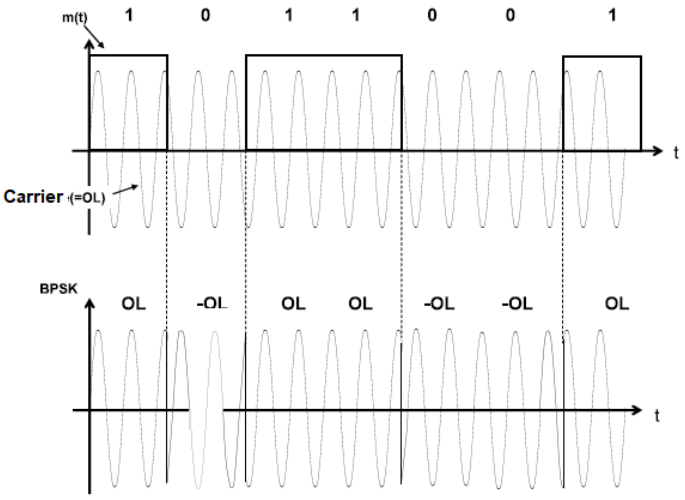


Figure (III-1): BPSK signal

III-2-2 Simulation

1- Using Simulink, create the following assembly

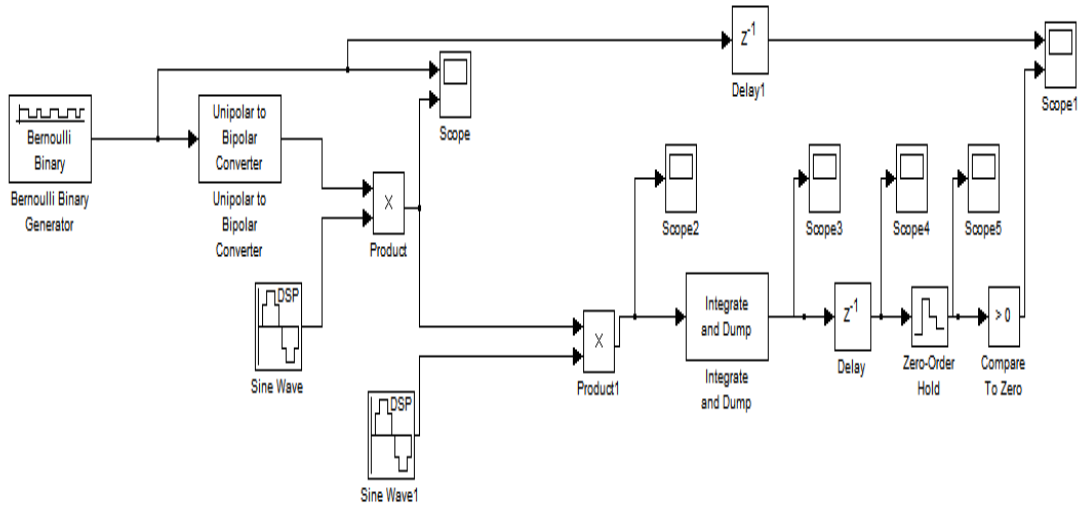


Figure (III-2): Modulation and demodulation BPSK simulation by Simulink

2- Configure all the blocks as follows

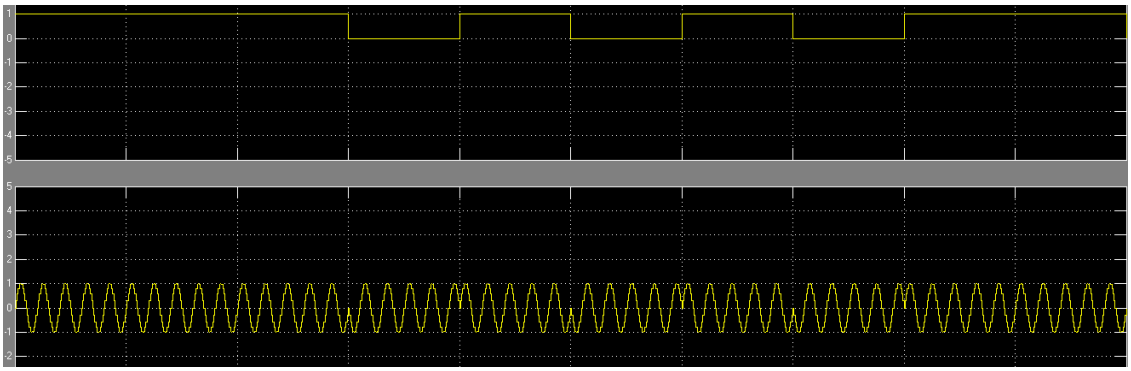
- Bernoulli Binary Generator
  - Probability of zero: 0.5
  - Initial seed: 37
  - Output data type: single
- Unipolar to bipolar Converter
  - M-ary number:2

- Sine Wave and Sine Wave 1:
  - Amplitude:1
  - Frequency (Hz): 5
  - Phase offset (rad): 0
  - Sample mode: Discrete
  - Output complexity: Real
  - Computation method: Trigonometric fcn
  - Sample time: 1/100
  - Samples per frame: 1
- Integrate and Dump:
  - Integration period (number of samples):100
  - Offset (number of samples): 0
  - Output intermediate values
- Delay:
  - Delay length: Source (Dialog), value:1
  - Initial condition: Source (Dialog), value:0.0
  - External reset: none
  - Sample time:-1
- Compare To Zero:
  - Operator: >

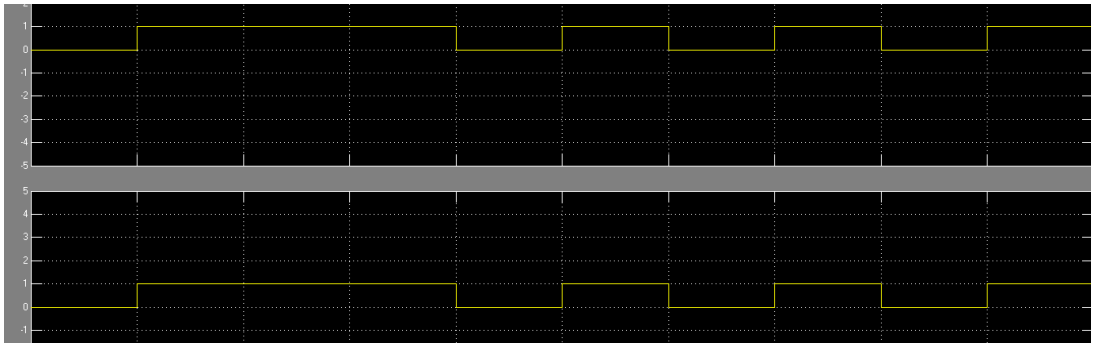
3- What is the utility of using the blocks "Integrate and Dump".

4- What is the role of the block "Zero-Order hold?

5- verify that the signals: modulating and modulated signals will be represented by the scope as follows:



6- verify the comparison between modulating and demodulated signals



III-3 Quadrature Phase Shift Keying modulation and demodulation (QPSK)

III-3-1 Introduction:

Quadrature Phase Shift Keying (QPSK) is a form of Phase Shift Keying in which two bits are modulated at once, selecting one of four possible carrier phase shifts (0, 90, 180, or 270 degrees). QPSK allows the signal to carry twice as much information as ordinary PSK using the same bandwidth. QPSK is used for satellite transmission of MPEG2 video, cable modems, videoconferencing, cellular phone systems, and other forms of digital communication over an RF carrier.

III-3-2 Simulation 1:

1- Using Simulink, create the following assembly

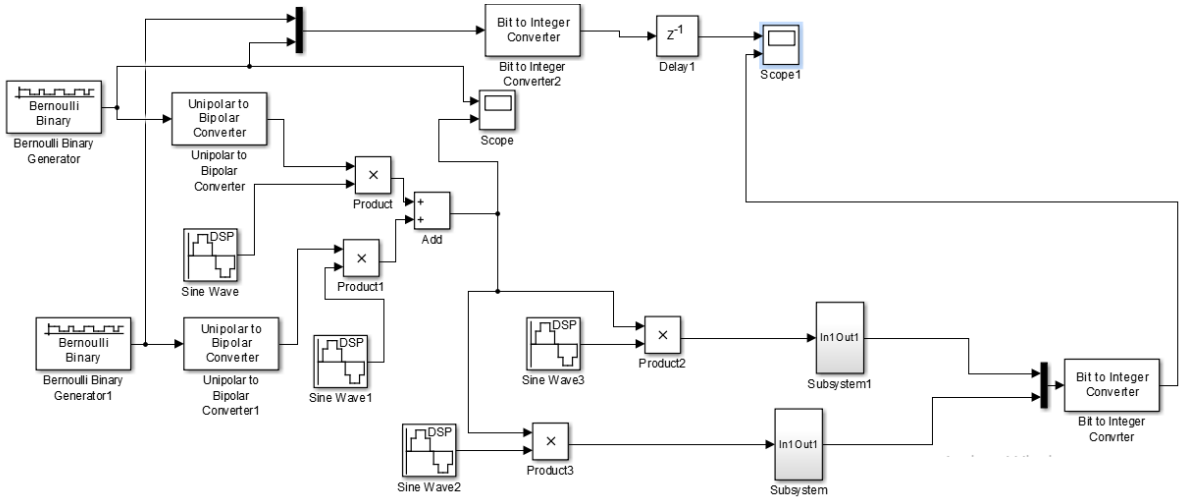


Figure (III-3): Modulation and demodulation QPSK simulation by Simulink

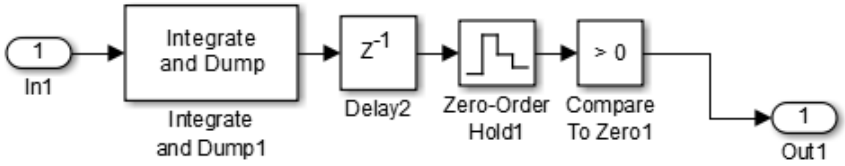
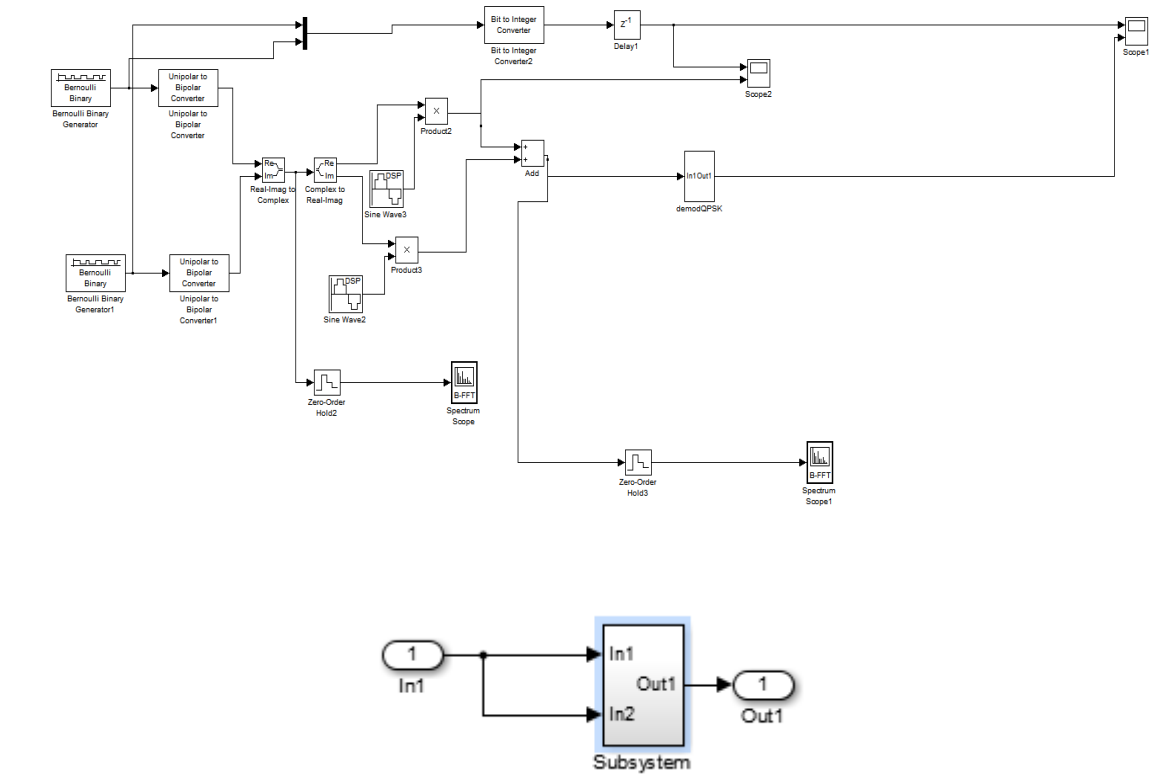


Figure (III-4): Subsystem bloc

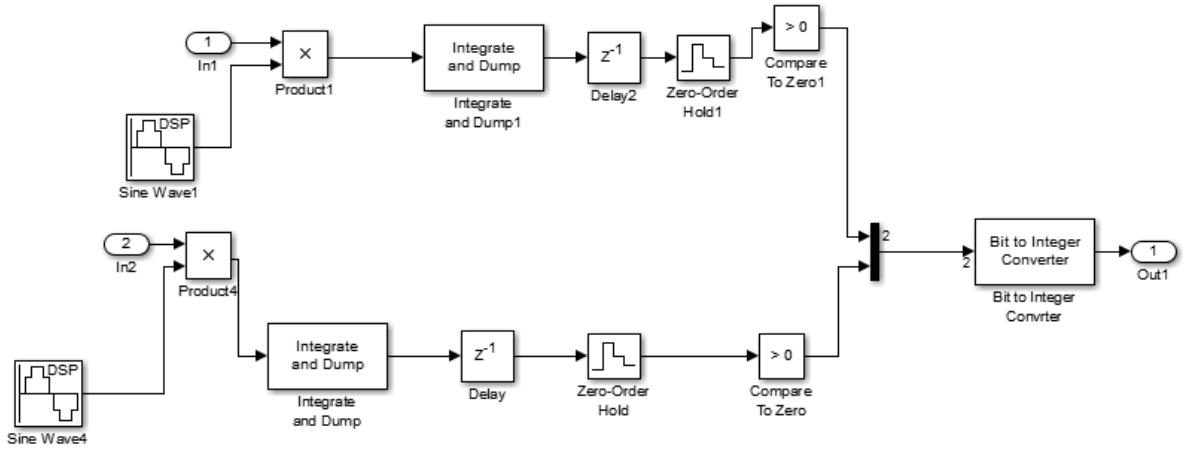
2- Configure all the blocks as follows

- Bernoulli Binary Generator: same parameters of BPSK one.
- Unipolar to Bipolar Converters: same parameters of BPSK ones.

III-3-2 Simulation 2:

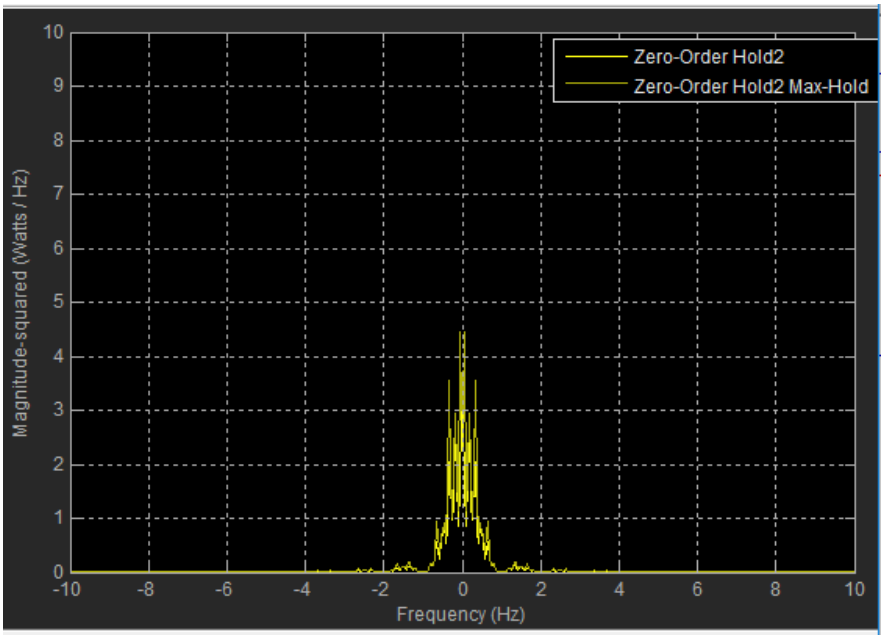


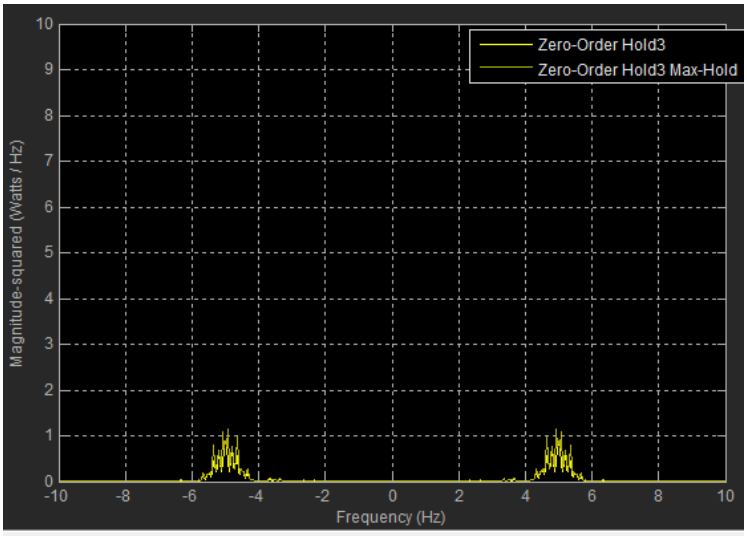
(a)

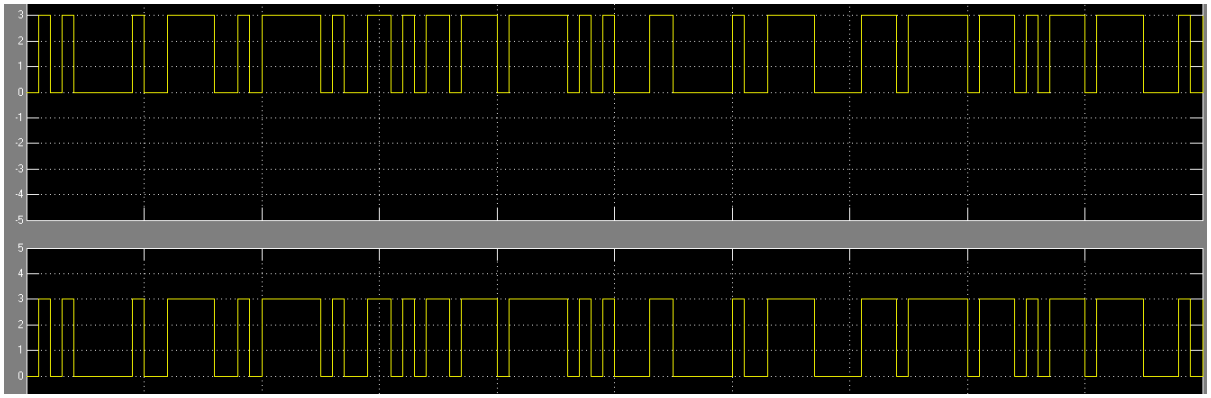


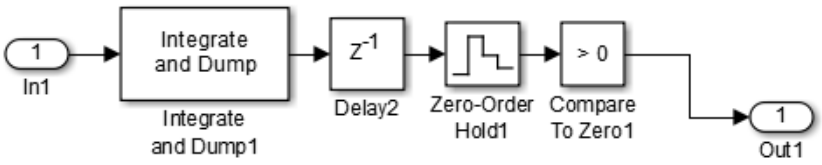
(b)

Figure (III-3) : QPSK demodulation subsystem bloc


Zero-Order Hold2
Zero-Order Hold2 Max-Hold
Magnitude-squared (Watts / Hz)
Frequency (Hz)
10
9
8
7
6
5
4
3
2
1
0
-10
-8
-6
-4
-2
0
2
4
6
8
10


Zero-Order Hold3
Zero-Order Hold3 Max-Hold
Magnitude-squared (Watts / Hz)
Frequency (Hz)
10
9
8
7
6
5
4
3
2
1
0
-10
-8
-6
-4
-2
0
2
4
6
8
10




1
In1
Integrate
and Dump
Integrate
and Dump1
Z-1
Delay2
Zero-Order
Hold1
> 0
Compare
To Zero1
1
Out1