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Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	10				
3	14				
4	15				
5	15				
6	10				
7	15				
8	10				
9	10				
Total	100				

You may ask for clarification but you are ultimately responsible for the answer you write on the paper. If you make any assumptions state them.

Please look through the entire test before starting. WE MEAN IT!!!

Illegible answers are wrong answers.

Show your work in the space provided to get any credit for problem-oriented questions.

Good luck!

1. (1 point, 1 min)
The newly named chair of the School of Computer Science:
(a) Annie Anton (b) Lance Fortnow
(c) Zvi Galil (d) Ellen Zegura
(e) Charles Isbell (e) George Burdell

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Memory management

2. (10 points, 10 min)

a) (4 points)
The number of virtual pages is defined by the ratio:

_____/_____.

The number of physical frames is defined by the ratio:

_____/_____.

The page table is set up by the _____.

The page table is looked up on every memory access by the _____.

b) (2 points) (circle the right choice) Given 32-bit virtual address; 28-bit physical address; 4 KB page size; 8 processes currently executing, the number of page tables in memory is:

1. 4
2. 2^{20}
3. 8
4. 28
5. 12
6. 2^{16}
7. 32

c) (2 points) One scheme to implement a TRUE LRU policy for page replacement by the OS is the following:

- Have a hardware stack wherein each entry of the stack holds the page frame number accessed by the CPU; CPU updates the stack on each memory access
- Have an instruction in the ISA for the OS to read the LRU page frame from the stack

Why is this idea infeasible to implement?

d) (2 points) How is the reference bit per page table entry used in implementing an approximate LRU using the second chance page replacement policy (limit to 3 or 4 concise bullets please)?

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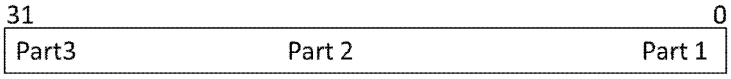
Cache

3. (14 points, 15 min)

a) (6 points)

A computer has the following characteristics:

- It is **byte-addressed** and the address is 32 bits long (little endian)
- It has a **4-way set-associative cache** with each data block holding 64 bytes of data
- The cache has a total of **16 K data blocks**



The above figure shows how the address is divided into three parts to perform a cache access. Name the parts (below) and the number of bits associated with each part.

Part 1: _____ (name) _____ (number of bits)

Part 2: _____ (name) _____ (number of bits)

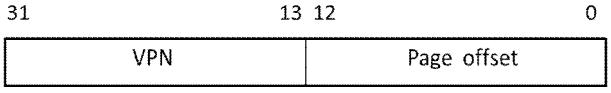
Part 3: _____ (name) _____ (number of bits)

b) (3 points)(fill in using the words, "capacity", "compulsory", "conflict")

Consider a 2-way set associative cache.

1) CPU accesses memory location X for the **first time**. This is a _____ miss.
2) The cache is **not full**. The CPU has made a number of accesses including to locations X, Y, Z, P, Q, and R in that order. CPU now makes a reference to location X again. If X is **not** in the cache and has to be brought from memory, then this is a _____ miss.
3) At some later point in time the **cache is full**. The CPU makes a reference to location X again. If X is **not** in the cache and has to be brought from memory, then this is a _____ miss.

c) (5 points) Consider a **virtually indexed physically tagged** cache. The virtual address is 32 bits. The page size is 8K bytes.



The cache is **direct mapped** with **512 KB** and a **block size** of **64 bytes**. How many low order bits of the VPN should remain unchanged in the translation process for the above cache to work correctly?

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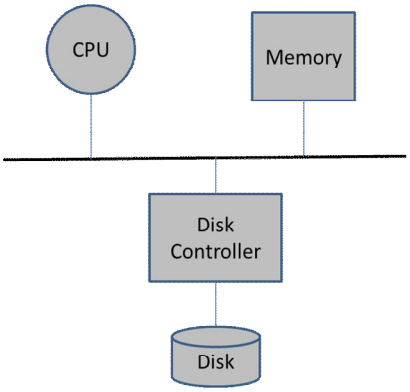
Input/Output and Disk

4. (15 points, 20 min)

a) (10 points) Design a DMA controller for a disk drive. You have to design only the way the controller interfaces with the CPU and the memory bus. You don't have to worry about the device electronics side of the controller. Recall that a disk address is a tuple: {cylinder#, platter#, track#, sector#). Clearly show the registers in the controller for interfacing to the CPU and the memory, describe succinctly their purpose, and how the CPU communicates with the controller and vice versa, and how the data transfer is effected by the controller.



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b) (5 points) Given the following specifications for a disk drive:
512 bytes per sector
400 sectors per track
6000 tracks per surface
3 platters
Rotational speed 15000 RPM

What is the transfer rate of the disk?

File Systems

5. (15 points, 15 min)
a) (6 points)
Notes:

- Unix "**touch <file>**" command creates a zero byte new file or updates the timestamp of the named file
- Unix "**ln <file1> <file2>**" command creates a hard link
- Unix "**ln –s <file1> <file2>**" command creates a sym link
- Unix "**rm** <file>" removes the named file

In the following table, assume **none of the files exist to start with** in the current directory. Fill in the table. The reference count in the table pertains to the i-node that is affected by the command in that row. If a new i-node is created, show the old reference count for that i-node as 0.

Command	New i-node created (yes/no)	Reference count	
		old	new
touch f1			
ln f1 f2			
ln f2 f3			
rm f1			
ln –s f2 f4			
ln f4 f5			

Use this area for rough work for this question.

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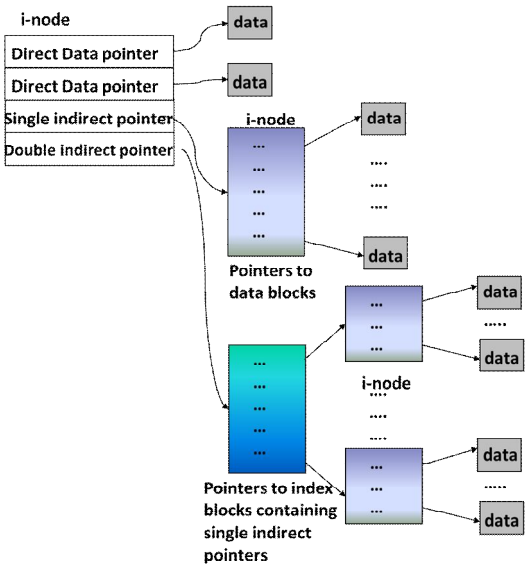
b) (9 points)
Using C like syntax, write the i-node data structure. Note that an i-node may represent a directory, a data file, or a symbolic link. If it represents a data file it has the structure shown in the figure: it could be a top level i-node, or an intermediate index block as shown in the figure.



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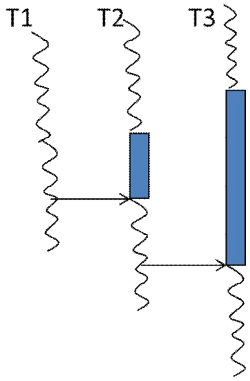
Parallel Systems

6. (10 points, 10 min)

X = 0;



The Shared variable X is initialized to 0;

- T3 is waiting for X to become 2
- T2 is waiting for X to become 1
- T1 changes X to 1 and signals T2
- T2 changes X to 2 and signals T3

Write the code snippets that implement the above synchronization among the threads T1, T2, and T3.

Note:

- Busy waiting solution gets NO CREDIT.
- Loss of concurrency **except when needed** to implement the required synchronization will not get full credit.
- Of course you have to ensure there are no deadlocks.

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7. (15 points, 20 min)
a) (7 points) Given mutex lock m, and condition variable c, the following events happen in the order of occurrence shown below:

- T1 executes mutex-lock(m); assume no one has the lock so T will win
- T1 executes cond-wait(c, m)
- T2 executes mutex-lock(m)
- T3 executes mutex-lock(m)
- T2 executes cond-signal(c)

Show the waiting queues associated with m and c.

- Clearly, show which thread is currently holding the mutex lock, and which threads are in the waiting queue for the lock.
- Note that if a thread is waiting on a condition variable, you should also show the mutex lock it needs for resuming execution.

(i) State of waiting queues before T2 executes cond-signal

(ii) State of waiting queues after T2 executes cond-signal

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b) (3 points)
Fill in the blanks using a subset of the following phrases exactly once.

Hardware **operating system** **page table** **cache** **registers**

In an SMP that supports hardware cache coherence, the _____ is responsible for ensuring that the copies of the same memory location in the different caches are kept consistent; the _____ is responsible for ensuring that the TLBs in the different processors are kept consistent; the _____ is shared among all the threads of the same process.

c) (5 points)
Given a **dual core cache-coherent** processor with **per core cache** and shared memory:
Cache coherence protocol: **write-invalidate**
(i.e., write by a core to its cache invalidates the peer core cached copy if present)
Cache to memory policy: **write-back**
(i.e., cached copy in a core may be more up to date than memory; upon a cache miss for a memory location, a peer core will supply the data if its copy is more up to date compared to memory)
Initially:
The **caches** are **empty.**
Memory locations: **A contains 33; B contains 15**
(use **NP** for a memory location not present in the cache; **I** if the cached content is invalid)

I. **Core 1** executes: **Load A**
Show the contents of the caches and memory for memory address A

	Core 1 cache	Core 2 cache	Memory
A			

II. **Core 2** executes: **Store #99, A**; (write immediate value 99 into A)
Show the contents of the caches and memory for memory address A

	Core 1 cache	Core 2 cache	Memory
A			

III. **Core 1** executes: **Store #22, B** (write immediate values 22 into B)
Show the contents of the caches and memory for memory address B

	Core 1 cache	Core 2 cache	Memory
B			

IV. **Core 2** executes: **Load B**
Show the contents of the caches and memory for memory address B

	Core 1 cache	Core 2 cache	Memory
B			

V. **Core 2 evicts A from its cache**
Show the contents of the caches and memory for memory address A

	Core 1 cache	Core 2 cache	Memory
A			

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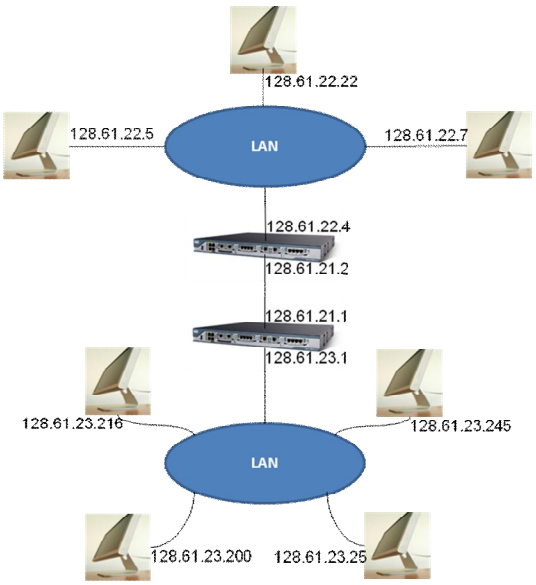
Networking

8. (10 points, 10 min)

a) (2 points) How many IP Networks are there in the following Figure? Assume that the top 24 bits of the 32-bit address name an IP network.



Your answer:

b) (3 points) Give three short reasons to justify the need for a separate network layer in the protocol stack.

-
-
-

c) (5 points)

A packet header consists of the following fields:

Destination address	8 bytes
Source address	8 bytes
Number of packets in message	4 bytes
Sequence number	4 bytes
Actual packet size	4 bytes
Checksum	4 bytes

Assuming that the maximum packet size is 1574 bytes, what is the maximum payload in each packet?

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9. (10 points, 10 mins)
Given the following:

Sender overhead	= 1 ms
Message size	= 200,000 bits
Wire bandwidth	= 100,000,000 bits/sec
Time of flight	= 2 ms
Receiver overhead	= 1 ms

Compute the observed bandwidth. Recall that the message transmission time consists of sender overhead, time on the wire, time of flight, and receiver overhead. Ignore ACKs.