CS 2200 Spring 2010 Test 2

Prism ID:____________

Name: Kishore________________ GTID#: 9____________

Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	10				
3	15				
4	12				
5	6				
6	10				
7	14				
8	12				
9	5				
10	15				
Total	100				

- **You may ask for clarification but you are ultimately responsible for the answer you write on the paper.**
- **Illegible answers are wrong answers.**
- **Please do not discuss this test by any means (until 5 pm today)**
- **Please look through the entire test before starting. WE MEAN IT!!!**

Illegible answers are wrong answers.
Good luck!

1. (1 point, 1 min) (circle one)
Yellow Jackets and the 2010 NCAA Basketball tournament.

Yellow Jackets

a) never got invited b) lost in the first round

[✓ c) lost in the second round] d) made it to sweet 16

e) made it to elite 8 e) made it to final 4

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Pipelining

2. (10 points, 5 min)
Use the following phrases in the sentences below. Each phrase should be used only once. **Not all phrases may be needed.**

(1) compiler (2) operating system (3) useful instructions (4) delayed branch
(5) branch prediction (6) delay slots (7) pipeline depth (8) always
(9) never (10) predicted (11) sequential (12) mispredicted
(13) flushed (14) target addresses (15) addresses (16) expected outcomes
(17) hardware device (18) target (19) executed (20) software data structure

- If a processor uses delayed branch, it is the responsibility of the Compiler to find useful instructions to fill the delay slots.

- With delayed branch, some number of instructions equal in number to the delay slots will always be executed regardless of the outcome of the branch.

- If a processor uses branch prediction, it allows the predicted stream of instructions into the pipeline following the branch.

- Upon detecting that a branch is mispredicted, the instructions following the branch are flushed.

- Branch target buffer is a hardware device that is pre-loaded before the program starts with the expected outcomes and the target addresses of the branches in the program.

Note: It is ok to switch the two Phrases in the last sentence.

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Process Scheduling

3. (15 points, 15 min)

Recall that *Shortest Remaining Time First (SRTF)* is a variant of Shortest Job First (SJF) with preemption added in. Consider the following three processes vying for the CPU. The scheduler uses SRTF. The scheduler re-evaluates which process to run only upon the arrival of a new process into the scheduling queue, or the completion of a process. The table shows the arrival time of each process.

Process	**Arrival Time**	**Execution Time**
P1	T_0	5ms
P2	T_0+2ms	4ms
P3	T_0+3ms	1ms

The scheduling starts at time T_0.

Fill in the table below with the process that is executing on the processor during each time slot. (10 points)

Interval T_0+	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
Running	P1	P1	P1	P3	P1	P1	P2	P2	P2	P2			

Use the following tables to show your work as to how you arrived at the above schedule. +1 for each correct entry in the table

Time T_0:

Process	Remaining time
P1	5ms
P2	Not arrived yet
P3	Not arrived yet

Time T_0+2: (Process P2 arrives)

(2 points)

Process	Remaining time
P1	3 ms
P2	4 ms
P3	Not arrived yet

Time T_0+3: (Process P3 arrives)

(3 points)

Process	Remaining time
P1	2 ms
P2	4 ms
P3	1 ms

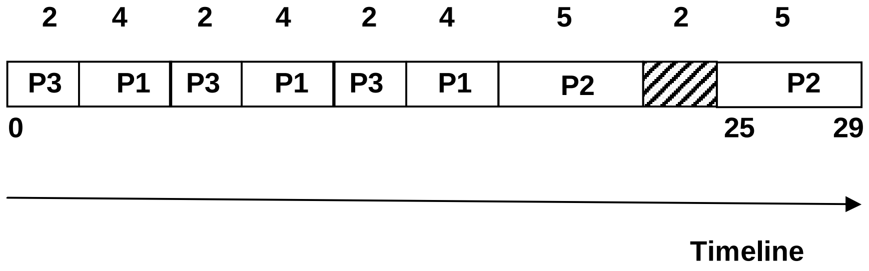
4. (12 points, 15 min)
There are three processes in the scheduling queue and assume that all three of them are ready to run. Assume that P1 arrived a little before P2; and P2 arrived a little before P3. Scheduling starts at time t = 0. The CPU and I/O burst patterns of the three processes are as shown below:

	CPU	I/O	CPU	I/O	CPU	
P1	4	2	4	2	4	P1 is done
P2	5	2	5			P2 is done
P3	2	2	2	2	2	P3 is done

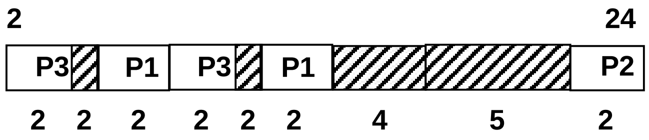
Each process exits the system once its CPU and I/O bursts as shown above are complete.

You are given the following schedule.

CPU Schedule (time allotted to each process is shown below)



I/O Schedule



(a) (3 points) What type of scheduler (FCFS, SJF, SRTF, RR) will produce the above schedule? Explain your answer.

- Not FCFS since arrival time ignored
- Not RR from inspection of schedule

** SJF or SRTF **

+1 for stating SJF or SRTF

+2 for mentioning some plausible reason

(b) (6 points) What is the waiting time for each process?

P1's waiting time = turnaround time - Exectime

= 18 - 16 = 2

P2's waiting time = 30 - 12 = 18

P3's waiting time = 14 - 10 = 4

(+2 for each right answer)

(c) (3 points) what is the average throughput of the system?

Total time = 30

Throughput = $\frac{\text{number of processes completed}}{\text{total time}}$

(All or nothing)

$= 3/30 = \boxed{1/10 \text{ processes per unit time}}$

Memory Management

5. (6 points, 5 min)

(a) (select one of the following)

The necessary conditions for a paging memory system are

a. The virtual and physical addresses have to be of the same size

b. The sizes of the virtual page and the physical frame have to be the same

c. The number of physical frames should be larger than the number of virtual pages

d. (a) and (b)

e. (b) and (c)

f. (a) and (c)

g. (a), (b), and (c)

(b) (select one of the following)

To implement paging the minimum additional hardware needed in the CPU data path

a. One Page table implemented in hardware

b. Multiple page table (one per process) implemented in hardware

c. One Page Table Base Register (PTBR)

d. Multiple PTBR (one per process)

e. None of the above

6. (10 points, 10 min)

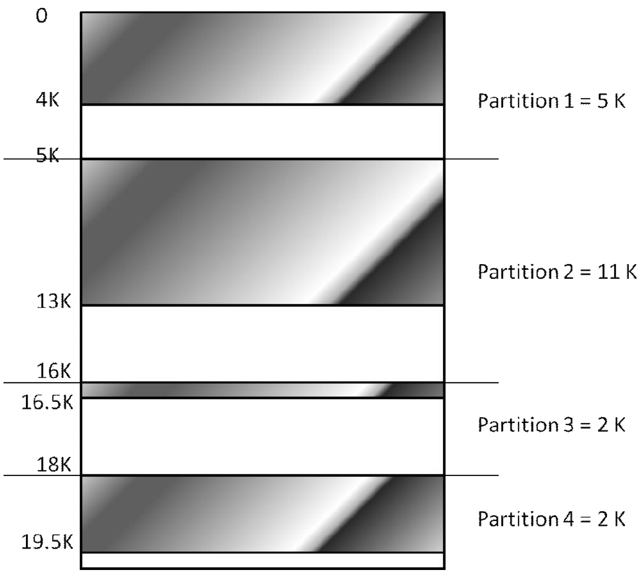


Figure 6(a)

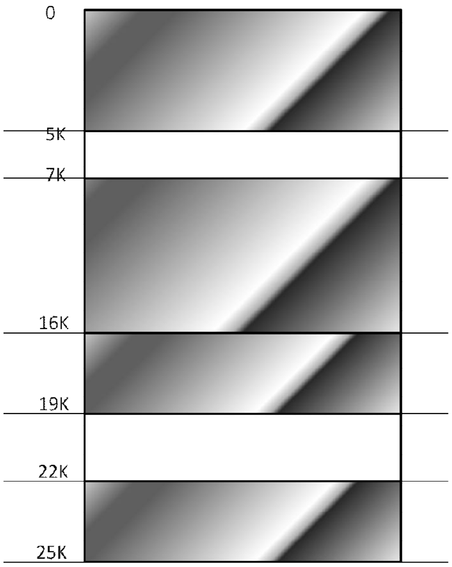


Figure 6(b)

(a) Consider the memory occupancy shown in Figure 6(a) for a fixed sized partition memory allocation. There are four partitions (5K, 11K, 2K, and 2K). In each partition, the shaded region is used, and the white space is the unused portion of the partition. For example, in partition 3, 0.5 Kbytes is used, and 1.5 Kbytes is unused. What is the total amount of internal fragmentation?

Internal fragmentation in partition 1 = 5K-4K = 1K

—— do ———— partition 2 = 11K_8K = 3K

—— do ———— partition 3 = 2K-0.5K = 1.5K

—— do ———— partition 4 = 2K-1.5K = 0.5K

Total internal fragmentation = 6K (+1 for each line)

(b)Consider the memory occupancy shown in Figure 6(b) for a variable sized partition memory allocation. There are 6 partitions. The shaded areas are the "in use" partitions, and the white spaces are the freed up partitions. What is the total amount of external fragmentation?

Total space in non-contiguous partitions

= 2K + 3K = 5K

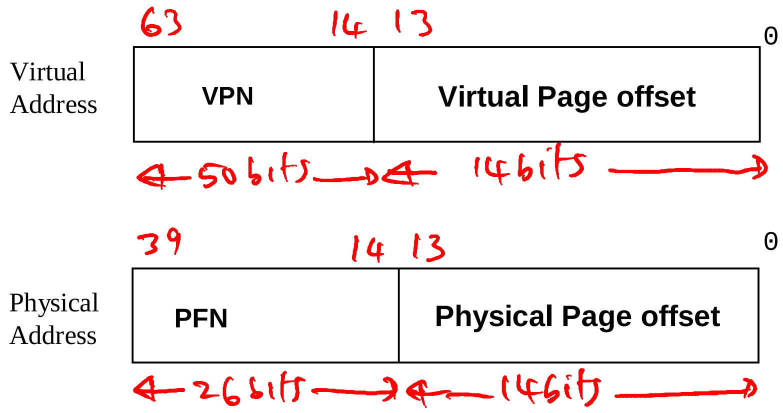
Total external fragmentation = 5K

(All or nothing?)

Virtual Memory

7. (14 points, 15 min)
Consider a memory system with 64-bit virtual addresses and 40-bit physical addresses. The page size is 16 KB.

(a) (8 points) Assuming little-endian notation show the bit positions occupied by the VPN, Virtual Page Offset, PFN, and the Physical Page Offset in the figures below.



# of bits in page offset

$= \log_2 16K$

$= 14$ bits

(+4 for page offset
+2 for VPN
+2 for PFN)

(b) (3 points) How many entries are there in the page table?

# of entries in PT $= 2^{VPN}$

$= 2^{50}$ entries

(c) (3 points) How many page frames are there in the memory system?

# of page frames $= 2^{PFN}$

$= 2^{26}$ page frames

Working set

8. (12 points, 10 min)
During the time interval t1 - t2, the following virtual page accesses are recorded for the three processes P1, P2, and P3, respectively.

P1: 0, 1, 2, 1, 2

P2: 0, 1, 2, 1, 2, 1, 2, 1, 2

P3: 0, 1, 2, 3, 4, 5, 6, 7, 8, 0

a) (6 points) What is the **working set** for each of the above three processes for this time interval?

(+2 for each)

P1: { 0, 1, 2 }

P2: { 0, 1, 2 }

P3: { 0, 1, 2, 3, 4, 5, 6, 7, 8 }

b) (6 points) What is the **cumulative memory pressure** on the system during this interval?

WS size P1 = 3
WS size P2 = 3
WS size P3 = 9
(+2 for each)

Cumulative memory pressure = 15 page frames

Caching

9. (5 points, 5 min)
A pipelined processor has an average CPI of 1.5 not considering memory effects. On an average each instruction incurs a cache miss rate of 1%, and the miss penalty is 100 cycles What is the effective CPI taking into account memory stalls?

Effective CPI = Average CPI without cach effects + memory stalls due to cach misses
(+1 for formula)

memory stalls due to cache misses
(+2 for this)
= miss rate * miss penalty
= $\frac{1}{100} * 100$ = 1 cycle

Effective CPI = 1.5 + 1 = 2.5 (+2 for this)

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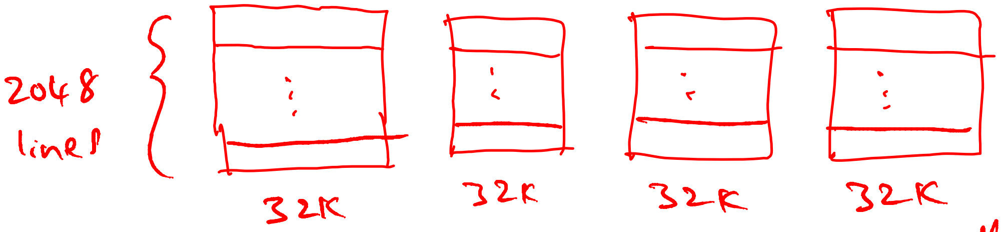
10. (15 points, 15 min)

Given the following

Memory address	=	32 bits
Cache size	=	128 Kbytes
Blocksize	=	16 bytes
Organization	=	4-way set associative

(a) (6 points) How many cachelines are there in the above memory hierarchy? Recall that the number of cachelines is the number of uniquely indexed rows in the cache organization. (Use pictures to explain your answer)



1) With 128K bytes total size and 4-way, each of the four parallel caches has 32Kbytes.

2) Since the blocksize is 16bytes, the number of lines in the organization = 32K/16 = 2K

(+3 for each point) = 2048 lines

(b) (3 points) How many index bits are needed to lookup the cache?

Number of indexbits = $\log_2$ # of cachelines

= $\log_2 2048$ = 11 bits

(c) (3 points) How many tag bits are needed for each cache entry?

Number of tag bits = bits in memory address − index bits − blockoffset bits

(−1 for missing block offset bits) = 32 − 11 − 4 = 17 bits

(d) (3 points) How many hardware comparators are needed for this cache?

1 for each parallel cache

total 4 (all or nothing)