CS 2200 Spring 2009 Test 1

Prism ID:_____

Name:_____ GTID#: 9_____

Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	9				
3	10				
4	10				
5	15				
6	20				
7	10				
8	10				
9	15				
Total	100				

- **You may ask for clarification but you are ultimately responsible for the answer you write on the paper.**
- **Illegible answers are wrong answers.**
- **Please do not discuss this test by any means (until 5 pm today)**
- **Please look through the entire test before starting. WE MEAN IT!!!**

Good luck!

1. (1 point, 1 min) (circle one – you get a point regardless of your choice)

Paper or plastic?:

(a) Paper
(b) Plastic
(c) No preference,
(d) I don't care about politics

CS 2200 Spring 2009 Test 1

Prism ID:_____

Name:_____ GTID#: 9_____

Processor design

2. (10 points, 10 mins)
Given the software convention for registers:

```
      a0-a2:  parameter passing
      s0-s2:  callee saves if need be
      t0-t2:  caller saves if need be
      v0:     return value
      ra:     return address
      at:     target address
      sp:     stack pointer
```

Recall that JAL instruction of LC-2200 has the following semantics:

```
      JAL at, ra;       ra <- PC_incremented (return address)
                  ;     PC <- at (entry point of procedure)
```

The state of the stack is as shown below. To help you out, we have put down the action corresponding to saving s registers on the stack. Fill out the actions similarly for the other entries on the stack (who is responsible for the action caller/callee, and what is the action).

Your answer:

Stack

Stack Pointer→

Local Variables	
Saved s Registers	Callee saves any s registers it plans to use in the procedure
Prev Return Address	_____
Add'l Return Values	_____
Add'l parameters	_____
Saved t registers	_____

Prism ID:_____

Name:_____ GTID#: 9_____

3. (9 points, 5 mins)
What is the program counter used for? Consider both storing a value into it and saving what is in the PC somewhere else.… Be brief.

Your answer (need three valid reasons for full credit):

4. (10 points, 5 mins)(select the correct choice)
(a) An activation record of a procedure

_____ is usually on the stack

_____ is usually kept in processor registers

_____ is usually kept in a special hardware

_____ is usually allocated in the heap space of the program

_____ is usually allocated in the static (global) data space of the program

_____ all of the above

_____ none of the above

(b) A Frame Pointer

_____ is the same as a stack pointer

_____ is a fixed harness into the activation record for the currently executing procedure

_____ is not a register at all

_____ is implemented in memory

_____ is used for parameter passing during procedure call

_____ all of the above

_____ none of the above

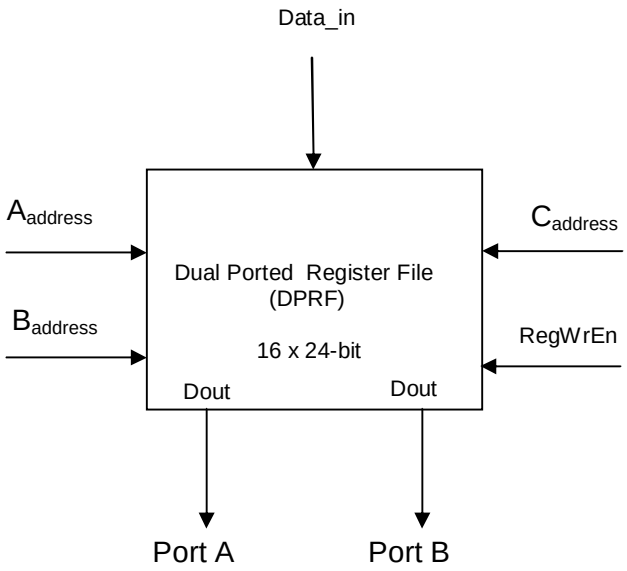
CS 2200 Spring 2009 Test 1

Prism ID:_____

Name:_____ GTID#: 9_____

Datapath elements

5. (15 points, 10 mins)
Shown below is a 16 element dual-ported register file (DPRF). Each register has 24 bits. $A_{address}$ and $B_{address}$ are the register addresses for reading the 24-bit register contents on to Ports A and B, respectively. $C_{address}$ is the register address for writing Data_in into a chosen register in the register file. RegWrEn is the write enable control for writing into the register file.



Answer the following:

(a) Data_in has _____ wires

(b) Port A has _____ wires

(c) Port B has _____ wires

(d) $A_{address}$ has _____ wires

(e) $B_{address}$ has _____ wires

(f) $C_{address}$ has _____ wires

(g) RegWrEn has _____ wires

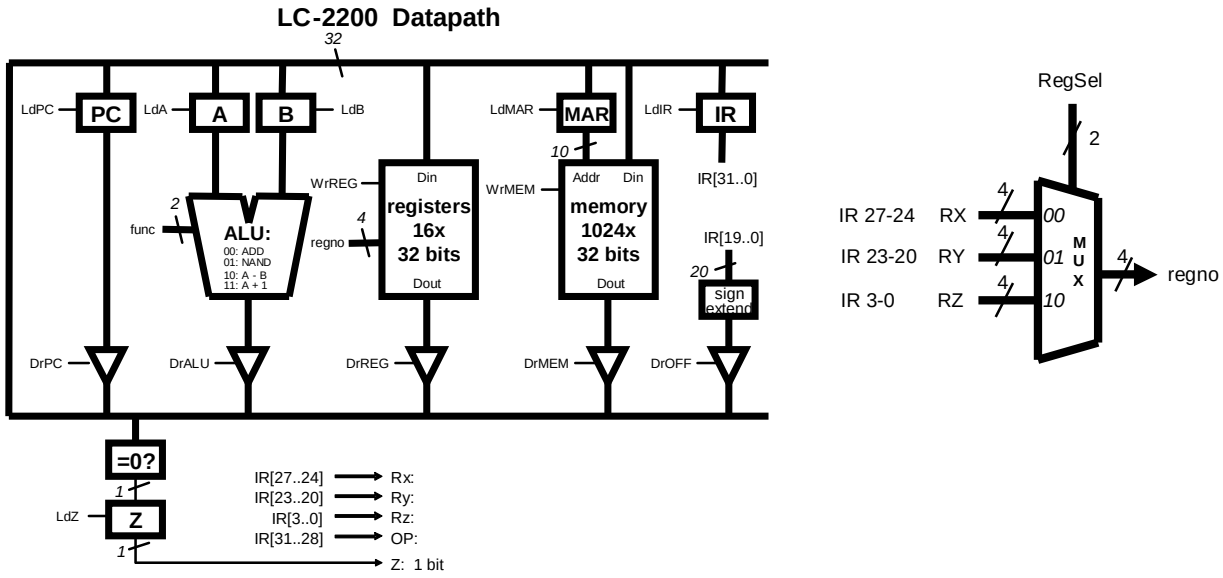
CS 2200 Spring 2009 Test 1

Prism ID:_____

Name:_____ GTID#: 9_____

Control

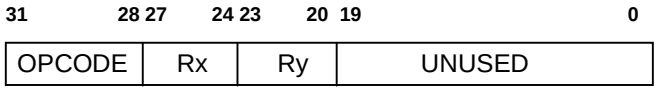
6. (19 points, 15 min)
You are given below a datapath similar to what we have discussed in class.



We have decided to add a complex instruction **POPM** to LC-2200. The semantics of this instruction is as follows:

```
POPM  Rx, (Ry++)  ;     Rx <- MEM[Ry];
                        Ry <- Ry + 1;
```

The instruction format is as shown below:



Write the sequence for implementing the POPM (you don't need to write the fetch sequence for the instruction). For each microstate, show the datapath action (in register transfer format such as A <- Rx) along with the control signals you need to enable for the datapath action (such as DrREG).

Write your answer on the next page.

Prism ID:_____

Name:_____ GTID#: 9_____

6. (Continued)

CS 2200 Spring 2009 Test 1

Prism ID:_____

Name:_____ GTID#: 9_____

Interrupts, exceptions, and traps

7. (10 points, 10 mins)

(a) Fill the table below (-1 point for each incorrect choice) with an "X" under the column that applies for a given row.

	Asynchronous with processor execution	**Synchronous with processor execution**	**Internal to the processor**	**External to the processor**
Exception				
Trap				
Interrupt				

(b) (no penalty for incorrect answer)

An example for exception:

An example for trap:

An example for interrupt:

CS 2200 Spring 2009 Test 1

Prism ID:_____

Name:_____ GTID#: 9_____

Performance

8. (10 points, 10 mins)
Based on typical workloads, HAL engineers figured out the following dynamic instruction frequencies for the three types of instructions:

A – 40%
B – 20%
C – 20%

Two engineering teams independently design processors for the same instruction set and come out with the following designs:

Ma:

Clock cycle time = 1 ns

Type	CPI
A	5
B	3
C	2

Mb:

Clock cycle time = 1.5 ns

Type	CPI
A	4
B	2
C	2

(a) Which machine is faster?

(b) what is the speedup of the faster machine over the slower machine

(c) what is the percentage improvement in the execution time of the faster machine over the slower machine?

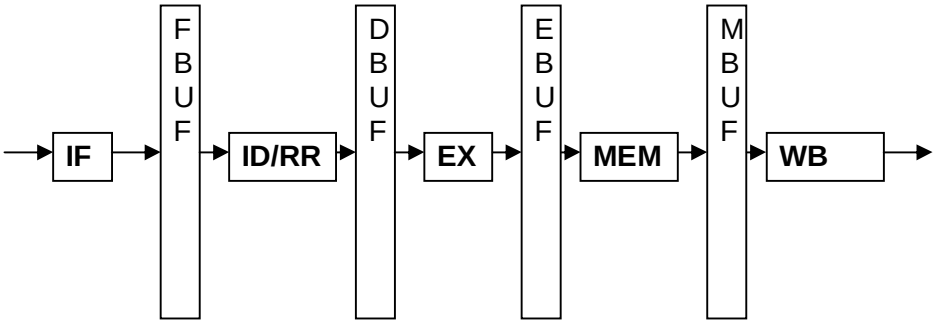
CS 2200 Spring 2009 Test 1

Prism ID:_____

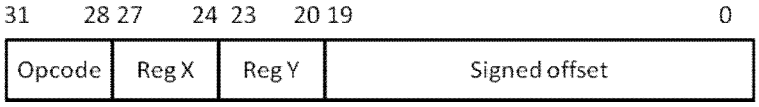
Name:_____ GTID#: 9_____

Pipelining

9. (15 points, 10 mins)
For the LC-2200 instruction set we are considering a pipelined processor design using a 5-stage pipeline as shown below



Assume the instruction going through the pipeline is
SW Rx, Ry, offset; MEM[Ry + signed offset] <- Rx



Considering only the SW instruction, show each item that must be stored in each of the pipeline registers along with its size in bits. You may assume the opcode is in all four of the registers

FBUF (IF:ID/RR)

DBUF (ID/RR:EX)

EBUF (EX:MEM)

MBUF (MEM:WB)