

# CS 2200 Spring 2009 Test 2 Section A

Prism ID: \_\_\_\_\_

Name: \_\_\_\_\_ GTID#: 9 \_\_\_\_\_

Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	10				
3	10				
4	10				
5	20				
6	12				
7	12				
8	12				
9	13				
Total	100				

- You may ask for clarification but you are ultimately responsible for the answer you write on the paper.
- Illegible answers are wrong answers.
- Please do not discuss this test by any means (until 5 pm today)
- Please look through the entire test before starting. WE MEAN IT!!!

**Illegible answers are wrong answers.**

Good luck!

## Icebreaker

1. (1 point, 1 min)

Name at least 2 teams that are still alive in the NCAA tournament

a.) \_\_\_\_\_

b.) \_\_\_\_\_

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## General

2. (10 points)

Fill in the table with your best guess as to whether the topic in the left hand column is a function carried out by the: hardware/architecture or software (including compilers and OS). We have started you off with the first two in the table.

Topic	Hardware/Architecture	Software (OS, compiler, ...)
Compilation		√
Instruction set design	√	
Control unit design		
Processor scheduling		
Page fault recognition		
Page replacement algorithm		
Cache hit/miss recognition		
Cache replacement algorithm		
VA to PA address translation		
Page table set up		
TLB lookup		
Context switching		

## Memory

3. (10 points)

(a) (select one of the following)

In most modern day operating systems

1. There is exactly one program in residence in memory at any point of time
2. There are multiple programs in residence in memory at any point of time
3. There is exactly one program but multiple processes in residence in memory at any point of time
4. All of the above
5. None of the above

(b) (select one of the following)

Once a program is run, there could be

1. Exactly one active entity called a process
2. Multiple active entities called threads
3. Two active entities, one a thread and the other a process
4. Three active entities, one a task, the second a thread, and third a process
5. Four active entities, one a job, the second a task, the third a thread, and the fourth a process

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## Pipelining

4. (10 points)

(a) (5 points) (select one correct choice)

Branch target buffer is

- (a) An area of memory reserved for branch instructions
- (b) A hardware device that keeps the outcome and target addresses of recent branches encountered during the program execution
- (c) A hardware device that is pre-loaded before the program starts with the expected outcome and the target addresses of the branches in the program
- (d) An extra stage in the pipeline for efficient handling of control hazards
- (e) None of the above
- (f) All of the above

(b) (5 points)

$I_1: R1 \leftarrow R2 + R3$

$I_2: R4 \leftarrow R1 + R5$



If  $I_2$  is immediately following  $I_1$  in the pipeline **with no forwarding** it will results in

- 1. Zero bubbles
- 2. One bubble
- 3. Two bubble
- 4. Three bubbles
- 5. None of the above

You may optionally use this table to help determine the correct answer

IF	ID/RR	EX	MEM	WB

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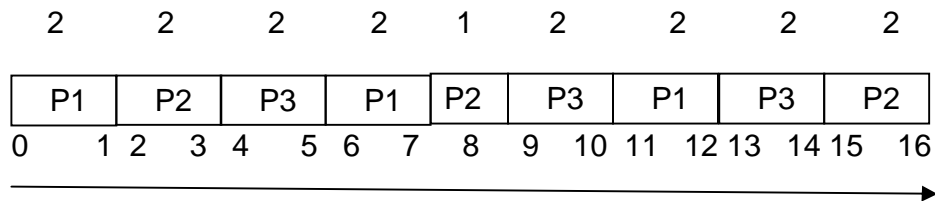
## Process Scheduling

5. (20 points)

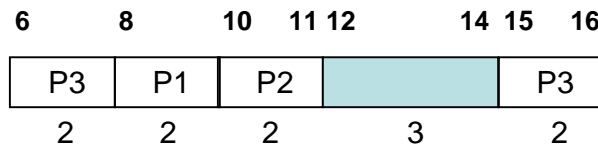
Given the following schedule for three processes (starts at time = 0):

Note P1 completes at  $t = 12$  (i.e., it takes a total of 13 time units to complete), P2 completes at  $t = 16$ , and P3 completes at  $t = 16$ .

### CPU Schedule



### I/O Schedule



(a) What is the average waiting time experienced by the processes in the above schedule?

(b) What is the average throughput of the system?

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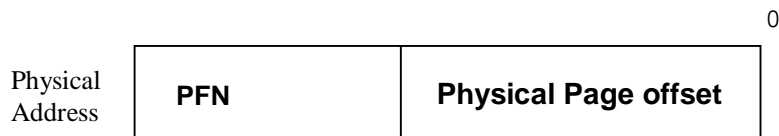
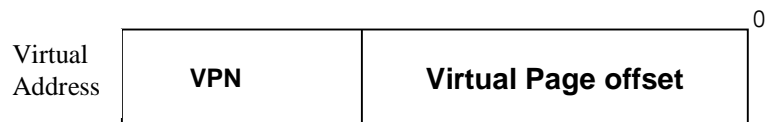
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## Memory

6. (12 points)

Consider a memory system with 40-bit virtual addresses and 32-bit physical addresses. The page size is 8 KB.

- (a) Assuming little-endian notation show the bit positions occupied by the VPN, Virtual Page Offset, PFN, and the Physical Page Offset in the figures below.



- (b) How many entries are there in the page table?

- (c) How many page frames are there in the memory system?

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## Memory

7. (12 points)

During the time interval  $t_1 - t_2$ , the following virtual page accesses are recorded for the three processes P1, P2, and P3, respectively.

P1: 0, 10, 1, 0, 1, 2, 10, 2, 1, 1, 0

P2: 0, 100, 101, 102, 103, 0, 101, 102, 104

P3: 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5

a) What is the **working set** for each of the above three processes for this time interval?

P1:

P2:

P3:

b) What is the **cumulative memory pressure** on the system during this interval?

## Memory

8. (12 points)

(a) Matching: Next to each of the page replacement policies, place the hardware assist needed from the following choices :

### Oracle

Push down stack

Reference bit per page

A. True LRU

B. Belady's Min (Optimum)

C. Clock (second chance)

\_\_\_\_\_  
\_\_\_\_\_  
\_\_\_\_\_

(b) Associate definitions below (A, B, C) with the type of miss choosing from

**compulsory miss,**

**conflict miss,**

**capacity miss.**

A. Miss incurred when the cache is full \_\_\_\_\_

B. Miss incurred since memory location accessed for the first time by CPU \_\_\_\_\_

C. Miss incurred due to limited associativity even though the cache is not full \_\_\_\_\_

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## Caching

9. (13 points)

A pipelined processor has an average CPI of 1.5 not considering memory effects. On an average each instruction incurs a cache read miss rate of 1%, and cache write miss rate of 0.5%. The read miss penalty is 100 cycles and the write miss penalty is 5 cycles. What is the effective CPI taking into account memory stalls?