CS 2200 Spring 2008 Test 1

Name:____Kishore_____GT Number: gt_____

Please indicate your GT number in the grid below so we have some chance of being able to read it.

G											
t											
0	1	2	3	4	5	6	7	8	9	0	e	g
0	1	2	3	4	5	6	7	8	9	0		
0	1	2	3	4	5	6	7	8	9	0		
0	1	2	3	4	5	6	7	8	9	0		

a	B	c	d	e	F	G	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z

Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	9				
3	10				
4	10				
5	15				
6	20				
7	10				
8	10				
9	15				
Total	100				

- **You may ask for clarification but you are ultimately responsible for the answer you write on the paper.**
- **Illegible answers are wrong answers.**
- **Please look through the entire test before starting. WE MEAN IT!!!**

Good luck!

1. (1 point, 1 min) (circle one – you get a point regardless of your choice) The number of delegates needed to win the presidential primary:
(a) same for republican and democratic candidates, **(b) different for republican and democratic candidates**, (c) no idea, (d) I don't care about politics

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Processor design
2. (10 points, 10 mins)
Given the software convention for registers:

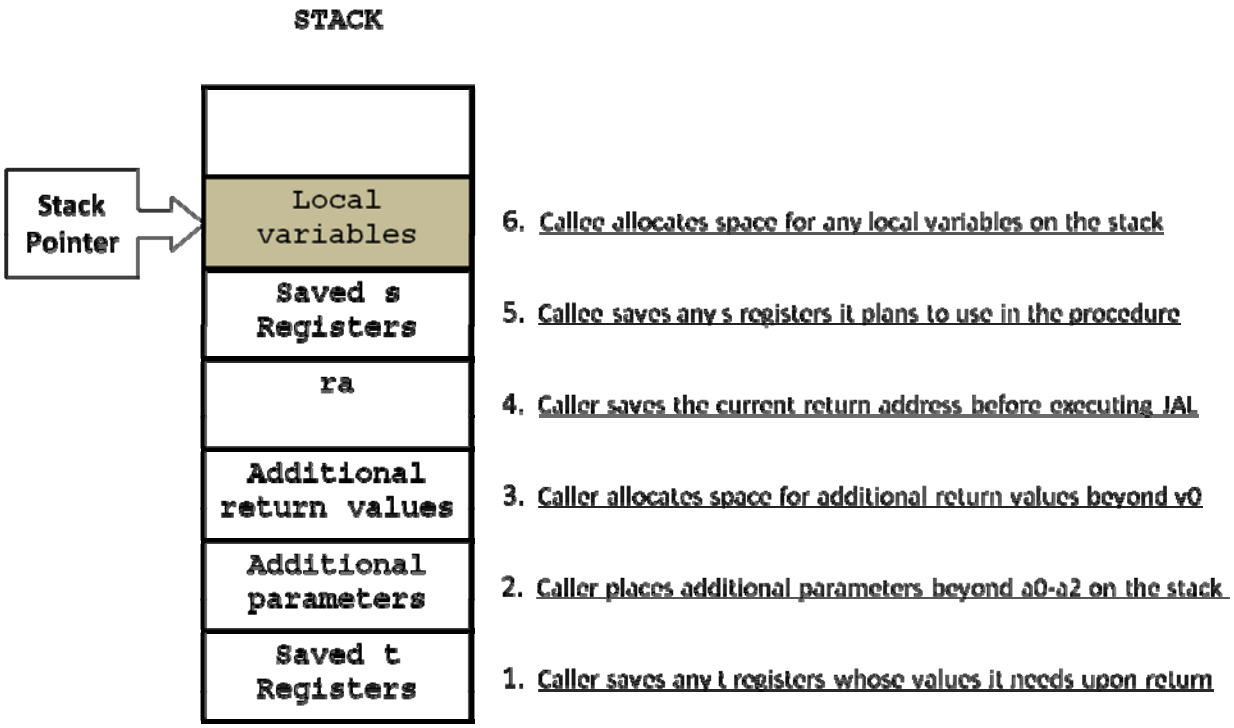
```
      a0-a2:  parameter passing
      s0-s2:  callee saves if need be
      t0-t2:  caller saves if need be
      v0:     return value
      ra:     return address
      at:     target address
      sp:     stack pointer
```

Recall that JAL instruction of LC-2200 has the following semantics:

```
      JAL at, ra;       ra <- PC_incremented (return address)
                  ;     PC <- at (entry point of procedure)
```

The state of the stack is as shown below. To help you out, we have put down the action corresponding to step 6. Fill out the actions similarly for the other steps (who is responsible for the action caller/callee, and what is the action).

Your answer:



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3. (9 points, 5 mins)
Why does an architecture provide a register called Program Counter (PC)?

Your answer (need three valid reasons for full credit):

1) **Need to know where to return to after a procedure call**

2) **Need to know where to jump to on branches and procedure calls**

3) **Need to know where to resume execution of a program after an interrupt**

4. (10 points, 5 mins)(select the correct choice)
(a) An activation record of a procedure

___**X**___ is usually on the stack

_____ is usually kept in processor registers

_____ is usually kept in a special hardware

_____ is usually allocated in the heap space of the program

_____ is usually allocated in the static (global) data space of the program

_____ all of the above

_____ none of the above

(b) A Frame Pointer

_____ is the same as a stack pointer

___**X**___ is a fixed harness into the activation record for the currently executing procedure

_____ is not a register at all

_____ is implemented in memory

_____ is used for parameter passing during procedure call

_____ all of the above

_____ none of the above

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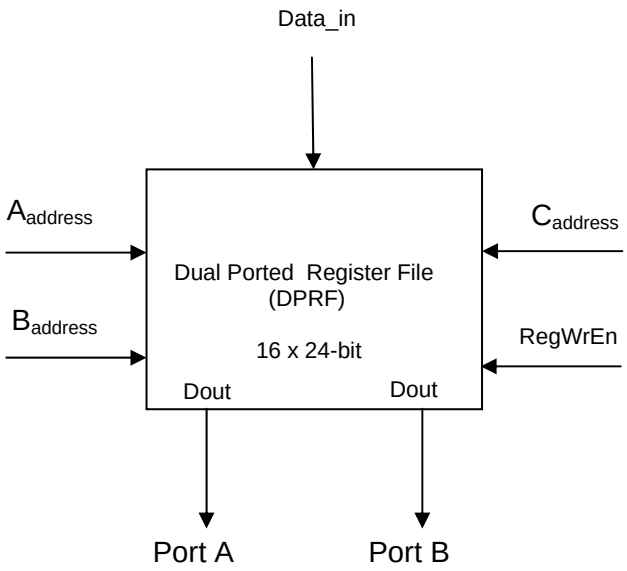
Datapath elements

5. (15 points, 10 mins)

Shown below is a 16 element dual-ported register file (DPRF). Each register has 24 bits. $A_{address}$ and $B_{address}$ are the register addresses for reading the 24-bit register contents on to Ports A and B, respectively. $C_{address}$ is the register address for writing Data_in into a chosen register in the register file. RegWrEn is the write enable control for writing into the register file.



Answer the following:

(a) Data_in has _____**24**_____ wires

(b) Port A has _____**24**_____ wires

(c) Port B has _____**24**_____ wires

(d) $A_{address}$ has _____**4**_____ wires

(e) $B_{address}$ has _____**4**_____ wires

(f) $C_{address}$ has _____**4**_____ wires

(g) RegWrEn has _____**1**_____ wires

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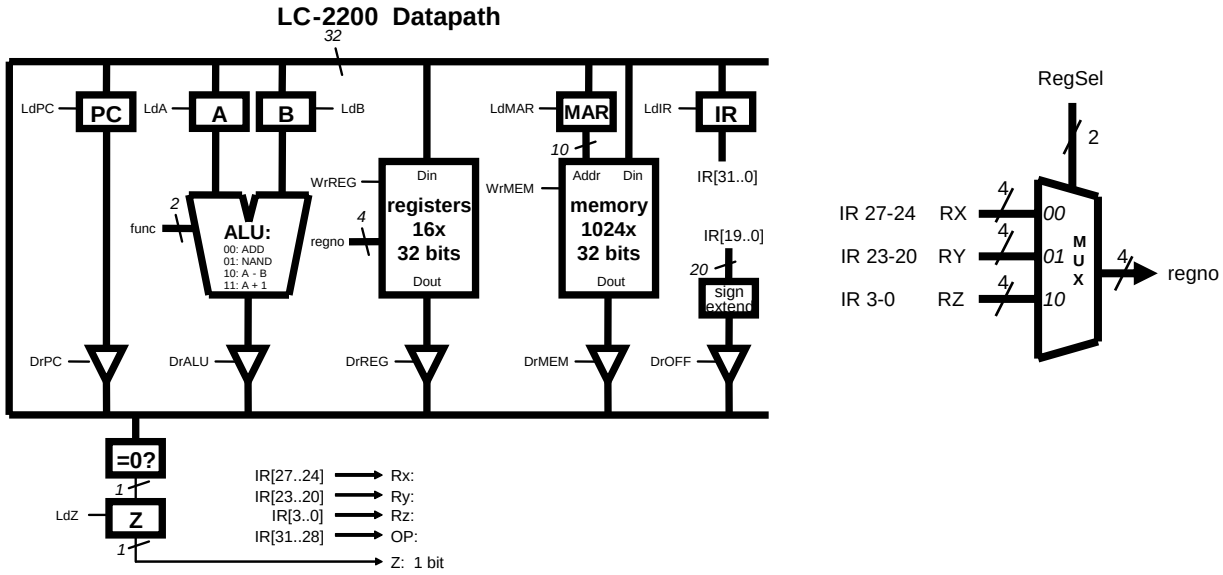
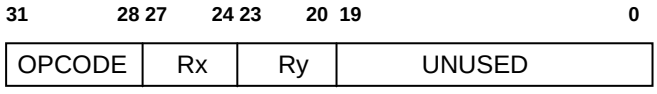
Control
6. (19 points, 15 min)
You are given below a datapath similar to what we have discussed in class.



We have decided to add a complex instruction **ADDM** to LC-2200. The semantics of this instruction is as follows:

```
ADDM  Rx, (Ry)    ;     MEM[Ry] <- MEM[Ry] + Rx;
```

The instruction format is as shown below:



Write the sequence for implementing the ADDM (you need to write the sequence **ONLY** for the execution macro state of the instruction). For each microstate, show the datapath action (in register transfer format such as A ← Rx) along with the control signals you need to enable for the datapath action (such as DrREG).

Write your answer on the next page.

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Addm1:
Ry -> MAR
Control signals needed:
RegSel = 01
DrREG
LdMAR

Addm2:
MEM[MAR] -> A
Control signals needed:
DrMEM
LdA

Addm3:
Rx -> B
Control Signals needed:
RegSel = 00
DrREG
LdB

Addm4: (NOTE: MAR already has the memory address pre-loaded from Addm1 state)
A+B -> MEM[MAR]
Control signals needed:
func = 00
DrALU
WrMEM

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Interrupts, exceptions, and traps
7. (10 points, 10 mins)

(a) Fill the table below (-1 point for each incorrect choice) with an "X" under the column that applies for a given row.

	Asynchronous with processor execution	**Synchronous with processor execution**	**Internal to the processor**	**External to the processor**
Exception		**X**	**X**	
Trap		**X**	**X**	
Interrupt	**X**			**X**

(b) (no penalty for incorrect answer)

An example for exception:**Divide by zero**

An example for trap: **System calls**

An example for interrupt:**Device I/O (example: keyboard)**

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Performance

8. (10 points, 10 mins)
Based on typical workloads, HAL engineers figured out the following dynamic instruction frequencies for the three types of instructions:

A – 40%
B – 20%
C – 20%

Two engineering teams independently design processors for the same instruction set and come out with the following designs:

Ma:

Clock cycle time = 1 ns

Type	CPI
A	5
B	3
C	2

Mb:

Clock cycle time = 1.5 ns

Type	CPI
A	4
B	2
C	2

(a) Which machine is faster?

Let E_a and E_b be the normalized execution times of Ma and Mb.

$E_a = (N_A * CPI_A + N_B * CPI_B + N_C * CPI_C)_a * CYCLE\text{-}TIME_a$
$= (0.4 * 5 + 0.2 * 3 + 0.2 * 2) * 1$ ns
$=$ 3 ns

$E_b = (N_A * CPI_A + N_B * CPI_B + N_C * CPI_C)_b * CYCLE\text{-}TIME_b$
$= (0.4 * 4 + 0.2 * 2 + 0.2 * 2) * 1.5$ ns
$= 2.4 * 1.5$ ns
$=$ 3.6 ns

Ma is faster than Mb

(b) what is the speedup of the faster machine over the slower machine

Speedup of Ma over Mb = execution time of Mb/execution time of Ma
= 3.6/3
= 1.2

(c) what is the percentage improvement in the execution time of the faster machine over the slower machine?

Percentage improvement of Ma over Mb
= (difference in execution time/execution time on Mb) * 100
= ((3.6-3)/3.6)* 100 = (0.6/3.6) * 100 = 16.6%

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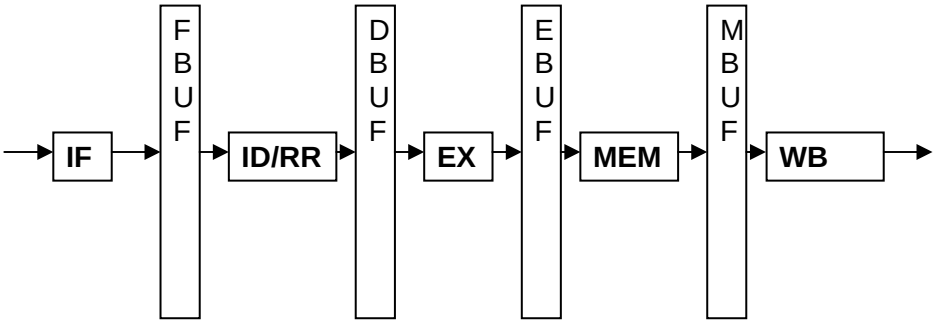
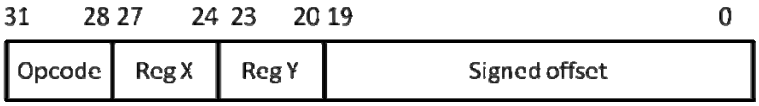
Pipelining
9. (15 points, 10 mins)
For the LC-2200 instruction set we are considering a pipelined processor design using a 5-stage pipeline as shown below



Assume the instruction going through the pipeline is
LW Rx, Ry, offset; Rx <- MEM[Ry + signed offset]



Considering only the LW instruction, quantify the sizes of the various buffers between the stages of the above pipeline.

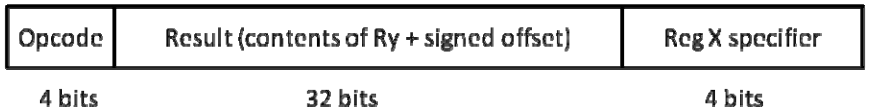
Your answer:

Size of FBUF (same as the size of an instruction in LC-2200) = 32 bits

Size of DBUF:
Contents of DBUF

(Note: it is OK if students show contents of Rz in DBUF as well)
Size = 60 bits (92 bits if they show contents on Rz in DBUF)

Size of EBUF:
Contents of EBUF



Size = 40 bits

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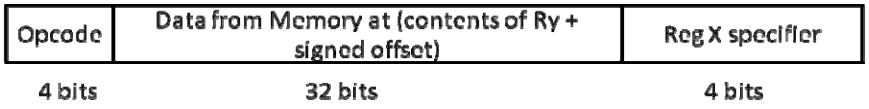
Size of MBUF:
Contents of MBUF



Size = 40 bits