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Name:_____Kishore_____GT Number: _____

Problem	Points	Lost	Gained	Running Total	TA
1	1				
2	10				
3	15				
4	15				
5	5				
6	10				
7	5				
8	10				
9	10				
10	10				
11	9				
Total	100				

You may ask for clarification but you are ultimately responsible for the answer you write on the paper.

Please look through the entire test before starting. WE MEAN IT!!!

Illegible answers are wrong answers.

Show your work in the space provided to get any credit for problem-oriented questions.

Good luck!

1. (1 point, 1 min)
Atlanta Hawks have not made it to their division finals during playoffs since
a) 1969-70
b) 2009-2010
c) 1957-58
d) They came to Atlanta
e) Who are Atlanta Hawks?
f) What is playoff?

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Memory management

2. (10 points, 5 mins)

a) (2 points) During the time interval t1–t2, the following virtual page accesses are recorded for the three processes P1, P2, and P3, respectively:

- P1: 0, 25, 1, 0, 1, 2, 10, 2, 1, 1, 0 — 5
- P2: 0, 1, 101, 102, 103, 0, 1, 104, 105, 106 — 8
- P3: 0, 1, 2, 3, 4, 5, 0, 1, 2, 3, 4, 5 — 6

The cumulative memory pressure is (circle one)

1. 33
2. 11
3. 12
4. 10
5. 19

b) (2 points) To implement paging the minimum additional hardware needed in the CPU data path (circle one)

1. One Page table implemented in hardware
2. Multiple page table (one per process) implemented in hardware
3. One Page Table Base Register (PTBR)
4. Multiple PTBR (one per process)
5. None of the above

c) (2 points) External fragmentation occurs in the following memory management policies (circle one)

1. Fixed size partitions
2. Variable size partitions
3. Paging
4. (1) and (2)
5. (2) and (3)
6. (1) and (3)
7. (1), (2), and (3)

d) (2 points) Virtual address 20 bits; page size 1K bytes. Number of entries in the page table (circle one)

1. 2048
2. 1024
3. 2^{20}
4. Cannot determine with the given data

e) (2 points) Physical address 24 bits; page size 8K bytes; Maximum number of physical page frames possible (circle one)

1. 1024
2. 2048
3. 2^{24}
4. 8K
5. Cannot determine with the given data

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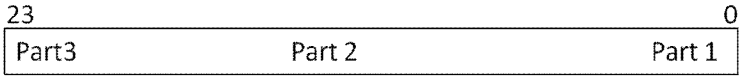
Cache

3. (15 points, 15 min)

a) (6 points)

A computer has the following characteristics:

- It is **word-addressed** and the address is 24 bits long (little endian)
- It has a **direct-mapped cache** with each block holding 32 words of data
- The direct-mapped cache has **2048 sets**



The above figure shows how the address is divided into three parts to perform a cache access. Name the parts (below) and the number of bits associated with each part.

Part 1: Offset (name) 5 (number of bits)

Part 2: Index (name) 11 (number of bits)

Part 3: tag (name) 8 (number of bits)

(+1 for each correct)

b) (5 points)

A fully associative cache is initially empty, has only four blocks, and uses the **FIFO replacement policy**. The processor performs a total of eight accesses, to memory blocks A, B, C, D, A, E, A, and B, in that order. For each of these accesses, specify (by filling in the table below) whether it is a cache hit or a cache miss, and the memory block evicted (if any).

Memory Access	Hit/miss	Block evicted from cache
A	Miss (cold)	-
B	Miss (cold)	-
C	Miss (cold)	-
D	Miss (cold)	-
A	Hit	-
E	Miss (cold)	A
A	Miss (capacity)	B
B	Miss (capacity)	C

+1 +1 +1 +1 +1

+0.5 for each

c) (2 points) Average CPI = 1.5; average cache miss per instruction = 3%; miss penalty = 20. The effective CPI is

1. 1.8
2. 2.1
3. 21.5
4. 7.5

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d) (2 points) Temporal locality suggest that
1. Once brought into the cache, we should keep the data around as long as possible
2. On a miss, we should bring in adjacent memory locations into the cache
3. The memory location being brought in due to a miss is not likely to be referenced in the future
4. None of the above

Input/Output

4. (15 points, 10 min)

a) Given the following specifications for a disk drive:

256 bytes per sector
12 sectors per track
20 tracks per surface
3 Platters
2 surfaces per platter
Seek time 20 ms
Rotational speed 3600 RPM

i)(2 points) What is the total capacity of such a drive in bytes assuming normal recording?

3 * 2 * 20 * 12 * 256 = 360K bytes (where K = 1024)

(all or nothing)

ii)(3 points) Assume a zoned bit recording with 3 zones
Zone 3 (outermost): 8 tracks, 18 sectors per track
Zone 2: 7 tracks, 14 sectors per track
Zone 1: 5 tracks, 12 sectors per track

What is the total capacity of this drive with the zoned-bit recording?

3 * 2 * (8 * 18 + 7 * 14 + 5 * 12) * 256 bytes
= 3 * (72 + 49 + 30) K bytes
= 3 * 151 K Bytes
= 453 K bytes (where K = 1024)

+2 for this

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iii) (6 points) Assuming normal recording, calculate the average time needed to read 2 contiguous sectors from the same track (Note: the head can be anywhere).

Average time to seek to the cylinder = 20 ms
Rotational latency = 1/3600 min = 16.66 ms
Average rotational latency to get to the desired sector = 16.66/2 ms
In one revolution the head reads 12 sectors,
Therefore, the time to read one sector = 16.66/12 ms = 1.39 ms
Time to read 2 consecutive sectors = 2 * (16.66/12) ms = 2.78 ms

Putting all this together, the time to read two consecutive sectors
= seek time + average rotational latency + time to read two sectors
= 20 ms + 8.33 ms + 2.78 ms
= 31.11 ms

b) (2 point) Give an example of a synchronous I/O device and an example of an asynchronous I/O device.

Asynchronous -> Keyboard
Synchronous -> Disk

c) (2 points) Programmed transfer
1. Refers to the processor being able to access memory directly
2. Refers to the device controller being able to move data from/to the device to/from the memory directly
3. Refers to the processor moving the data from/to the device to/from the memory using load/store instructions
4. None of the above

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Disk Scheduling

5. (5 points, 10 min)
Given the following:
Total number of cylinders in the disk = 1024
Current head position is at cylinder 78, and before that it was 71.
Current requests in order of arrival =
768, 20, 513, 69, 104, 745, 25, 320, 99

a) (1 point) Show the order in which these requests are serviced using FCFS

768, 20, 513, 69, 104, 745, 25, 320, 99

(all or nothing)

b) (2 points) Show the order in which these requests are serviced using SSTF

69, 99, 104, 25, 20, 320, 513, 745, 768

(all or nothing)

c) (2 points) Show the order in which these requests are serviced using LOOK

99, 104, 320, 513, 745, 768, 69, 25, 20

(all or nothing)

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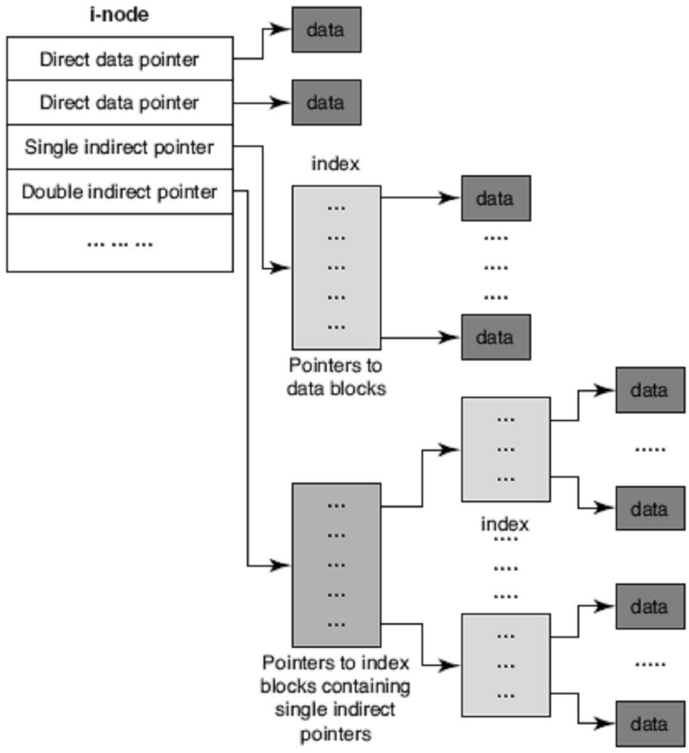
File Systems

6. (10 points, 15 mins)
Given the following:
Size of index block = 1024 bytes
Size of Data block = 1024 bytes
Size of pointer = 8 bytes (to index or data blocks)

The i-node consists of
2 direct data block pointers,
1 single indirect pointer, and
1 double indirect pointer.

Note that the index blocks and data blocks are allocated on a need basis. An index block is used for the i-node as well as for the index blocks store pointers to other index blocks and data blocks (see Figure).



a) (2 points) How many pointers does each index block contain?

Number of pointers = 1024 / 8 = 128 **(all or nothing)**

b) (2 points) How many data blocks are used to store a 2 MB file?

Number of data blocks = size of file / size of data block
= 2 * 2^{20} bytes / 2^{10} bytes
= 2048
(-1 for minor mistake)

c) (3 points) How many index blocks (including the i-node for the file) are needed to store a 2 MB file?

We need metadata to access 2048 data blocks for a 2 MB file
1 i-node (gets you access to 2 data blocks) **(+1)**
1 index block for single level indirect (1st level) **(+1)**
(gets you access to 128 data blocks)
1 index block for double level indirect (2nd level) **(+1)**
We need to get to (2048-130 =) 1918 data blocks from here
This requires 15 more 1st level index blocks
(14 1st level index blocks gets you access to 1792 data blocks, plus you need 1 more 1st level index block to access the remaining 126 data blocks)

Total number of index blocks needed = 18

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d) (3 points) What is the largest file size that can be supported in this file system?

Direct data blocks = 2 (1)
1st level indirect data blocks = 128 (2)
2nd level indirect data blocks = 128 * 128 (3)

Largest size file that can be supported by the system
= ((1) + (2) + (3)) 1024 bytes
= (2 + 128 + 128*128) Kbytes (where K = 1024)
= (2+128+16384) K bytes
= 16514 KBytes

7. (5 points, 5 min)

Notes:

- Unix **"touch file1"** command creates a zero byte new file
- Unix **"ln file1 file2"** command creates a hard link
- Unix **"ln –s file1 file2"** command creates a sym link

Fill in the table below. The reference count in the table pertains to the i-node that is affected by the command in that row. If a new i-node is created, show the old reference count for that i-node as 0.

Command	New i-node created (yes/no)	Reference count old	new
touch f1	Yes	-	1
ln –s f1 f2	Yes	-	1
ln –s f2 f3	Yes	-	1
ln f1 f4	No	1	2
ln f4 f5	No	2	3

Use this area for rough work for this question.

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Parallel Systems

8. (10 points, 10 min)
In a parallel program, it is frequently necessary to divide a range of elements among threads. For example, if four threads are used to zero out all elements of array A which has a 1000 elements numbered 0 through 999, one thread can zero out elements 0 through 249, another zeores out elements 250 through 499, still another initializes elements 500 through 749, and the remaining threads initializes elements 750 through 999. However, each thread needs to know which part of the array to process. Instead of writing different code for each thread, we can use a **shared counter variable** to assign an index to each thread. The counter starts at value zero. Each thread reads its index value from the counter and then increments the counter. The following code snippet shows the static initialization of the counter and the function called by each thread.

```
int counter = 0; /* shared counter initialized to 0 */

/* This is the function called by each thread */
void threadfun(void){
  int myindex;

  myindex = counter;
  counter++;

  // Now zero out my part of the array
  for(i = 0; i < 249; i++)
    a[myindex*250 + i] = 0;
}
```

a) (5 points)
What is the problem with the above code?

Unsynchronized access to counter variable by multiple threads
(all or nothing)

b) (5 points) How can you fix the above code with minimal loss of concurrency?

Put mutex lock around access to counter:

```
mutex_lock m1;      /* new variable visible to all theads */

Lock(m1);
      myindex = counter;
      counter++;
Unlock(m1)
```

(+1 for recognizing need for mutex)
(+5 for correct solution)

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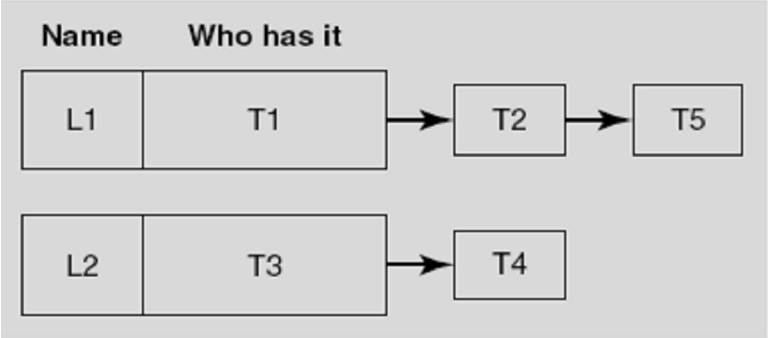
9. (10 points, 10 min)

a) (5 points) Assume that the following events happen in the order shown (T1–T5 are threads of the same process):

T1 executes thread_mutex_lock(L1);
T2 executes thread_mutex_lock(L1);
T3 executes thread_mutex_lock(L2);
T4 executes thread_mutex_lock(L2);
T5 executes thread_mutex_lock(L1);

Assuming that there have been no other calls to the threads library prior to this, show the state of the internal queues in the threads library after the given five calls.



(+1 for each thread in right spot)

b) (3 points) Fill in the blanks using a subset of the following phrases exactly once.

Hardware **operating system** **page table** **cache** **registers**

In an SMP that supports hardware cache coherence, the _hardware_____ is responsible for ensuring that the copies of the same memory location in the different caches are kept consistent; the __operating system_____ is responsible for ensuring that the TLBs in the different processors are kept consistent; the _____page table__ is shared among all the threads of the same process.

c) (2 points) Deadlock (choose one of the following)

1. Is a condition where threads are not using mutex locks
2. Is a condition where all the locks variables are in use
3. A lock variable that is dead
4. Is a condition where one or more threads are waiting for an event that will never happen
5. None of the above

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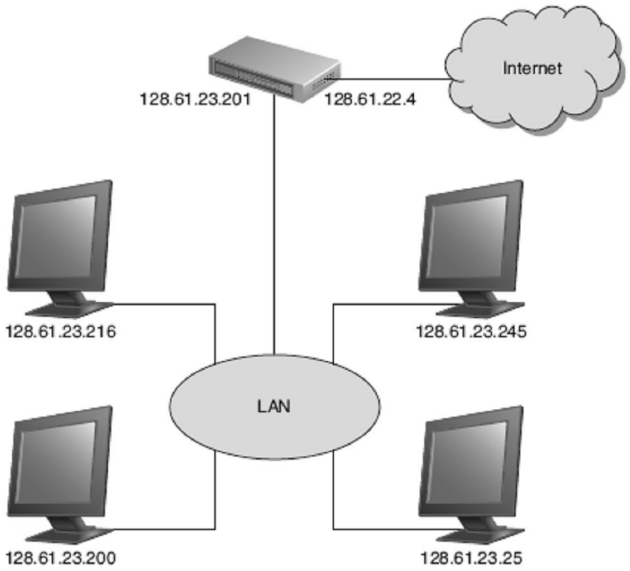
Networking
10. (10 points)
a) (2 points) How many IP Networks are there in the following Figure? Assume that the top 24 bits of the 32-bit address name an IP network.



Your answer:

Two (128.61.23/24 and 128.61.22/24 are the two IP networks)
(all or nothing)

b) (2 points) (**Answer True/False with justification**) Circuit switching results in inefficient use of network resources.

True. Network resources are allocated individually for each circuit leading to a lot of "dead time" on the links.
(+1 for T/F; +1 for justification)

c) (2 points)(**Answer True/False with justification)** Message switching and packet switching mean exactly the same thing.

False. Message switching is at the granularity of an entire message; packet switching is at the granularity of packets that are part of the same message.
(+1 for TF; +1 for justification)

d) (2 points) The sequence number in a packet
1. Gives the destination address
2. Is needed for message reconstruction at the destination
3. Assures the integrity of the packet
4. Is computed using cyclic redundancy check (CRC) algorithm
5. Is the same for every packet in a given message

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e) (2 points) Fill in the blanks using a subset of the following phrases exactly once.

Ethernet **Token ring** **Stop-and-wait** **IP** **TCP**

In a LAN, under high load, __token ring_____ protocol would result in a better performance; under light load, __ethernet_____ protocol would result in a better performance.

11. (10 points, 10 min)
a) (4 points) Given the following:
Message size = 100,000 bytes
Header size per packet = 100 bytes
Packet size = 1100 bytes

How many packets are needed to transmit the message assuming a 10% packet loss? Ignore fractional packet loss. Ignore ACKs. Show your work for partial credit.

Payload in each packet = packet size – header = 1100 – 100 = 1000 bytes
Number of data packets to be sent = message size / payload
= 100,000/1000
= 100

Packets sent	Lost	successful
100	10	90
10	1	9
1	0	1 (data transmission complete)

Total number of packets sent = 111

b) (5 points)
A message has 10 packets, and the RTT is 2 msec. Assuming that the time to send/receive the packet and the ACK are negligible compared with the propagation time on the medium, and given no packet loss, how much time is required to complete the transmission with the sliding window protocol with a window size of 5?

RTT = 2 msec.
The source sends a window of 5 packets and then waits for the ACK.
The first ACK is received 2 msec after the first packet is sent.
Therefore, in one cycle of 2 msec (RTT), the source has successfully completed transmission of 5 packets (since we are ignoring all other times except the propagation time on the medium).
Two such cycles are needed to complete the transmission.
The total time for the message transmission = 2 * RTT = 2 * 2 msec = 4 msec.