CS 2200 Spring 2012 Test 1

Prism ID:_____

Name:_____Kishore _____ GTID#: 9_____

Problem	Points	Lost	Gained	Running Total	TA
1	1 (0 min)				
2	15 (5 min)				
3	10 (5 min)				
4	21 (15 min)				
5	20 (10 min)				
6	15 (5 min)				
7	18 (10 min)				
Total	100 (50 min)				
8. Bonus Question	4				

- **You may ask for clarification but you are ultimately responsible for the answer you write on the paper.**
- **Illegible answers are wrong answers.**
- **Please look through the entire test before starting. WE MEAN IT!!!**

Good luck!

1. (1 point, 0 min) (select one)

This class meets from 11 to noon in

- The fish bowl
- Smith 245
- Klaus 1443
- CCB 16
- It meets?
- All lectures are on video, so no live lectures

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Processor design

2. (15 points, 5 mins) (circle the correct choice in each of the following)

a) Saving and restoring of registers on a procedure call…

(i) Is always done by the caller
(ii) Is always done by the callee
(iii) Is never done since hardware magically takes care of it
(iv) Is done on a need basis partly by the caller and partly by the callee

b) Local variables in a procedure….

(i) Are usually allocated on the stack
(ii) Are usually kept in processor registers
(iii) Are usually kept in a special hardware
(iv) Are usually allocated in the heap space of the program
(v) Are usually allocated in the static (global) data space of the program

c) Frame pointer…

(i) Is another name for stack pointer
(ii) Changes every time items are pushed and popped on the stack
(iii) Changes every time local variables for a procedure are allocated on the stack
(iv) Is a fixed harness into the activation record of a currently executing procedure

d) An Instruction Set….

(i) Serves as a level of abstraction between software and hardware
(ii) Provides the details of the machine implementation
(iii) Deals with the datapath and control of the processor
(iv) Is decided by the amount of silicon available in the processor

e) Endianness of an architecture…

(i) Is a key determinant of processor performance
(ii) Is a key determinant of how the compiler lays out data structures in memory
(iii) Matters if one declares a datatype of a particular precision and accesses it as another precision
(iv) Signifies how many registers are available for use by the programmer

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3. (5 min) Given the following software convention for programmer visible registers:

```
a0-a2:  parameter passing
s0-s2:  callee saves if need be
t0-t2:  caller saves if need be
v0:     return value
ra:     return address
at:     target address
sp:     stack pointer
```

A. (8 points)
Which addressing mode is used for the underlined operand in each of these instructions?

```
ADDI    $v0, $t2, 12      Mode: _____Register_____
ADDI    $a0, $zero, 1     Mode: _____Immediate_____
LW      $t0, 8($sp)       Mode: _____Base+offset_____
BEQ     $a0, $a1, label   Mode: _____PC-relative_____
```

Choose from these modes: **Register, PC-relative, Base + Offset, Immediate**

B. (2 points)
Callee executes the following code to pop a saved register from the stack:

```
LW    $s0, 0($sp)
ADDI  $sp, $sp, 1
```

The stack grows toward (circle the correct choice)

a) Higher addresses b) Lower addresses c) Cannot be determined

Datapath and control

4. (15 min)

A. (6 points) There are two next-state modifiers discussed in class. The T-bit allows a two-way microbranch from the current microstate. The M-bit allows a multi-way microbranch from the current microstate. This question pertains to when those bits are enabled in the implementation of the LC-2200 ISA.

a) (circle the correct choice) The two-way modifier bit T is enabled
(i) In the first microstate of the Fetch macrostate
(ii) In the last microstate of the Fetch macrostate
(iii) In the middle of BEQ macrostate after operand comparison
(iv) In the first microstate of BEQ macrostate
(v) Always

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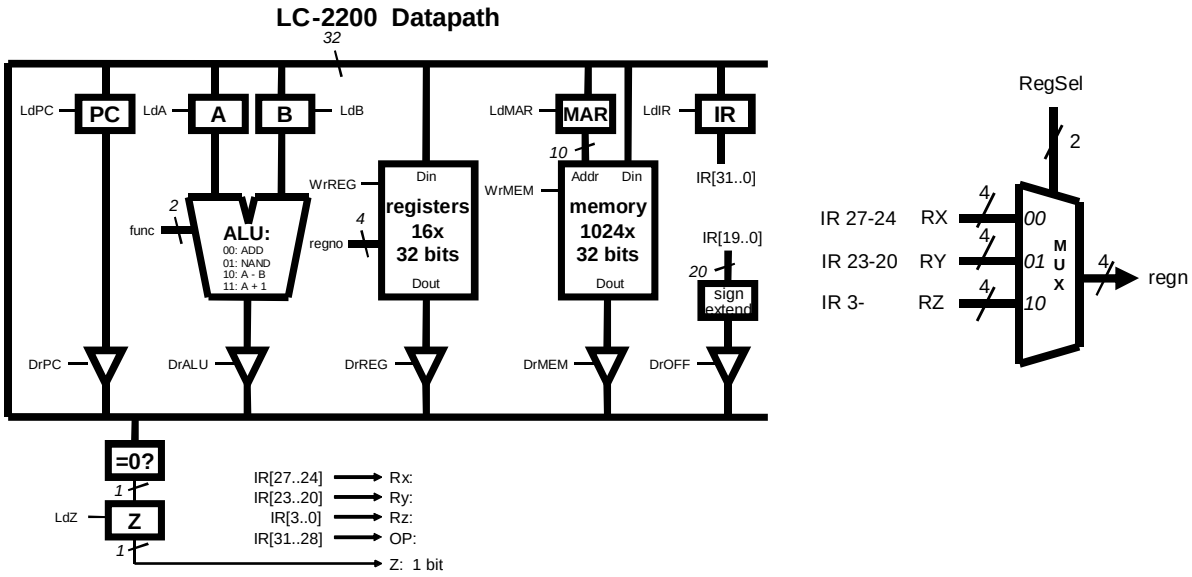
b) (circle the correct choice) The multi-way modifier bit M is enabled
(i) In the first microstate of the Fetch macrostate
(ii) In the last microstate of the Fetch macrostate
(iii) In the first microstate of every Execute macrostate
(iv) During BEQ execution
(v) Always

B. (15 points)
You are given below a datapath similar to what we have discussed in class.



We are introducing a new instruction: SUB. The syntax and semantics of the LWI instruction are as follows:

SUB Rx, Ry, Rz; Rx ← Ry - Rz;

The instruction format is as shown below:

Write the microcode sequence for the EXECUTE macro state of the SUB instruction (**you don't need to write the fetch sequence for the instruction**). For each microstate, show the datapath action (in register transfer format such as A <- Rx) along with the control signals you need to enable for the datapath action (such as DrREG).

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(SPACE FOR ANSWER TO QUESTION 4.B)

SUB1:

Ry → A
Control signals needed:
RegSel = 01
DrREG
LdA

} +5

-1 if register Xfer action not shown

SUB2:

Rz → B
Control signals needed:
RegSel = 10
DrREG
LdB

} +5

SUB3:

A-B → Rx
Control signals needed:
func = 10
DrALU
RegSel = 00
WrREG

} +5

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Interrupts

5. (5 mins)

A. (5 points)

The following actions happen in the INT macro state of the processor (**Select ALL that apply: +1 for correct choice; -1 for incorrect choice**).
(Note: There are exactly 5 correct choices)

(1) Current PC has to be saved in some known place
(2) The registers have to be saved in some known place
(3) Interrupts have to be disabled
(4) Interrupts have to be enabled
(5) Acknowledge interrupt
(6) Retrieve handler address from a known place and place it in PC
(7) Change to user mode
(8) Change to kernel mode
(9) Retrieve mode bit from the system stack
(10) Load PC from a general purpose register

B. (10 points) (circle the correct choice)

a) An interrupt handler saves/restores
(i) Processor registers as in the convention for normal procedure calls
(ii) All the processor registers
(iii) None of the processor registers

b) The stack used by an interrupt handler is
(i) Always the system stack
(ii) Always the user stack
(iii) User or system stack depending on the mode (user/kernel) bit

c) Upon executing an RTI instruction the processor always goes back to
(i) user mode
(ii) system mode
(iii) mode prior to entering this interrupt handler

d) The interrupt vector table
(i) can be set up dynamically by any user program
(ii) is set up at boot time by the operating system
(iii) is contained in a ROM pre-set by the hardware

e) The difference between an external device interrupt and an internal trap or exception is that
(i) there is none
(ii) the vector number for a trap/exception is internally generated by the processor
(iii) the vector number for a trap/exception is provided by the user in one of the general-purpose registers
(iv) the vector number put out by a device, changes each time it interrupts

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Performance

6. (10 mins)

A. (10 points)
Consider the program shown below that consists of 1000 instructions.

```
      I1:
      I2:
      ..
      ..
      ..
      I10:              }
      I11: ADD          }
      I12:              } loop
      I13:              }
      I14: COND BR I10  }
      ..
      ..
      I1000:
```

The ADD instruction occurs exactly once in the program as shown. Instructions I10-I14 constitute a loop that gets executed 800 times. All other instructions execute exactly once.

a) What is the static frequency of the ADD instruction?

The memory footprint of the program is 1000 instructions. Out of these 1000 instructions, Add occurs exactly once.

Hence the static frequency of Add instruction = 1/1000 * 100 = **0.1%**

-2 for minor error -3 for major error

b) What is the dynamic frequency of the ADD instruction?

Total number of instructions executed
= loop execution + other instruction execution
= (800 * 5) + (1000-5) * 1
= 4995

} +2

Add is executed once every time the loop is executed.
So, the number of Add instructions executed = 800
Dynamic frequency of Add instruction
= (number of Add instructions executed/total number of instructions executed) * 100
= (800 / (995+4000)) * 100 = **16%**

} +3

-1 for minor error
-3 for major error

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B. (10 points)
A smart architect re-implements a given instruction-set architecture. She reduces the CPI for 60% of the instructions by 50%; the CPI for the remaining 40% of the instructions is unchanged. The clock cycle time for the processor is increased by 10%. How much faster is the new implementation compared to the original? Assume that the usage of all instructions are equally likely in determining the execution time of any program for the purposes of this problem.

Solution:

Old Avg CPI	= 1
Old Clock Cycle Time	= 1
Old Total Exec Time	= 1 * 1 = 1
New Avg CPI	= 0.6 * 0.5 + 0.4 * 1
	= 0.7
New Clock Cycle Time	= 1.1
New Total Exec Time	= 0.7 * 1.1 = 0.77
Speedup	= Old Total Time / New Total Time
	= 1 / 0.77 = **1.3**
OR	
Improvement	= (old – new)/old
	= ((1-0.77)/1) * 100 %
	= **23%**

+2 +3 +2 +3 +3

-2 for new/old

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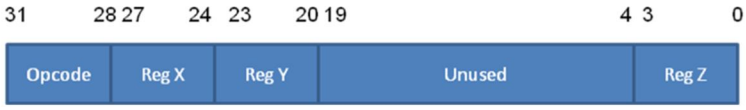
Pipelining

7. (10 mins)

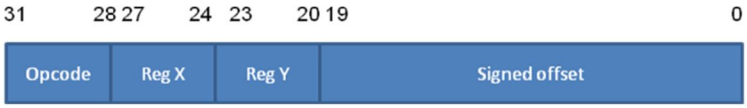
A.

Recall the format of the 32-bit CS 2200 ISA is as follows:

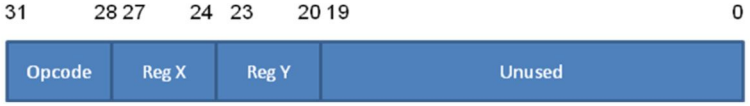
- R-type instructions (add, nand)



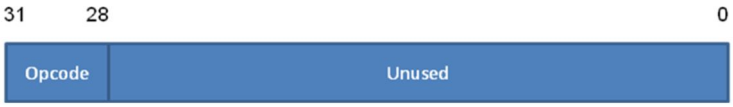
- I-type instructions (addi, lw, sw, beq)



- J-type instructions (jalr)



- O-type instructions (halt)



Considering the passage of all the instructions in LC-2200, we determined that the **DBUF** (the buffer between the ID/RR and EX stages of the pipeline) should have the following fields: **Opcode**, **Rx Specifier**, **two operand fields A and B**, an **Immediate field**, and a **PC field**

a) (6 points)

The width of each field in the DBUF is:

Opcode _____4_____ bits

Rx Specifier _____4_____ bits

A field _____32_____ bits

B field _____32_____ bits

Immediate field _____20_____ bits

PC field _____32_____ bits

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b) (6 points)

For each of the instructions shown in the first column, indicate what will be filled in each field of DBUF during the ID/RR stage of the pipeline. **We have shown the first instruction as an example.**
(Note: NA indicates a particular field is not applicable for this instruction; Ri indicates the register number; [Ri] indicates the register contents)

to·s for each correct entry

Instruction	DBUF					
	Opcode	Rx Specifier	A	B	Immediate	PC
ADD Rx, Ry, Rz	ADD	Rx	[Ry]	[Rz]	NA	NA
JALR Rx, Ry	JALR	Rx	[Ry]	NA	NA	PC
BEQ Rx, Ry, Offset	BEQ	NA	[Ry]	[Rx]	IR19-0	PC

******NOTE: OK if A and B fields switched in the Table ******
****** OK if "Offset" shown instead of IR19-0 in the Table ******

B. (6 points) (Fill in the blanks)

a) A non-pipelined processor takes an average of 5 clocks per instruction (including, fetch, decode, and execute).

The throughput of the processor is ____1/5_____ instructions per clock cycle.

b) A pipelined processor is implemented with a 5 stage pipeline, i. e, each instruction incurs a latency of 5 cycles from the beginning of instruction fetch to completion of instruction execution.

Assuming ideal conditions (i.e., no pipeline stalls) the throughput of the processor is ____1_____ instructions per clock cycle.

8. (4 points) **Bonus Question**

a) Structural hazard is due to _____hardware and datapath_____ limitation.

b) Code sequence
R1 <- R2 + R3
R4 <- R1 + R5
Represents a _____RAW_____ data hazard

c) Code sequence
R2 <- R1 + R3
R1 <- R4 + R5
Represents a _____WAR_____ data hazard

d) Code sequence
R2 <- R1 + R3
R2 <- R4 + R5
Represents a _____WAW_____ data hazard