GR8-1 : 8-bit Home-Brew CPU

Architecture Overview

Edward Gonell

GR8-1 Notes

- Exploration of ideas.
  - Pipelining
  - Multiple Execution Units
    - ALU
    - Register Bank
  - Dual Issue Fetch
- Precursor to the actual goal, GR8-2.
  - Deeper pipeline
  - Instruction Buffer
  - More Execution Units
    - 2 x ALU
    - Larger Register Bank

GR8-1 Dual Issue Fetch and Decode

GR8-1 fetch Unit

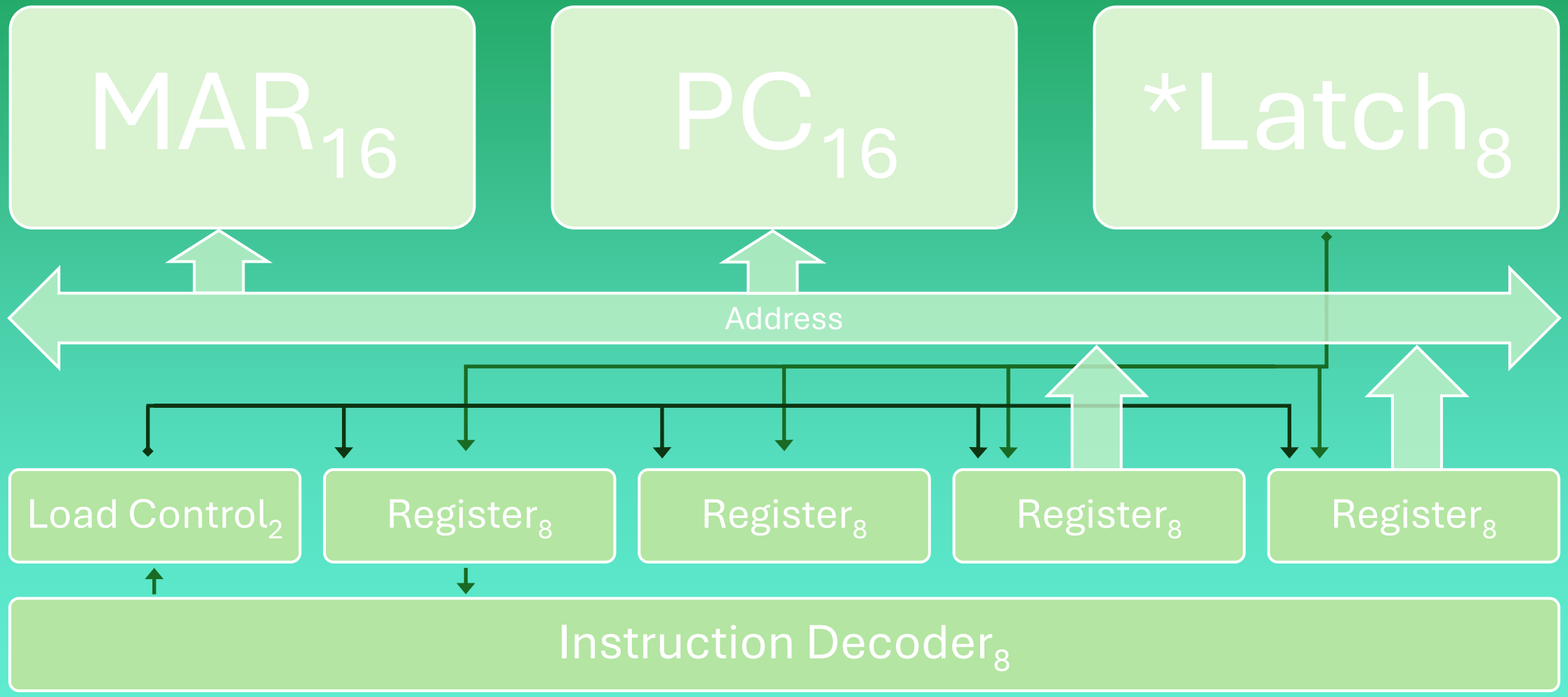
MAR_{16}

PC_{16}

$*Latch_{8}$

Decode

GR8-1 fetch and Decode

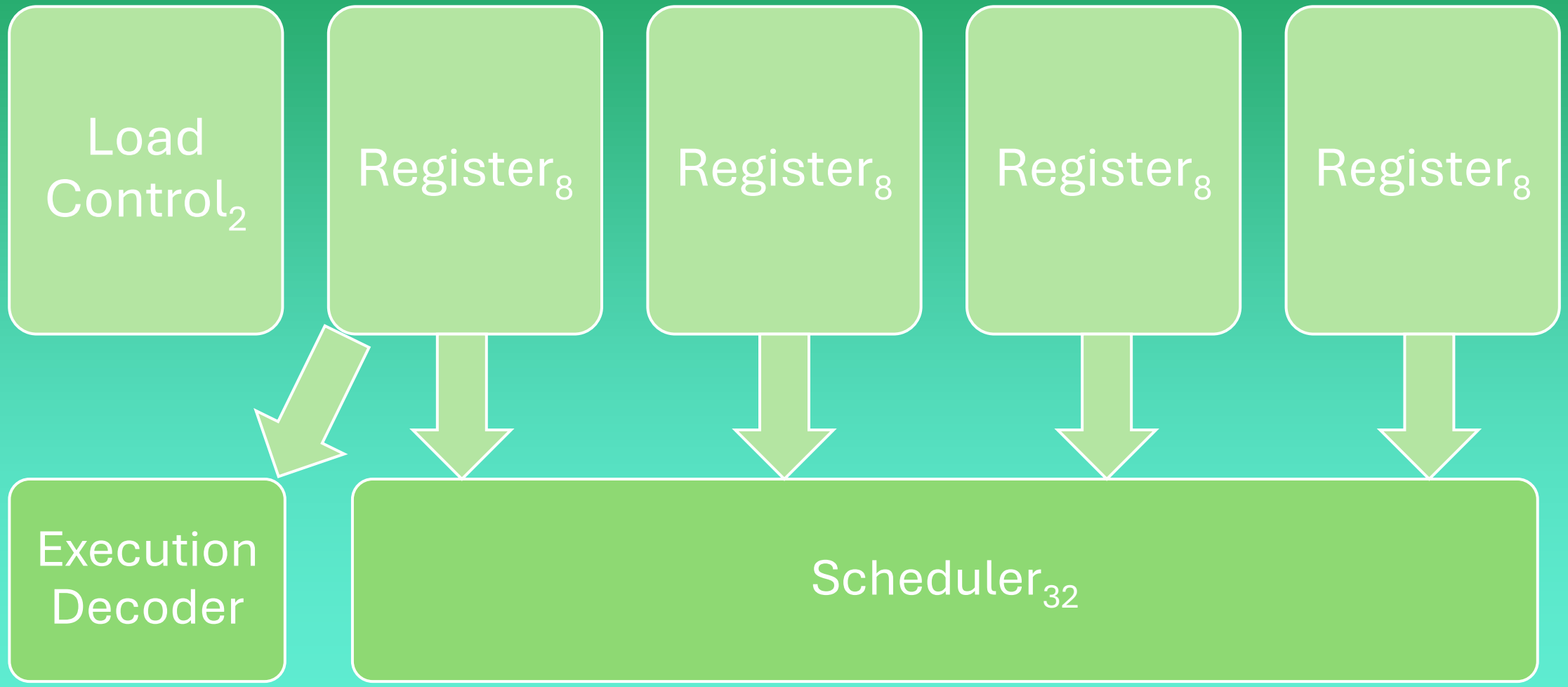


GR8-I Variable length Instruction

- Up to 4 bytes long

$Instruction_8$	$Data/Address_8$	$Data/Address_8$	$Data/Address_8$
Load	$Register_A$	0xBE	0xE7

GR8-1 Decode Unit



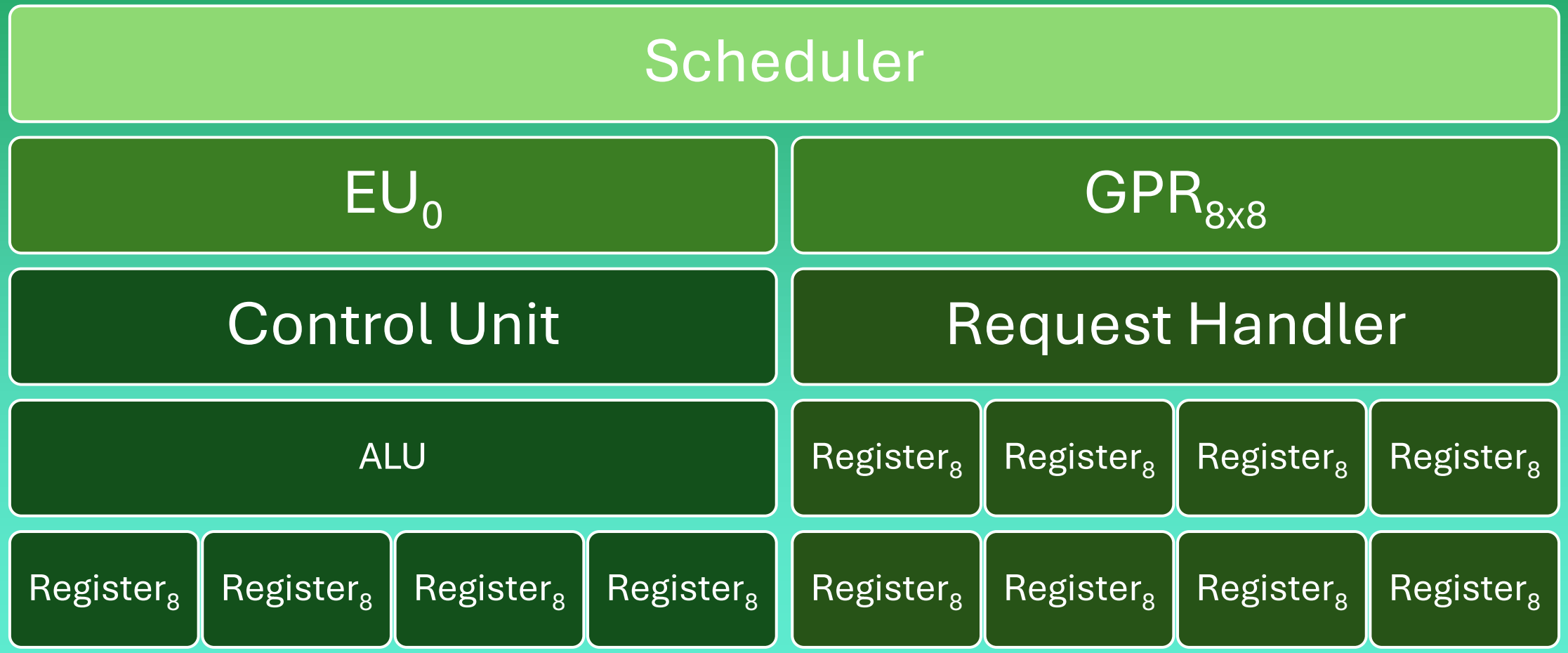
GR8-I Scheduler and Execution Units

Scheduler

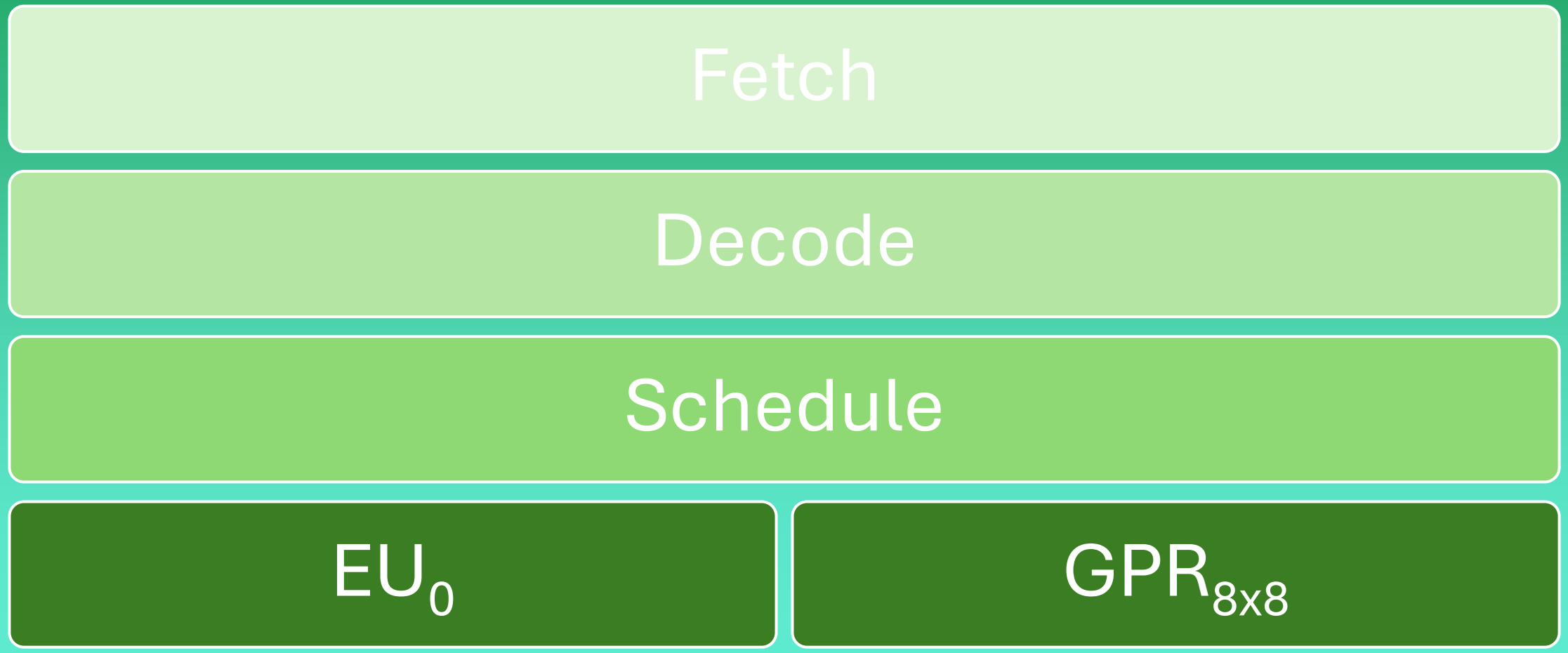
EU_0

GPR_{8x8}

GR8-1 Execution Units



GR8-1 Topology



GR8-1 Detailed Topology