

2521/203      2602/202  
2601/202      2603/202  
**DIGITAL AND ANALOGUE**  
**ELECTRONICS II**  
June/July 2017  
Time: 3 hours



**THE KENYA NATIONAL EXAMINATIONS COUNCIL**

**DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING**  
**(POWER OPTION)**  
**(TELECOMMUNICATION OPTION)**  
**(INSTRUMENTATION OPTION)**

**MODULE II**

**DIGITAL AND ANALOGUE ELECTRONICS II**

**3 hours**

**INSTRUCTIONS TO CANDIDATES**

*You should have the following for this examination:*

*Answer booklet;*

*Mathematical tables/scientific calculator;*

*Drawing instruments.*

*This paper consists of TWO sections, A and B.*

*Answer any TWO questions from section A, and any THREE questions from section B.*

*All questions carry equal marks.*

*Maximum marks for each part of a question are as indicated.*

*Candidates should answer the questions in English.*

## SECTION A: ANALOGUE ELECTRONICS II

*Answer any TWO questions from this section*

(a)

Table 1 shows the data of a transistor used in a single-ended transformer-coupled class A amplifier with a load resistor of  $6\ \Omega$ . The transformer has a turns ratio of 6.3:2 and negligible d.c resistance. The supply voltage is 20 V and the quiescent base current is 10 mA.

**Table 1**

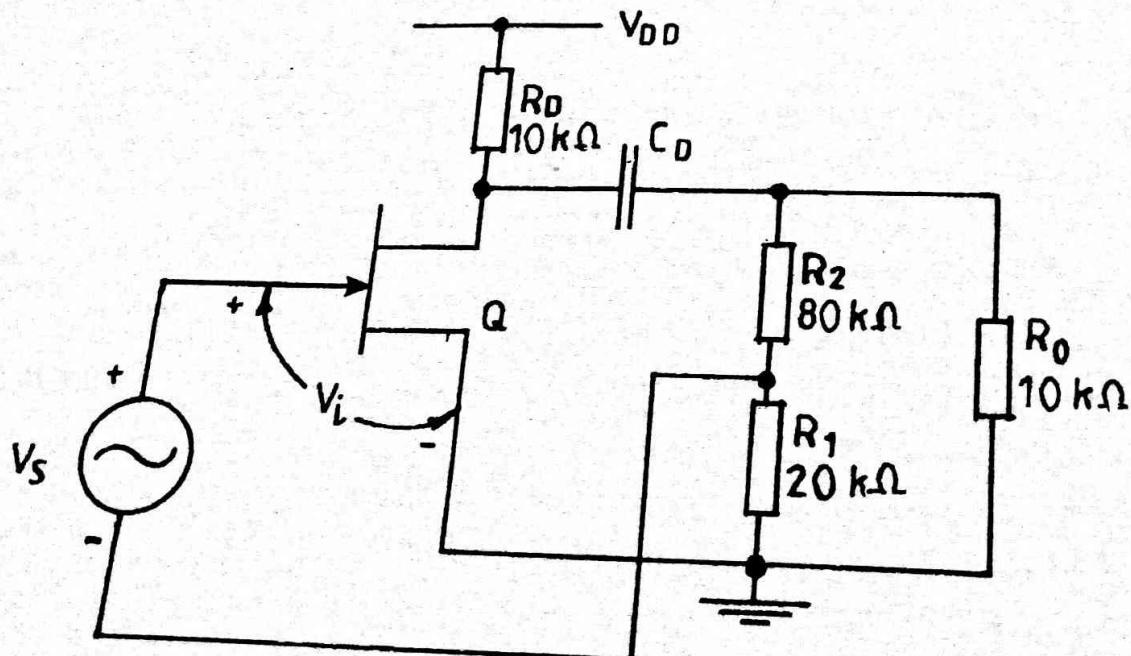
$V_{ce}$ (V)	$I_c$ (A)				
	$I_b = 2\text{ mA}$	$I_b = 6\text{ mA}$	$I_b = 10\text{ mA}$	$I_b = 14\text{ mA}$	$I_b = 18\text{ mA}$
1	0.02	0.22	0.40	0.60	0.80
40	0.20	0.40	0.60	0.80	1.00

- (i) plot the output characteristics of the transistor;
- (ii) draw the d.c and a.c loadlines;
- (iii) determine the:

- (I) input power;
- (II) output power;
- (III) efficiency.

(12 marks)

- (i) Figure 1 shows the circuit diagram of a FET amplifier with voltage-series negative feedback.



**Fig. 1**

Taking  $g_m = 4000 \mu\text{S}$ , determine the:

- (I) effective load resistance on the amplifier;
- (II) voltage gain without feedback;
- (III) feedback factor.

(ii) State the effect of the feedback in (b) (i) on the input and output impedances of the amplifier. (8 marks)

(a) (i) Define the following with respect to optoelectronics:

- (I) light;
- (II) incandescence.

(ii) With the aid of a circuit diagram, describe the operation of a transistor-based temperature-compensated drive for a light emitting diode. (8 marks)

(b) (i) Draw the circuit diagram of a transistor R-C phase-shift oscillator and describe its operation.

(ii) State any two factors that affect the frequency stability of the oscillator in (b) (i). (8 marks)

(c) A unijunction transistor has an intrinsic stand off ratio of 0.6 and the resistance of base 1 is  $4.8 \text{ K}\Omega$ . The supply voltage is 10 V. Determine the:

- (i) inter-base resistance;
- (ii) base current.

(4 marks)

(i) (i) State any three characteristics of an ideal operational amplifier (OP AMP).  
(ii) Figure 2 shows a circuit diagram of an OP AMP-based amplifier.

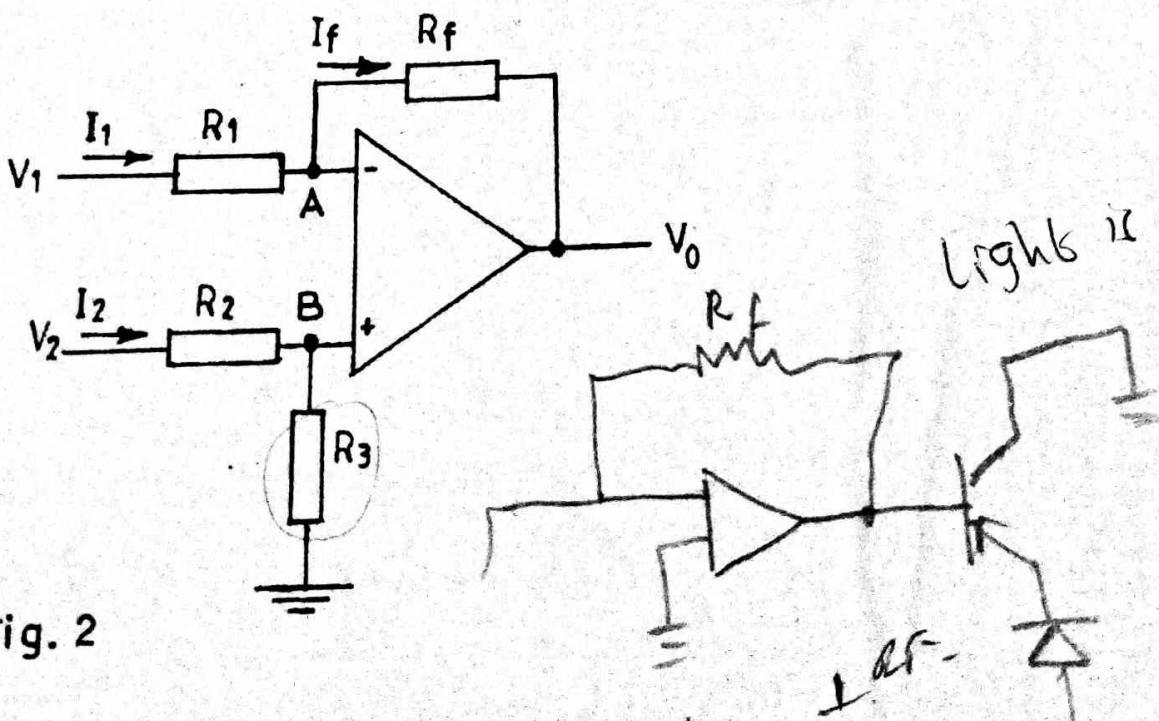


Fig. 2

- Assuming an ideal OP AMP, derive the expression for the output voltage,  $V_o$ , in terms of the input voltages  $V_1$  and  $V_2$ . (9 marks)
- (b) With the aid of a circuit diagram, describe the operation of a discrete-component astable multivibrator. (7 marks)
- (c) Figure 3 (a) shows the waveform of the input voltage to the diode clumper in figure 3 (b). Explain the operation of the circuit and draw the waveform of the output voltage. (4 marks)

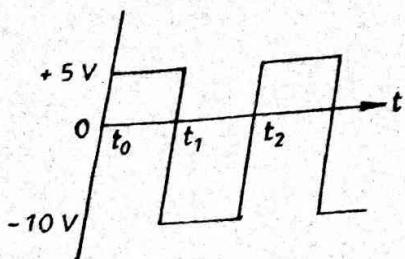


Fig. 3 (a)

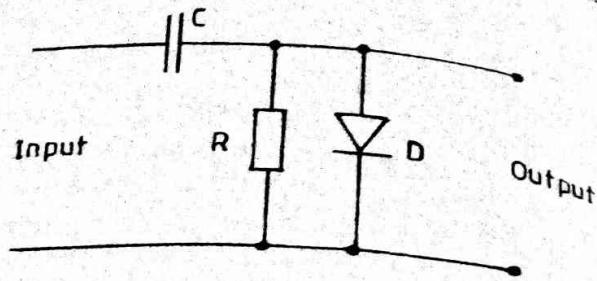


Fig. 3 (b)

## SECTION B: DIGITAL ELECTRONICS

Answer any THREE questions from this section

70111  
81000  
91001  
A 101010  
B 111011  
C 111100  
D 131101  
E 141110  
F 151111

- (a) Perform the following number system conversion:

- $1101.000101_2$  to decimal;
- $1011110100011000111_2$  to octal;
- $2C9_{16}$  to decimal.

- (b) (9 marks)
- Add  $-29$  to  $+14$  using 8-bit two's complement arithmetic.
  - Express the excess-3 number  $0110101111000111$  as decimal.
  - Divide  $11100_2$  by  $100_2$ .

12  
(11 marks)

- (a) (i) State **two** demerits of open-collector gates.  
 (ii) With the aid of a circuit diagram, describe the operation of a two-input CMOS NAND gate. (9 marks)

(b) (i) Use a truth table to show that:  $\overline{A+B} = \overline{A} \cdot \overline{B}$ .  
 (ii) Use Boolean algebra to simplify the expression:  
 $F = ABC\bar{C} + A\bar{B}\bar{C} + \bar{A}BC + ABC$ .  
 (iii) Implement the simplified expression in (b) (ii) using logic gates. (11 marks)

- (a) (i) State any **three** areas of application of binary counters.  
 (ii) Figure 4 shows a logic diagram of a binary counter. With the aid of a truth table, determine its counting sequence. (7 marks)

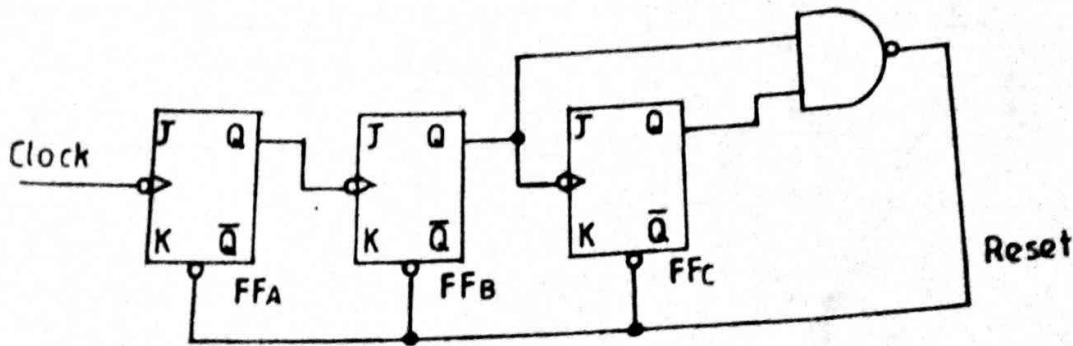


Fig. 4

Draw a logic diagram of a 4-bit Johnson's counter and construct its sequence table. (7 marks)

$$F = AB(\bar{C} + \bar{Q}) + A\bar{B}C + \bar{A}BC$$

$$F = AB + A\bar{B}C + \bar{A}BC' +$$

$$F = R(A + BC) + AB^T C$$

$$= BC + O + AC$$

$$= AB + BC + CA \in M_2(\mathbb{R}) = M_2 + (B + \bar{B}A)$$

$$(\mu_1 + \mu_2)_{\text{min}} \geq \mu_1 \mu_2 - C_1 \delta + A$$

1985-BC-AC

(c) A ripple counter has 7 cascaded flip flops. Each flip flop introduces a time delay of 65 nS. Determine the:

- (i) maximum count for the counter;
- (ii) propagation delay of the counter;
- (iii) maximum clock frequency.

(6 marks)

7. (a) (i) Define the following with respect to digital-to-analogue converters:

- (I) monotonicity;
- (II) resolution.

(ii) A 5-bit digital-to-analogue converter has a reference voltage of 10 V. Determine the:

- (I) maximum analogue voltage representing the most significant bit;
- (II) maximum analogue voltage representing the least significant bit;
- (III) percentage error of the converter.

(9 marks)

(b) With the aid of a circuit diagram, describe the operation of a bipolar static RAM cell.

(7 marks)

(c) Draw a diagram illustrating how two  $16 \times 4$  RAM chips can be configured to realise a  $32 \times 4$  RAM.

(4 marks)

(a) (i) Draw the truth table of a full adder.

(ii) From the table in (a) (i), obtain the simplified Boolean expression for the adder outputs.

(iii) Implement the simplified expression in (a) (ii) using logic gates.

(13 marks)

(b) (i) State the function of the following data circuits:

- (I) multiplexer;
- (II) decoder.

Figure 5 shows a circuit diagram of an encoder. Draw the truth table that describes the operation of the circuit. (7 m)

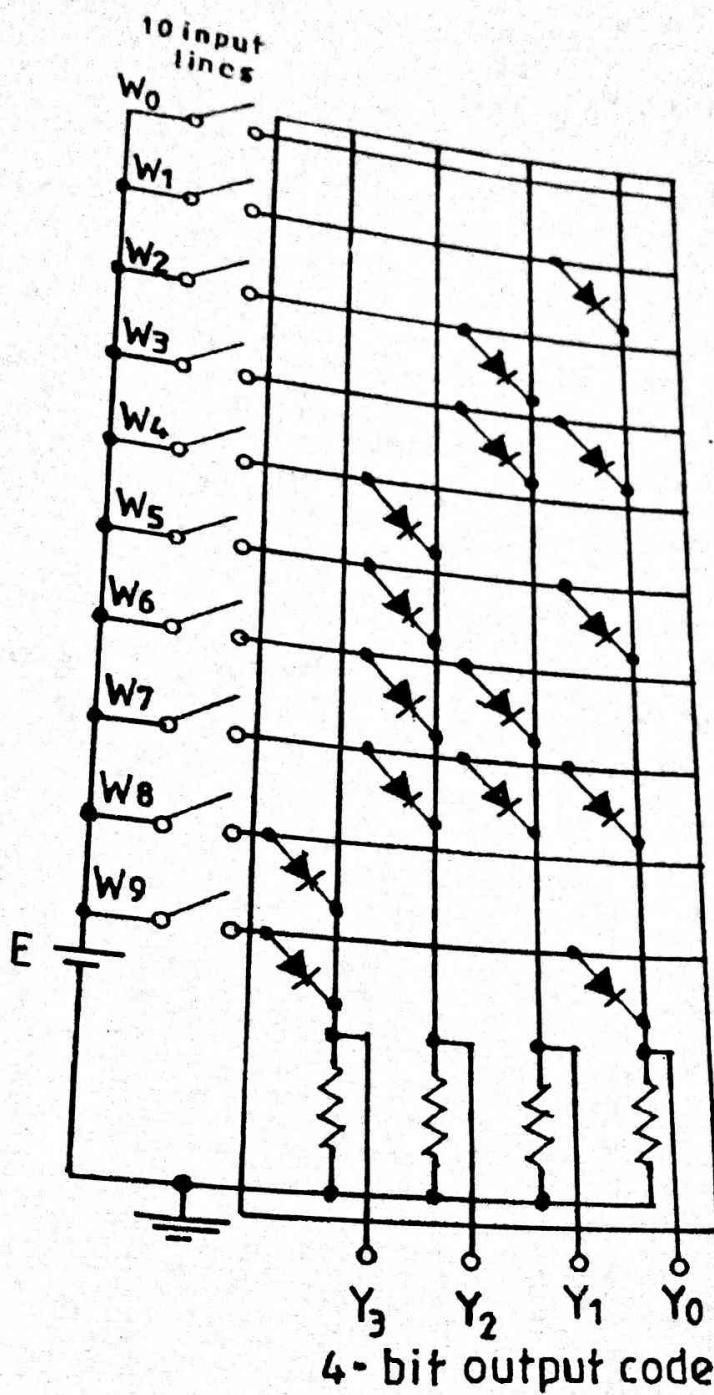


Fig. 5

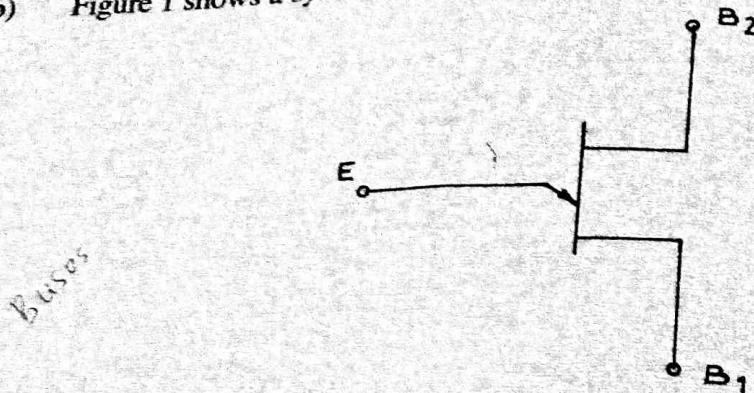
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**SECTION A: ANALOGUE ELECTRONICS II**

Answer any **TWO** questions from this section.

1. (a) Draw the V.I. characteristic curve of an SCR indicating each of the following:
- holding current;
  - latching current;
  - reverse breakdown voltage;
  - forward breakdown voltage.

- (b) Figure 1 shows a symbol of a semiconductor device.



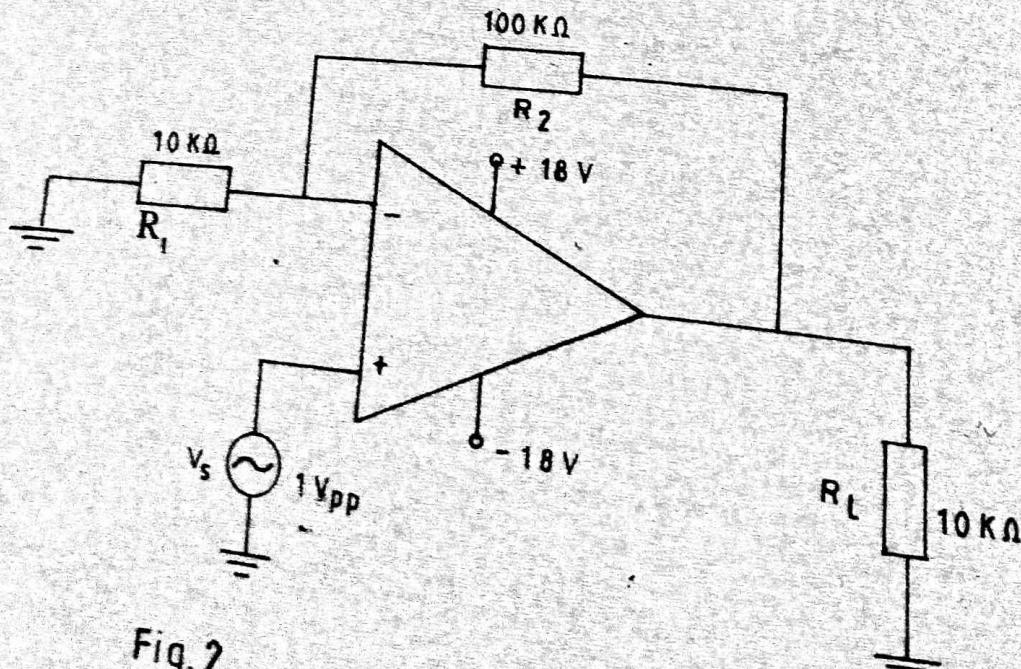
(5 marks)

**Fig. 1**

- (i) state the name of the device.  
 (ii) draw the equivalent circuit of b(i) and use it to explain the operation of the device.
- (c) Figure 2 shows a circuit diagram of a non-inverting amplifier. If the device has common mode gain of 0.001 and a slew rate of  $0.5 \text{ V}/\mu\text{s}$ , determine the

(8 marks)

- closed loop gain ( $A_{CL}$ );
- common mode rejection ration (CMRR);
- maximum operating frequency



(7 marks)

**Fig. 2**

Name \_\_\_\_\_

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**DIGITAL AND ANALOGUE  
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Index No. \_\_\_\_\_

Candidate's Signature \_\_\_\_\_

Date \_\_\_\_\_



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**(POWER OPTION)**  
**(TELECOMMUNICATION OPTION)**  
**(INSTRUMENTATION OPTION)**  
**MODULE II**

**DIGITAL AND ANALOGUE ELECTRONICS II**

**3 hours**

**INSTRUCTIONS TO CANDIDATES**

Write your name and index number in the spaces provided above.  
and write the date of the examination in the spaces provided above.  
should have the following for this examination:

Mathematical tables/non programmable calculator;

Drawing instruments;

paper consists of **TWO** sections; **A** and **B**.

Answer any **TWO** questions from section **A** and any **THREE** questions from section **B** in the spaces provided in this question paper.

Questions carry equal marks. All workings must be shown.

Number of marks for each part of a question are as indicated.

DO NOT remove any pages from this booklet.

Candidates should answer the questions in English.

**For Examiner's Use Only**

Section	Question	Maximum Score	Candidate's Score
		20	

(a)

Figure 3 shows a circuit diagram of a common collector amplifier with the following set of h-parameters  $h_{ie} = 2k\Omega$ ,  $h_{fe} = 51$ ,  $h_{re} = 1$  and  $h_{oe} = 25 \times 10^6$  Mhos.

- draw its equivalent a.c circuit.
- determine the following values of the amplifier stage:

- input resistance;
- output resistance;
- current gain;
- voltage gain;

(13 marks)

(b)

Define the following terms in relation to operational amplifiers.

- slew rate;
- common mode rejection ration (CMRR);
- common mode gain.

(3 marks)

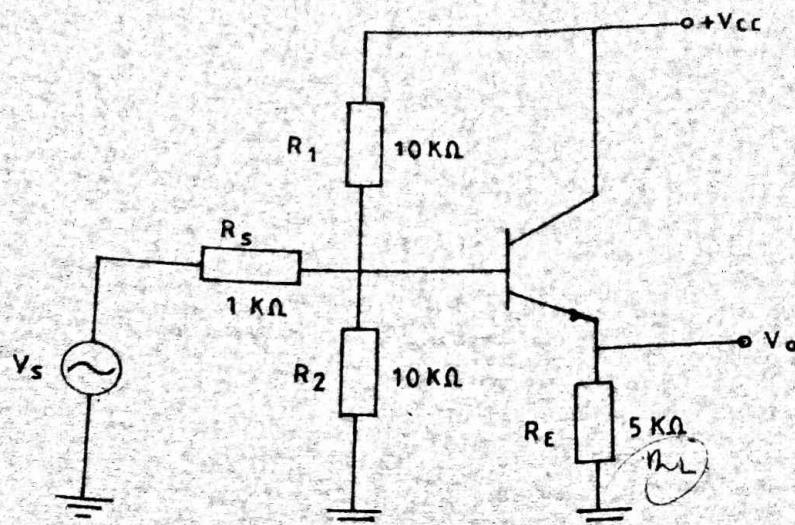


Fig. 3

(c)

Figure 4 shows a non-inverting mode of an operation Amplifier. Derive its gain.

(4 marks)

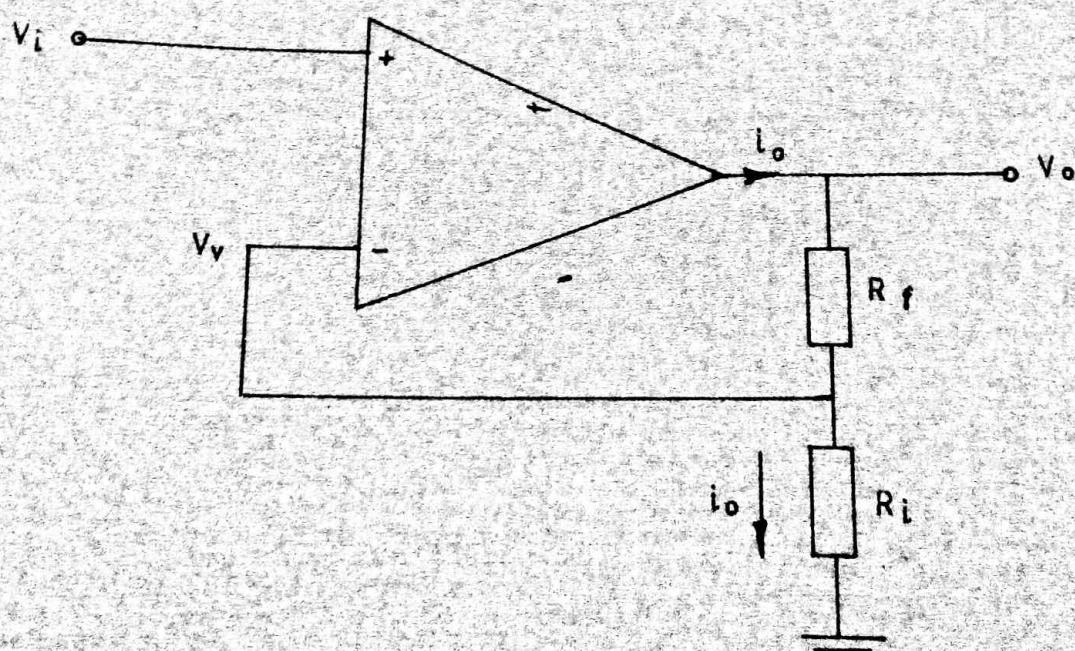


Fig. 4

3. (a) (i) State any two merits of negative feedback connection in feedback amplifiers  
 (ii) With the aid of a block schematic diagram of a feed back amplifier show that for a positive feedback:
- $$A'_v = \frac{A_v}{1 - \beta \cdot A_v}$$
- Where  $\beta$  = feedback ratio  
 $A_v$  = voltage gain without feedback  
 $A'_v$  = voltage gain with feedback.
- (b) With the aid of a circuit diagram describe the operation of a transistorized hartley oscillator. (7 marks)
- (c) An amplifier with negative feedback gives an output of 12.5 V for an input of 1.5 V. When the feed back is removed it requires 0.25 V input for the same output. Determine the: (7 marks)
- (i) value of voltage gain without feedback;
  - (ii) value of  $\beta$  if the input and output are in phase and  $\beta$  is real.

## SECTION B: DIGITAL ELECTRONICS (6 marks)

*Answer any THREE questions from this section.*

4. (a) (i) Convert the following numbers:

I  $(2A6)_{16}$  to binary

II  $(1024)_8$  to hexadecimal

- (ii) Perform the following operations;

I  $(101)_2 \times (111)_2$

\* II Subtract signed decimal numbers -19 from -25 using 8 bit 2's complement.

(10 marks)

- (b) A binary word 1000101 is to be sent through the telephone line from a field devise to a server. Determine the sent word using the following error detection methods;

- (i) even parity;
- (ii) odd parity.

- c) (i) Simplify the following expression using Boolean rules. (4 marks)

$$F(x, y, z) = (Z + Y + XY)(X + Z)$$

- (ii) State the Demorgan's theorems. (6 marks)

(a)

(i)

(ii)

State any two merits of using integrated circuits (ICs) in digital systems.

Figure 5 shows a Transistor - Transistor logic (TTL) gate.

- I      identify the logic function;  
 II     describe its operation.

(8 marks)

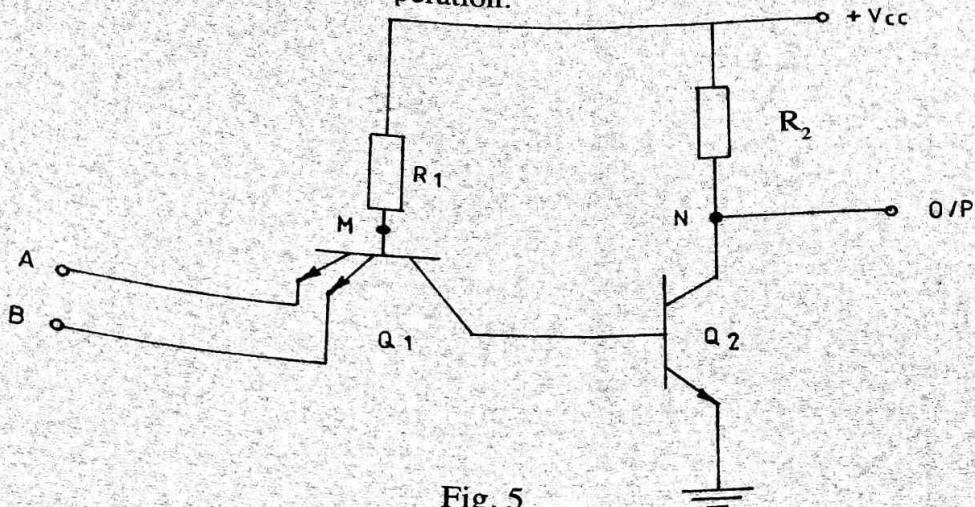


Fig. 5

(b)

A 16-to-1 multiplexer is to be constructed using 4-to-1 multiplexers.

(i)  
 (ii)

- determine the number of 4-to-1 multiplexers required;  
 draw a labelled block diagram to implement the 16-to-1 multiplexer.

(8 marks)

c)

Implement the following function using a 3-to-8 decoder and OR gate(s)  
 $f(A,B,C) = \sum m(0,1,4,5,7)$

(4 marks)

State two operational difference between synchronous and a synchronous counters.

(2 marks)

A 64 kHz input square wave signal is to be divided into a 2 kHz square wave output; using J-K flip flops.

- (i)  
 (ii)

determine the number of flipflops required;

implement the circuit.

(10 marks)

A given application requires PROM space of  $4 K \times 8$  and RAM space of  $4 K \times 8$ . The only available devices are PROMs of  $2 K \times 8$  and RAMs of  $1K \times 8$ . The PROM memory occupy the lower address space starting from  $0000\text{ H}$  followed immediately by the RAM.

- (i)  
 (ii)

determine the number of memory chips for each memory type;

draw a memory map of the system indicating the starting and end address for each chip.

8 marks

7. (a) Define each of the following converter parameters:

- (i) quantization;
- (ii) speed.

(b) With the aid of a schematic block diagram describe the operation of a successive approximation analogue-to-digital converter (ADC). (2 marks)

(c) Table 1 shows a truth table of a control system. (8 marks)

(i) Obtain simplified expressions for:

- I Sum of product (SOP)  
II Product of sum (POS)

(ii) Compare the results of c(i) I and II, then comment. (10 marks)

Table 1

Inputs			Output
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

i) Figure 6 (a) shows the logic symbol of a J-K flip flop that responds to the falling edge on its clock pulse and has active low asynchronous input. The J-K inputs are tied High. The waveforms in figure 6(b) are fed to corresponding inputs of the flip flop. Assuming that initially  $Q = 0$ , determine the  $Q$  output waveform in response to those waveforms. (5 marks)

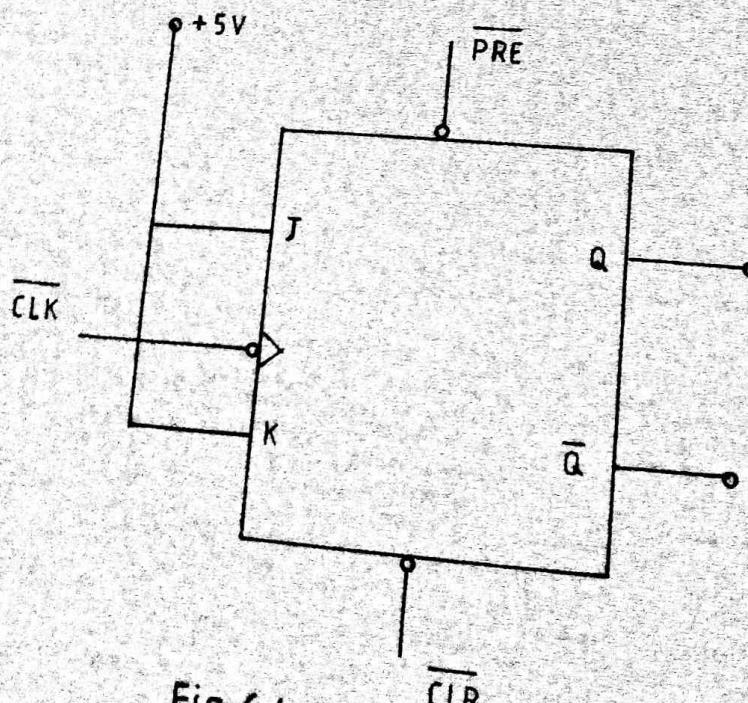


Fig. 6(a)

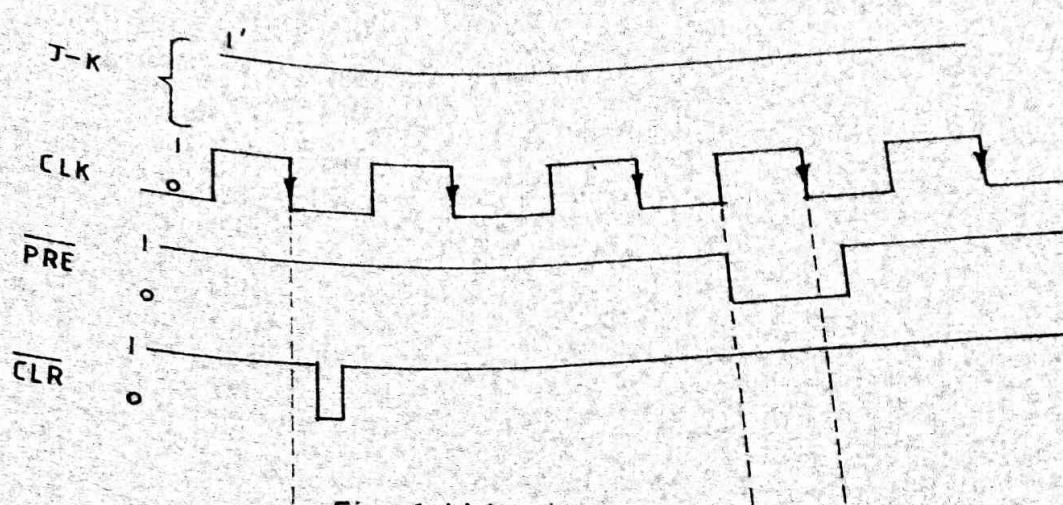


Fig 6 (b)

- (b) A certain J-K flip flop has  $t_{pd} = 12\text{ns}$ . The flip flop was used to construct a counter to operate upto 10 MHz. Determine the largest MOD counter that can be constructed from these flip flops. (4 marks)

- (c) A coin operated juice dispenser will provide a paper cup of mango or orange juice diluted with water under the following conditions:

the correct coin is inserted (C)  
 a paper cup is in position (P)  
 diluting water should be available (W)  
 the selector switch is set at mango (M) or orange ( $\bar{M}$ ) juice.

Obtain of this dispenser the:

- (i) truth table;  
 (ii) simplified boolean expression for selecting;

I      mango juice;  
 II     orange juice.

- (iii) logic circuit diagram.

(11)

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**MODULE II**

**DIGITAL AND ANALOGUE ELECTRONICS II**

**3 hours**

**INSTRUCTIONS TO CANDIDATES**

*You should have the following for this examination:*

*Mathematical table/Non-programmable calculator;*

*Drawing instruments;*

*Drawing paper size A2.*

*The paper consists of EIGHT questions in TWO sections; A and B.*

*Answer any TWO questions from Section A and any THREE questions from Section B in the answer booklet provided.*

*All questions carry equal marks.*

*Maximum marks for each part of the question are as indicated.*

*Candidates should answer all questions in English.*

**This paper consists of 7 printed pages.**

**Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.**

**SECTION A: ANALOGUE ELECTRONICS II**

*Answer any TWO questions from this section.*

1. (a) (i) State **three** characteristics of ideal operational amplifier (OP AMP).
- (ii) Figure 1 shows a circuit diagram of a amplifier. Determine the magnitude of the output voltage  $V_o$ .

(6 marks)

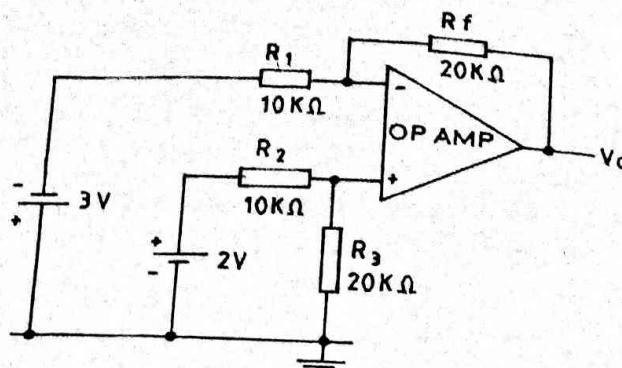


Fig. 1

- (b) Figure 2 shows a circuit diagram of a transistor amplifier. Assuming  $h_{oe}$  and  $h_{re}$  are negligible:
- (i) draw the  $h$ -parameter equivalent circuit;
- (ii) obtain the expression for the voltage gain from the circuit in b(i).

(8 marks)

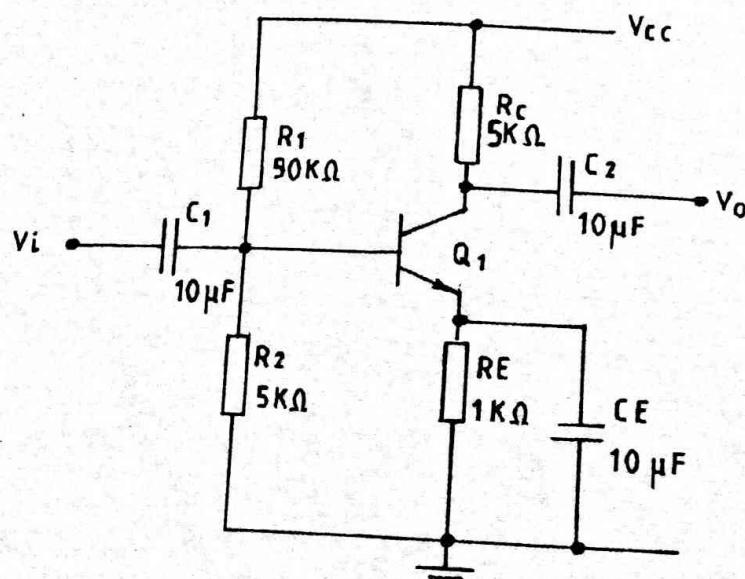


Fig. 2

A transistor used in a class A audio-power amplifier draws a collector bias current of 5mA from a 10V supply. A sinusoidal input signal causes the collector voltage to vary between 2V and 18V while the collector current varies between 8mA and 2mA.

Determine the:

- (i) power input;
- (ii) power output;
- (iii) efficiency of the amplifier.

2. (a) (6 marks)

(b) With the aid of a labelled diagram describe the operation of a ruby laser. (7 marks)

A series-resonant circuit consisting of a  $10\Omega$  resistor, a  $50\ \mu\text{H}$  inductor and a variable capacitor is connected across a  $0.01\ \text{V}$  supply. Determine the:

- (i) capacitance required to tune the circuit to resonance at  $5\ \text{mHz}$ ;
- (ii) resonant current;
- (iii) voltage across the capacitor at resonance.

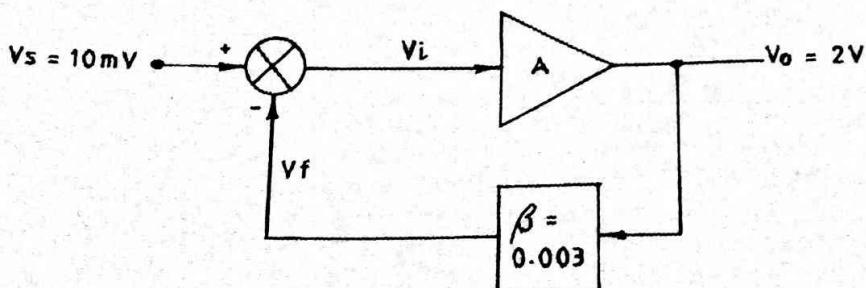
(6 marks)

(c)

Figure 3 shows a schematic block diagram of a negative feedback amplifier. Determine the:

- (i) magnitude of the voltage  $V_i$ ;
- (ii) gain without feedback;
- (iii) gain with feedback.

(7 marks)



$$V_i =$$

Fig. 3

- (i) State **four** applications of silicon controlled rectifiers (SCR).
- (ii) With the aid of equivalent circuit describe the operation of a unijunction transistor (UJT).

Applications of SCR

(10 marks)

~~Design of power permit~~

- (b) Figure 4 shows a circuit diagram of an astable multivibrator. For the output voltage waveform determine the:

- (i) periodic time;
- (ii) frequency;
- (iii) duty cycle.

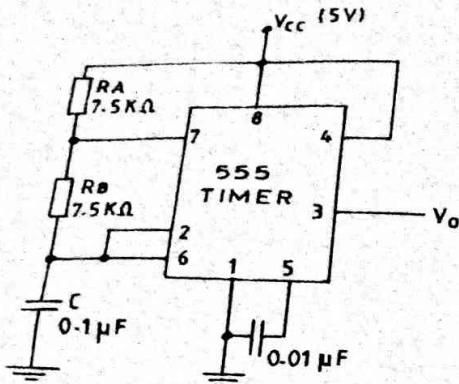
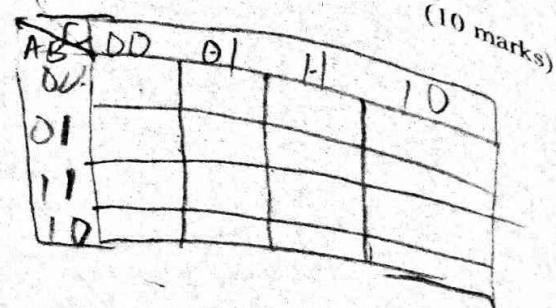


Fig. 4



## SECTION B: DIGITAL ELECTRONICS

*Answer any THREE questions from this section.*

- (a) Perform the following arithmetic operations in the given bases:

- (i)  $110110_2 \div 101_2$ ;
- (ii)  $(-17_{10}) + (-30_{10})$  in 8-bit two's complement arithmetic;
- (iii)  $6A_{16} \times DD_{16}$

11111111

10  
11  
11  
100

(10 marks)

- (b) Perform the following operations in the corresponding codes:

- (i) add 3 to 2 in 4-bit Excess - 3 code;
- (ii) convert binary number 1001011 to Gray code;
- (iii) encode the data bits 1011 into a 7-bit even-parity Hamming code.

A → 1010  
1011

(10 marks)

(a)

Table 1 shows the truth table for a certain logic operation.

INPUTS			OUTPUT
A	B	C	F
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	1
1	0	1	1
0	1	1	0
1	1	1	1

$$\begin{aligned}
 & A\bar{B}\bar{C} \\
 & A\bar{B}\bar{C} \\
 & A\bar{B}\bar{C} \\
 & A\bar{B}T \\
 & A\bar{B}C \\
 & A\bar{B}C \\
 & A\bar{B}C \\
 & A\bar{B}C
 \end{aligned}$$

- (i) Obtain the Boolean expression for the system.
- (ii) Simplify the expression in a(i) using Karnaugh map.
- (iii) Implement the simplified expression in a(ii) using NAND gates only.

(b)

With the aid of a truth table, design a decimal-to-BCD decoder. (9 marks)

(a) (i) Define the following with respect to logic circuits:

- (I) noise immunity;
- (II) current sink.

(ii) Figure 5 shows a circuit diagram of a transistor switch. Explain how the diode improves on the switching speed of the transistor. (5 marks)

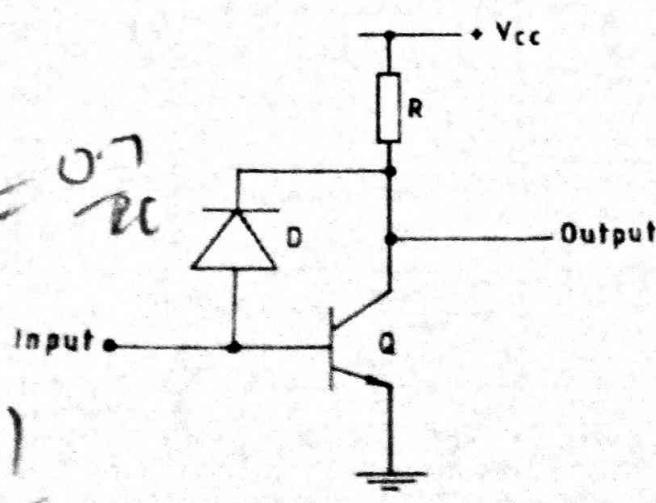


Fig. 5

(b) Draw circuit diagrams illustrating each of the following:

- (i) interfacing TTL to CMOS, both sharing the same power supply;
- (ii) interfacing CMOS to TTL, each with a separate power supply.

(c) Draw the:

(6 marks)

- (i) pin layout of the 7400 quad 2-input TTL NAND gate IC;

- (ii) logic diagram of the wired AND connection of two DTL gates and obtain the expression of the output.

(9 marks)

- (a) (i) State the **two** methods used to overcome the difficulties associated with strobed operation of flip-flops. *use edge triggered*

- (ii) Draw the state table of a JK flip-flop, hence obtain its characteristic equation.

(10 marks)

- (b) Draw a block diagram of a 4-bit ring counter and its sequence table assuming the first and third stages are preset.

(6 marks)

- (c) A ripple counter has 4 cascade flip-flops. Each flip-flop has a propagation delay of 75 ns. For the counter determine the:

- (i) maximum count;

- (ii) total propagation delay.

(4 marks)

- (a) (i) State **two** advantages of dual-slope integration over ramp-type analog-to-digital converters (ADCs).

- (ii) Draw the flow chart for the successive approximation ADC.

(8 marks)

- (b) A 5-bit digital-to-analog converter has a reference voltage of 16V. If the input to the converter is  $10110_2$ , determine the:

- (i) value of the analog output voltage;

- (ii) resolution of the converter.

(4 marks)

(i)

Figure 6 shows a block diagram of a DRAM. Explain how one of the 256 rows and one of the 256 columns can be selected.

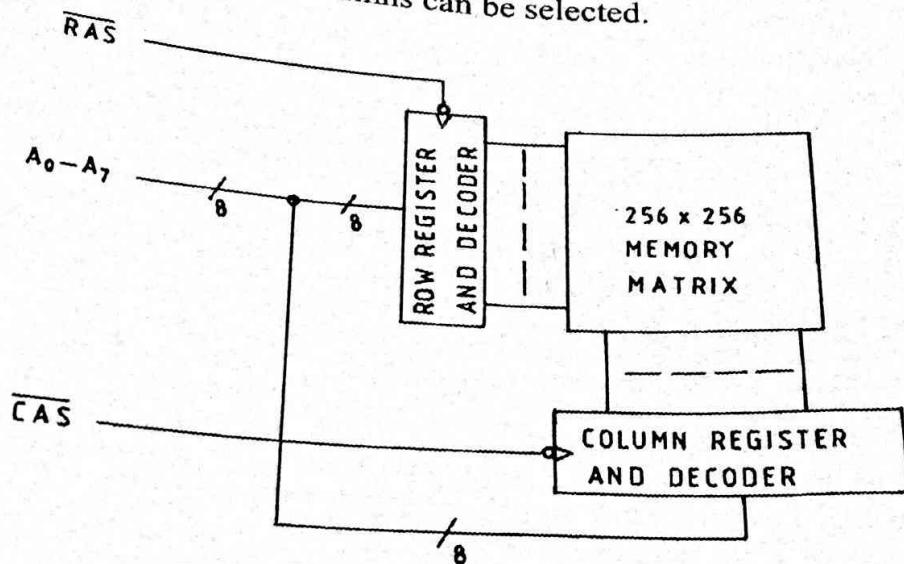


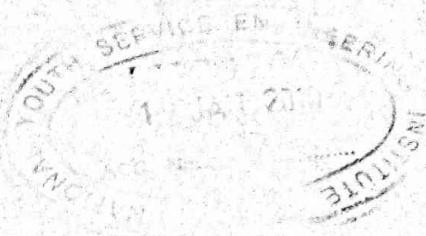
Fig. 6

(ii)

Draw a diagram illustrating how two 32 x 8 PROM can be configured to realise a 64 x 8 PROM.  
(8 marks)

$SR \Rightarrow JK$

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**DIGITAL AND ANALOGUE**  
**ELECTRONICS II**  
Oct./Nov. 2017  
Time: 3 hours



**THE KENYA NATIONAL EXAMINATIONS COUNCIL**

**DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING**  
**(POWER OPTION)**  
**(TELECOMMUNICATION OPTION)**  
**(INSTRUMENTATION OPTION)**  
**MODULE II**

**DIGITAL AND ANALOGUE ELECTRONICS II**

**3 hours**

**INSTRUCTIONS TO CANDIDATES**

*You should have the following for this examination:*

*Mathematical tables/Scientific calculator;*

*Drawing instruments;*

*Answer booklet.*

*This paper consists of EIGHT questions in TWO sections; A and B.*

*Candidates should answer TWO questions in section A and THREE questions from section B in the answer book provided.*

*All questions carry equal marks.*

*The maximum marks for each part of a question are as indicated.*

*Candidates should answer the questions in English.*

**This paper consists of 7 printed pages.**

**Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.**

## SECTION A: ANALOGUE ELECTRONICS II

*Answer any TWO questions from this section.*

1. (a) (i) State two applications of varactor diodes. *for modulator*

(ii) With the aid of a diagram and characteristic curve, describe the operation of a diac. *(10 marks)*

- (b) Figure 1 shows a circuit diagram of light measuring system using photoresistors. Describe its operation. *(4 marks)*

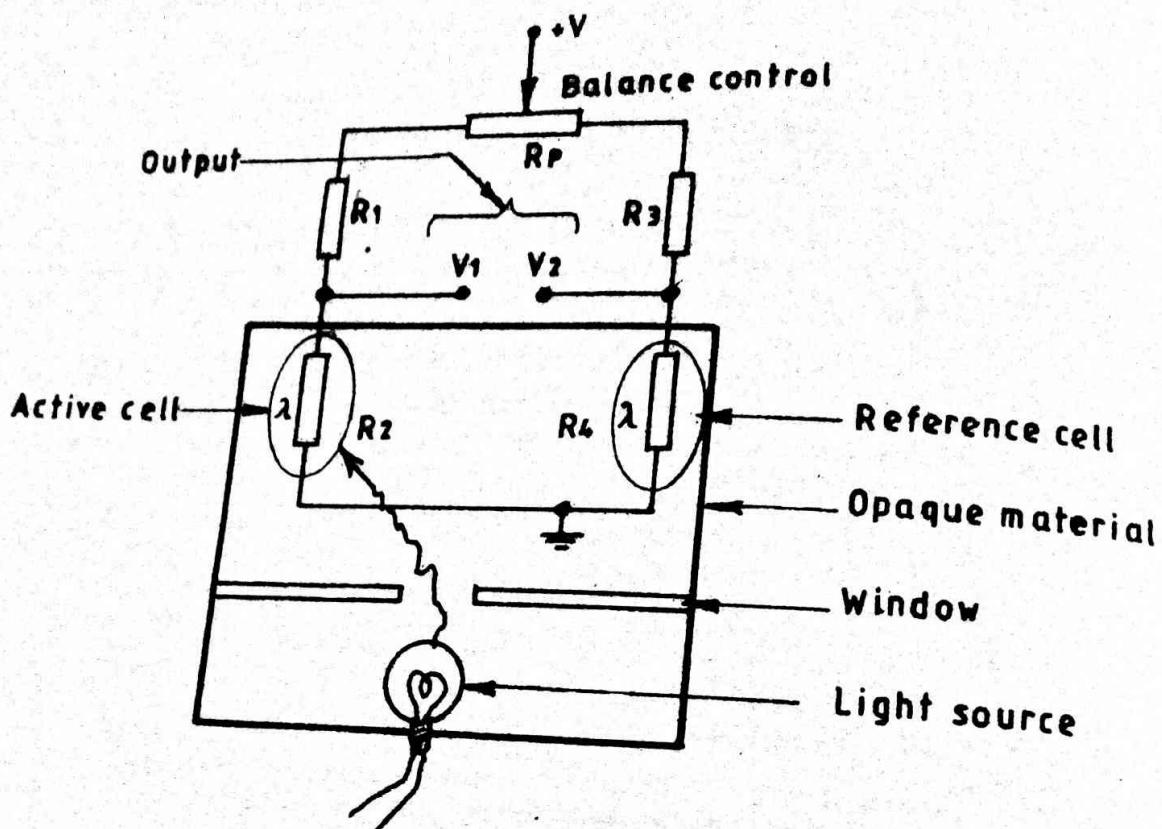


Fig. 1

- (c) A photodiode operated at  $25^\circ\text{C}$  has a dark current of  $600 \text{ pA}$  and supplies a load of  $10\text{M}\Omega$ . Taking the bandwidth of the noise current as  $10 \text{ Hz}$ , electronic charge =  $1.6 \times 10^{-19} \text{ C}$  and Boltzman's constant =  $1.38 \times 10^{-23} \text{ J/K}$ , determine the:
- (i) shot noise current;
  - (ii) thermal noise current;
  - (iii) total noise current.

*(6 marks)*

2.

(a)

Figure 2 (a) shows the waveform of the input voltage to the R-C circuit in Figure 2(b). Sketch the output waveform for each of the following conditions:

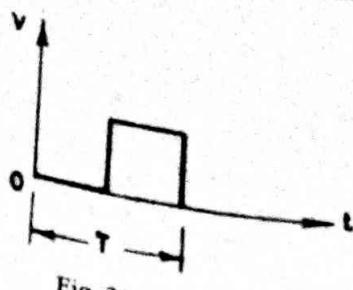


Fig. 2(a)

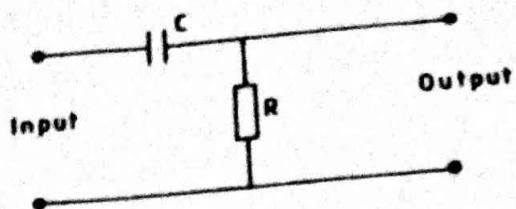


Fig. 2(b)

- (i)  $T = RC$ ;
- (ii)  $T \ll RC$ ;
- (iii)  $T \gg RC$ .

where  $T$  is the period of the waveform and  $RC$  is the time constant.

(6 marks)

(b)

An amplifier has a voltage gain of 100, input impedance of  $2\text{ k}\Omega$  and output impedance of  $40\text{ k}\Omega$  before negative feedback is applied. If voltage - series negative feedback is now applied with a feedback factor  $\beta = 0.1$ , determine the:

- (i) voltage gain;
- (ii) input impedance;
- (iii) output impedance.

$$A'v = \frac{AV}{1 + \beta AV}$$

$$f_{hof} = R_I(1 + \beta AV) \quad (6 \text{ marks})$$

$$R_{if} = \frac{R_o}{1 + \beta AV}$$

(c)

A differential amplifier has input voltages of  $150\text{ }\mu\text{V}$  and  $100\text{ }\mu\text{V}$ . The amplifier has a differential mode gain of 1000 and a common mode rejection ratio of 100. Determine the:

- (i) differential input voltage;  $-V_1 - V_2$
- (ii) common mode input voltage;  $\frac{V_1 + V_2}{2}$
- (iii) output voltage;
- (iv) percent error in the output voltage due to common mode voltage.

(8 marks)

(a)

- (i) Draw the circuit diagram of a transistor Hartley oscillator and derive the expression for the resonant frequency, assuming mutual coupling exists between the coils.

- (ii) State two advantages of colpitts oscillator over the oscillator in a(i).

(10 marks)

$$C_{MAX} = \frac{A_{cl}}{A_{cm}}$$

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(b) Describe the following types of distortion in amplifiers:

- (i) phase distortion;
- (ii) non-linear distortion.

(c)

An IF transformer has identical primary and secondary windings. Each winding has inductance of  $400 \mu\text{H}$  and is tuned by a capacitor. The 3 dB bandwidth of the stage is 20 kHz centred on 450 kHz. For critical coupling, determine the:

- (i) value of the capacitor to tune the stage;
- (ii) coefficient of coupling;
- (iii) mutual inductance of the transformer.

(4 marks)

(6 marks)

## SECTION B: DIGITAL ELECTRONICS

Answer any THREE questions from this section.

- (a)
- (i) State the two methods used to minimize the difficulties associated with strobed operation of a flip flop.  
Reset method  
Feedback method
  - (ii) Draw a truth table that describes the logical operation of S-R flip flop.
  - (iii) With the aid of a Karnaugh map, obtain the characteristic equation of the flip flop in a(ii).

- (b) Figure 3, shows a logic diagram of a binary counter. Describe its operation.

(10 marks)

(4 marks)

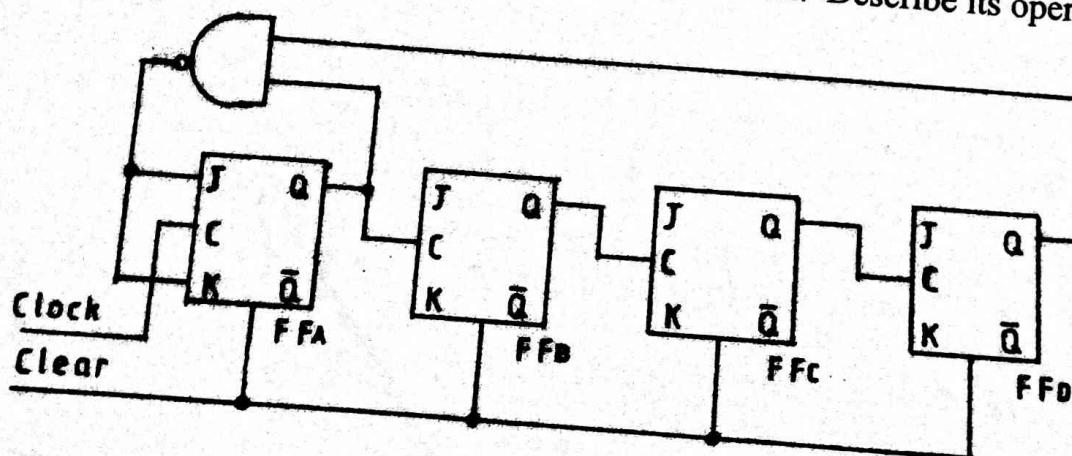


Fig. 3

- (i) Draw a logic diagram of a 4-bit serial-in serial-out shift register.
- (ii) With the aid of a state table, illustrate how the data 1011 would be clocked into the register in c(i).

(6 marks)

5.

(a)

(i)

Define the following with respect to memories:  
(I) access time;  
(II) volatile.

(ii)

With the aid of a labelled diagram, describe the features of a floppy disk.

(8 marks)

(b)

Figure 4 shows a circuit diagram of a parallel analog-to-digital converter. Describe its operation.

(5 marks)

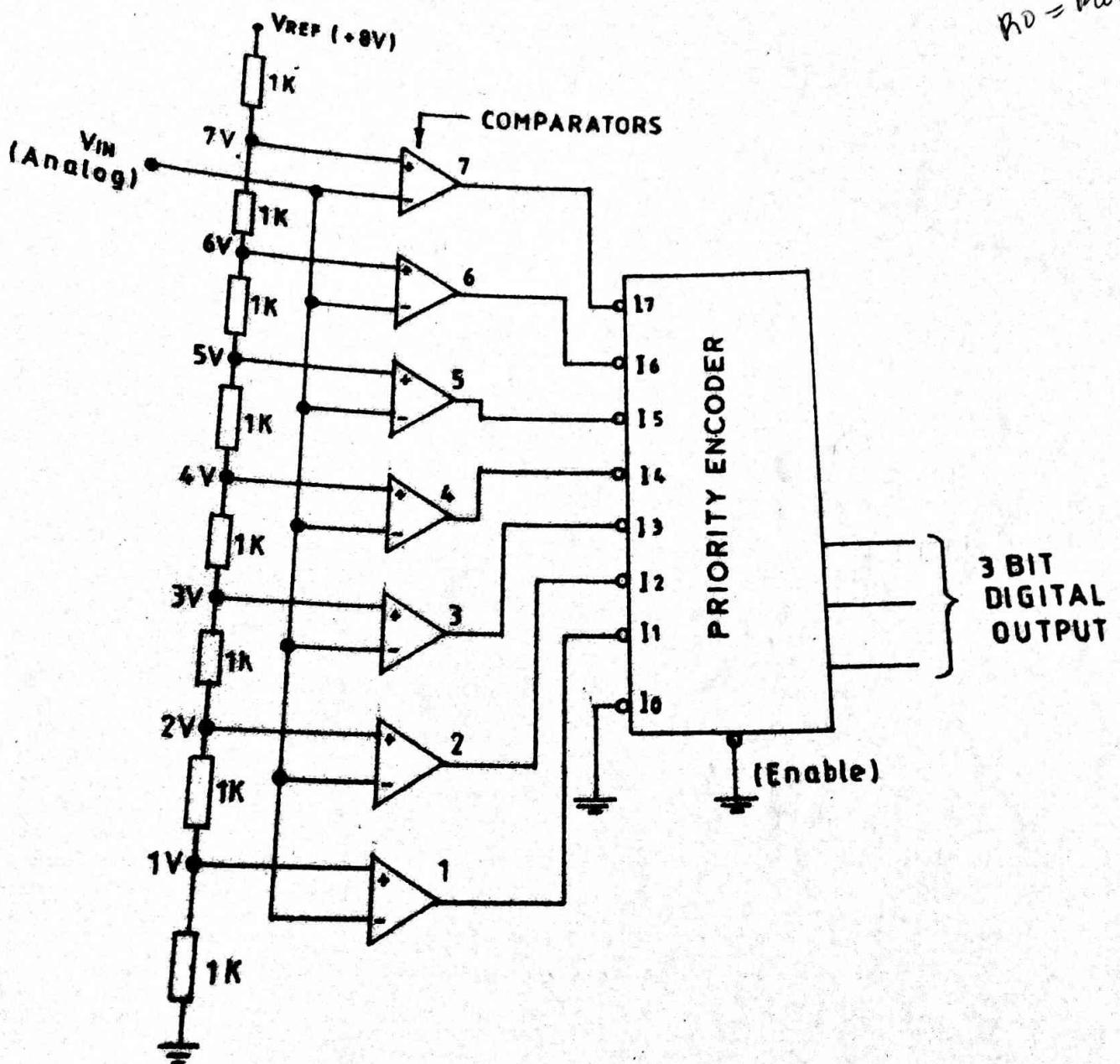
 $R_D = R_{ref}$ 

Fig. 4