Chapter-3

Bipolar Junction Transistors

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Bipolar Junction Transistors: Structure, typical doping, Principle of operation, concept of different configurations. Detailed study of input and output characteristics of common base and common emitter configuration, current gain, comparison of three configurations.

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Transistor as amplifier: RC coupled amplifier and frequency response

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3.1 Introduction

The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits, which led to electronics changing the way we work, play, and indeed, live. The invention of the BJT also eventually led to the dominance of information technology and the emergence of the knowledge-based economy.

The transistor is the main building block "element" of electronics. It is a semiconductor device and it comes in two general types: the Bipolar Junction Transistor (BJT) and the Field Effect Transistor (FET). Here we will discuss the structure and operation of the BJT and also describe the different BJT configurations.We also explain amplifying and switching action of BJT.

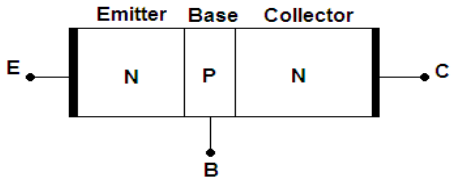
3.2 Structure and Principle of Operation

Transistor is a three terminal active device which transforms current flow from low resistance path to high resistance path. This transfer of current through resistance path, given the name to the device '*transfer resistor*' as **transistor**. Transistors consists of junctions within it, are called junction transistors. The *bipolar junction transistor* (BJT) is a three terminal device consists of two P-N junctions connected back to back. Current carries inside is by two opposite polarities of charge carriers (electrons and holes), hence the name *bipolar* junction transistor.

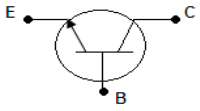
If a P-type material is sandwiched between two N-type materials as shown in fig (a), the resulting structure is called *NPN transistor*. Similarly when N-type material is sandwiched between the two P-type materials as shown in fig (b), the resulting structure is called *PNP transistor*. In both cases, the first layer where the emission or injection of the carriers starts is called ***emitter***. The second layer through which carriers passes is called the ***base*** and the third layer which collects the injected carriers is called ***collector***. In the symbol, the emitter has an arrowed head; it points the direction of the conventional emitter current (from P to N region).

Table:Transistor Operation

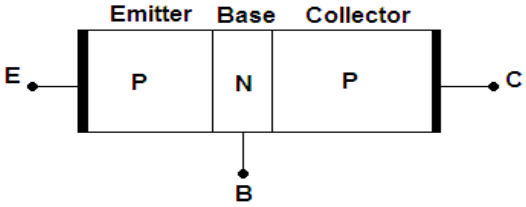
Emitter junction	Collector junction	Region of operation
Reverse biased	Reverse biased	Cut-off region
Forward biased	Reverse biased	Active region
Forward biased	Forward biased	Saturation region
Reverse biased	Forward biased	Inverse action



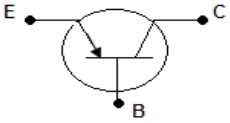
Fig(a): **NPN Transistor**



Symbol



Fig(b): **PNP Transistor**



Symbol

Although the emitter and collector are same type of material, they have different physical and electrical properties. The collector section is physically larger than the emitter section, since it has to collect all injected carriers and to withstand the large reverse bias voltage. The base is very thin and lightly doped. The size of the emitter falls between the base and collector region and is heavily doped. The doping level of collector region is between heavily doped emitter and lightly doped base.

A transistor has two junctions namely emitter base junction(emitter junction) and collector base junction(collector junction).These two junctions can be biased in four different ways, so that transistor operates in four different regions as stated in the following table.

3.3 Operation of NPN Transistor:

In the case of NPN transistor, forward biased applied across the emitter junction (by using $\mathbf{V_{EE}}$) lowers the emitter-base potential barrier, where reverse biased applied across the collector-base junction increases the collector base potential barrier. Due to this, electron in the emitter moves into the base and holes in the base moves into the emitter. The injected electrons, which are minority carriers in the base, diffuse across the base layer and gives rise to a current $\mathbf{I_{nE}}$. Injected holes from base to emitter constitute hole current $\mathbf{I_{pE}}$. The $\mathbf{I_{nE}}$ is very greater than $\mathbf{I_{pE}}$. As the base is thin lightly doped P-material, the number of holes in the base is small

and only few electrons will recombine with the holes at the base constitute base current. Due to high reverse bias at the collector junction (by using V_{cc}). The remaining electrons reaches the collector constitute collector current I_{nC}.

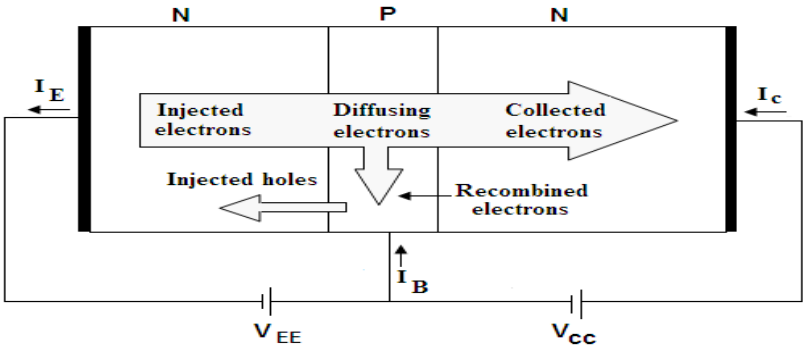


Fig: Operation of NPN Transistor

3.4 Transistor Configurations:

The most common application of a transistor is as amplifier. An amplifier requires two input terminals and two output terminals. But while using a three terminal device such as transistor as amplifier, one of its terminals has to be common to the input and output circuits. A transistor can be arranged to have any one of its terminal is common to both input and output. Thus it can be connected in following three configurations.

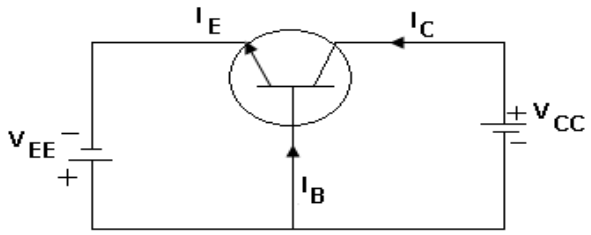
- Common Base (CB).
- Common Emitter (CE).
- Common Collector (CC).

Input and Output Characteristics of Bipolar Transistors

To describe the behavior of a three terminal device, it requires two sets of characteristics. The relation between the input voltage and input current for different values of the output voltage is called the input characteristics and output characteristics show the relation between the output current and output voltage for different values of input current.

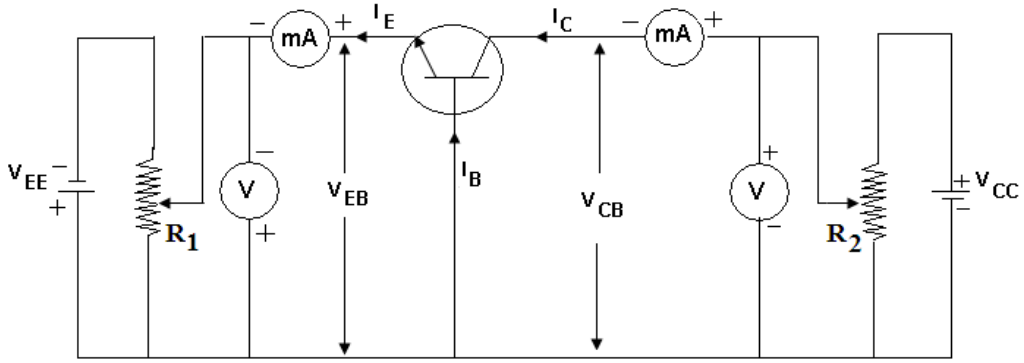
3.4.1 Common Base Configuration

The common base configuration for NPN transistor is shown in fig (a). In this arrangement input is given between emitter and base, while output is taken across the collector and base. Here base is common to both input and output. The forward-biased emitter –base voltage is regarded as the input voltage and emitter current is considered to be the input current where as the reversed-biased collector -base voltage is regarded as the output voltage and collector current is the output current.



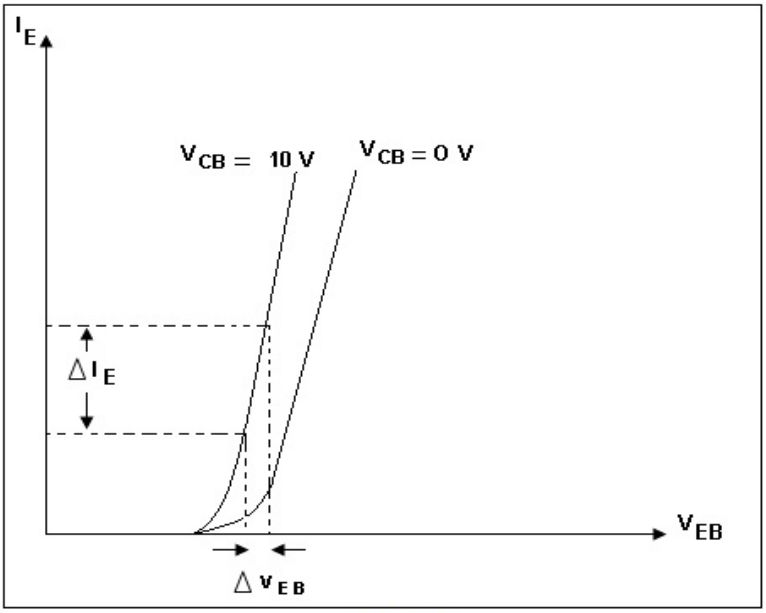
Fig(a):

Fig(b) shows the circuit arrangement for determining CB characteristics of a NPN transistor. Here the emitter-base voltage can be varied by means of rheostat $\mathbf{R_1}$. The collector voltage can be varied by adjusting the rheostat $\mathbf{R_2}$**.**The required currents and voltages can read from the milliammeters and voltmeters connected in the circuit.



Fig(b):

- **Input Characteristics:**



Fig(c):

Input characteristics of a CB configuration is the plot of emitter current IE as a function of emitter base voltage $\mathbf{V_{EB}}$ at constant collector-base voltage $\mathbf{V_{CB}}$. Different curves can be plotted for different values of $\mathbf{V_{CB}}$. Fig (c) shows a set of typical input characteristic curves for a NPN transistor, plotted at different $\mathbf{V_{CB}}$ (0, 10,and 20 volts).

For a given value of $\mathbf{V_{CB}}$ (for eg: 0volt) the input characteristic curve of a CB configuration is just like the forward characteristic of a junction diode (because the emitter base is a PN junction and is forward biased).However due to *early effect* an increase in the magnitude of the collector-base voltage $\mathbf{V_{CB}}$, slightly increases the emitter current for a given $\mathbf{V_{EB}}$.

Input Resistance:

Dynamic input resistance is the ratio of change in emitter base voltage to resulting change in emitter current at a constant collector-base voltage.

$$r_i = \Delta V_{EB} / \Delta I_E \quad | \; V_{CB} \; Constant$$

EARLY EFFECT

Because of reverse bias at collector junction, the depletion layer is wide and it penetrates both in to the base region and collector region. But the doping of the base region is much smaller than that of collector region. Hence the penetration of the depletion layer into the base region is much greater than the penetration into the collector region. Therefore the effective width of the base gets reduced. As the magnitude of the reverse bias at the junction increases, the effective base width decreases. This phenomenon is known as ***early effect*** or ***Base width modulation***.

The plot of the collector current $\mathbf{I_c}$ as a function of the collector to the base voltage $\mathbf{V_{CB}}$ with constant emitter current $\mathbf{I_E}$ is referred to as common base output characteristics. A set of typical output characteristics of NPN transistor is shown in fig(d).

The output characteristics can be divided in to three distinct regions.

- Active region
- Saturation region
- Cut off region

Active region:

This is the normal operating region of the transistor, when used as an amplifier. In this region the emitter junction will be in forward bias and collector junction will be in reverse bias. When the emitter current is zero, collector current $\mathbf{I_c}$ is not zero and there will be a very small current in the collector. This is the *reverse leakage current* $\mathbf{I_{CBO}}$. When the emitter-base junction is forward biased to get emitter current $\mathbf{I_E}$**:** Note that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also that the collector current will raise even when $\mathbf{V_{CB}}$ is zero. As the collector voltage $\mathbf{V_{CB}}$ is increased, there will no much change in collector current. But an increase in emitter current, there will be a corresponding change in $\mathbf{I_c}$.Thus collector current is almost independent of collector to base voltage $\mathbf{V_{CB}}$ and is dependent only on emitter current. Therefore the curve appears to be almost flat. The curves clearly indicate that *a first approximation to the relationship between I_E and I_C in the active region is given by*

$$I_C \cong I_E$$

Saturation region:

The region, where both the emitter-base and collector-base junctions remain forward biased is known as the *saturation region* of the transistor. The region is located to the left of the line $\mathbf{V_{CB}}$=0.When $\mathbf{V_{CB}}$ is slightly negative, the collector to base becomes forward biased. Here collector current decreases sharply for a small increase in forward bias across collector junction.

Cut off region:

The region to the right of the line $\mathbf{V_{CB}}$=0 and below the characteristics for $\mathbf{I_E}$=0 is the cut off region of the transistor. In this region both junctions of the transistor are reverse biased and hence only leakage current will flow through the transistor.

Output Resistance:

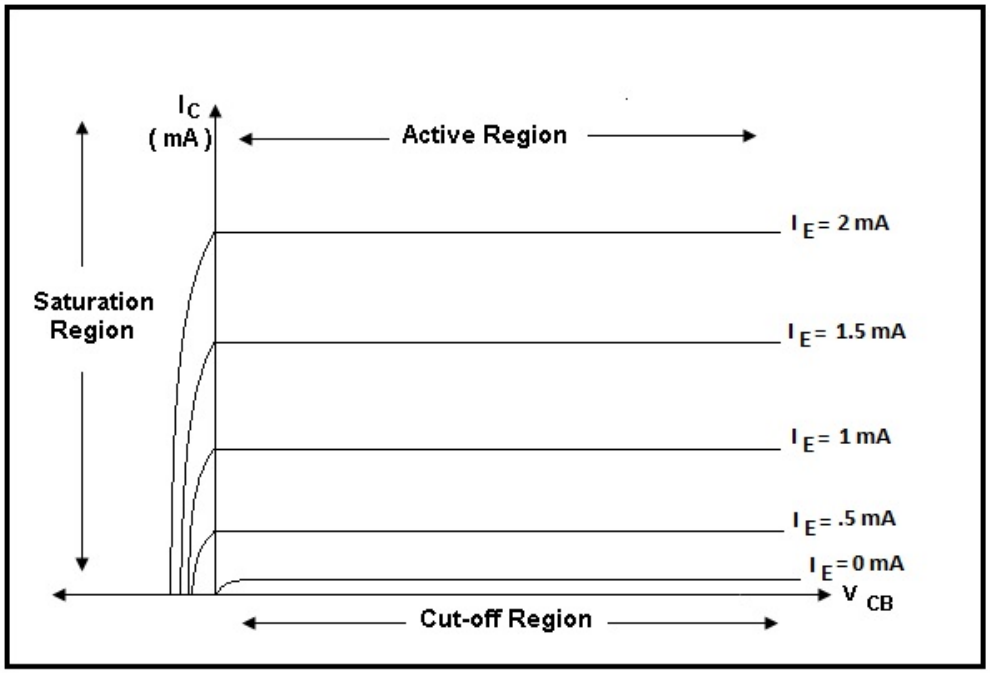
The dynamic output resistance is the ratio of change in collector to base voltage to the corresponding change in collector current at constant emitter current.

$$r_o = \Delta V_{CB}/\Delta I_C \quad | \; I_E \; Constant$$

Common Base Current Gain

The current gain for a common base configuration is denoted by 'α' and is given by

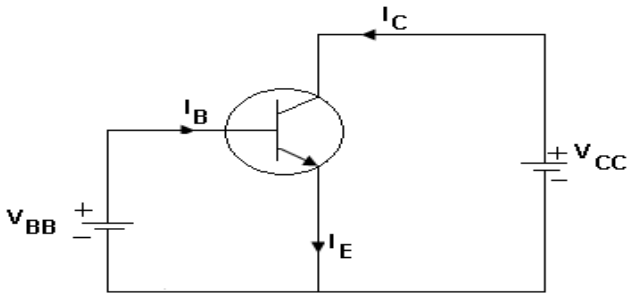
$$\alpha = I_C/I_E$$



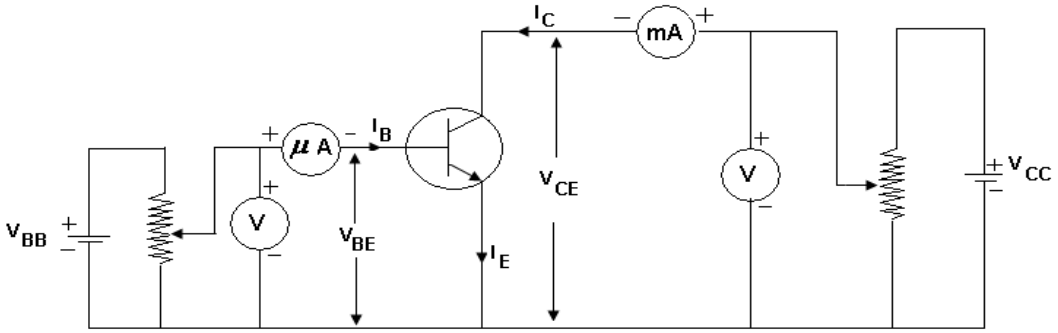
Fig(d) : Common Base output characteristics

3.4.2 Common Emitter Configuration

The common emitter configuration for NPN transistor is shown in fig(a). In this arrangement input is given between base and emitter, while output is taken across the collector and emitter. Here emitter is common to both input and output. The forward-biased emitter –base voltage is regarded as the input voltage and base current is considered to be the input current where as the reversed-biased collector –emitter voltage is regarded as the output voltage and collector current is the output current.



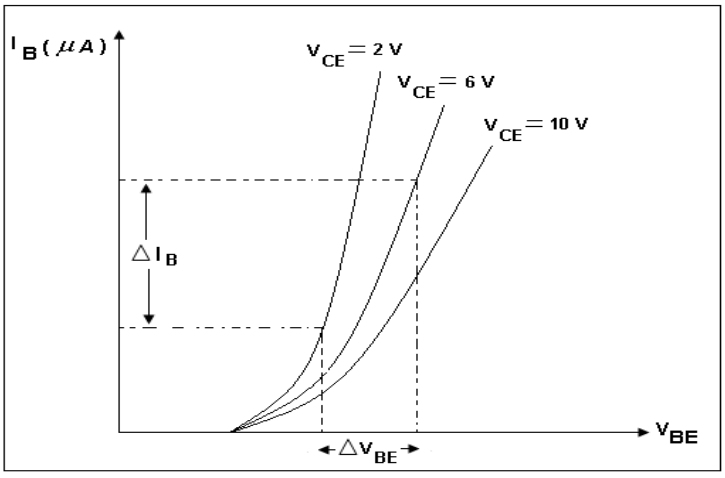
Fig(a):



Fig(b):

- **Input Characteristics:**

Input characteristics of a CE configuration is the plot of emitter current $\mathbf{I_B}$ as a function of emitter base voltage $\mathbf{V_{BE}}$ at constant collector-emitter voltage $\mathbf{V_{CE}}$. Different curves can be plotted for different values of $\mathbf{V_{CE}}$.Fig (c) shows a set of typical input characteristic curves for a NPN transistor, plotted at different $\mathbf{V_{CE}}$(2,6,and 10 volts).



Fig(c):

For a given value of $\mathbf{V_{CE}}$ (for eg: 2volt) the input characteristic curve of a CE configuration is just like the forward characteristic of a junction diode (because the emitter base is a PN junction and is forward

biased).How ever due to *early effect* an increase in the magnitude of the collector-emitter voltage $\mathbf{V_{CE}}$, slightly decreases the base current for a given $\mathbf{V_{BE}}$.

Input Resistance:

Dynamic input resistance in CE configuration is the ratio of change in emitter base voltage to resulting change in base current at a constant collector-emitter voltage.

$$r_i = \Delta V_{BE}/\Delta I_B \quad | V_{CE} = Constant$$

- **Output Characteristics:**

The plot of the collector current $\mathbf{I_c}$ as a function of the collector to the emitter voltage $\mathbf{V_{CE}}$ with constant emitter current $\mathbf{I_B}$ is referred to as common emitter output characteristics. A set of typical output characteristics of NPN transistor is shown in fig(d). Note that on the characteristics, the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

The output characteristics can be divided into three distinct regions.

- Active region
- Saturation region
- Cut off region

Active region:

This is the normal operating region of the transistor, when used as an amplifier. In this region the base-emitter junction will be in forward bias and collector-emitter junction will be in reverse bias. When the base current is zero, collector current $\mathbf{I_c}$ is not zero and there will be a very small current in the collector. This is the *reverse leakage current* $\mathbf{I_{CEO}}$. When the emitter-base junction is forward biased to get base current $\mathbf{I_B}$**.** The collector current will raise even when $\mathbf{V_{CE}}$ is zero. As the collector voltage $\mathbf{V_{CE}}$ is increased, the collector current first increases and then rate of increase is quite small and $\mathbf{I_c}$ become nearly constant. But the curves are not horizontal, because for a fixed values of base current $\mathbf{I_B}$ the magnitude of collector current increases slightly with increase in $\mathbf{V_{CE}}$**.** The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

Saturation region:

The region, where both the base- emitter and collector-emitter junctions remain forward biased is known as the *saturation region* of the transistor. Under this condition, the collector current is independent and it doesn't depend upon the input current $\mathbf{I_B}$.

Cut off region:

The region to the right of the line V_{CE}=0 and below the characteristics for I_B=0 is the cut off region of the transistor. In this region both junctions of the transistor are reverse biased and hence only leakage current will flow through the transistor.

Output Resistance:

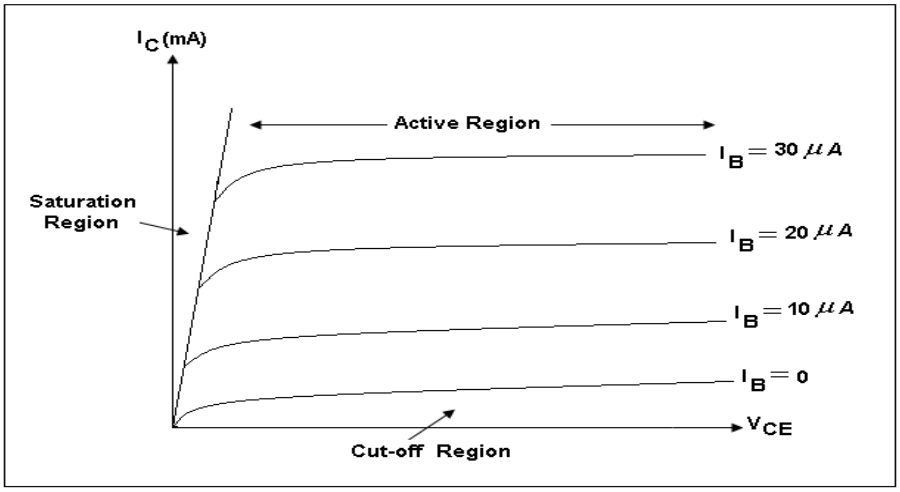
The dynamic output resistance in CE configuration is the ratio of change in collector to emitter voltage to the corresponding change in collector current at constant base current.

$$r_o = \Delta V_{CE}/\Delta I_C \quad | I_B = Constant$$

Common Emitter Current Gain

The current gain for a common emitter configuration is denoted by 'β' and is given by

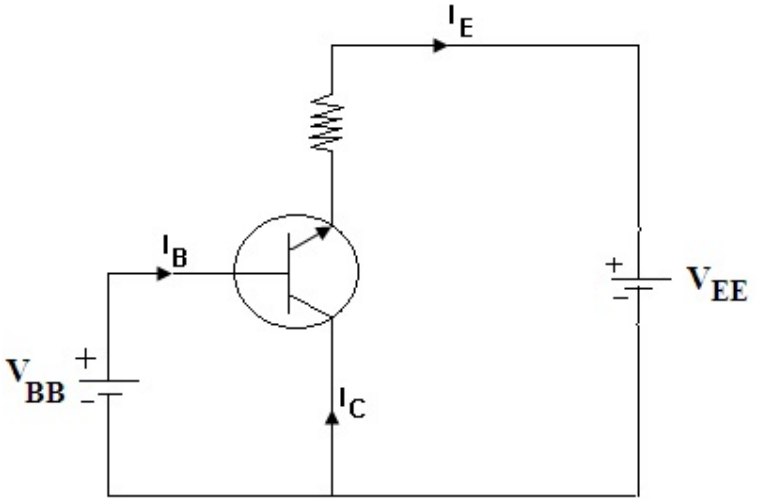
$$\alpha = I_C/I_B$$



Fig(d):

3.4.3 Common Collector Configuration

In common collector configuration, collector terminal is common to both input and output. Circuit arrangement in CC configuration for NPN transistor is shown in figure below. Here input is applied between base and collector, while output is taken from emitter.CC configuration provides very high input resistance and very low output resistance. Due to this reason the voltage gain of this configuration is less than unity. Therefore this circuit is not used for amplification. It can be used for impedance matching for driving a low impedance load from a high impedance source.



Comparison between Three Transistor Configurations

Properties	Common Base	Common Emitter	Common Collector
Input Impedance	Low	Medium	High
Output Impedance	Very High	High	Low
Voltage Gain	High	Medium	Low
Current Gain	Low	Medium	High
Power Gain	Low	Very High	Medium

3.5 Relation between I_c, I_B, I_E, α and β

The current that flows across the emitter-base junction is known as emitter current I_E, which is the sum of electron current and hole current. The direction of I_E is out of the emitter lead, which is in the direction of hole current and opposite to the direction of the electron current.However,the electron component is much larger than the hole component, the emitter current is dominated by the electron component. Thus,

$$I_E = I_{nE} + I_{pE} = I_{nE}\left(1 + \frac{I_{pE}}{I_{nE}}\right) = I_{nE} \qquad eq(1)$$

A few electrons, which are unable to reach the collector-base junction, will recombine with holes, which are majority carriers in the base. It accounts for a small base current (I_B) that is supplied from the base contact.

$$I_B = I_{pE} + (I_{nE} - I_{nC}) - I_{CBO} \qquad eq(2)$$

Where I_{CBO} is the collector reverse saturation current and is contributed from thermally generated minority carriers.The current direction of I_{CBO} is opposite to that of other two current components.

Most of the diffusing electrons will reach the boundary of the collector-base depletion region. Because the collector is more positive than base, the diffused electrons will swept across the collector-base depletion region into the collector. They will be collected to constitute the collector current(**I_c**).

$$I_C = I_{nC} + I_{CBO} \qquad eq\ (3)$$

I_{CBO} is small compared to **I_{nc}**. Therefore,

$$I_C = I_{nC} \qquad eq\ (4)$$

The emitter current is the sum of the collector and the base current. Hence,

$$I_E = I_B + I_C \qquad eq\ (5)$$

The ratio of the output current to the input current is known as *current gain*. The emitter and collector are respectively the input and output terminals in common base configuration and base is the common terminal. The parameter α is the ratio of the collector current to emitter current is known as ***common base current gain***.

$$\alpha = \frac{I_{nC}}{I_E} = \frac{I_C}{I_E} \qquad eq\ (6)$$

α will always be less than one. From the eqn(3) and (6).We get,

$$\alpha = \frac{I_C - I_{CBO}}{I_E} \qquad eq\ (7)$$

$$I_C = \alpha I_E + I_{CBO} \qquad eq\ (8)$$

From the eqns (1), (3) and (7).We get,

$$\alpha = \frac{I_{nC}}{I_{nE} + I_{pE}} = \gamma\beta^T \qquad eq\ (9)$$

$$\gamma = \frac{I_{nE}}{I_{nE} + I_{pE}} \qquad eq\ (10)$$

$$\beta^T = \frac{I_{nC}}{I_{nE}} = \frac{number\ of\ electrons\ arriving\ at\ the\ collector}{number\ of\ injected\ electrons} \qquad eq\ (11)$$

γ is defined as ***emitter injection efficiency*** and specifies the portion of minority carriers injected in to the base.

β^T is defined as the ***base transport factor***, which designate the portion of surviving electrons. Now substituting the value of **I_c** from eqn (5) and (8), we get

$$I_C = \alpha(I_C + I_B) + I_{CBO} \qquad eq\ (12)$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO} \qquad eq\ (13)$$

$$I_C = \frac{\alpha}{(1-\alpha)} I_B + \frac{1}{(1-\alpha)} I_{CBO} \qquad eq\ (14)$$

Thus,

$$I_C = \beta I_B + \frac{\beta}{\alpha} I_{CBO}$$

$$I_C = \beta I_B + I_{CEO} \qquad eq\ (15)$$

Where,

$$\beta = \frac{\alpha}{(1-\alpha)} \qquad and \qquad I_{CEO} = \frac{I_{CBO}}{1-\alpha}$$

The parameter **β** is called common emitter current gain. For a particular transistor **α** is less than unity and **β** is very large.

Relation between α and β

$\alpha = I_C/I_E$ We know that $I_E = I_B + I_C$ $\alpha = \frac{I_C}{I_B + I_C}$ Dividing numerator and denominator by I_B Therefore, $\alpha = \frac{I_C/I_B}{\frac{I_B}{I_B} + \frac{I_C}{I_B}}$ $\boldsymbol{\alpha = \frac{\beta}{1+\beta}}$	$\beta = I_C/I_B$ $\beta = {I_C}/{I_E - I_C}$ Dividing numerator and denominator by I_E Therefore, $\beta = \frac{I_C/I_E}{\frac{I_E}{I_E} + \frac{I_C}{I_E}}$ $\boldsymbol{\beta = \frac{\alpha}{1-\alpha}}$

3.6 BJT as an Amplifier:

Signal amplification is the simplest and most important signal procesing task and is essential because of weak signal available from the transducer.Such signals are too small for reliable processing signal magnitude should be large enough for easy signal processing without error.The process of increasing the the amplitude of an input signal is called **amplification** and the device used for this process is called **amplifier**.The magority of amplifiers are primarly intended to operate on very small input signal.The objective is to make the signal magnitude larger and therefore are thought of as voltage amplifier.These amplifiers are known as **Small signal voltage amplifier.**

One of the basic feature of the amplifier is that the output wave form must be identical in nature to those in the input waveform.The amplifier preserves the details of the signal waveform and any deviation of the output waveform from the shape of the input waveform is considered as distortion.

The main utility of transisitor lies in its ability of amplifying weak signals.The weak signal is applied at input terminals and the amplified output is obtained across the output terminals as illstrated in figure.

A transistor alone cannot prform the functions of amplification and some passive components such as resistors and capacitors are needed.**Common emitter (CE)** configuration,because of its high current,voltage and power gains,is much suited for most of amplifier circuits.

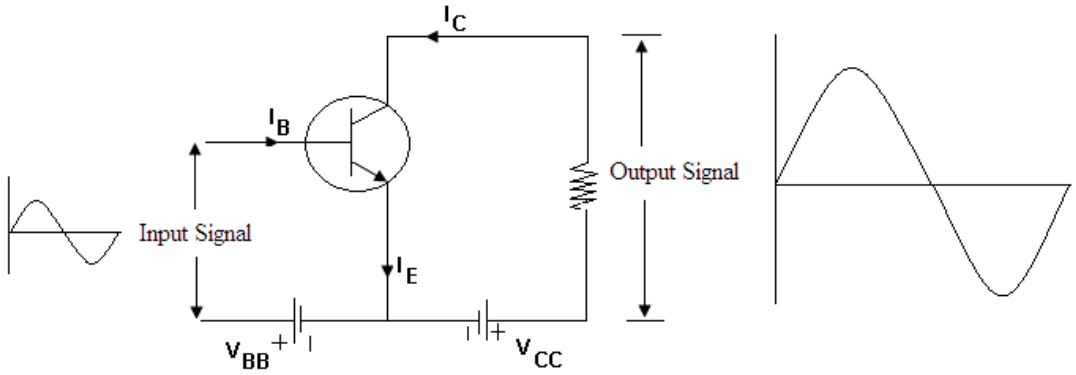
Biasing of an Amplifier

The purpose of biasing of an amplifier is to set dc operating point,ie to fix base current I_B,collector current I_C and collector emitter voltage V_{CE} such that transistor operate in the linear region of the output characteristics even after the superposition of ac signal voltage at the base .The process which set up the initial d.c values of I_B ,I_C and V_{CE} in a transistor is called **Biasing**.

Necessity of Biasing

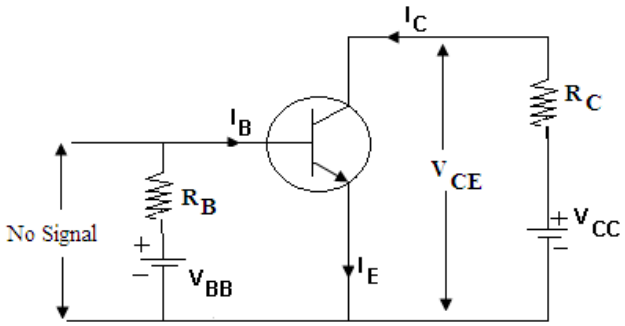
For most of applications,transistors are required to operate as linear amplifiers (i.e, to amplify the output voltage as a linear function of the input voltage).To achive this, it is necessary to operate the transistor over region of its characteristic curves which are linear,parallel and equi-spaced for equel increments of the parameter.Such an operation can be ensured by proper selection of zero signal operating point and limiting the operation of the transistor over the linear operation of the characteristics.For proper selection of zero signal operating point,proper biasing i.e,the application of d.c voltages at emitter to base junction and collector to base junction is required.If transistor is not biased properly,it would work inefficiently and produce distortion in the output signal.

The figure shows the basic amplifier in CE configuration with an NPN transistor.When an input signal is applied in the emitter-base junction,the signal is superimposed in the d.c voltage (**VBB**) at emitter-base junction.Therefore during the positive half-cycle of the input signal the forward bias across the junction increases,because it is already positive with respect to ground.This increase in forward bias increases the base current $\mathbf{I_B}$.Due to increase in base current the collector curent also increases.In **CE** configuration the corresponding increase in collector current will be '**β**' times the increase in $\mathbf{I_B}$.This increase in collector current produces more voltage drop across the output terminal.During negative half-cycle of the input signal the forward bias across emitter junction will be decreased and decreases base curent.This decrease in base current results in corresponding (**β**-times) decrease in collector current.Consequently the drop across output terminals will be decreased.It is clear that the collector current varies according to the input signal applied and variation is **β**-times to that of input current variation.Due to this action an amplified form of input signal can be obtained at the output terminal.



3.7 D.C Load Line

In the amplifier circuit shown in figure, no signal is applied to its input. At this state transistor is said to be ***quiescent condition***. At quiescent state $\mathbf{V_{CC}}$ sends a collector current I_C through the transistor. This current is called **zero signal collector current**. The magnitude of this current depends on the supply voltage $\mathbf{V_{CC}}$, the load resistance $\mathbf{R_c}$ and collector emitter voltage $\mathbf{V_{BE}}$ of the transistor.As $\mathbf{I_c}$ flows through $\mathbf{R_c}$ and the transistor,it will make voltage drops across $\mathbf{R_c}$ and transistor.



Applying krichoffs voltage law (KVL) to the collector circuit,We get

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$I_C = \left(\frac{V_{CC} - V_{CE}}{R_C}\right)$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

$$I_C = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C}$$

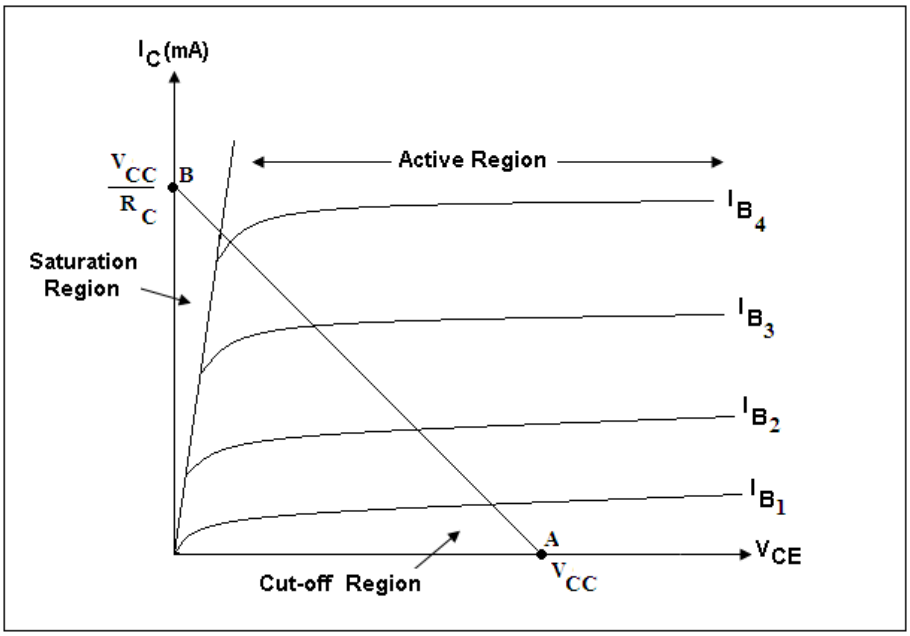
$$I_C = (-1/R_C)V_{CE} + \frac{V_{CC}}{R_C}$$

As R_C and V_{CC} are constants, the above equation is of the form

$$y = mx + b$$

which is standard form of the equation of a straight line AB.

If this equation is plotted on the output characteristics of the transistor, we get a straight line as shown in figure. The slope of the line is $(-1/R_c)$.This straight line is called **d.c load line.**



Here the co-ordinates of A are obtained by writing I_c=0 in equation of V_{cc}.

$$V_{CC} = 0 \times R_C + V_{CE}$$

$$V_{CC} = V_{CE}$$

Thus the co-ordinates of end 'A' are

$$V_{CE} = V_{CC}$$

$$I_C = 0$$

The co-ordinates of end 'B' are obtained by writing $V_{CE} = 0$ in the equation

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CC} = I_C R_C + 0$$

$$I_C = {}^{V_{CC}}/_{R_C}$$

Thus the co-ordinates of end 'B' are

$$V_{CE} = 0$$

$$I_C = {}^{V_{CC}}/_{R_C}$$

Knowing the values of R_c and V_{cc} the end points of the load line can be located. By joining the end points by a straight line, we get d.c load line.

Selection of Operating Point

In order to get faithful amplification,the operating point must be well within the active region of the transistor.For useful operation,the collector current should not exceed the maximum current rating. Also the collector to emitter voltage V_{CE} should not exceed the value prescribed by the manufacturer.

3.8 Stabilisation

The collector current in a transistor changes rapidly when

(*i*) the temperature changes,

(*ii*) the transistor is replaced by another of the same type. This is due to the inherent variations of transistor parameters.

When the temperature changes or the transistor is replaced, the operating point (*i.e.* zero signal I_C and V_{CE}) also changes. However, for faithful amplification, it is essential that operating point remains fixed. This necessitates to make the operating point independent of these variations. This is known as stabilisation. *The process of making operating point independent of temperature changes or variations in transistor parameters is known as* **stabilisation.**

Once stabilisation is done, the zero signal *IC* and *VCE* become independent of temperature variations or replacement of transistor *i.e.* the operating point is fixed. A good biasing circuit always ensures the stabilisation of operating point.

Need for stabilisation. Stabilisation of the operating point is necessary due to the following reasons :

(*i*) Temperature dependence of I_C

(*ii*) Individual variations

(*iii*) Thermal runaway

(*i*) Temperature dependence of I_C. The collector current I_C for CE circuit is given by:

$I_C = \beta I_B + I_{CEO} = \beta I_B + (\beta + 1) I_{CBO}$

The collector leakage current I_{CBO} is greatly influenced (especially in germanium transistor) by temperature changes. A rise of 10°C doubles the collector leakage current which may be as high as 0.2 mA for low powered germanium transistors. As biasing conditions in such transistors are generally so set that zero signal I_C = 1mA, therefore, the change in I_C due to temperature variations cannot be tolerated. This necessitates to stabilise the operating point *i.e.* to hold I_C constant in spite of temperature variations.

(*ii*) Individual variations. The value of β and V_{BE} are not exactly the same for any two transistors even of the same type. Further, V_{BE} itself decreases when temperature increases. When a transistor is replaced by another of the same type, these variations change the operating point. This necessitates to stabilise the operating point *i.e.* to hold *IC* constant irrespective of individual variations in transistor parameters.

(*iii*) Thermal runaway. The collector current for a *CE* configuration is given by : $I_C = \beta I_B + (\beta + 1) I_{CBO}$. The collector leakage current I_{CBO} is strongly dependent on temperature. The flow of collector current produces heat within the transistor. This raises the transistor temperature and if no stabilisation is done, the collector leakage current I_{CBO} also increases. It is clear from the above equation that if I_{CBO} increases, the collector current I_C increases by $(\beta + 1) I_{CBO}$. The increased I_C will raise the temperature of the transistor, which in turn will cause I_{CBO} to increase. This effect is cumulative and in a matter of seconds, the collector current may become very large, causing the transistor to burn out. *The self-destruction of an unstabilised transistor is known as* **thermal runaway.**

In order to avoid thermal runaway and consequent destruction of transistor, it is very essential that operating point is stabilised *i.e*. I_C is kept constant. In practice, this is done by causing I_B to decrease automatically with temperature increase by circuit modification. Then decrease in βI_B will compensate for the increase in $(\beta + 1) I_{CBO}$, keeping *IC* nearly constant. In fact, this is what is always aimed at while building and designing a biasing circuit.

The biasing network associated with the transistor should meet the following requirements:

(*a*) It should ensure proper zero signal collector current.

(*b*) It should ensure that V_{CE} does not fall below 0.5 V for *Ge* transistors and 1 V for silicon transistors at any instant.

(*c*) It should ensure the stabilisation of operating point.

Stability Factor (S)

To what extend the collector current has been stabilized in respect of variation in temperature is expressed in terms of stability factor 'S' .The stability factor is defined as the rate of change of the collector current with respect to the leakage current when other parameters (I_B,β)are held constant.

i.e , $S = \frac{dI_C}{dI_{CO}}$; I_B, β constant

Stability factor shows the change in collector current I_c because of change in collector leakage current I_{co}. Here the smaller value of 'S' better will be the stability. Therefore stability factor should be kept small as possible. The ideal value of stability factor is one, but it is not practicable.

Expression for the Stability Factor

We Know

$$I_C = \beta I_B + (\beta + I_{CO})$$

Differentiating above expression *w.r.t*. I_C, we get,

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1)) \frac{dI_{CO}}{dI_C}$$

$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S} \qquad Since,\ S = \frac{dI_C}{dI_{CO}}$$

$$S = \frac{(\beta+1)}{1-\beta(\frac{dI_B}{dI_C})}$$

3.9 Transistor Biasing Circuits:

The BJT can be biased to fix the quiescent operating point by different methods.

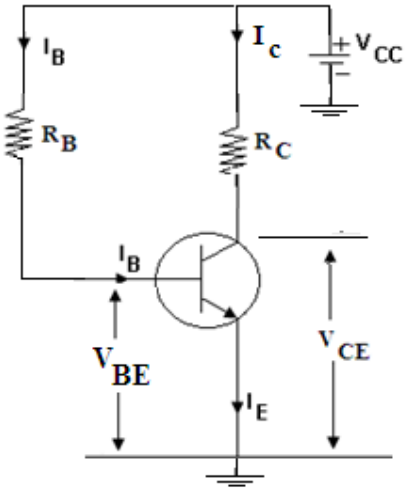
The following are the commonly used methods for transistor biasing;

- Fixed bias (base resistor bias)

- Collector to base bias (Feed back resistor bias)
- Emitter resistor bias
- Voltage divider bias

3.9.1 Fixed Bias (base resistor bias)

This is the simplest type of transistor biasing. In this method a single resistor $\mathbf{R_B}$ is connected between the base and positive terminal of $\mathbf{V_{cc}}$ as shown in figure. Here a single battery $\mathbf{V_{cc}}$ is used to provide both $\mathbf{V_{cc}}$ and $\mathbf{V_{BB}}$. The value of $\mathbf{R_B}$ has to be chosen suitably so as to get the desired operating point.



Analysis of input section

Applying KVL to the input section,we get

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = {(V_{CC} - V_{BE})}/{R_B}$$

$$I_B = {V_{CC}}/{R_B} \qquad (since\ V_{BE} \ll V_{CC})$$

Then the value of the base resistor can be determined by

$$R_B = {V_{CC}}/{I_B}$$

Since the supply voltage **Vcc** is a fixed known value, once $\mathbf{R_B}$ is chosen the base current $\mathbf{I_B}$ will be fixed in value. For this reason this biasing circuit is called ***Fixed bias circuit***.

Analysis of output section

Considering the output section, the collector current is given by,

$$I_C = \beta I_B + I_{CEO}$$

The leakage current $\mathbf{I_{CEO}}$ is small compared to the total collector current, there fore

$$I_C = \beta I_B$$

Applying Kirchhoff's voltage law to the output circuit, We get

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

This value of $\mathbf{V_{CE}}$ and calculated value of $\mathbf{I_c}$ provide the co-ordinates of the operating point.

Advantages

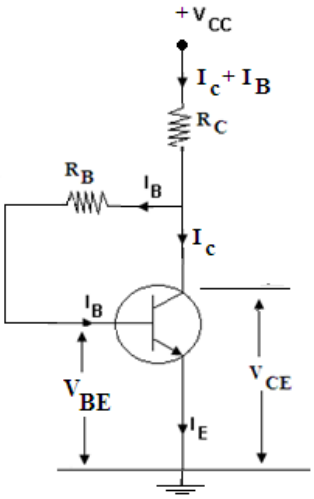
- Very simple in construction.
- Operating point can be fixed at any desired part of the active region just by suitably changing the value of $\mathbf{R_B}$.

Disadvantages

- Temperature stabilization of the operating point is very poor; because rise in temperature increases the collector current and thus the operating point is shifted.
- High stability factor.

3.9.2 Collector to base bias (Feed back resistor bias)

Here the base resistor $\mathbf{R_B}$ is connected to the collector instead of connecting to the $\mathbf{V_{cc}}$ as shown in figure.



Analysis of input section

Applying KVL to the input section,we get

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_C R_C + I_B(R_C + R_B) + V_{BE} \qquad eq\ (1)$$

$$I_B = \frac{(V_{CC} - I_C R_C) - V_{BE}}{R_C + R_B} \qquad eq\ (2)$$

Then

$$R_B = \frac{(V_{CC} - I_C R_C) - V_{BE}}{I_B} - R_C \qquad eq\ (3)$$

Analysis of output section

Applying KVL to the output section,we get

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C \qquad eq\ (4)$$

Substituting this value of **VCE** in eqn(2) we get,

$$I_B = \frac{V_{CE} - V_{BE}}{R_C + R_B}$$

The collector current I_C is given by

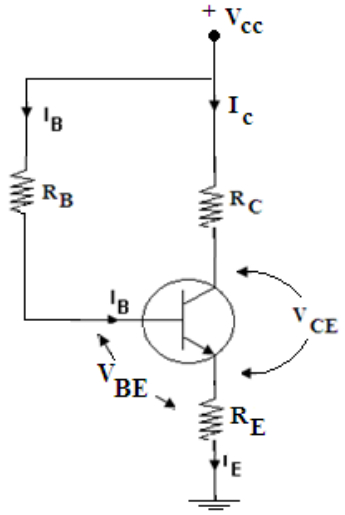
$$I_C = \beta I_B$$

$$I_C = \beta \left(\frac{V_{CE} - V_{BE}}{R_C + R_B}\right)$$

The co-ordinates of the operating point $\mathbf{V_{CE}}$ and $\mathbf{I_c}$ are now obtained.

3.9.3 Emitter resistor bias

Here the resistor R_E is connected in between the emitter and ground as shown in figure.



Analysis of input section

Applying KVL to the input section,we get

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E \qquad eq\ (1)$$

$$I_B = {(V_{CC} - V_{BE} - I_E R_E)}/{R_B}$$

$$I_B = {(V_{CC} - I_E R_E)}/{R_B} \qquad \text{eq (2)}$$

$$(Since\ V_{BE} \ll V_{CC})$$

We know

$$I_E = (\beta + 1) I_B$$

Substituting this in eq (1), we get

$$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

$$I_B = {(V_{CC} - V_{BE})}/{(R_B + (\beta + 1) R_E)}$$

$$I_B = {V_{CC}}/{(R_B + \beta R_E)}$$

$$(Since\ V_{BE} \ll V_{CC}\ and\ 1 \ll \beta\ )$$

We know

$$I_C = \beta I_B$$

$$I_C = {\beta V_{CC}}/{(R_B + \beta R_E)}$$

$$I_C = \frac{V_{CC}}{R_E + (R_B/\beta)}$$

This gives the one co-ordinate I_C of operating point

Analysis of output section

Applying KVL to the output section, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

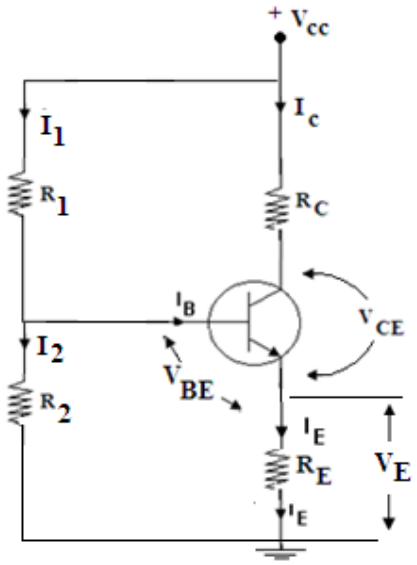
$$V_{CE} = V_{CC} - (R_C + R_E) I_C$$

$$(Since\ I_C \cong I_E)$$

This gives the second co-ordinate (V_{CE}) of the operating point.

3.9.4 Voltage Divider Bias

This is the most widely used method for providing biasing and stabilization for transistor. The figure shows the voltage divider biasing arrangement for an NPN transistor. Here two resistors **R_1** and **R_2** in series are connected across the supply voltage V_{cc}. A resistor **R_E** is also connected in the emitter circuit.



Analysis of input section

Here current through R_1 is will almost completely flow through R_2.ie, **I_B** is very small.

$$I_1 = I_2$$

Applying KVL to the input section, we get

$$V_{CC} = I_1R_1 + I_1R_2$$

$$I_1 = {}^{V_{CC}}/_{(R_1 + R_2)}$$

Then the voltage at the base relative to the ground is given by

$$V_B = I_1R_2$$

$$V_B = \frac{V_{CC}}{(R_1 + R_2)}R_2$$

The drop across R_E is the difference between V_B and V_{BE}.

$$I_ER_E = V_B - V_{BE}$$

$$I_E = (V_B - V_{BE})/R_E$$

$$I_C = (V_B - V_{BE})/R_E \qquad (Since\ I_C = I_E)$$

$$I_C = V_B/R_E \qquad (Since\ B_{BE} \ll V_B)$$

Now one co-ordinate (I_C) of the operating point is obtained.

Analysis of output section

Applying KVL to the output section, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_C$$

$$(Since\ I_C \cong I_E)$$

Now the second co-ordinate of the operating point (V_{CE}) is also obtained. Here the value of **β** has never entered in to the calculation. Hence, change in **β** value has no effect on the operating point.

Advantage

- Super in stabilization hence it is most popular.

3.9.5 Design of Transistor Biasing Circuits

In practice, the following steps are taken to design transistor biasing and stabilisation circuits :

Step 1. It is a common practice to take R_E = 500 – 1000Ω. Greater the value of R_E, better is the stabilisation. However, if R_E is very large, higher voltage drop across it leaves reduced voltage drop across the collector load. Consequently, the output is decreased. Therefore, a compromise has to be made in the selection of the value of R_E.

Step 2. The zero signal current I_C is chosen according to the signal swing. However, in the initial stages of most transistor amplifiers, zero signal I_C = 1mA is sufficient. The major advantages of selecting this value are :

(*i*) The output impedance of a transistor is very high at 1mA. This increases the voltage gain.

(*ii*) There is little danger of overheating as 1mA is quite a small collector current.

It may be noted here that working the transistor below zero signal I_C = 1mA is not advisable because of strongly non-linear transistor characteristics.

Step 3. The values of resistances R_1 and R_2 are so selected that current I_1 flowing through R_1 and R_2 is atleast 10 times I_B *i.e.* $I_1 \geq 10\ I_B$. When this condition is satisfied, good stabilisation is achieved.

Step 4. The zero signal I_C should be a little more (say 20%) than the maximum collector current swing due to signal. For example, if collector current change is expected to be 3mA due to signal, then select zero signal $I_C \cong$ 3.5 mA. It is important to note this point. Selecting zero signal I_C below this value may cut off a part of negative half-cycle of a signal. On the other hand, selecting a value much above this value (say 15mA) may unnecessarily overheat the transistor, resulting in wastage of battery power. Moreover, a higher zero signal I_C will reduce the value of R_C (for same V_{CC}), resulting in reduced voltage gain.

3.10 R-C Coupled Amplifier:

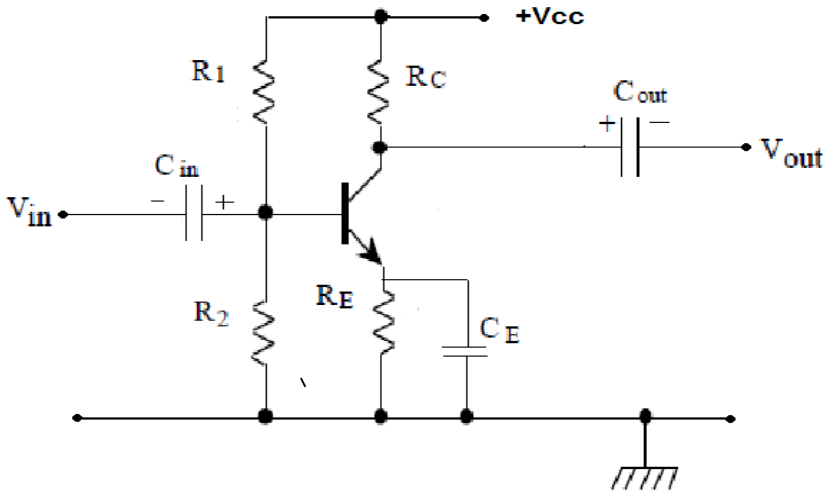


Fig:R-C Coupled Amplifier

Circuit description

The figure shows the single stage Common emitter R-C Coupled amplifier circuit.Here both forward bias voltage at emitter-base junction and reverse bias voltage at the collector-emitter junction are derived from the single supply voltage $\mathbf{V_{cc}}$.

The magnitude of these bias voltages are adjusted to operate the transistor in active region.In this arrangement base is the input terminal and collector is the output terminal.The resistors $\mathbf{R_1}$,$\mathbf{R_2}$ and $\mathbf{R_E}$ form the biasing network.In multistage amplifiers coupling from one stage to next stage is obtained by a coupling capacitor followed by a connection to a shunt resistor,therefore such amplifiers are called **Resistance-Capacitance coupled** or **R-C Coupled amplifiers**.The input capacitor $\mathbf{C_{in}}$ couples a.c signal voltage to base of the transistor.In the absence of $\mathbf{C_{in}}$ the signal source will be in parallel with resistor $\mathbf{R_2}$ and the bias will be affected.Thus the function of $\mathbf{C_{in}}$ is to allow only the alternating current from the signal source to flow in to the input circuit.The emitter bypass capacitor $\mathbf{C_E}$,offers low reactance path to the signal.If it is not present ,the the voltage drop across $\mathbf{R_E}$ will reduce the effective voltage available across the base-emitter terminals (the input voltage) and thus reduces the gain.The coupling capacitor $\mathbf{C_{out}}$ transmits a.c signal but blocks the d.c voltage of the first stage from reaching the base of the second stage in the case of multistage amplifiers.Thus the d.c biasing of the next stage in not interfered with.For this reason,the coupling capasitor $\mathbf{C_{out}}$ is also called the blocking capacitor.

Working

When an input signal is applied in the emitter-base junction,the signal is superimposed in the d.c voltage at emitter-base junction.Therefore during the positive half-cycle of the input signal the forward bias across the junction increases,because it is already positive with respect to ground.This increase in forward bias

increases the base current $\mathbf{I_B}$.Due to increase in base current the collector current also increases. In **CE** configuration the corresponding increase in collector current will be '**β**' times the increase in $\mathbf{I_B}$. This increase in collector current produces more voltage drop across the output terminal. During negative half-cycle of the input signal the forward bias across emitter junction will be decreased and decreases base curent. This decrease in base current results in corresponding (**β**-times) decrease in collector current.Consequently the drop across output terminals will be decreased.It is clear that the collector current varies according to the input signal applied and variation is **β**-times to that of input current variation.Due to this action an amplified form of input signal can be obtained at the output terminal.

In common emitter amplifier the input and output voltages are of 180 degree out of phase,even though the input and output currents are in phase.It means that when the input voltage increases in positive direction the output voltage increases in negative direction and vice versa.When the input signal increases in the positive half cycle it increases the forward bias on emitter junction,which inturn increase the base current and results in increase of collector current.Hence the drop across $\mathbf{R_c}$ increases.$\mathbf{V_{cc}}$ is kept constant.The output of the circuit is taken from collector and emitter and is given by the equation,$\mathbf{V_{CE}=V_{cc}-I_cR_c}$.This indicates that as the signal voltage increases in the positive half cycle,the output voltage increases in negative direction.

Frequency Response and Bandwidth:

An important characterization of an amplifier is in terms of its response to input sinusoids of different frequencies.Such characterization of amplifier perfomance is known as **frequency response** of the amplifier. The ratio of the amplitude of the output sinusiod (Vo) to the amplitude of the input sinusiod (Vi) is the magnitude of the amplifier gain at frequency,**f**.

$$|\boldsymbol{A_v(f)}| = \boldsymbol{V_o/V_i} \;\; \boldsymbol{and} \;\; \angle \boldsymbol{A_v(f)} = \boldsymbol{0^0}$$

The values of $|\boldsymbol{A_v}|$ and $\angle \boldsymbol{A_v}$ are measured with different frequencies of the input sinusoid and the gain magnitude and phase angle are plotted with frequency.These two plots together constitute the frequency response of the amplifier ; the first is known as *amplitude response* and second is known as *phase response.*The voltage gain in decibel(dB) may be expressed as

$$Voltage\ gain\ in\ dB = 20\ log_{10}\ V_o/V_i$$

The frquency response curve of a typical R-C Coupled amplifier is shown in figure.

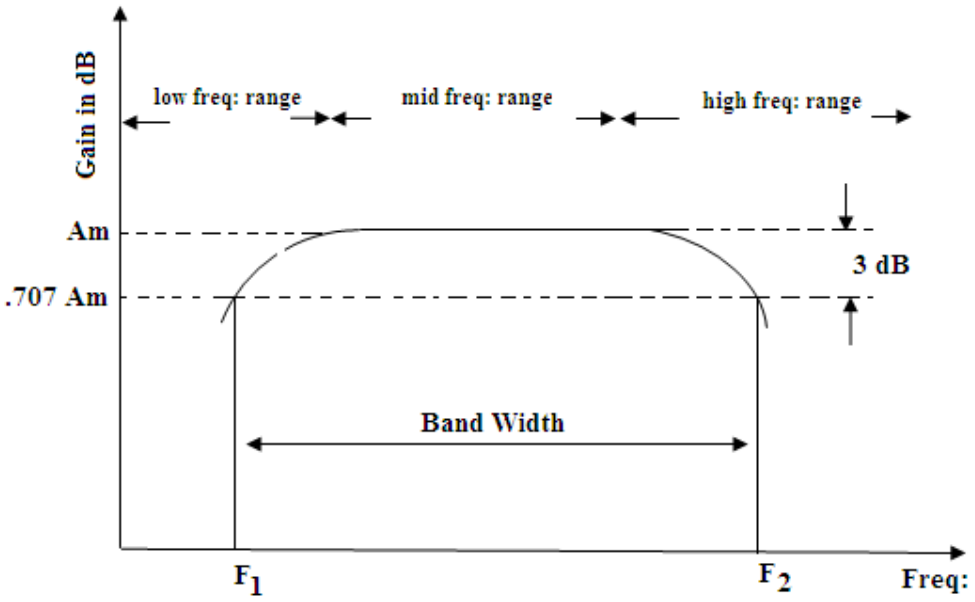


Fig: **Frequency Response of an RC Coupled Amplifier**

At *lower frequencies* (below 50Hz) higher capacitive reactance of coupling capacitor allows very small part of signal to pass from one stage to next and also because of higher reactance of emitter bypass capacitor C_E,the emitter resistor R_E is not shunted. Thus the voltage gain falls off at low frequencies.

In the *mid frequency ran*ge (50Hz -20KHz),the voltage gain of the amplifier is constant.With increase in frequency in this range ,the reactance of the coupling capacitor reduces thereby increasing the gain but at the same time lower capacitive reactance causes higher loading resulting in lower voltage gain.Thus the two effect cancel each other and uniform gain is obtained in mid frequency range.

At *high frequencies* (exceeding 20 KHz),gain of amplifier decreases with increase in frequency. At high frequencies,the reactance of coupling capacitor become very small and it behaves as a short-circuit.This increases the loading of the next stage and reduces the voltage gain. The other factor responsible for the reduction in gain at higher frequencies is the presence of inter electrode capacitance C_{bc} between base and collector.It connects the output with the input. Because of this, negative feedback takes place in the circuit and the gain decreases. This feedback effect is more, when C_{bc} provides a path for higher frequency ac currents.

In the figure f1 and f2 are lower and upper cut-off frequencies respectively.The difference between *upper cut-off frequency*(f_2) and *lower cut-off frequency*(f_1) is called the **Bandwidth(BW)**.

$$Bandwidth = f_2 - f_1$$

A_m is the maximum gain or mid frequency of the amplifier.It means at these frequencies ,the output voltage is $1/\sqrt{2}$ times the maximum voltage.Since the power is proportional to the square of the voltage,the

output power at these cut-off frequencies become one half of the power at mid-frequencies.On dB scale this is equal to a reduction in power by 3dB.For this reason these frequencies are also called **3 dB frequencies.**

Advantages of R-C Coupled Amplifier:

- Excellent frequency response.
- Cheaper in cost.
- Very compact circuit.

Disadvantages of R-C Coupled Amplifier:

- Low voltage and power gain.
- Tendency of becoming noisy with age.
- Poor impedence matching.

Aplications

Widely used as **voltage amplifiers** because of their excellent audio-fidelity over a wide range of frequency.

3.11 Transistor As a Switch

When used as an AC signal amplifier, the transistors Base biasing voltage is applied in such a way that it always operates within its "active" region, that is the linear part of the output characteristics curves are used. However, both the NPN & PNP type bipolar transistors can be made to operate as "ON/OFF" type solid state switches by biasing the transistors base differently to that of a signal amplifier.

Solid state switches are one of the main applications for the use of transistors, and transistor switches can be used for controlling high power devices such as motors, solenoids or lamps, but they can also used in digital electronics and logic gate circuits.

The areas of operation for a Transistor Switch are known as the Saturation Region and the Cut-off Region**.** This means then that we can ignore the operating Q-point biasing and voltage divider circuitry, which are required for amplification, and use the transistor as a switch by driving it back and forth between its "fully-OFF" (cut-off) and "fully-ON" (saturation) regions.

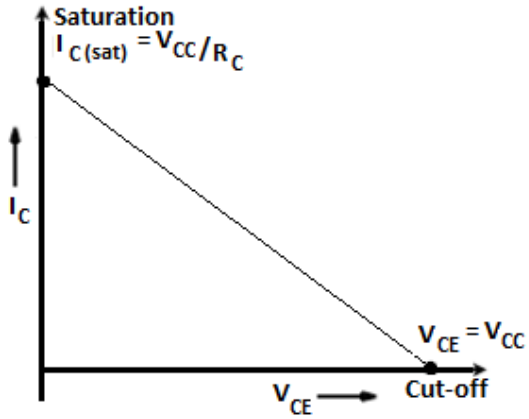


Fig: Load Line

In the cut-off region, both junctions are reverse biased, $V_{BE} < 0.7v$. So input base current (I_B) and output collector current (I_C) are zero. Therefore, no current is flowing through the device. Therefore the transistor is switched "Fully-OFF". In saturation region both junctions are forward biased so that the maximum amount of base current is applied, resulting in maximum collector current. So that maximum current flowing through the transistor. Therefore the transistor is switched "Fully-ON".

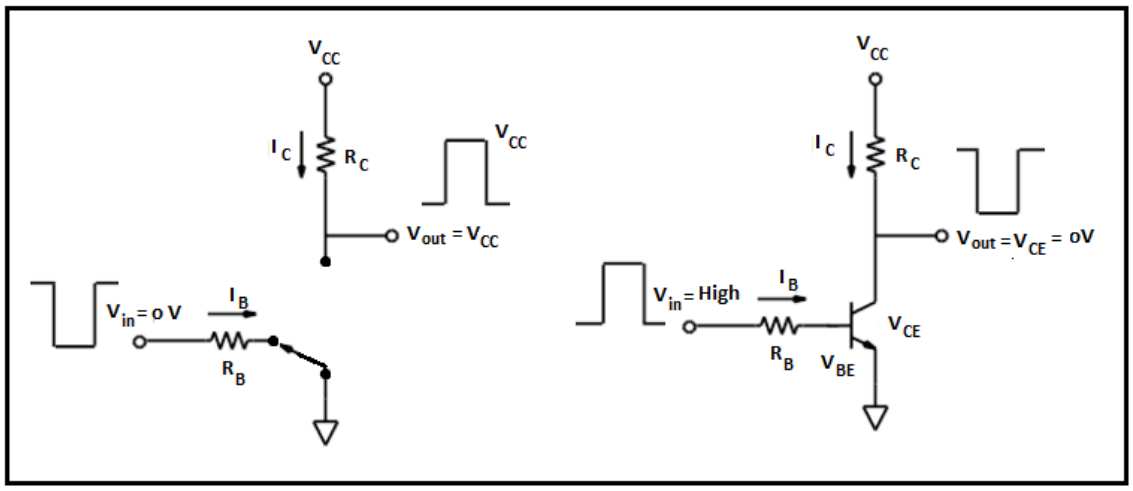


Fig: Transistor as a Switch

When the input voltage (v_{in})= 0, transistor will be in cut-off, $I_C = 0$, and $v_{out} = V_{CC}$ (open switch). When the input voltage (v_{in}) is in "high" state, transistor will be in saturation with $v_{out} = v_{CE} = V_{sat} \approx 0.2$ V and $I_C = (V_{CC} - V_{sat})/R_C$ (closed switch). When R_C is replaced with a load, this circuit can switch a load ON or OFF.

An actual BJT switch differs from the ideal switch in several aspects. In practice, even in cutoff there is some leakage current through the transistor. Also, in saturation, there is always some voltage dropped across the transistor's internal resistance. Typically, this will be between 0.2 and 0.4 V in saturation depending on the collector current and size of the device. These variations from the ideal are generally minor with a properly sized device, so we can assume near ideal conditions when analyzing or designing a BJT switch circuit.

3.12 Transistor Specification Parameters

Type number	The type number of the device is a unique identifier given to each type of transistor. There are three international schemes that are widely used: European Pro-Electron scheme; US JEDEC (numbers start with 2N for transistors); and the Japanese system (numbers start with 2S).
Case	There is a wide variety of case styles. They often start with TOxx for leaded devices or SOTxxx for surface mount devices.
Polarity	There are two types of transistor: NPN and PNP. It is important to choose the correct type otherwise all the circuit polarities will be wrong.
Material	The two main types of material used for transistors are germanium and silicon. Other materials are used, but in very specialised transistors. A knowledge of the type of material used is important because it affects many properties, e.g. forward bias for the base emitter junction is 0.2 - 0.3 V for germanium and ~0.6 V for silicon.
V_{CEO}	Collector to Emitter breakdown voltage. This is the maximum voltage that can be placed from the collector to the emitter. It is normally measured with the base open circuit - hence the letter "0" in the abbreviation. The value should not be exceeded in the operation of the circuit otherwise damage may occur.
V_{CBO}	Collector to base breakdown voltage. This is the maximum collector base voltage - gain it is generally measured with the emitter left open circuit. This value should not be exceeded in the operation of the circuit.
I_C	Collector current, normally defined in milliamps, but high power transistors may be quoted in amps. The important parameter is the maximum level of collector current. This figure should not be exceeded otherwise the transistor may be subject to damage.
V_{CEsat}	The collector emitter saturation voltage, i.e. the voltage across the transistor (collector to emitter) when the transistor is turned hard on. It is normally quoted for a particular base and collector current values.

hfe	hfe (common-emitter current gain or static forward current transfer ratio) is defined as the ratio of the input dc current and the output dc current of the transistor (static current gain). This parameter is also known as β. The ratio of collector current to base current, β is the fundamental parameter characterizing the amplifying ability of a bipolar transistor. β is usually assumed to be a constant figure in circuit calculations, but unfortunately this is far from true in practice. As such, manufacturers provide a set of β (or "hfe") figures for a given transistor over a wide range of operating conditions, usually in the form of maximum/minimum/typical ratings. One popular small-signal transistor, the 2N3903, is advertised as having a β ranging from 15 to 150 depending on the amount of collector current. Generally, β is highest for medium collector currents, decreasing for very low and very high collector currents.
FT	Frequency Transition - the frequency where current gain falls to unity. The transistor should normally be operated well below this frequency.
P_{tot}	Total power dissipation for the device. It is normally quoted for an ambient external temperature of 25^{o}C unless otherwise stated. The actual dissipation across the device is the current flowing through the collector multiplied by the voltage across the device itself.

3.13 Transistor Numbering

There are two main numbering systems for semiconductor diodes, transistors. One numbering or code system is used more widely in Europe and the other in the USA. The European based system is known as the Pro-electron system, sometimes also written as Pro-Electron system, and the one used more widely in North America is the JEDEC coding system.

Joint Electron Device Engineering Council (JEDEC)

These part numbers take the form: digit, letter, sequential number, [suffix]

The letter is always 'N', and the first digit is 1 for diodes, 2 for transistors, 3 for four-leaded devices, and so forth. But 4N and 5N are reserved for opto-couplers. The sequential numbers run from 100 to 9999 and indicate the approximate time the device was first made. If present, a suffix could indicate various things. For example, a 2N2222A is an enhanced version of a 2N2222. It has higher gain, frequency, and voltage ratings. Always check the data sheet.

Examples: 1N914 (diode), 2N2222, 2N2222A, 2N904 (transistors).

NOTE: When a metal-can version of a JEDEC transistor is remade in a plastic package, it is often given a number such as PN2222A which is a 2N2222A in a plastic case.

Pro-Electron

These part numbers take the form: two letters, [letter], sequential number, [suffix]

The first letter indicates the material:

A = Ge

B = Si

C = GaAs

R = compound materials.

The second letter indicates the device type and intended application:

A: diode, RF

B: diode,varactor

C: transistor, AF, small signal

D: transistor, AF, power

E: Tunnel diode

F: transistor, HF, small signal

K: Hall effect device

L: Transistor, HF, power

N: Opto-coupler

P: Radiation sensitive device

Q: Radiation producing device

R: Thyristor, Low power

T: Thyristor, Power

U: Transistor, power, switching

Y: Rectifier

Z: Zener, or voltage regulator diode

The third letter indicates if the device is intended for industrial or commercial applications. It's usually a W, X, Y, or Z. The sequential numbers run from 100-9999.

Examples: BC108A, BAW68, BF239, BFY51.

Instead of 2N and so forth, some manufacturers use their own system of designations. Some common prefixes are:

MJ: Motorola power, metal case

MJE: Motorola power, plastic case

MPS: Motorola low power, plastic case

MRF: Motorola HF, VHF and microwave transistor

RCA: RCA device

TIP: Texas Instruments (TI) power transistor, plastic case

TIPL: TI planar power transistor

TIS: TI small signal transistor (plastic case)

ZT: Ferranti

ZTX: Ferranti

Examples: ZTX302, TIP31A, MJE3055.

Review Questions

Short Answer Questions

1. Why there is a need for biasing an amplifier?

2. Compare the different transistor configurations.

3. Derive the relationship between α and β.

4. Explain early effect.

5. Difine stability factor and explain the need for stabilisation

Essay Questions

1. Draw and explain the output characteristics of CE configuration.
2. Explain the working of RC Coupled transistor amplifier with neat circuit diagram.
3. Expain the frequency response of RC coupled amplifier.
4. Explain the switching action of a transistor.
5. Explain the different specification parameters of a transistor.