to control switching devices in a charge pump, according to any combination of one or more of the following features, each of which contribute to low noise generation in a charge pump. Because it is desirable for the output to have low harmonic content, one distinguishing feature of an embodiment of a charge pump is a clock with an output having low harmonic content as defined by any of the specific harmonic content limits set forth herein. As harmonic content of a clock output is reduced it generally becomes more sinusoidal, so such a clock output may be defined as substantially sine-like. Alternatively, the harmonic power divided by the power at the fundamental frequency fo (*i.e.*, total harmonic distortion "THD"), may be limited to not more than -5 dB, or -10 dB, or -20 dB, or even -30 dB. As a further alternative, such a clock output may be defined as restricted to having third harmonic power that is less than -20 dB, -30 dB, or -40 dB compared to the power at fo. The clock waveform may also be described as containing amplitudes of each harmonic of the fundamental frequency that decrease by at least 20 dB per decade, or by at least 30 dB per decade, or at least 40 dB per decade. Thus, for a waveform having a fundamental operating frequency fo of 8 MHz and an amplitude A_1 for its 8 MHz sinusoidal wave component, the amplitude A_N of every harmonic sinusoidal component at frequency N*fo, N an integer, may be required to be no greater than A_1 reduced by 20, 30 or 40 dB/decade, *i.e.*, A_N (dBA) $\leq A_1$ (dBA) - 2*N, or A_N (dBA) $\leq A_1$ (dBA) - 3*N, or A_N (dBA) $\leq A_1$ (dBA) - 4*N. Which of these varying quality levels is required for the clock waveform will typically depend upon the problem, based on a particular hardware implementation in combination with desired emission limits, which the embodiments described herein are employed to solve.

[012] Low harmonic content signals are not readily produced, or reproduced, by digital circuits, which leads to several features that distinguish and define embodiments of a bias generation method or apparatus with reference to their controlling clocks. Embodiments of certain charge pumps may be defined by having their clock output(s) capacitively coupled to most or all transfer capacitor switches they control, which is rendered advantageous for suitable low-harmonic clock signals due to the limitations of digital circuits. Also, particularly because suitable clock waveforms typically drive a switch into conduction with only half of the peak-to-peak amplitude, it is important that the waveform be large compared to the supply available to generate it. Suitable clock waveforms may be required to have a peak-to-peak amplitude that is at least 95%, 98% or 99% of the amplitude of a supply from which such clock is generated.

[013] As an aid to biasing capacitively coupled control signals to the transfer capacitor switching devices, it may be helpful to employ active bias "resistors," active circuits that couple a bias voltage on a first node to a second node coupled to a transistor control node. A goal is to couple the first node bias voltage to the second node without unduly reducing the amplitude of an alternating drive signal also applied to the second node, which drive signal may be oscillating and may moreover be substantially sine-like. Embodiments of such active bias-coupling circuits may be configured to substantially reduce, compared to the voltage between the two nodes, a voltage appearing across an impedance limiting current between the two nodes, or alternatively may entirely avoid the presence of significant resistors and limit current conduction by capacitive charging, with further current through active devices as may be suitable. They may also substantially preclude current from flowing between the first and second nodes when a voltage therebetween is small compared to peak voltages between the nodes, small being defined as less than about 0.4V, or about 0.8V, or about 1.2V, or being alternatively defined as less than about 25%, or about 50%, or about 70% of the peak voltages. Embodiments may further comprise a capacitive element to charge to a portion of the peak voltage between the first and second nodes, and may be a bridge circuit whereby alternating polarity voltage between the two nodes causes a varying but unipolar voltage across a current limiting circuit. The current limiting circuit comprises a series circuit of a resistor of less than