# *Project 3 Report*

# *4-bit full adder*

# *&*

# *subtractor*

*By:*

*Efai De Leon ID: 36641349*

*Date:*

*11/28/19*

*Professor*

*Maqsood A. Chaudhry*

*EECS 119*

**Introduction:**
In this project, we implement a full adder and subtractor using a standard cell approach. The standard cell approach allows for the design of VLSIC (Very large scale integrated circuits). The method allows the designer to focus on the lowest level aspect of the design process, the layout of the circuit. In this project, we implemented a layout and schematic for every meaningful component. The components are XOR, OR, AND, Inverter, and a 2 to 1 Multiplexer. In order to implement a 4-bit full adder, a simple adder component was fabricated composed of smaller gates.

1. **Circuit Design**

To implement the standard cell approach, the schematic for every gate integrated into the circuit was designed independently. The following are the gates at the schematic level showing the connections for every transistor.

**2 input XOR gate schematic:**
The XOR gate implemented below is an 8 transistor design for 2 inputs. It includes 2 CMOS inverters. The design for the xor gate itself is a transmission gate format. The transistors follow 360-nanometer technology. 5 different terminals are defined: B, S, Vdd, gnd, and xorout.

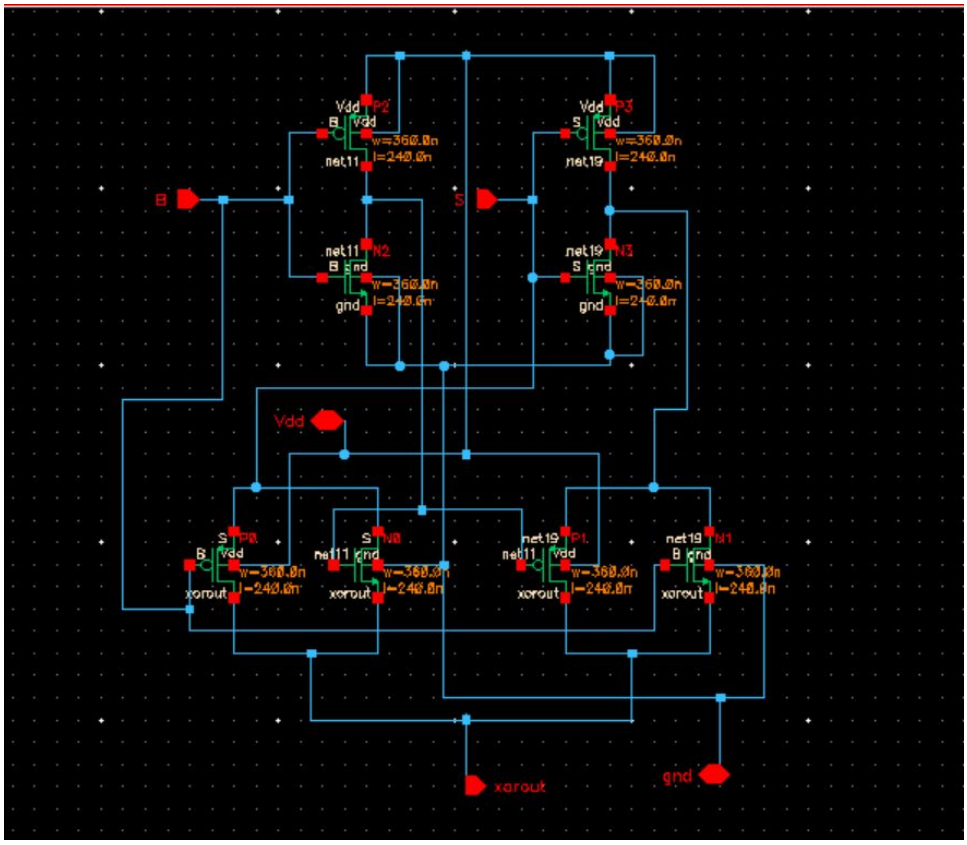



*Figure 1: 2 input XOR gate schematic*

**2 input OR gate schematic:**

The 2-input OR gate implementation below is 6 transistor design. It includes 2 CMOS transistors. The OR gate itself a transmission gate format. The transistors are 360-nanometer technology. 5 terminals are defined: or_input_A, or_input_B, Vdd, gnd, and or_out.

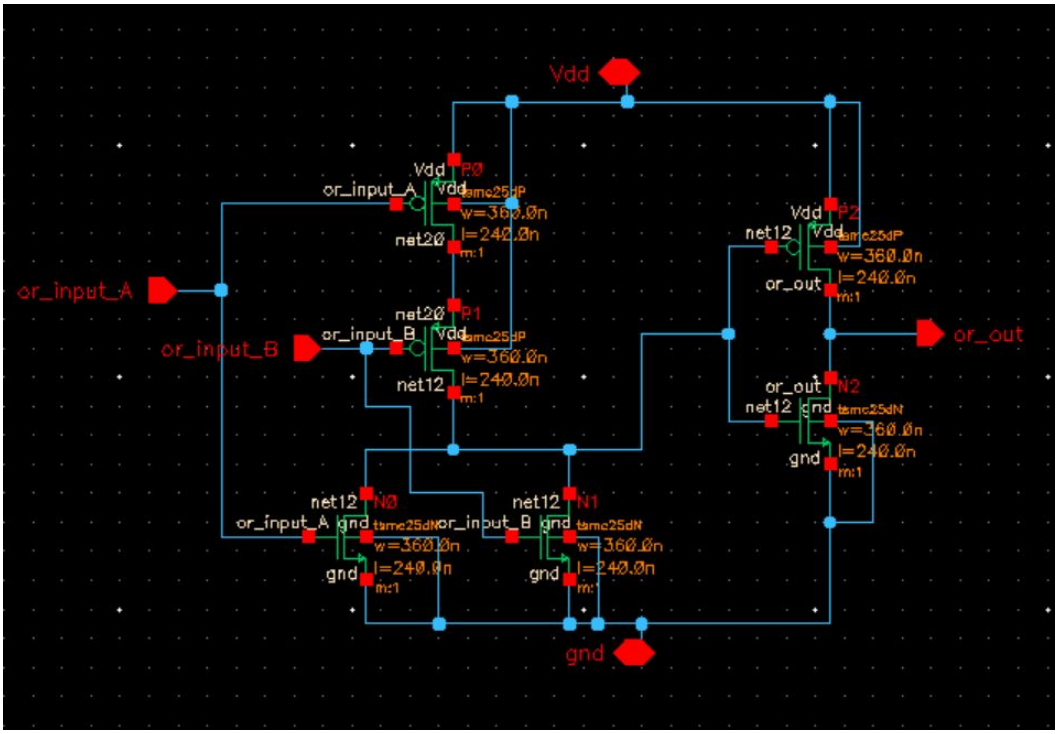



*Figure 2: 2 input OR gate schematic*

**2 input AND gate schematic:**

The 2-input AND gate implementation below is a 6 transistor design. The design is a NAND gate with a CMOS inverter connected to the output. Transistors follow 360-nanometer technology. 5 terminals are defined: and_input_A, and_input_B, Vdd, gnd, and and_out.

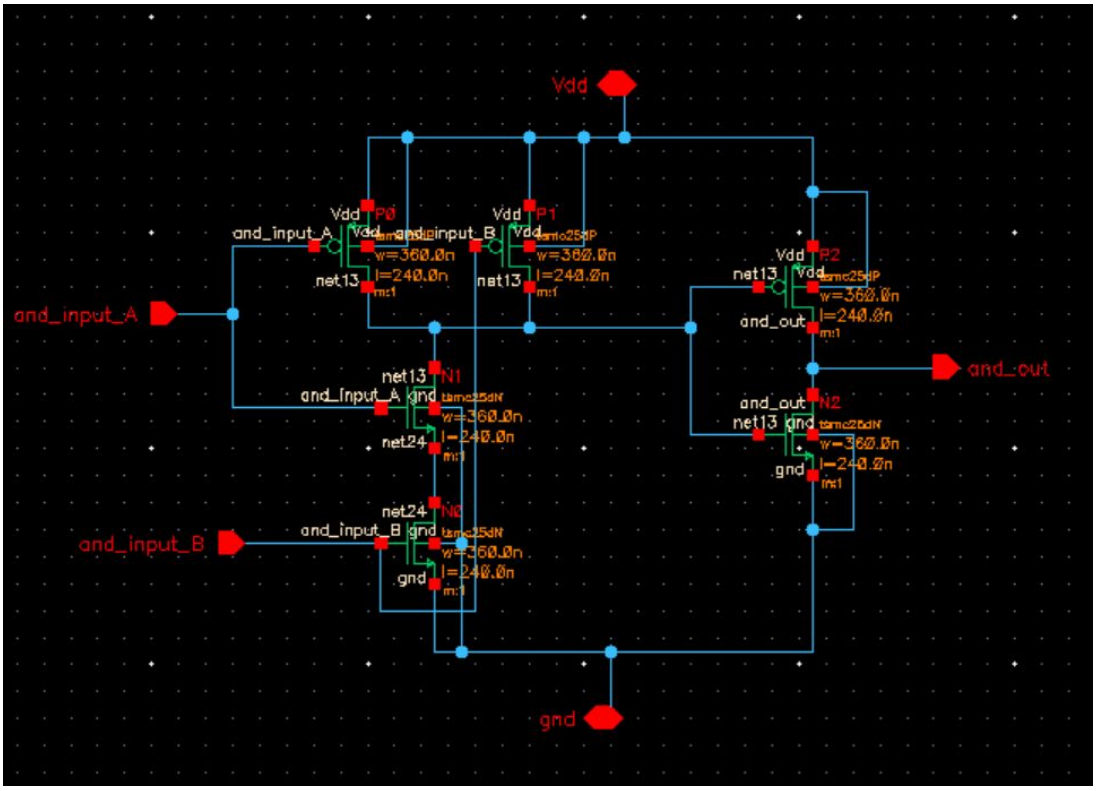



*Figure 3: 2 input AND gate schematic*

**Inverter schematic:**

The following is a simple CMOS inverter. The transistors follow 360-nanometer technology. 4 terminals are defined: inverter_input, Vdd, gnd, and inverter_out. The designed has 2 transistors.

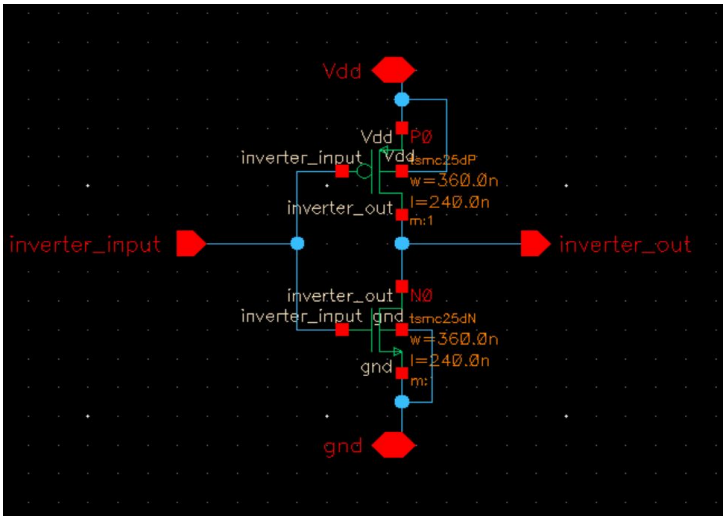



*Figure 4: Inverter Schematic*

**2 input Adder schematic:**

The following is implementation is for a single 2-input adder. The design has 34 transistors all of which follow a 360-nanometer technology. At the top left we have the Terminals S, which determines addition or subtraction (S = 1: subtraction, S = 0: addition), A and B. At the bottom left there are 2 XOR gates with CMOS inverters. At the right side of the schematic, we have two AND gates connected to an OR gate. The adder has 7 terminals: A, B, S, Vdd, gnd, Sum_out, and Cout.

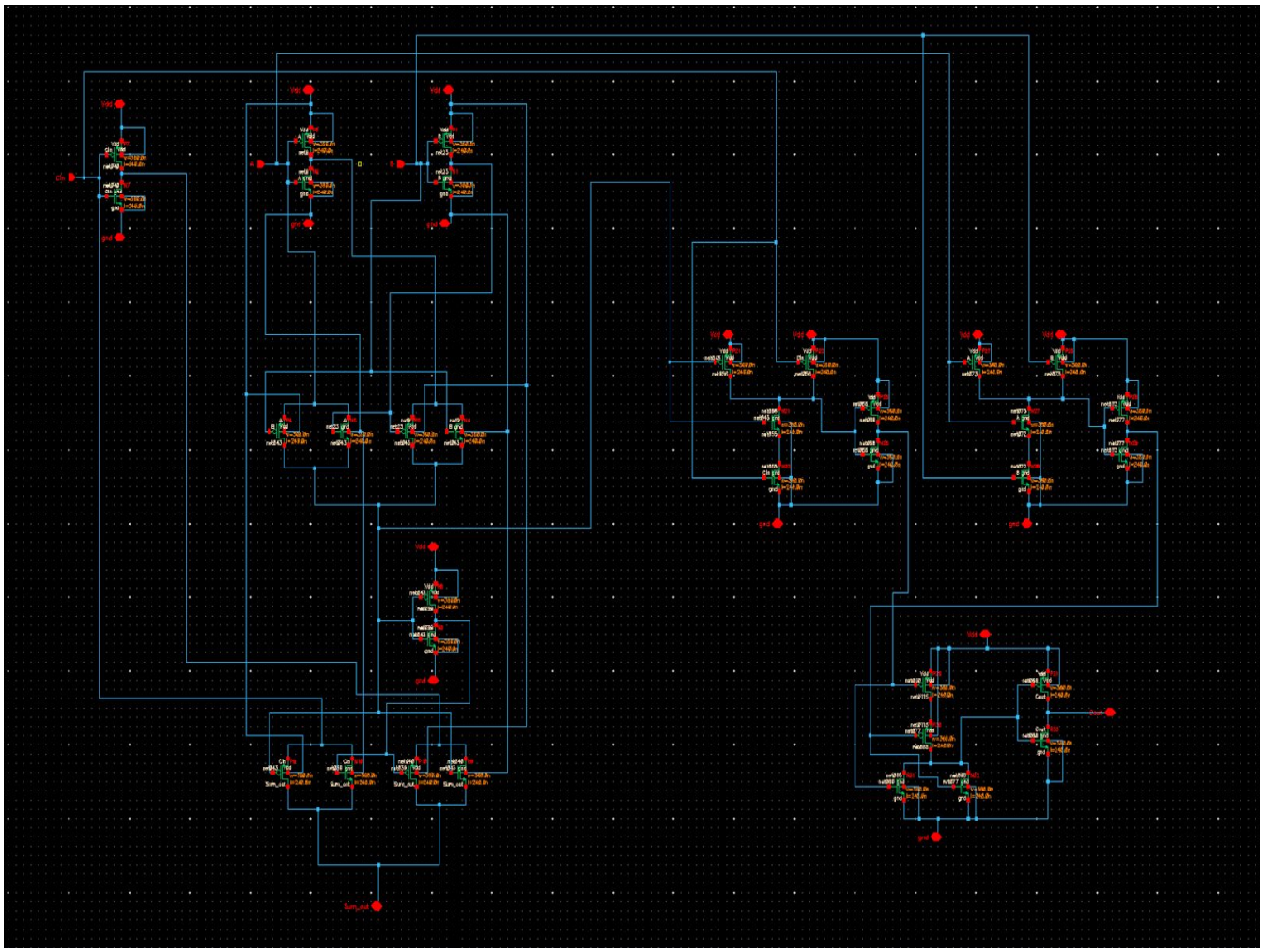


*Figure 5: 2 input Adder schematic*

**2 to 1 MUX schematic:**

The following is the implementation for a 2 to 1 multiplexer. The design has 6 transistors. The circuit has an inverter and two transmission gates. The transistors follow a 360-nanometer architecture. The MUX has 6 terminals: M, D, C, Vdd, gnd, and mux_out.

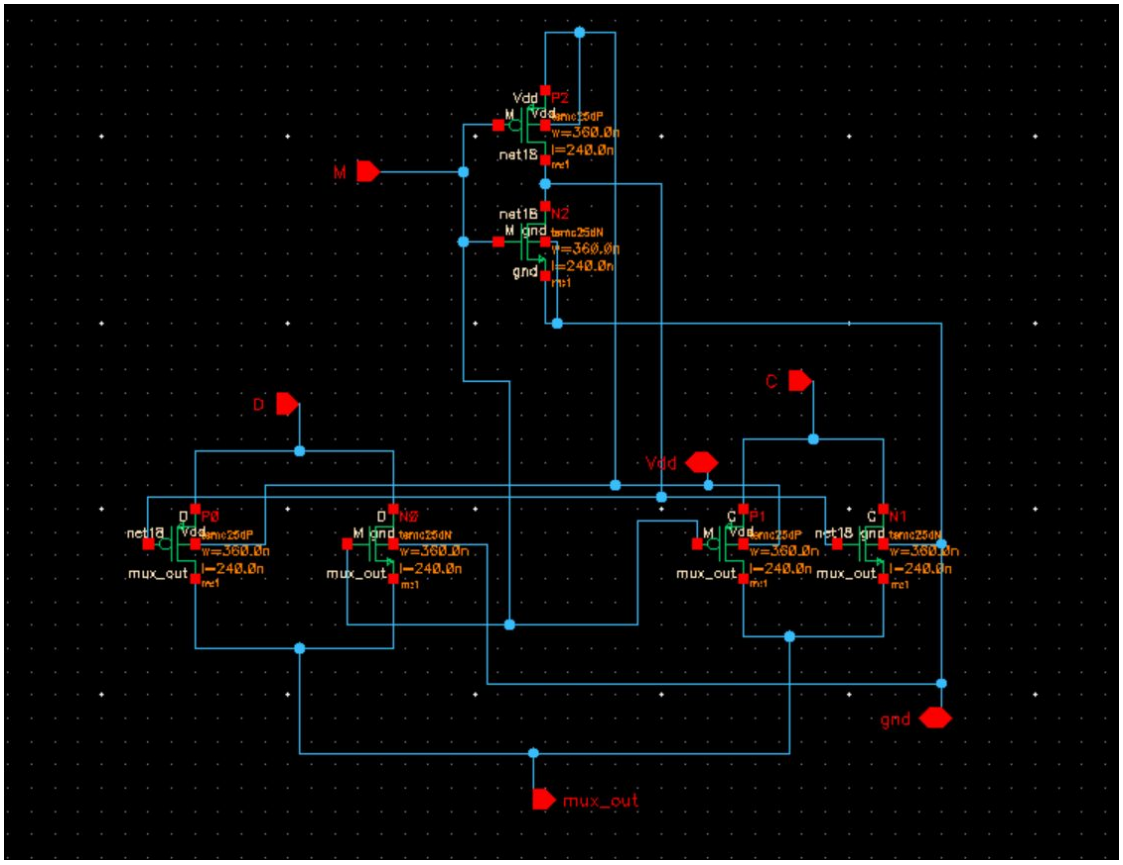



*Figure 6: 2 to 1 Multiplexer schematic*

**Zoomed in section of circuit:**

The following a part of the full adder and subtractor circuit implementation. Each gate and component is compacted into a single cell. This section shows a single adder with the 2s complement solution for subtractions.

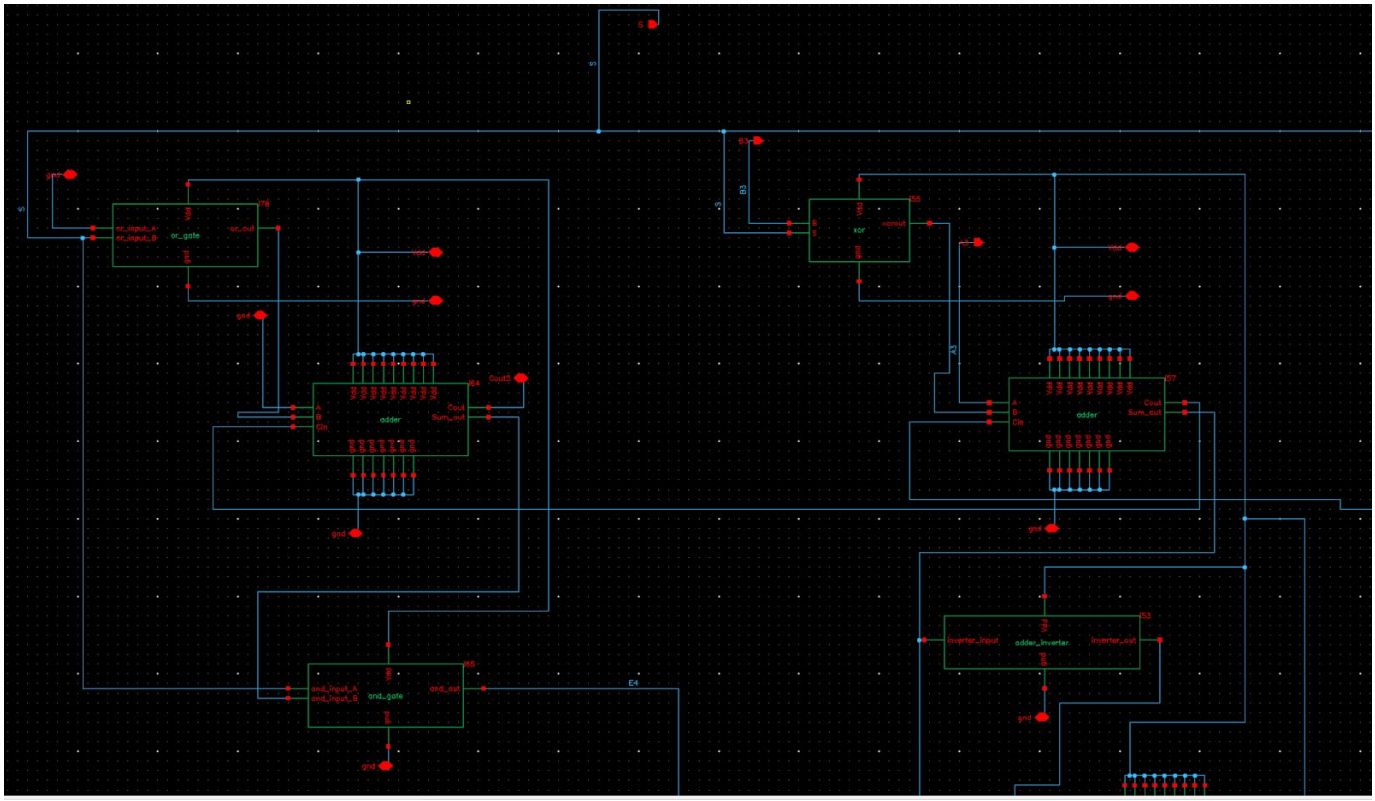


*Figure 7: Zoomed in section of full adder part 1*

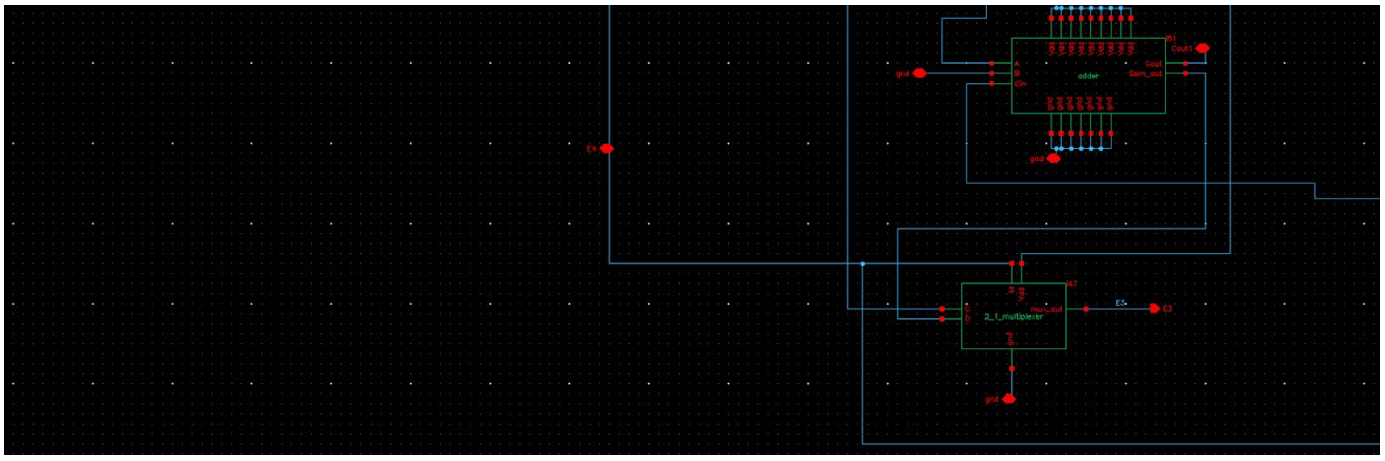


*Figure 8: Zoomed in section of full adder part 2*

**4-Bit Full Adder and Subtractor Circuit Schematic:**

The 4-bit full adder and subtractor circuit implementation using the following gates and components:1 2-input OR gate, 9 adder,1 AND gate,4 2-to-1 Multiplexer, 4 2-input XOR gates, and 4 inverters. Each component is represented as a cell. The adder circuit schematic has 18 terminals: A0, A1, A2, A3, B0, B1, B2, B3, S, Vdd, gnd, E0, E1, E2, E3, E0, Cout1, and Cout2. The design has 382 transistors.

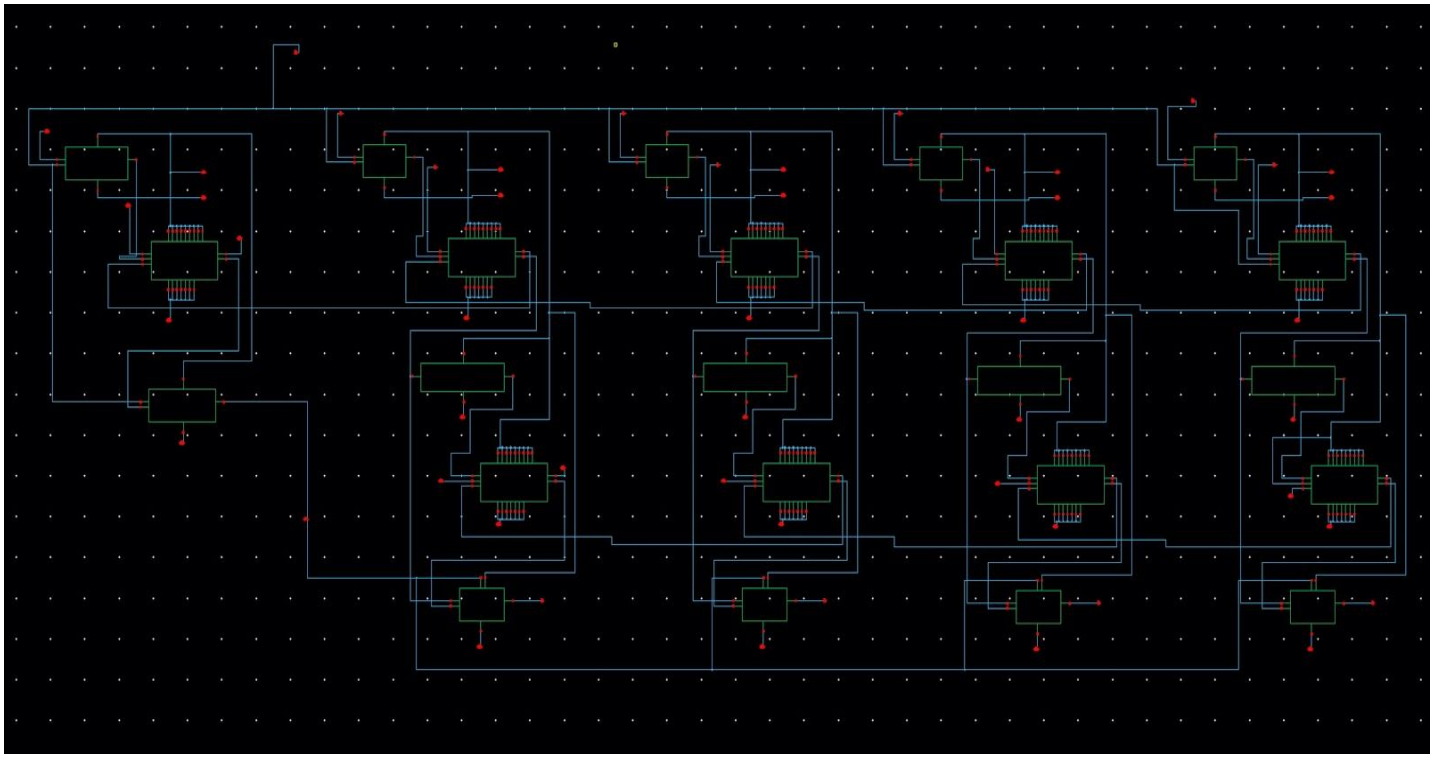


*Figure 9: 4-Bit Full Adder and Subtractor Circuit Schematic*

2. **Layout of the circuit**

   The layout for the circuit using a standard cell approach. The layout incorporates different component's layout such as adder, xor gate, or gate, and gate, inverter, and multiplexer. A single rail connects Vdd and gnd to each component. The layouts do not follow the uninterrupted strip design. The following are two levels for viewing the layout.

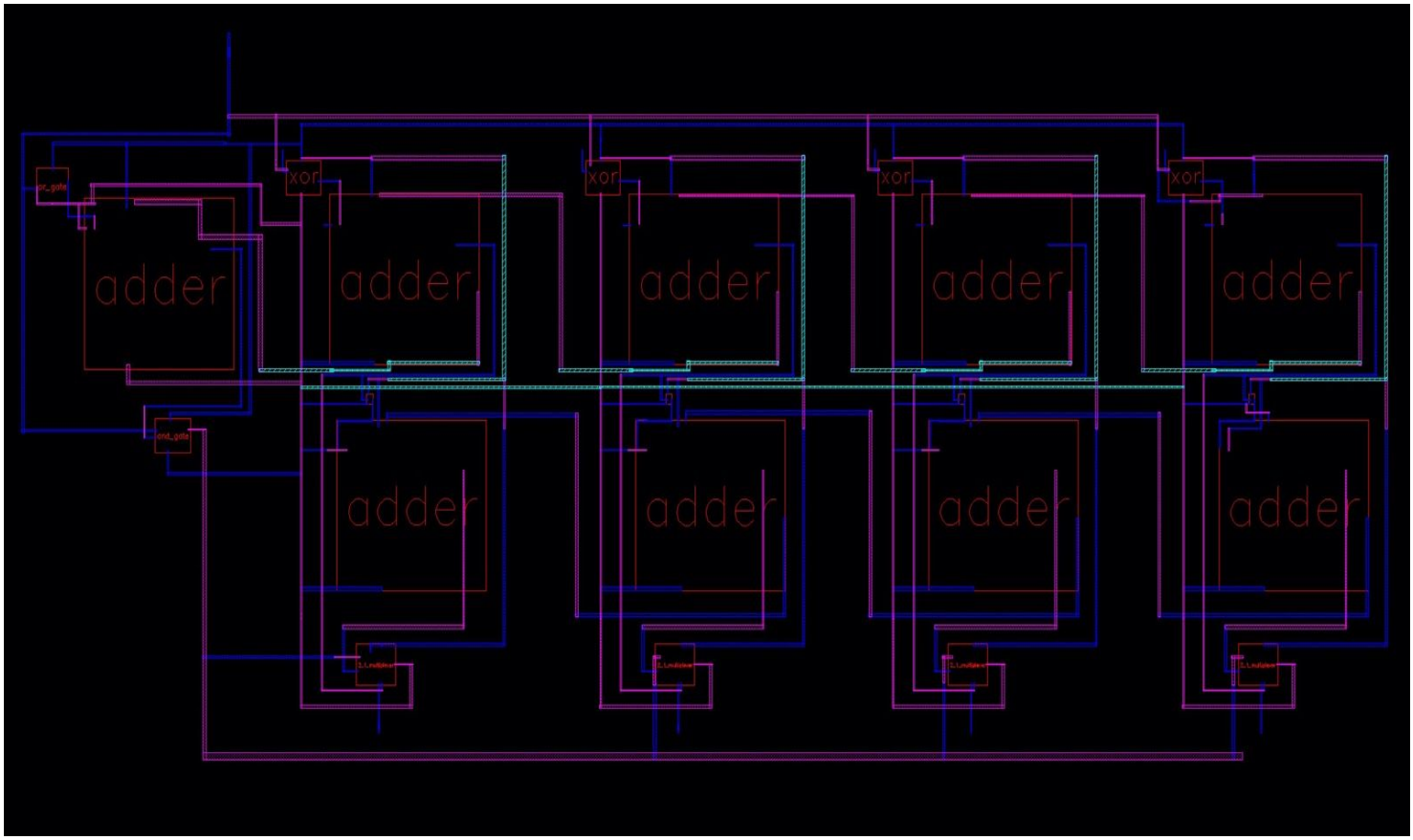



*Figure 10: Layout of 4-Bit Full Adder and Subtractor*

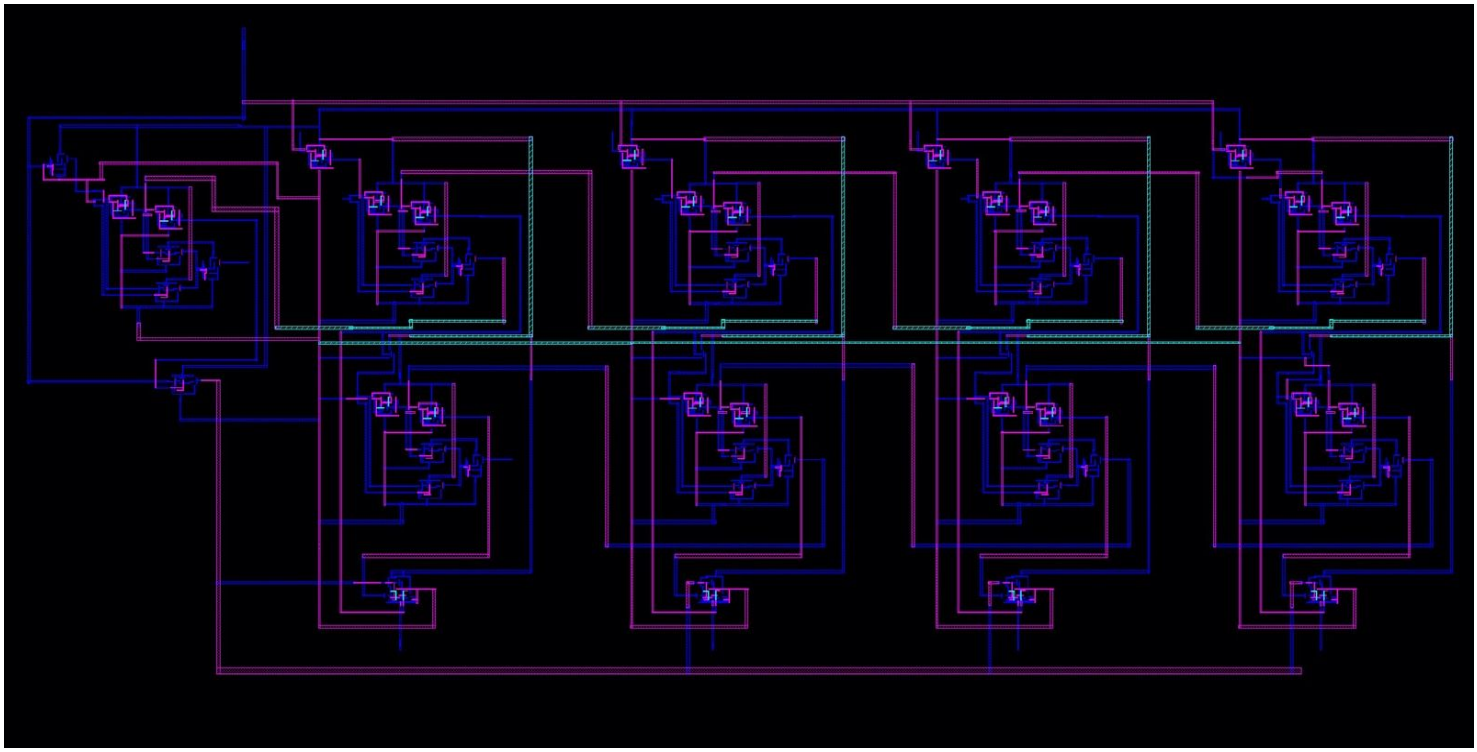


*Figure 11: Layout of 4-Bit Full Adder and Subtractor*

### 3. Use standard cell approach for your layouts

The following are layouts for each cell defined above used to enable Standard Cell Approach.

**2 input XOR gate layout:**

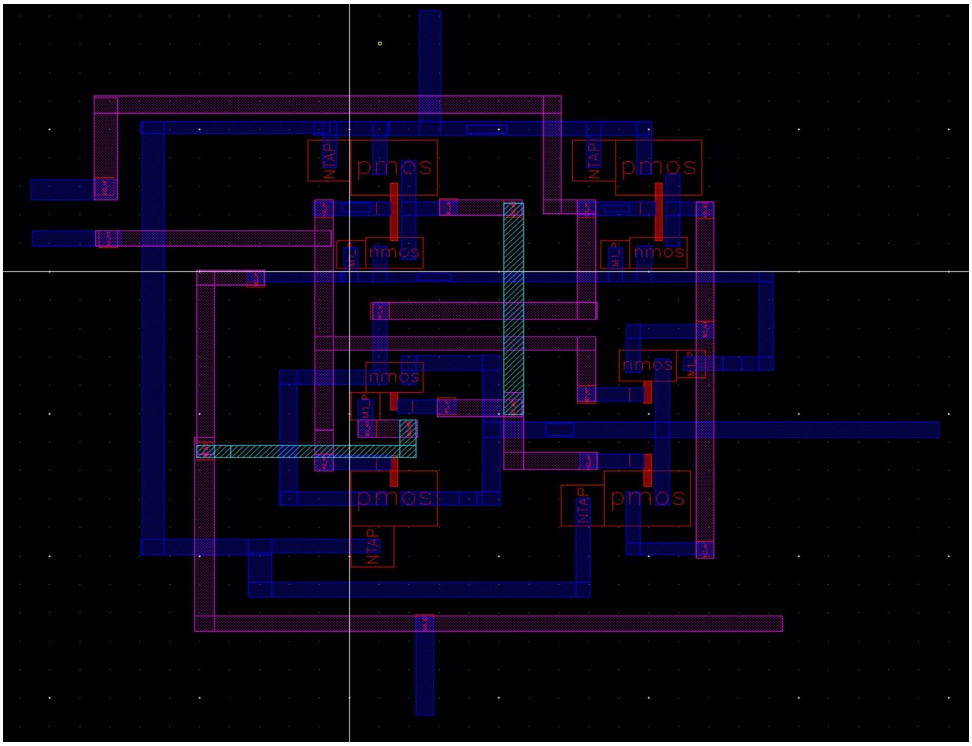



*Figure 12: 2 input XOR gate layout (not uninterrupted strip design)*

**2 input OR gate layout:**


*Figure 13: 2 input OR gate layout (not uninterrupted strip design)*

**2 input AND gate layout:**

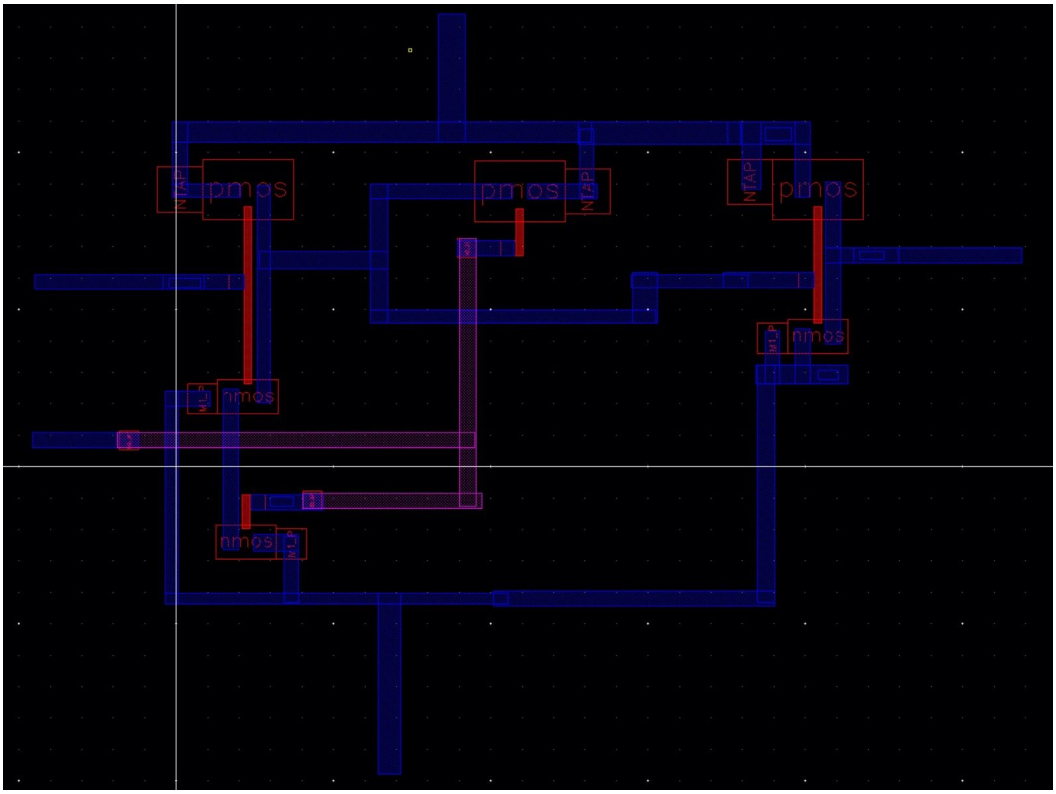



*Figure 14: 2 input AND gate layout (not uninterrupted strip design)*

**Inverter gate layout:**

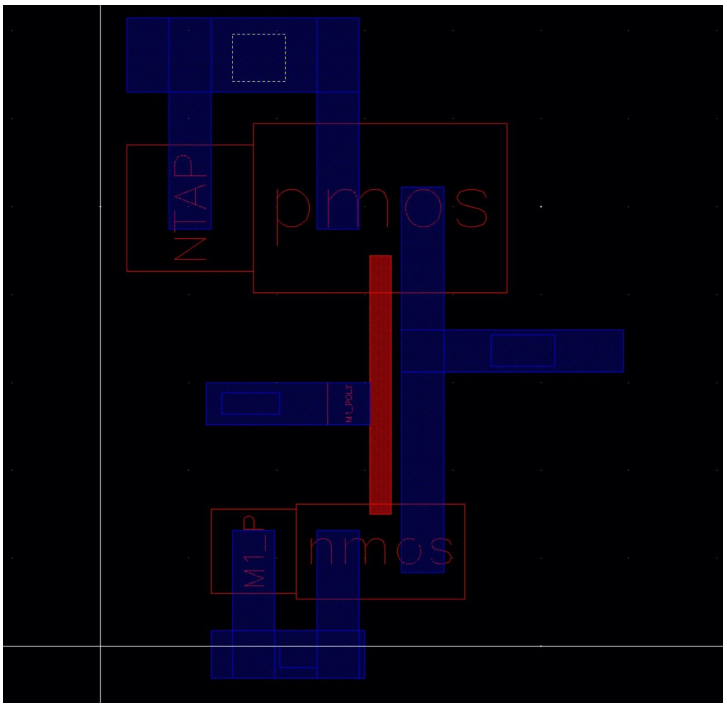



*Figure 15: 2 input Inverter layout*

**2 input Adder layout:**

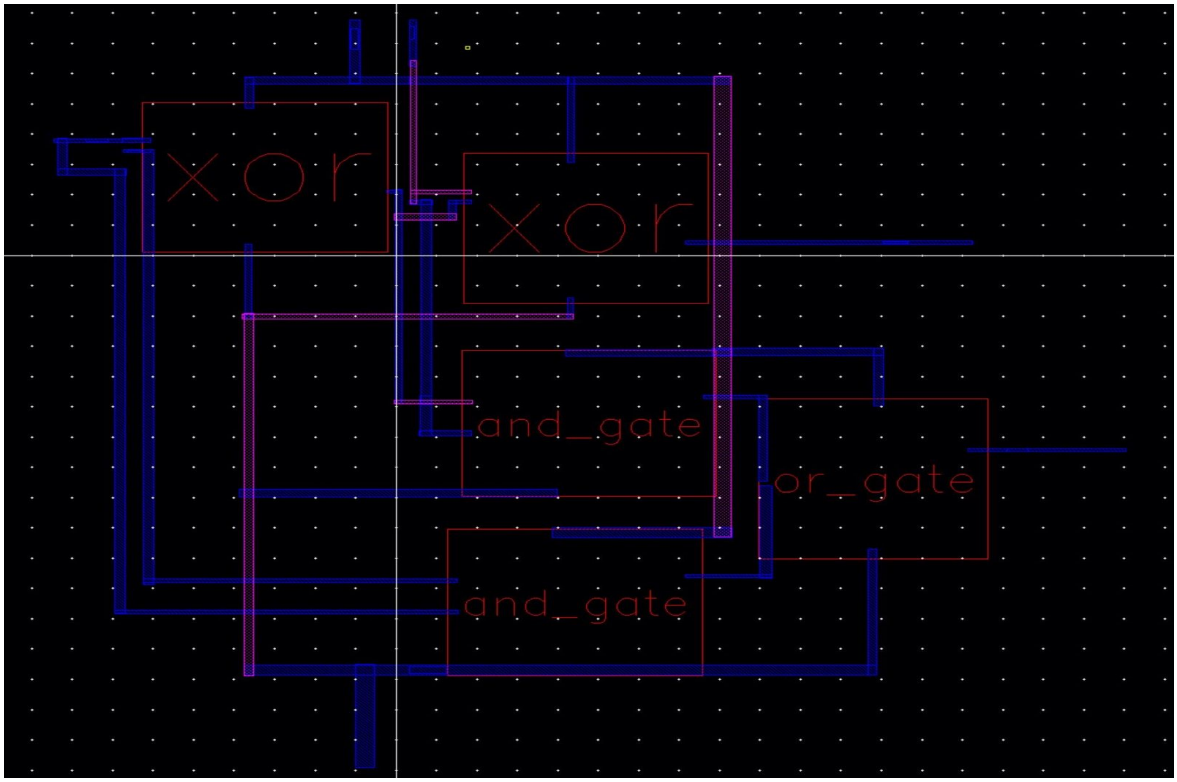



*Figure 16: 2 input Adder Layout (not uninterrupted strip design)*

**2 to 1 MUX layout:**

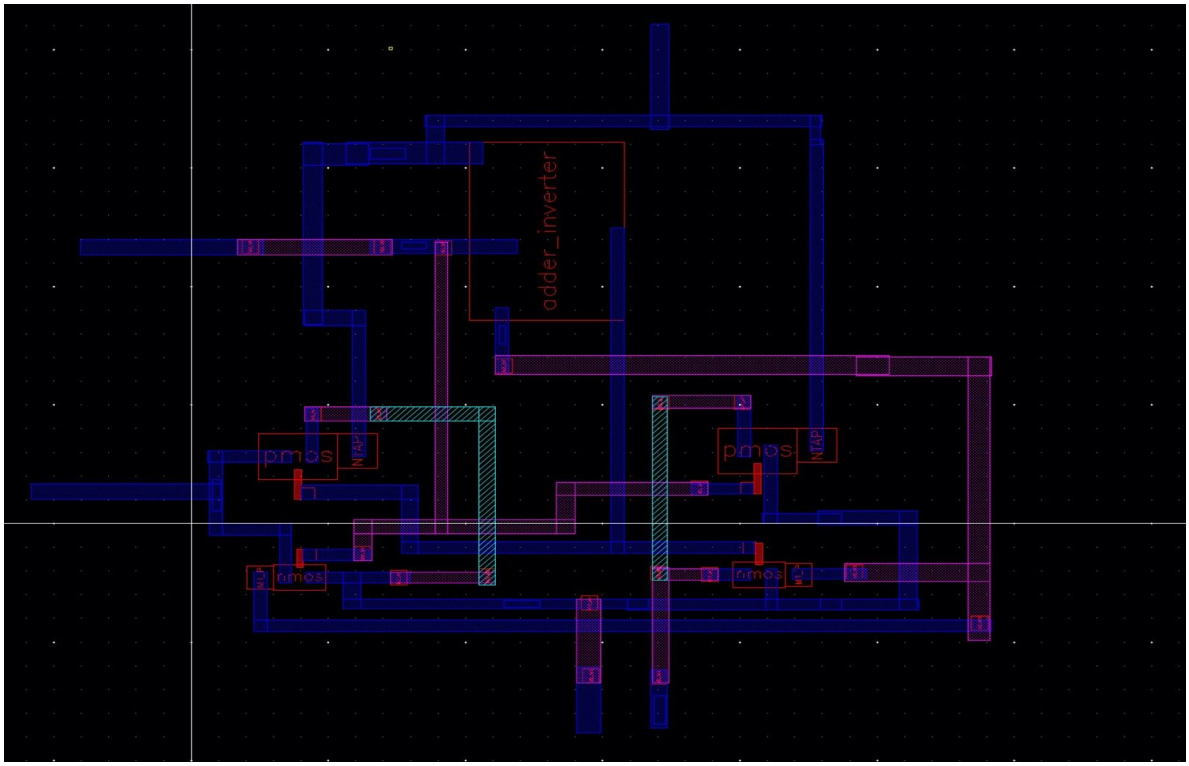
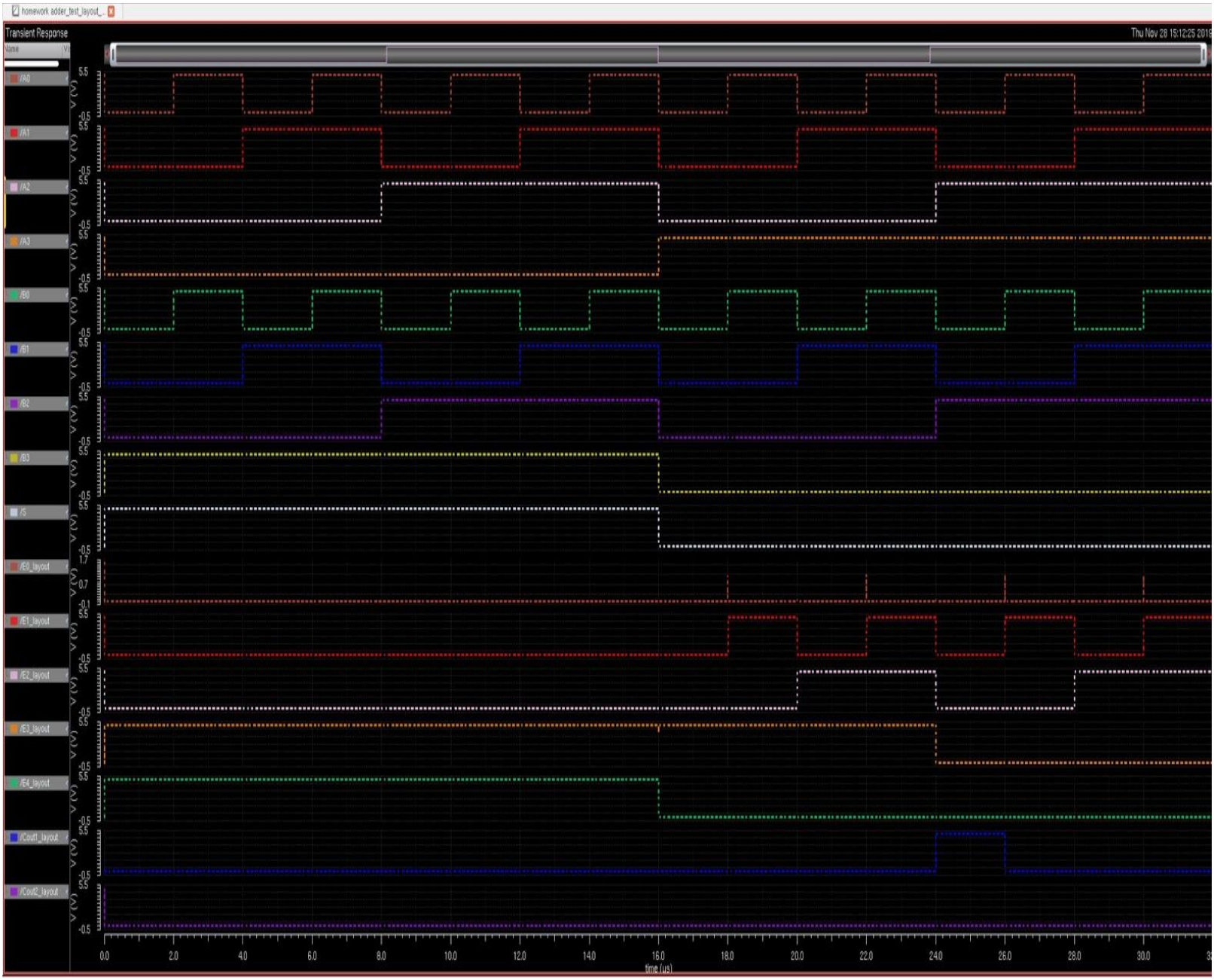



*Figure 17: 2 to 1 Multiplexer layout (not uninterrupted strip design)*

## 4. Simulate the circuit and show that the circuit works

The following is the output for sample inputs. The runtime is 32us. From 0 to 16us, the values for A (A3A2A1A0) ranges from 0 (0000) to 7 (0111) and the value for B (B3, B2, B1, B0) ranges from 8(1000) to 15 (1111). From 16us to 32us, the values of A range from 8 to 15 and the value of B ranges from 0 to 7. From 0 to 16us S is high, therefore, the circuit computes a subtraction and from 16us to 32us S is low, thus, the circuit executes and addition. The last 6 variables, in order, are E0, E1, E2, E3, E4, Cout1, and Cout2. For example, between 14us and 16us the value for A is 7 (0111) and B is 15 (1111). S is high, therefore, The operation A-B is executed. The output for 7-15 is -8. This is represented by E, where E0 = 0, E1 = 0, E2 = 0, E3 = 1, E4 = 1, (1000) where E4 is the sign bit. If E4 is 1 the number is negative and 0 it is positive. (note 1 means high voltage and 0 means low voltage)



**Conclusion:**

The project is a great introduction to the “Standard Cell Approach” which enables VLSI circuit technology. The project was challenging as we encountered errors that required a great understanding of the circuit and layout design to resolve. Overall the encapsulates the necessary skills and fundamental knowledge to design a simple circuit.