CS 303 – LAB#3 Section F

In Lab-3, you are given two .dig files named counter4test.dig and upcounter.dig. The upcounter.dig file contains a 4-bit counter with enable and parallel-load inputs.

Your task for this laboratory assignment is to modify the upcounter.dig file to design a counter that counts from 2 to 11 in decimal and then goes back to 2 again in the next clock cycle.

Note that when the circuit is run, it is normal to see the output as zero before the first clock cycle arrives. So do not worry about that 😊

To accomplish this, you need to modify the "input" component of the upcounter.dig file so that when the circuit is run, the counter starts counting from 2 automatically without the need for any external inputs.

Please note that since you will be modifying the input structure, the counter4test.dig file will not be used for this assignment, but it is provided to help you better understand the mechanism of the circuit. Therefore, you are only asked to submit the modified version of the upcounter.dig file.

Best of luck!

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