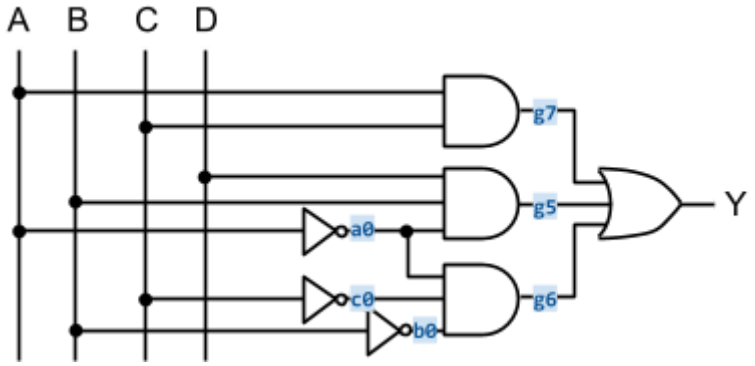
Lab 6: Simulation and Testbenches [Worksheet]

ECE 211: Digital Circuits I — Spring 2025

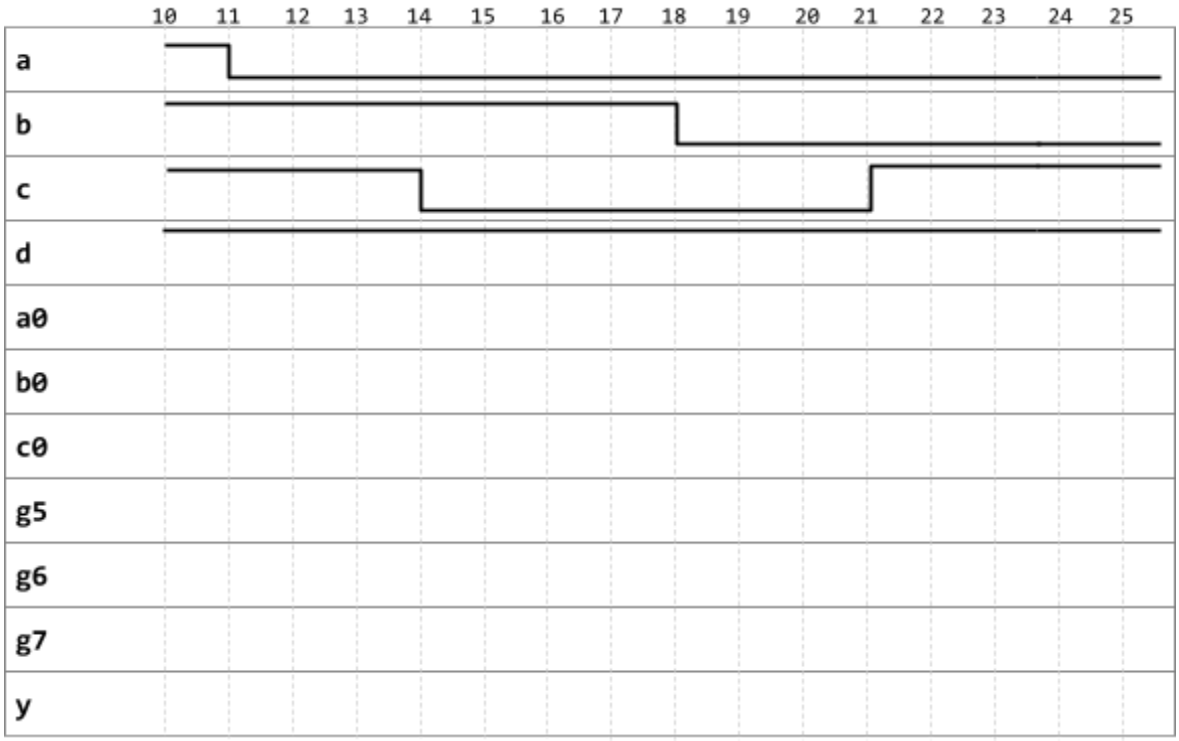
There is no lab report for Lab 6. Instead of submitting a lab report, your lab team will hand in this worksheet, which you will complete alongside each part of the lab assignment. The numbers on this worksheet align with the procedure of the lab manual.

Part 1: Simulating with the Vivado Simulator

The following schematic illustrates the circuit implemented by `circuit_p1.sv`. Intermediate wires are labeled based on the names used in the SystemVerilog module implementation.



Q4. Sketch the expected waveform for this circuit. Assume there is a 1 ns delay for every gate.



Q6. Answer the following question using the Vivado Wave view:

- What are the values of a, b, and y at 12.5 ns?

- At the beginning of the simulation (time = 0), the signal **y** is red on the waveform. What does the red color mean? Why does the signal **y** have this value?

Q8. Customize the waveform from Part 1 using names, colors, and dividers. Show your customized waveform to an instructor and have them initial here:

Q9. ~~The circuit implemented by `circuit_p1.sv` has a glitch in the output y, as shown by your timing diagram. Modify the SystemVerilog implementation to resolve the glitch by adding additional gates to the implementation. Draw a schematic of your glitch-free circuit here.~~

~~*Hint: One suggested way to proceed is to start by writing the Boolean equation and creating a K-Map for the current circuit. By analyzing the K-Map and adding consensus terms, you can resolve the glitches in this circuit.*~~

Q10. Before moving to the next part, remove the delay statements within the file `circuit_p1.sv`. How does your waveform change? How does SystemVerilog model gate delays when delay statements are excluded? Write your thoughts about these questions on the lab worksheet.

Part 2: Creating Testbenches

Q16. Did you find the waveform or the display monitor more helpful at verifying your `adder_4b` circuit? Explain why.

Q16. Demonstrate your adder_4b testbench to an instructor and have them initial here:

Part 3: Using Testbenches to Identify Bugs

Q17. Write a set of useful test cases for an eight-to-three decoder.

Q20. What were the bugs? How did you identify them using the Vivado simulation?

Q21. Demonstrate your working priority encoder circuit to an instructor and have them initial here: