PIC18-Q20 Family Programming Specification

Introduction

This programming specification describes an SPI-based programming method for the PIC18-Q20 family of microcontrollers. The Programming Algorithms section describes the programming commands, programming algorithms and electrical specifications used in that particular programming method. Appendix B contains individual part numbers, device identification values, pinout and packaging information, and Configuration Bytes.

Important:

- This is an SPI-compliant programming method with 8-bit commands.
- The low-voltage entry code is now 32 clocks and MSb first, unlike earlier PIC18 devices, which had 33 clocks and LSb first.

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1. Overview

1.1 Programming Data Flow

Nonvolatile Memory (NVM) programming data can be supplied by either the high-voltage In-Circuit Serial Programming™ (ICSP™) interface or the low-voltage ICSP interface. Data can be programmed into the Program Flash Memory (PFM), Data EEPROM, dedicated User ID locations and the Configuration Bytes.

1.2 Pin Utilization

Five pins are needed for ICSP programming. The pins are listed in the table below. For pin locations and packaging information, refer to the table in Appendix B.

Table 1-1. Pin Descriptions During Programming

Pin Name	During Programming		
	Function	Pin Type	Pin Description
ISCPCLK	ICSPCLK	I	Clock Input – Schmitt Trigger Input
ISCPDAT	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}/V_{PP}$	Program/Verify mode	I(1)	Program Mode Select
V_{DD}	V_{DD}	P	Power Supply
V_{SS}	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note:

1. The programming high voltage is internally generated. To activate the Program/Verify mode, high voltage needs to be applied to the $\overline{MCLR}$ input. Since the $\overline{MCLR}$ is used for a level source, $\overline{MCLR}$ does not draw any significant current.

1.3 Hardware Requirements

1.3.1 High-Voltage ICSP™ Programming

In High-Voltage ICSP mode, the device requires two programmable power supplies: One for V_{DD} and one for the $\overline{MCLR}/V_{PP}$ pin.

1.3.2 Low-Voltage ICSP™ Programming

In Low-Voltage ICSP mode, the device can be programmed using a single V_{DD} source in the device operating range. The $\overline{MCLR}/V_{PP}$ pin does not have to be brought to the programming voltage, but can instead be left at the normal operating voltage.

1.3.2.1 Single-Supply ICSP™ Programming

The device's LVP Configuration bit enables single-supply (low-voltage) ICSP programming. The LVP bit defaults to a '1' (enabled). The LVP bit may only be programmed to '0' by entering the High-Voltage ICSP mode, where the $\overline{MCLR}/V_{PP}$ pin is raised to V_{IHH}. Once the LVP bit is programmed to a '0', only the High-Voltage ICSP mode is available and can be used to program the device.

Important:
- The High-Voltage ICSP mode is always available, regardless of the state of the LVP bit, by applying V_{IHH} to the $\overline{MCLR}/V_{PP}$ pin.
- While in Low-Voltage ICSP mode, $\overline{MCLR}$ is always enabled regardless of the MCLRE bit. Also, the $\overline{MCLR}$ pin can no longer be used as a general purpose input.

1.4 Write and/or Erase Section

Erasing or writing is selected according to the command used to begin operation (see ICSP™ Command Set Summary). The terminologies used in this document, related to erasing/writing to the program memory, are defined in the table below.

Table 1-2. Programming Terms

Term	Definition
Programmed Cell	A memory cell at logic '0'
Erased Cell	A memory cell at logic '1'
Erase	Change memory cell from a '0' to a '1'
Write	Change memory cell from a '1' to a '0'
Program	Generic erase and/or write

1.4.1 Erasing Memory

Memory is erased by 128-word pages or in bulk, where 'bulk' includes many subsets of the total memory space. The duration of the data memory erase is determined by the size of the data memory. All Bulk ICSP Erase commands have minimum V_{DD} requirements, which are higher than the Page Erase and Write requirements.

Page erasing pertains to PFM and User ID memory only. The configuration bytes(1) and data memory will be erased by the Bulk Erase command. For self-write operations, each byte write to data memory includes an automatic erase cycle for the location about to be programmed.

Important:
- The CONFIG14 byte cannot be Bulk Erased and the CONFIG9 byte cannot be Bulk Erased if the $\overline{SAFLOCK}$ bit is set. Refer to the Enhanced Code Protection section for details.

1.4.2 Writing Memory

Memory is written one word at a time. The duration of the write is determined internally.

Note: The size of the word is 16 bits for the Program Flash Memory and 8 bits for the Configuration memory EEPROM, but the same 24-bit payload is used for both memory regions.

2. Memory Map

This section provides details on how the program memory and EEPROM are organized for this device.

Figure 2-1. Program and Data EEPROM Memory Map

<table>
<tr><th rowspan="2">Address</th><th colspan="3">Device</th></tr>
<tr><th>PIC18Fx4Q20</th><th>PIC18Fx5Q20</th><th>PIC18Fx6Q20</th></tr>
<tr><td>00 0000h
to
00 3FFFh</td><td>Program Flash Memory (8KW)(1)</td><td rowspan="2">Program Flash Memory (16 KW)(1)</td><td rowspan="3">Program Flash Memory (32 KW)(1)</td></tr>
<tr><td>00 4000h
to
00 7FFFh</td><td rowspan="4">Not Present(2)</td></tr>
<tr><td>00 8000h
to
00 FFFFh</td><td rowspan="3">Not Present(2)</td></tr>
<tr><td>01 0000h
to
01 FFFFh</td><td rowspan="2">Not Present(2)</td></tr>
<tr><td>02 0000h
to
1F FFFFh</td></tr>
<tr><td>20 0000h
to
20 003Fh</td><td colspan="3">User IDs (32 Words)(3)</td></tr>
<tr><td>20 0040h
to
2B FFFFh</td><td colspan="3">Reserved</td></tr>
<tr><td>2C 0000h
to
2C 00FFh</td><td colspan="3">Device Information Area (DIA)(3,5)</td></tr>
<tr><td>2C 0100h
to
2F FFFFh</td><td colspan="3">Reserved</td></tr>
<tr><td>30 0000h
to
30 0019h</td><td colspan="3">Configuration Bytes(3)</td></tr>
<tr><td>30 001Ah
to
37 FFFFh</td><td colspan="3">Reserved</td></tr>
<tr><td>38 0000h
to
38 00FFh</td><td colspan="3">Data EEPROM (256 Bytes)</td></tr>
<tr><td>38 0100h
to
3B FFFFh</td><td colspan="3">Reserved</td></tr>
<tr><td>3C 0000h
to
3C 0008h</td><td colspan="3">Device Configuration Information(3,4,5)</td></tr>
<tr><td>3C 0009h
to
3F FFFBh</td><td colspan="3">Reserved</td></tr>
<tr><td>3F FFFCh
to
3F FFFDh</td><td colspan="3">Revision ID (1 Word)(3,4,5)</td></tr>
<tr><td>3F FFFEh
to
3F FFFFh</td><td colspan="3">Device ID (1 Word)(3,4,5)</td></tr>
</table>

Note 1: A configurable Storage Area Flash is implemented as part of the User Flash, if enabled.
2: The addresses do not roll over. The region is read as '0'.
3: Not code-protected.
4: Hard-coded in silicon.
5: This region cannot be written by the user and it's not affected by a Bulk Erase.

2.1 User ID Location

The user may store identification information (User ID) in 32 designated locations. The User ID locations are mapped to addresses 20 0000h-20 003Fh. Each location is 16 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

2.2 Device/Revision ID

The 16-bit Device ID Word is located at the address 3F FFFEh and the 16-bit Revision ID is located at the address 3F FFFCh. These locations are read-only and cannot be erased or modified. See the Device ID and Revision ID registers for more details.

2.3 Device Configuration Information (DCI)

The Device Configuration Information (DCI) is a dedicated region in the memory that holds information about the device which is useful for programming and bootloader applications. The data stored in this region are read-only and cannot be modified/erased. Refer to the table below for the complete DCI table addresses and description.

Table 2-1. Device Configuration Information

Address	Name	Description	Value			Units
			PIC18F04/14Q20	PIC18F05/15Q20	PIC18F06/16Q20	
3C 0000h	ERSIZ	Erase page size	128			Words
3C 0002h	WLSIZ	Number of write latches per row	0			Words
3C 0004h	URSIZ	Number of user-erasable pages	128	256	512	Pages
3C 0006h	EESIZ	Data EEPROM memory size	256			Bytes
3C 0008h	PCNT	Pin count	14/20	14/20	14/20	Pins

2.4 Configuration Bytes

The devices have 13 Configuration Bytes, starting at address 30 0000h. The Configuration bits enable or disable specific features, placing these controls outside the normal software process. They also establish configured values prior to the execution of any software.

⚠ CAUTION The address location for the Configuration bytes on these devices does not increment sequentially. Refer to the Register Summary for address locations.

In terms of programming, consider the following Configuration bits:

1. **$\overline{\text{SAFLOCK}}$: Storage Area Flash (SAF) Lock Enable bit** (1)
   - 1 = OFF: SAF Lock disabled
   - 0 = ON: SAF Lock enabled, SAF areas are locked and the SAFSZ bits cannot be erased.
2. **LVP: Low-Voltage Programming Enable bit**
   - 1 = ON: Low-Voltage Programming is enabled. $\overline{\text{MCLR}}/V_{PP}$ pin function is $\overline{\text{MCLR}}$. The MCLRE Configuration bit is ignored.
   - 0 = OFF: High voltage on $\overline{\text{MCLR}}/V_{PP}$ must be used for programming.

   It is important to note that the LVP bit cannot be written (to '0') while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state. For more information, refer to the Low-Voltage Programming (LVP) Mode section.
3. **MCLRE: Master Clear ($\overline{\text{MCLR}}$) Enable bit**
   - If LVP = 1: RA3 pin function is $\overline{\text{MCLR}}$

  - If LVP = 0
    - 1 = RA3 pin is $\overline{\text{MCLR}}$
    - 0 = RA3 pin function is a port-defined function
4. **$\overline{\text{CP}}$: User NVM Program Memory Code Protection bit**
   - 1 = OFF: User NVM code protection is disabled
   - 0 = ON: User NVM code protection is enabled
5. **$\overline{\text{CPD}}$: Data EEPROM Code Protection bit**
   - 1 = OFF: Data EEPROM code protection is disabled
   - 0 = ON: Data EEPROM code protection is enabled

⚠ CAUTION

1. Once enabled, the $\overline{\text{SAFLOCK}}$ bit CANNOT be disabled. Bulk Erase and self-erase operations are not possible.

2.5 Device ID

Name: DEVICEID
Offset: 3F FFFEh

Device ID Register

Bit	15	14	13	12	11	10	9	8
	DEV[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	DEV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bits 15:0 – DEV[15:0] Device ID

Device	Device ID
PIC18F04Q20	7AE0h
PIC18F05Q20	7AA0h
PIC18F06Q20	7A60h
PIC18F14Q20	7AC0h
PIC18F15Q20	7A80h
PIC18F16Q20	7A40h

2.6 Revision ID

Name: REVISIONID
Offset: 3F FFFCh

Revision ID Register

Bit	15	14	13	12	11	10	9	8
	1010[3:0]				MJRREV[5:2]			
Access	R	R	R	R	R	R	R	R
Reset	1	0	1	0	q	q	q	q

Bit	7	6	5	4	3	2	1	0
	MJRREV[1:0]		MNRREV[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	q	q	q	q	q	q	q	q

Bits 15:12 – 1010[3:0] Read as `'b1010`
These bits are fixed with value `'b1010` for all devices in this family.

Bits 11:6 – MJRREV[5:0] Major Revision ID
These bits are used to identify a major revision (A0, B0, C0, etc.).
Revision A = `'b00 0000`
Revision B = `'b00 0001`

Bits 5:0 – MNRREV[5:0] Minor Revision ID
These bits are used to identify a minor revision.
Revision A0 = `'b00 0000`
Revision B0 = `'b00 0000`
Revision B1 = `'b00 0001`

Tip: For example, the REVISIONID register value for revision B1 will be `0xA041`.

3. Programming Algorithms

3.1 Program/Verify Mode

In Program/Verify mode, the program memory and the Configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted MSb first. Data changes on the rising edge of the ICSPCLK and is latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK pins are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state; all I/Os are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

3.1.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different modes of entering Program/Verify mode via high voltage:

- V_{PP}-First Entry mode
- V_{DD}-First Entry mode

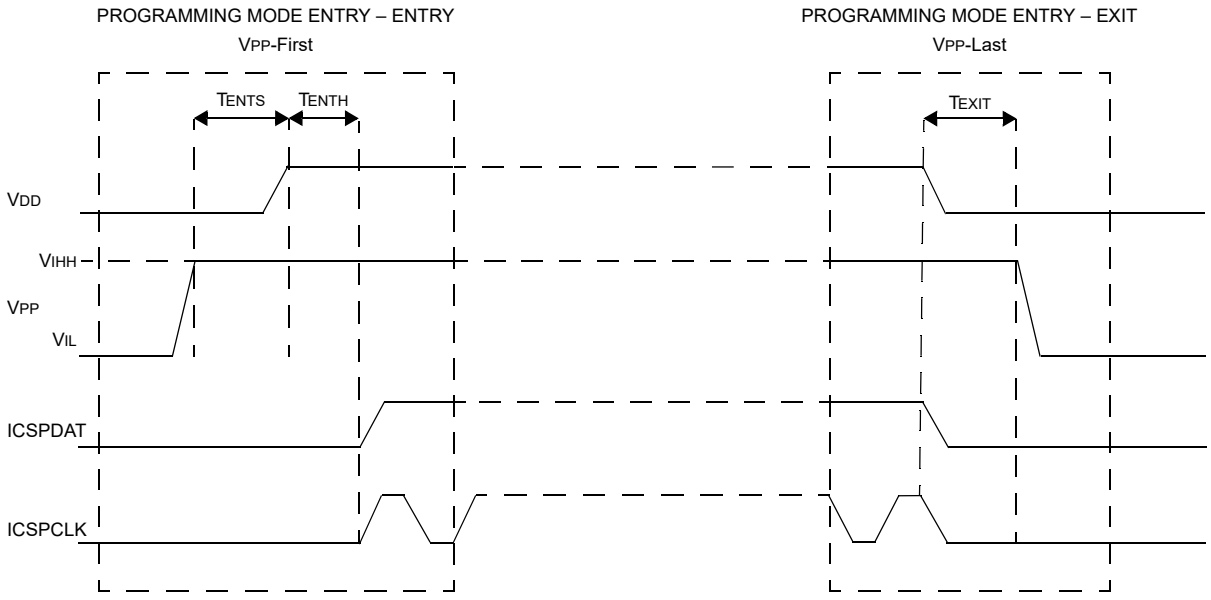
3.1.1.1 V_{PP}-First Entry Mode

To enter Program/Verify mode via the V_{PP}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on $\overline{MCLR}$ from 0V to V_{IHH}.
3. Raise the voltage on V_{DD} from 0V to the desired operating voltage.

The V_{PP}-First Entry mode prevents the device from executing code prior to entering the Program/Verify mode. For example, when the Configuration Byte has already been programmed to have $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer disabled ($\overline{PWRTE}$ = 0) and the internal oscillator selected, the device will execute the code immediately. V_{PP}-First Entry mode is strongly recommended as it prevents the user code from executing. See the timing diagram in Figure 3-1.

Figure 3-1. Programming Entry and Exit Modes – V_{PP}-First and Last



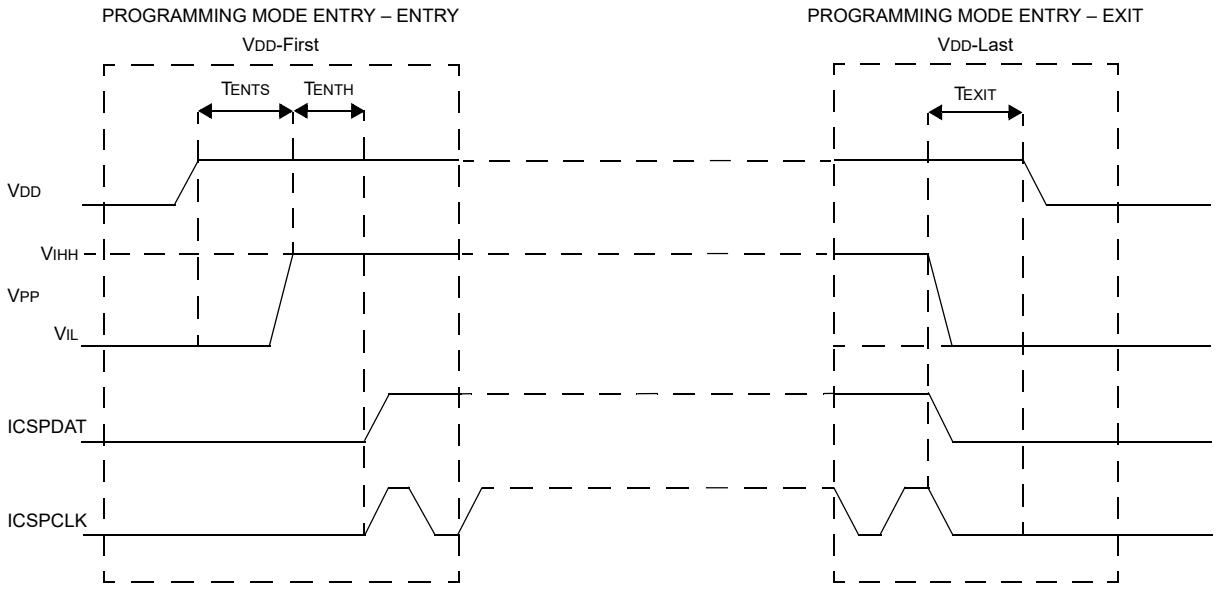
3.1.1.2 V_{DD}-First Entry Mode

To enter the Program/Verify mode via the V_{DD}-First Entry mode, the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on V_{DD} from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from V_{DD} or below to V_{IHH}.

The V_{DD}-First Entry mode is useful for programming the device when the V_{DD} is already applied. It is not necessary to disconnect V_{DD} to enter the Program/Verify mode. See the timing diagram in Figure 3-2.

Figure 3-2. Programming Entry and Exit Modes – V_{DD}-First and Last



3.1.1.3 Program/Verify Mode Exit

To exit the Program/Verify mode, lower $\overline{MCLR}$ from V_{IHH} to V_{IL}. The V_{PP}-First Entry mode will use the V_{PP}-Last Exit mode (see Figure 3-1). The V_{DD}-First Entry mode will use the V_{DD}-Last Exit mode (see Figure 3-2).

3.1.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the devices to be programmed using V_{DD} only, without high voltage. When the LVP bit in the Configuration Byte register is set to '1', the Low-Voltage ICSP Programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A 32-bit key sequence is presented on ICSPDAT, clocked by ICSPCLK. The Least Significant bit (LSb) of the pattern is a 'don't care X'. The Program/Verify mode entry pattern detect hardware verifies only the first 31 bits of the sequence and the last clock is required before the pattern detect goes Active.

The key sequence is a specific 32-bit pattern, '32'h4d434850' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit (MSb) of the Most Significant Byte must be shifted in first. Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode needs to be maintained. For Low-Voltage Programming timing, see Figure 3-3 and Figure 3-4.

Figure 3-3. LVP Entry (Powered)

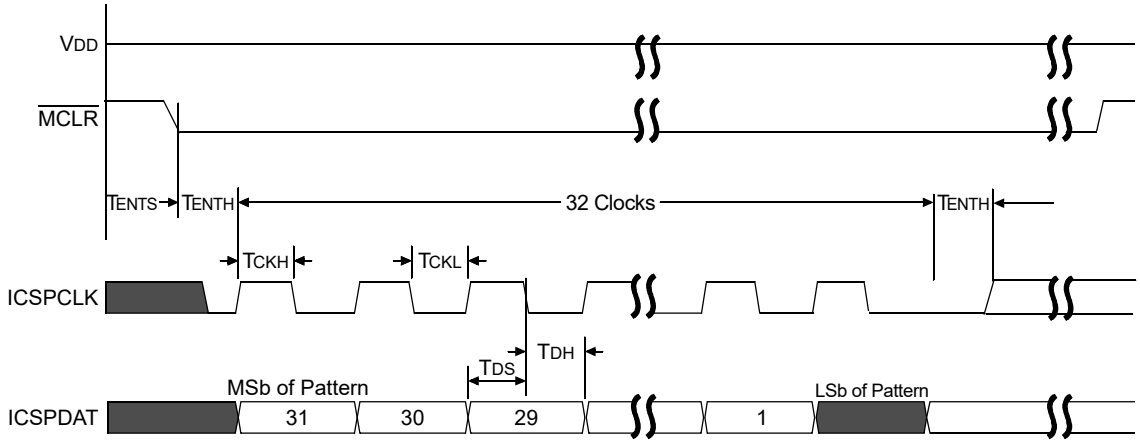
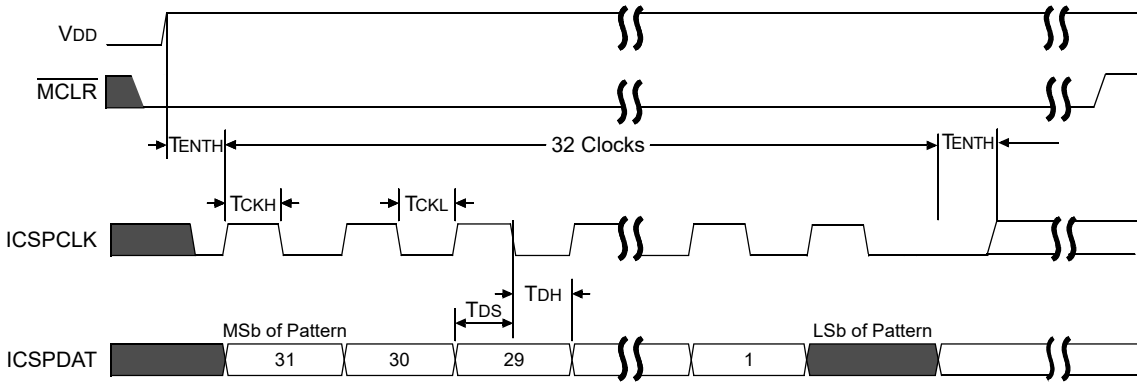


Figure 3-4. LVP Entry (Powering Up)



Exiting the Program/Verify mode is done by raising $\overline{MCLR}$ from below V_{IL} to V_{IH} level (or higher, up to V_{DD}).

Important:
To enter LVP mode, the MSb of the Most Significant nibble must be shifted in first. This differs from entering the key sequence on some other device families.

3.1.3 Program/Verify Commands

Once a device has entered the ICSP Program/Verify mode (using either high-voltage or LVP entry), the programming host device may issue seven commands to the microcontroller, each eight bits in length. The commands are summarized in Table 3-1 and are used to erase or program the device based on the location of the Program Counter (PC).

Some 8-bit commands also have an associated data payload (such as Load PC Address and Read Data from NVM).

If the host device issues an 8-bit command byte that has an associated data payload, the host device is responsible for sending additional 24 clock pulses (e.g., three 8-bit bytes) to send or receive the payload data associated with the command.

The payload field size is compatible with many 8-bit SPI-based systems. Within each 24-bit payload field, the first bit transmitted is always a Start bit, followed by a variable number of Pad bits, then by the useful data payload bits and ending with one Stop bit. The useful data payload bits are always transmitted MSb first.

When the programming device issues a command that involves a host to the microcontroller payload (e.g., Load PC Address), the Start, Stop and Pad bits will all be driven by the programmer to '0'. When the programming host device

issues a command that involves the microcontroller to host payload data (e.g., Read Data from NVM), the Start, Stop and Pad bits will be treated as 'don't care' bits and the values will be ignored by the host.

When the programming host device issues an 8-bit command byte to the microcontroller, the host will wait a specified minimum amount of delay (which is command-specific) prior to sending any additional clock pulses (associated with either a 24-bit data payload field or the next command byte).

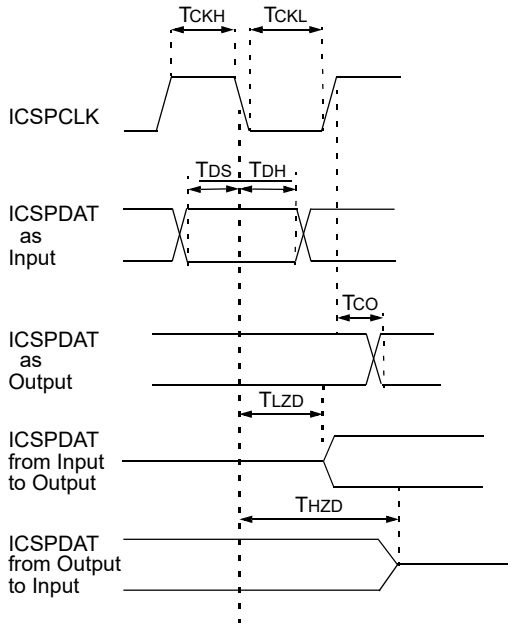
Table 3-1. ICSP™ Command Set Summary(1)

Command Name	Command Value		Payload Expected	Delay after Command	Data/Note
	Binary (MSb ... LSb)	Hex			
Load PC Address	1000 0000	80	Yes	T_{DLY}	Payload value = PC
Bulk Erase	0001 1000	18	Yes	T_{ERAB}	The payload carries the information of the regions that need to be bulk erased
Page Erase Program Memory	1111 0000	F0	No	T_{ERAS}	The page addressed by the MSbs of the PC is erased; LSbs are ignored
Read Data from NVM	1111 11J0	FC/FE	Yes	T_{DLY}	Data output '0' if code-protect is enabled: J = 0: PC is unchanged; J = 1: PC = PC + n(2) after reading
Increment Address	1111 1000	F8	No	T_{DLY}	PC = PC + n(2)
Program Data	11J0 0000	C0/E0	Yes	T_{PROG}	Payload value = Data Word; J = 0: PC is unchanged; J = 1: PC = PC + n after writing
Program Access Enable	0100 1100	4C	Yes	T_{DLY}	Payload value = 22'h27A1A5

Important:

1. All the clock pulses for both the 8-bit commands and the 24-bit payload fields are generated by the host programming device. The microcontroller does not drive the ICSPCLK line. The ICSPDAT signal is a bidirectional data line. For all commands and payload fields, except the Read Data from NVM payload, the host programming device continuously drives the ICSPDAT line. Both the host programmer device and the microcontroller will latch received ICSPDAT values on the falling edge of the ICSPCLK line. When the microcontroller receives ICSPDAT line values from the host programmer, the ICSPDAT values must be valid a minimum of T_{DS} before the falling edges of ICSPCLK and will remain valid for a minimum of T_{DH} after the falling edge of ICSPDAT. See Figure 3-5.
2. PC is incremented by n = 1 for data memory and Configuration bytes, and n = 2 for all other regions.

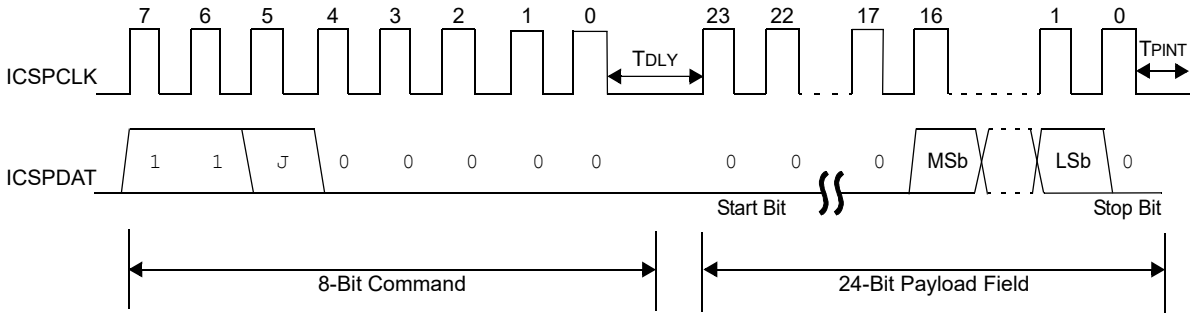
Figure 3-5. Clock and Data Timing



3.1.3.1 Program Data

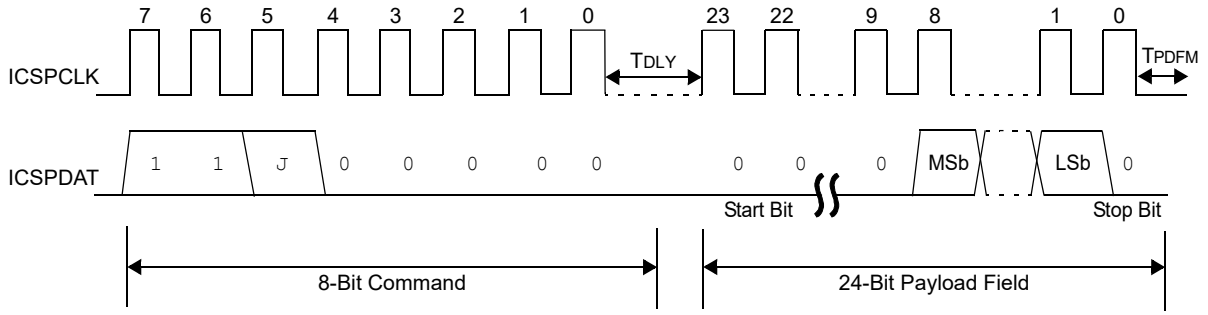
The Program Data command is used to program one NVM word (e.g., one 16-bit instruction word for program memory/User ID memory or one 8-bit data for a Data EEPROM Memory address). The payload data are written into program or EEPROM memory immediately after the Programming Data command is issued (see Programming Algorithms). Depending on the value of bit 5 of the command, the PC may or may not be incremented (see ICSP ™ Command Set Summary). This command will not work on memory areas that are code protected or write protected.

Figure 3-6. Program Data (Program Memory and User IDs)



Important:
The Program Access Enable command and corresponding payload must be sent immediately before writing to the $\overline{\text{SAFLOCK}}$ bit in the CONFIG14 register.

Figure 3-7. Program Data (DATA EEPROM and Configuration Bytes)



3.1.3.2 Read Data from NVM

The Read Data from the NVM command will transmit data bits out of the current PC address. The ICSPDAT pin will go into Output mode on the first falling edge of the ICSP data payload clock and it will revert to Input mode (high-impedance) after the 24th falling edge of the ICSP data payload clock. The Start and Stop bits are only one-half of a bit time wide. Therefore, they must be ignored by the host programmer device since the latched value may be indeterminate. Additionally, the host programmer device needs to only consider the MSb to LSb payload bits as valid and can ignore the values of the Pad bits. If the memory region is code-protected , the data will be read as zeros (see Figure 3-8 and Figure 3-9). Refer to Enhanced Code Protection section for details. Depending on the value of bit 1 of the command, the PC may or may not be incremented (see ICSP™ Command Set Summary). The Read Data from the NVM command can be used to read data for the Program Flash Memory (see Figure 3-8) or the Data EEPROM Memory (see Figure 3-9).

Figure 3-8. Read Data from NVM (PFM and User IDs)

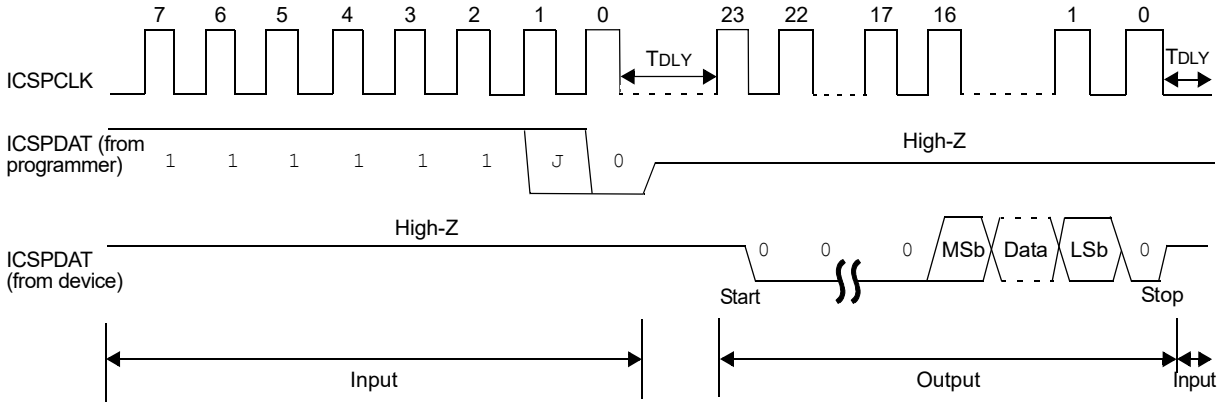
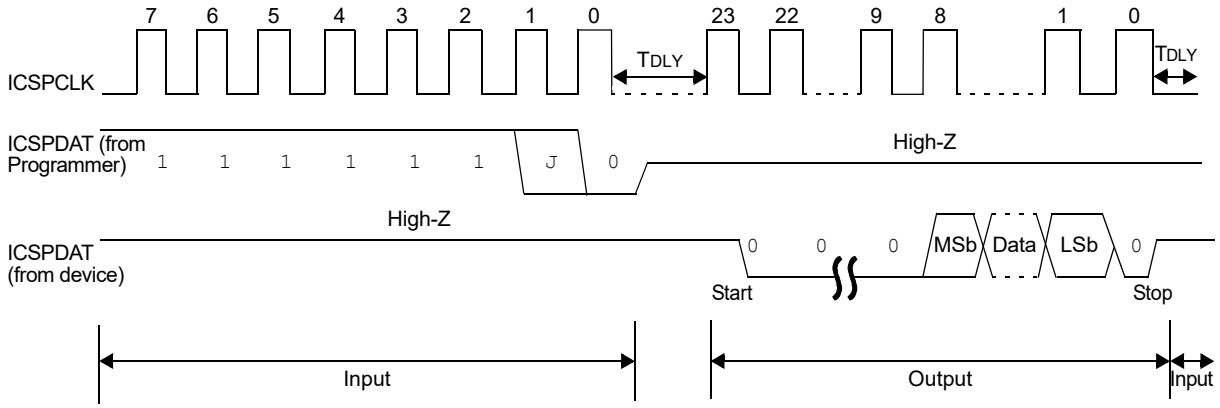


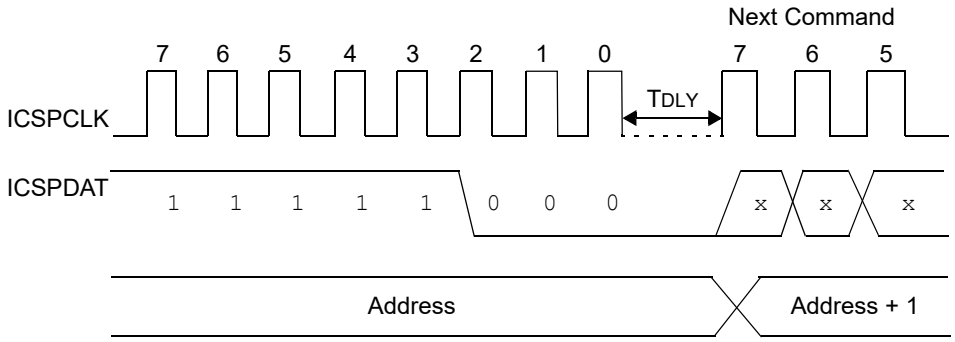
Figure 3-9. Read Data from NVM (DATA EEPROM and Configuration Bytes)



3.1.3.3 Increment Address

The address is incremented when this command is received. Depending on the current value of the Program Counter, the increment varies. If the PC points to PFM, then the PC is incremented by 2. If the PC points to the Data EEPROM or Configuration Space, then it is incremented by 1. It is not possible to decrement the address. To reset the Program Counter, the user must use the Load PC Address command.

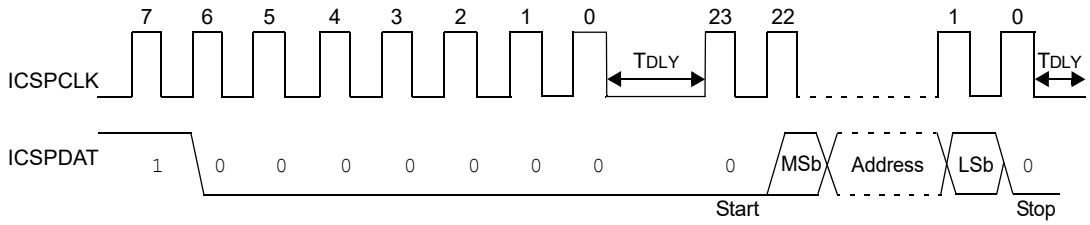
Figure 3-10. Increment Address



3.1.3.4 Load PC Address

The PC value is set using the supplied data. The address indicates the memory location (PFM or Data EEPROM Memory or Configuration memory) to be accessed (see Figure 3-11).

Figure 3-11. Load PC Address



3.1.3.5 Bulk Erase

The Bulk Erase command is used to completely erase different memory regions. The area selection is a bit field in the payload.

By setting the following bits of the payload, the corresponding memory regions can be bulk erased. Setting multiple bits is valid.

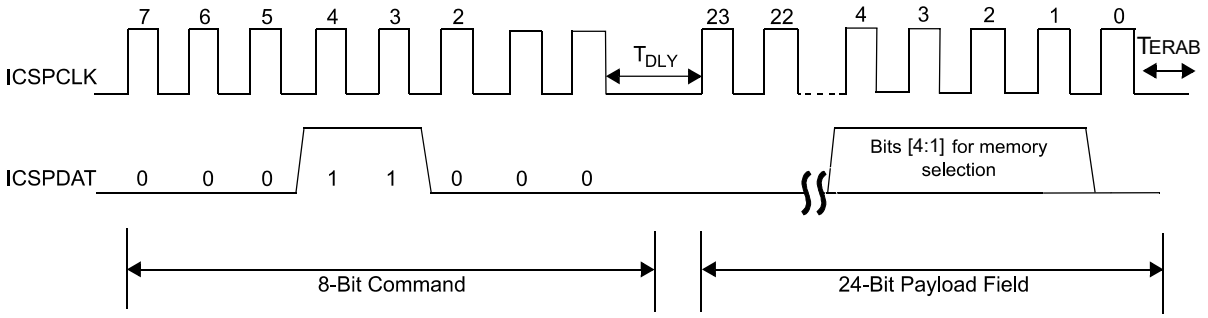
1. Bit 0: Data EEPROM
2. Bit 1: Flash memory
3. Bit 2: User ID memory
4. Bit 3: Configuration memory

Important:

1. If the device is code-protected and a Bulk Erase command for the Configuration memory is issued, all other regions are also bulk erased.
2. Once set, the SAFLOCK bit cannot be bulk erased and the SAF space defined by the SAFSZ bits cannot be bulk erased.

After receiving the Bulk Erase command, the erase will complete after the time interval, T_{ERAB}. See Figure 3-12 for the Bulk Erase command structure.

Figure 3-12. Bulk Erase Memory

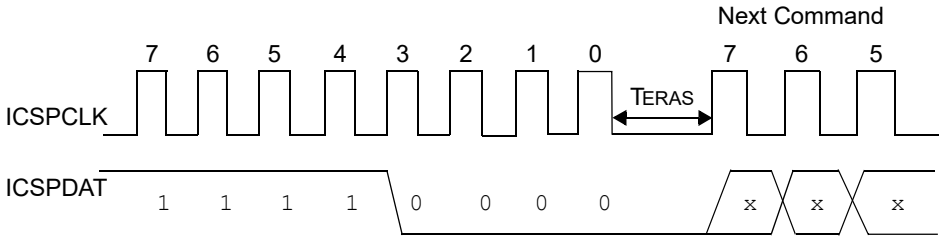


3.1.3.6 Page Erase Program Memory

The Page Erase Program Memory command will erase an individual page based on the current address of the Program Counter. If the program memory is code-protected, the Page Erase Memory command will be ignored. The Bulk Erase command must be used to erase code-protected memory.

The Flash memory page defined by the current PC will be erased. The user must wait T_{ERAS} for erasing to be complete (see Figure 3-13). Page Erase may be used for the program memory and User ID regions only. The configuration and data regions must be erased with the Bulk Erase method.

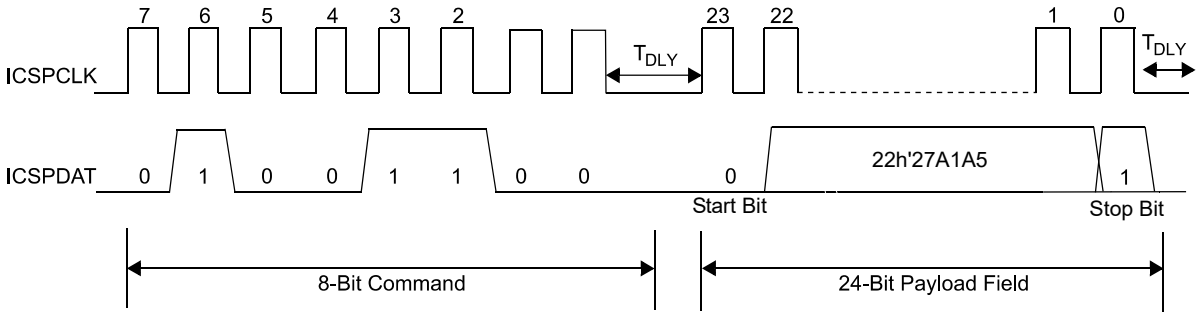
Figure 3-13. Page Erase Memory



3.1.3.7 Program Access Enable

The Program Access Enable command is used to program the $\overline{\text{SAFLOCK}}$ bit. By default, write-access to the $\overline{\text{SAFLOCK}}$ bit is blocked for safety to prevent inadvertent changes to device configuration. Refer to Enhanced Code Protection for details. Using the Program Data command to write to these CONFIG bits will not work without sending the Program Access Enable command first. Sending the Program Access Enable (`0x4C`) command with the `22'h27A1A5` payload (the total 32-bit value is `32'h4C4F434B`, more easily remembered as LOCK in ASCII) will grant write-access to these Configuration bits for a limited-time command window duration. The write-access is terminated once the command window has passed, regardless of the command that is executed during that window. On PIC18 devices, the write-access window is for a duration of one command, so the Program Access Enable command must be issued immediately before every write to the $\overline{\text{SAFLOCK}}$ bit.

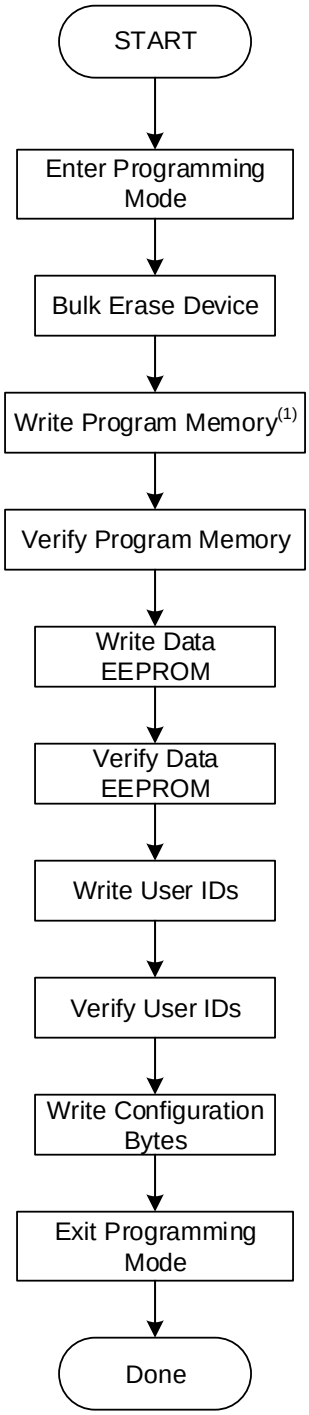
Figure 3-14. Program Access Enable Timing Diagram



3.2 Programming Algorithms

The Program Flash Memory and User ID are programmed one word at a time. The EEPROM memory and configuration regions are programmed one byte at a time.

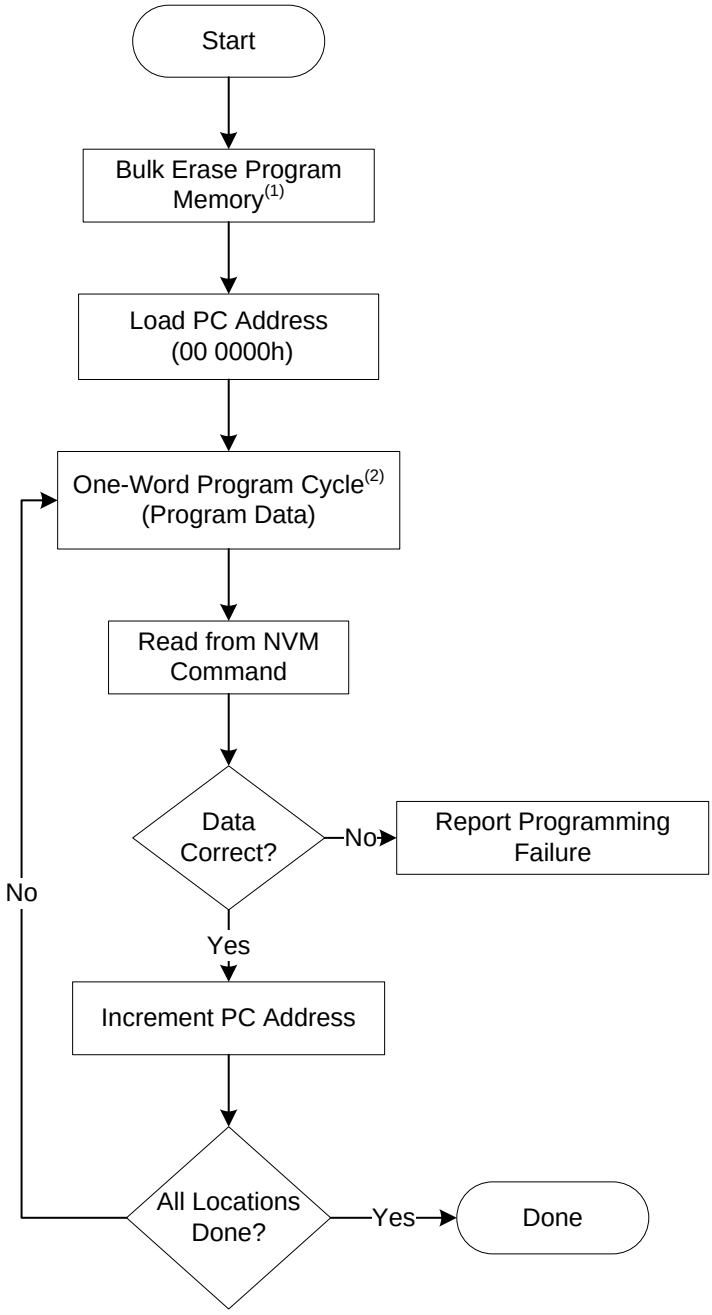
Figure 3-15. Device Program/Verify Flowchart



Notes:

1. See Figure 3-16.
2. See Figure 3-18.

Figure 3-16. Program Memory Flowchart



Notes:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. If the device is code-protected or must be completely erased, then Bulk Erase the device, as shown in Figure 3-19.

Figure 3-17. One-Word Program Cycle

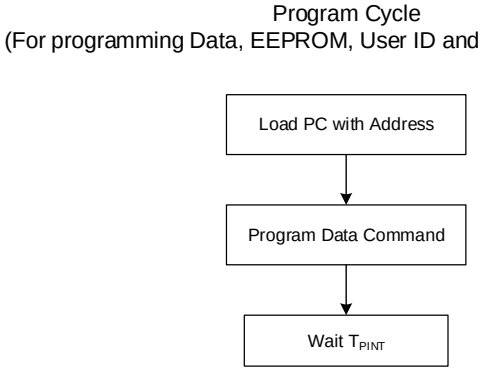
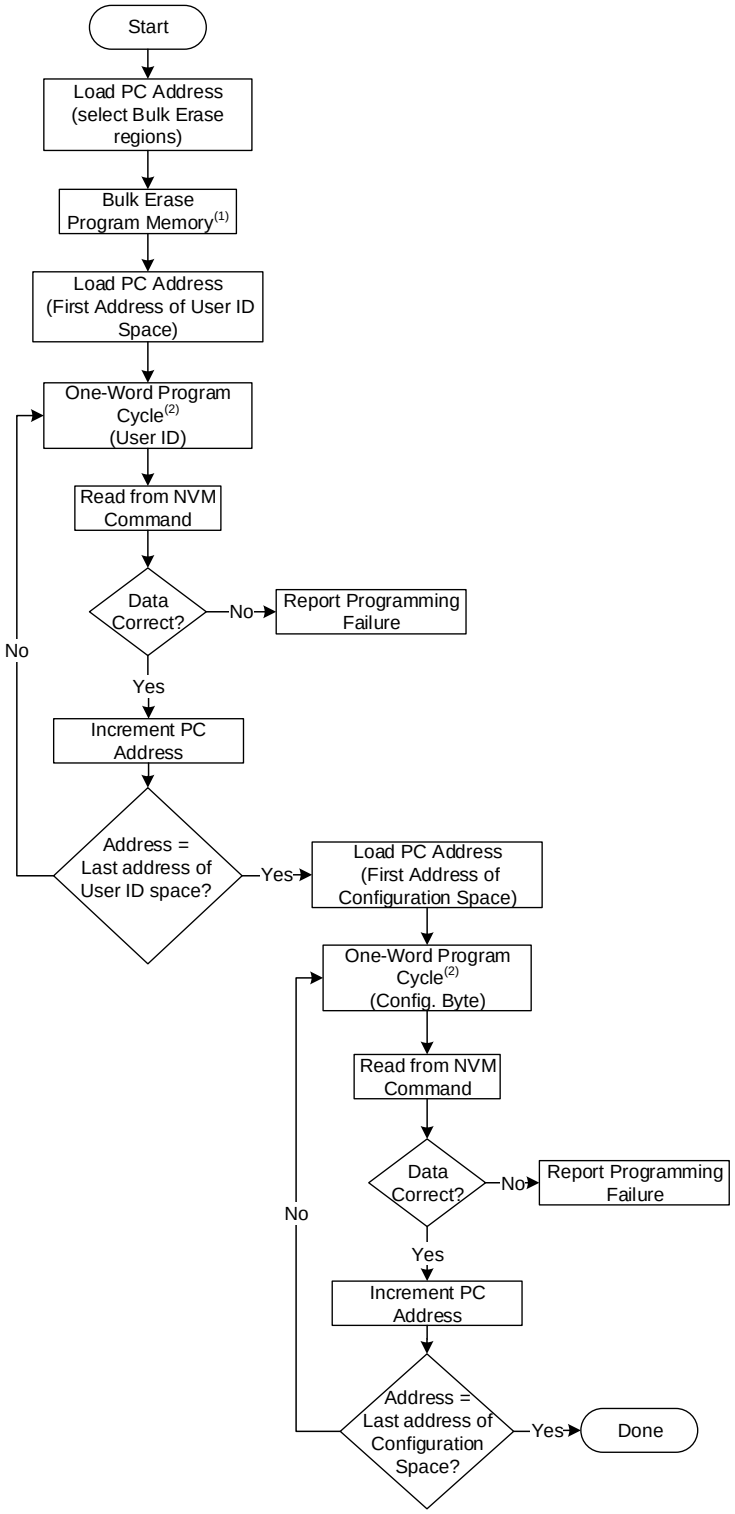


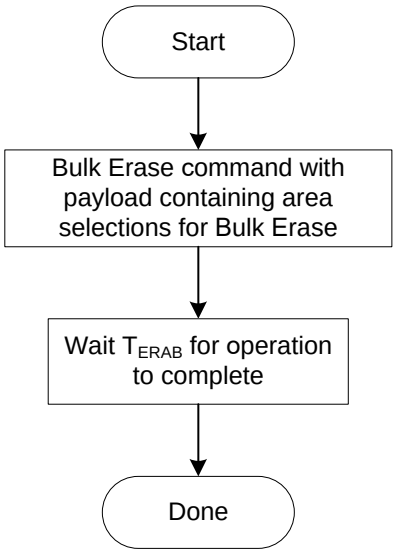
Figure 3-18. User ID and Configuration Memory Program Flowchart



Notes:

1. This step is optional if the device has already been erased or has not been previously programmed.
2. See Figure 3-17.

Figure 3-19. Bulk Erase Flowchart



3.3 Enhanced Code Protection

Code protection is controlled by utilizing the $\overline{CP}$ and $\overline{CPD}$ bits, the $\overline{WRTB}$, $\overline{WRTC}$, $\overline{WRTD}$, $\overline{WRTSAF}$, and $\overline{WRTAPP}$ bits, and the $\overline{SAFLOCK}$ bit in conjunction with the $\overline{SAFSZ}$ bits.

The $\overline{CP}$ and $\overline{CPD}$ bits control the code protection for the program memory and the Data EEPROM, respectively. When enabled, the corresponding memory location reads as '0' and further programming is disabled until a Bulk Erase operation is performed on the Configuration memory region. The program memory and Data EEPROM can still be programmed and read during program execution. Self-writes to the program memory and EEPROM are still possible through the NVM firmware.

The only way to disable code protection is to use the Bulk Erase command with the bit associated with Configuration memory in the payload set to '1'. This will clear the disable code protection and also erase all the memory locations.

The $\overline{WRTB}$, $\overline{WRTC}$, $\overline{WRTD}$, $\overline{WRTSAF}$ and $\overline{WRTAPP}$ bits control the write protection for the Boot Block, Configuration registers, Data EEPROM, Storage Area Flash (SAF), and the Application Block, respectively. When enabled, the corresponding memory location is write-protected and further programming is disabled until a Bulk Erase operation is performed on the Configuration memory region. The Boot Block, Data EEPROM, the SAF, and/or the Application Block can still be programmed and read during program execution through the NVM firmware.

The $\overline{SAFLOCK}$ bit allows for one-time programmability of the Storage Area Flash (SAF). This bit can only be enabled once. Once enabled (1), this bit cannot be disabled (even through a Bulk Erase operation) and locks the designated SAF area and the $\overline{SAFSZ}$ bits.

Setting the $\overline{SAFLOCK}$ bit requires the following sequence:

1. Send **Program Access Enable** Command with appropriate payload.
2. Send the **Program Data** Command to write to the $\overline{SAFLOCK}$ bit.

⚠ CAUTION

1. Once $\overline{SAFLOCK}$ bit is enabled, it CANNOT be disabled. Bulk Erase and self-erase operations are not possible. Use extreme caution with the $\overline{SAFLOCK}$ bit.

3.4 Hex File Usage

3.4.1 Embedding Configuration Information in the Hex File

To allow the portability of the code, a programmer is required to read the Configuration Byte locations from the hex file. If the Configuration Byte information is not present in the hex file, then a simple warning message will be issued. Similarly, when saving a hex file, all the Configuration Byte information will be included. An option not to include the Configuration Byte information may be provided. When embedding Configuration Byte information in the hex file, it will start at address 30 0000h.

Important:
This feature is highly important for the benefit of the end customer.

3.4.2 Embedding Data EEPROM Information in the Hex File

To allow the portability of the code, a programmer is required to read the Data EEPROM information from the hex file. If Data EEPROM information is not present, a simple warning message will be issued. Similarly, when saving a hex file, all Data EEPROM information must be included. An option not to include the Data EEPROM information may be provided. When embedding Data EEPROM information in the hex file, it will start at address 38 0000h.

Important:
This feature is highly important for the benefit of the end customer.

3.5 CRC Checksum Computation

Unlike older PIC® devices, the Microchip toolchain runs a 32-bit CRC calculation on the entire hex file to calculate its checksum. The checksum uses the standard CRC-32 algorithm with the polynomial 0x4C11DB7 $\left(x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1\right)$.

4. Electrical Specifications

Refer to the device specific data sheet for absolute maximum ratings.

Table 4-1. AC/DC Characteristics Timing Requirements for Program/Verify Mode

AC/DC Characteristics		Standard Operating Conditions Production Tested at +25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Programming Supply Voltages and Currents						
V_{DD}	Supply Voltage (V_{DDMIN}, V_{DDMAX})	1.80	—	5.50	V	**(Note 1)**
V_{PEW}	Read/Write and Page Erase Operations	V_{DDMIN}	—	V_{DDMAX}	V	
V_{BE}	Bulk Erase Operations	V_{BORMAX}	—	V_{DDMAX}	V	**(Note 2)**
I_{DDI}	Current on V_{DD}, Idle	—	—	1.0	mA	
I_{DDP}	Current on V_{DD}, Programming	—	—	10	mA	
I_{PP}	**V_{PP}**					
	Current on $\overline{MCLR}/V_{PP}$	—	—	600	µA	
V_{IHH}	High Voltage on $\overline{MCLR}/V_{PP}$ for Program/Verify Mode Entry	7.9	—	9.0	V	
T_{VHHR}	$\overline{MCLR}$ Rise Time (V_{IL} to V_{IHH}) for Program/Verify Mode Entry	—	—	1.0	µs	
V_{IH}	**I/O Pins**					
	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input High Level	0.8 V_{DD}	—	V_{DD}	V	
V_{IL}	(ICSPCLK, ICSPDAT, $\overline{MCLR}/V_{PP}$) Input Low Level	V_{SS}	—	0.2 V_{DD}	V	
V_{OH}	ICSPDAT Output High Level	V_{DD} – 0.7	—	—	V	I_{OH} = 3 mA, V_{DD} = 3.0V
V_{OL}	ICSPDAT Output Low Level	—	—	V_{SS} + 0.6	V	I_{OL} = 6 mA, V_{DD} = 3.0V
Programming Mode Entry and Exit						
T_{ENTS}	Programing Mode Entry Setup Time: ICSPCLK, ICSPDAT Setup Time before V_{DD} or $\overline{MCLR}$↑	100	—	—	ns	
T_{ENTH}	Programing Mode Entry Hold Time: ICSPCLK, ICSPDAT Hold Time before V_{DD} or $\overline{MCLR}$↑	1	—	—	ms	
Serial Program/Verify						
T_{CKL}	Clock Low Pulse Width	100	—	—	ns	
T_{CKH}	Clock High Pulse Width	100	—	—	ns	
T_{DS}	Data in Setup Time before Clock↓	100	—	—	ns	
T_{DH}	Data in Hold Time after Clock↓	100	—	—	ns	
T_{CO}	Clock↑ to Data Out Valid (during a Read Data command)	0	—	80	ns	
T_{LZD}	Clock↓ to Data Low-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{HZD}	Clock↓ to Data High-Impedance (during a Read Data from NVM command)	0	—	80	ns	
T_{DLY}	Data Input not Driven to Next Clock Input (delay required between command/data or command/command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase Cycle Time	—	—	11	ms	Program, Config and ID
T_{ERAS}	Page Erase Cycle Time	—	—	11	ms	
T_{PDFM}	Internally Timed DFM (EEPROM) Programming Operation Time	—	—	11	ms	EEPROM Memory and Configuration Bytes
T_{PINT}	Internally Timed Programming Operation Time	—	—	75	µs	Program Memory and Configuration Bytes

.....continued						
AC/DC Characteristics		Standard Operating Conditions Production Tested at +25°C				
Sym.	Characteristics	Min.	Typ.	Max.	Units	Conditions/Comments
T_{EXIT}	Time Delay when Exiting Program/Verify Mode	1	—	—	µs	

Notes:

1. Bulk erased devices default to Brown-out Reset enabled with BORV = `11` (low trip point). V_{DDMIN} is the V_{BOR} threshold (with BORV = `1`) when performing Low-Voltage Programming on a bulk erased device to ensure that the device is not held in Brown-out Reset.
2. The hardware requires V_{DD} to be above the BOR threshold, at the ~2.85V nominal setting, to perform Bulk Erase operations. This threshold does not depend on the BORV Configuration bit settings. Refer to the microcontroller device data sheet specifications for Min./Typ./Max. limits of the V_{BOR} level.

5. Appendix A: Revision History

Doc Rev.	Date	Comments
B	03/2022	Updated Sections 1.4.1, 2.4, 3.1, 3.1.3.1, 3.1.3.5, 3.1.3.7, and 3.3. Updated Figure 2-1.
A	06/2021	Initial document release.

6. Appendix B

This section provides information about the device IDs and pinout descriptions.

Table 6-1. Programming Pin Locations by Package Type

Device	Package	Package Code	V_{DD}	V_{SS}	$\overline{MCLR}$		ICSPCLK		ICSPDAT	
			PIN	PIN	PIN	PORT	PIN	PORT	PIN	PORT
PIC18F04Q20 PIC18F05Q20 PIC18F06Q20	14-Pin SOIC	SL	1	14	4	RA3	12	RA1	13	RA0
	14-Pin TSSOP	ST	1	14	4	RA3	12	RA1	13	RA0
PIC18F14Q20 PIC18F15Q20 PIC18F16Q20	20-Pin PDIP	P	1	20	4	RA3	18	RA1	19	RA0
	20-Pin SOIC	SO	1	20	4	RA3	18	RA1	19	RA0
	20-Pin SSOP	SS	1	20	4	RA3	18	RA1	19	RA0
	20-Pin VQFN	REB	18	17	1	RA3	15	RA1	16	RA0

Note:
The most current package drawings are located in the Microchip Packaging Specification, DS00000049 (http://www.microchip.com/packaging). The drawing numbers listed above do not include the current revision designator, which is added at the end of the number.

6.1 CONFIG1

Name: CONFIG1
Offset: 30 0000h

Configuration Byte 1

Bit	7	6	5	4	3	2	1	0
		RSTOSC[2:0]				FEXTOSC[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		1	1	1		1	1	1

Bits 6:4 – RSTOSC[2:0] Power-up Default Value for COSC
This value is the Reset default value for COSC and selects the oscillator first used by user software. Refer to COSC operation.

Value	Description
111	EXTOSC operating per FEXTOSC bits
110	HFINTOSC with HFFRQ = 4 MHz and CDIV = 4:1. Resets COSC/NOSC to b'110'
101	LFINTOSC
100	SOSC
011	Reserved
010	EXTOSC with 4x PLL, with EXTOSC operating per FEXTOSC bits
001	Reserved
000	HFINTOSC with HFFRQ = 64 MHz and CDIV = 1:1. Resets COSC/NOSC to b'110'

Bits 2:0 – FEXTOSC[2:0] External Oscillator Mode Selection

Value	Description
111	ECH (external clock) above 8 MHz
110	ECM (external clock) for 500 kHz to 8 MHz
101	ECL (external clock) below 500 kHz
100	Oscillator not enabled
011	HS (crystal oscillator) up to 32 MHz
010	HS (crystal oscillator) up to 24 MHz
001	HS (crystal oscillator) up to 16 MHz
000	HS (crystal oscillator) up to 8 MHz

6.2 CONFIG2

Name: CONFIG2
Offset: 30 0001h

Configuration Byte 2

Bit	7	6	5	4	3	2	1	0
	FCMENS	FCMENP	FCMEN		CSWEN	$\overline{\text{BBEN}}$	PR1WAY	$\overline{\text{CLKOUTEN}}$
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset	1	1	1		1	1	1	1

Bit 7 – FCMENS Fail-Safe Clock Monitor Enable - Secondary XTAL Enable

Value	Description
1	Fail-Safe Clock Monitor enabled; the timer will flag the FSCMS bit and OSFIF interrupt on SOSC failure
0	Fail-Safe Clock Monitor disabled

Bit 6 – FCMENP Fail-Safe Clock Monitor Enable - Primary XTAL Enable

Value	Description
1	Fail-Safe Clock Monitor enabled; the timer will flag the FSCMP bit and OSFIF interrupt on EXTOSC failure
0	Fail-Safe Clock Monitor disabled

Bit 5 – FCMEN Fail-Safe Clock Monitor Enable

Value	Description
1	Fail-Safe Clock Monitor enabled
0	Fail-Safe Clock Monitor disabled

Bit 3 – CSWEN Clock Switch Enable

Value	Description
1	Writing to NOSC and NDIV is allowed
0	The NOSC and NDIV bits cannot be changed by user software

Bit 2 – $\overline{\text{BBEN}}$ Boot Block Enable(1)

Value	Description
1	Boot Block disabled
0	Book Block enabled

Bit 1 – PR1WAY PRLOCKED One-Way Set Enable

Value	Description
1	PRLOCKED bit can be cleared and set only once; Priority registers remain locked after one clear/set cycle
0	PRLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 0 – $\overline{\text{CLKOUTEN}}$ Clock Out Enable
If FEXTOSC = 0xx, then this bit is ignored.
Otherwise:

Value	Description
1	CLKOUT function is disabled; I/O or oscillator function on OSC2
0	CLKOUT function is enabled; F_{OSC}/4 clock appears at OSC2

Note:

1. Once protection is enabled through ICSP or a self-write, it can only be reset through a Bulk Erase.

6.3 CONFIG3

Name: CONFIG3
Offset: 30 0002h

Configuration Byte 3

Bit	7	6	5	4	3	2	1	0
	BOREN[1:0]		$\overline{\text{LPBOREN}}$	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 12:6 – BOREN[6:0] Brown-out Reset Enable
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit.

Value	Description
11	Brown-out Reset enabled, SBOREN bit is ignored
10	Brown-out Reset enabled while running, disabled in Sleep; SBOREN is ignored
01	Brown-out Reset enabled according to SBOREN
00	Brown-out Reset disabled

Bit 5 – $\overline{\text{LPBOREN}}$ Low-Power BOR Enable

Value	Description
1	Low-Power Brown-out Reset is disabled
0	Low-Power Brown-out Reset is enabled

Bit 4 – IVT1WAY IVTLOCK One-Way Set Enable

Value	Description
1	IVTLOCK bit can be cleared and set only once; IVT registers remain locked after one clear/set cycle
0	IVTLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)

Bit 3 – MVECEN Multi-Vector Enable

Value	Description
1	Multi-vector is enabled; Vector table used for interrupts
0	Legacy interrupt behavior

Bits 2:1 – PWRTS[1:0] Power-up Timer Selection

Value	Description
11	PWRT is disabled
10	PWRT is set at 64 ms
01	PWRT is set at 16 ms
00	PWRT is set at 1 ms

Bit 0 – MCLRE Master Clear ($\overline{\text{MCLR}}$) Enable

Value	Condition	Description
x	If LVP = 1	RA3 pin function is $\overline{\text{MCLR}}$
1	If LVP = 0	$\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$
0	If LVP = 0	$\overline{\text{MCLR}}$ pin function is a port defined function

6.4 CONFIG4

Name: CONFIG4
Offset: 30 0003h

Configuration Byte 4

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{XINST}}$	$\overline{\text{DEBUG}}$	LVP	STVREN	PPS1WAY		BORV[1:0]	
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	1	1	1	1	1		1	1

Bit 7 – $\overline{\text{XINST}}$ Extended Instruction Set Enable

Value	Description
1	Extended Instruction Set and Indexed Addressing mode disabled (Legacy mode)
0	Extended Instruction Set and Indexed Addressing mode enabled

Bit 6 – $\overline{\text{DEBUG}}$ Debugger Enable

Value	Description
1	Background debugger disabled
0	Background debugger enabled

Bit 5 – LVP Low-Voltage Programming Enable
The LVP bit cannot be written (to zero) while operating from the LVP programming interface. The purpose of this rule is to prevent the user from dropping out of LVP mode while programming from LVP mode, or accidentally eliminating LVP mode from the Configuration state.

Value	Description
1	Low-Voltage Programming enabled. $\overline{\text{MCLR}}/V_{PP}$ pin function is $\overline{\text{MCLR}}$. The MCLRE Configuration bit is ignored.
0	High Voltage on $\overline{\text{MCLR}}/V_{PP}$ must be used for programming

Bit 4 – STVREN Stack Overflow/Underflow Reset Enable

Value	Description
1	Stack Overflow or Underflow will cause a Reset
0	Stack Overflow or Underflow will not cause a Reset

Bit 3 – PPS1WAY PPSLOCKED One-Way Set Enable

Value	Description
1	The PPSLOCK bit can be cleared and set only once after an unlocking sequence is executed; once PPSLOCK is set, all future changes to PPS registers are prevented
0	The PPSLOCK bit can be set and cleared as needed (unlocking sequence is required)

Bits 1:0 – BORV[1:0] Brown-out Reset Voltage Selection (1)

Value	Description
11	Brown-out Reset Voltage (V_{BOR}) set to 1.90V
10	Brown-out Reset Voltage (V_{BOR}) set to 2.45V
01	Brown-out Reset Voltage (V_{BOR}) set to 2.7V
00	Brown-out Reset Voltage (V_{BOR}) set to 2.85V

Note:
1. The higher voltage setting is recommended for an operation at or above 16 MHz.

6.5 CONFIG5

Name: CONFIG5
Offset: 30 0004h

Configuration Byte 5

Bit	7	6	5	4	3	2	1	0
		WDTE[1:0]		WDTCPS[4:0]				
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	1	1	1	1	1

Bits 6:5 – WDTE[1:0] WDT Operating Mode

Value	Description
11	WDT enabled regardless of Sleep; SEN bit in WDTCON0 is ignored
10	WDT enabled while Sleep = 0, suspended when Sleep = 1; SEN bit in WDTCON0 is ignored
01	WDT enabled/disabled by SEN bit in WDTCON0
00	WDT disabled, SEN bit in WDTCON0 is ignored

Bits 4:0 – WDTCPS[4:0] WDT Period Select

WDTCPS	WDTCON0[WDTPS] at POR				Software Control of WDTPS?
	Value	Divider Ratio		Typical Time Out (F_{IN} = 31 kHz)	
11111	01011	1:65536	2^{16}	2s	Yes
11110 to 10011	11110 to 10011	1:32	2^{5}	1 ms	No
10010	10010	1:8388608	2^{23}	256s	No
10001	10001	1:4194304	2^{22}	128s	No
10000	10000	1:2097152	2^{21}	64s	No
01111	01111	1:1048576	2^{20}	32s	No
01110	01110	1:524288	2^{19}	16s	No
01101	01101	1:262144	2^{18}	8s	No
01100	01100	1:131072	2^{17}	4s	No
01011	01011	1:65536	2^{16}	2s	No
01010	01010	1:32768	2^{15}	1s	No
01001	01001	1:16384	2^{14}	512 ms	No
01000	01000	1:8192	2^{13}	256 ms	No
00111	00111	1:4096	2^{12}	128 ms	No
00110	00110	1:2048	2^{11}	64 ms	No
00101	00101	1:1024	2^{10}	32 ms	No
00100	00100	1:512	2^{9}	16 ms	No
00011	00011	1:256	2^{8}	8 ms	No
00010	00010	1:128	2^{7}	4 ms	No
00001	00001	1:64	2^{6}	2 ms	No
00000	00000	1:32	2^{5}	1 ms	No

6.6 CONFIG6

Name: CONFIG6
Offset: 30 0005h

Configuration Byte 6

Bit	7	6	5	4	3	2	1	0
			WDTCCS[2:0]			WDTCWS[2:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:3 – WDTCCS[2:0] WDT Input Clock Selector

Value	Condition	Description
x	WDTE = 00	These bits have no effect
111	WDTE ≠ 00	Software control
110 to 011	WDTE ≠ 00	Reserved
010	WDTE ≠ 00	WDT reference clock is the SOSC
001	WDTE ≠ 00	WDT reference clock is the 32 kHz MFINTOSC
000	WDTE ≠ 00	WDT reference clock is the 31.0 kHz LFINTOSC

Bits 2:0 – WDTCWS[2:0] WDT Window Select

WDTCWS	WDTCON1[WINDOW] at POR			Software Control of WINDOW	Keyed Access Required?
	Value	Window Delay Percent of Time	Window Opening Percent of Time		
111	111	n/a	100	Yes	No
110	110	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

6.7 CONFIG7

Name: CONFIG7
Offset: 30 0006h

Configuration Byte 7

Bit	7	6	5	4	3	2	1	0
							VDDIO3MD	VDDIO2MD
Access							R/W	R/W
Reset							1	1

Bit 1 – VDDIO3MD V_{DDIO3} Supply Mode

Value	Description
1	Dual Supply mode, POR in V_{DDIO3} domain is armed by BOR in V_{DDIO3} domain. All analog functions are disabled on V_{DDIO3} pins except for I^2C and I3C®.
0	Single Supply mode, POR and BOR in V_{DDIO3} domain are disabled. All analog functions are available on V_{DDIO3} pins unless otherwise restricted.

Bit 0 – VDDIO2MD V_{DDIO2} Supply Mode

Value	Description
1	Dual Supply mode, POR in V_{DDIO2} domain is armed by BOR inV_{DDIO2} domain. All analog functions are disabled on V_{DDIO2} pins except for I^2C and I3C.
0	Single Supply mode, POR and BOR in V_{DDIO2} domain are disabled. All analog functions are available on V_{DDIO2} pins unless otherwise restricted.

6.8 CONFIG8

Name: CONFIG8
Offset: 30 0007h

Configuration Byte 8

Bit	7	6	5	4	3	2	1	0
	BBSIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – BBSIZE[7:0] Boot Block Size Selection(1)

Table 6-2. Boot Block Size

$\overline{\text{BBEN}}$	BBSIZE	End Address of Boot Block	Boot Block Size (words)		
			PIC18Fx4Q20	PIC18Fx5Q20	PIC18Fx6Q20
1	xxxxxxxx	N/A	N/A		
0	01111111	00 7FFFh	N/A		16384
0	01111110	00 7EFFh	N/A		16256
...	...	...	...		
0	01000000	00 40FFh	N/A		8320
0	00111111	00 3FFFh	N/A	8192	
0	00111110	00 3EFFh	N/A	8064	
...	...	...	...		
0	00100000	00 20FFh	N/A	4224	
0	00011111	00 1FFFh	4096		
0	00011110	00 1EFFh	3968		
...	...	...	...		
0	00000011	00 03FFh	512		
0	00000010	00 02FFh	384		
0	00000001	00 01FFh	256		
0	00000000	00 00FFh	128		

Note:

1. BBSIZE[7:0] bits can only be changed when $\overline{\text{BBEN}}$ = 1. Once $\overline{\text{BBEN}}$ = 0, BBSIZE[7:0] can only be changed through a Bulk Erase.

6.9 CONFIG9

Name: CONFIG9
Offset: 30 0019h

Configuration Byte 9

Bit	7	6	5	4	3	2	1	0
	SAFSZ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – SAFSZ[7:0] SAF Block Size Selection(1, 2)

Table 6-3. SAF Block Size

$\overline{\text{WRTSAF}}$	$\overline{\text{SAFLOCK}}$	SAFSZ[7:0]	Size of SAF Block			Bulk Erase	Self-write
			PIC18Fx4Q20	PIC18Fx5Q20	PIC18Fx6Q20		
1	1	1111 1111	–			Yes	Yes
1	1	1111 1110	Last 128 words of PFM			Yes	Yes
1	1	1111 110x	Last 256 words of PFM			Yes	Yes
1	1	1111 10xx	Last 384 words of PFM			Yes	Yes
1	1	1111 0xxx	Last 512 words of PFM			Yes	Yes
1	1	1110 xxxx	Last 640 words of PFM			Yes	Yes
1	1	110x xxxx	Last 768 words of PFM			Yes	Yes
1	1	10xx xxxx	Last 896 words of PFM			Yes	Yes
1	1	0xxx xxxx	Last 1024 words of PFM			Yes	Yes
0	1	1111 1111	–			Yes	No
0	1	1111 1110	Last 128 words of PFM			Yes	No
0	1	1111 110x	Last 256 words of PFM			Yes	No
0	1	1111 10xx	Last 384 words of PFM			Yes	No
0	1	1111 0xxx	Last 512 words of PFM			Yes	No
0	1	1110 xxxx	Last 640 words of PFM			Yes	No
0	1	110x xxxx	Last 768 words of PFM			Yes	No
0	1	10xx xxxx	Last 896 words of PFM			Yes	No
0	1	0xxx xxxx	Last 1024 words of PFM			Yes	No
x	0	1111 1111	–			No	No
x	0	1111 1110	Last 128 words of PFM			No	No
x	0	1111 110x	Last 256 words of PFM			No	No
x	0	1111 10xx	Last 384 words of PFM			No	No
x	0	1111 0xxx	Last 512 words of PFM			No	No
x	0	1110 xxxx	Last 640 words of PFM			No	No
x	0	110x xxxx	Last 768 words of PFM			No	No
x	0	10xx xxxx	Last 896 words of PFM			No	No
x	0	0xxx xxxx	Last 1024 words of PFM			No	No

Notes:

1. When $\overline{\text{SAFLOCK}}$ = 0, once a SAFSZ bit is programmed to 0 through ICSP or a self-write, it can never be erased to a '1', not even through a Bulk Erase. Refer to "Enhanced Code Protection" section for details.
2. When $\overline{\text{SAFLOCK}}$ = 1, once a SAFSZ bit is programmed to 0 through ICSP or a self-write, it can only be reset though a Bulk Erase.

6.10 CONFIG10

Name: CONFIG10
Offset: 30 0008h

Configuration Byte 10

Bit	7	6	5	4	3	2	1	0
	$\overline{\text{WRTAPP}}$				$\overline{\text{WRTSAF}}$	$\overline{\text{WRTD}}$	$\overline{\text{WRTC}}$	$\overline{\text{WRTB}}$
Access	R/W				R/W	R/W	R/W	R/W
Reset	1				1	1	1	1

Bit 7 – $\overline{\text{WRTAPP}}$ Application Block Write Protection(1)

Value	Description
1	Application Block is not write-protected
0	Application Block is write-protected

Bit 3 – $\overline{\text{WRTSAF}}$ Storage Area Flash (SAF) Write Protection(1)

Value	Description
1	SAF is not write-protected
0	SAF is write-protected

Bit 2 – $\overline{\text{WRTD}}$ Data EEPROM Write Protection(1)

Value	Description
1	Data EEPROM is not write-protected
0	Data EEPROM is write-protected

Bit 1 – $\overline{\text{WRTC}}$ Configuration Register Write Protection(1)

Value	Description
1	Configuration registers are not write-protected
0	Configuration registers are write-protected

Bit 0 – $\overline{\text{WRTB}}$ Boot Block Write Protection (1,2)

Value	Description
1	Boot Block is not write-protected
0	Boot Block is write-protected

Notes:

1. Once protection is enabled through ICSP™ or a self-write, it can only be reset through a Bulk Erase.
2. Applicable only if $\overline{\text{BBEN}}$ = 0.

6.11 CONFIG11

Name: CONFIG11
Offset: 30 0009h

Configuration Byte 11

Bit	7	6	5	4	3	2	1	0
								$\overline{CP}$
Access								R/W
Reset								1

Bit 0 – $\overline{CP}$ User Program Flash Memory (PFM) Code Protection(2)

Value	Description
1	User PFM code protection is disabled
0	User PFM code protection is enabled

Notes:

1. Since device code protection takes effect immediately, this Configuration Byte will be written last.
2. Once protection is enabled, it can only be reset through a Bulk Erase.

6.12 CONFIG12

Name: CONFIG12
Offset: 30 000Ah

Configuration Byte 12

Bit	7	6	5	4	3	2	1	0
								$\overline{\text{CPD}}$
Access								R/W
Reset								1

Bit 0 – $\overline{\text{CPD}}$ Data EEPROM Code Protection(2)

Value	Description
1	Data EEPROM code protection is disabled
0	Data EEPROM code protection is enabled

Notes:

1. Since device code protection takes effect immediately, this Configuration Byte will be written last.
2. Once protection is enabled, it can only be reset through a Bulk Erase.

6.13 CONFIG14

Name: CONFIG14
Offset: 30 0018h

Configuration Byte 14

Bit	7	6	5	4	3	2	1	0
								$\overline{\text{SAFLOCK}}$
Access								R/W
Reset								1

Bit 0 – $\overline{\text{SAFLOCK}}$ SAF Lock Enable[(1)]

Value	Description
1	SAF Lock disabled
0	SAF Lock enabled, SAF areas are locked and SAFSZ bits cannot be erased

⚠ CAUTION

1. This is a one-way bit. Once cleared it cannot be set again. Reset through bulk erase and self erase are also not possible.

6.14 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
00 ... 2FFFFF	Reserved									
300000	CONFIG1	7:0		RSTOSC[2:0]				FEXTOSC[2:0]		
300001	CONFIG2	7:0	FCMENS	FCMENP	FCMEN		CSWEN	BBEN	PR1WAY	CLKOUTEN
300002	CONFIG3	7:0	BOREN[1:0]		LPBOREN	IVT1WAY	MVECEN	PWRTS[1:0]		MCLRE
300003	CONFIG4	7:0	XINST	DEBUG	LVP	STVREN	PPS1WAY		BORV[1:0]	
300004	CONFIG5	7:0		WDTE[1:0]		WDTCPS[4:0]				
300005	CONFIG6	7:0			WDTCCS[2:0]			WDTCWS[2:0]		
300006	CONFIG7	7:0							VDDIO3MD	VDDIO2MD
300007	CONFIG8	7:0	BBSIZE[7:0]							
300008	CONFIG10	7:0	WRTAPP				WRTSAF	WRTD	WRTC	WRTB
300009	CONFIG11	7:0								CP
30000A	CONFIG12	7:0								CPD
30000B ... 300017	Reserved									
300018	CONFIG14	7:0								SAFLOCK
300019	CONFIG9	7:0	SAFSZ[7:0]							

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ISBN: 978-1-5224-9935-0

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