Control integrated power system (CIPOS™)

CIPOS™ Mini IPM technical description

About this document

Scope and purpose

The scope of this application note is to describe the CIPOS™ Mini intelligent power modules (IPM) and the basic requirements for operating the products in the recommended mode. It includes integrated components such as IGBTs, gate driver ICs, and the design of the required external circuitry such as bootstrap and interfacing.

Intended audience

Power electronics engineers who want to design reliable and efficient CIPOS™ Mini IPM applications.

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1 Scope

Integrating discrete power semiconductors and drivers into one package reduces the time and effort spent on design. To meet the strong demand for small size and higher power density, Infineon has developed a new family of highly integrated intelligent power modules that comprise nearly all semiconductor components required to drive electronically-controlled, variable-speed electric motors. They incorporate a silicon-on-insulator (SOI) gate driver and Infineon's leading-edge TRENCHSTOP™ IGBT and anti-parallel diode, or reverse-conducting IGBT for drives.

1.1 Product line-up

Table 1 Products covered in this application note

Part number	Rating		Inverter circuit	Package	Isolation voltage	Main applications
	Current [A]	Voltage [V]				
IM523-S6A	6	600	Open emitter	Full-pack dual-in-line module	2000 V_{rms} sinusoidal, 1 min.	Washing machines, fans, pumps
IM523-M6A	10	600				
IM523-L6A	15	600				
IM523-X6A	17	600				
IM535-U6D	30	600		DCB dual-in-line module		Air conditioners, general purpose drives
IM535-U6DS	30	600				

1.2 Nomenclature

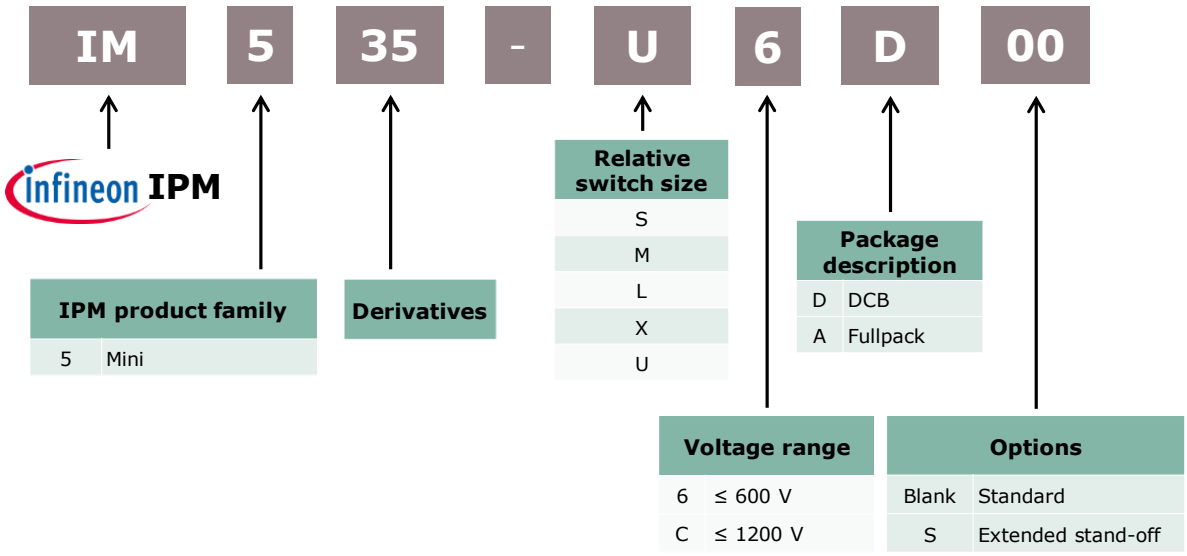


Figure 1 CIPOS™ Mini IPM product nomenclature

2 Internal components and package technology

2.1 Power transistor technology

Infineon introduced the TRENCHSTOP™ IGBT technology in 2000 [1]. This field-proven technology provides features such as short-circuit withstand capability and high maximum junction temperature. All advantages of this technology have been utilized to achieve the highest efficiency and power density through low saturation voltage and excellent dynamic parameters.

2.2 Power diode technology

The emitter-controlled diode is Infineon's unique, fast-recovery diode technology. The ultra-thin wafer and fieldstop technology make the emitter-controlled diode ideal for consumer and industrial applications, lowering the turn-on losses of the IGBT with soft recovery. The emitter-controlled diode has been optimized for Infineon's IGBT technology [2].

2.3 Control IC: six-channel gate driver IC

The basic feature of this technology is the separation of the active silicon from the base material by a buried silicon oxide layer. The buried silicon oxide provides an insulation barrier between the active layer and the silicon substrate, hence reducing the parasitic capacitance tremendously. This insulation barrier also disables leakage or latch-up currents between adjacent devices. It prevents latch-up effect even in the case of high dv/dt switching under elevated temperatures, thus providing improved robustness. In addition, the thin-film SOI technology provides benefits such as lower power consumption and higher immunity to radioactive radiation or cosmic rays [3]. A monolithic single-control IC for all six IGBTs provides further advantages, such as bootstrap circuitry, matched propagation delay times, built-in deadtime, and cross-conduction prevention. In addition, all six IGBTs turn off under fault situations such as undervoltage lockout (UVLO) or overcurrent.

2.4 Thermistor

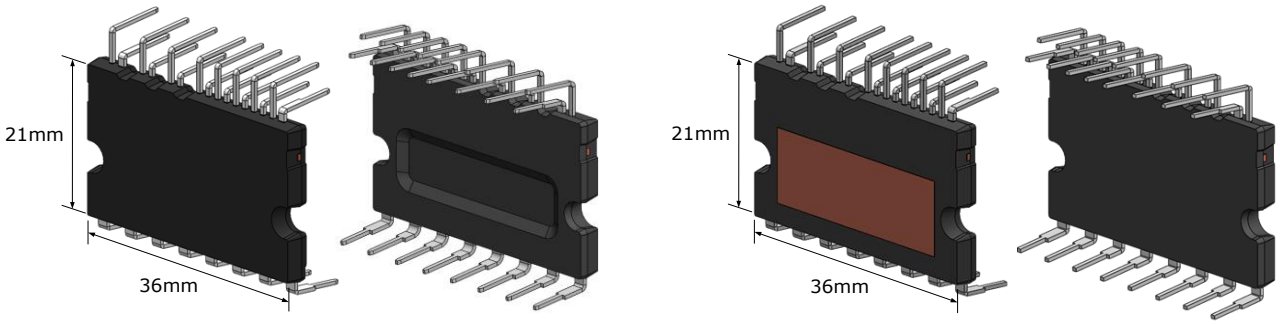
In the CIPOS™ Mini, the thermistor is integrated on the internal printed circuit board (PCB). It is connected between the V_{FO} and V_{SS} pins. A circuit proposal using the thermistor for overtemperature protection is discussed in Section 5.4.

Table 2 Raw data of the thermistor used in CIPOS™ Mini

Temperature [°C]	R_{min} [kΩ]	R_{typ} [kΩ]	R_{max} [kΩ]	Tolerance [%]
-40	2662.292	2962.540	3262.789	10.1
-35	1925.308	2133.692	2342.076	9.8
-30	1407.191	1553.414	1699.637	9.4
-25	1038.949	1142.63	1246.312	9.1
-20	774.497	848.747	922.997	8.7
-15	582.690	636.369	690.048	8.4
-10	442.252	481.410	520.568	8.1
-5	338.491	367.303	396.114	7.8
0	261.164	282.537	303.910	7.6
5	203.056	219.036	235.016	7.3
10	159.044	171.081	183.118	7.0
15	125.454	134.586	143.717	6.8
20	99.630	106.605	113.580	6.5
25	79.638	85.000	90.362	6.3
30	64.055	68.203	72.352	6.1
35	51.831	55.059	58.287	5.9
40	42.182	44.708	47.235	5.7
45	34.520	36.508	38.496	5.4
50	28.400	29.972	31.545	5.2
55	23.485	24.735	25.985	5.1
60	19.517	20.515	21.514	4.9
65	16.296	17.097	17.898	4.7
70	13.670	14.315	14.960	4.5
75	11.517	12.039	12.561	4.3
80	9.745	10.169	10.593	4.2
85	8.279	8.625	8.971	4.0
90	7.062	7.345	7.628	3.9
95	6.046	6.279	6.511	3.7
100	5.199	5.388	5.576	3.5
105	4.468	4.640	4.811	3.7
110	3.856	4.009	4.163	3.8
115	3.338	3.477	3.615	4.0
120	2.900	3.024	3.149	4.1
125	2.527	2.639	2.751	4.2

2.5 Package technology

The CIPOS™ Mini offers a small package size, while providing high power density. The molding compound or the ceramic layer of the direct copper bonding (DCB) that is simultaneously the thermal contact to the heat sink, provides the electric insulation. To decrease the thermal impedance further the internal lead frame design has been optimized [4]. All low-power components such as the gate drive IC and thermistor are assembled on the PCB. Figure 2 shows the external view of CIPOS™ Mini package options.



(a) Full-pack type *(b) DCB type*

Figure 2 External view of CIPOS™ Mini IPM packages

3 Product overview

3.1 Internal circuit and features

Figure 3 shows the internal block diagram of the CIPOS™ Mini IPM. It consists of a 3-phase IGBT inverter circuit and a driver IC with control functions. Detailed features and integrated functions of this IPM are described as follows:

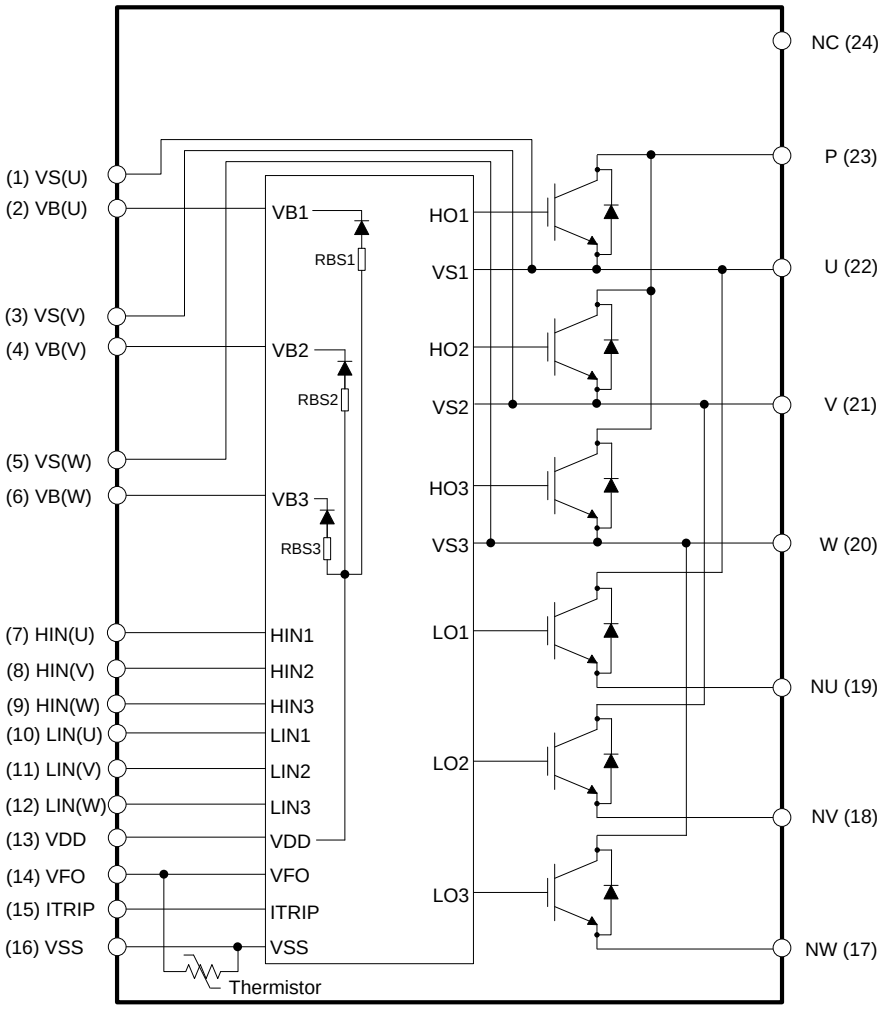


Figure 3 Internal circuit

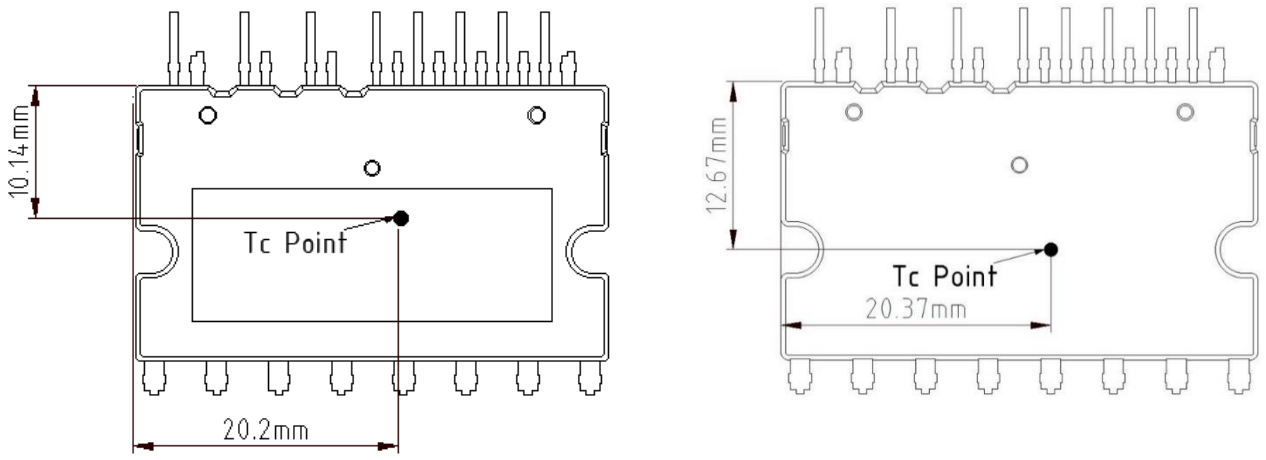
- Package
  - Fully isolated dual in-line (DIL) molded module
  - Lead free terminal plating; RoHS-compliant
- Inverter
  - TRENCHSTOP™ IGBTs with separate freewheeling diode or RC IGBTs
  - SOI gate driver technology robust against transient and negative voltage
  - Integrated bootstrap functionality
  - Matched delay time of all channels
  - Built-in deadtime
- SOI gate driver functions

- Overcurrent shutdown
- Temperature monitor
- Undervoltage lockout at all channels
- Anti cross-conduction
- All six switches turn off during protection
- Active-high input signal logic

3.2 Maximum electrical ratings

Table 3 Detailed description of absolute maximum ratings for IM535-U6D

Item	Symbol	Rating	Description
Max. blocking voltage	V_{CES}	600 V	The sustained collector-emitter voltage of internal IGBTs
Continuous collector current	I_C	±30 A	The allowed continuous IGBT current at T_C = 25°C
Junction temperature	T_J	-40 ~ 150°C	Considering the temperature ripple on power chips, the maximum junction temperature rating of CIPOS™ Mini is 150°C
Operating case temperature range	T_C	-40 ~ 125°C	T_C (case temperature) is defined as the temperature of the package surface underneath the specified power chip. To get the accurate temperature, a temperature sensor must be mounted on the heat sink surface at the position shown in Figure 4



(a) IM535 series (b) IM523 series

Figure 4 T_C measurement point

3.3 Description of the input and output pins

Table 4 defines the CIPOS™ Mini IPM input and output pins. The detailed functional descriptions are as follows:

Table 4 Pin description of CIPOS™ Mini IPM

Pin number	Pin name	Pin description
1	V_S(U)	U-phase, high-side floating IC supply offset voltage
2	V_B(U)	U-phase, high-side floating IC supply voltage
3	V_S(V)	V-phase, high-side floating IC supply offset voltage
4	V_B(V)	V-phase, high-side floating IC supply voltage
5	V_S(W)	W-phase, high-side floating IC supply offset voltage
6	V_B(W)	W-phase, high-side floating IC supply voltage
7	HIN(U)	U-phase, high-side gate driver input
8	HIN(V)	V-phase, high-side gate driver input
9	HIN(W)	W-phase, high-side gate driver input
10	LIN(U)	U-phase, low-side gate driver input
11	LIN(V)	V-phase, low-side gate driver input
12	LIN(W)	W-phase, low-side gate driver input
13	V_{DD}	Low-side control supply
14	V_{FO}	Fault output / temperature monitor
15	ITRIP	Overcurrent shutdown input
16	V_{SS}	Low-side control negative supply
17	NW	W-phase, low-side emitter
18	NV	V-phase, low-side emitter
19	NU	U-phase, low-side emitter
20	W	Motor W-phase output
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No connection

High-side bias voltage pins for driving the IGBT

Pins: V_B(U), V_S(U), V_B(V), V_S(V), V_B(W), V_S(W)

- These pins provide the gate drive power to the high-side IGBTs
- Using a bootstrap circuit scheme for the high-side IGBTs eliminates the need for external power supplies
- Each bootstrap capacitor is charged from the V_{DD} supply during the on-state of the corresponding low-side IGBT or during the freewheeling state of the low-side freewheeling diode
- To prevent malfunctioning caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to these pins

Low-side bias voltage pin

Pin: V_{DD}

- This is the control supply pin for the internal gate driver
- To prevent malfunctioning caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted very close to this pin

Low-side common supply ground pin

Pin: V_{SS}

- This pin connects the control ground for the internal gate driver

Signal input pins

Pins: HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)

- These pins control the operation of the internal IGBTs
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt trigger circuit composed of 5 V-class CMOS
- The signal logic of these pins is active-high. The IGBT associated with each of these pins will be turned "on" when a sufficient logic voltage is applied to the pins
- The wiring of each input should be as short as possible to protect the CIPOS™ Mini against noise
- To prevent signal oscillations, an RC filter is recommended as shown in Figure 8

Overcurrent detection pin

Pin: ITRIP

- The current sensing shunt resistor should be connected between the pin N (emitter of low-side IGBT) and the power ground to detect short-circuit current (see Figure 10). An RC filter should be connected between the shunt resistor and the ITRIP pin to eliminate noise
- The integrated comparator is triggered if the voltage V_{ITRIP} is higher than 0.525 V. The shunt resistor should be selected to meet this level for the specific application. In case of a trigger event, the voltage at pin V_{FO} pin is pulled down to low
- The connection length between the shunt resistor and ITRIP pin should be minimized

Fault output and temperature-monitoring pin

Pin: V_{FO}

- This is the fault output alarm pin. An active-low output is given on this pin for a fault-state condition in the CIPOS™ Mini. The alarm conditions are overcurrent detection and low-side bias undervoltage operation
- The V_{FO} output is open-drain configured. The V_{FO} signal line should be pulled up to the logic power supply (5 V / 3.3 V) with proper resistance. The pull-up resistor value should be properly selected considering the internal thermistor between the V_{FO} and V_{SS} pins

Positive DC-link pin

Pin: P

- This is the DC-link positive power supply pin of the CIPOS™ Mini IPM
- It is connected internally to the collectors of the high-side IGBTs
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin. Typically, metal film capacitors are used

Negative DC-link pins

Pins: NU, NV, NW

- These are the DC-link negative power supply pins (power ground) of the inverter
- These pins are connected to the low-side IGBT emitters of each phase

Inverter power output pins

Pins: U, V, W

- These are the inverter output pins for connecting to the inverter load (e. g. motor)

3.4 Outline drawings

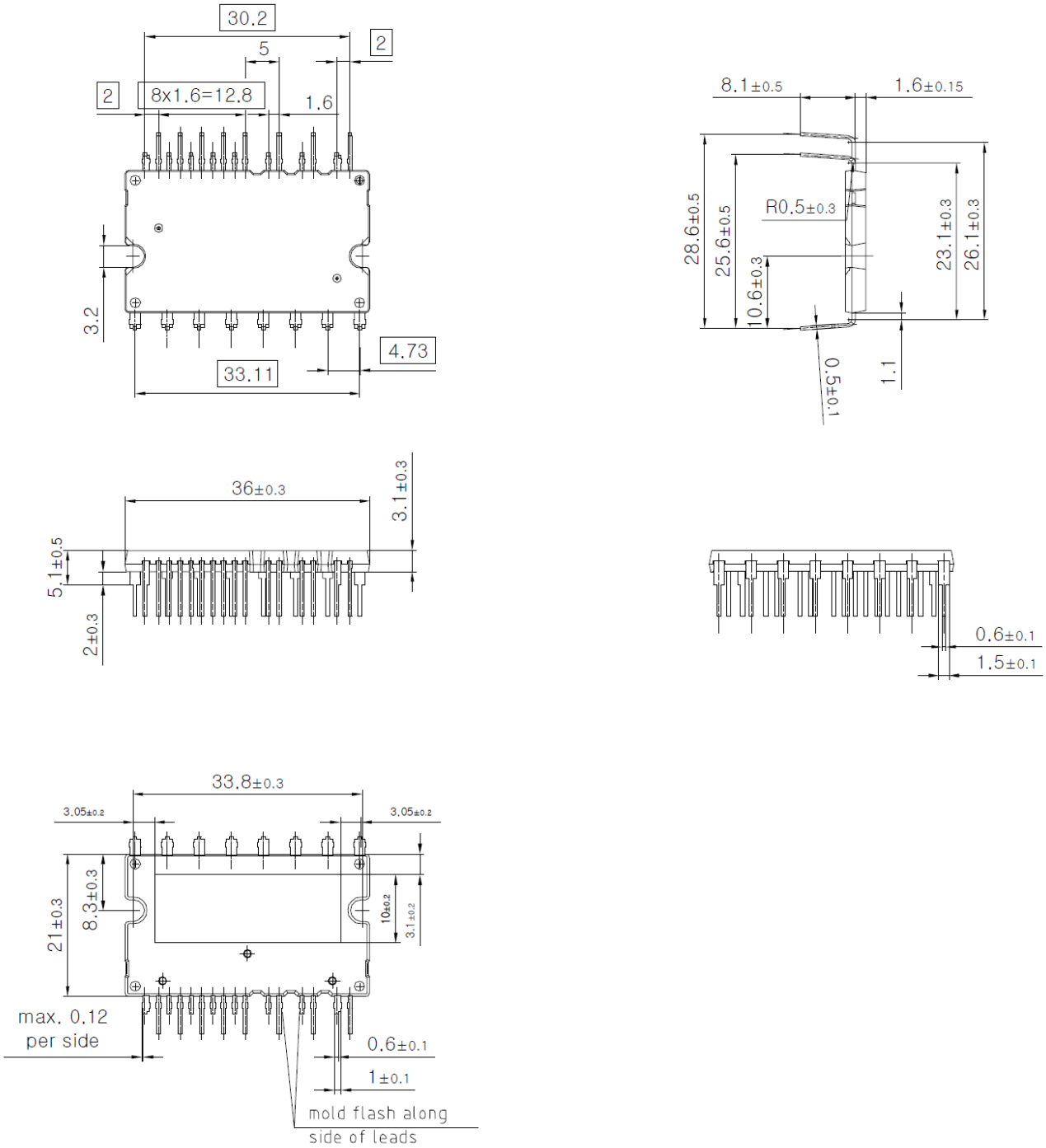


Figure 5 Package outline dimensions of DCB type (unit: mm)

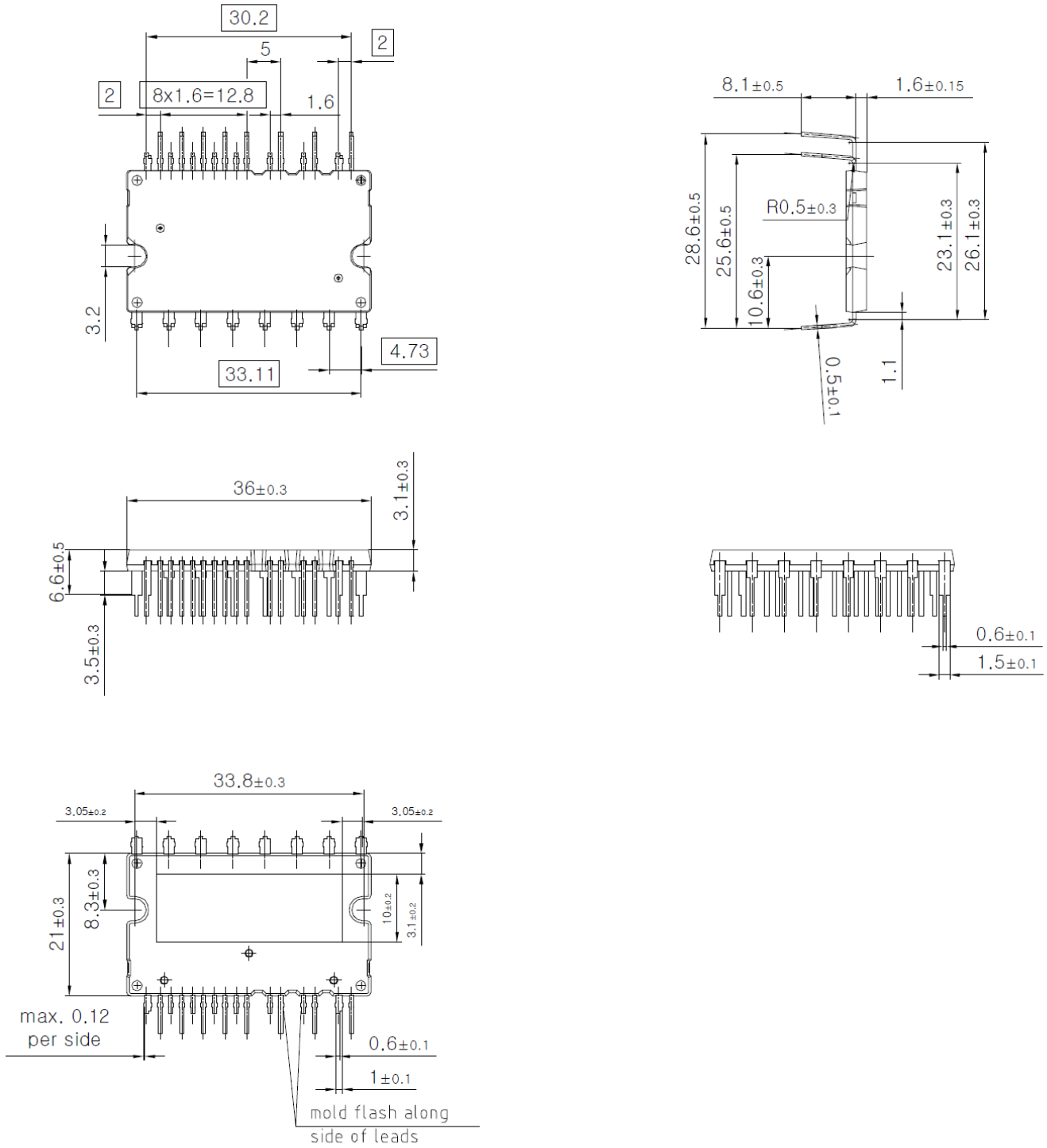


Figure 6 Package outline dimensions of DCB extended stand-off type (unit: mm)

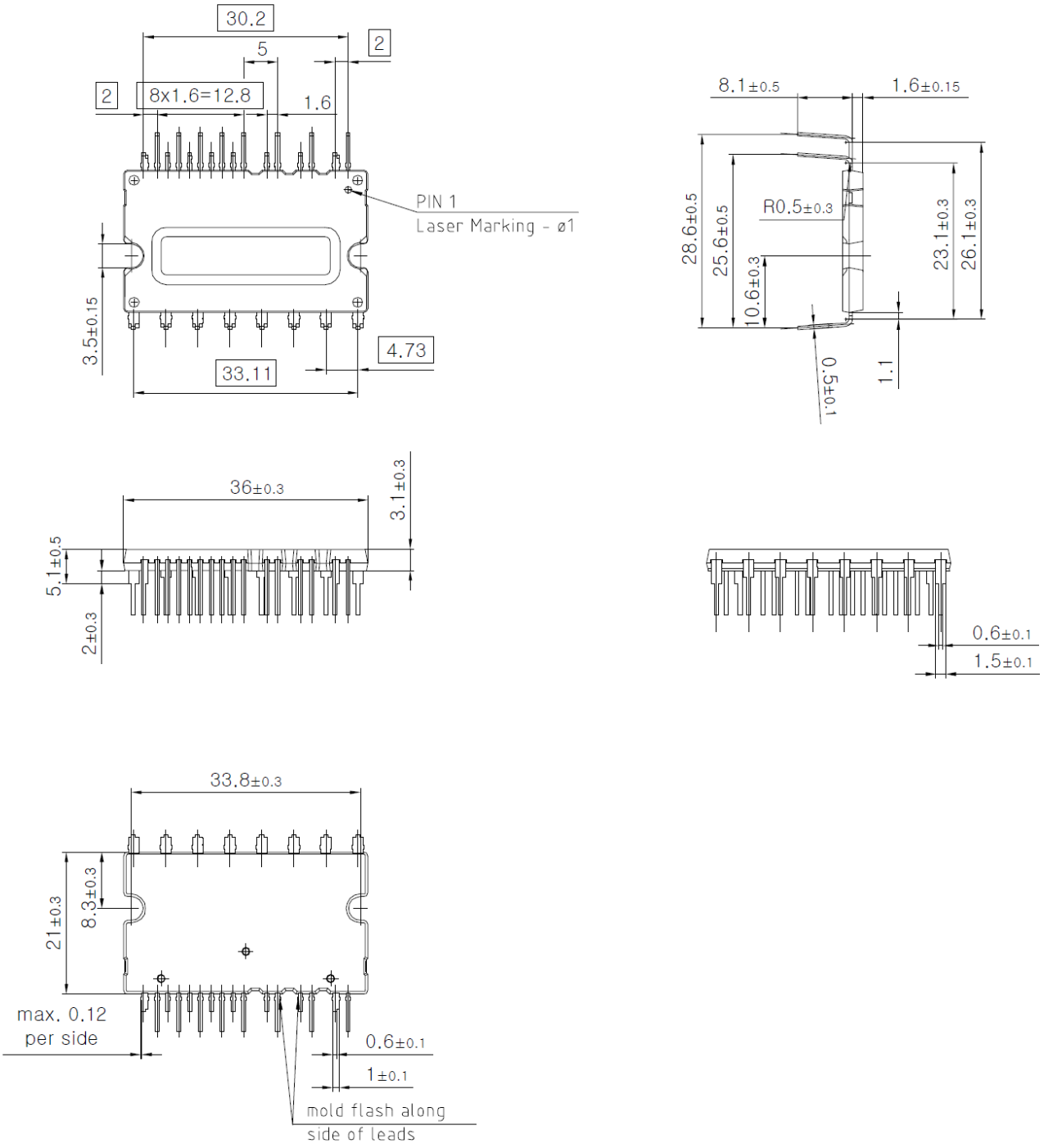


Figure 7 Package outline dimensions of full-pack type (unit: mm)

4 Interface circuit and layout guide

4.1 Input and output signal connection

Figure 8 shows the I/O interface circuit between the microcontroller and the CIPOS™ Mini. The CIPOS™ Mini input logic is active-high with internal pull-down resistors. External pull-down resistors are not needed. V_{FO} output is open-drain configured. This signal should be pulled up to the positive side of 5 V or 3.3 V external logic power supply with a pull-up resistor. The pull-up resistor value should be properly selected, e.g. 3.6 kΩ, considering the internal thermistor between the V_{FO} and V_{SS} pins.

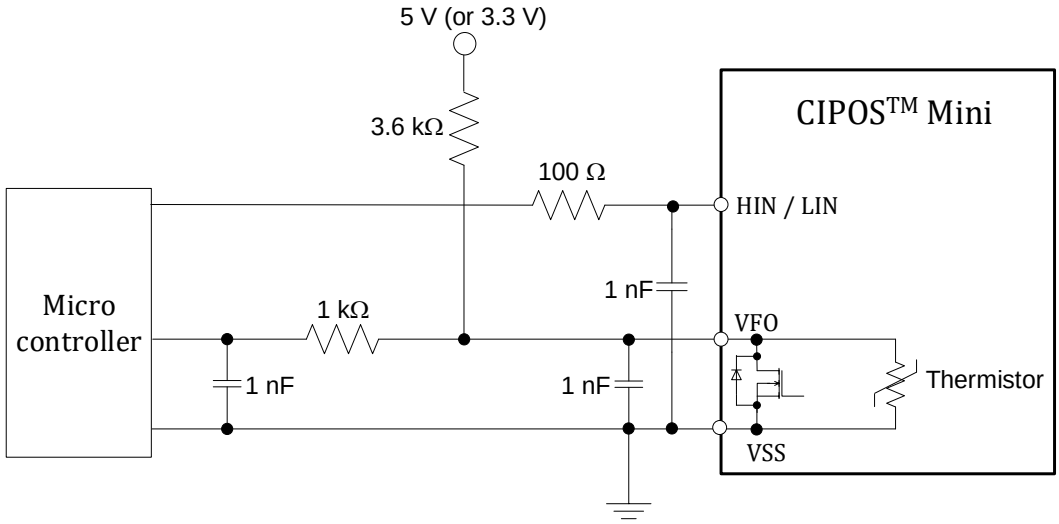


Figure 8 Recommended microcontroller I/O interface circuit

Table 5 Maximum ratings of input and V_{FO} pins

Item	Symbol	Condition	Rating	Unit
Module supply voltage	V_{DD}	Applied between V_{DD} – V_{SS}	20	V
Input voltage	VIN	Applied between HIN(U), HIN(V), HIN(W) – V_{SS} LIN(U), LIN(V), LIN(W) – V_{SS}	-5.5 ~ V_{DD}+0.5	V
Fault output supply voltage	V_{FO}	Applied between V_{FO} – V_{SS}	-0.5 ~ V_{DD}+0.5	V

The maximum rating voltages of input and fault output are listed in Table 5. Since the fault output is open-drain configured and its rating is V_{DD}+0.5 V, a 15 V supply interface is possible. However, it is recommended that the fault output be configured with a 5 V logic supply that is the same as the input signals. It is also recommended to place the bypass capacitors as close as possible to the V_{FO} and signal lines from the microcontroller and to the CIPOS™ Mini.

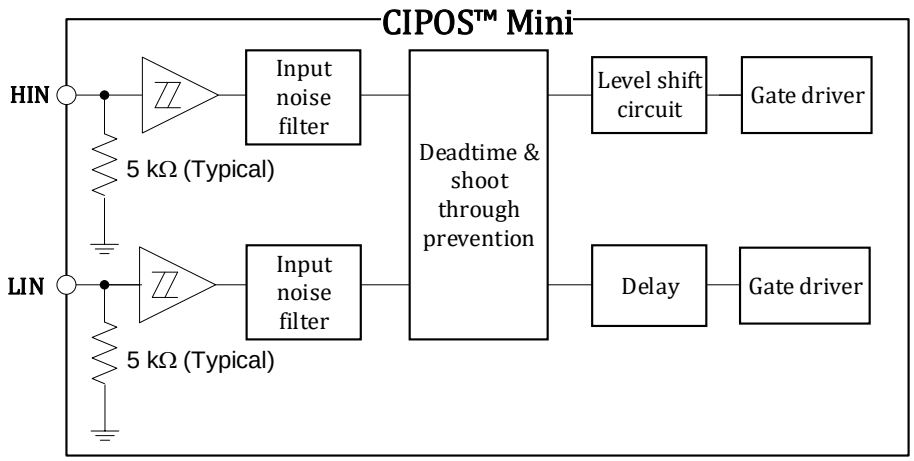


Figure 9 Simplified block diagram of the CIPOS™ Mini control IC

As the CIPOS™ Mini family employs active-high input logic, the power sequence restriction between the control supply and the input signal during start-up or shut-down operation does not exist. This makes the system fail-safe. In addition, pull-down resistors are built into each input circuit eliminating the need for external pull-down resistors. This reduces the required external component count. Input Schmitt triggers, noise filters, deadtime, and shoot-through prevention functions provide beneficial noise rejection to short input pulses. Furthermore, by lowering the turn-on and turn-off threshold voltage of the input signal, as shown in Table 6, a direct connection to a 3.3 V class microcontroller or DSP is possible.

Table 6 Input threshold voltage (at V_{DD} = 15 V, T_J = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic "1" input voltage (LIN, HIN)	V_{IH_TH}	HIN – V_{SS} LIN – V_{SS}	1.7	2.0	2.3	V
Logic "0" input voltage (LIN, HIN)	V_{IL_TH}		0.7	0.9	1.1	V

As shown in Figure 9, the CIPOS™ Mini input signal section integrates a 5 kΩ (typical) pull-down resistor. So, when using an external filtering resistor between the microcontroller output and the CIPOS™ Mini input, the signal voltage drop at the CIPOS™ Mini input terminals must be checked. It should meet the logic "1" input voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown in Figure 8.

4.2 Example of general interface circuit

Figure 10 shows a typical application circuit of the CIPOS™ Mini IPM. In this example, control signals come from the microcontroller directly.

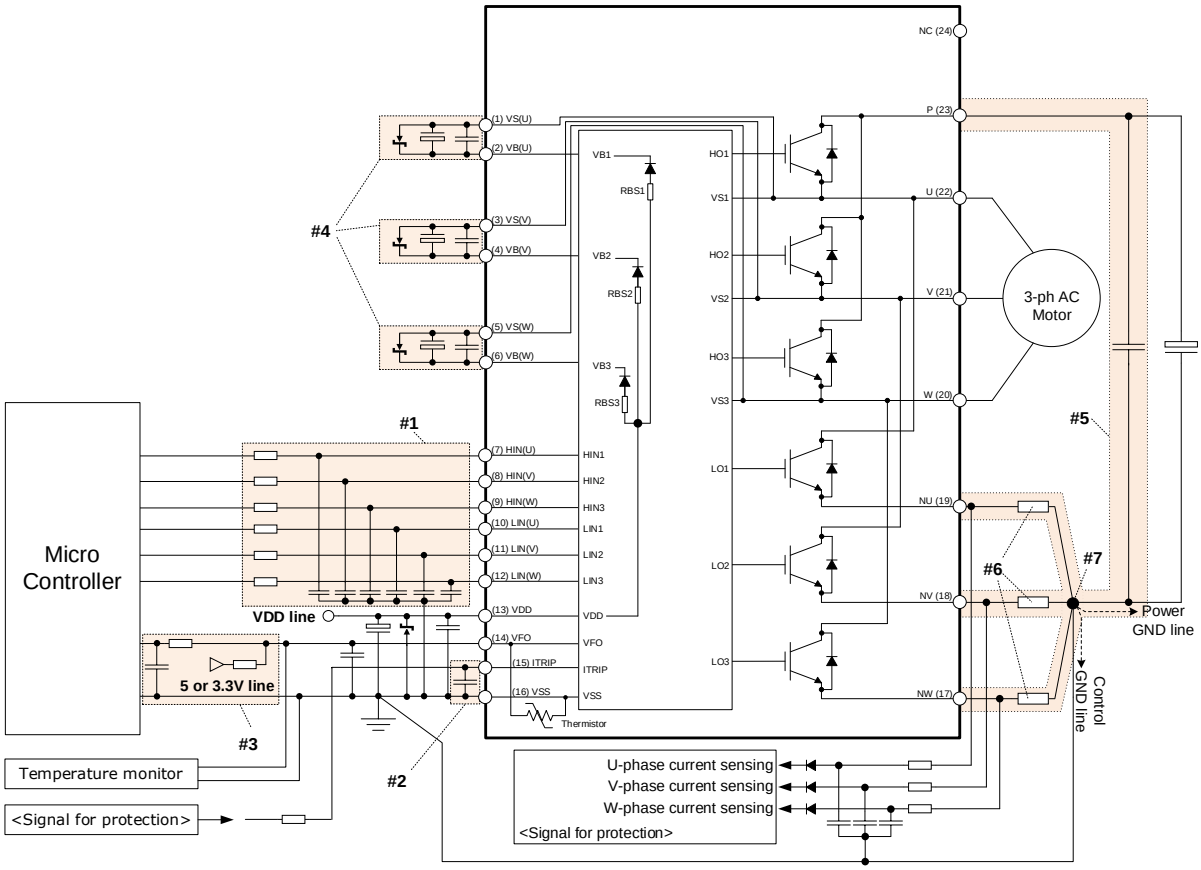


Figure 10 Application circuit example

Please ensure the following for an optimized application circuit design:

- Input circuit
  - To reduce the input signal noise by high-speed switching, an RC filter circuit can be used (e.g. 100 Ω, 1 nF)
  - The filter capacitor should be placed as close to the V_{SS} pin as possible
- ITRIP circuit
  - To prevent protection function errors, an RC filter circuit is recommended
  - The filter capacitor should be placed as close to the ITRIP and V_{SS} pins as possible
- V_{FO} circuit
  - V_{FO} is an open-drain output. This signal line should be pulled up to the positive side of the 5 V/3.3 V logic power supply with a proper resistor
  - It is recommended that the RC filter be placed as close to the controller as possible
- V_B-V_S circuit
  - Capacitors for high-side floating supply voltage should be placed as close to the V_B and V_S pins as possible
  - TVS or Zener diode is recommended for protection from external surge voltage
- Snubber capacitor

- The wiring between the CIPOS™ Mini and the snubber capacitor, including the shunt resistor, should be as short as possible
- Shunt resistor
  - A SMD-type resistor is strongly recommended to minimize stray inductance
- Ground pattern
  - Each ground pattern should be connected at a single point

4.3 Rated output current of control power supply

Control and gate drive power for the CIPOS™ Mini are normally provided by a single 15 V supply that is connected to the module V_{DD} and V_{SS} terminals. The circuit current of V_{DD} control supply of the IM535-U6D/U6DS is listed in Table 7.

Table 7 The circuit current of control power supply

Condition		Current
V_{DD} = 15 V	f_{SW} = 5 kHz	7.9 mA
	f_{SW} = 20 kHz	25.4 mA

The circuit current of the 5 V logic power supply (V_{FO} and input terminals) is about 20 mA.

Finally, the recommended minimum circuit current of the power supply is listed in Table 8. This is the considered ripple current with sufficient margins for the worst conditions, e.g. 5 times higher than the calculated value. Therefore, all IM535/IM523 series IPM products can refer to the values in Table 8.

Table 8 The recommended minimum circuit current of control power supply

Item	The circuit current of +15 V control supply	The circuit current of +5 V logic supply
$V_{DD} \leq 17.5$ V, $f_{SW} \leq 20$ kHz	130 mA	45 mA

4.4 Layout for overcurrent protection (OCP) and short-circuit protection (SCP) function

It is recommended that the ITRIP filter capacitor connections to the CIPOS™ Mini pins be as short as possible. The ITRIP filter capacitor should be connected to the V_{SS} pin directly without overlapping ground pattern. The signal ground and power ground should be as short as possible and connected at only one point by the filter capacitor of the V_{DD} line.

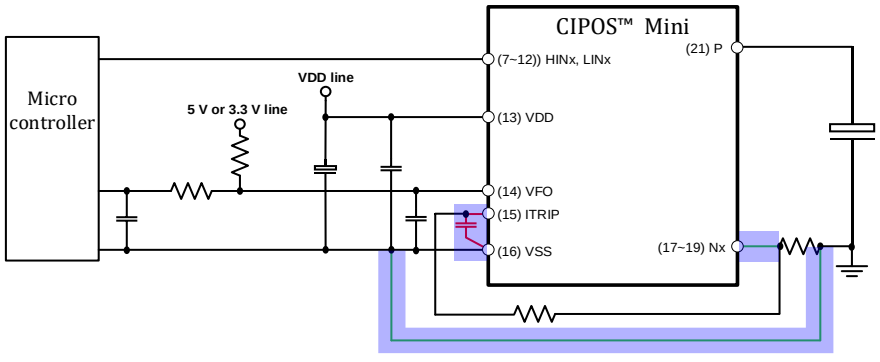


Figure 11 Recommended layout for the OCP and SCP functions

4.5 Shunt resistor and snubber capacitor location

An external current sensing resistor is used to detect overcurrent of phase currents. A long pattern between the shunt resistor and the CIPOS™ Mini will cause excessive surges that might damage the CIPOS™ Mini's internal IC and current detection components. The long pattern may also distort the sensing signal. To decrease the pattern inductance, the connection between the shunt resistor and CIPOS™ Mini should be as short as possible. As shown in Figure 12, the snubber capacitor should be placed in such a way as to suppress surge voltages effectively. Generally a high-frequency, non-inductive capacitor of around 0.1 ~ 0.22 µF is recommended. If the snubber capacitor placement is not correct, e.g. at location '1' in Figure 12, the snubber capacitor will not be able to suppress the surge voltage effectively. If the capacitor is placed at location '2,' the charging and discharging currents generated by the parasitic inductance and the snubber capacitor will appear on the shunt resistor. This will impact the current-sensing signal, and the short-circuit protection level will be lower than the calculated design value. Although the surge-suppression effect is better at location '2' than at location '3,' '3' is a reasonable compromise with better suppression without impacting the current-sensing signal accuracy. Therefore, location '3' is generally used.

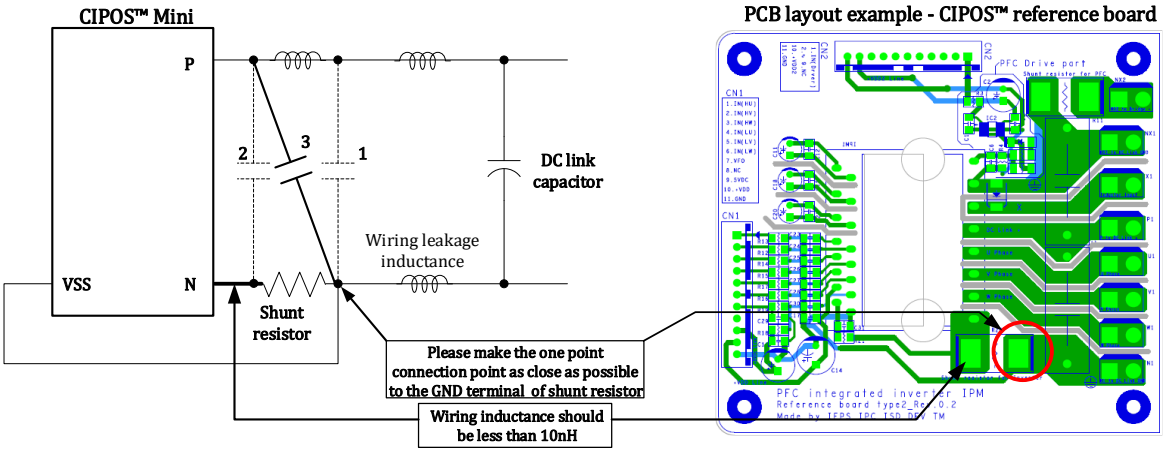


Figure 12 Recommended location of the shunt resistor and snubber capacitor

4.6 Pin and screw hole coordinates

Figure 13 shows the position of the CIPOS™ Mini package on the PCB to indicate center coordinates of each pin and screw hole listed in Table 9.

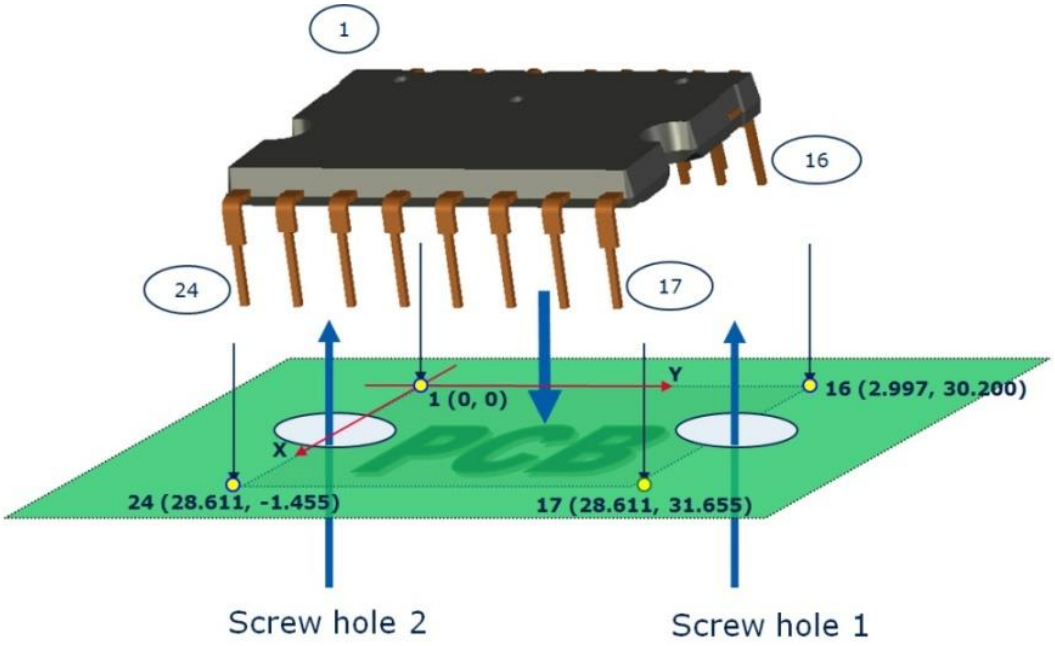


Figure 13 CIPOS™ Mini package position on PCB (unit: [mm])

Table 9 Pin and screw hole coordinates for CIPOS™ Mini package footprint (unit: [mm])

Pin number		X	Y	Pin number		X	Y
Signal pins	1	0.000	0.000	Signal pins	14	2.997	26.600
	2	2.997	2.000		15	0.000	28.200
	3	0.000	5.400		16	2.997	30.200
	4	2.997	7.000	Power pins	17	28.611	31.655
	5	0.000	10.400		18	28.611	26.925
	6	2.997	12.000		19	28.611	22.195
	7	0.000	15.400		20	28.611	17.465
	8	2.997	17.000		21	28.611	12.735
	9	0.000	18.600		22	28.611	8.005
	10	2.997	20.200		23	28.611	3.275
	11	0.000	21.800		24	28.611	-1.455
	12	2.997	23.400	Screw holes	25	17.950	32.000
	13	0.000	25.000		26	17.950	-1.800

5 Protection features

5.1 Undervoltage protection

Control and gate drive power for the CIPOS™ Mini are normally provided by a single 15 V supply that is connected to the module V_{DD} and V_{SS} terminals. For proper operation, this voltage should be regulated to 15 V ± 10%. Table 10 lists the behavior of the CIPOS™ Mini for various control supply voltages. The control supply should be well filtered with a low impedance electrolytic capacitor and a high-frequency decoupling capacitor connected at the CIPOS™ Mini's pins.

High-frequency noise on the supply might cause the internal control IC to malfunction and generate erroneous fault signals. To avoid these problems, the maximum ripple on the supply should be less than ± 1 V/µs.

The potential at the V_{SS} terminal is not the same as that at the N terminal due to the voltage drop across the current sensing resistor. It is important that all control circuits and power supplies be, therefore, referred to the V_{SS} terminal, and not to the N terminal. If the circuits are connected improperly, the additional current flowing through the sense resistor might cause the short-circuit protection function to malfunction. In general, the best practice is to make the common reference (V_{SS}) a ground plane in the PCB layout.

The main control power supply is also connected to the bootstrap circuits to generate floating supplies for the high-side gate drives.

When control supply voltage (V_{DD} and V_{BS}) falls below the UVLO level, the IGBT will turn off ignoring the input signal.

Table 10 CIPOS™ Mini functions versus control power supply voltage

Control voltage range [V]	CIPOS™ Mini function operations
0 ~ 13.1	As the UVLO function is activated, control input signals are blocked and a fault signal V_{FO} is generated
13.1 ~ 17.5	Normal operation. This is the recommended operating condition. V_{DD} of 14.5 ~ 17 V is recommended when only integrated bootstrap circuitry is used
17.5 ~ 20	As the driving voltage is above the recommended range, the IGBT's switching is faster. This causes increased system noise and peak short-circuit current might be too large for proper operation of the short-circuit protection. Operation in this V_{DD} range is not recommended
Over 20	Control circuit in the CIPOS™ Mini might be damaged

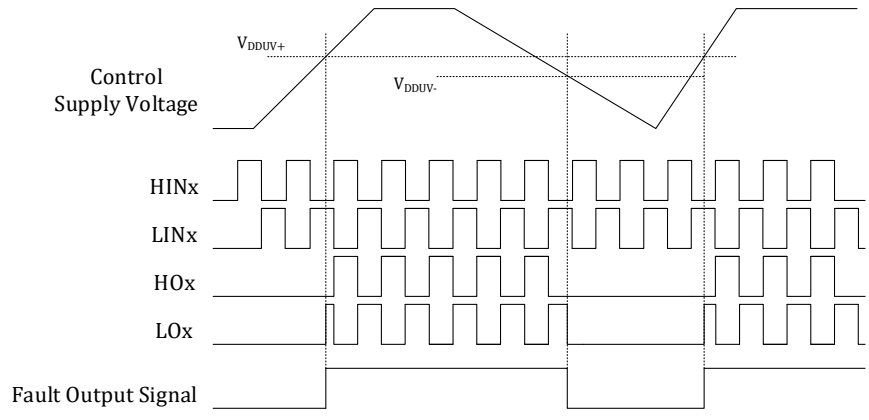


Figure 14 Timing chart of low-side UVLO protection function

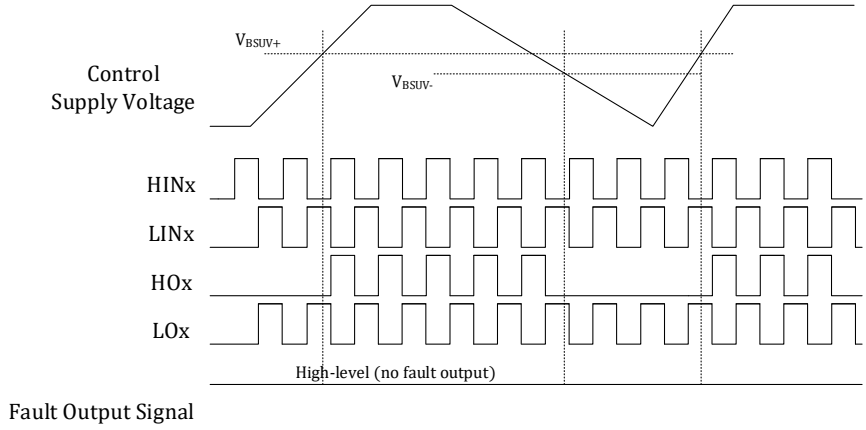


Figure 15 Timing chart of high-side UVLO protection function

5.2 Overcurrent protection

5.2.1 Timing chart of overcurrent (OC) protection

The CIPOS™ Mini has an overcurrent shutdown function. Its internal IC monitors the voltage of the ITRIP pin, and if this voltage exceeds the $V_{IT,TH+}$ specified in the device's datasheet, a fault signal is activated and all IGBTs are turned off. Typically, the maximum short-circuit current magnitude is dependent on the gate-voltage – a higher gate voltage results in a higher short-circuit current. To avoid this potential problem, the maximum overcurrent trip level is generally set two times below the nominal rated collector current. The overcurrent protection timing chart is shown in Figure 16.

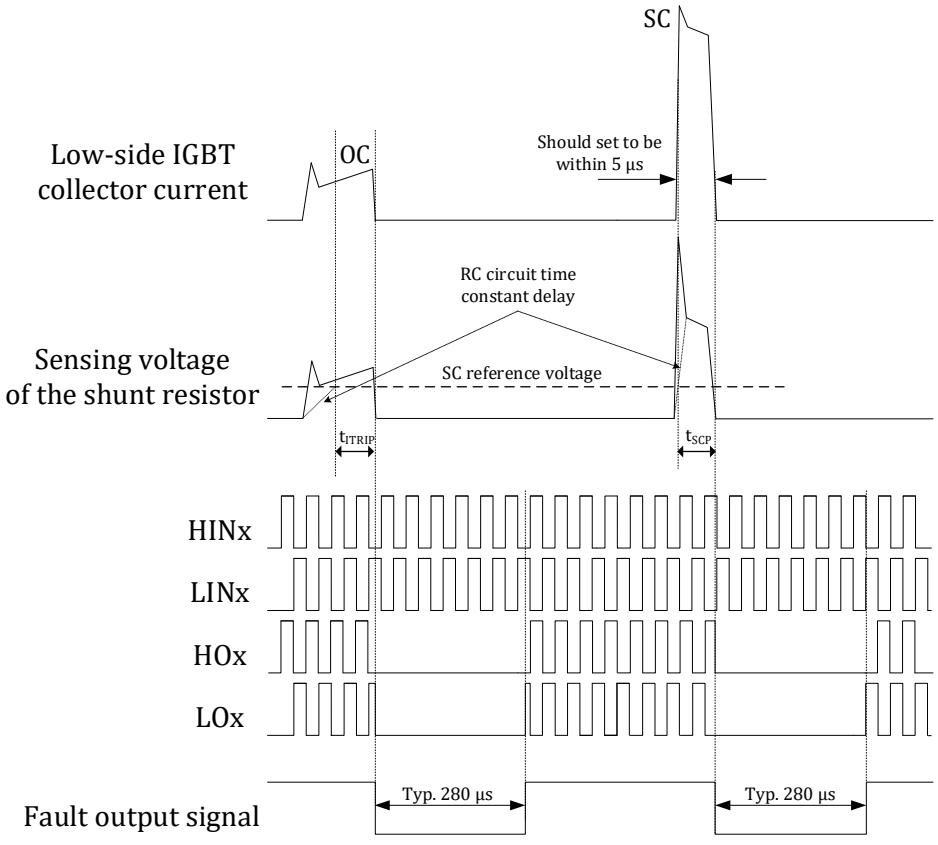


Figure 16 Timing chart of the overcurrent protection function

5.2.2 Selecting current-sensing shunt resistor

The value of the current-sensing resistor is calculated by the following equation:

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}} \quad (1)$$

Where $V_{IT,TH+}$ is the ITRIP positive-going threshold voltage of the CIPOS™ Mini. It is typically 0.525 V. I_{OC} is the current at overcurrent detection level.

The maximum value of the overcurrent protection level should be set lower than the repetitive peak collector current specified in the datasheet keeping in mind the tolerance of the shunt resistor.

For example, the maximum peak collector current of IM535-U6D is 60 A_{peak} and thus, the recommended value of the shunt resistor is calculated as:

$$R_{SH(min)} = \frac{0.525}{60} = 8.75\ m\Omega$$

For the power rating of a shunt resistor, the following list should be considered:

- Maximum load current of inverter (I_{RMS})
- Shunt resistor value at T_C = 25°C (R_{SH})
- Power derating ratio of shunt resistor at T_{SH} = 100°C according to the manufacturer's datasheet
- Safety margin

The shunt resistor power rating is calculated using the following equation:

$$P_{SH} = \frac{I_{RMS}^2 \times R_{SH} \times margin}{derating\ ratio} \quad (2)$$

An example in the case of IM535-U6D and R_{SH} = 8.75 mΩ is as follows:

- Max. load current of the inverter: 16 A_{RMS}
- Derating of shunt resistor power at T_{SH} = 100°C: 80%
- Safety margin: 30%

$$P_{SH} = \frac{16^2 \times 0.00875 \times 1.3}{0.8} = 3.64\ W$$

A proper power rating of the shunt resistor is over 3.64 W, e.g. 4 W.

Please note that resistance and power rating higher than the minimum value should be chosen considering the overcurrent protection level required in the application.

5.2.3 Delay time

An RC filter is necessary in the overcurrent sensing circuit to prevent the malfunction of overcurrent protection caused by noise. The RC time constant is determined by considering the noise duration and short-circuit withstand time of the IGBT. When the sensing voltage on the shunt resistor exceeds the ITRIP positive-going threshold ($V_{IT,TH+}$), this voltage is applied to the ITRIP pin of CIPOS™ Mini through the RC filter. Table 11 lists the specification of the overcurrent protection reference level. There is a delay time (t_{FILTER}) caused by the filter, and it can be calculated using equation (3) and (4):

$$V_{IT,TH+} = R_{SH} \cdot I_C \cdot \left(1 - \frac{1}{e^{\frac{t_{Filter}}{\tau}}}\right) \quad (3)$$

$$t_{Filter} = -\tau \cdot \ln(1 - \frac{V_{IT,TH+}}{R_{SH} \cdot I_C}) \quad (4)$$

Where, $V_{IT,TH+}$ is the ITRIP pin input voltage, I_C is the peak current, R_{SH} is the shunt resistor value, and τ is the RC time constant. In addition, there is a short-circuit propagation delay (t_{SCP}). Please refer to Table 12.

Table 11 Specification of OC protection reference level '$V_{IT,TH+}$'

Item	Min.	Typ.	Max.	Unit
ITRIP positive-going threshold $V_{IT,TH+}$	0.475	0.525	0.57	V

Table 12 Internal delay time of OC protection circuit

Item	Device	Condition	Min.	Typ.	Max.	Unit
Short-circuit propagation delay time (t_{SCP})	IM535-U6D	from $V_{IT,TH+}$ to 10% I_{SC}	-	1550	-	ns
	IM535-U6DS		-	1550	-	
	IM523-S6A		-	1150	-	
	IM523-M6A		-	1150	-	
	IM523-L6A		-	1150	-	
	IM523-X6A		-	1150	-	

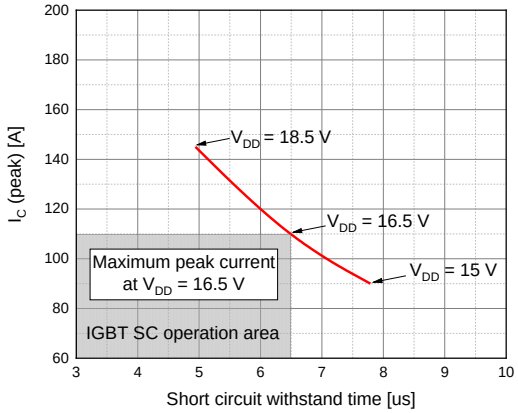
Therefore, the total delay becomes:

$$t_{Total} = t_{Filter} + t_{SCP} \quad (5)$$

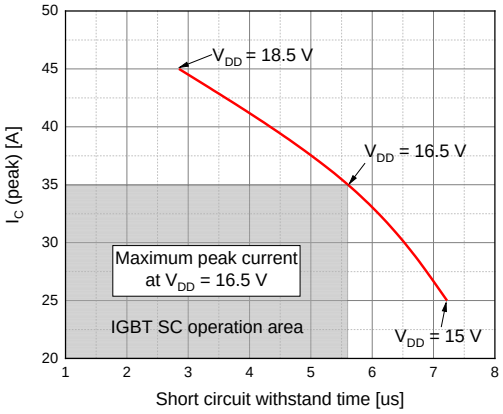
The total delay must be less than the short-circuit withstand time (t_{SC}) given in the datasheet. Since the t_{SC} varies with the control supply voltage or DC-link voltage, it is recommended that the RC time constant be set with a margin.

5.2.4 Short-circuit safe operating area

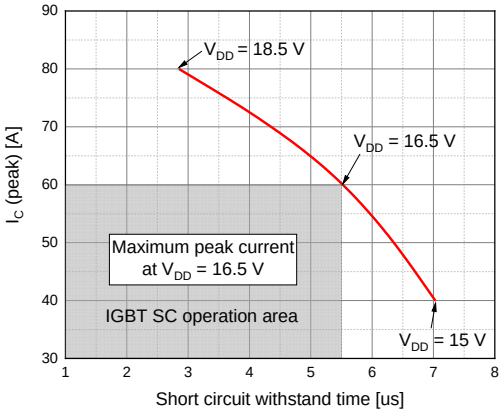
Figure 17 shows a typical short-circuit safe operating area (SCSOA) of the IGBT used in CIPOS™ Mini with conditions – V_{PN} = 400 V, non-repetitive, $V_{PN(surge)}$ < 600 V, starting T_J = 150°C. Under a control supply voltage of 16.5 V, the IGBT in IM535-U6D can be turned off safely if the short-circuit condition lasts less than 6.5 µs, and the typical short-circuit current is about 110 A peak. This, however, does not mean that the IPM or IGBT will fail if short-circuit current is higher than 110 A. Depending on the lot, the short-circuit current varies by V_{TH} or transconductance of the IGBT even with a fixed V_{DD}.



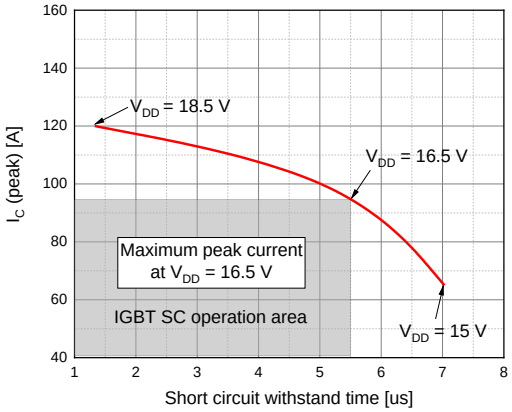
(a) Typical SCSOA curve of IM535-U6D/U6DS



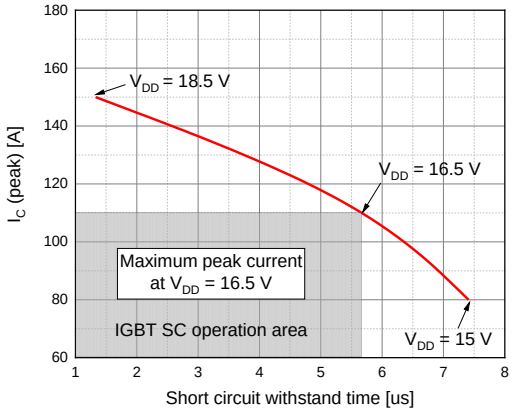
(b) Typical SCSOA curve of IM523-S6A



(c) Typical SCSOA curve of IM523-M6A



(d) Typical SCSOA curve of IM523-L6A



(e) Typical SCSOA curve of IM523-X6A

Figure 17 Typical SCSOA curve

5.3 Fault output circuit

Table 13 Fault output maximum ratings

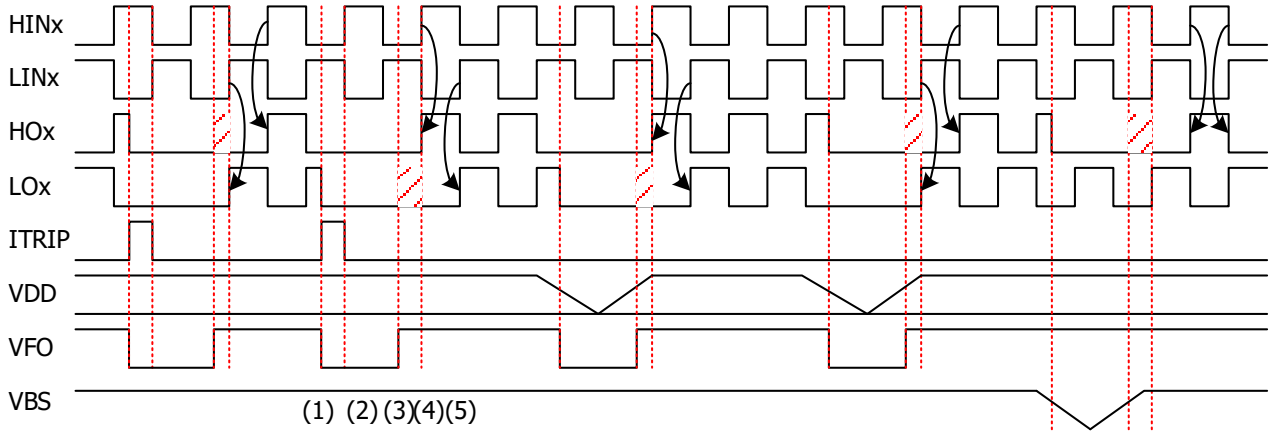
Item	Symbol	Condition	Rating	Unit
Fault output supply voltage	V_{FO}	Applied between V_{FO}-V_{SS}	-0.5 ~ V_{DD} + 0.5	V
Fault output current	I_{FO}	Sink current at V_{FO} pin	10	mA

Table 14 Electric characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output current	I_{FO}	V_{ITRIP} = 0 V, V_{FO} = 5 V	-	60	-	µA
Fault output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.35	-	V

As the V_{FO} terminal is an open-drain type, it must be pulled up to a high level using a pull-up resistor. The resistor must be calculated according to the specifications mentioned in Table 13 and Table 14.

The sleep function is activated after each trigger of ITRIP or UVLO. A new edge of each individual control input signal is required to activate the corresponding output after fault-clear time as shown in Figure 18.



(1) Overcurrent is detected through the ITRIP pin and a fault output is activated

(2) All LOx and HOx are turned off by protection

(3) The fault output is cleared, but LOx is still off due to the sleep function even though LINx is high

(4) A new edge of HINx is detected and HOx is activated

(5) LOx is activated by a new edge of LINx

Figure 18 Sleep function timing diagram

5.4 Overtemperature protection

CIPOS™ Mini has one pin for both fault output and temperature sensing. Figure 19 shows the internal thermistor resistance characteristics as a function of the thermistor temperature. A circuitry is introduced in this section for over-temperature protection. As shown in Figure 20, the V_{FO} pin is connected directly to the analog-to-digital converter (ADC) and fault detection terminals of the microcontroller. This circuit is very simple and allows the IGBTs to be shut down by the microcontroller. For example, as shown in Figure 21, when R1 is 3.6 kΩ and the thermistor temperature is 100°C, the V_{FO} is 2.95 V at V_{ctr} = 5 V or 1.95 V at V_{ctr} = 3.3 V. Note that the V_{FO} for overtemperature protection should not be less than the fault trip level of the microcontroller.

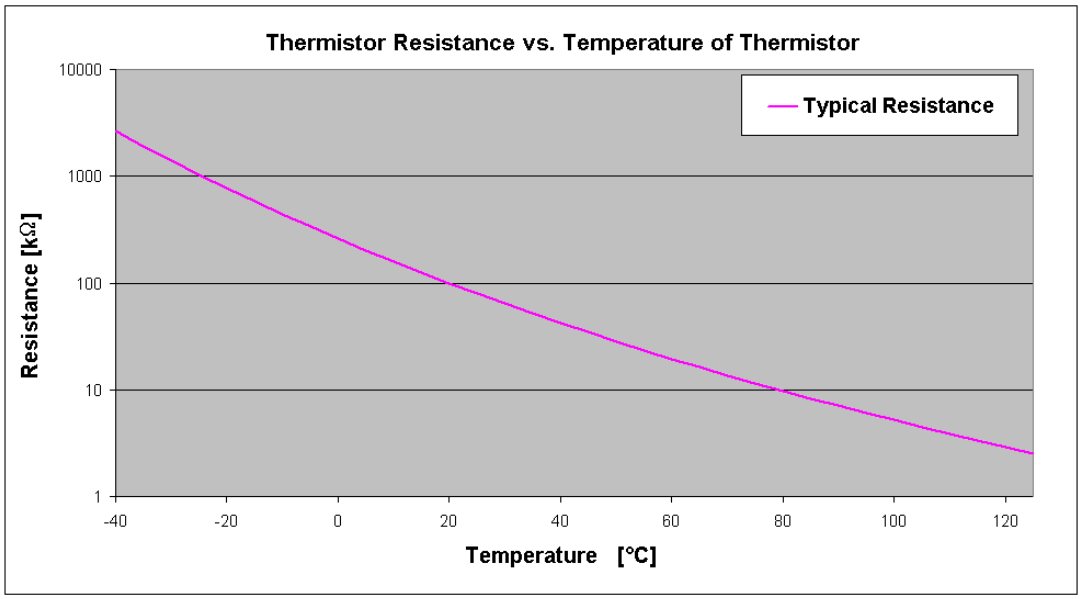


Figure 19 Internal thermistor resistance as a function of thermistor temperature

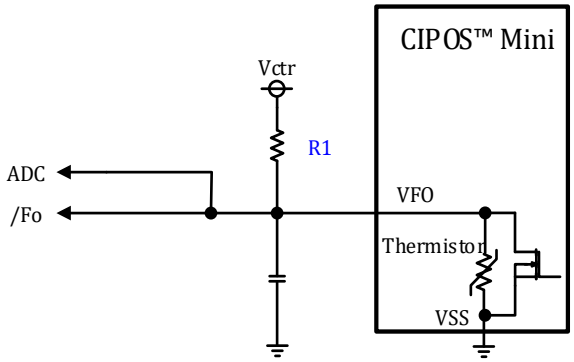


Figure 20 Circuit proposals for over-temperature protection

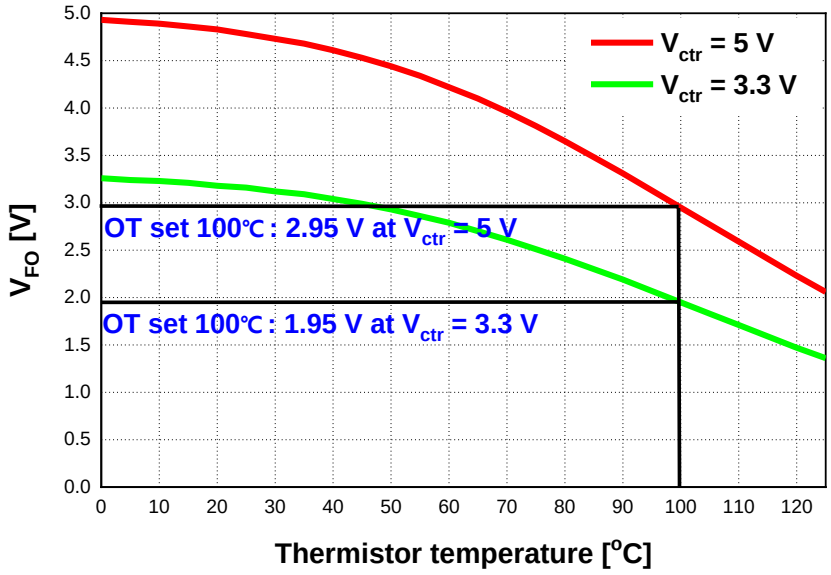


Figure 21 Voltage of the V_{FO} pin according to the thermistor temperature

6 Bootstrap circuit

6.1 Bootstrap circuit operation

The V_{BS} voltage, which is the voltage difference between $V_{B\,(U,V,W)}$ and $V_{S\,(U,V,W)}$, provides the supply to the IC within the CIPOS™ Mini. This supply voltage must be in the range of 13.0~17.5 V to ensure that the IC can fully drive the high-side IGBT. The CIPOS™ Mini includes an undervoltage detection function for the V_{BS} to ensure that the IC does not drive the high-side IGBT when the V_{BS} voltage drops below a specified voltage (refer to the datasheet). This function prevents the IGBT from operating with a high power dissipation. Please note that the UVLO function of any high-side section acts only on the triggered channel without any feedback to the control level.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and cheap. However, the duty cycle and on-time duration are limited by the requirement to refresh the charge in the bootstrap capacitor. Figure 22 shows the bootstrap supply, which is formed by a combination of diode, resistor and capacitor, and the current path of the bootstrap circuit. When V_S is pulled down to ground (e.g. through the low side or the load), the bootstrap capacitor (C_{BS}) is charged by the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

6.2 Internal bootstrap functionality characteristics

CIPOS™ Mini includes the bootstrap functionality in the internal driver IC that consists of three diodes and three resistors, as shown in Figure 3. The typical value of an internal bootstrap resistor is 37 Ω at room temperature. For more information, please refer to Table 15.

V_{DD} of 16 V is recommended when only the integrated bootstrap circuitry is used.

Table 15 Electric characteristics of internal bootstrap parameters

Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Repetitive peak reverse voltage		V_{RRM}	600	-	-	V
Bootstrap diode forward current between V_{DD} and V_B	V_F = 4 V	I_{F_BSD}	-	54	-	mA
Bootstrap diode resistance	V_{F1} = 4 V, V_{F2} = 5 V	R_{BSD}	-	37	-	Ω
Bootstrap diode forward voltage between V_{DD} and V_B	I_F = 0.3 mA	V_{F_BSD}	-	1.0	-	V

If it is necessary to reduce the bootstrap resistance, an external bootstrap circuitry is recommended. For example, when a 39 Ω resistor and the 1N4937 diode are connected externally to the CIPOS™ Mini, the bootstrap resistance is around 23 Ω, as shown in Table 16.

Table 16 Bootstrap resistance with external bootstrap circuitry (39 Ω and 1N4937)

Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Bootstrap resistance	T_J = 25°C T_J = 125°C	R_{BS}	-	22.9 26.5	-	Ω

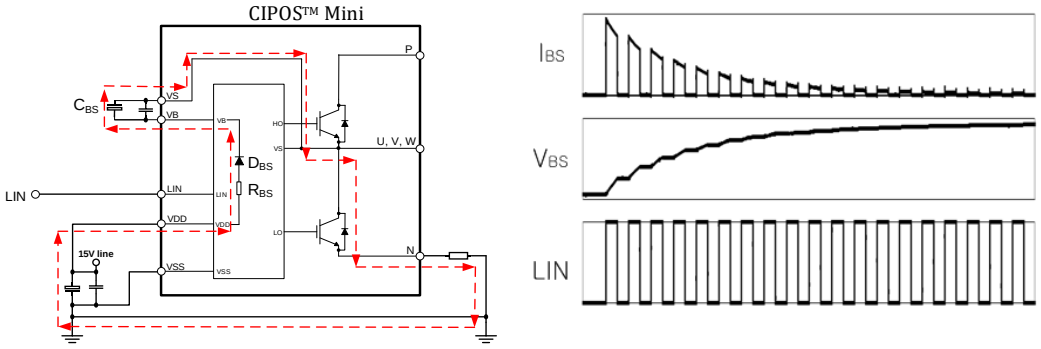
6.3 Initial charging of a bootstrap capacitor

Adequate on-time duration of the low-side IGBT is required to fully charge the bootstrap capacitor for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} \geq C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln\left(\frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_{FD} - V_{LS}}\right) \quad (6)$$

Where,

- V_{FD} = Forward-voltage drop across the bootstrap diode
- $V_{BS(min)}$ = The minimum value of the bootstrap capacitor voltage
- V_{LS} = Voltage drop across the low-side IGBT
- δ = Duty ratio of pulse width modulation (PWM)



(a) Bootstrap circuit (b) Timing chart of initial bootstrap charging

Figure 22 Bootstrap circuit operation and initial charging

6.4 Bootstrap capacitor selection

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V} \quad (7)$$

Where,

- Δt = maximum on-pulse width of high-side IGBT
- ΔV = the allowable discharge voltage of the C_{BS}
- I_{leak} = maximum discharge current of the C_{BS} mainly by the following mechanisms:
  - Gate charge for turning on the high-side IGBT
  - Quiescent current to the high-side circuit in the IC
  - Level-shift charge required by level-shifters in the IC
  - Leakage current in the bootstrap diode
  - C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
  - Bootstrap diode reverse recovery charge

In practice, leakage current of 1 mA is recommended as a calculation basis for the CIPOS™ Mini. Taking into consideration dispersion and reliability, the selected capacitance must generally be two to three times higher than the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, inherently, there is a minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

The bootstrap capacitor should always be placed as close to the pins of the CIPOS™ Mini as possible. At least one low ESR capacitor should be used to provide good local de-coupling. For example, a separate ceramic

capacitor close to the CIPOS™ Mini is essential if an electrolytic capacitor is used for the bootstrap capacitor. If the bootstrap capacitor is either a ceramic or tantalum type, it should be adequate for local de-coupling.

6.5 Charging and discharging of the bootstrap capacitor during PWM inverter operation

The bootstrap capacitor C_{BS} charges through the bootstrap diode D_{BS} and the resistor R_{BS}, as seen in Figure 22, from the V_{DD} supply when the high-side IGBT is off, and the V_S voltage is pulled down to ground. It discharges when the high-side IGBT or diode are on.

Example 1: Selection of the initial charging time

An example of the calculation of the minimum value of the initial charging time is given with reference to equation (6).

Conditions:

- C_{BS} = 4.7 µF, R_{BS} = 37 Ω, duty ratio (δ) = 0.5, D_{BS} = internal bootstrap diode, V_{DD} = 15 V, V_{FD} = 1.0 V
- $V_{BS\,(min)}$ = 13 V, V_{LS} = 0.1 V

$$t_{charge} \geq 4.7\ \mu F \times 37\ \Omega \times \frac{1}{0.5} \times \ln\left(\frac{15\ V}{15\ V - 13\ V - 1\ V - 0.1\ V}\right) \cong 0.98\ ms$$

To ensure safety, it is recommended that the charging time is at least three times longer than the calculated value.

Example 2: The minimum value of the bootstrap capacitor

Conditions:

- ΔV = 0.1 V, I_{leak} = 1 mA

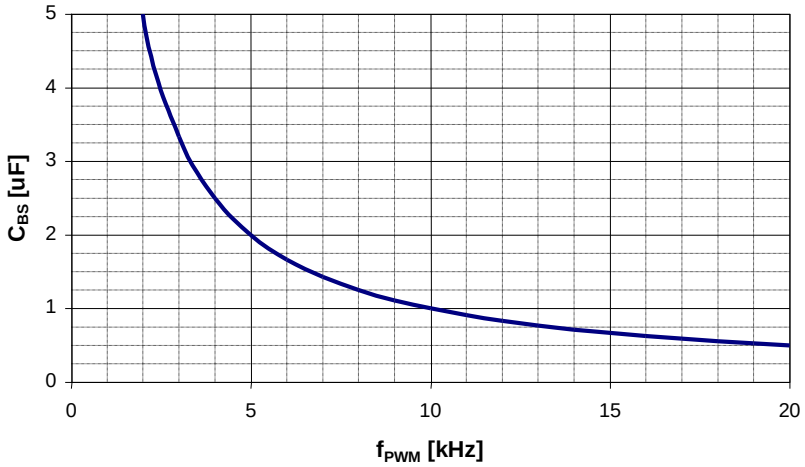


Figure 23 Bootstrap capacitance as a function of the switching frequency

Figure 23 shows the curve corresponding to equation (7) for a continuous sinusoidal modulation, if the voltage ripple ΔV_{BS} is 0.1 V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is, therefore, in the range of up to 4.7 µF for most switching frequencies. In other PWM cases such as discontinuous sinusoidal modulation, the t_{charge} must be set at the longest off period of the low-side IGBT. Please note that this result is only an example. It is recommended that the system design is done based on actual control pattern and lifetime of the components.

7 Thermal system design

7.1 Introduction

The thermal design of a system is key for CIPOS™ Mini IPM in electronic systems such as drives. To avoid overheating and/or to increase reliability, two design criteria are important:

- Low power losses
- Low thermal resistance from junction to ambient

The first criterion is fulfilled when the CIPOS™ Mini family is selected as the IPM for the application. To get the most out of the system, choosing a proper heat sink is necessary. A good thermal design enables users to either maximize the power or to increase the reliability of the system by reducing the maximum temperature. This chapter provides a short introduction on power losses and heat sinks, helping users understand the mode of operation and to find the right heat sink for any specific application.

The following are required for the thermal design:

- The maximum power losses $P_{sw,i}$ of each power switch
- The maximum junction temperature $T_{J,max}$ of the power semiconductors
- The junction-to-ambient transient thermal response $Z_{th,J-A}$. For stationary considerations, the static thermal resistance $R_{th,J-A}$ is sufficient. This thermal resistance comprises the junction-to-case thermal resistance $R_{th,J-C}$ as provided in the datasheets, the case-to-heat sink thermal resistance $R_{th,C-HS}$ accounting for the heat flow through the thermal interface material between the heat sink and the power module, and the heat sink-to-ambient thermal resistance $R_{th,HS-A}$. Each thermal resistance can be extended to its corresponding thermal impedance by adding the thermal capacitances
- The maximum allowable ambient temperature $T_{A,max}$

Furthermore, all heat flow paths need to be identified. Figure 24 shows a typical, simplified, equivalent circuit for the thermal network of CIPOS™ Mini IPM. This circuit is simplified as it omits thermal capacitances and typically negligible heat paths such as the heat transfer from the module surface directly to the ambient via convection and radiation.

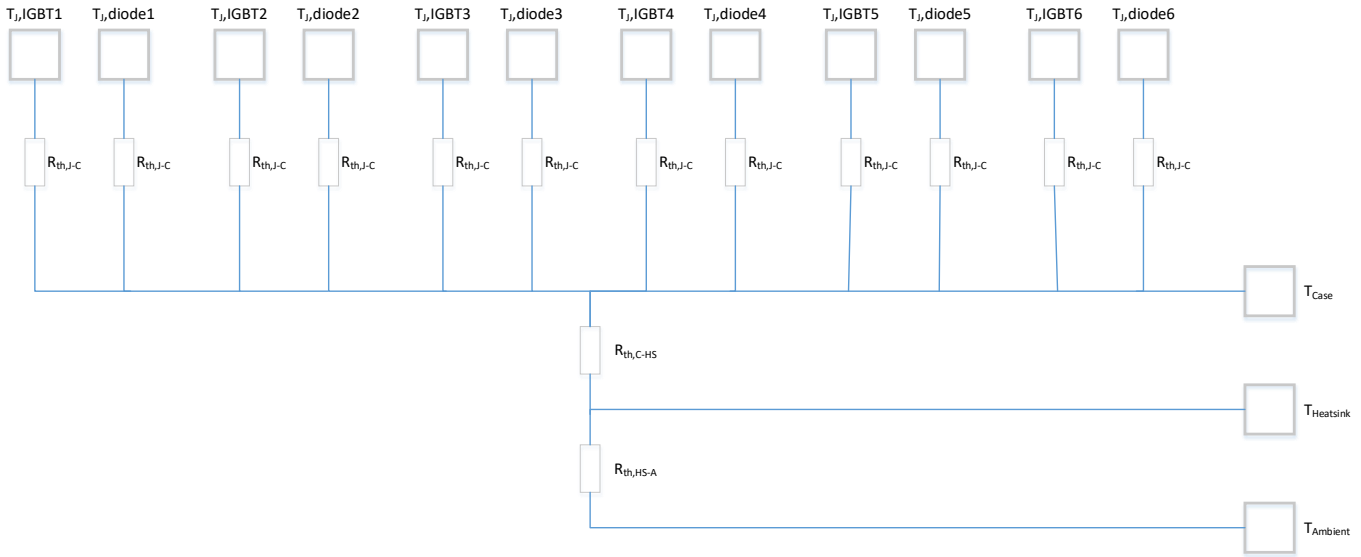


Figure 24 Simplified thermal equivalent circuit

7.2 Power losses

The power losses the CIPOS™ Mini IPM are composed of conduction and switching losses in the IGBTs and diodes. The loss during the turn-off steady state can be ignored because it is very low and has little effect on increasing the temperature in the device. The conduction loss depends on the DC electrical characteristics of the device, i.e. saturation voltage. Therefore, it is a function of the conduction current and the device's junction temperature. On the other hand, the switching loss is determined by dynamic characteristics such as turn-on/off time and overvoltage/current. Therefore, to obtain the accurate switching loss, the DC-link voltage of the system, the applied switching frequency, and the power circuit layout should also be considered in addition to current and temperature.

In this chapter, based on a PWM-inverter system for motor-control applications, detailed equations are shown to calculate the losses of the CIPOS™ Mini for a 3-phase continuous sinusoidal PWM. For other cases such as 3-phase discontinuous PWMs, please refer to [5].

7.2.1 Conduction losses

The typical characteristics of forward-drop voltage are approximated by the following linear equation for the IGBT and the diode, respectively. Figure 25 shows an example of a linear approximation of typical output characteristics.

$$V_{IGBT} = V_I + R_I \cdot i$$
$$V_{DIODE} = V_D + R_D \cdot i \qquad (8)$$

- V_I = threshold voltage of IGBT
- V_D = threshold voltage of diode
- R_I = on-state slope resistance of IGBT
- R_D = on-state slope resistance of diode

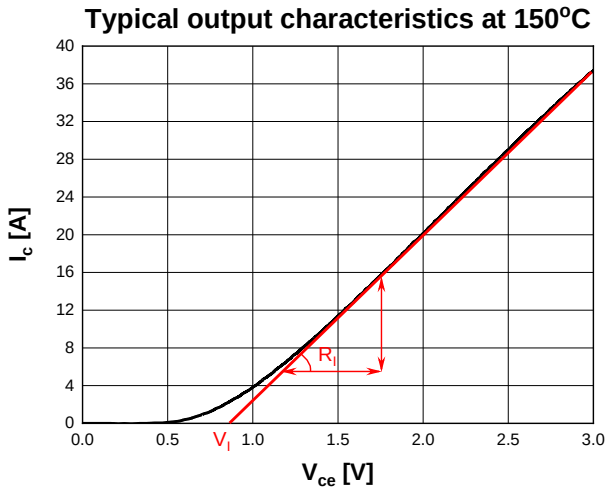


Figure 25 Linear approximation of output characteristics

Assuming that the switching frequency is high, the output current of the PWM inverter can be assumed to be sinusoidal. That is,

$$i = I_{peak}\cos(\theta - \varphi) \qquad (9)$$

Where, φ is the phase-angle difference between output voltage and current. Using equations (8) and (9), the conduction loss of one IGBT and its freewheeling diode can be obtained as follows:

$$P_{con.I} = \frac{1}{2\pi}\int_0^{\pi} \xi(V_{IGBT} \times i)d\theta = \frac{I_{peak}}{2\pi}V_I + \frac{I_{peak}}{8}V_I MI\cos\varphi + \frac{I_{peak}^{\ 2}}{8}R_I + \frac{I_{peak}^{\ 2}}{3\pi}R_I MI\cos\varphi \quad (10)$$

$$P_{con.D} = \frac{1}{2\pi}\int_0^{\pi} (1-\xi)(V_{DIODE} \times i)d\theta = \frac{I_{peak}}{2\pi}V_D - \frac{I_{peak}}{8}V_D MI\cos\varphi + \frac{I_{peak}^{\ 2}}{8}R_D - \frac{I_{peak}^{\ 2}}{3\pi}R_D MI\cos\varphi \quad (11)$$

$$P_{con} = P_{con.I} + P_{con.D} \quad (12)$$

Where, ξ is the duty cycle in the given PWM method.

$$\xi = \frac{1 + MI\cos\theta}{2} \quad (13)$$

Where, MI is the PWM modulation index (MI is defined as the peak phase voltage divided by half of the DC-link voltage).

Please note that the total inverter conduction losses are six times that of the P_{con}.

7.2.2 Switching losses

Switching losses vary according to the device technology, the working voltage/current, and the operating temperature/frequency. However, the turn-on/off loss energy (Joule) can be measured indirectly during tests by multiplying the current and voltage and integrating the multiplied value over time, under a given circumstance. Therefore, the linear dependency of the switching energy loss on the switched current is expressed during one switching period as follows:

$$\text{Switching energy loss} = (E_I + E_D) \times i\ [J] \quad (14)$$

$$E_I = E_{I.ON} + E_{I.OFF} \quad (15)$$

$$E_D = E_{D.ON} + E_{D.OFF} \quad (16)$$

Where, E_I is the switching loss energy of the IGBT per ampere and E_D is for the diode. E_I and E_D can be considered approximately as constants. They are determined by technologies, and different IGBTs and diodes have different E_I and E_D values. E_I and E_D should, therefore, be derived by measurements during experiments.

As mentioned in equation (9), the output current can be considered a sinusoidal waveform and the switching loss occurs every PWM period for continuous PWM schemes. Therefore, depending on the switching frequency f_{sw}, the switching loss of one device is represented in the following equation (17):

$$P_{sw} = \frac{1}{2\pi}\int_0^{\pi} (E_I + E_D)\ i\ f_{sw} d\varphi = \frac{(E_I + E_D) f_{sw} I_{peak}}{\pi} \quad (17)$$

From the equation (17), it can be noted that the switching losses are a linear function of current, and directly proportional to the switching frequency.

7.3 Thermal impedance

In practical operations, the power loss P_D is cyclic, and therefore the transient impedance needs to be considered. The thermal impedance is typically represented by an RC equivalent circuit, as shown in Figure 26. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature, and thus permits a heavier loading of the CIPOS™ Mini. Figure 27 and Figure 28 show junction-to-case thermal impedance curves of power devices. The thermal resistance goes into saturation after about ten seconds.

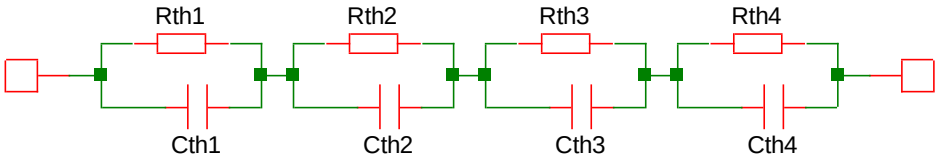


Figure 26 Thermal impedance RC equivalent circuit

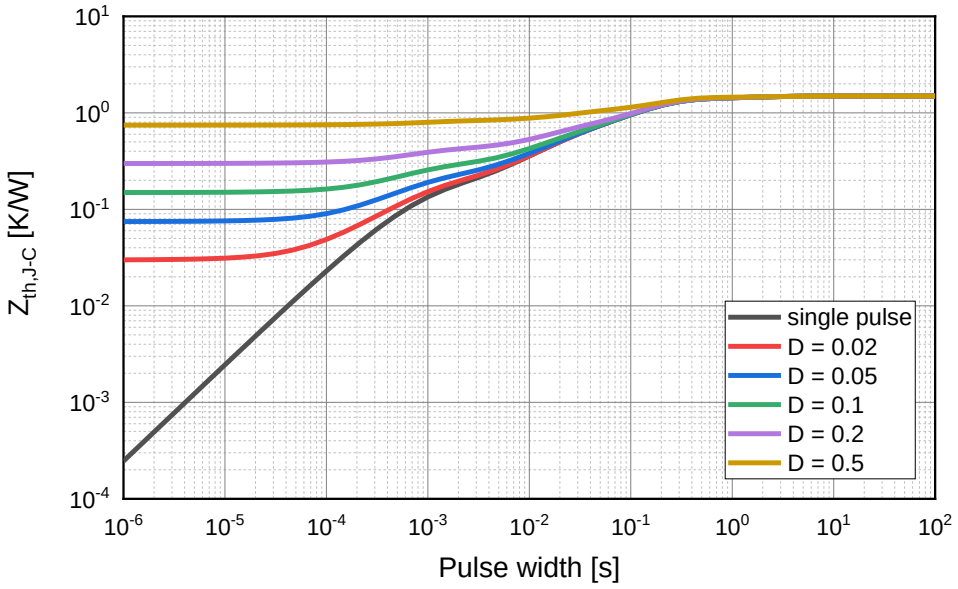


Figure 27 Thermal impedance curves (IM535-U6D/U6DS, IGBT)

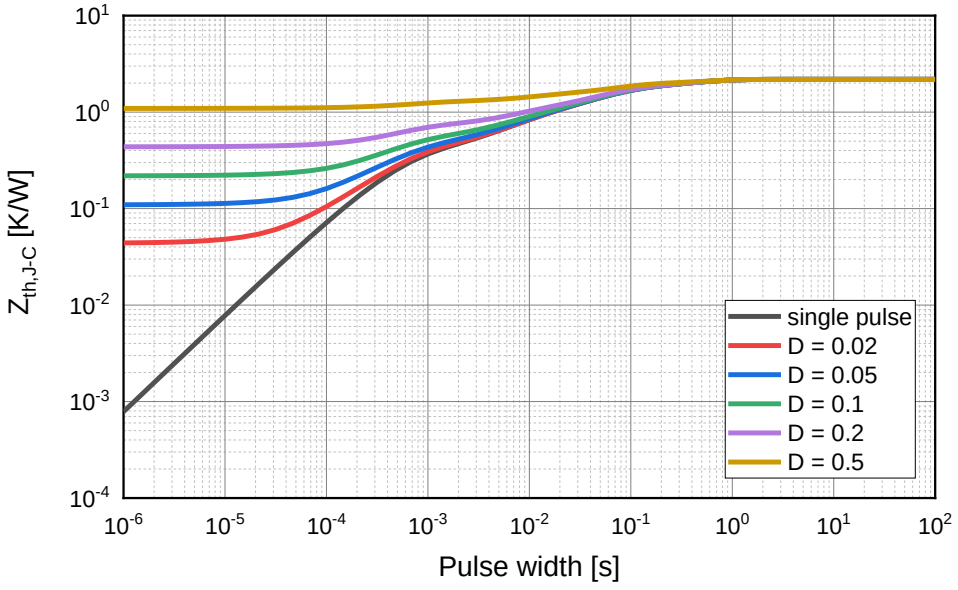


Figure 28 Thermal impedance curves (IM535-U6D/U6DS, diode)

7.4 Example of temperature rise consideration and calculation

The on-line simulation tool for CIPOS™ Mini IPMs is available on Infineon's product homepage. It allows for calculation of power losses and estimated temperature. Figure 29 shows an example of IM535-U6D with V_{PN} = 300 V, V_{DD} = 15 V, f_{SW} = 8 kHz, f_{OUT} = 60 Hz, PF = 0.8, V_{motor} = 147 V, I_{motor} = 14 A, T_A = 35°C, $R_{th.sa}$ = 0.6 K/W and $R_{th.TIM}$ = 0.1 K/W.

Inverter Losses

	Part Name	Total	Efficiency	Output Power	Avg. Case Temp.
All Switches	IM535-U6D	60.14 W			
All Diodes	IM535-U6D	16.37 W			
Inverter	IM535-U6D	76.51 W	97.32 %	2852 W	88.66 °C

Phase A High Side Device Losses and Junction Temperatures

	Part Name	EOn	EOff	Total Switching	Cond.	Avg. Junction Temp.	Max Junction Temp.
Switch	IM535-U6D	2.04 W	1.06 W	3.10 W	6.93 W	103.6 °C	108.1 °C
Diode	IM535-U6D		0.41 W	0.41 W	2.33 W	94.63 °C	97.92 °C

Phase A Low Side Device Losses and Junction Temperatures

	Part Name	EOn	EOff	Total Switching	Cond.	Avg. Junction Temp.	Max Junction Temp.
Switch	IM535-U6D	2.03 W	1.05 W	3.08 W	6.91 W	103.7 °C	108.1 °C
Diode	IM535-U6D		0.41 W	0.42 W	2.31 W	94.62 °C	97.90 °C

Figure 29 Power losses and junction temperature at given conditions

7.5 Heat sink selection guide

7.5.1 Required heat sink performance

If the power losses, the junction-to-case thermal resistance values, and the maximum ambient temperature are known, the required thermal resistance of the heat sink and the thermal interface material can be calculated based on Figure 26 from:

$$T_{\mathrm{J\_IGBT,max}} = T_{\mathrm{A,max}} + \sum_k (P_{\mathrm{D\_IGBT,k}} + P_{\mathrm{D\_diode,k}}) \cdot R_{\mathrm{th,HS-}A} + \sum_k (P_{\mathrm{D\_IGBT,k}} + P_{\mathrm{D\_diode,k}}) \cdot R_{\mathrm{th,C-HS}} + \mathrm{Max}(P_{\mathrm{D\_IGBT,k}} \cdot R_{\mathrm{th,J\text{-}C\_IGBT,k}}) \quad (18)$$

Where $P_{D,k}$ and $R_{th,J\text{-}C,k}$ are power loss and thermal resistance respectively of each power switch inside the IPM.

The equation (18) assumes that the IGBTs run hotter than diodes which is valid for motor drive applications for home appliances. The equation needs to be modified for operating modes such as braking or rectification where the diodes run hotter than the IGBTs.

For 3-phase bridges, it can be assumed that all power switches dissipate the same power and all have the same $R_{th,J\text{-}C}$. This leads to the required thermal resistance from case to ambient:

$$R_{\mathrm{th,C-}A} = R_{\mathrm{th,C-HS}} + R_{\mathrm{th,HS-}A} = \frac{T_{\mathrm{J,max}} - P_{\mathrm{D\_IGBT}} \cdot R_{\mathrm{th,J\text{-}C\_IGBT}} - T_{\mathrm{A,max}}}{\sum P_{\mathrm{D}}} \quad (19)$$

For example, the IGBT and diode of the IM535-U6D dissipate 10 W and 3 W maximum each; the maximum ambient temperature is 50°C, the maximum junction temperature is 150°C, and the R_{th,JC_IGBT} is 1.5 K/W. In this case, the required thermal resistance from case to ambient becomes:

$$R_{th,C-A} \leq \frac{150^oC - 10\,W \times 1.5\,K/W - 50^oC}{6 \times 13\,W} = 1.1\ \mathrm{K/W}$$

If the heat sink temperature is limited to 100°C, an even lower thermal resistance is required:

$$R_{th,C-A} \leq \frac{100^oC - 50^oC}{6 \times 13\,W} = 0.64\,K/W$$

Smaller heat sinks with higher thermal resistances may be acceptable if the maximum power is only required for a short time (below the time constant of the thermal resistance and the thermal capacitance). However, this requires a detailed analysis of the transient power and temperature profiles. The larger the heat sink and its thermal capacitance, the longer it takes to heat up the heat sink.

7.5.2 Heat sink characteristics

Heat sinks are characterized by three parameters:

- Heat transfer from the power source to the heat sink
- Heat transfer within the heat sink (to all surfaces of the heat sink)
- Heat transfer from heat sink surfaces to ambient

7.5.2.1 Heat transfer from heat source to heat sink

In the case of IPM products, the heat source is the junction of power devices, as shown in Figure 24. The thermal path from junction to case is determined when the appropriate IPM product is selected for the target application. There are two factors to be considered for providing good thermal contact between the case and heat sink:

- **Flatness of the contact area**
  Due to unevenness of surfaces, a thermal interface material has to be applied between the case and heat sink. However, such materials have a rather low thermal conductivity (<10 K/W). Therefore, the material should be as thin as possible. On the other hand, it needs to fill out the space between the case and heat sink. Therefore, the heat sink should be as even as possible. In addition, the particle size of the interface material must conform to the roughness of the module and the heat sink surfaces. Particles that are too large will unnecessarily increase the thickness of the interface layer, thereby increasing the thermal resistance. Particles that are too small will not provide a good contact between the two surfaces, and lead to higher thermal resistance as well.
- **Mounting pressure**
  Higher the mounting pressure, the better the interface material disperses, and excessive interface material is pressed out. This creates a thinner interface layer with lower thermal resistance. Please refer to Table 18 for guideline on mounting torque.

7.5.2.2 Heat transfer within the heat sink

The heat transfer within the heat sink is mainly determined by the:

- **Heat sink material**
  The material needs to be a good thermal conductor. Most heat sinks are made of aluminum (λ ≈ 200 W/ (m*K)). Copper is heavier and more expensive, but also nearly twice as efficient (λ ≈ 400 W/ (m*K))
- **Fin thickness**
  If the fins are too thin, thermal resistance from the heat source to fin is too high and the efficiency of the fin decreases. Therefore, it does not make sense to make the fins thinner just to have more fins to increase the surface area

7.5.2.3 Heat transfer from heat sink surface to ambient

Heat is transferred to the ambient mainly through convection. The corresponding thermal resistance can be defined as:

$$R_{th,conv} = \frac{1}{\alpha \cdot A} \quad (20)$$

Where α is the heat transfer coefficient and A is the surface area.

There are two important parameters to consider:

- **Surface area:** Heat sinks require a huge surface area to easily transfer the heat to the ambient. However, as the heat source is assumed to be concentrated at one point and not uniformly distributed, the total thermal resistance of a heat sink does not change linearly with length. Also, increasing the surface area by increasing the number of fins does not necessarily reduce the thermal resistance as discussed in Section 7.5.2.2
- **Heat transfer coefficient (aerodynamics):** This coefficient depends heavily on the air flow velocity, as shown in Figure 30. It is natural convection if there is no externally induced air flow, but otherwise it is forced convection. Heat sinks with very small fin spacing do not enable a good air flow. If a fan is used, the fin gap can be smaller than with natural convection as the fan forces the air through the space between the fins

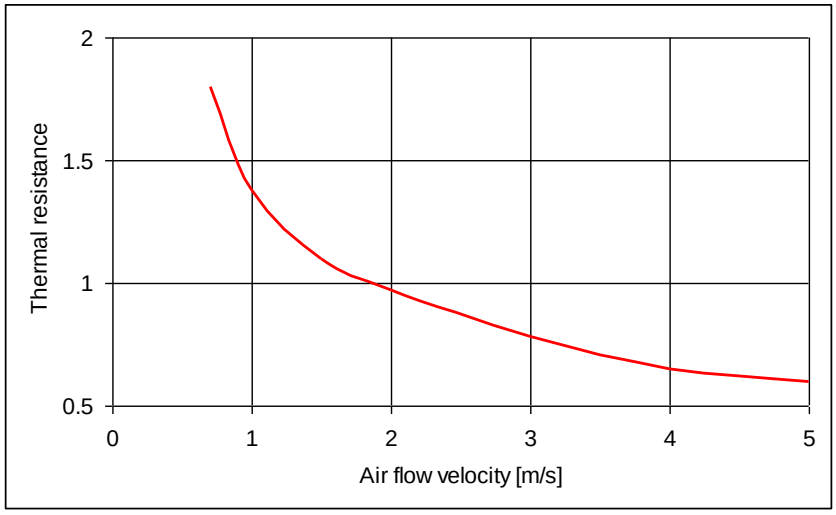


Figure 30 Thermal resistance as a function of the air flow velocity

Furthermore, in the case of natural convection, the heat sink efficiency depends on the temperature difference between the heat sink and the ambient (i.e. on the dissipated power). Some manufacturers, such as Aavid Thermalloy, provide a correction table which helps users calculate the thermal resistance depending on the temperature difference. Figure 31 shows the heat sink efficiency degradation for natural convection as provided in [6]. Please note that the thermal resistance is 25% higher at 30 K than at 75 K.

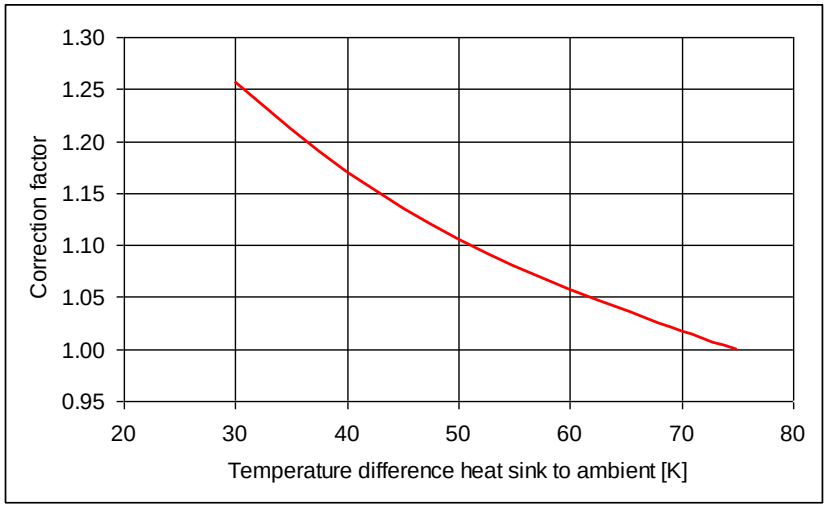


Figure 31 Correction factors for temperature

The positioning of the heat sink also plays an important role for aerodynamics. In the case of natural convection, the best mounting is with vertical fins as the heated air tends to move upwards due to buoyancy. It should be ensured that there are no significant obstructions impeding the air flow.

Radiation occurs as well, supporting the heat transfer from the heat sink to the ambient. To increase the radiated heat, you can use anodized heat sinks with a black surface. This decreases the thermal resistance of the heat sink only by a few percent in the case of natural convection. Radiated heat is negligible with forced convection. Hence, black heat sinks can be used if a fan is not used with the heat sink.

The discussion in this section clearly shows that there cannot be one single thermal resistance value assigned to a certain heat sink.

7.5.3 Selecting a heat sink

Unfortunately, there are no straightforward formulas for selecting heat sinks. Finding an appropriate heat sink includes an iterative process of selecting and testing. To get a first rough estimation of the required volume of the heat sink, start with the estimated volumetric thermal resistances, as listed in Table 17 (taken from [7]). This table provides only an initial overview as the actual resistance may vary depending on many parameters such as actual dimensions, type, orientation, and so on.

Table 17 Volumetric thermal resistance

Flow conditions [m/s]	Volumetric resistance [cm^3 °C/W]
Natural convection	500 ~ 800
1.0	150 ~ 250
2.5	80 ~ 150
5.0	50 ~ 80

The volume of a heat sink roughly needs to be quadrupled to cut its thermal resistance in half. This gives an idea whether natural convection is sufficient for the available space, or if forced convection is required.

To find an optimized heat sink for an application, contact heat sink manufacturers or consultants. Further overview and references can be found in [7].

When contacting heat sink manufacturers for a suitable heat sink, find out the conditions under which the stated thermal resistance values are valid. They might be valid either for a point source or for a heat source that

is evenly distributed over the entire base area of the heat sink. Also, ensure that the fin spacing is optimized for the corresponding airflow conditions.

8 Heat sink mounting and handling guidelines

8.1 Heat sink mounting

8.1.1 General guidelines

Adequate heat sinking capability of the CIPOS™ Mini can only be achieved if it is suitably mounted. It is fundamental to meet the electrical and thermal performance requirements of the module. The following general points related to the heat sink should be observed when mounting the CIPOS™ Mini on a heat sink:

- The screw holes should be countersunk
- There should be no unevenness or scratches on the heat sink
- The surface of the module should be completely in contact with the heat sink
- There should be no oxidation, stains, or burrs on the surface of the heat sink

To improve thermal conductivity, silicone grease must be applied to the contact surface between the CIPOS™ Mini and heat sink. An even layer of grease with a thickness of 100 µm should be spread over the CIPOS™ Mini substrate surface. Non-planar surfaces of the heat sink may require a thicker layer of grease. Please refer to the specifications of the heat sink manufacturer. It is important to ensure that the heat sink covers the entire back side of the module. If the IPM does not have a good contact with the heat sink, its functional behavior may change.

To prevent poor heat dissipation due to warping of the substrate, the mounting screws should be tightened gradually while maintaining a left/right balance in the pressure applied.

The design of the application PCB must ensure that the plane of the back side of the module and that of the heat sink are parallel to each other. This ensures minimal package tension and optimal contact between the module and the heat sink. Please refer to the mechanical specifications of the module given in the datasheets.

Good engineering requires that the function and thermal conditions be checked through detailed measurements. Using a final application inverter system that is assembled with the final production process is the best way to proceed to achieve high-quality applications.

8.1.1.1 Recommended tightening torque

As listed in Table 18, the maximum tightening torque of M3 screws is specified as 0.78 N·m. The screw holes must be centered on the screw openings of the mold compound so that the screws do not come in contact with the mold compound. If an insulating sheet is used, the sheet must be larger than the CIPOS™ Mini and should be aligned accurately when attached. It is important to ensure that no air is enclosed within the insulating sheet. Generally speaking, insulating sheets are used in the following cases:

- When the ability to withstand primary and secondary voltages is necessary to achieve the required safety standards against a hazardous situation. An alternative solution is to use a convex heat sink instead of a flat heat sink and insulating sheet
- When measuring the module, to reduce radiated noise or eliminate other signal-related problems

Table 18 Mechanical characteristics and ratings

Item	Condition	Package type	Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw: M3	DCB	0.49	-	0.78	N·m
		Full-pack	0.59	0.69	0.78	
Device flatness	(Note Figure 32)		-50	-	+100	µm
Heat sink flatness	(Note Figure 33)		0	-	+100	µm
Weight		DCB	-	6.58	-	g
		Full-pack	-	6.15	-	

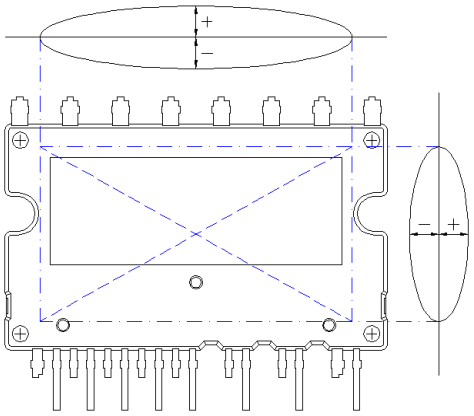


Figure 32 Device flatness measurement position

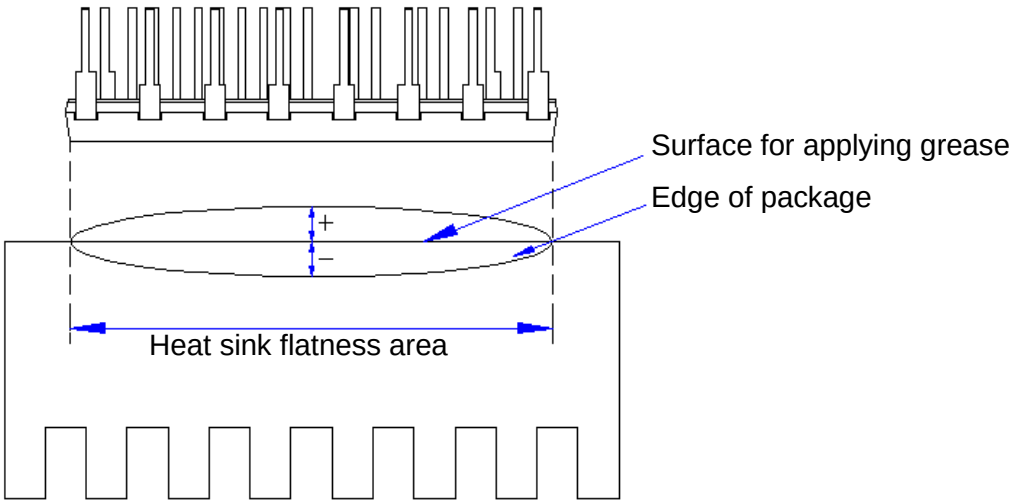


Figure 33 Heat sink flatness measurement position

8.1.1.2 Screw tightening to heat sink

Tightening of the screws is the main process in attaching a module to the heat sink. It is assumed that an interface pad that extends to the edge of the module and is aligned to the fixing holes is attached to the heat sink surface. It is recommended that M3 fixing screws be used in conjunction with a spring washer and a plain washer. The spring washer must be assembled between the plain washer and the screw head. The screw torque must be monitored by the fixing tool.

Tightening process:

1. Align the module with the fixing holes.
2. Insert screw A with washers to touch only the position (pre-screwing).
3. Insert screw B with washers (pre-screwing).
4. Tighten screw A to final torque.
5. Tighten screw B to final torque.

Note: The pre-screwing torque is set to 20~30% of maximum torque rating.

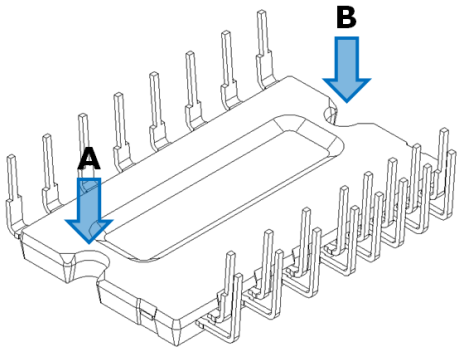


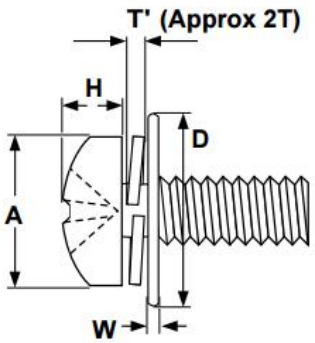
Figure 34 Recommended screw-tightening process: pre-screwing A → B, final screwing A → B

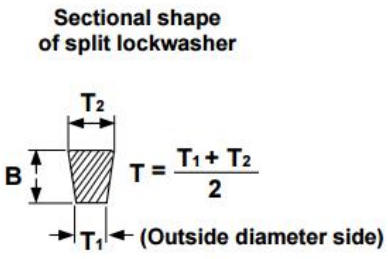
8.1.1.3 Mounting the screw

M3 SEMS screw (JIS B1256/JIS B1188) is recommended based on data listed in Table 19.

Table 19 Recommended screw specification (typical)

Screw dimensions				Flat washer		Spring washer	
Size	Thread pitch	A	H	D	W	D1	B x T
		Head diameter	Head height	Outer diameter	Thickness	Outside diameter	
M3	0.5	5.2	2.0	7.8	0.58	5	1.1 x 0.7





8.1.2 Recommended heat sink shape and system mechanical structure

A shock or vibration through the PCB or heat sink could lead to cracking of the package mounted on the heat sink. To avoid a broken or cracked package and to ensure that the PCB or heat sink can endure shock or vibration, a heat sink shape is recommended as shown in Figure 35. The heat sink must be fixed to the PCB with screws or eyelets. During the mass production stage, the process sequence for system assembly in terms of device soldering on PCB, heat sink mounting, casing, and so on should be considered to prevent mechanical stress on the device pins, package mold compound, heat sink, system enclosure, and other parts.

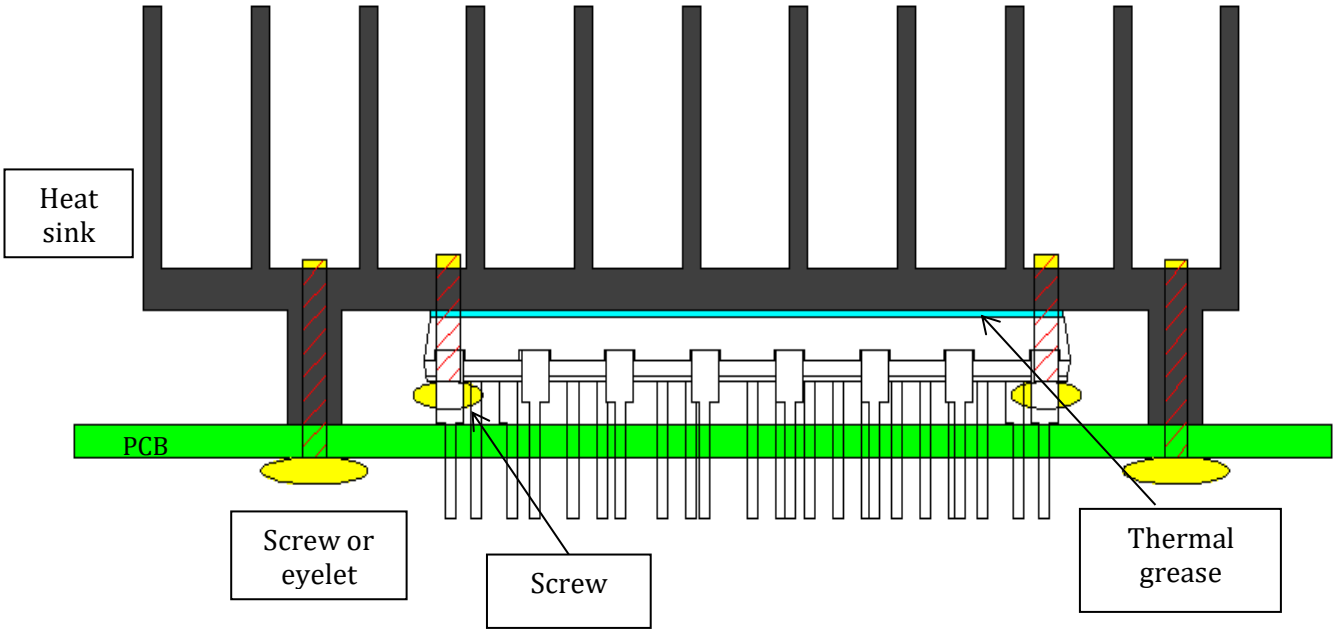


Figure 35 Recommended heat sink shape

8.2 Handling guidelines

While installing a module to the heat sink, an excessive uneven tightening force might apply stress on the inside chips that could lead to breakage or degradation of the device. An example of recommended fastening order is shown in Figure 34.

Over-torque should be avoided when mounting the screws. Excessive mounting torque may damage the module hole as well as the screw and the heat sink.

- One-sided tightening stress must also be avoided as uneven mounting can damage the module hole
- A torque wrench must be used to tighten to the specified torque rating. Exceeding the maximum torque limit might damage or degrade the module

For effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance.

The thermal interface material must be applied properly over the contact surface between the module and the heat sink. It also protects the contact surface from corrosion. The thermal interface material should be of stable quality; possessing long-term endurance within a wide operating temperature range.

The contact surface between the module and the heat sink must be dirt free. All equipment used for handling or mounting the CIPOS™ Mini IPMs must comply with the relevant ESD standards. This includes e.g. transportation, storage, and assembly. This is because the module is an ESD-sensitive device and might get damaged in case of ESD shocks.

Do not shake or handle by gripping the heat sink alone. This might put stress on the PCB and could break or crack the package.

8.3 Storage guidelines

8.3.1 Recommended storage conditions

Temperature: 5 ~ 35℃

Relative humidity: 45 ~ 75%

Rapid temperature changes can cause moisture condensation on the stored CIPOS™ Mini, resulting in lead oxidation or corrosion. This degrades its solderability. Therefore:

- Exposing the CIPOS™ Mini family to moisture or direct sunlight must be avoided. Particular care must be taken during periods of rain or snow
- Storage areas with minimal temperature fluctuations must be used

The CIPOS™ Mini products must not be exposed to corrosive gasses or dusty conditions. While in storage, it must be ensured that excessive external force or load is not applied on them.

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Revision history

Document version	Date of release	Description of changes
V 1.0	20-09-2022	Initial release

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Edition 2022-09-20

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN2022-06

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