TABLE I

AREA AND WIRE LENGTH COMPARISON ON MCNC BENCHMARK WITH VARIOUS ALGORITHMS WHEN α=0.5 AND β=0.5

Performance measures	apte		xerox		hp		ami33		ami49	
	Area(mm^2)	WL(mm)	Area(mm^2)	WL(mm)	Area(mm^2)	WL(mm)	Area(mm^2)	WL(mm)	Area(mm^2)	WL(mm)
MCNC benchmark										
RL(ICCD2020)	47.08	403	20.42	633	**9.21**	195	1.24	69	38.65	1724
BCSA	48.05	474.62	20.42	385.21	9.25	157.07	1.23	53.55	38.1	705.20
ISSAA	48.47	408.47	20.42	387.64	9.40	153.05	1.26	49.28	37.76	824.49
VOAS	47.05	246	20.45	**379.6**	9.46	149.8	**1.22**	59.5	37.82	667
Fast-SA	50.3	541.43	20.41	421.15	9.6	214.35	1.29	59.96	40.36	816.51
DPSO	47.31	263	**20.2**	477	9.5	136	1.28	69	38.8	880
ESA	49.38	205.54	20.54	621.05	9.36	510.24	1.25	108.5	**36.73**	1371
Genetic Algorithm	**46.9**	**191**	20.2	500	9.85	**68.3**	1.29	**46.2**	39.5	912
O-tree	51.9	321	20.4	381	9.5	153	1.28	51	39.6	689
Enhanced O-tree	52.0	321	20.4	381	9.4	152	1.30	52	39.9	703
TCG	48.5	378	20.4	385	9.5	152	1.24	50	38.2	**663**
CS	48.5	380	20.4	381	9.6	149	1.25	48.1	38.2	690

WL wire length

Shunmugathammal, M., Christopher Columbus, C. & Anand, S. A Novel B*tree Crossover-Based Simulated Annealing Algorithm for Combinatorial Optimization in VLSI Fixed-Outline Floorplans. Circuits Syst Signal Process 39, 900–918 (2020). https://doi.org/10.1007/s00034-019-01054-9

TABLE II

AREA AND WIRE LENGTH COMPARISON ON GCRS BENCHMARK WITH VARIOUS ALGORITHMS. BETTER RESULTS ARE EMPHASIZED IN BOLD.

Performance measures	n100			n200			n300		
	Area($\times 10^5$)	WL($\times 10^5$)	RT(s)	Area($\times 10^5$)	WL($\times 10^5$)	RT(s)	Area($\times 10^5$)	WL($\times 10^5$)	RT(s)
GSRC benchmark									
RL	**1.95**	1.55	**389.4**	2.15	3.48	**784.9**	3.40	**5.25**	3766.9
SA	1.97	**1.54**	396.2	**2.01**	**3.34**	1101.9	**3.29**	5.44	**2062.3**

WL wire length, *RT* run time

Z. He et al., "Learn to Floorplan through Acquisition of Effective Local Search Heuristics," 2020 IEEE 38th International Conference on Computer Design (ICCD), 2020, pp. 324-331, doi: 10.1109/ICCD50377.2020.00061.